(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 June 2017 (29.06.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/112219 A1

(51) International Patent Classification:
G01R 31/317 (2006.01) *G01R 31/3193* (2006.01)
G01R 31/3185 (2006.01) *G11C 29/56* (2006.01)

(21) International Application Number:
PCT/US2016/063122

(22) International Filing Date:
21 November 2016 (21.11.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/998,200 24 December 2015 (24.12.2015) US

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, CA 95054 (US).

(72) Inventors: **PAPPU, Lakshminarayana**; 1480 Leonard Ct, Folsom, California 95630 (US). **ADLER, Robert P.**; 2668 Forbes Ave., Santa Clara, California 95051 (US). **BHATT, Suketu U.**; 1483 Lewis Way, Folsom, California 95630 (US). **DE GRUIJL, Robert**; 3514 25th St., San Francisco, California 94110 (US). **YEEM, Kah Meng**; 110 Camberwell Way, Folsom, California 95630 (US).

(74) Agent: **NICHOLSON, JR., Wesley, E.**; 5 Centerpointe Dr. Suite 400, Lake Oswego, Oregon 97035 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: CHIP FABRIC INTERCONNECT QUALITY ON SILICON

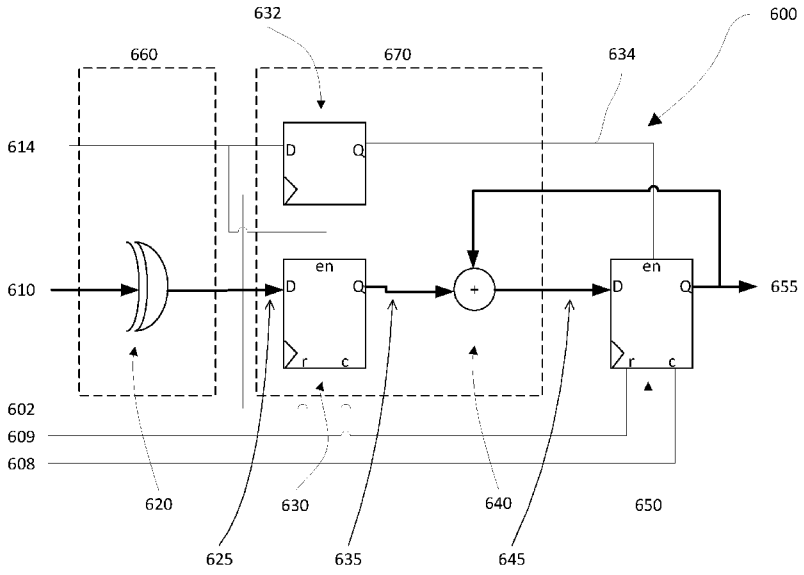

Fig. 9

(57) Abstract: Described is a signature accumulator with a first set of logic devices, a second set of logic devices, and a memory device. The first set of logic devices includes compaction logic that couples an N-bit input bus to a K-bit first intermediate bus. The second set of logic devices includes commutative arithmetic operation logic that couples both the K-bit first intermediate bus and a K-bit signature bus to a K-bit second intermediate bus. The memory storage device includes a storage element that couples the K-bit second intermediate bus to the K-bit signature bus. The K-bit signature bus is also coupled to a valid-data input signal path.

WO 2017/112219 A1

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

CHIP FABRIC INTERCONNECT QUALITY ON SILICON

CLAIM FOR PRIORITY

[0001] This application claims priority to U.S. Non-Provisional Patent Application Serial No. 14/998,200, filed on 24 December 2015, and entitled "CHIP FABRIC INTERCONNECT QUALITY ON SILICON", and which is incorporated by reference in entirety.

BACKGROUND

[0002] Silicon components are typically tested after being manufactured in order to ensure functionality and quality. Testing of silicon components in production lines is sometimes called HVM (High-Volume Manufacturing) testing. One type of HVM testing, "sort" testing, may be performed on components that are unpackaged and still exist as die on a manufactured silicon wafer. Another type of HVM testing, "class" testing, may be performed on components that exist as die that have been cut from a manufactured silicon wafer and subsequently packaged for potential sale to customers.

[0003] HVM testers—i.e., the machines used to perform HVM tests—are complex and expensive. As a result, the amount of time required to test a component on an HVM tester may contribute significantly to the cost required to manufacture the component. There is accordingly a tension between testing components to ensure their functionality and quality, and limiting the time required to perform the testing on HVM testers.

[0004] A variety of types of HVM tests may be performed on a component at sort testing, at class testing, or both. These tests may use a variety of DFT (Design for Test) and DFM (Design for Manufacturability) features of the component which are designed to maximize the comprehensiveness of the tests while minimizing the time required to perform the tests.

[0005] For example, a particular circuit or feature of the component such as a Random-Access Memory (RAM) might be designed to include Built-In Self Test (BIST) circuitry which may be activated to perform relatively rapid and/or comprehensive testing of the circuit or feature. As another example, for components with substantial portions implemented through a mix of combinational logic and sequential logic, the elementary units of the sequential logic (e.g. shift registers) may be designed to accommodate "scan" inputs and "scan" outputs, which are auxiliary

inputs and outputs of the shift registers. The scan output of one register may then be connected to the scan input of another register, and so on, and one or more "scan chains" of registers may thereby be formed on the component. Once formed, an HVM test may load the scan chains with an arbitrary sequence of values, then apply one clock cycle to the shift registers. Such scan tests will in turn exercise some portion of the combinational logic.

[0006] Another type of test that may be applied to a component are functional tests. Under a functional test, the component may be subjected to stimulus of the sort it would experience in actual working conditions. The response of the component to the stimulus may then be compared to the expected response of the component to that stimulus. Functional tests may help to improve test coverage achieved by DFT and DFM tests such as BIST testing or scan testing. In other words, if the suite of DFT-based tests and DFM-based tests do not cover certain portions of the design, then functional tests may be written to cover those previously-uncovered design portions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure. However, while the drawings are to aid in explanation and understanding, they are only an aid, and should not be taken to limit the disclosure to the specific embodiments depicted therein.

[0008] **Fig. 1** illustrates a block diagram of a signature accumulator, according to some embodiments of the disclosure.

[0009] **Fig. 2** illustrates a diagram of a signature accumulator, according to some embodiments of the disclosure.

[0010] **Fig. 3** illustrates a diagram of a data compactor, according to some embodiments of the disclosure.

[0011] **Fig. 4** illustrates a first fabric incorporating signature accumulators, according to some embodiments of the disclosure.

[0012] **Fig. 5** illustrates a second fabric incorporating signature accumulators, according to some embodiments of the disclosure.

[0013] **Fig. 6** illustrates a block diagram of a signature accumulator, according to some embodiments of the disclosure.

[0014] **Fig. 7** illustrates a block diagram of a signature accumulator, according to some embodiments of the disclosure.

[0015] **Fig. 8** illustrates a block diagram of a signature accumulator, according to some embodiments of the disclosure.

[0016] **Fig. 9** illustrates a block diagram of a signature accumulator, according to some embodiments of the disclosure.

[0017] **Fig. 10** illustrates a system incorporating a component having a signature accumulator, according to some embodiments of the disclosure.

[0018] **Fig. 11** illustrates a method of accumulating a signature, according to some embodiments of the disclosure.

[0019] **Fig. 12** illustrates a method of accumulating a signature, according to some embodiments of the disclosure.

DETAILED DESCRIPTION

[0020] HVM tests rely heavily upon the deterministic response of a component to a stimulus applied to it. Components are typically deemed to fail if they do not respond in the manner that a particular HVM test indicates that they should respond—and, crucially, at the time that the HVM test indicates that they should respond.

[0021] Meanwhile, for flexibility in view of factors such as cost and development time, component designs have increasingly come to embrace SoC (System-on-a-Chip) design methodologies. Some SoC components may be designed to incorporate IP (Intellectual Property) cores, as well as fabrics interconnecting the IP cores, for purposes of flexibility. For some components, on-die fabrics including interconnect between various ports may extend over a very large portion of the physical component, and may be subject to a correspondingly large portion of the potential defects or faults of the component. However, SoC design methodologies may be prone to nondeterministic performance on HVM testers. Some IP cores on a component may use one clock while other IP cores on the component use another clock, for example, and it may be difficult to establish those clocks in an HVM test environment in such a way that would lead to deterministic behavior.

[0022] In order to flexibly accommodate SoC design methodologies, signature accumulators can sample values along various datapaths within a design. These signature accumulators can accumulate a signature that is a function of the entire

history of the traffic on the datapath, and that signature can be independent of the order in which the traffic has been sent on the datapath.

[0023] As a result, functional HVM test patterns may be used to subject a component having such a signature accumulator to very high levels of traffic, and the signature accumulator will be able to indicate proper functionality for the design even if nondeterministic behavior on the HVM tester results in the traffic passing through the datapath in a nondeterministic order. Functional HVM tests may thereby exercise and cover very extensive portions of the potential "faults" within the component. Those faults may be particularly valuable to cover, since they may correspond to faults that are most easily exercised in normal operation.

[0024] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent to one skilled in the art, however, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0025] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate a greater number of constituent signal paths, and/or have arrows at one or more ends, to indicate a direction of information flow. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0026] Throughout the specification, and in the claims, the term "connected" means a direct electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" or "module" may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" may refer to at least one current signal,

voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0027] The terms "substantially," "close," "approximately," "near," and "about" generally refer to being within +/- 10% of a target value. Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

[0028] For the purposes of the present disclosure, the phrases "A and/or B" and "A or B" mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

[0029] In addition, the various elements of combinatorial logic and sequential logic discussed in the present disclosure may pertain both to physical structures (such as AND gates, OR gates, or XOR gates), or to synthesized or otherwise optimized collections of devices implementing the logical structures that are Boolean equivalents of the logic under discussion.

[0030] **Fig. 1** illustrates a signature accumulator 100, according to some embodiments of the disclosure. Signature accumulator 100 has several inputs, including a clock 102, an enable 104, an N-bit input data 110, and a valid data indicator 114. As will be discussed further below, input data 110 may be connected to a datapath on a component, such as a datapath on a sideband fabric or a primary fabric.

[0031] Enable 104 is set to '1' when signature accumulator 100 is enabled (which may be due to a "global trigger" sent to many signature accumulators on the same component). Valid data indicator 114 is set to '1' when N-bit input data 110 is deemed to be valid data that signature accumulator 100 should account for (and in particular when input data 110 does not have any 'X' or indeterminate data).

[0032] Beyond input data 110 is an N-bit validated input data 115. In **Fig. 1**, the progress of data being inputted to signature accumulator 100 is made conditional upon both enable 104 and valid data indicator 114. Accordingly, when enable 104 and valid data indicator 114 are both set to '1,' the value on input data 110 is passed to validated input data 115; otherwise, the bits of validated input data 115 are set to '0.'

[0033] Validated input data 115 is then passed to a data compactor 120, which compacts N-bit validated input data 115 and passes the result to a K-bit first intermediate bus 135. In general, that compaction may take any form in which each of the K bits of first intermediate bus 135 is related by some Boolean function to one or more of the N bits of validated input data 115. Data compactor 120 may accordingly compact the N bits of validated input data 115 into the K bits of first intermediate bus 135 in a wide variety of ways. For example, data compactor 120 may set each of the K bits of first intermediate bus 135 to the evaluation of either an "OR" function or an "AND" function with respect to two or more of the N bits of validated input data 115. In other embodiments, data compactor 120 may set each of the K bits of first intermediate bus 135 to the evaluation of any Boolean function with respect to any of the N bits of validated input data 115.

[0034] In some embodiments, data compactor 120 may compact input data 115 using a tree of XOR logic. By way of example, **Fig. 3** illustrates a data compactor according to some embodiments of the disclosure. Data compactor 320 uses XOR tree logic to compact an N-bit input data 310 and pass the results to a K-bit first intermediate bus 335.

[0035] Data compactor 320 includes a number S of stages of XOR logic, beginning with stage 316 (i.e., stage 1 out of S), then proceeding to stage 317 (stage 2 out of S), and so on, to stage 318 (stage S out of S). More generally, in various embodiments, data compactor 320 may have an N-bit input, a K-bit output, and a number of stages S, where N, K, and S have the following relationship to each other:

$$N = K * 2^S$$

Accordingly, the ratio of N to K is a power of two.

[0036] In various embodiments, N could be 8, 16, 32, 64, or 128, and K could be chosen to require a suitably low amount of implementing logic. For a primary fabric, for example, N might be 64 or 128and K might be 16 whereas for a sideband fabric N might be 16 or 32 and K might be 16.

[0037] Each of stages 316-318 includes a number of two-input XOR gates in parallel. An advantage of using a tree of XOR logic is that for random input data, each bit of the K-bit output is as likely to have a '0' value as a '1' value. However, other embodiments of data compactor 320 may include either OR gates or AND gates instead of XOR gates, or may include logic implementing an output related to multiple inputs by any Boolean function. Moreover, while the number of stages S of

logic may be greater than one in many embodiments, some embodiments may have only one stage of logic. In addition, other embodiments of data compactor 320 may include two-input gates, three-input gates, or gates with any number of inputs. In such embodiments, N, K, and S have the following relationship to each other (where W indicates the number of inputs per gate):

$$N = K * W^S$$

[0038] Returning to **Fig. 1**, data compactor 120 may be similar to data compactor 320. In other words, data compactor 120 may in some embodiments use an XOR logic tree to compact the N bits of validated input data 115 to the K bits of first intermediate bus 135. The K bits of first intermediate bus 135 are then passed to a commutative arithmetic operator 140, along with a K-bit signature bus 155 (which this discussion will return to shortly). Commutative arithmetic operator 140 performs a commutative arithmetic operation between the value on first intermediate bus 135 and the value on signature bus 155. In some embodiments, the commutative arithmetic operation may be addition. In other embodiments, the operation may be multiplication, or any other commutative arithmetic operation. Commutative arithmetic operator 140 then sets a K-bit second intermediate bus 145 to the result of the commutative arithmetic operation.

[0039] Second intermediate bus 145 is then input to a memory device 150, which may include a flip-flop or register, and which incorporates a clock input connected to clock 102 and an output connected to K-bit signature bus 155. Upon a predetermined stimulus on clock 102 (such as a rising edge of clock 102), the value on second intermediate bus 145 is passed onto signature bus 155. Accordingly, signature bus 155 carries the previous value of second intermediate bus 145 (e.g., the value of second intermediate bus 145 at the end of the previous clock cycle). Signature bus 155 may then be passed to a register storage 160, which can capture and preserve a value on signature bus 155 for further use.

[0040] As such, either the N-bit data on input data 110 is passed to validated input data 115 (when enable 104 and valid data indicator 114 are both '1'), or '0' is placed on the bits of validated input data 115. Data compactor 120 then compacts the N bits of validated input data 115 onto the K bits of first intermediate bus 135. Commutative arithmetic operator 140 may then, for example, add the value on first intermediate bus 135 to the value on signature bus 155 (which is the value that was on second intermediate bus 145 at the end of the previous clock cycle), then output the

result onto second intermediate bus 145. Afterward, memory device 150 may capture the value on second intermediate bus 145 at the end of the current clock cycle and place the value on signature bus 155 on the next clock cycle. The value on signature bus 155 may then be captured by memory device 160.

[0041] Once all traffic has passed through the datapath, the value in memory device 160 may be read out during an HVM test (for example, by a Peripheral Component Interconnect (PCI) configuration register read, or other register read) to determine whether all expected transactions passed through the datapath. Since the addition operation (or other arithmetic operation) performed by commutative arithmetic operator 140 is commutative, after all traffic has passed through the datapath connected to input data 110, the value placed on signature bus 155 will be the same regardless of the order in which the traffic passed through the datapath. Actual silicon components may therefore be capable of passing this HVM test, even if the transactions have passed through the datapath in a different order than expected due to non-determinism in the HVM tester environment.

[0042] **Fig. 2** illustrates a diagram of another signature accumulator, according to some embodiments of the disclosure. A signature accumulator 200 has inputs including a clock 202, an enable 204, an enable override 205, an N-bit input data 210, a raw valid data indicator 212, and a raw valid data indicator override 213. Input data 210 may be connected to a datapath on a component, such as a datapath on a sideband fabric or a primary fabric.

[0043] Enable 204 is set to '1' when signature accumulator 200 is enabled (which may be due to a "global trigger" sent to many signature accumulators on the same component). Raw valid data indicator 212 is set to '1' when N-bit input data 210 is deemed to be valid data that signature accumulator 200 should account for (and in particular when input data 210 does not have any 'X' or indeterminate data). In signature accumulator 200, if both enable 204 and raw valid indicator 212 are set to '1,' then a valid data indicator 214 will be set to '1.' However, signature accumulator 200 includes two override inputs for use in causing alternate functionality, such as in a debug mode. Enable override 205, when set, will permit valid data indicator 214 to be set to '1' when enable 204 is not set to '1.' Similarly, raw valid data indicator override 213 will permit valid data indicator 214 to be set to '1' when raw valid data indicator 212 is not set to '1.'

[0044] Input data 210 is passed to data compactor 220. Data compactor 220 may be similar to data compactor 320 of **Fig. 3**. Accordingly, in some embodiments, data compactor 220 may use an XOR logic tree to compact the N bits of input data 210 and place the resulting value on a K-bit additional bus 225.

[0045] Additional bus 225 is then input to a memory device 230, which may include a flip-flop or register, and which incorporates a clock input connected to clock 202, an output connected to a K-bit first intermediate bus 235, and an enable input connected to valid data indicator 214. When valid data indicator 214 is '1,' and upon a predetermined stimulus on clock 202 (such as a rising edge of clock 202), the value on additional bus 225 at the end of the previous clock cycle may be passed onto first intermediate bus 235.

[0046] Meanwhile, alongside this data path within signature accumulator 200, valid data indicator 214 is also input to an additional memory device 232. Upon a predetermined stimulus on clock 202 (such as a rising edge of clock 202), the value on valid data indicator 214 at the end of the previous clock cycle may be passed onto a staged valid data indicator 233.

[0047] An advantage of the incorporation of memory device 230 and additional memory device 232 into signature accumulator 200 is that the extra stages of delay may assist signature accumulator 200 in meeting timing requirements. Signature accumulator 200 may accordingly be easier to incorporate into a component.

[0048] Returning to the data path within signature accumulator 200, the K bits of first intermediate bus 235 are then passed to a commutative arithmetic operator 240, along with a K-bit signature bus 255. Commutative arithmetic operator 240 performs a commutative arithmetic operation between the value on first intermediate bus 235 and the value on signature bus 255. The commutative arithmetic operation may be addition, or multiplication, or any other commutative arithmetic operation. Commutative arithmetic operator 240 then places the result of the commutative arithmetic operation on a K-bit second intermediate bus 245.

[0049] Second intermediate bus 245 is thereafter input to a memory device 250, which may include a flip-flop or register, and which incorporates a clock input connected to clock 202 and an output connected to a K-bit signature bus 255. Memory device 250 also includes an enable input connected to staged valid data indicator 233. Accordingly, when staged valid data indicator 233 is '1,' and upon a

predetermined stimulus on clock 202 (e.g. a rising edge), the value on second intermediate bus 245 is passed onto signature bus 255. Accordingly, signature bus 255 carries the previous value of second intermediate bus 245 (i.e., the value of second intermediate bus 245 at the end of the previous clock cycle). Signature bus 255 may then be passed to a register storage element to capture and preserve the value on signature bus 255 for further use (such as PCI configuration register reads or other register reads).

[0050] Finally, signature accumulator 200 has two clear-related inputs—a raw clear 206 and a clear override 207—as well an active-low reset-related input, asynchronous reset 209. An internal synchronous clear 209 will be set to '1' when either raw clear 206 or clear override 207 is set to '1.' Both memory device 230 and memory device 250 have synchronous clear inputs connected to synchronous clear 209, and asynchronous reset inputs connected to an inverted asynchronous reset 209. In various other embodiments, additional memory device 232 may also have a synchronous clear input connected to synchronous clear 209, an asynchronous reset input connected to the inverted asynchronous reset 209, or both.

[0051] As such, data compactor 220 compacts the N bits of input data 210 onto the K bits of additional bus 225. Then, either the K-bit data on additional bus 225 is latched by memory device 230 and placed upon first intermediate bus 235 on the next clock cycle (e.g., when enable 204 and raw valid data indicator 212 are both '1'), or memory device 230 retains and places the most recently latched value of additional bus 225 upon first intermediate bus 235. Commutative arithmetic operator 240 may then, for example, add the value on first intermediate bus 235 to the previous value on signature bus 255, and output the result onto second intermediate bus 245. Afterward, memory device 250 may capture the value on second intermediate bus 245 at the end of one clock cycle and place the value on signature bus 255 for the next clock cycle.

[0052] The value on signature bus 255 may then be captured by a memory device and, once all traffic has passed through the datapath, the value may be read out during an HVM test (by, e.g., a PCI configuration register read or other register read) to determine whether all expected transactions passed through the datapath. Since the addition operation (or other arithmetic operation) performed by commutative arithmetic operator 240 is commutative, after all traffic has passed through the datapath connected to input data 210, the value placed on signature bus 255 will be

the same regardless of the order in which the traffic passed through the datapath. Actual silicon components may therefore be capable of passing this HVM test, even if the transactions have passed through the datapath in a different order than expected due to non-determinism in the HVM tester environment.

[0053] **Fig. 4** illustrates a first fabric incorporating signature accumulators, according to some embodiments of the disclosure. A sideband fabric 400 includes a plurality of inbound datapaths 412 and a plurality of outbound datapaths 414, which are connected in pairs to a plurality of fabric ports 420. Each fabric port 420 includes ingress logic and egress logic. The internal sides of each fabric port 420 is connected to a separate ingress datapath bus 432 and an ingress control bus 433. Meanwhile, the internal sides of all of the fabric ports 420 are connected to an egress datapath bus 434 (which is shared among the ports) and an egress control bus 435.

[0054] Sideband fabric 400 also includes an outbound data multiplexer 440, an inbound ID multiplexer 450, and a set of routing arbitrators 460. Ingress control busses 433 exchange information about inbound traffic with routing arbiters 460 via the ingress control busses 433, which routing arbiters 460 use to maintain information about the traffic sent to the component. Based on that information, routing arbiters 460 select some of the bits of a transaction on one of the ingress datapath busses 432 to determine the destination fabric port 420 for the transaction. Routing arbiters 460 then select which of the ingress datapath busses 432 to connect to the egress datapath bus 434, and exchange information about outbound traffic with fabric ports 420 via the egress control busses 435.

[0055] In this context, each fabric port 420 includes an inbound signature accumulator 472 and an outbound signature accumulator 474. Inbound signature accumulators 472 are connected to the inbound datapaths 412, and outbound signature accumulators 474 are connected the outbound datapaths 414. In this configuration, signature accumulators may separately cover inbound traffic on the fabric and outbound traffic on the fabric for each port. Signature accumulators may be advantageously connected to individual ports of a fabric, such as individual ports of sideband fabric 400, when significant traffic is not expected to traverse centralized datapaths.

[0056] In various other embodiments, sideband fabric 400 may incorporate separate signature accumulators to cover each of a variety of traffic types passing through a particular datapath. For example, the inbound side of a fabric port 420 may

include a separate inbound signature accumulator 472 for posted transactions, or for non-posted transactions, or for completion transactions, or for any combination thereof. Similarly, the outbound side of a fabric port 420 may include a separate outbound signature accumulator 474 for posted transactions, or for non-posted transactions, or for completion transactions, or for any combination thereof.

[0057] **Fig. 5** illustrates a second fabric incorporating signature accumulators, according to some embodiments of the disclosure. A primary fabric 500 includes a first interconnect side 510, a second interconnect side 560, and a link arbiter 505. First interconnect side 510 and second interconnect side 560 have similar structures and interact with each other through link arbiter 505.

[0058] First interconnect side includes a plurality of first side agents 515, a first side inbound multiplexer 520, a first side inbound decode and queueing logic 525, a first side outbound multiplexer 530, and a first side outbound arbiter 535. Similarly, second interconnect side includes a plurality of second side agents 565, a second side inbound multiplexer 570, a second side inbound decode and queueing logic 575, a second side outbound multiplexer 580, and a second side outbound arbiter 585.

[0059] Each first side agent 515 transmits inbound traffic on a dedicated first side inbound agent datapath 516 to first side inbound multiplexer 520, and sends information regarding that agent's inbound traffic on a dedicated first side inbound agent control bus 517 to first side inbound decode and queueing logic 525. First side inbound multiplexer 520 routes data from one of the first side inbound agent datapaths 516 to a first side inbound datapath 521, which is an input to both first side outbound multiplexer 530 and second side outbound multiplexer 580. First side inbound multiplexer 520 also sends information to first side inbound decode and queueing logic 525, which in turn sends information to link arbiter 505 via a first side inbound request 526, which connects to a first request/grant bus 506.

[0060] Similarly, each second side agent 565 transmits inbound traffic on a dedicated second side inbound agent datapath 566 to second side inbound multiplexer 570, and sends information regarding that agent's inbound traffic on a dedicated second side inbound agent control bus 567 to second side inbound decode and queueing logic 575. Second side inbound multiplexer 570 routes data from one of the second side inbound agent datapaths 566 to a second side inbound datapath 571, which is an input to both first side outbound multiplexer 530 and second side

outbound multiplexer 580. Second side inbound multiplexer 570 also sends information to second side inbound decode and queueing logic 575, which in turn sends information to link arbiter 505 via a second side inbound request 576, which connects to a second request/grant bus 508.

[0061] Link arbiter 505 coordinates with first side outbound arbiter 535 to handle outbound traffic on first interconnect side 510 via first link-arbiter-to-outbound-arbiter bus 507 and first side outbound grant 536. First side outbound arbiter 535 then selects to route either first side inbound datapath 521 (from first side inbound multiplexer 520) or second side inbound datapath 571 (from second side inbound multiplexer 570) to a first side outbound agent datapath 531, through first side outbound multiplexer 530.

[0062] Similarly, link arbiter 505 coordinates with second side outbound arbiter 585 to handle outbound traffic on second interconnect side 560 via second link-arbiter-to-outbound-arbiter bus 509 and second side outbound grant 586. Second side outbound arbiter 585 then selects to route either first side inbound datapath 521 (from first side inbound multiplexer 520) or second side inbound datapath 571 (from second side inbound multiplexer 570) to a second side outbound agent datapath 581, through second side outbound multiplexer 580.

[0063] In this context, first interconnect side 510 includes a first side signature accumulator 540 connected to first side inbound datapath 521, and second interconnect side 560 includes a second side signature accumulator 590 connected to second side inbound datapath 571. In this embodiment, one signature accumulator may cover inbound traffic from all first side agents 515, and another signature accumulator may cover inbound traffic from all second side agents 565. Signature accumulators may be advantageously connected to shared ports of a fabric, such as shared ports of primary fabric 500, when most of the traffic is expected to traverse centralized datapaths.

[0064] In various embodiments, signature accumulators may be integrated with any type of interconnect fabric. Various types of interconnect fabric may include an Intel® IOSF fabric (On-Chip System Fabric), an AMBA fabric (Advanced Microcontroller Bus Architecture), SoC-it fabric, or CoreConnect fabric. (Intel is a trademark of Intel Corporation in the U.S. and/or other countries.)

[0065] Incorporating a signature accumulator such as those described above into an SoC-based component may have various advantages. Such signature

accumulators may advantageously permit functional HVM tests to cover potential defects or faults within the component when manufactured. If the signature accumulator is integrated within the design in such a way that the value on the signature bus is captured by registers accessible through PCI configuration register reads or other register reads targeting the component, then existing register access paths may be advantageously used to read out the value on the signature bus. In addition, register reads such as PCI configuration register reads may bypass much slower interfaces, such as register reads sent through a JTAG (Joint Test Action Group) test access port. Since the signature accumulators require a relatively small amount of logic, they can advantageously impose a relatively small cost on the component. At the same time, since the signature accumulators accommodate a measure of non-deterministic silicon performance on HVM testers, they can advantageously improve the reliability of functional HVM tests.

[0066] **Figs. 6-9** illustrate block diagrams of signature accumulators, according to some embodiments of the disclosure. With reference to **Fig. 6**, signature accumulator 600 has a number of input signal paths, including a clock 602, an input bus 610 having a number N of signal paths, and a valid-data input signal path 614. Signature accumulator 600 also includes a first intermediate bus 635 having a number K of signal paths, a second intermediate bus 645 having the number K of signal paths, and a signature bus 655 having the number K of signal paths.

[0067] Signature accumulator 600 incorporates a first set of logic devices 660 and a second set of logic devices 670. The first set of logic devices 660 includes compaction logic 620, which couples the N signal paths of input bus 610 to the K signal paths of first intermediate bus 645. The second set of logic devices 670 includes commutative arithmetic operation logic 640, which couples both the K signal paths of first intermediate bus 645 and the K signal paths of signature bus 655 to the K signal paths of second intermediate bus 645. Signature accumulator 600 also incorporates a memory device 650, which includes a storage element coupling the K signal paths of second intermediate bus 645 to the K signal paths of signature bus 655. Signature accumulator 600 also includes a synchronous clear signal 608 and an asynchronous reset signal 609, which are coupled to clear and reset inputs, respectively, of memory device 650.

[0068] In signature accumulator 600, signature bus 655 is coupled to the valid-data input signal path 614, through an enable input on memory device 650. In

other embodiments, signature bus 655 may be coupled to the valid-data input signal path 614 through first intermediate bus 645, such as by making the value on input bus 610 conditional upon the valid-data input signal path 614 being set to '1.' Signature accumulator 600 may also include a register memory having an input coupled to signature bus 655. For example, signature accumulator 600 may be incorporated within an interconnect fabric and coupled to one or more ports within the interconnect fabric by datapaths associated with the one or more ports. Such a register memory may be within an address space of associated with the one or more ports.

[0069] Signature accumulator 600 may thus include a first logic, a second logic, and a storage unit. The first logic may have an input coupled to input bus 610 and an output coupled to first intermediate bus 635, for which the first logic is operable to perform a compaction operation on the bits of the input bus. The second logic may have a first input coupled to first intermediate bus 635, a second input coupled to signature bus 655, and an output coupled to second intermediate bus 645, for which the second logic is operable to perform a commutative arithmetic operation between first intermediate bus 635 and signature bus 655. The storage unit may have an input coupled to second intermediate bus 645 and an output coupled to signature bus 655, for which the storage unit includes memory devices operable to store the K bits of data on second intermediate bus 645.

[0070] **Fig. 8** includes structures substantially similar to those in **Fig. 6**, but also -includes an additional bus 625 having a number K of signal paths. Furthermore, the second set of logic devices 670 includes an additional memory device 632 and another additional memory device 630. Memory device 632 has a first additional storage element that couples valid-data input signal path 614 to the enable input of memory device 650 via a staged valid data indicator 634. Memory device 630 has a second additional storage element that couples the K signal paths of additional bus 625 to the K signal paths of first intermediate bus 635.

[0071] Signature accumulator 600 may thus include an additional bus 625 and a first additional storage unit coupling the enable input of the storage unit to the valid-data input signal path 614. The second logic may include a second additional storage element coupling first intermediate bus 635 to additional bus 625.

[0072] In the embodiments illustrated in **Figs. 7 and 9**, compaction logic 620 is an XOR tree incorporating a number S of stages of XOR logic (as discussed above

with respect to **Fig. 3**). In addition, commutative arithmetic operation logic 640 performs an addition operation.

[0073] **Fig. 10** illustrates a system incorporating a component having a signature accumulator, according to some embodiments of the disclosure. More particularly, **Fig. 10** illustrates a block diagram of an embodiment of an SoC in which signature accumulators are used. In some embodiments, system 1000 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device.

[0074] It will be understood that certain components are shown generally, and not all components of such a device are shown in system 1000. In addition, in various embodiments, system 1000 may be an SoC, or a computer system, or a smart device. Moreover, while some of the components may be physically separate, others may be integrated within the same physical package, or even on the same physical silicon die. Accordingly, the separation between the various components as depicted in **Fig. 10** may not be physical in some cases, but may instead be a functional separation.

[0075] In some embodiments, system 1000 includes an interconnect fabric component 1010 having a number of ports connected to other components in system 1000. One or more of the ports has a signature accumulator connected to a datapath associated with that port.

[0076] System 1000 includes a processor 1090, which may be a general-purpose processor or CPU (Central Processing Unit). In some embodiments, processor 1090 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1090 may include the execution of an operating platform or operating system on which applications and/or device functions may then be executed. The processing operations may also include operations related to one or more of the following: I/O (input/output) with a human user or with other devices; power management; connecting system 1000 to another device; audio I/O; and/or display I/O.

[0077] In some embodiments, system 1000 includes an audio subsystem 1020, which represents hardware components (e.g., audio hardware and audio circuits) and software components (e.g., drivers and codecs) associated with providing audio functions to system 1000. Audio functions can include speaker and/or headphone output as well as microphone input. Devices for such functions can be integrated into

system 1000 or connected to system 1000. In one embodiment, a user interacts with system 1000 by providing audio commands that are received and processed by processor 1090.

[0078] In some embodiments, system 1000 includes a display subsystem 1030. Display subsystem 1030 represents hardware components (e.g., display devices) and software components (e.g., drivers) that provide a visual and/or tactile display for a user to interact with the system 1000. Display subsystem 1030 may include a display interface 1032, which may be a particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1032 includes logic separate from processor 1090 to perform at least some processing related to the display. In some embodiments, display subsystem 1030 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0079] In some embodiments, system 1000 includes an I/O controller 1040 associated with hardware devices and software components related to interaction with a user. I/O controller 1040 is operable to manage hardware that is part of audio subsystem 1020 and/or display subsystem 1030. Additionally, I/O controller 1040 may be a connection point for additional devices that connect to system 1000, through which a user might interact with the system. For example, devices that can be attached to the system 1000 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0080] As mentioned above, I/O controller 1040 can interact with audio subsystem 1020 and/or display subsystem 1030. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of system 1000. Additionally, audio output can be provided instead of, or in addition to, display output. In another example, if display subsystem 1030 includes a touch screen, the display device may also act as an input device, which can be at least partially managed by I/O controller 1040. There can also be additional buttons or switches on system 1000 to provide I/O functions managed by I/O controller 1040.

[0081] In some embodiments, I/O controller 1040 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in system 1000. The input can be part of direct user interaction, and may provide environmental input to the system to influence its

operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0082] In some embodiments, system 1000 includes a power management component 1050 that manages battery power usage, charging of the battery, and features related to power saving operation.

[0083] A memory subsystem 1060 includes memory devices for storing information in system 1000, coupled to processor 1090. Memory subsystem 1060 can include nonvolatile memory devices (whose state does not change if power to the memory device is interrupted) and/or volatile memory devices (whose state is indeterminate if power to the memory device is interrupted). Memory subsystem 1060 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of system 1000.

[0084] Some portion of memory subsystem 1060 may also be provided as a non-transitory machine-readable medium for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0085] In some embodiments, system 1000 includes a network interface within a connectivity component 1070, such as a cellular interface 1072 or a wireless interface 1074, so that a system embodiment may be incorporated into a wireless device such as a cell phone or personal digital assistant. In some embodiments, connectivity component 1070 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers or protocol stacks) to enable system 1000 to communicate with external devices. System 1000 could include separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0086] In some embodiments, connectivity component 1070 can include multiple different types of network interfaces, such as one or more wireless interfaces for allowing processor 1090 to communicate with another device. To generalize, system 1000 is illustrated with cellular connectivity 1072 and wireless connectivity 1074. Cellular connectivity 1072 refers generally to wireless interfaces such as cellular network connectivity provided by wireless carriers, such as provided via GSM or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless interface 1074 refers generally to wireless interfaces that are not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0087] In some embodiments, system 1000 has various peripheral connections 1080. Peripheral connections 1080 may include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that system 1000 could both be a peripheral device to other computing devices (via "to" 1082), as well as have peripheral devices connected to it (via "from" 1084). System 1000 may have a "docking" connector to connect to other computing devices for purposes such as managing content on system 1000 (e.g., downloading and/or uploading, changing, synchronizing). Additionally, a docking connector can allow system 1000 to connect to certain peripherals that allow system 1000 to control content output, for example, to audiovisual or other systems.

[0088] In addition to a proprietary docking connector or other proprietary connection hardware, system 1000 can make peripheral connections 1080 via common or standards-based connectors. Common types of connectors can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), a DisplayPort or MiniDisplayPort (MDP) connector, a High Definition Multimedia Interface (HDMI) connector, a Firewire connector, or other types of connectors.

[0089] **Figs. 11 and 12** illustrate methods of accumulating a signature, according to some embodiments of the disclosure. Although the blocks in the flowchart with reference to **Figs. 11 and 12** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of

the blocks and/or operations listed in **Figs. 11 and 12** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0090] With reference to **Fig. 11**, a method 1100 may include a compacting 1110 of N-bit input data, a performing 1130 of a commutative arithmetic operation, and a registering 1140 of K-bit second intermediate data. More particularly, in compacting 1110, an N-bit input data may be compacted to generate a K-bit first intermediate data. Then, in performing 1130, a commutative arithmetic operation may be performed between the K-bit first intermediate data and a K-bit signature data to generate a K-bit second intermediate data. Finally, in registering 1140, the K-bit second intermediate data may be registered to generate the K-bit signature data, wherein a valid data signal is coupled to the K-bit signature data.

[0091] With reference to **Fig. 12**, in some embodiments, method 1100 may additionally include a registering 1120 of K-bit first intermediate data. More particularly, in registering 1120, the K-bit first intermediate data may be registered to generate a K-bit registered first intermediate data. In some embodiments, a valid-data signal may also be registered to generate a registered valid-data signal.

[0092] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0093] Furthermore, the particular features, structures, functions, or characteristics disclosed may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second

embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0094] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0095] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[0096] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[0097] In one example, an apparatus is provided which may comprise: an input bus having a number N of signal paths, a valid-data input signal path, a first intermediate bus having a number K of signal paths, a second intermediate bus having the number K of signal paths, a signature bus having the number K of signal paths, a first set of logic devices, a second set of logic devices, and a memory device. The first set of logic devices may include compaction logic coupling the N signal paths of the input bus to the K signal paths of the first intermediate bus. The second set of logic devices may include commutative arithmetic operation logic coupling both the K signal paths of the first intermediate bus and the K signal paths of the signature bus to the K signal paths of the second intermediate bus. The memory device may include

a storage element coupling the K signal paths of the second intermediate bus to the K signal paths of the signature bus. The signature bus may be coupled to the valid-data input signal path.

[0098] In some embodiments, the compaction logic may include at least one stage of XOR logic. In some embodiments, the commutative arithmetic operation logic may include adder logic. In some embodiments, the ratio of N to K may be a power of two. In some embodiments, the apparatus may comprise a register memory having an input coupled to the signature bus. In some embodiments, the register memory may be within an address space of a port within the interconnect fabric.

[0099] In some embodiments, the apparatus may comprise an additional bus and an additional memory device. The additional bus may have the number K of signal paths. The additional memory device may include a first additional storage element coupling the enable input of the memory device to the valid-data input signal path. The second set of logic devices may include a second additional storage element coupling the K signal paths of the first intermediate bus to the K signal paths of the additional bus. The commutative arithmetic logic may couple the K signal paths of the additional bus and the K signal paths of the signature bus to the K signal paths of the second intermediate bus. In some embodiments, the apparatus may be coupled to at least two ports within an interconnect fabric.

[00100] In another example, an apparatus is provided which may comprise: a first logic, a second logic, and a storage unit. The first logic may have an input coupled to an input bus and an output coupled to a first intermediate bus, and the first logic may be operable to perform a compaction operation on the bits of the input bus. The second logic may have a first input coupled to the first intermediate bus, a second input coupled to a signature bus, and an output coupled to a second intermediate bus, and the second logic may be operable to perform a commutative arithmetic operation between the first intermediate bus and the signature bus. The storage unit may have an input coupled to the second intermediate bus and an output coupled to the signature bus, and the storage unit may include memory devices operable to store K bits of data on the second intermediate bus. The signature bus may be coupled to a valid-data input.

[00101] In some embodiments, the compaction operation may include at least one stage of XOR operations. In some embodiments, the commutative arithmetic operation may be an addition operation. In some embodiments, the input bus may

have a width of N bits, the first intermediate bus may have a width of K bits, the second intermediate bus may have a width of K bits, and the third intermediate bus may have a width of K bits. In some embodiments, the ratio of N to K may be a power of two. Some embodiments may comprise a register memory having an input coupled to the signature bus. In some embodiments, the register memory may be within an address space of the port within the interconnect fabric.

[00102] In some embodiments, the apparatus may comprise an additional bus and a first additional storage unit. The first additional storage unit may couple the enable input of the storage unit to the valid-data input. The second logic may include a second additional storage element coupling the first intermediate bus to the additional bus. The second logic may be operable to perform a commutative arithmetic operation between the additional bus and the signature bus.

[00103] In another example, a system is provided which may comprise a memory, a processor coupled to the memory, and a wireless interface for allowing the processor to communicate with another device, the processor including any of the exemplary apparatus described above.

[00104] In another example, a system is provided which may comprise: a memory, a processor coupled to the memory, and a wireless interface for allowing the processor to communicate with another device. The processor may include an input bus, a first set of logic devices, a second set of logic devices, and a memory device. The input bus may have a number N of signal paths, a valid-data input signal path, a first intermediate bus having a number K of signal paths, a second intermediate bus having the number K of signal paths, and a signature bus having the number K of signal paths. The first set of logic devices may include compaction logic coupling the N signal paths of the input bus to the K signal paths of the first intermediate bus. The second set of logic devices may include commutative arithmetic operation logic coupling both the K signal paths of the first intermediate bus and the K signal paths of the signature bus to the K signal paths of the second intermediate bus. The memory device may include a storage element coupling the K signal paths of the second intermediate bus to the K signal paths of the signature bus. The signature bus may be coupled to the valid-data input signal path.

[00105] In some embodiments, the compaction logic may include at least one stage of XOR logic, and the commutative arithmetic operation logic may include adder logic. In some embodiments, the ratio of N to K may be a power of two.

[00106] In some embodiments, the system may comprise an additional bus and an additional memory device. The additional bus may have the number K of signal paths. The additional memory device may include a first additional storage element coupling the enable input of the memory device to the valid-data input signal path. The second set of logic devices may include a second additional storage element coupling the K signal paths of the first intermediate bus to the K signal paths of the additional bus. The commutative arithmetic logic may couple the K signal paths of the additional bus and the K signal paths of the signature bus to the K signal paths of the second intermediate bus.

[00107] In another example, a method is provided which may comprise: compacting an N-bit input data to generate a K-bit first intermediate data; registering the K-bit first intermediate data to generate a K-bit registered first intermediate data; registering a valid-data signal to generate a registered valid-data signal; performing a commutative arithmetic operation between the K-bit registered first intermediate data and a K-bit signature data to generate a K-bit second intermediate data; and registering the K-bit second intermediate data to generate the K-bit signature data, wherein a valid data signal is coupled to the K-bit signature data.

[00108] In some embodiments, the compaction may include one or more stages of XOR operations. In some embodiments, the commutative arithmetic operation may be an addition operation. In some embodiments, the ratio of N to K may be a power of two. In some embodiments, the K-bit signature data may be registered in a register memory within an address space of a port within an interconnect fabric.

[00109] In another example, machine readable storage media having machine executable instructions stored thereon are provided. The instructions, when executed, may cause one or more processors to perform a method according to any of the exemplary methods discussed above.

[00110] In another example, machine readable storage media having machine executable instructions stored thereon are provided. The instructions, when executed, may cause one or more processors to perform an operation comprising: compact an N-bit input data to generate a K-bit first intermediate data; register the K-bit first intermediate data to generate a K-bit registered first intermediate data; register a valid-data signal to generate a registered valid-data signal; perform a commutative arithmetic operation between the K-bit registered first intermediate data and a K-bit signature data to generate a K-bit second intermediate data; and register the K-bit

second intermediate data to generate the K-bit signature data, wherein a valid data signal is coupled to the K-bit signature data.

[00111] In some embodiments, the compaction may include one or more stages of XOR operations. In some embodiments, the commutative arithmetic operation may be an addition operation. In some embodiments, the ratio of N to K may be a power of two. In some embodiments, the K-bit signature data may be registered in a register memory within an address space of a port within an interconnect fabric.

[00112] In another example, an apparatus may comprise: means for compacting an N-bit input data to generate a K-bit first intermediate data; means for registering the K-bit first intermediate data to generate a K-bit registered first intermediate data; means for registering a valid-data signal to generate a registered valid-data signal; means for performing a commutative arithmetic operation between the K-bit registered first intermediate data and a K-bit signature data to generate a K-bit second intermediate data; and means for registering the K-bit second intermediate data to generate the K-bit signature data, wherein a valid data signal is coupled to the K-bit signature data.

[00113] In some embodiments, the means for compacting may include one or more stages of XOR operations. In some embodiments, the commutative arithmetic operation may be an addition operation. In some embodiments, the ratio of N to K may be a power of two. In some embodiments, the K-bit signature data may be registered in a register memory within an address space of a port within an interconnect fabric.

[00114] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:

an input bus having a number N of signal paths, a valid-data input signal path, a first intermediate bus having a number K of signal paths, a second intermediate bus having the number K of signal paths, and a signature bus having the number K of signal paths;

a first set of logic devices including compaction logic coupling the N signal paths of the input bus to the K signal paths of the first intermediate bus;

a second set of logic devices including commutative arithmetic operation logic coupling both the K signal paths of the first intermediate bus and the K signal paths of the signature bus to the K signal paths of the second intermediate bus; and

a memory device including a storage element coupling the K signal paths of the second intermediate bus to the K signal paths of the signature bus,

wherein the signature bus is coupled to the valid-data input signal path.

2. The apparatus of claim 1, wherein the compaction logic includes at least one stage of XOR logic.

3. The apparatus of claim 1, wherein the commutative arithmetic operation logic includes adder logic.

4. The apparatus of claim 1, wherein the ratio of N to K is a power of two.

5. The apparatus of claim 1, comprising a register memory having an input coupled to the signature bus.

6. The apparatus of claim 5, wherein the register memory is within an address space of a port within the interconnect fabric.

7. The apparatus of claim 1, comprising:

an additional bus having the number K of signal paths; and

an additional memory device including a first additional storage element coupling the enable input of the memory device to the valid-data input signal path,

wherein the second set of logic devices includes a second additional storage element coupling the K signal paths of the first intermediate bus to the K signal paths of the additional bus; and

wherein the commutative arithmetic logic couples the K signal paths of the additional bus and the K signal paths of the signature bus to the K signal paths of the second intermediate bus.

8. The apparatus of claim 1, wherein the apparatus is coupled to at least two ports within an interconnect fabric.

9. A system comprising a memory, a processor coupled to the memory, and a wireless interface for allowing the processor to communicate with another device, the processor including the apparatus of any of claims 1 through 8.

10. A method comprising:

compacting an N-bit input data to generate a K-bit first intermediate data;

registering the K-bit first intermediate data to generate a K-bit registered first intermediate data;

registering a valid-data signal to generate a registered valid-data signal;

performing a commutative arithmetic operation between the K-bit registered first intermediate data and a K-bit signature data to generate a K-bit second intermediate data; and

registering the K-bit second intermediate data to generate the K-bit signature data, wherein a valid data signal is coupled to the K-bit signature data.

11. The method of claim 10, wherein the compacting includes one or more stages of XOR operations.

12. The method of claim 10, wherein the commutative arithmetic operation is an addition operation.

13. The method of claim 10, wherein the ratio of N to K is a power of two.

14. The method of claim 10, wherein the K-bit signature data is registered in a register memory within an address space of a port within an interconnect fabric.

15. Machine readable storage media having machine executable instructions stored thereon that, when executed, cause one or more processors to perform a method according to any one of claims 10 through 15.

16. An apparatus comprising:

means for compacting an N-bit input data to generate a K-bit first intermediate data;

means for registering the K-bit first intermediate data to generate a K-bit registered first intermediate data;

means for registering a valid-data signal to generate a registered valid-data signal;

means for performing a commutative arithmetic operation between the K-bit registered first intermediate data and a K-bit signature data to generate a K-bit second intermediate data; and

means for registering the K-bit second intermediate data to generate the K-bit signature data, wherein a valid data signal is coupled to the K-bit signature data.

17. The apparatus of claim 16, wherein the means for compacting includes one or more stages of XOR operations.

18. The apparatus of claim 16, wherein the commutative arithmetic operation is an addition operation.

19. The apparatus of claim 16, wherein the ratio of N to K is a power of two.

20. The apparatus of claim 16, wherein the K-bit signature data is registered in a register memory within an address space of a port within an interconnect fabric.

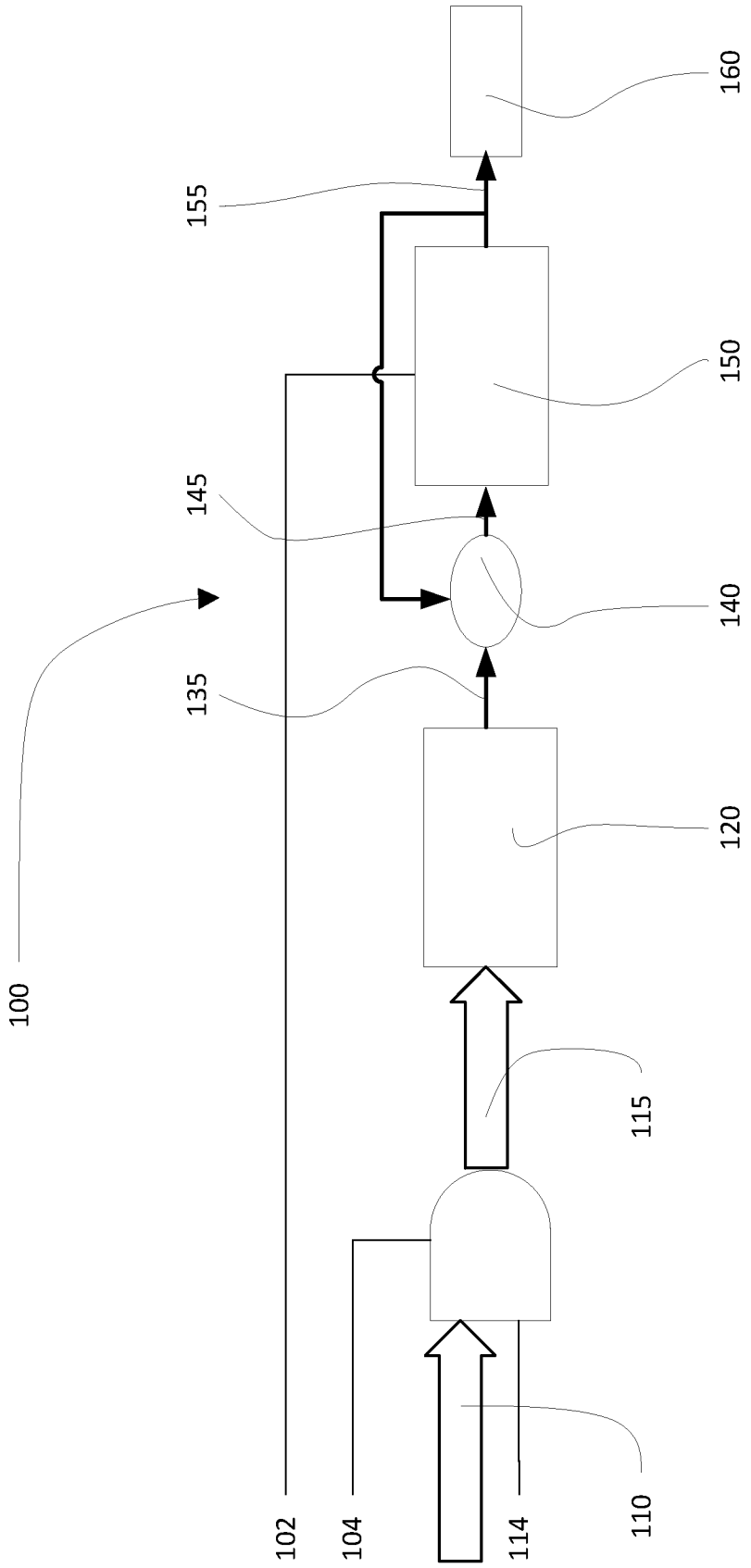

Fig. 1

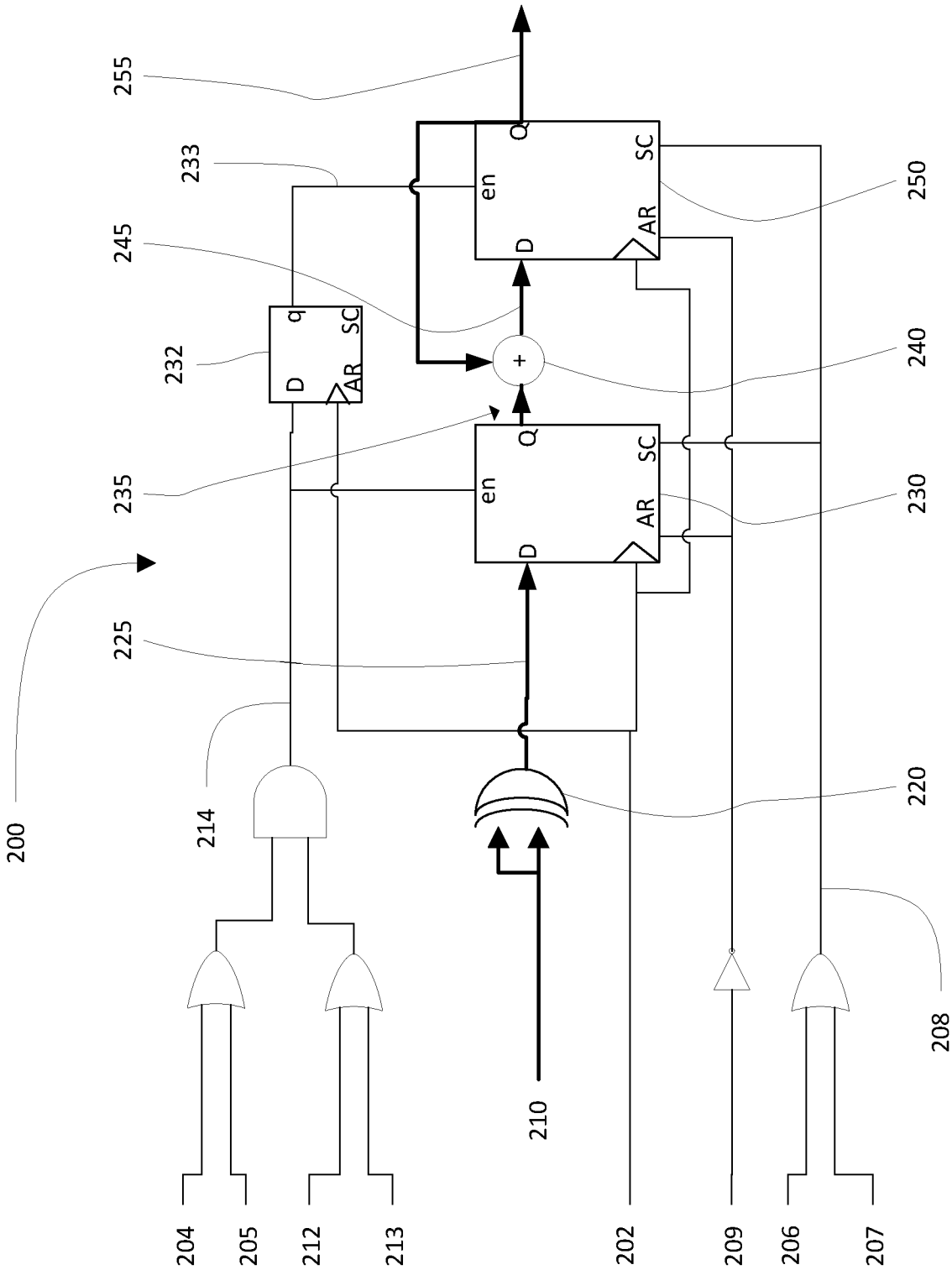
255
233
245
232
235
225
200
214
204
205
212
213
210
202
209
206
207
208
220
230
240
250
Q
en
D
SC
AR
q
+

Fig. 2

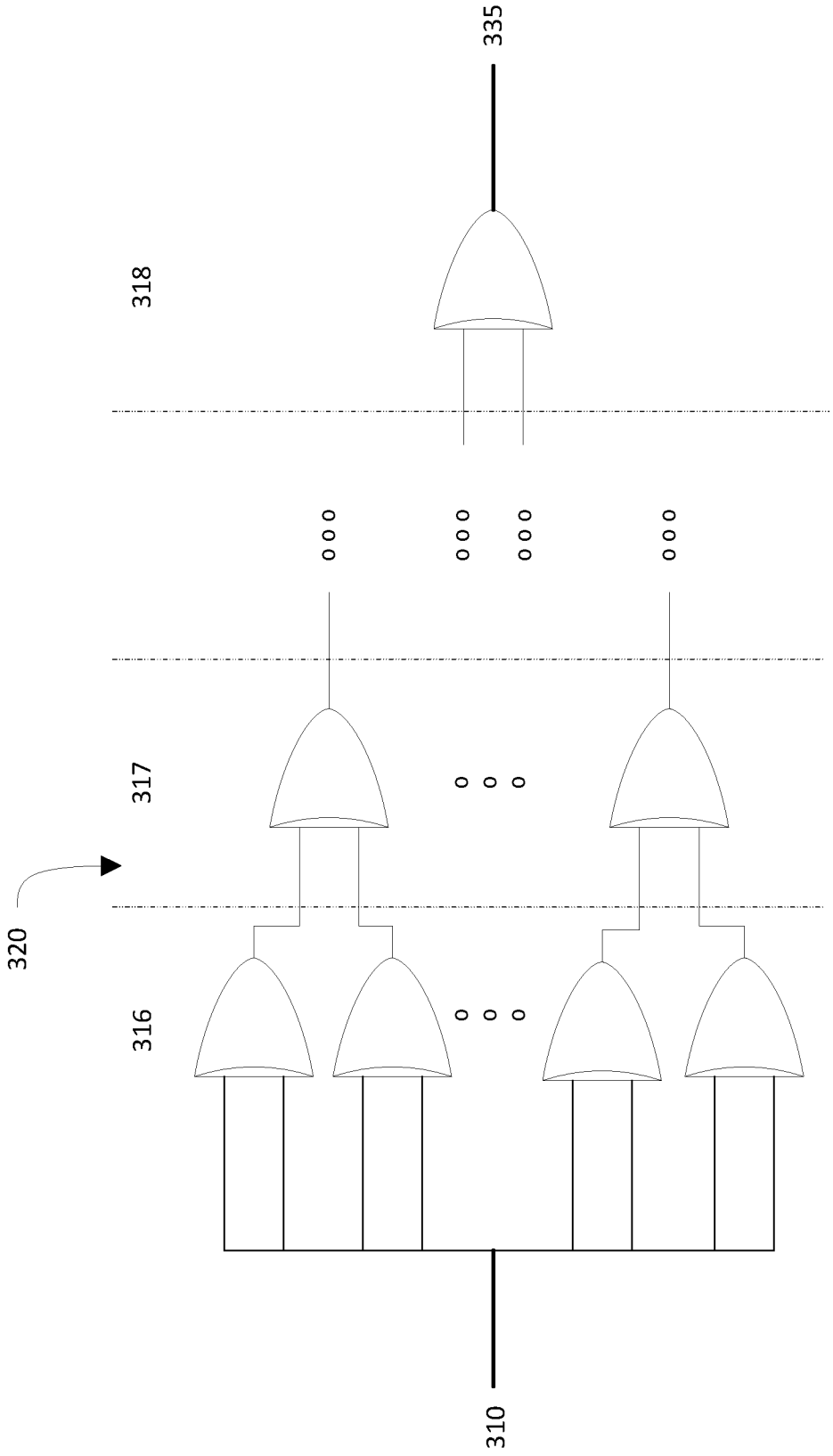

Fig. 3

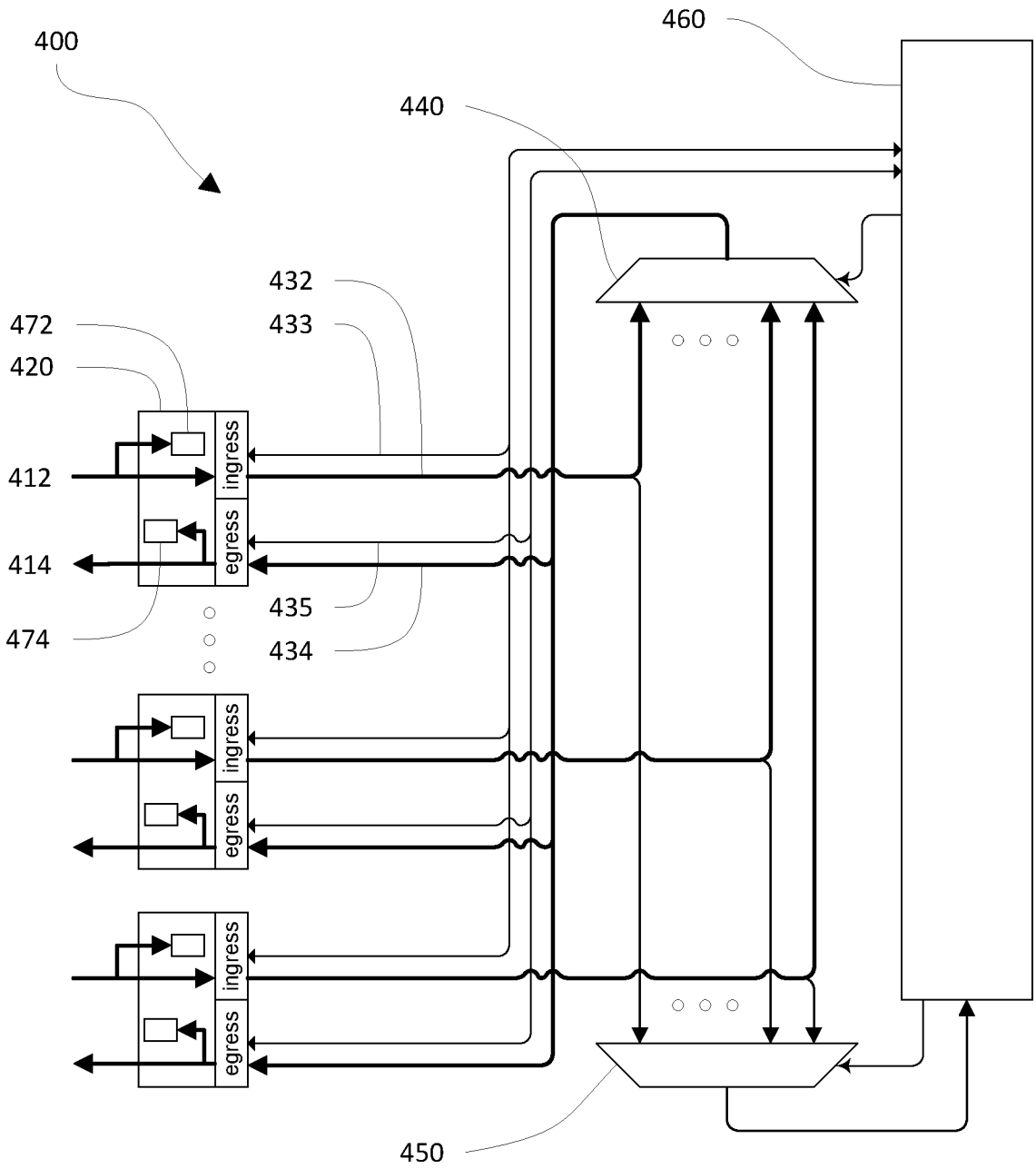
400
460
440
432
433
472
420
412
414
474
435
434
ingress
egress
ingress
egress
ingress
egress
450

Fig. 4

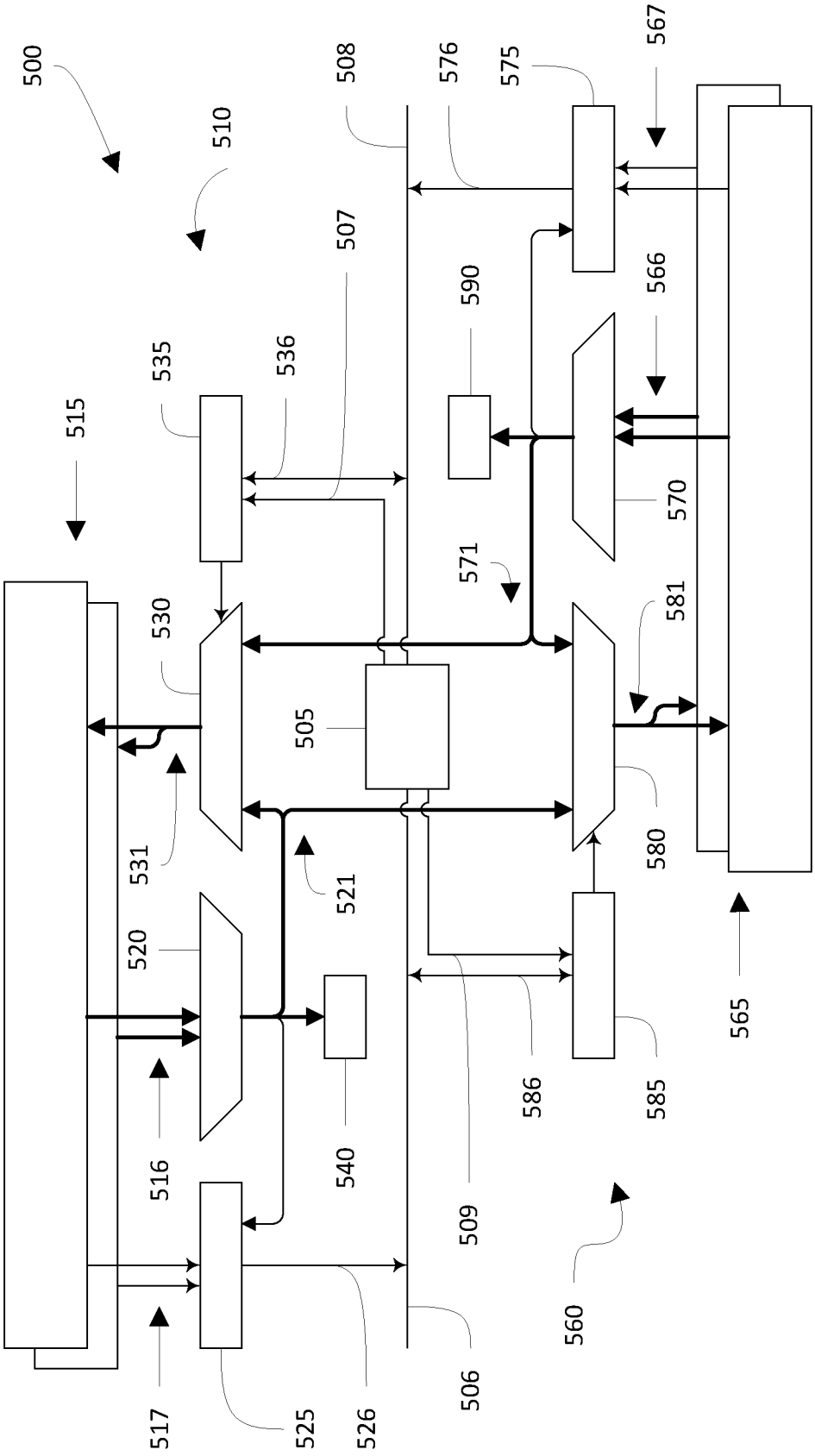
500
510
508
576
575
567
507
590
566
535
536
515
570
571
530
581
505
580
531
521
520
565
586
585
516
540
509
560
517
525
526
506

Fig. 5

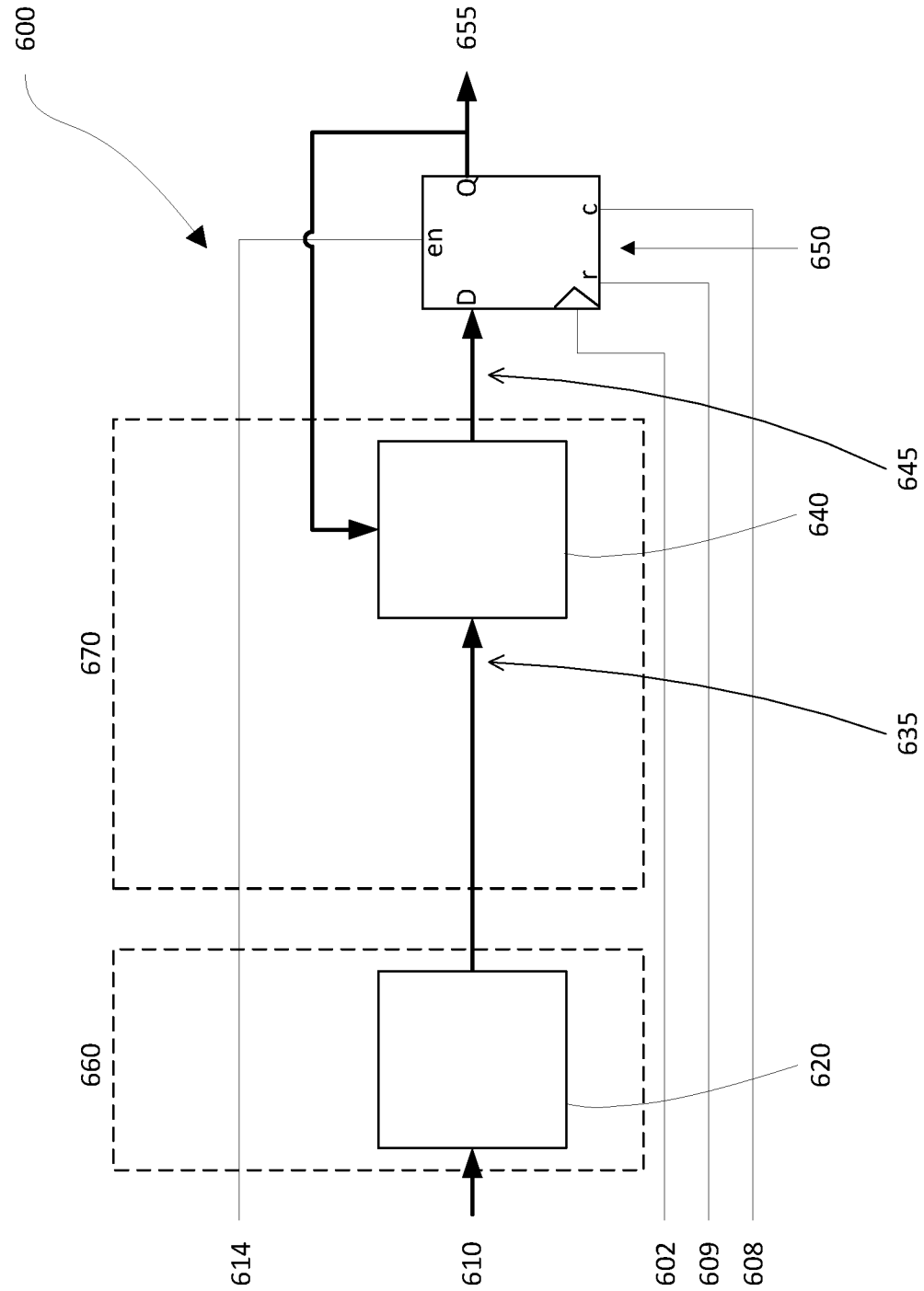

Fig. 6

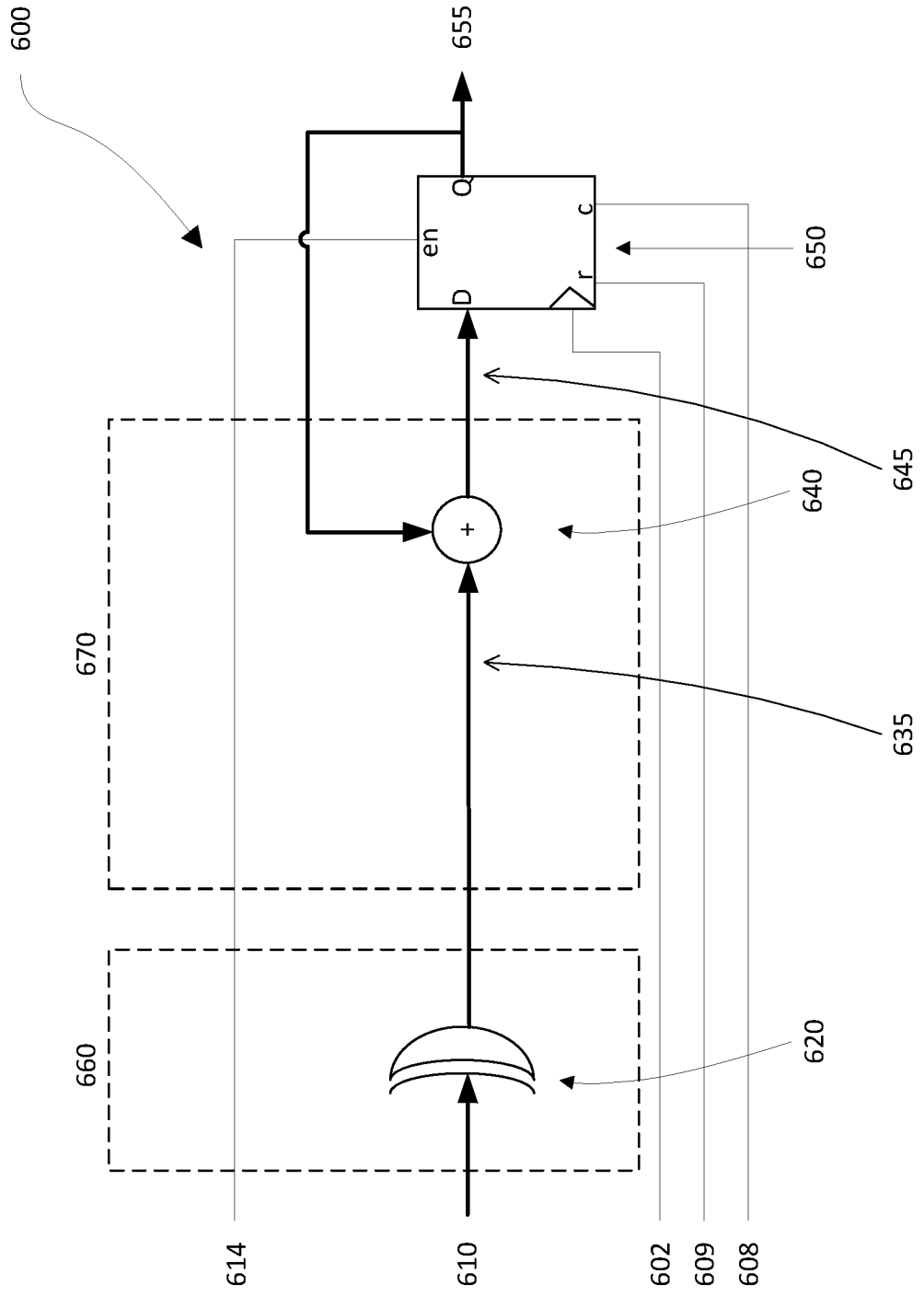

Fig. 7

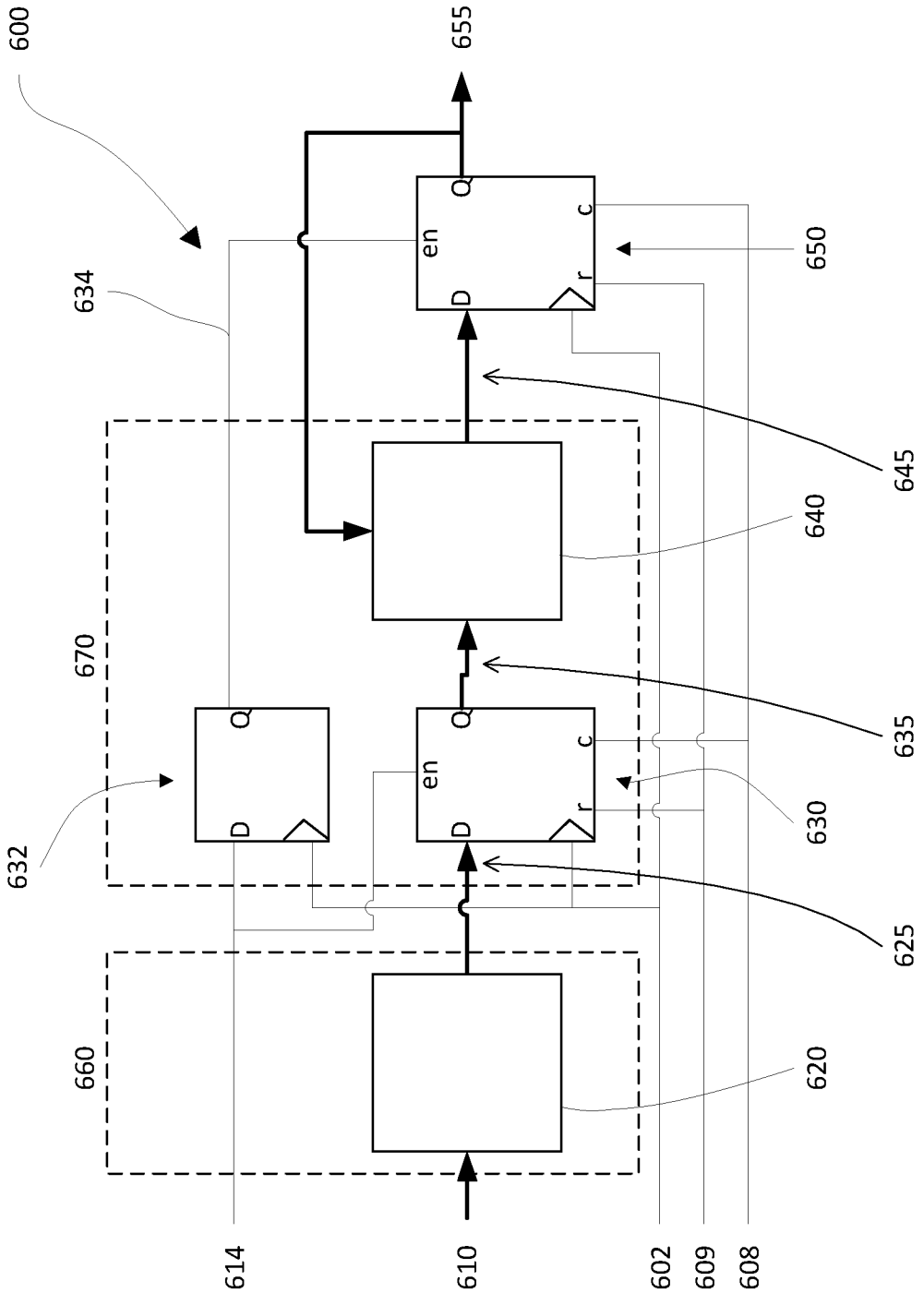
600
655
634
650
645
640
670
635
632
630
625
660
620
614
610
602
609
608
Q
en
c
r
D

Fig. 8

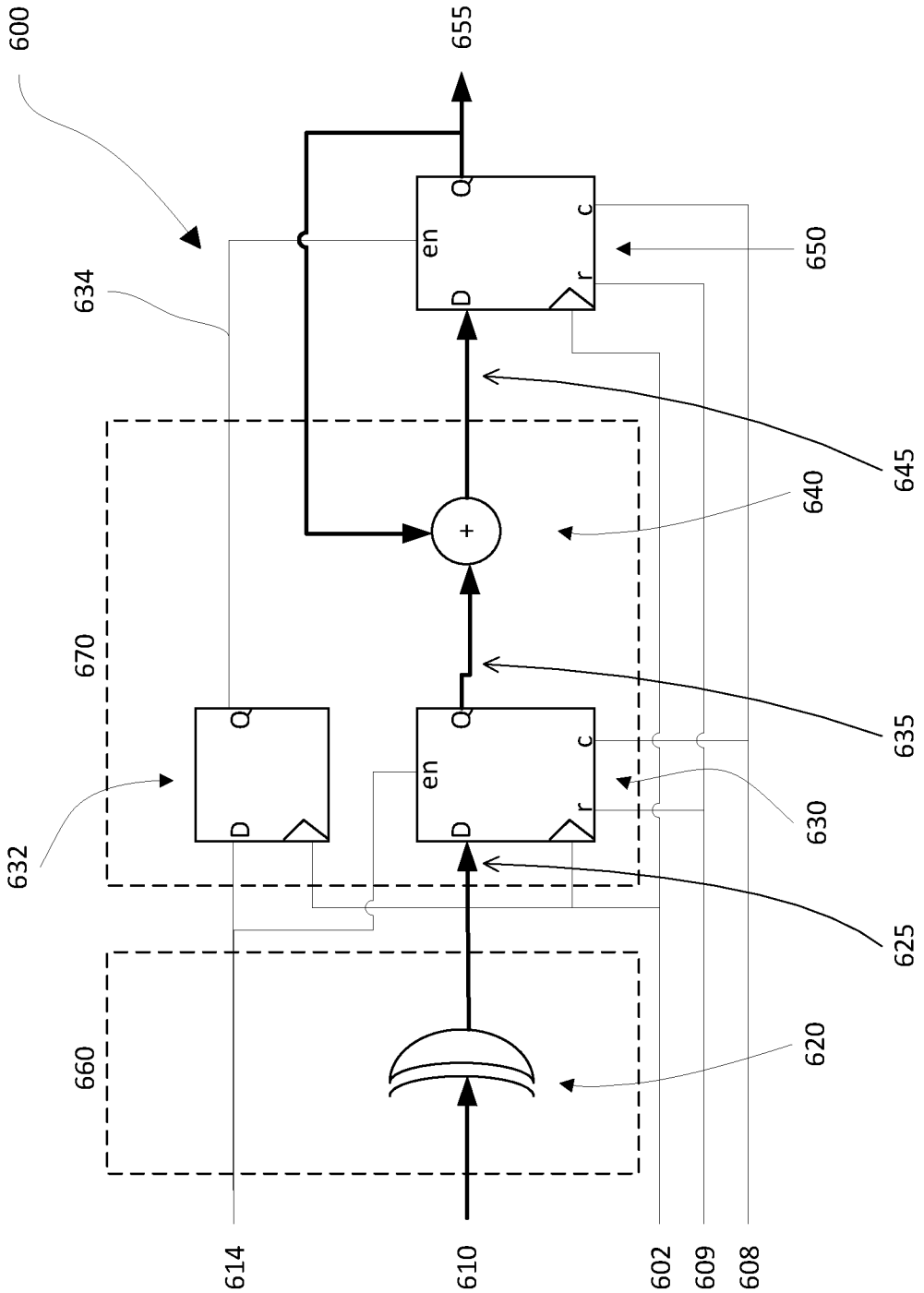
600
655
634
650
645
640
670
635
632
630
625
660
620
614
610
602
609
608
Q
en
D
c
r
+

Fig. 9

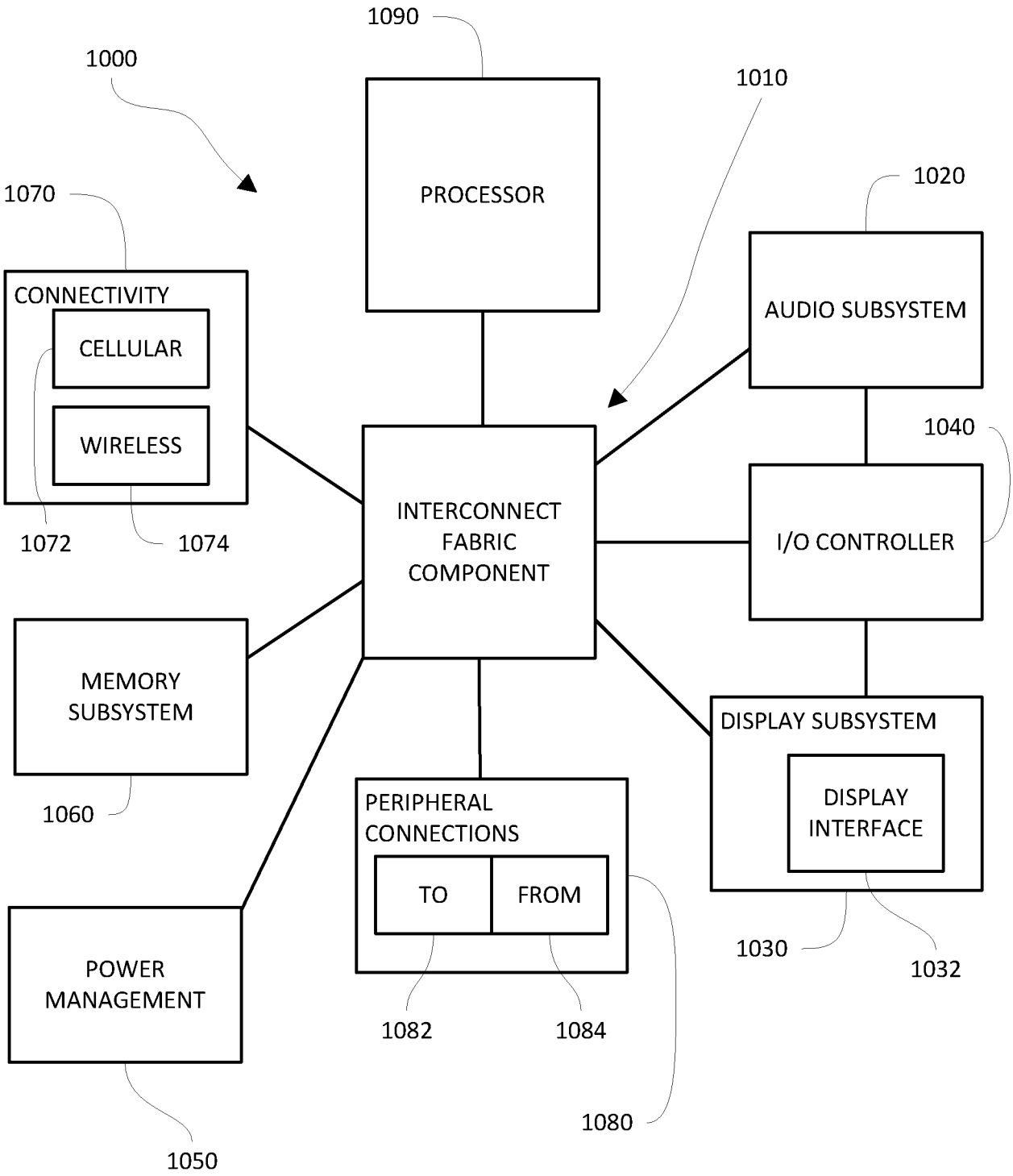
1090
1000
1010
PROCESSOR
1070
1020
CONNECTIVITY
CELLULAR
WIRELESS
AUDIO SUBSYSTEM
1040
INTERCONNECT FABRIC COMPONENT
I/O CONTROLLER
1072
1074
MEMORY SUBSYSTEM
1060
DISPLAY SUBSYSTEM
DISPLAY INTERFACE
PERIPHERAL CONNECTIONS
TO
FROM
POWER MANAGEMENT
1030
1032
1082
1084
1080
1050

Fig. 10

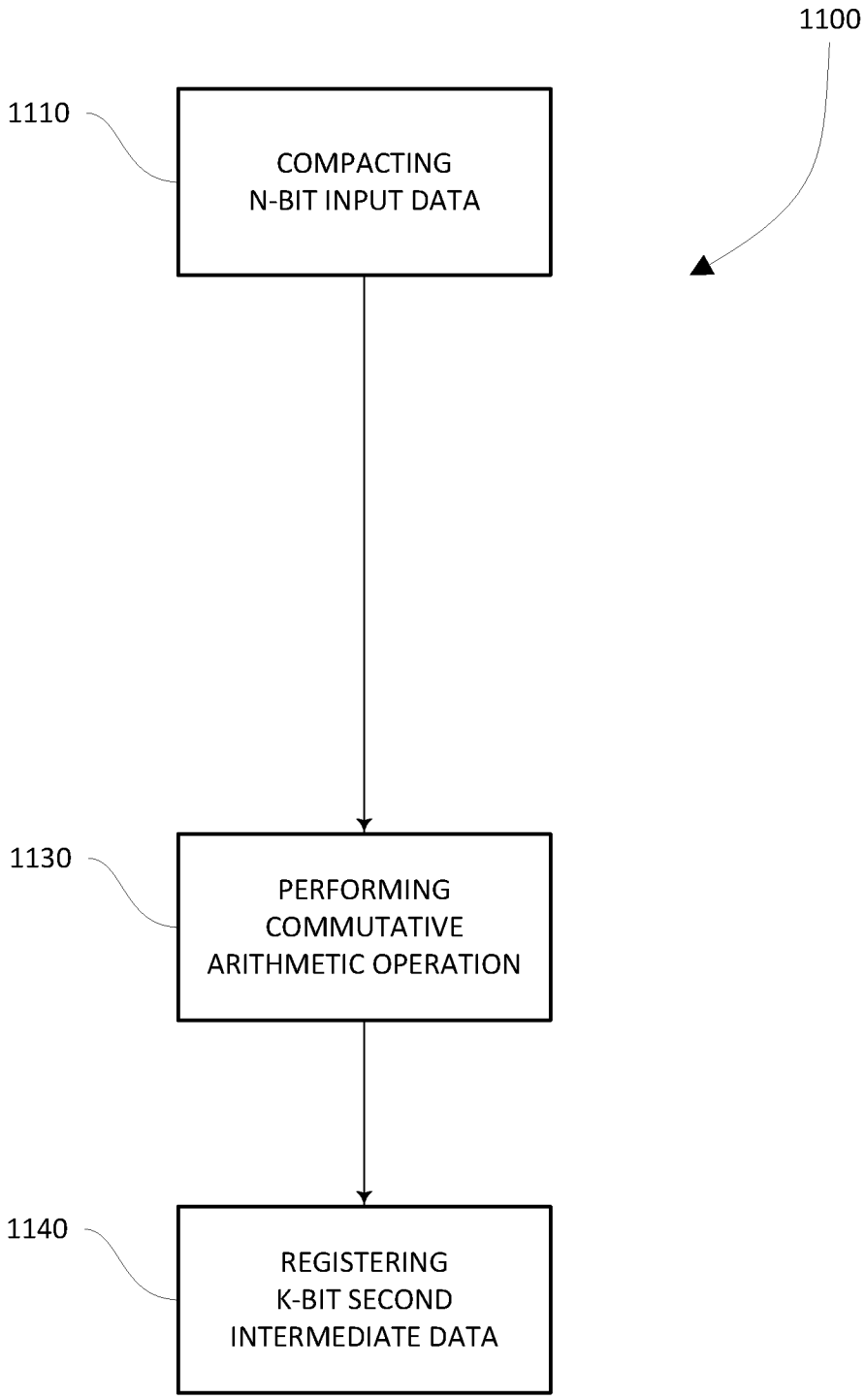
1100
1110
COMPACTING
N-BIT INPUT DATA
1130
PERFORMING
COMMUTATIVE
ARITHMETIC OPERATION
1140
REGISTERING
K-BIT SECOND
INTERMEDIATE DATA

Fig. 11

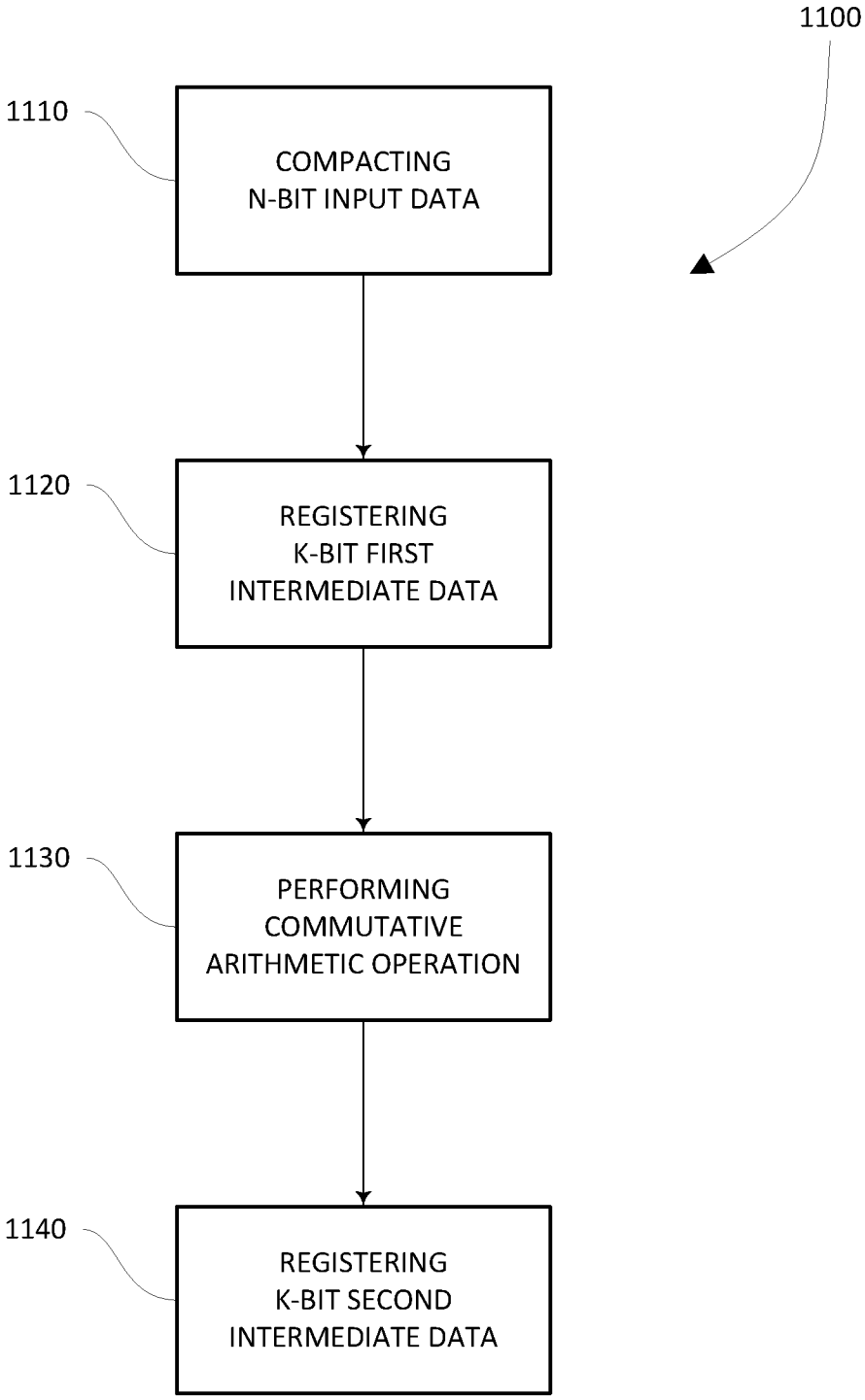
1100
1110
COMPACTING
N-BIT INPUT DATA
1120
REGISTERING
K-BIT FIRST
INTERMEDIATE DATA
1130
PERFORMING
COMMUTATIVE
ARITHMETIC OPERATION
1140
REGISTERING
K-BIT SECOND
INTERMEDIATE DATA

Fig. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/063122

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/317(2006.01)i, G01R 31/3185(2006.01)i, G01R 31/3193(2006.01)i, G11C 29/56(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R 31/317; G01R 31/3177; G06F 11/25; G06F 15/78; G06F 13/40; G01R 31/28; G01R 31/3185; G01R 31/3193; G11C 29/56

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: chip, interconnect, test, compact, logic, signature, memory

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0257417 A1 (RAJSKI et al.) 07 October 2010 See claims 34,82 and figures 7-12.	1-20
A	US 2007-0260950 A1 (MORRISON et al.) 08 November 2007 See claims 1-9 and figures 1,2.	1-20
A	US 9189439 B2 (INTEL CORPORATION) 17 November 2015 See claims 1-3 and figures 1-5.	1-20
A	US 2005-0005215 A1 (NAPOLITANO) 06 January 2005 See paragraphs [20]-[44] and figures 1-3.	1-20
A	US 7506234 B2 (LEE et al.) 17 March 2009 See claims 1-9 and figure 3.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 2017 (28.02.2017)	**03 March 2017 (03.03.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Yeon Kyung
Telephone No. +82-42-481-3325

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/063122

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0257417 A1	07/10/2010	AT 400845 T	15/07/2008
		AT 532133 T	15/11/2011
		EP 1595211 A2	16/11/2005
		EP 1595211 A4	30/11/2005
		EP 1595211 B1	09/07/2008
		EP 1978446 A1	08/10/2008
		EP 1978446 B1	02/11/2011
		JP 2006-518855 A	17/08/2006
		JP 4791954 B2	12/10/2011
		US 2004-0230884 A1	18/11/2004
		US 2006-0041812 A1	23/02/2006
		US 2006-0041813 A1	23/02/2006
		US 2006-0041814 A1	23/02/2006
		US 2008-0133987 A1	05/06/2008
		US 2009-0249147 A1	01/10/2009
		US 7302624 B2	27/11/2007
		US 7370254 B2	06/05/2008
		US 7437640 B2	14/10/2008
		US 7509550 B2	24/03/2009
		US 7743302 B2	22/06/2010
		US 7890827 B2	15/02/2011
		US 7962820 B2	14/06/2011
		WO 2004-072660 A2	26/08/2004
		WO 2004-072660 A3	28/04/2005
US 2007-0260950 A1	08/11/2007	JP 2009-527821 A	30/07/2009
		JP 5373403 B2	18/12/2013
		KR 10-1318697 B1	16/10/2013
		KR 10-2008-0098609 A	11/11/2008
		TW 200817704 A	16/04/2008
		TW I403744 B	01/08/2013
		US 7444568 B2	28/10/2008
		WO 2007-103591 A2	13/09/2007
		WO 2007-103591 A3	04/12/2008
US 9189439 B2	17/11/2015	BR PI1005611 A2	28/02/2012
		CN 102103569 A	22/06/2011
		CN 102103569 B	27/05/2015
		EP 2345969 A2	20/07/2011
		EP 2345969 A3	21/03/2012
		RU 2010151717 A	20/06/2012
		RU 2470350 C2	20/12/2012
		TW 201140324 A	16/11/2011
		TW I465921 B	21/12/2014
		US 2011-0145909 A1	16/06/2011
		US 2014-0108695 A1	17/04/2014
		US 8650629 B2	11/02/2014
US 2005-0005215 A1	06/01/2005	EP 1475891 A1	10/11/2004

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/063122

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		EP 1475891 B1	15/03/2006
		US 7284173 B2	16/10/2007
US 7506234 B2	17/03/2009	DE 102006033189 A1	22/03/2007
		KR 10-0599215 B1	12/07/2006
		US 2007-0030051 A1	08/02/2007