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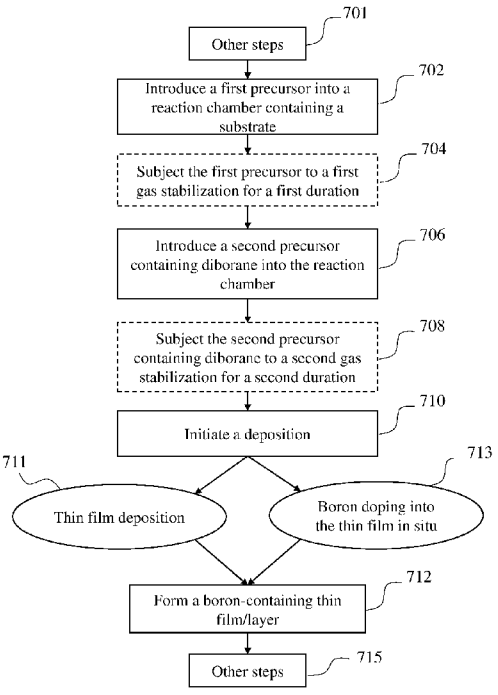

FIG. 7

(57) Abstract: The present disclosure relates to a method of forming a boron-containing thin film. The method comprises introducing a first precursor into a reaction chamber containing a substrate, subjecting the first precursor to a first gas stabilization step for a first duration, introducing a second precursor containing diborane into the reaction chamber, subjecting the second precursor to a second gas stabilization step for a second duration; and initiating a deposition process to form a boron-containing thin film on the substrate, wherein the second duration is shorter than the first duration. The method can be employed for use in fabricating devices that require the deposition of a boron-containing thin film.

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METHOD OF FORMING BORON-CONTAINING THIN FILMS AND DEVICES MADE THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority to the Singapore patent application no. 10202301700T filed on 15 June 2023, the contents of which are hereby incorporated by reference in their entirety for all purposes.

TECHNICAL FIELD

[0002] The present disclosure relates to a method of forming a boron-containing thin film, and more particularly to a method of forming boron-containing thin film using diborane precursor as a dopant source.

BACKGROUND

[0003] To produce silicon heterojunction solar cells and other devices, the deposition of boron-doped amorphous silicon thin film is one of the essential processes. FIG. 1A and FIG. 1B show flow diagrams of p-type amorphous silicon (p-aSi) deposition process via Plasma Enhanced Chemical Vapor Deposition (PECVD) using different dopant precursors. FIG. 1A shows deposition using trimethylborane (TMB) as the dopant precursor gas, while FIG. 1B shows deposition using diborane (B_2H_6) as the dopant precursor gas.

[0004] TMB is typically used as the dopant gas precursor in the PECVD process to produce boron-doped amorphous silicon thin films for hole-transport layers in silicon heterojunction solar cells and other devices. TMB is a molecule containing one boron atom bonded to three methyl (CH_3) groups. Thin film layers made using TMB are known to result in good device performance in a laboratory environment when it is used as a hole-transport layer in silicon heterojunction solar cells or in other devices. However, due to its low boron content, a higher gas flow of TMB is necessary to achieve the desired boron doping concentration in the deposited layer. Furthermore, the price of TMB is higher compared to other alternative doping gases such as diborane. This results in higher operating expenses (OPEX). Hence, large-scale manufacturing using TMB is less attractive.

[0005] Diborane, in contrast, consists of two boron atoms and six hydrogen atoms. Because diborane contains twice the boron of TMB, it requires lower gas flow and is cheaper, making it more cost-effective for large-scale manufacturing.

[0006] FIG. 2 is a schematic graph illustrating the process cost analysis of p-aSi deposition using PECVD, with dopant precursor gases like TMB and diborane being used individually. Diborane gas contains 2 boron atoms, twice of that of TMB. As a result, to achieve the same boron content in the deposited layer, the gas flow rate of diborane required is half or less than half of that needed for TMB. Consequently, the gas consumption rate of diborane is lower. Additionally, diborane is typically priced lower than TMB. This results in lower overall operating expenses (OPEX) when using diborane. Therefore, diborane proves more cost-effective for large-scale manufacturing of devices that use boron-doped thin films grown using PECVD.

[0007] However, the diborane-based PECVD process, as known in the current state of the art, may result in low device performance. For instance, heterojunction (HJT) solar cells fabricated using the diborane-based PECVD method known in the current state of the art exhibit low device performance. FIG. 3 is a schematic diagram showing the structure of a conventional HJT solar cell. Conventional HJT solar cell requires an intrinsic amorphous silicon (i-aSi) layer deposited on top of the silicon wafer substrate to passivate the crystalline silicon (wafer) surface. If the layer deposited immediately above the i-aSi layer causes damage to the i-aSi layer or the i-aSi layer is otherwise defective, it can impact the passivation of the silicon wafer, resulting in lower device performance. On the p-type side of the HJT cell (typically the rear side), a p-aSi layer is typically deposited onto the i-aSi layer.

[0008] FIG. 4 is a flow diagram illustrating a typical PECVD deposition process. The process begins with the introduction of all gaseous species to be reacted into a reaction chamber (401). This is followed by a gas stabilization step (403), allowing the gas flow to stabilize and the chamber to reach the desired process pressure. Subsequently, plasma is ignited (405), followed by the deposition of the target film (407). In a PECVD process, the deposition of the target film usually occurs only after plasma ignition. Therefore, it is generally assumed that no deposition occurs during the gas stabilization step, prior to plasma ignition.

[0009] FIG. 5 is a flow diagram illustrating a typical PECVD deposition process using diborane as the p-type dopant precursor for the deposition of p-aSi layer in the fabrication of an HJT cell. The process involves introducing diborane and other gases into the reaction chamber (501), followed by subjecting the mixture to a gas stabilization step (503). This step ensures stable pressure and a consistent gas mixture comprising all the desired precursor gases. The gas stabilization step occurs prior to plasma ignition (505) for the deposition of the p-aSi layer. During the gas stabilization step, no layer deposition occurs since plasma has not yet been ignited. However, the substrate and/or the pre-existing layers, such as the i-aSi layer present in the reaction chamber, are still exposed to the precursor gases. The exposure can last from a few seconds to a few minutes. The exposure of the i-aSi layer to diborane and other gases in the absence of plasma leads to reduced passivation of the silicon wafer surface, as a defective interface layer is formed between the i-aSi and the p-aSi layers.

[0010] FIG. 6 is a schematic diagram illustrating a conventional HJT solar cell (600) with a defective interface layer (601) formed at the i-aSi/p-aSi interface. This defective interface layer (601) reduces the performance of the HJT solar cell, resulting in a higher cost per watt ($/W) of the solar cell or module device. Additionally, such defective interface layers could form and degrade the performance of other devices utilizing the i-aSi/p-aSi stacks, including thin-film transistor (TFT) devices, among others.

[0011] In addition to low device performance resulting from the formation of defective interface layers during the gas stabilization process, a typical diborane-based PECVD process also suffers from low throughput. The PECVD process for p-aSi deposition is one of the major contributors to the overall cost of manufacturing an HJT solar cell relative to other processes. This is due to both the high overall operating expenses (OPEX) and the significant capital expenditure (CAPEX) associated with PECVD equipment. The high CAPEX further increases the effective OPEX due to higher depreciation/amortization-related costs. Additionally, PECVD equipment typically exhibits lower throughput compared to equipment used for other processes required in HJT solar cell manufacturing. As a result, the PECVD process for p-aSi deposition becomes one of the throughput-limiting processes within an HJT solar cell production line. To match the overall throughput of the production line, multiple PECVD process equipment may need to be installed so that the

total throughput of all PECVD equipment running in parallel equals the desired line throughput. Furthermore, the gas stabilization step can consume a significant portion of the total process time within the PECVD p-aSi deposition process. A longer gas stabilization step would consequently reduce the overall throughput of the PECVD process for p-aSi deposition. This has two negative impacts: firstly, for an existing production line, the lower PECVD process throughput increases the process cost per wafer, leading to a higher cost per watt ($/W). Secondly, for a new production line or a line expansion utilizing PECVD for p-aSi deposition, the total capital expenditure (CAPEX) required is higher due to the low throughput of existing processes.

[0012] In view of the foregoing, there is a desire to provide an improved method for forming boron-containing thin film which seeks to address at least one of the problems described hereinabove, or at least to provide an alternative solution.

SUMMARY

[0013] In one aspect of the present disclosure, a method of forming a boron-containing thin film is provided. The method comprises introducing a first precursor into a reaction chamber containing a substrate; subjecting the first precursor to a first gas stabilization step for a first duration; introducing a second precursor containing diborane into the reaction chamber; subjecting the second precursor to a second gas stabilization step for a second duration; and initiating a deposition process to form a boron-containing thin film on the substrate, wherein the second duration is shorter than the first duration.

[0014] In various embodiments, the second precursor comprises a mixture of diborane and the first precursor.

[0015] In various embodiments, the second gas stabilization step is performed for the second duration ranging from 0 to 5 seconds prior to initiating the deposition process.

[0016] In various embodiments, the first precursor may comprise a compound selected from the group consisting of silane (SiH_4), tungsten hexacarbonyl, diethylzinc, titanium tetraisopropoxide or other compounds for the deposition of silicon, silicon oxide, silicon carbide, other binary compounds of silicon, tertiary compounds of silicon, metal oxides, and metal nitrides.

BRIEF DESCRIPTION OF DRAWINGS

[0001] Various embodiments of the present disclosure are described hereinbelow in the detailed description with reference to the following drawings:

[0002] FIG. 1A is a flow diagram illustrating an exemplary prior art p-aSi deposition process using Plasma Enhanced Chemical Vapor Deposition (PECVD) and trimethylborane (TMB) as the dopant precursor gas.

[0003] FIG. 1B is a flow diagram illustrating an exemplary prior art p-aSi deposition process using PECVD and diborane as the dopant precursor gas.

[0004] FIG. 2 is a graph illustrating the process cost analysis of the exemplary prior art p-aSi deposition processes depicted in FIG. 1A and FIG. 1B, where dopant precursor gases TMB and diborane are used individually.

[0005] FIG. 3 is a schematic diagram illustrating the structure of an exemplary prior art of a conventional HJT solar cell.

[0006] FIG. 4 is a flow diagram illustrating an exemplary prior art of a conventional PECVD deposition process.

[0007] FIG. 5 is a flow diagram illustrating an exemplary prior art of a conventional PECVD deposition process using diborane as the dopant precursor for the deposition of a p-aSi layer.

[0008] FIG. 6 is a schematic diagram illustrating the structure of an exemplary prior art of a conventional HJT solar cell with a defective interface layer (601).

[0009] FIG. 7 is a flow diagram illustrating a method of forming a boron-containing thin film in accordance with some embodiments of the present disclosure.

[0010] FIG. 8 is a flow diagram illustrating a PECVD deposition process using diborane as the dopant precursor for the deposition of a p-aSi layer in accordance with some embodiments of the present disclosure.

[0011] FIG. 9 is a schematic diagram illustrating the structure of a silicon HJT solar cell

device fabricated using the method in accordance with an embodiment of the present disclosure.

[0012] FIG. 10 is a schematic diagram illustrating the structure of an aSi solar cell device fabricated using the method in accordance with an embodiment of the present disclosure.

[0013] FIG. 11 is a schematic diagram illustrating the structure of an N-i-p aSi photodetector fabricated using the method in accordance with an embodiment of the present disclosure.

[0014] FIG. 12 is a schematic diagram illustrating the structure of an N-i-p aSi LED device fabricated using the method in accordance with an embodiment of the present disclosure.

[0015] FIG. 13 is a schematic diagram illustrating the structure of an N-i-p aSi temperature sensor fabricated using the method in accordance with an embodiment of the present disclosure.

[0016] FIG. 14 is a schematic diagram illustrating the structure of an N-i-p aSi thin-film transistor fabricated using the method in accordance with an embodiment of the present disclosure.

[0017] FIG. 15 is a graph showing the defect levels in boron-doped films at different exposure doses of diborane (B_2H_6) before plasma ignition using the method in accordance with an embodiment of the present disclosure. The results show that performance decreases as the total volume of diborane exposure increases. The dark spots in the photoluminescence (PL) images indicate defects.

[0018] FIG. 16 is a graph showing the defect levels in boron-doped films at different exposure durations of diborane (B_2H_6) before plasma ignition using the method in accordance with an embodiment of the present disclosure. The results show that performance decreases as the duration of diborane exposure before plasma ignition increases. The dark spots in the photoluminescence (PL) images indicate defects.

[0019] FIG. 17 is a graph showing the defect levels in boron-doped films at different gas flow rates of diborane (B_2H_6) using the method in accordance with an embodiment of the present disclosure. The results show that performance decreases as gas flow rate increases.

The dark spots in the photoluminescence (PL) images indicate defects.

[0020] FIG. 18A is a schematic diagram of the structure of a finished solar cell fabricated using an exemplary prior art conventional method where a defective interface (181) between the i-aSi and p-aSi layers is formed.

[0021] FIG. 18B is a schematic diagram of the structure of a finished solar cell fabricated using the method in accordance with an embodiment of the present disclosure where no defective interface is formed.

[0022] FIG. 19 is a figure illustrating the solar cell device performance (efficiency) and the photoluminescence (PL) images of the finished solar cells using the conventional method (with an efficiency of 17.85%) and the method of the present disclosure (with an efficiency of 21.51%).

[0023] FIG. 20 is a schematic diagram illustrating the fabrication process of a wafer-based finished device (such as an HJT solar cell) using the method in accordance with an embodiment of the present disclosure.

[0024] FIG. 21 is a schematic diagram illustrating the fabrication process of an aSi solar cell (on glass) using the method in accordance with an embodiment of the present disclosure.

[0025] FIG. 22 is a schematic diagram illustrating the fabrication process of a solar cell with a Si/i-aSi/p-doped layer stack using the method in accordance with an embodiment of the present disclosure.

[0026] FIG. 23 is a schematic diagram illustrating the fabrication process of an HJT solar cell with an i/p stack, using p-type silicon-based layer as the hole-selective layer, deposited using the method in accordance with an embodiment of the present disclosure.

[0027] FIG. 24 is a schematic diagram illustrating the fabrication process of an HJT solar cell comprising metal oxide (MO) as a hole-selective layer, deposited using the method in accordance with an embodiment of the present disclosure.

[0028] FIG. 25 is a schematic diagram illustrating the fabrication process of a transition metal oxide, TMO/HJT solar cell, fabricated using the diborane-based deposition process in

accordance with an embodiment of the present disclosure.

[0029] FIG. 26 is a schematic diagram illustrating the fabrication process of an aSi solar cell deposited on glass, fabricated using the method in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0030] Reference throughout this specification to "one embodiment", "another embodiment" or "an embodiment" (or the like) means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearance of the phrases "in one embodiment" or "in an embodiment" or the like in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the described features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. In the following description, numerous specific details are provided to give a thorough understanding of embodiments. One skilled in the relevant art will recognize that the various embodiments be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, some or all known structures, materials, or operations may not be shown or described in detail to avoid obfuscation.

[0031] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments. As used herein, the singular 'a' and 'an' may be construed as including the plural "one or more" unless apparent from the context to be otherwise.

[0032] The terms "about" and "approximately" as applied to a stated numeric value encompass the exact value and a reasonable variance as will be understood by one of ordinary skill in the art, and the terms "generally" and "substantially" are to be understood in a similar manner, unless otherwise specified.

[0033] The present disclosure relates to a method of forming a boron-containing thin film using diborane (B_2H_6) as the dopant gas precursor. The method comprises steps which reduce the duration of exposure of diborane to a substrate or a pre-existing layer on a

substrate, thereby avoiding the formation of a defective interface layer prior to the deposition process. The method of the present disclosure can be applied to any thin-film devices that require i-aSi deposition, followed by deposition of boron doped p-aSi layer on the i-aSi deposition. Such devices will benefit from the several advantages of the present disclosure which include improved device performance, lower gas consumption rate, lower cost of precursors, lower overall operating cost (OPEX) which leads to higher throughput and more cost-effective for large-scale manufacturing of devices that employ the method of the present disclosure for forming boron-containing thin film within the devices.

[0034] FIG. 7 illustrates a general process flow for forming a boron-containing thin film in accordance with some embodiments of the present disclosure. The method comprises the steps of introducing a first precursor into a reaction chamber containing a substrate (702); subjecting the first precursor to a first gas stabilization step for a first duration (704); introducing a second precursor containing diborane into the reaction chamber (706); subjecting the second precursor to a second gas stabilization step for a second duration (708); and initiating a deposition process (710) to form a boron-containing thin film on the substrate (712), wherein the second duration is shorter than the first duration.

[0035] Prior to introducing the first precursor into the reaction chamber, other steps (701) may be involved, such as the deposition of other layers. For example, a-Si layer, i-aSi layer or other layers may be deposited depending on the applications and devices that are to be fabricated. In some embodiments, the method of the present disclosure is applied to existing thin or thick film layer for fabricating a new device or it can be applied to pre-existing thin or thick film layer of an existing device. In some embodiments, the existing or pre-existing thin or thick film layer is an intrinsic amorphous silicon layer (i-aSi).

[0036] During the first gas stabilization step, the substrate is exposed to the first precursor in the reaction chamber for the first duration. During the second gas stabilization step, the substrate is exposed to the second precursor for the second duration prior to the step of initiating the deposition process. The second duration is generally shorter than the first duration. In some embodiments, the second duration ranges from 0 to 5 seconds, 1 to 5 seconds, 2 to 5 seconds, 3 to 5 seconds, 0 to 3 seconds, or 1 to 3 seconds. In some embodiments, the first duration may vary from 1 to 3 mins.

[0037] In some embodiments, the second precursor containing the diborane has an exposure dose of 0 to 1 mbar·cm^{-3} prior to initiating the deposition process. In some embodiments, the second precursor containing the diborane has an exposure dose of 0 to 0.6 mbar·cm^{-3} prior to initiating the deposition process.

[0038] In some embodiments, the second precursor containing the diborane has a gas flow rate of not more than 0.5 sccm prior to initiating the deposition process. In some embodiments, the gas flow rate is not more than 0.3 sccm when the second precursor containing the diborane has an exposure dose of about 1.6 mbar·cm^{-3} for an exposure of about 3 seconds.

[0039] In some embodiments, the second precursor containing the diborane may comprise a mixture of diborane and the first precursor. In some embodiments, the second precursor may include hydrogen.

[0040] Although the method of the present disclosure described herein comprises a two-step gas stabilization process, one skilled in the art will appreciate that more than two gas stabilization steps may be employed as appropriate without departing from the scope of the present disclosure. In the embodiments where more than two gas stabilization steps are employed, the last gas stabilization step will be the step that involves stabilizing the precursor containing the diborane. This step will be carried out for a duration ranging from 0 to 5 seconds, 1 to 5 seconds, 2 to 5 seconds, 3 to 5 seconds, 0 to 3 seconds, or 1 to 3 seconds to minimize the exposure of the substrate, any layers on the substrate, and/or any pre-existing layers, to the diborane. The last gas stabilization step should be the step that immediately precedes the step of initiating a deposition process.

[0041] According to some embodiments of the present disclosure, the first precursor may contain silane (SiH_4), tungsten hexacarbonyl, diethylzinc, titanium tetraisopropoxide or other precursors for the deposition of silicon, silicon oxide, silicon carbide, other binary compounds of silicon, tertiary compounds of silicon, metal oxide, or metal nitride. In an exemplary embodiment, the first precursor is silane (SiH_4), and the second precursor is a mixture containing diborane and the first precursor, silane (SiH_4).

[0042] Referring to FIG. 7, during the deposition process, the first precursor contributes to

the deposition of the thin film (711), while the second precursor provides the boron dopant which facilitates boron doping into the thin film in situ (713), resulting in the boron-containing thin film (or layer). After the deposition of the boron-containing thin film on the substrate, other steps (715) may be involved to complete the deposition process and/or to complete the device fabrication.

[0043] In some embodiments, the boron-containing thin film can be in amorphous form. In other embodiments, the boron-containing thin film can be in crystalline form with varying degrees of crystallinity, such as nanocrystalline (nc-Si) form, microcrystalline Si form (μc-Si), etc. The boron-containing thin film formed by the method the present invention may comprise silicon, silicon oxide, silicon carbide, other binary compounds of silicon, tertiary compounds of silicon, metal oxides, or metal nitrides, depending on the type of first precursor that is used. Boron incorporation into such material occurs in situ during the deposition process.

[0044] In some embodiments, the boron-containing thin film has a thickness ranging from 1 nm to 3 μm. The boron-containing thin film can be formed in the form of a homogenous layer, a graded composition layer, or a layer stack with the boron-containing layer deposited first.

[0045] In various embodiments, the substrate can be a silicon wafer, glass, polymer, plastic, flexible substrate, metal sheet, or other suitable materials. In some embodiments, the substrate may comprise one or more pre-existing intrinsic amorphous silicon (i-aSi) layers onto which the boron-containing thin film is deposited or formed. The i-aSi layer can be a thin layer having a thickness of less than 15nm or it can be a thick layer having a thickness of more than 15nm. In some embodiments, the one or more pre-existing intrinsic amorphous silicon (i-aSi) layers can be grown using one of the methods selected from the group consisting of PECVD, APCVD, low-pressure chemical vapor deposition (LPCVD), sputtering and evaporation.

[0046] The method of the present disclosure can be adapted for use with various deposition processes to fabricate different devices, where boron-doped layer is to be deposited. In particular, the method of the present disclosure can be applied to any thin-film devices that require i-aSi deposition, followed by the deposition of a boron-doped p-aSi layer on the i-

aSi layer. The deposition process can be performed by one of the methods including plasma-enhanced chemical vapor deposition (PECVD), atmospheric pressure chemical vapor deposition (APCVD) or atomic layer deposition (ALD).

[0047] An exemplary embodiment is described herein to illustrate the use of PECVD for forming the boron-containing thin film in accordance with the method of the present disclosure. FIG. 8 illustrates a process flow of a PECVD deposition process using diborane as the dopant precursor for p-aSi layer deposition according to some embodiments of the present disclosure. In the exemplary embodiment, a first precursor is introduced into the reaction chamber containing a substrate with an i-aSi layer (802). In this embodiment, the first precursor contains silane (SiH_4). The first precursor is then subjected to a first gas stabilization step for a first duration (804). This is followed by the introduction of a second precursor into the reaction chamber (806). In this embodiment, the second precursor may contain a mixture of diborane and the first precursor, SiH_4. The second precursor is subjected to a second gas stabilization step for a second duration (808). At the end of the second duration, a deposition process is initiated by igniting plasma in the reaction chamber (810). This involves exposing the substrate surface to plasma to ignite a surface reaction between the first precursor, the second precursor, with the substrate surface to form the boron-containing thin film. The deposition process comprises depositing a thin film comprising silane (SiH_4) (811) and doping boron into the thin film (813) to form the boron-doped p-aSi layer on the i-aSi layer (812) on the substrate.

[0048] During the second gas stabilization step, the substrate comprising the i-aSi layer is exposed to the second precursor for the second duration prior to the step of initiating the plasma ignition. The second duration is generally shorter than the first duration, and in some embodiments, the second duration ranges from 0 to 5 seconds, 1 to 5 seconds, 2 to 5 seconds, 3 to 5 seconds, 0 to 3 seconds, or 1 to 3 seconds. Due to the short exposure time of diborane to the i-aSi layer during the second stabilization step just before plasma ignition, the formation of a defective interface layer between the i-aSi layer and the p-aSi layer is avoided. This results in an improved performance of the device compared to conventional methods where a defective interface exists. As mentioned hereinabove, the method of the present disclosure can be applied to any thin film devices that require the deposition of a layer such as an i-aSi layer, followed by the deposition of a boron-doped layer, such as a p-aSi layer.

Such devices include Type 1 devices which include semiconductor-based devices that utilize very thin i-aSi layers (less than 15nm) grown on a semiconducting substrate (e.g. silicon) that require good passivation of the surface of the semiconducting substrate (e.g. well-passivated Si in the areas where the Si/i-aSi/p-aSi stack is formed). Some examples of Type 1 devices include silicon-wafer-based photovoltaic devices, silicon-wafer-based diodes, and silicon-wafer-based thin-film transistors.

[0049] Type 2 devices include semiconductor-based devices that utilize thick i-aSi layers (more than 15nm) and require well-passivated i-aSi in the areas where the i-aSi/p-aSi interface exists. These are usually grown on glass or flexible (plastic/polymer) substrates or on metallic substrates. Some examples of Type 2 devices include photovoltaic cells using glass or flexible substrates, photodetectors, light-emitting diodes (LEDs), and thin-film transistors (TFTs).

[0050] Examples of some of the relevant devices benefiting from the present disclosure are illustrated in FIGS. 9 to 14. The devices include: (1) photovoltaic devices such as silicon HJT solar cell (FIG. 9), and aSi solar cell (FIG. 10); (2) diode-based devices such as N-i-p aSi photodetectors (FIG. 11), N-i-p aSi LEDs (FIG. 12), N-i-p aSi temperature sensors (FIG. 13); and (3) thin-film transistor (TFT) devices such as PNP aSi thin-film transistors (FIG. 14).

[0051] In particular, FIG. 9 depicts a schematic diagram of a photovoltaic device, such as a silicon HJT solar cell (900), with a p-type doped amorphous silicon layer (p-aSi) deposited in accordance with an embodiment of the method of the present disclosure.

[0052] FIG. 10 depicts a schematic diagram of a photovoltaic device, such as aSi solar cell (100) with a p-type doped amorphous silicon layer (p-aSi) deposited in accordance with an embodiment of the method of the present disclosure.

[0053] FIG. 11 depicts a schematic diagram of a n-i-p aSi diode-based device, such as a n-i-p aSi photodetector (110) with a p-type doped amorphous silicon layer (p-aSi) deposited in accordance with an embodiment of the method of the present disclosure.

[0054] FIG. 12 depicts a schematic diagram of a n-i-p aSi diode-based device, such as a n-i-p aSi LED (120) with a p-type doped amorphous silicon layer (p-aSi) deposited in

accordance with an embodiment of the method of the present disclosure.

[0055] FIG. 13 depicts a schematic diagram of a n-i-p aSi diode-based device, such as a n-i-p aSi temperature sensor (130) with a p-type doped amorphous silicon layer (p-aSi) deposited in accordance with an embodiment of the method of the present disclosure.

[0056] FIG. 14 depicts a schematic diagram of a thin-film transistor (TFT) device using i/p aSi stack (P-N-P a-Si thin-film transistor) (140) with a p-type doped amorphous silicon layer (p-aSi) deposited in accordance with an embodiment of the method of the present disclosure.

[0057] The Examples section below details the specific devices and their corresponding fabrication methods that benefit from the method described in the present disclosure.

[0058] The method described in the present disclosure eliminates the presence of a defective interface, resulting in improved performance compared to conventional methods known in the state of the art, where such a defective interface exists. This improvement in device performance significantly reduces the production costs ($/W). The method of the present disclosure can be applied to other devices, such as semiconductor devices, solar cells, diodes, and thin-film transistors, where similar issues such as the formation of a defective interface layer exist. Consequently, the method enhances the performance of all such devices.

[0059] The method of the present disclosure requires a relatively short gas stabilization time, ranging from 0 to 5 seconds, or 0 to 3 seconds. This reduces the overall process time for PECVD-based p-aSi deposition. This results in higher throughput for the PECVD process overall, offering several benefits.

[0060] Firstly, for existing production lines, the higher throughput of the method of the present disclosure leads to lower operating expenses (OPEX) due to reduced consumption of consumables such as gas and electricity, etc. for the same output. This decrease in production cost translates to lower overall costs per watt ($/W) for HJT solar cells.

[0061] Secondly, for new production lines or the expansion of existing ones, the improved throughput can reduce the number of new PECVD tools required to achieve a desired overall production line throughput when using the new process. Since PECVD tools are among the more expensive machines relative to other equipment, the higher-throughput new process,

requiring fewer tools for a given throughput, leads to a reduction in capital expenditures (CAPEX).

[0062] Thirdly, for new production lines utilizing the improved throughput and new process, the savings in capital expenditures (CAPEX) further reduces the amortization/depreciation-related costs and delivers further reductions in overall operating expenses (OPEX). Similar issues and cost considerations exist in the manufacturing of semiconductor devices other than solar cells, such as diodes and thin-film transistors, where a boron-containing thin film is deposited over a pre-existing intrinsic amorphous silicon (i-aSi) layer. The present disclosure has the potential of reducing manufacturing costs for all such devices.

[0063] To facilitate a better understanding of the present disclosure, the following examples of specific embodiments are given. In no way should the following examples be read to limit or define the entire scope of the disclosure. One skilled in the art will recognize that the examples set out below are not an exhaustive list of the embodiments of this disclosure.

EXAMPLES

Example 1

[0064] Exposure Dose of Diborane

[0065] Some experiments were conducted to determine the exposure doses of diborane and the effects of using different exposure doses. The experiments began with the fabrication of solar cell devices containing boron-containing thin films, deposited in accordance with an embodiment of the method of the present disclosure. Various exposure doses of diborane were employed during the fabrication process. The implied open circuit voltage of the completed solar cell devices was measured using a Sinton measurement tool, and photoluminescence images of each device were captured using photoluminescence measurement tool. The doses of diborane employed in the fabrication of the solar cell devices were calculated by multiplying the diborane gas flow rate with the exposure time of diborane to the substrate (or the layer on the substrate where diborane was to be deposited).

[0066] FIG. 15 is a graph showing the defect levels in boron-doped films at different

exposure doses of diborane (B_2H_6) using the method of the present disclosure. The figure also presents the implied open circuit voltage of the finished device versus the dose of B_2H_6 before plasma ignition. Each data point represents a finished solar cell fabricated using a certain dose of diborane. Photoluminescence (PL) images of each finished solar cell are shown in the figure. The dark areas observed in the PL images indicate the presence of defective regions within the samples. It is evident that defect levels in boron-doped films increase with higher exposure doses of diborane. Consequently, the performance of the final device decreases as the total volume of diborane exposure increases. The desired range of the exposure dose of diborane ranges from 0 to 1 $mbar \cdot cm^{-3}$, and preferably from 0 to 0.6 $mbar \cdot cm^{-3}$.

Example 2

[0067] Exposure Duration of Diborane

[0068] Some experiments were conducted to determine the exposure durations of diborane and the effects of using different exposure durations. The experiments began with the fabrication of solar cell devices containing boron-containing thin films, deposited in accordance with an embodiment of the method of the present disclosure. Various exposure durations were employed during the fabrication process. The implied open circuit voltage of the completed solar cell devices was measured using a Sinton measurement tool, and photoluminescence images of each device were captured using photoluminescence measurement tools. The exposure duration was calculated as the duration of diborane gas flow before plasma ignition.

[0001] FIG. 16 is a graph showing the defect levels in boron-doped films at different exposure durations of diborane (B_2H_6) using the method of the present disclosure. The figure also presents the implied open circuit voltage of the finished device versus the duration of B_2H_6 flow before plasma ignition. Each data point represents a finished solar cell fabricated using specific flow duration of diborane. Schematic diagrams illustrating different durations of diborane exposure are provided and shown in the figure. The solid colour box represents the flow of SiH_4 only while the patterned box represents the mixture of SiH_4, diborane, and H_2. Photoluminescence images of each finished solar cell corresponding to the duration of diborane exposure are displayed. The dark areas observed in the PL images indicate the

presence of defective regions within the samples. It is evident that defect levels in boron-doped films increase with longer flow durations of diborane. Consequently, the performance of the final device decreases as the duration of diborane exposure before plasma ignition increases. The optimal range of the exposure duration of diborane ranges from 0 to 5 seconds. In a preferred embodiment, the exposure duration of diborane ranges from 0 to 3 seconds, when the flow rate of diborane is 0.16 sccm and at a pressure of 1.6 mbar.

Example 3

[0002] Gas Flow Rate of Diborane

[0003] Some experiments were conducted to determine the gas flow rates of diborane and the effects of using different gas flow rates. The experiments began with the fabrication of solar cell devices containing boron-containing thin films, deposited in accordance with an embodiment of the method of the present disclosure. Various flow rates of diborane were employed during the fabrication process. The implied open circuit voltage of the completed solar cell devices was measured using a Sinton measurement tool, and photoluminescence images of each device were captured using photoluminescence measurement tools. The gas flow rate was calculated by calculating the volume of diborane gas in standard cubic centimeter per minute.

[0004] FIG. 17 is a graph showing the defect levels in boron-doped films at different gas flow rates of diborane (B_2H_6) using the method of the present disclosure. The figure also presents the implied open circuit voltage of the finished device versus the gas flow rate of B_2H_6 before plasma ignition. Each data point represents a finished solar cell fabricated using specific flow rate of diborane. In the figure, photoluminescence images of each finished solar cell corresponding to the gas flow rate of diborane are displayed. The dark areas observed in the PL images indicate the presence of defective regions within the samples. It is evident that defect levels in boron-doped films increase with a greater flow rate of diborane. Consequently, the performance of the final device decreases as the flow rate of diborane increases. The gas flow rate of diborane is not more than 0.5 sccm. In a preferred embodiment, the gas flow rate of diborane is not more than 0.3 sccm, when the exposure duration of diborane is 3 seconds and at a pressure of 1.6 mbar.

Example 4

[0005] Application on solar cell

[0006] FIG. 18A and 18B compare the structures of finished solar cells fabricated using the conventional method (FIG. 18A) and the method of the present disclosure (FIG. 18B). The solar cell fabricated using the conventional method, as shown in FIG. 18A, leads to the formation of a defective interface between the i-aSi and the p-aSi layers (181). In contrast, the solar cell fabricated using the method of the present disclosure minimizes or eliminates such interfacial defect, as demonstrated in FIG. 18B, where no defective interface is observed.

[0007] FIG. 19 depicts the solar cell device performance (efficiency) and the photoluminescence images of the finished solar cells fabricated using the conventional method and the method of the present disclosure. Darker regions in the PL images correspond to areas with defects. As evident from the figure, the method of the present disclosure significantly reduces defect levels within the solar cell device, leading to an improved overall performance (21.51%) compared to the conventional method (17.85%), due to higher implied V_{oc}.

Example 5

[0008] Application on HJT solar cell using silicon wafer as the substrate

[0009] FIG. 20 is a schematic diagram illustrating the fabrication process of a wafer-based finished device, such as an HJT solar cell, using the method of the present disclosure. The process begins with a silicon wafer substrate (200) as the initial substrate. After several other processing steps (201), the silicon wafer substrate is textured, and other layers are deposited on one side (202). Then, an i-aSi deposition (203) is carried out to deposit an i-aSi layer on the other side (204). Following this, a p-aSi deposition is carried out using the method of the present disclosure (205) to deposit a p-aSi layer on the i-aSi layer (206). This is followed by other processes (207) including the deposition of an n-type amorphous silicon (n-aSi) layer, a transparent conducting oxide (TCO) layer, and metal contacts, resulting in a wafer-based finished device (208). This example demonstrates that no defective interface is formed between the i-aSi and the p-aSi layers when using the method of the present

disclosure to fabricate the wafer-based finished device.

Example 6

[0010] Application on solar cell using non-wafer substrate

[0011] FIG. 21 is a schematic diagram illustrating the fabrication process of a finished device such as an amorphous silicon (aSi) solar cell deposited on a glass, plastic, or other substrate, using the method of the present disclosure. The process begins with using a glass, plastic, or other substrate (210) as the initial substrate. After several other processing steps (211), other layers are deposited on one side of the substrate (212). Then, an i-aSi deposition (213) is carried out to deposit an i-aSi layer on the other layers (214). Following this, a p-aSi deposition is carried out using the method of the present disclosure (215) to deposit a p-aSi layer on the i-aSi layer (216). This is followed by the deposition of other layers and metal contacts (217), resulting in the finished device, which is the amorphous silicon (aSi) solar cell deposited on a substrate such as glass, plastic, or other substrate (218). This example demonstrates that no defective interface is formed between the i-aSi and the p-aSi layers when using the method of the present disclosure to fabricate the the amorphous silicon (aSi) solar cell.

Example 7

[0012] Application on solar cell with Si/i-aSi/p-doped layer stack

[0013] FIG. 22 is a schematic diagram illustrating the fabrication process of a solar cell with Si/i-aSi/p-doped layer stack, using the method of the present disclosure. The process begins with an n-type Si substrate (220) as the initial substrate. After several other processing steps (221), the n-type Si substrate (220a) is textured and cleaned, and an i-aSi deposition (222) is carried out to deposit an i-aSi layer on one side (223). Then, deposition of other layers (224) are carried out to deposit other layers (225) on the other side. Following this, a p-aSi layer deposition is carried out using the method of the present disclosure (226) to deposit a p-aSi layer on the i-aSi layer (227). This is followed by the deposition of other layers (228) on the other layers, resulting in a solar cell with a Si/i-aSi/p-doped layer stack (229). This example demonstrates that no defective interface is formed between the i-aSi and the p-aSi layers when using the method of the present disclosure to fabricate the solar cell with a Si/i-

aSi/p-doped layer stack.

Example 8

[0014] Application on HJT solar cell with i/p stack

[0015] FIG. 23 is a schematic diagram illustrating the fabrication process of an HJT solar cell with an i/p stack using the method of the present disclosure. The process begins with an n-type Si substrate (230) as the initial substrate. After texturing and cleaning steps (231), the n-type Si substrate (230a) then undergoes a first i-aSi deposition process (232) where a first i-aSi layer is deposited on one side (233) of the substrate. A second i-aSi deposition and an n-aSi deposition are carried out (234) to deposit a second i-aSi layer and an n-aSi layer on the other side of the substrate (235). Following this, a p-type silicon-based layer deposition is carried out using the method of the present disclosure (236) to deposit a p-aSi layer on the first i-aSi layer (237). Then TCO layers are deposited on both sides of the substrate (238). This is followed by metallization, where metal contacts are fabricated on both sides of the substrate, resulting in an HJT solar cell with an i/p stack (239). The p-type silicon-based layer formed in this embodiment includes a layer in amorphous (aSi) form, nano-crystalline (nc-Si) form, or microcrystalline Si (μc-Si) form. Examples of such layers include a-SiOx, a-SiCx, nc-SiOx, nc-SiCx, μc-SiOx, μc-SiCx, etc. This example demonstrates that no defective interface is formed between the i-aSi and the p-aSi layers when using the method of the present disclosure to fabricate the HJT solar cell with i/p stack.

Example 9

[0016] Application on HJT solar cell with metal oxide

[0017] FIG. 24 is a schematic diagram illustrating the fabrication process of an HJT solar cell comprising metal oxide (MO) as the hole-selective layer (MO/HJT solar cell). The process uses the method of the present disclosure where the MO may grow with diborane as an in-situ dopant gas such as B:WO_x, B:ZnO_x, B:MoO_x, B:VO_x, B:NiO_x, B:TiO_x, B:SnO_x, etc.. The process begins with a n-type Si substrate (240) as the initial substrate. After texturing and cleaning steps (241), the n-type Si substrate (240a) then undergoes a first i-aSi deposition process (242) where a first i-aSi layer is deposited on one side (243) of the substrate. A second i-aSi deposition and an n-aSi deposition are carried out (244) to deposit

a second i-aSi layer and an n-aSi layer on the other side of the substrate (245). Following this, a p-doped metal oxide deposition is carried out using the method of the present disclosure (246) to deposit a p-MO layer on the first i-aSi layer (247). Then TCO layers are deposited on both sides of the substrate (248). This is followed by metallization, where metal contacts are fabricated on both sides of the substrate, resulting in a MO/HJT solar cell (249). This example demonstrates that no defective interface is formed between the i-aSi and the p-MO layers when using the method of the present disclosure to fabricate the MO/HJT solar cell.

Example 10

[0018] Fabrication of TMO/HJT solar cell with diborane-based thin film

[0019] FIG. 25 is a schematic diagram illustrating the fabrication process of a TMO/HJT solar cell using the method of the present disclosure. The process begins with a silicon wafer substrate (250) as the initial substrate. After several other processing steps (251), the silicon wafer substrate is textured and cleaned, and other layers are deposited on one side of the substrate (252). Then, an i-aSi deposition (253) is carried out to deposit an i-aSi layer on the other side of the substrate (254). Following this, a p-aSi deposition is carried out using the method of the present disclosure (255) to deposit a boron-doped layer (such as B:WO_x, B:ZnO_x, or other materials) on the i-aSi layer (256). This is followed by the deposition of other layers including n-type aSi layer, a second i-aSi layer, transparent conducting oxide (TCO) layers, and metal contacts, resulting in the TMO/HJT solar cell (257) fabricated using a diborane-based process in accordance with an embodiment of the present disclosure. This example demonstrates that no defective interface is formed between the i-aSi layer and the boron-doped layer when using the method of the present disclosure to fabricate the TMO/HJT solar cell.

Example 11

[0020] Application on aSi solar cell deposited on glass

[0021] FIG. 26 is a schematic diagram illustrating the fabrication process of an amorphous silicon (aSi) solar cell deposited on a glass substrate using the method of the present disclosure. The process begins with providing a glass (260) as the initial substrate. After

several other processing steps (261), other layers are deposited on one side of the glass substrate (262). An i-aSi deposition (263) is carried out to deposit an i-aSi layer on the same side of the glass substrate (264). Following this, a p-aSi deposition is carried out using the method of the present disclosure (265) to deposit a p-aSi layer on the i-aSi layer (266). This is followed by the deposition of other layers (267) including an n-aSi layer, a front contact layer and metal contacts, resulting in the aSi solar cell deposited on glass. This example demonstrates that no defective interface is formed between the i-aSi layer and the p-aSi layer when using the method of the present disclosure to fabricate the aSi solar cell on glass.

[0022] Besides the devices and fabrication processes described hereinabove, other i-p aSi diode-based devices, other i-p aSi TFT-based devices, and any other devices using i-aSi layer followed by PECVD, APCVD or ALD deposition involving diborane precursor gas can benefit from the present disclosure. The fabrication methods of other i-p aSi diode-based devices, other i-p aSi TFT-based devices, and any other devices using i-aSi layer followed by PECVD, APCVD or ALD deposition involving diborane precursor gas can also benefit from the present disclosure.

[0023] Although embodiments of the invention have been shown and described, the invention is not limited to the described embodiments. Instead, it would be appreciated by those skilled in the art that various modifications and variations can be made to the embodiments of the invention without departing from the scope of the invention, the scoop of which is set forth in the following claims.

CLAIMS

1. A method of forming a boron-containing thin film, the method comprising:
introducing a first precursor into a reaction chamber containing a substrate;
subjecting the first precursor to a first gas stabilization step for a first duration;
introducing a second precursor containing diborane into the reaction chamber;
subjecting the second precursor to a second gas stabilization step for a second duration; and
initiating a deposition process to form a boron-containing thin film on the substrate,
wherein the second duration is shorter than the first duration.

2. The method according to claim 1, wherein the second precursor comprises a mixture of diborane and the first precursor.

3. The method according to claim 1 or 2, wherein the substrate is exposed to the second precursor during the second gas stabilization step for the second duration prior to initiating the deposition process, wherein the second duration ranges from 0 to 5 seconds.

4. The method according to claim 1 or 2, wherein the second precursor has an exposure dose of 0 to 1 $mbar \cdot cm^{-3}$ prior to initiating the deposition process.

5. The method according to claim 1 or 2, wherein the second precursor has a gas flow rate of not more than 0.5 sccm prior to initiating the deposition process.

6. The method according to claim 1 or 2, wherein the deposition process comprises depositing a thin film and doping boron from the second precursor into the thin film to form the boron-containing thin film.

7. The method according to claim 1, wherein the boron-containing thin film is in amorphous form or crystalline form.

8. The method according to claim 1, wherein the boron-containing thin film has a thickness ranging from 1 nm to 3 μm.

9. The method according to claim 1, wherein the boron-containing thin film is in the form of a homogenous layer, a graded composition layer, or a layer stack with the boron-containing thin film deposited first.

10. The method according to claim 1, wherein the boron-containing thin film is composed of a material selected from the group consisting of silicon, silicon oxide, silicon carbide, other binary compounds of silicon, tertiary compounds of silicon, metal oxides, and metal nitrides.

11. The method according to claim 1, wherein the deposition process is performed via one of the methods selected from plasma-enhanced chemical vapor deposition, atmospheric pressure chemical vapor deposition or atomic layer deposition.

12. The method according to claim 1, wherein the deposition process is initiated by exposing the substrate surface to plasma, to ignite a surface reaction between the first precursor, the second precursor with the substrate surface to form the boron-containing thin film.

13. The method according to claim 1, wherein the substrate comprises one or more pre-existing intrinsic amorphous silicon (i-aSi) layers.

14. The method according to claim 13, wherein at least one of the pre-existing intrinsic amorphous silicon layers is a thin layer having a thickness of less than 15 nm.

15. The method according to claim 13, wherein at least one of the pre-existing intrinsic amorphous silicon layers is a thick layer having a thickness of more than 15 nm.

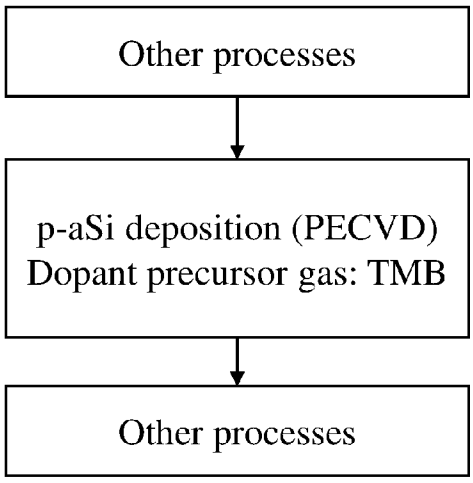
16. The method according to claim 13, wherein the boron-containing thin film is a p-type amorphous silicon (p-aSi) layer.

17. The method according to claim 14, wherein the boron-containing thin film is a p-

type amorphous silicon (p-aSi) layer deposited on at least one of the pre-existing intrinsic amorphous silicon layers having the thickness of less than 15 nm.

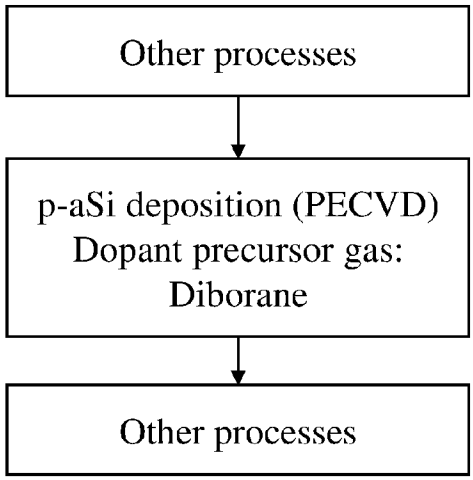
18. The method according to claim 15, wherein the boron-containing thin film is a p-type amorphous silicon (p-aSi) layer deposited on the at least one of the pre-existing intrinsic amorphous silicon layers having the thickness of more than 15 nm.

19. The method according to claim 13, wherein the one or more pre-existing intrinsic amorphous silicon layers are grown using one of the methods selected from the group consisting of plasma enhanced chemical vapor deposition, atmospheric pressure chemical vapor deposition, low-pressure chemical vapor deposition, sputtering and evaporation.



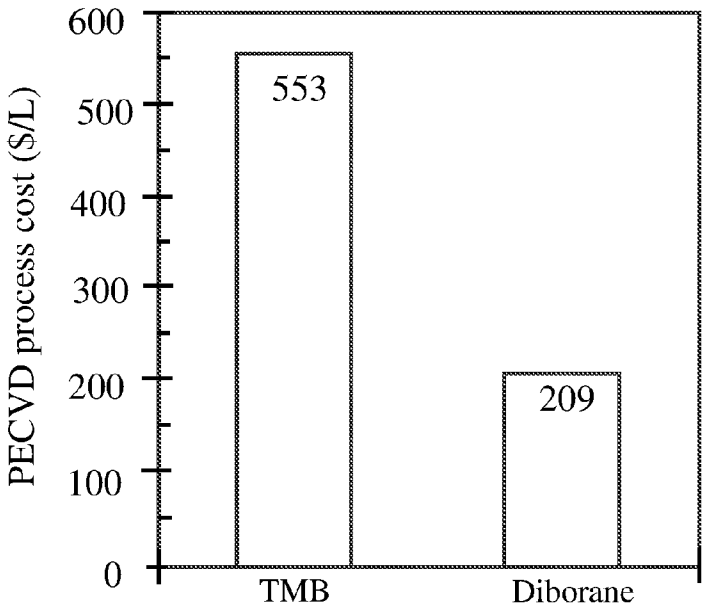
(Prior Art)

FIG. 1A



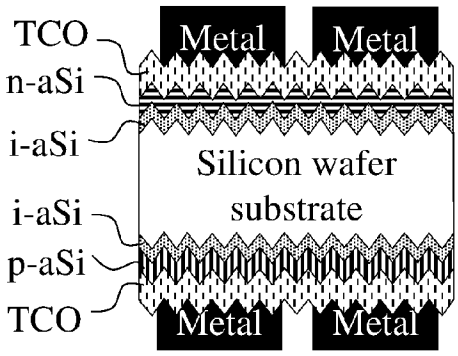
(Prior Art)

FIG. 1B



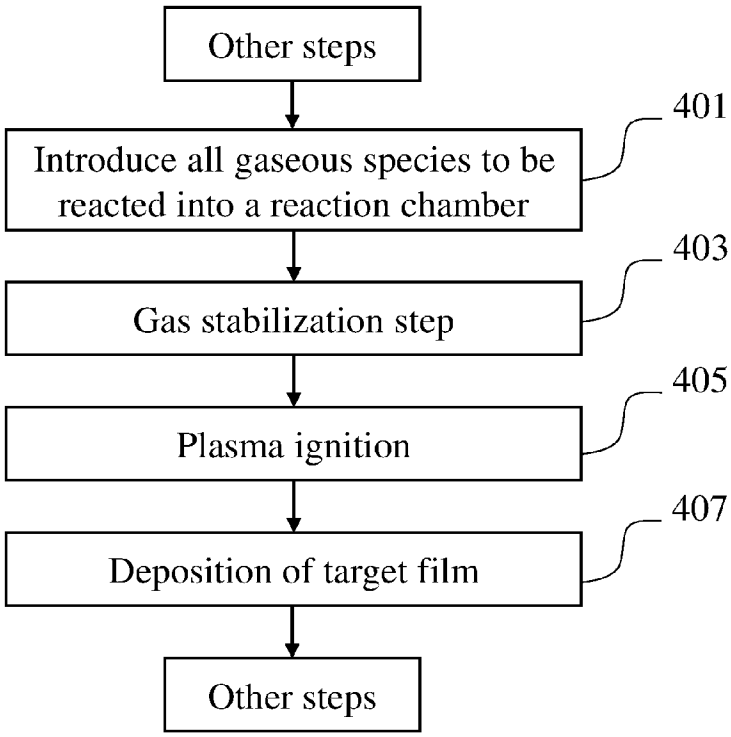
(Prior Art)

FIG. 2



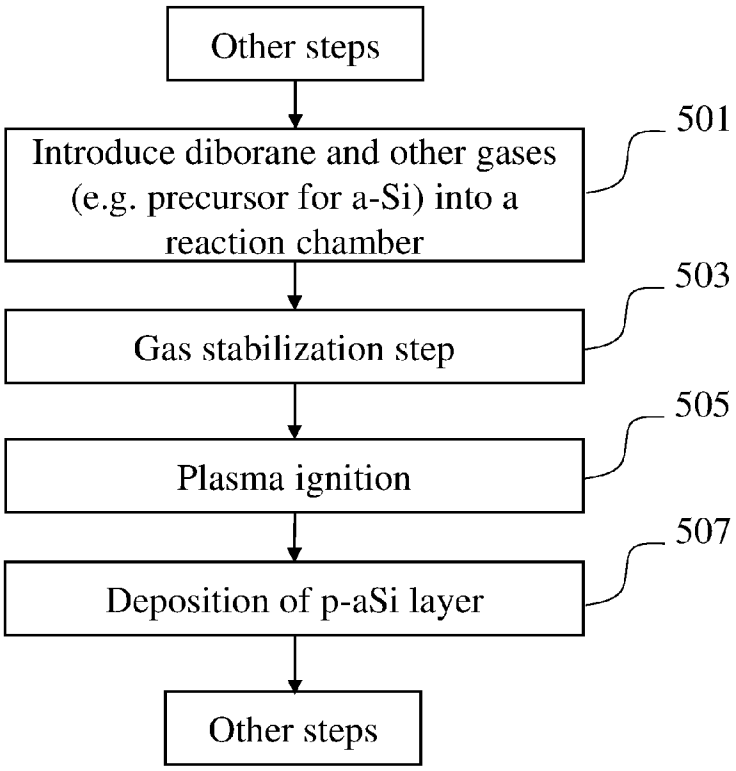
(Prior Art)

FIG. 3



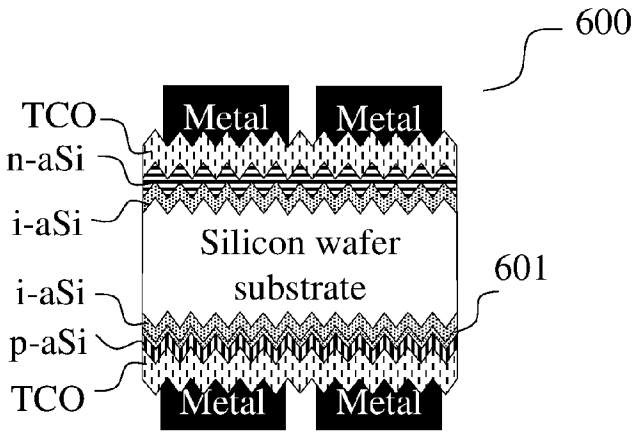
(Prior Art)

FIG. 4



(Prior Art)

FIG. 5



(Prior Art)

FIG. 6

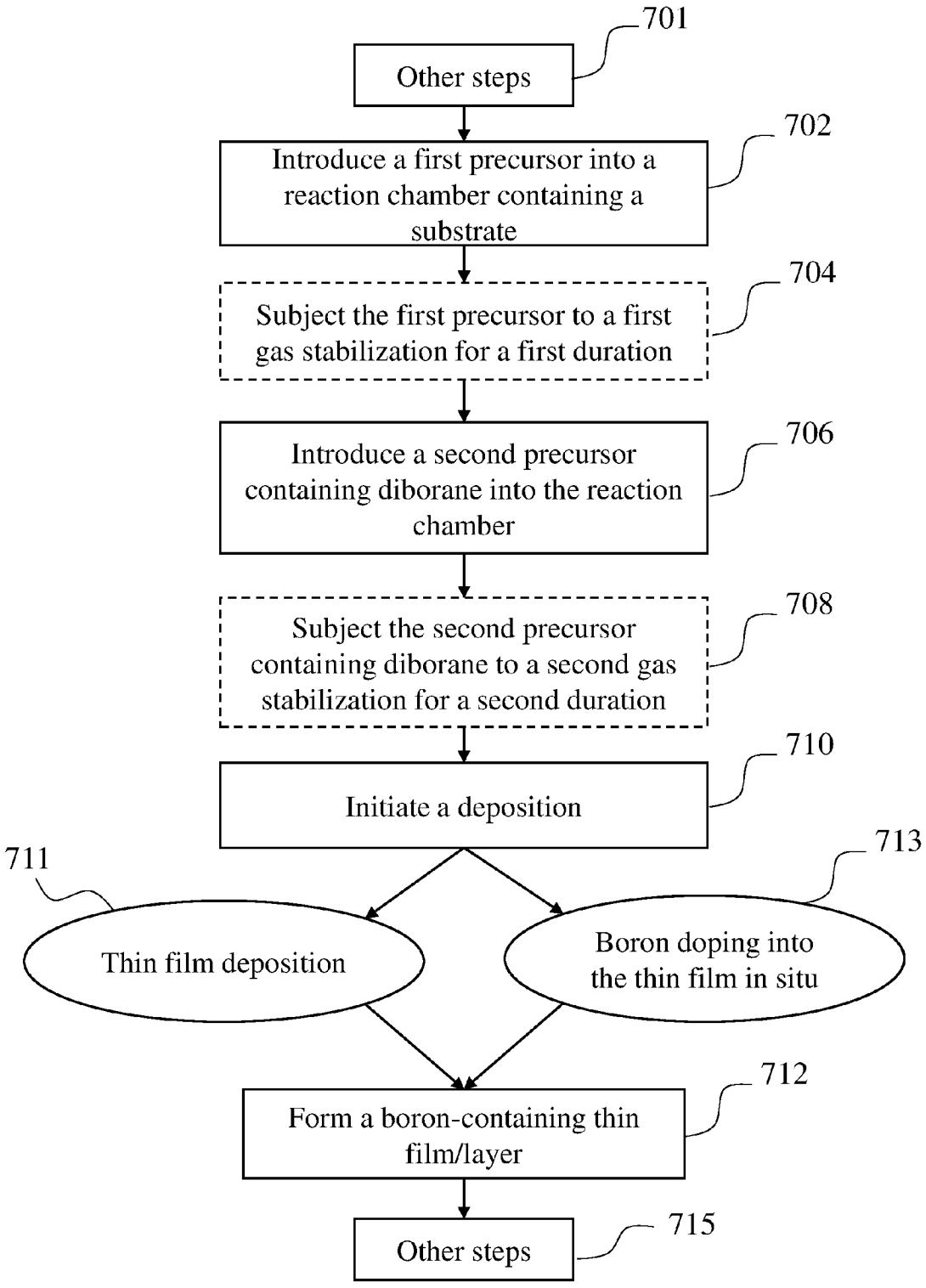

701
Other steps
702
Introduce a first precursor into a reaction chamber containing a substrate
704
Subject the first precursor to a first gas stabilization for a first duration
706
Introduce a second precursor containing diborane into the reaction chamber
708
Subject the second precursor containing diborane to a second gas stabilization for a second duration
710
Initiate a deposition
711
Thin film deposition
713
Boron doping into the thin film in situ
712
Form a boron-containing thin film/layer
715
Other steps

FIG. 7

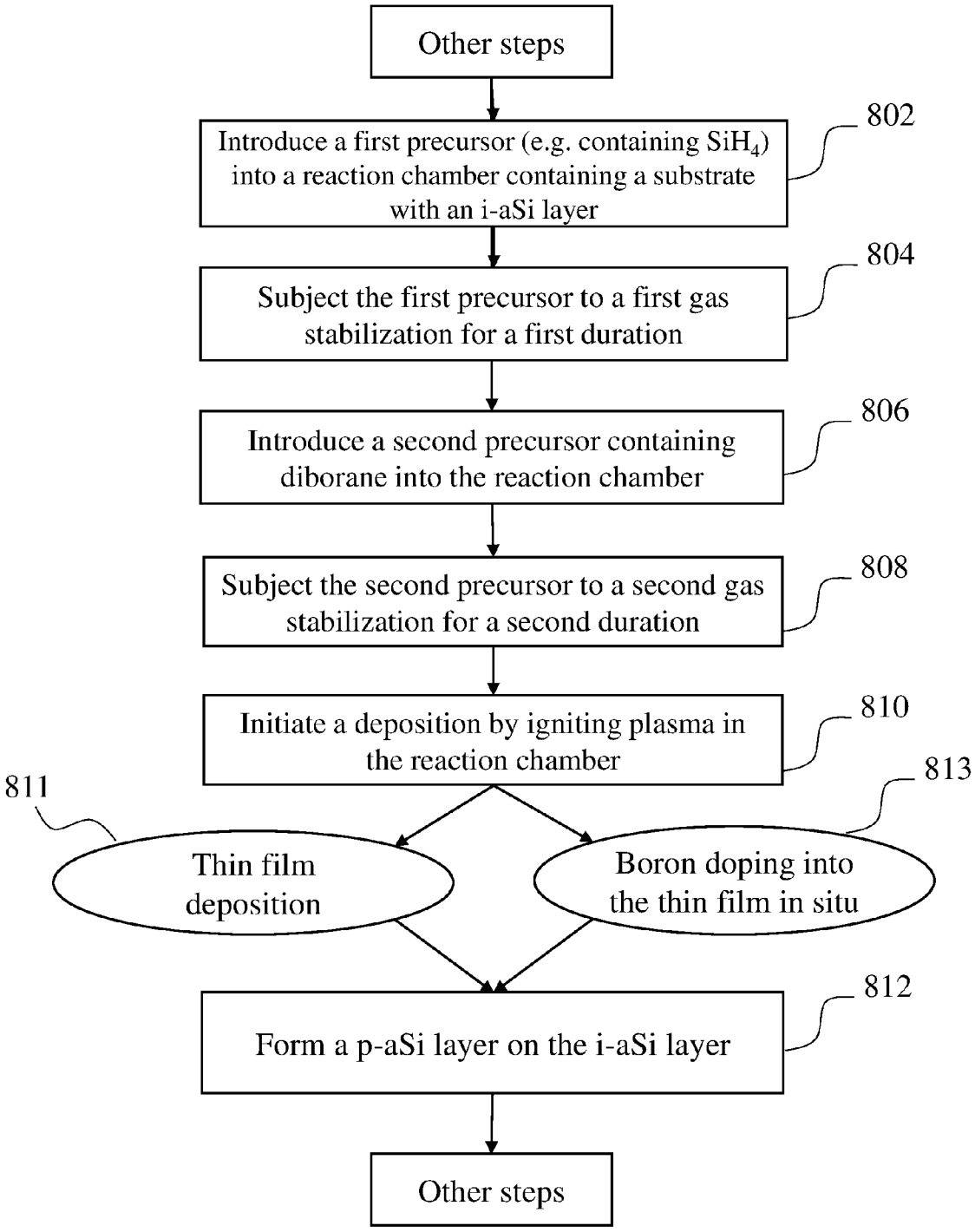

Other steps
Introduce a first precursor (e.g. containing SiH_4) into a reaction chamber containing a substrate with an i-aSi layer
802
Subject the first precursor to a first gas stabilization for a first duration
804
Introduce a second precursor containing diborane into the reaction chamber
806
Subject the second precursor to a second gas stabilization for a second duration
808
Initiate a deposition by igniting plasma in the reaction chamber
810
811
Thin film deposition
813
Boron doping into the thin film in situ
Form a p-aSi layer on the i-aSi layer
812
Other steps

FIG. 8

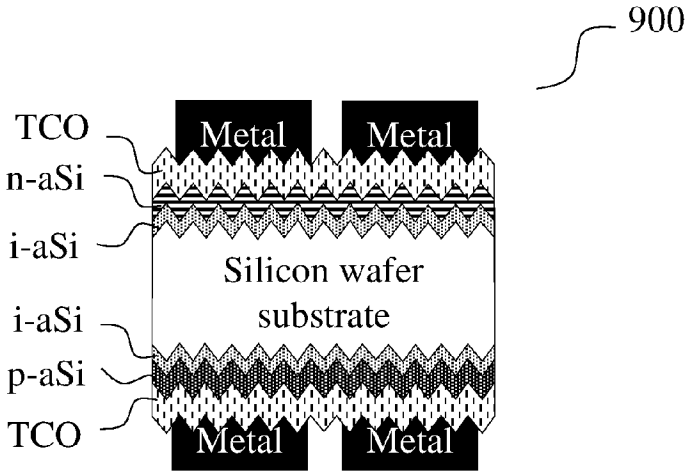

900
TCO
n-aSi
i-aSi
i-aSi
p-aSi
TCO
Metal
Metal
Silicon wafer substrate
Metal
Metal

FIG. 9

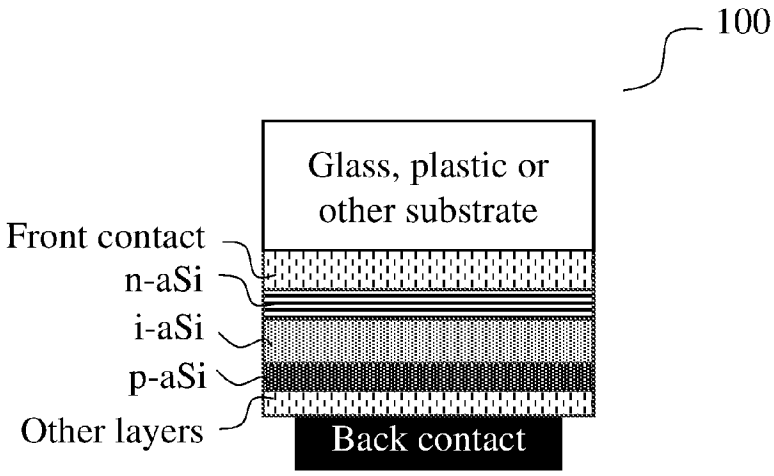

100
Glass, plastic or other substrate
Front contact
n-aSi
i-aSi
p-aSi
Other layers
Back contact

FIG. 10

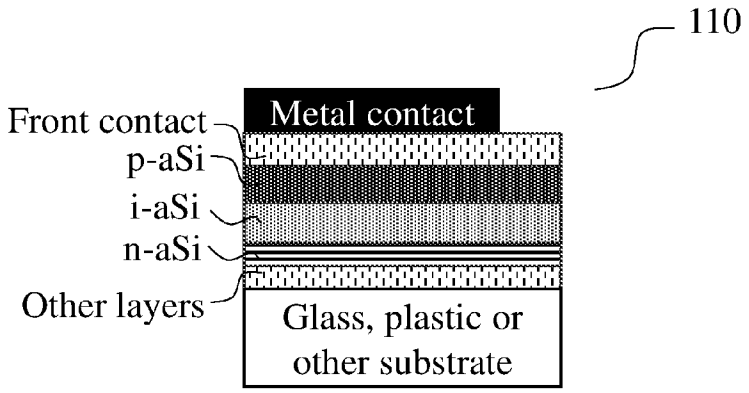


FIG. 11

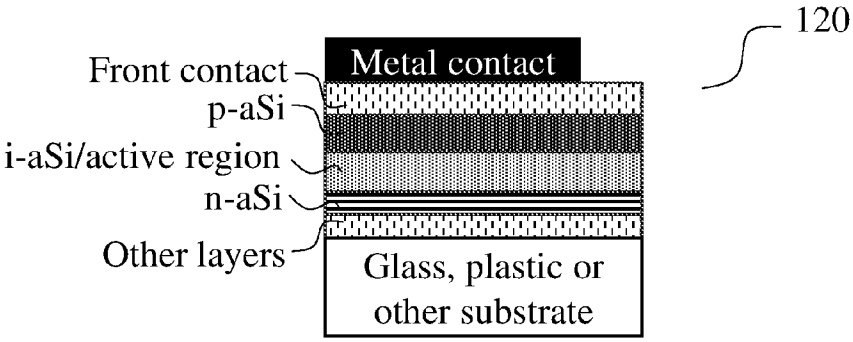


FIG. 12

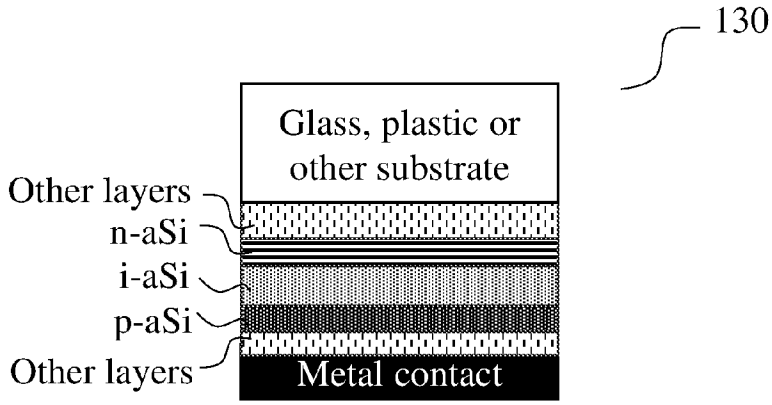


FIG. 13

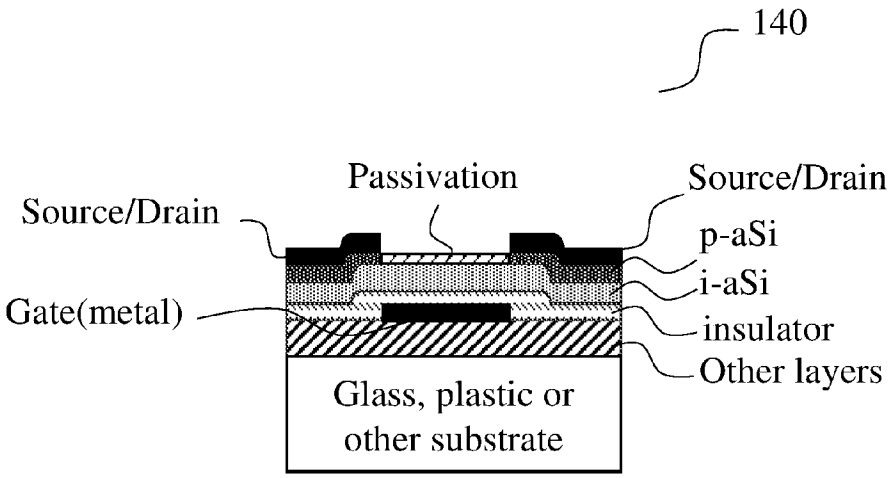

140
Passivation
Source/Drain
Source/Drain
p-aSi
i-aSi
Gate(metal)
insulator
Other layers
Glass, plastic or
other substrate

FIG. 14

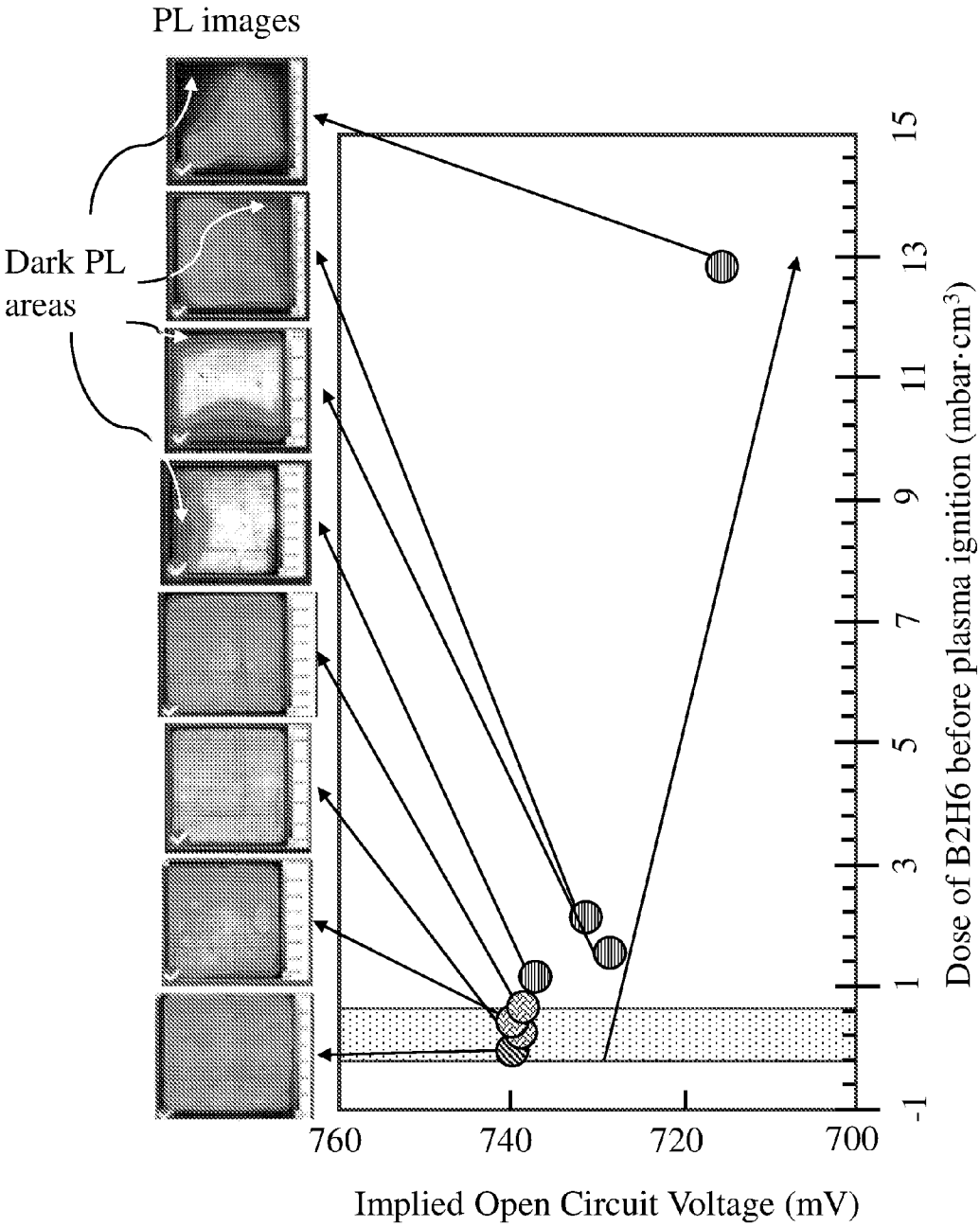

PL images
Dark PL areas
760
740
720
700
Implied Open Circuit Voltage (mV)
-1
1
3
5
7
9
11
13
15
Dose of B2H6 before plasma ignition (mbar·cm³)

FIG. 15

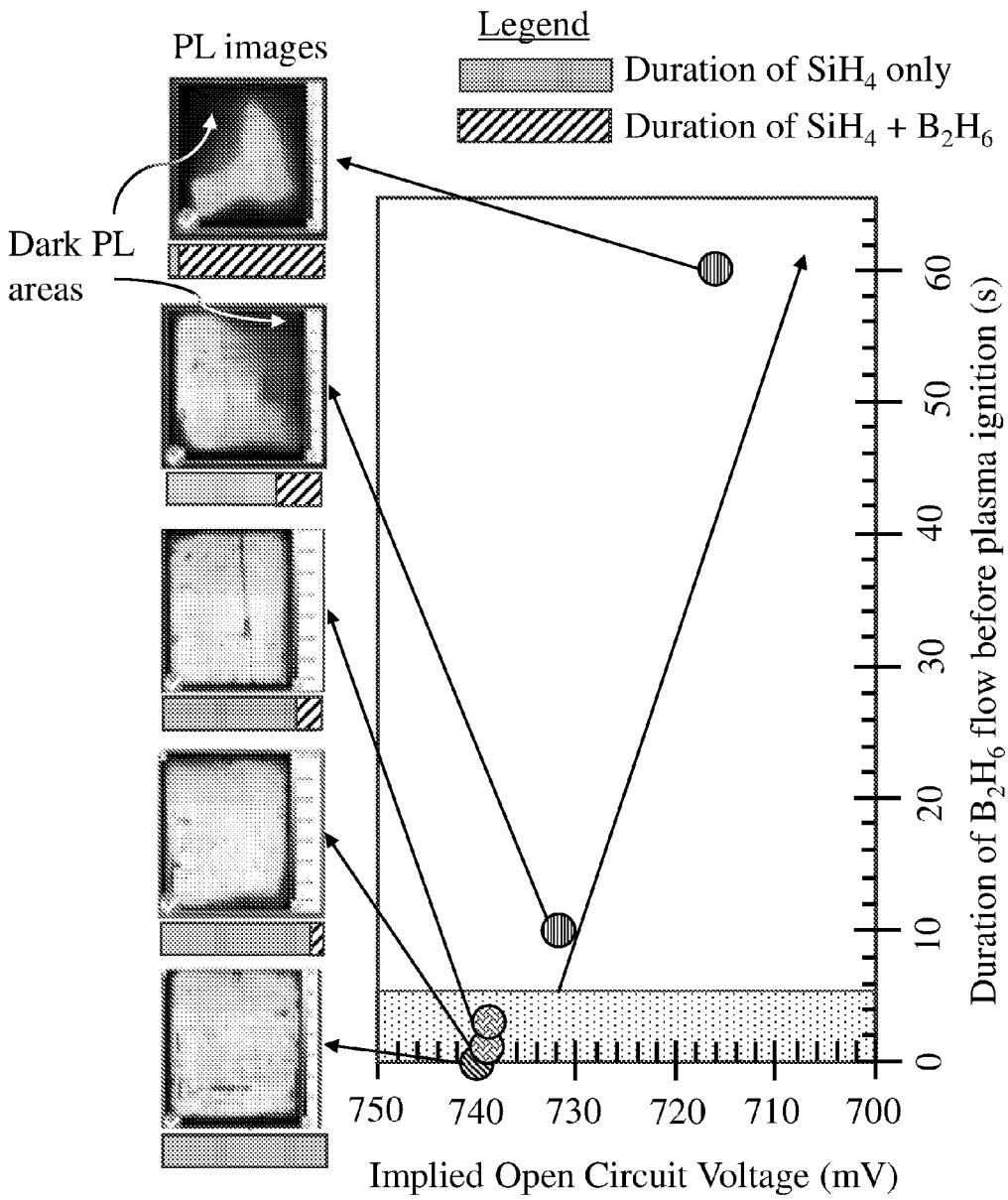

PL images
Dark PL areas
Legend
Duration of SiH_4 only
Duration of SiH_4 + B_2H_6
0
10
20
30
40
50
60
Duration of B_2H_6 flow before plasma ignition (s)
750
740
730
720
710
700
Implied Open Circuit Voltage (mV)

FIG. 16

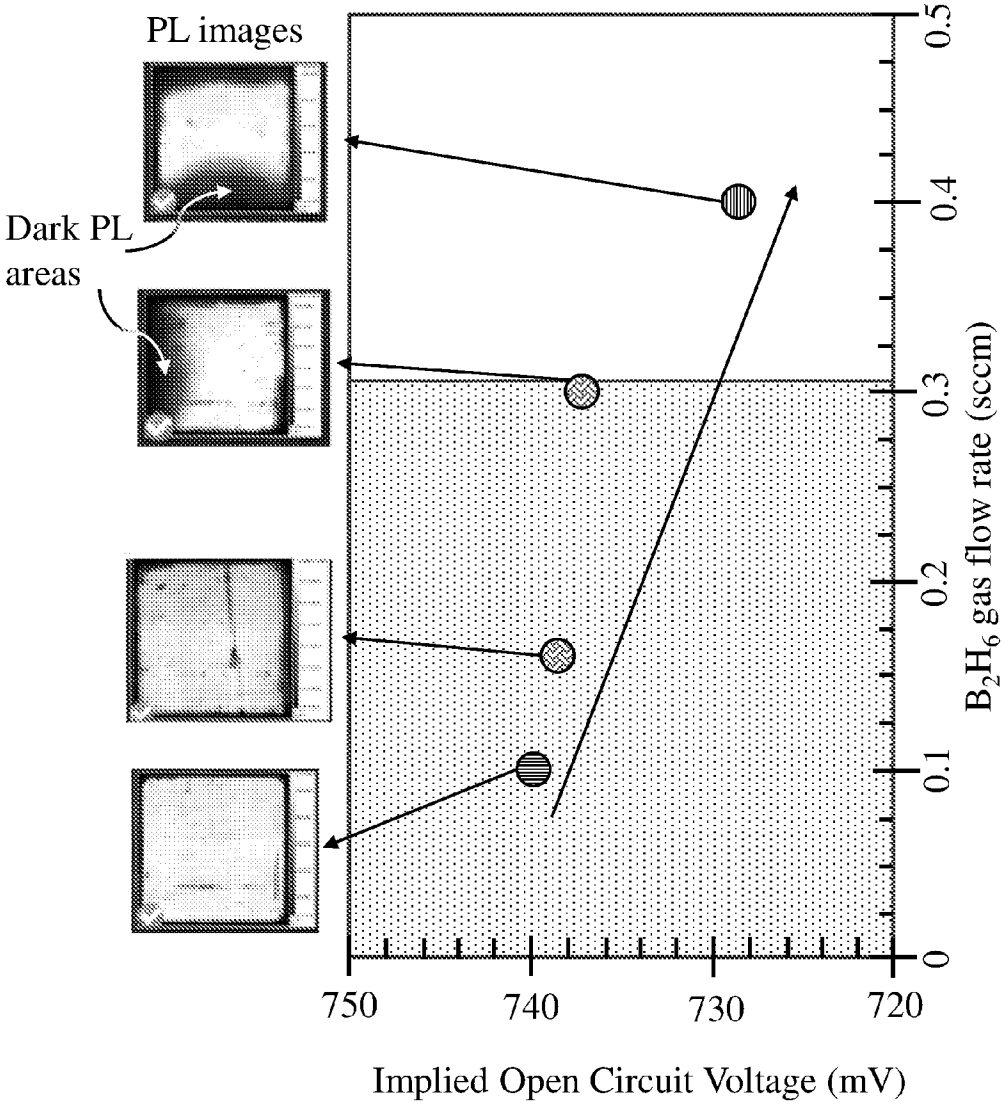
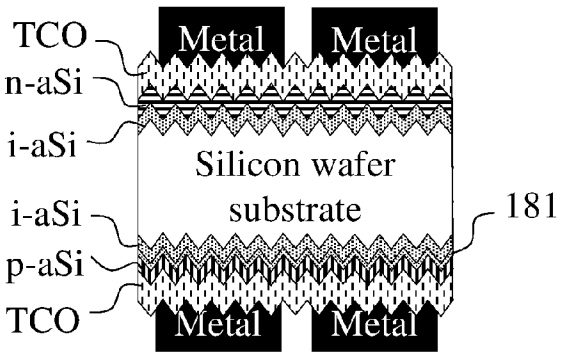

PL images
Dark PL areas
0.5
0.4
0.3
0.2
0.1
0
B_2H_6 gas flow rate (sccm)
750
740
730
720
Implied Open Circuit Voltage (mV)

FIG. 17



(Prior Art)

FIG. 18A

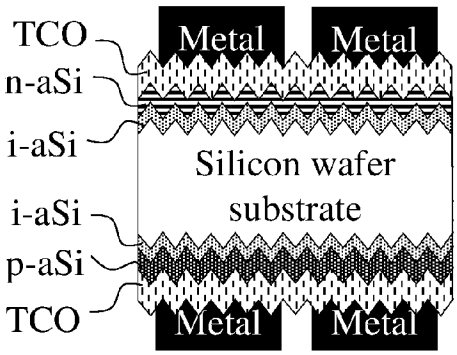


FIG. 18B

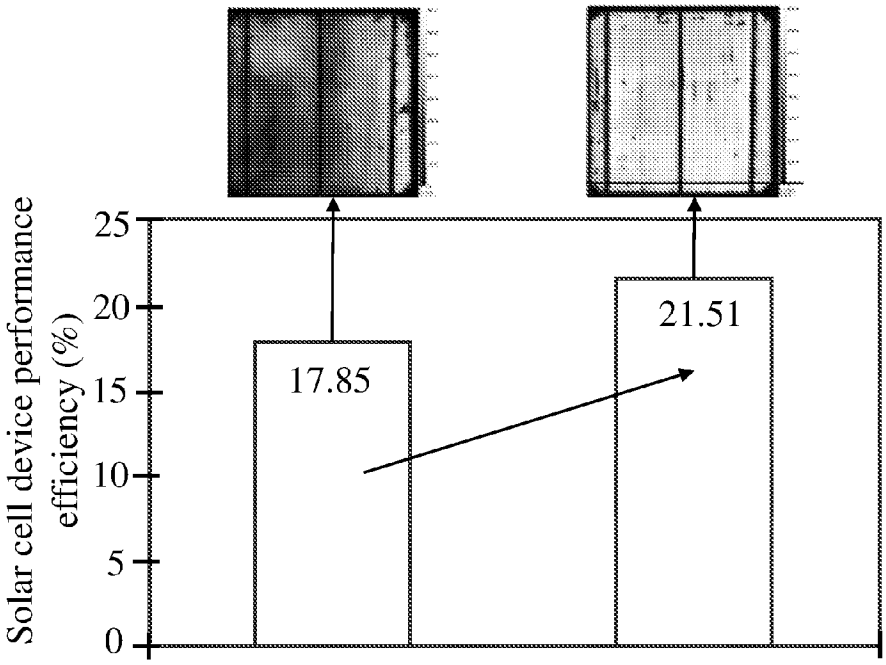

Solar cell device performance efficiency (%)
25
20
15
10
5
0
17.85
21.51

FIG. 19

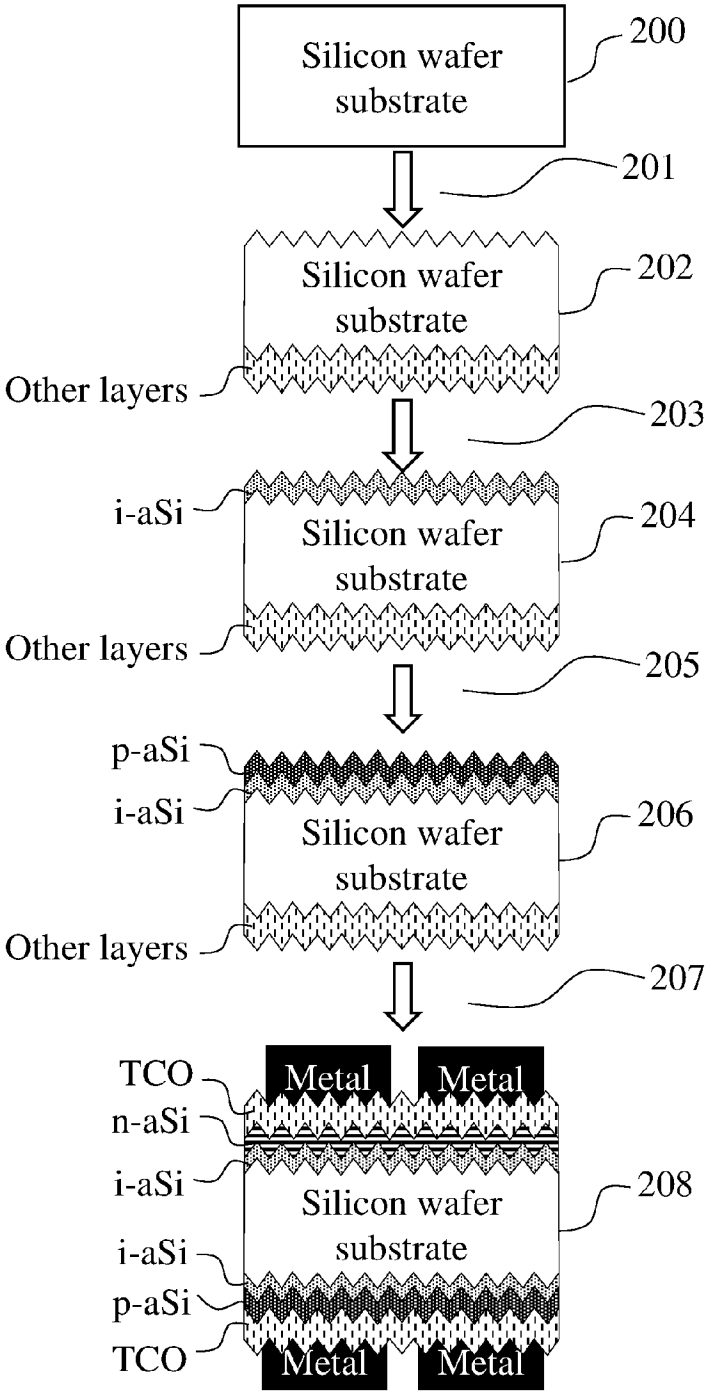

Silicon wafer substrate
200
201
Silicon wafer substrate
202
Other layers
203
i-aSi
Silicon wafer substrate
204
Other layers
205
p-aSi
i-aSi
Silicon wafer substrate
206
Other layers
207
TCO
Metal
Metal
n-aSi
i-aSi
Silicon wafer substrate
208
i-aSi
p-aSi
TCO
Metal
Metal

FIG. 20

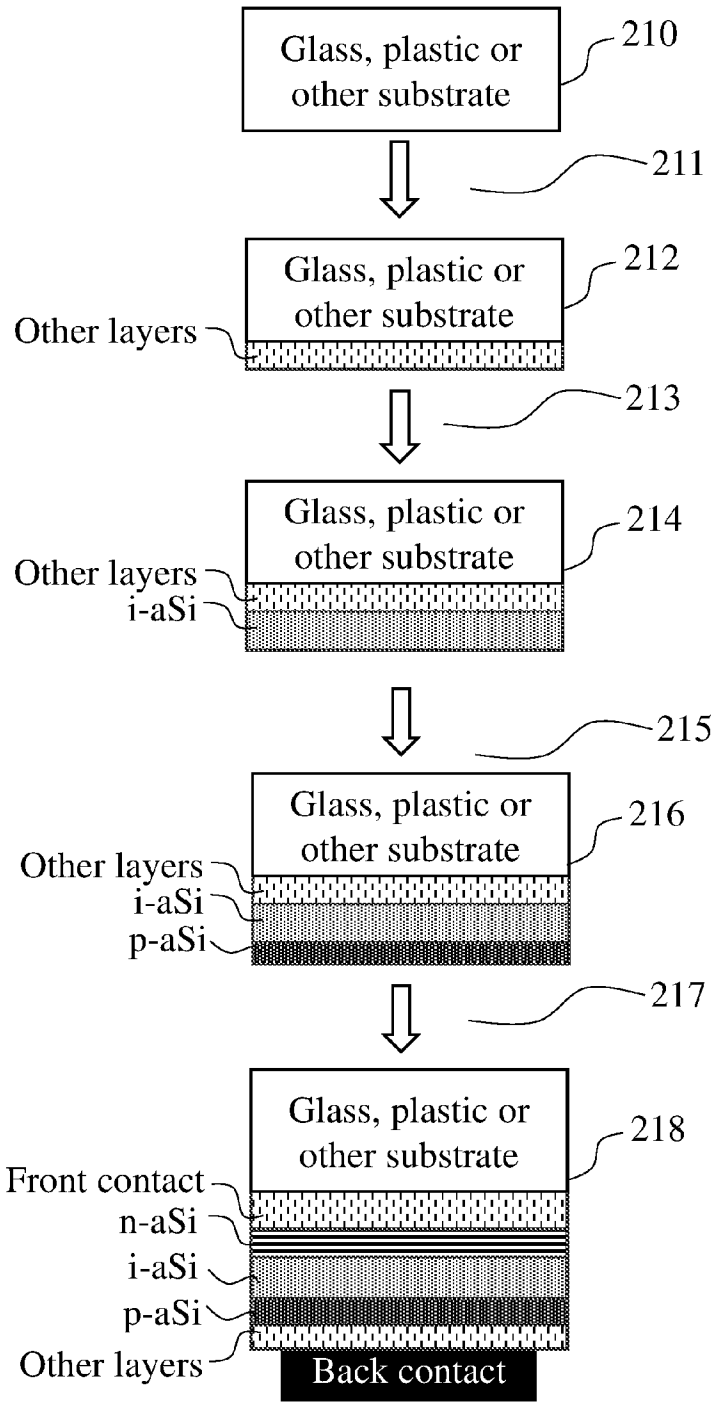

Glass, plastic or other substrate
210
211
Glass, plastic or other substrate
212
Other layers
213
Glass, plastic or other substrate
214
Other layers
i-aSi
215
Glass, plastic or other substrate
216
Other layers
i-aSi
p-aSi
217
Glass, plastic or other substrate
218
Front contact
n-aSi
i-aSi
p-aSi
Other layers
Back contact

FIG. 21

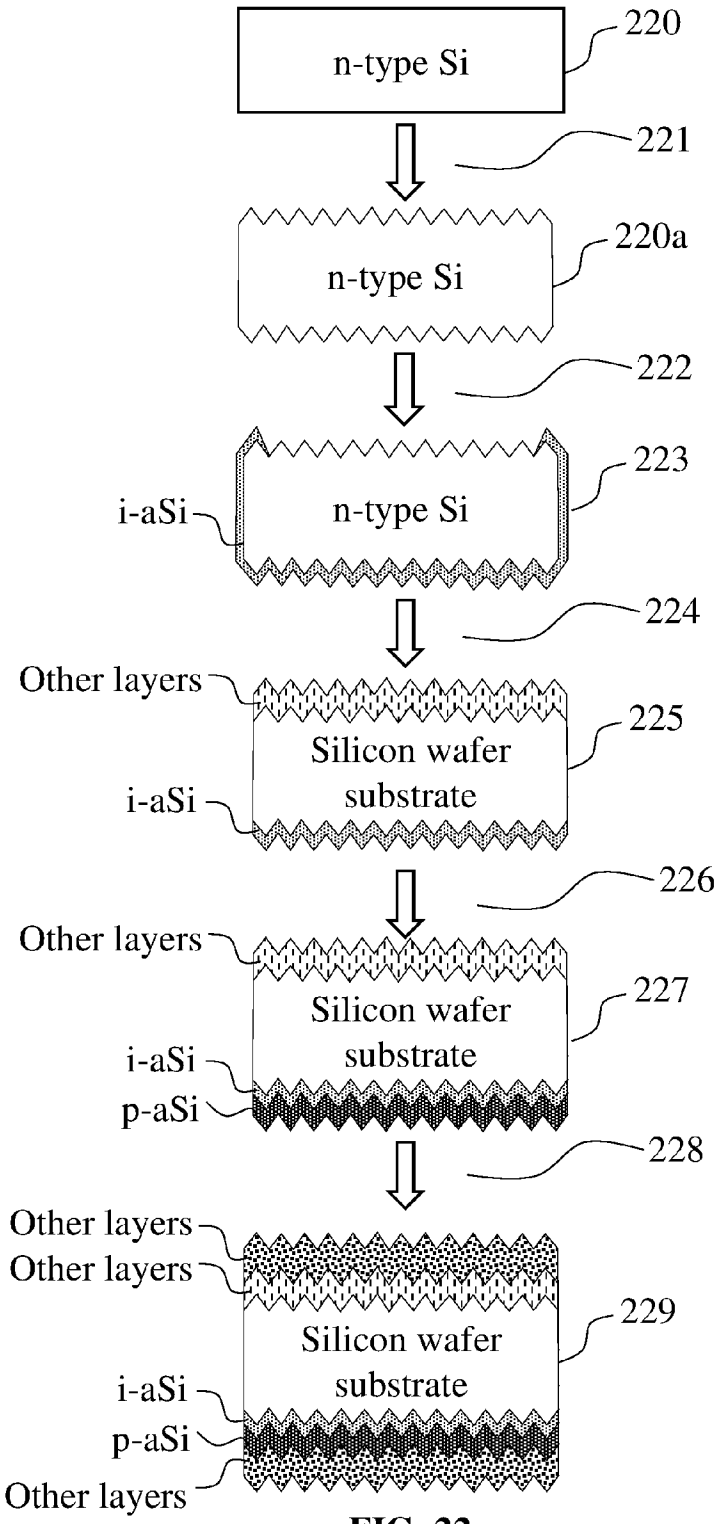

n-type Si
220
221
n-type Si
220a
222
i-aSi
n-type Si
223
224
Other layers
Silicon wafer substrate
225
i-aSi
226
Other layers
Silicon wafer substrate
227
i-aSi
p-aSi
228
Other layers
Other layers
Silicon wafer substrate
229
i-aSi
p-aSi
Other layers

FIG. 22

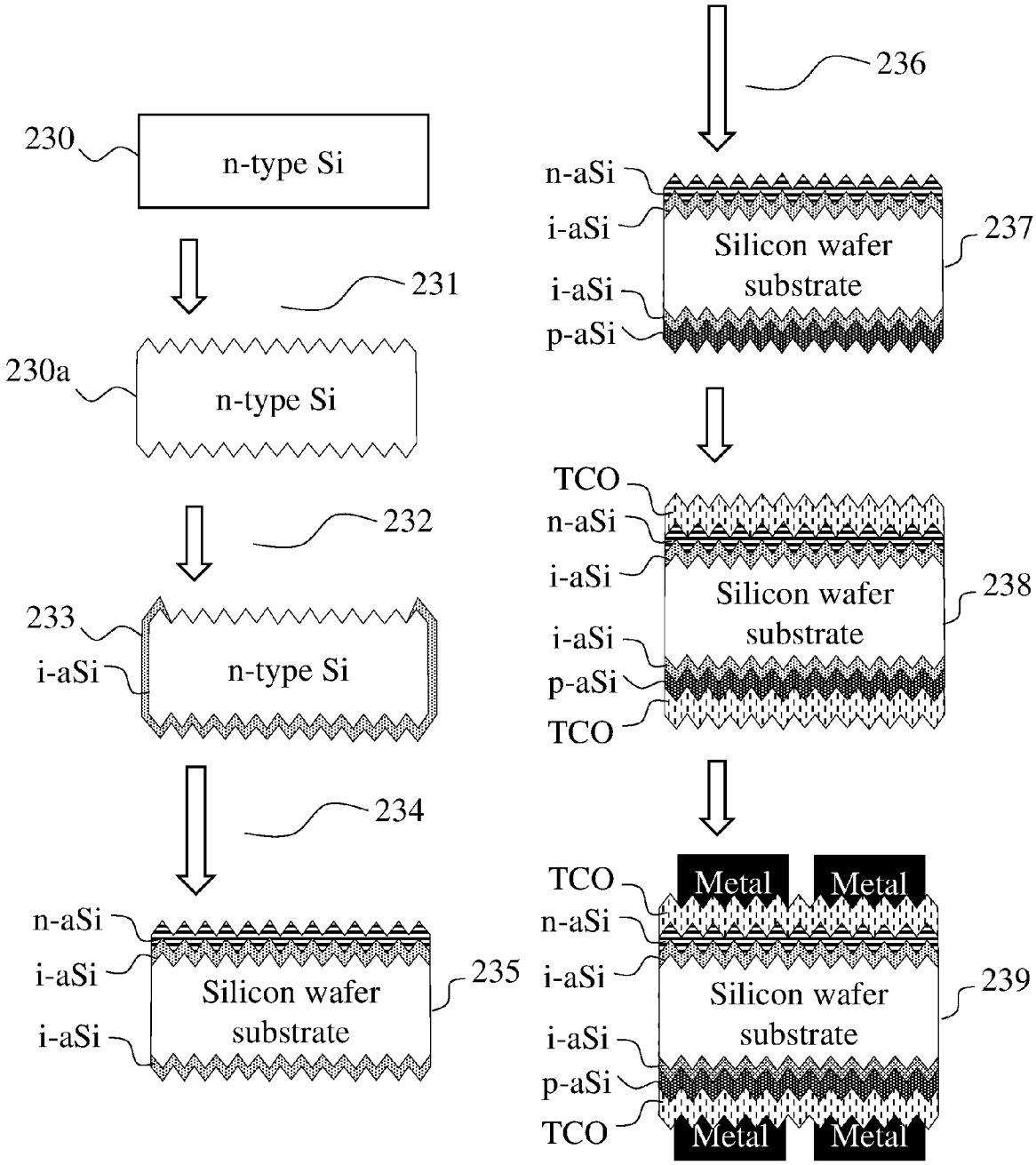

230
n-type Si
231
230a
n-type Si
232
233
i-aSi
n-type Si
234
n-aSi
i-aSi
Silicon wafer substrate
i-aSi
235
236
n-aSi
i-aSi
Silicon wafer substrate
i-aSi
p-aSi
237
TCO
n-aSi
i-aSi
Silicon wafer substrate
i-aSi
p-aSi
TCO
238
TCO
Metal
Metal
n-aSi
i-aSi
Silicon wafer substrate
i-aSi
p-aSi
TCO
Metal
Metal
239

FIG. 23

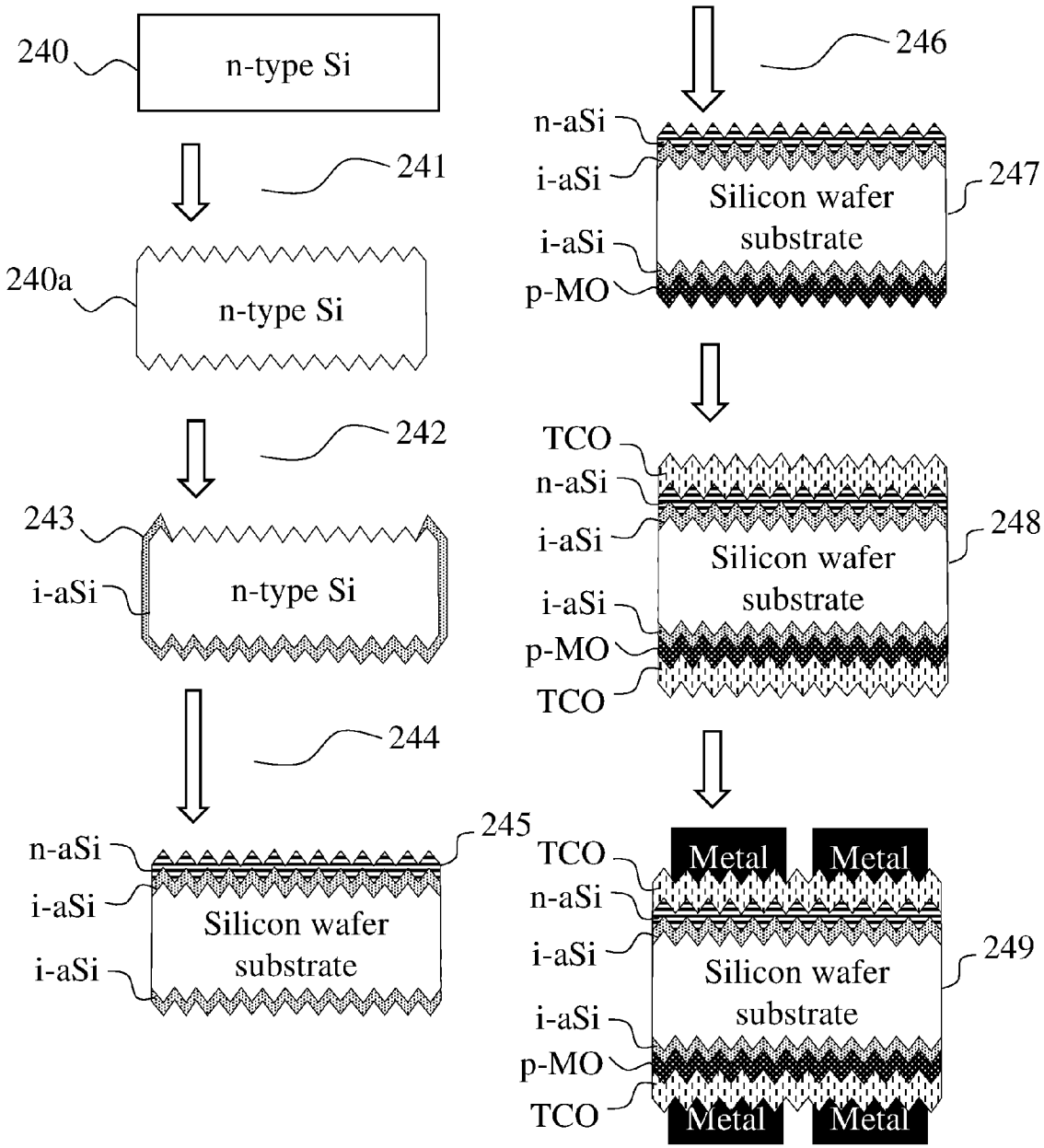

240
n-type Si
241
240a
n-type Si
242
243
i-aSi
n-type Si
244
n-aSi
i-aSi
i-aSi
Silicon wafer substrate
245
246
n-aSi
i-aSi
i-aSi
p-MO
Silicon wafer substrate
247
TCO
n-aSi
i-aSi
i-aSi
p-MO
TCO
Silicon wafer substrate
248
TCO
n-aSi
i-aSi
i-aSi
p-MO
TCO
Metal
Metal
Metal
Metal
Silicon wafer substrate
249

FIG. 24

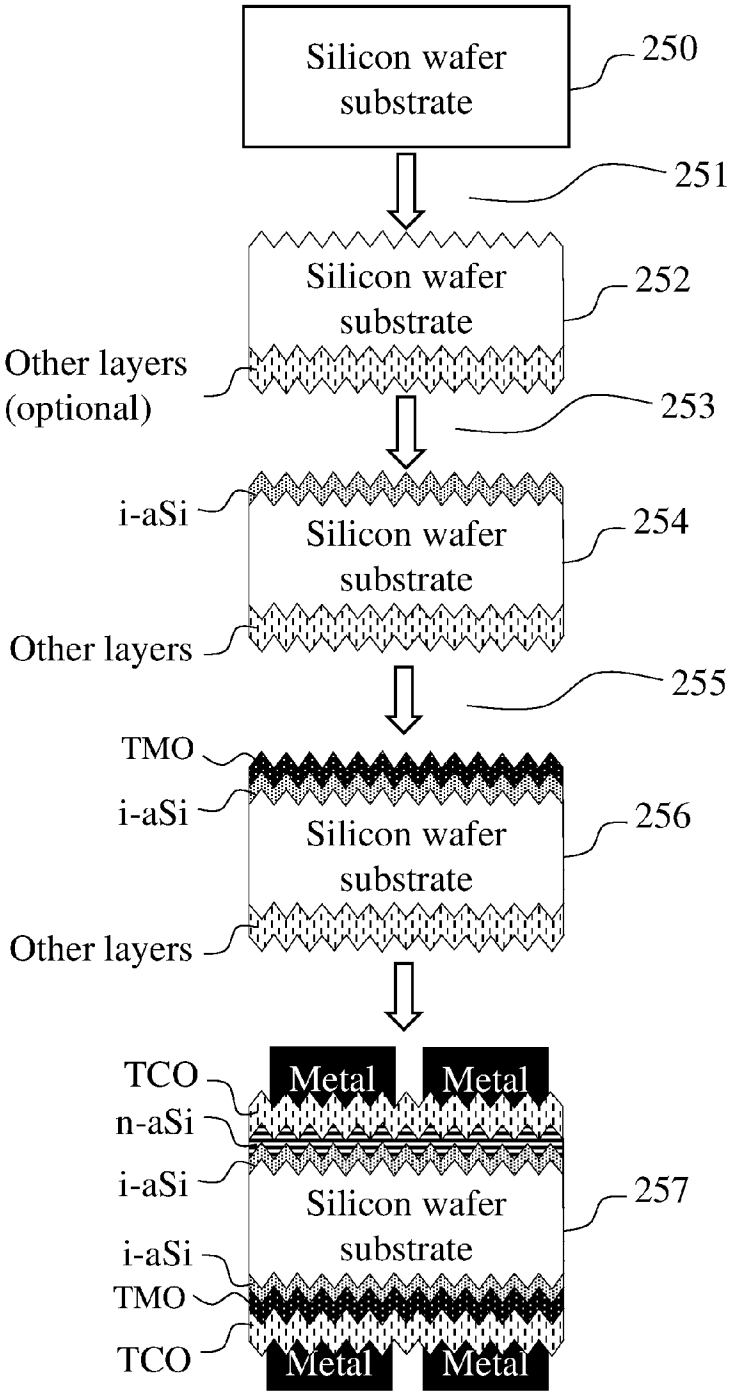

Silicon wafer substrate
250
251
Silicon wafer substrate
252
Other layers (optional)
253
i-aSi
Silicon wafer substrate
254
Other layers
255
TMO
i-aSi
Silicon wafer substrate
256
Other layers
TCO
Metal
Metal
n-aSi
i-aSi
Silicon wafer substrate
257
i-aSi
TMO
TCO
Metal
Metal

FIG. 25

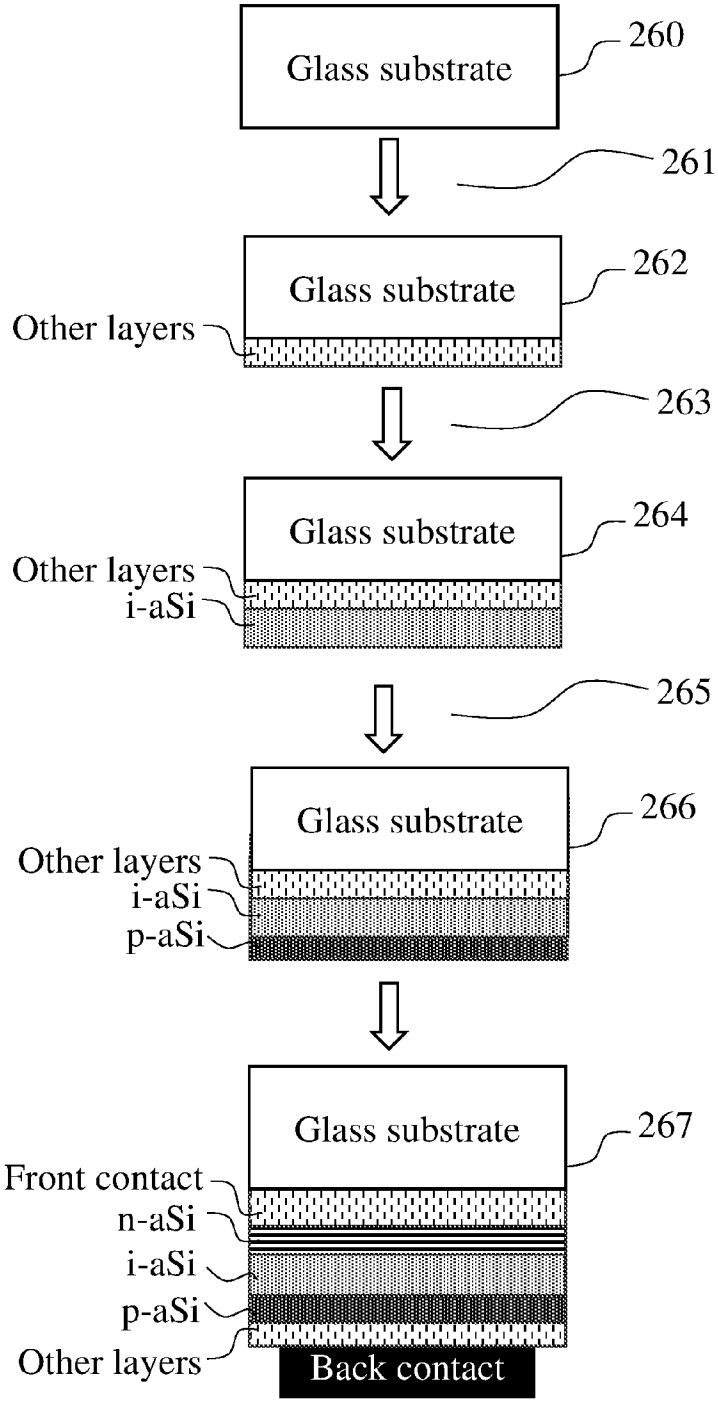

Glass substrate
260
261
Glass substrate
262
Other layers
263
Glass substrate
264
Other layers
i-aSi
265
Glass substrate
266
Other layers
i-aSi
p-aSi
Glass substrate
267
Front contact
n-aSi
i-aSi
p-aSi
Other layers
Back contact

FIG. 26

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2024/050399

A. CLASSIFICATION OF SUBJECT MATTER

C23C 16/22 (2006.01) H01L 21/205 (2006.01) H01L 31/0288 (2006.01) H01L 31/18 (2006.01)

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C23C, H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT: film, thin, amorphous, boron, p-type, p-aSi, precursor, reactant, SiH4, Silane, diborane, hydride, B2H6, duration, time, shorter, longer, gas, vapor, stabilization, exposure, and related terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2018/0033622 A1 (SWAMINATHAN, S. ET AL.) 1 February 2018 Figure 4; paragraphs [0039], [0055]-[0056], [0061]-[0071]	1-12 13-19
A	CN 115566094 A (CHANGZHOU S C EXACT EQUIP CO LTD) 3 January 2023 Whole document of the original non-English language document (a machine translation is enclosed **only** for your reference)	
A	US 2008/0145536 A1 (ZHANG, K. ET AL.) 19 June 2008 Whole document	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*Special categories of cited documents:

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29/08/2024 *(day/month/year)*	06/09/2024 *(day/month/year)*

Name and mailing address of the ISA/SG	Authorized officer
Intellectual Property Office of Singapore 1 Paya Lebar Link, #11-03 PLQ 1, Paya Lebar Quarter Singapore 408533	Meng Lei (Dr)
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/SG2024/050399

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2018/0033622 A1	01/02/2018	KR 20180013745 A JP 2018061007 A CN 107680903 A TW 201821637 A SG 10201705999T A CN 113488379 A KR 20210086594 A	07/02/2018 12/04/2018 09/02/2018 16/06/2018 27/02/2018 08/10/2021 08/07/2021
CN 115566094 A	03/01/2023	NONE	
US 2008/0145536 A1	19/06/2008	WO 2008/074016 A2	19/06/2008