

- [54] APPARATUS FOR DRIVING A LIGHT
EMITTING DIODE OF HOROLOGIC
DISPLAY
- [75] Inventor: R. Gary Daniels, Tempe, Ariz.
- [73] Assignee: Motorola, Inc., Franklin Park, Ill.
- [22] Filed: May 17, 1971
- [21] Appl. No.: 143,826
- [52] U.S. Cl. 58/50 R, 58/127 R
- [51] Int. Cl. G04b 19/30, G04b 19/06
- [58] Field of Search 58/23 R, 23 A, 127 R,
58/50 R; 235/92 EA

[56] References Cited

UNITED STATES PATENTS

3,194,003	7/1965	Polin	58/23 R
3,630,015	12/1971	Lehovec	58/50 R
3,664,116	5/1972	Emerson et al.	58/50 R X
3,576,099	3/1971	Walton	58/23 X

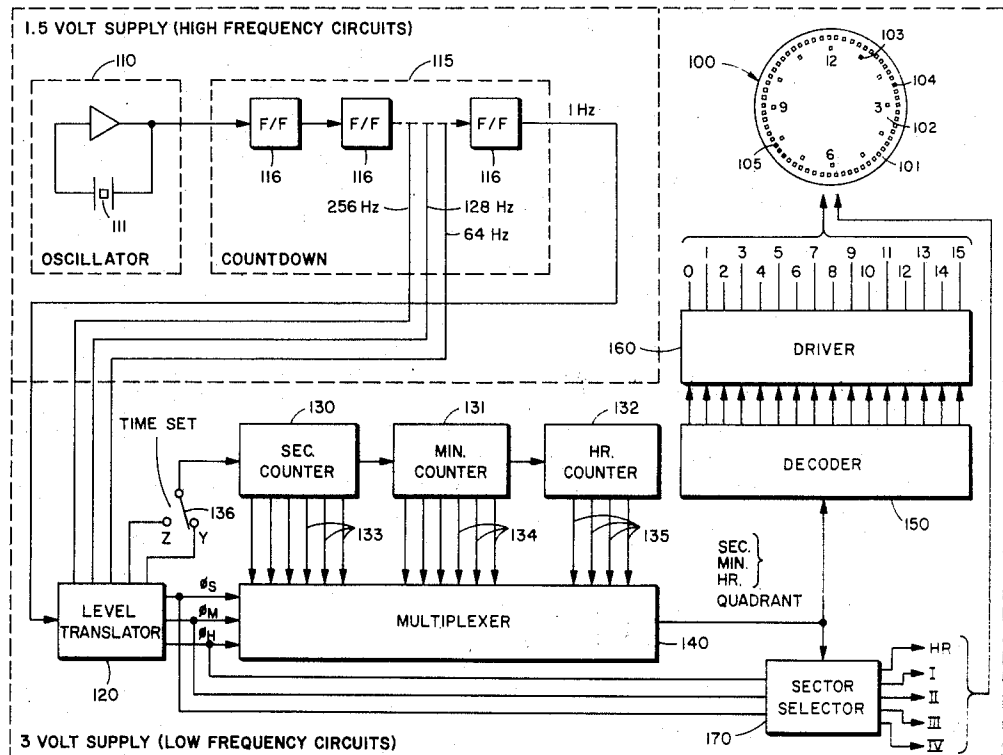
Primary Examiner—Richard B. Wilkinson
Assistant Examiner—Edith C. Jackmon
Attorney—Mueller and Aichele

[57] ABSTRACT

There is disclosed a logic and driving circuit for a light emitting diode type horologic display in which three diodes are read out at any given time to represent the time of day. Power consumption is kept to a minimum by the use of a two voltage level system with the lower voltage supplying those portions of the circuit working at a high frequency while the higher voltage supplies the display and those portions of the driving circuit op-

erating at a considerably lower frequency. In addition to a crystal frequency standard and a "divide-by-two" flip-flop countdown circuit which provides a 1 Hz signal to a series of toggle flip-flop counting circuits which function as the seconds, minutes and hours storage elements, there is provided a multiplexer coupled to the outputs of these counting circuits which is strobed with pulses having a combined duration of only a fraction of the sampling cycle. This results in a low duty cycle for the output of the multiplexer and thus for the display itself which conserves on the power necessary to drive the display. Since hour, minute and second information is sequentially sampled by the multiplexing circuit, multiplexing eliminates decoder and driver redundancy. Provision is made in the multiplexing logic for dividing the horological display into quadrants or sectors so as to further reduce the number of driver and decoder elements. As a result there is also provided a quadrant selecting circuit. The sampling pulses for the multiplexing circuit are conveniently derived from the frequency standard countdown circuit. The driving system utilizes complementary metal oxide semiconductor (CMOS) components in which power drain is minimized because these elements draw appreciable power only when switching. A further power consumption advantage is obtained by utilizing NAND gate logic to permit the use of these low power CMOS components. Toggle flip-flops are chosen for the counters because they are available in metal oxide semiconductor form and because the total number of transistors utilized is reduced. The logic described herein is used with a horologic display in which the minutes and seconds are displayed in the single ring of elements with the hours being displayed in another single ring of elements.

19 Claims, 13 Drawing Figures



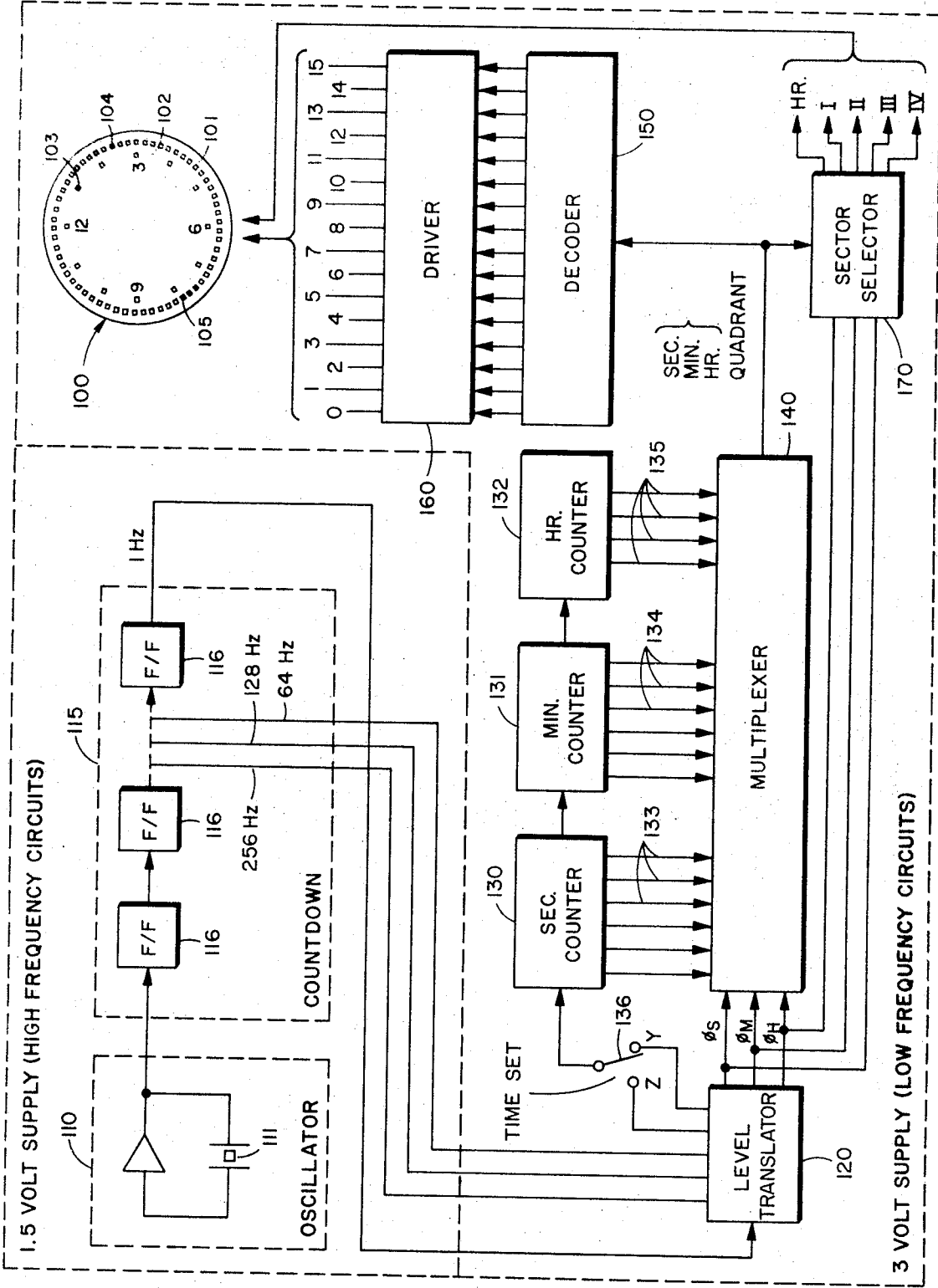
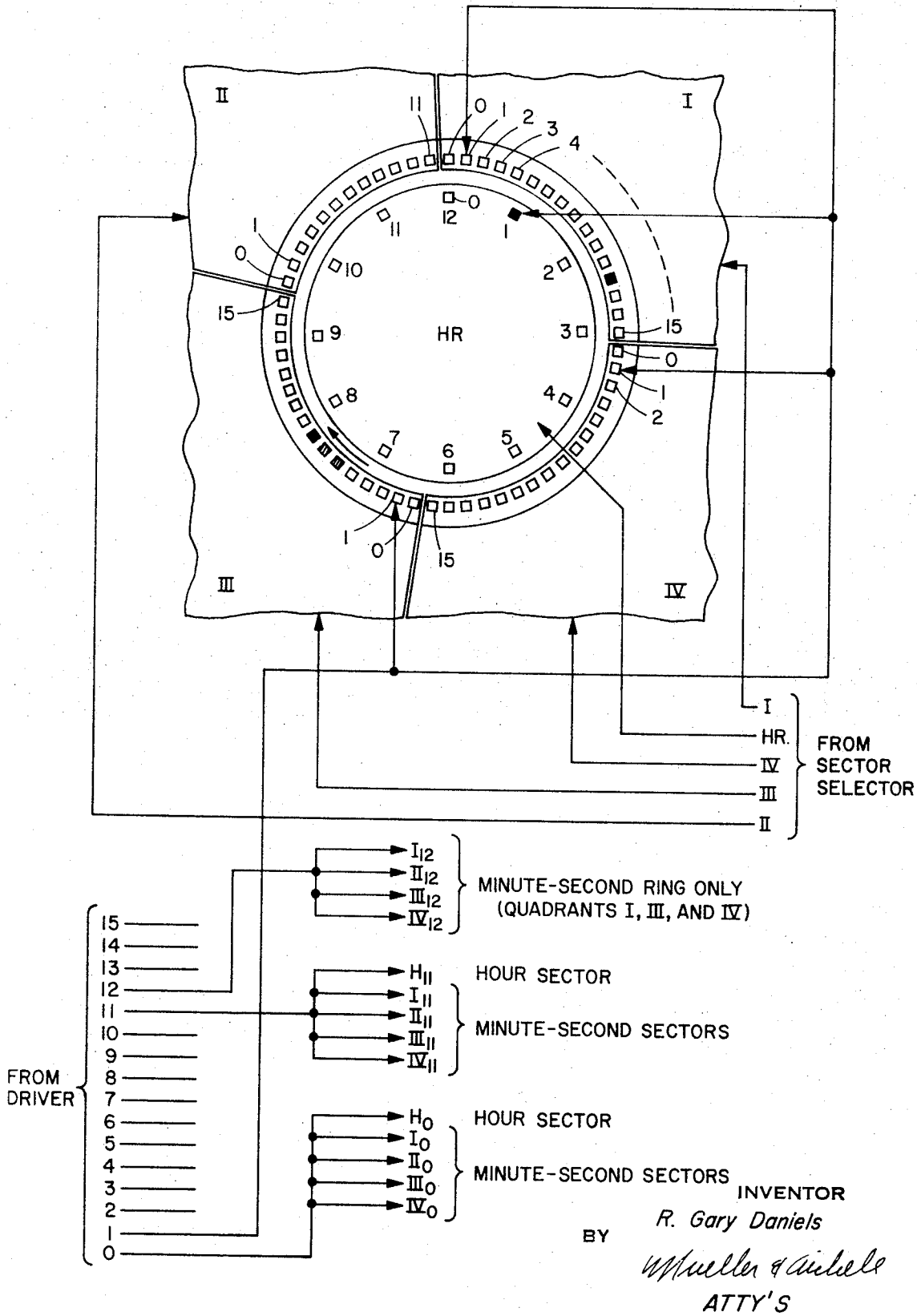
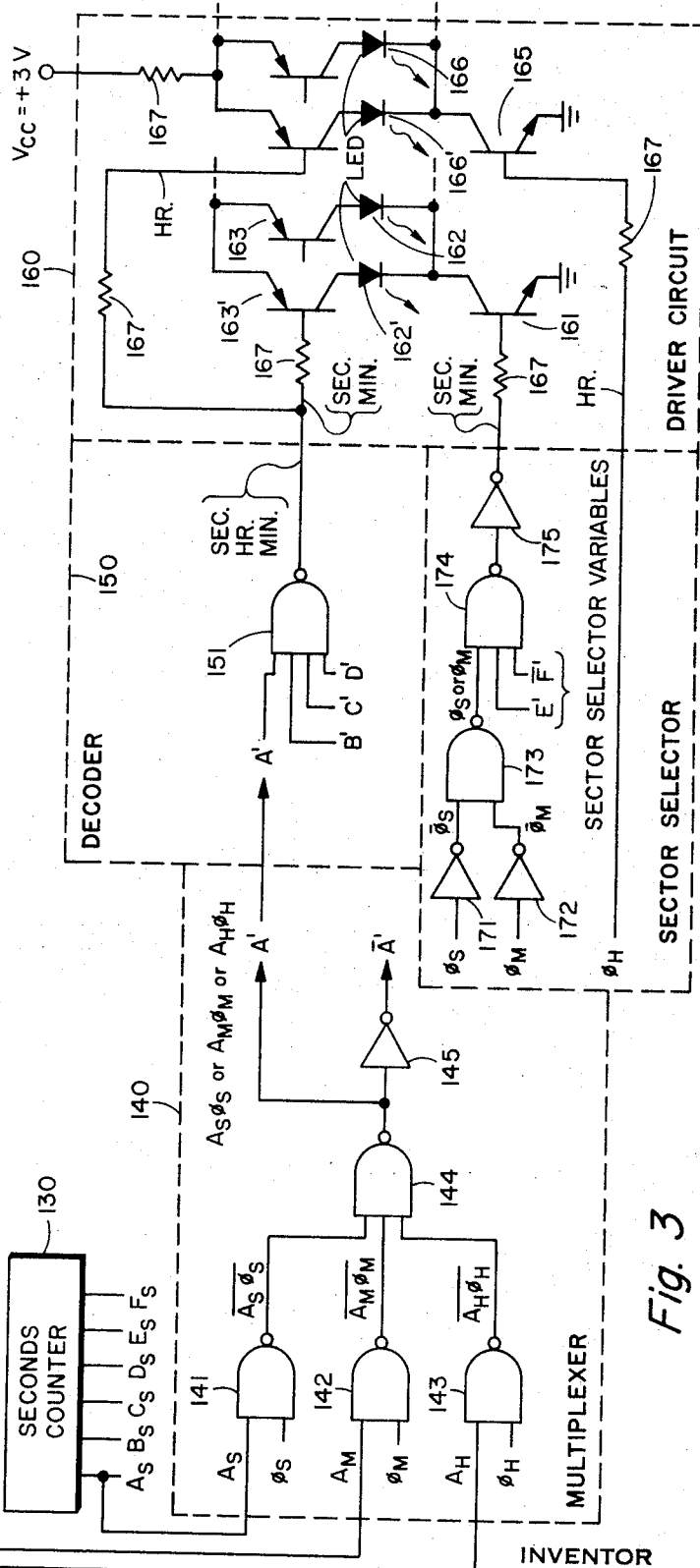
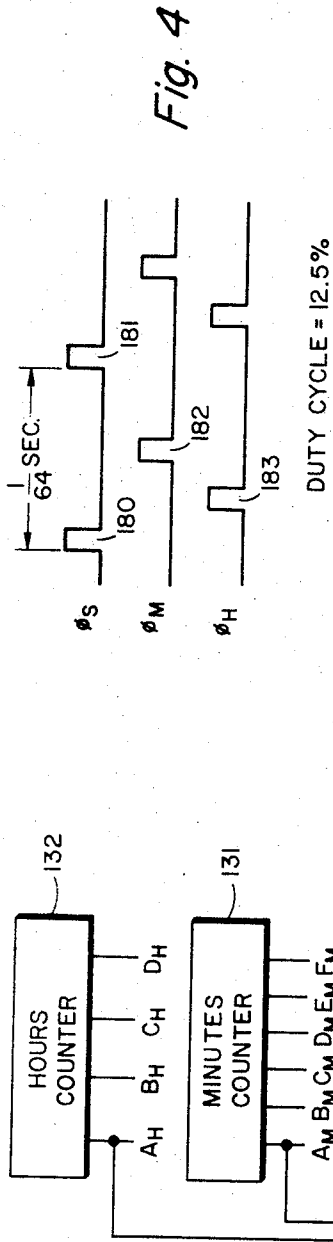


Fig. 1

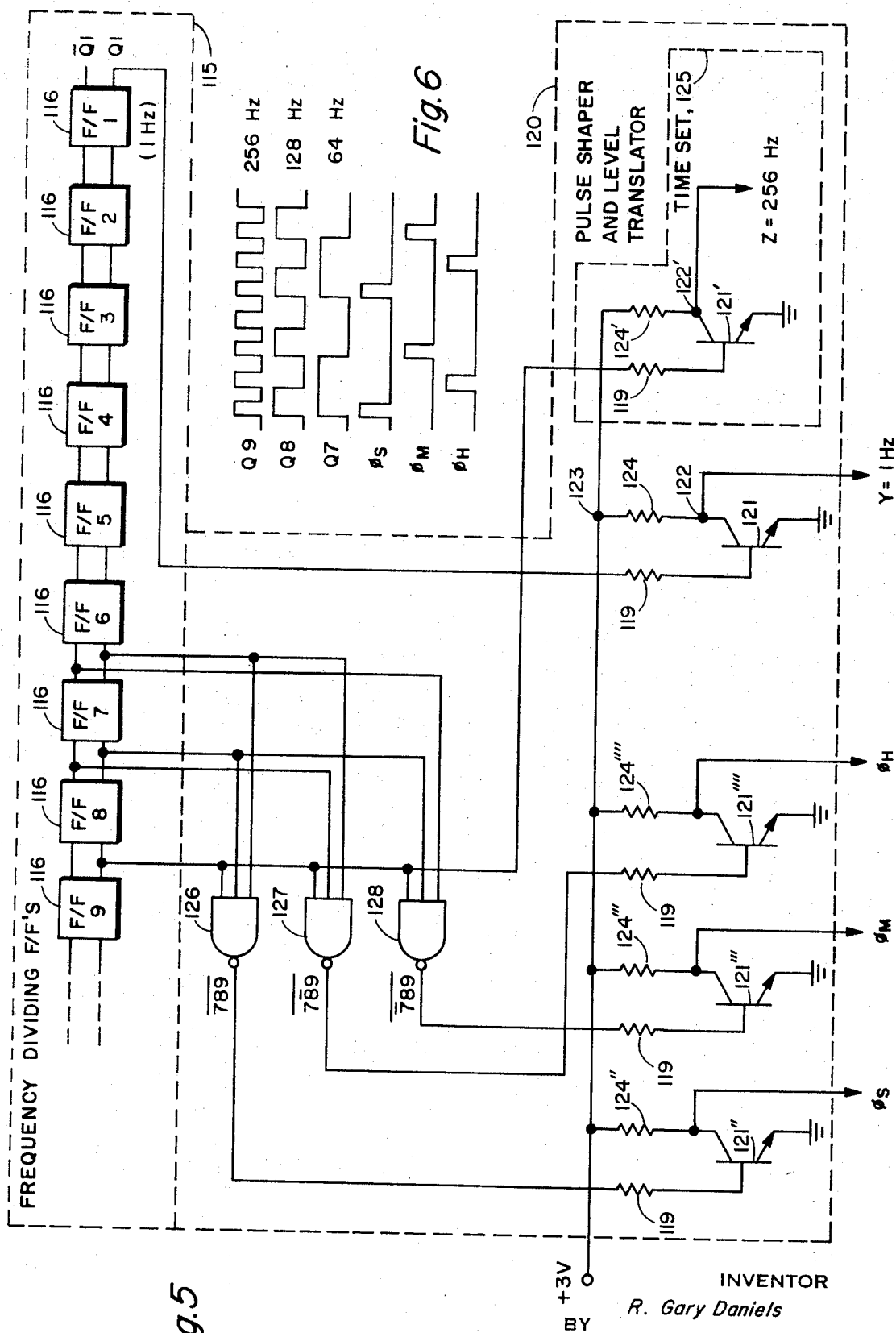
INVENTOR
R. Gary Daniels
BY
Mueller & Aichele
ATTY'S

Fig. 2





BY R. Gary Daniels
Muller + Siebel
 ATTY'S



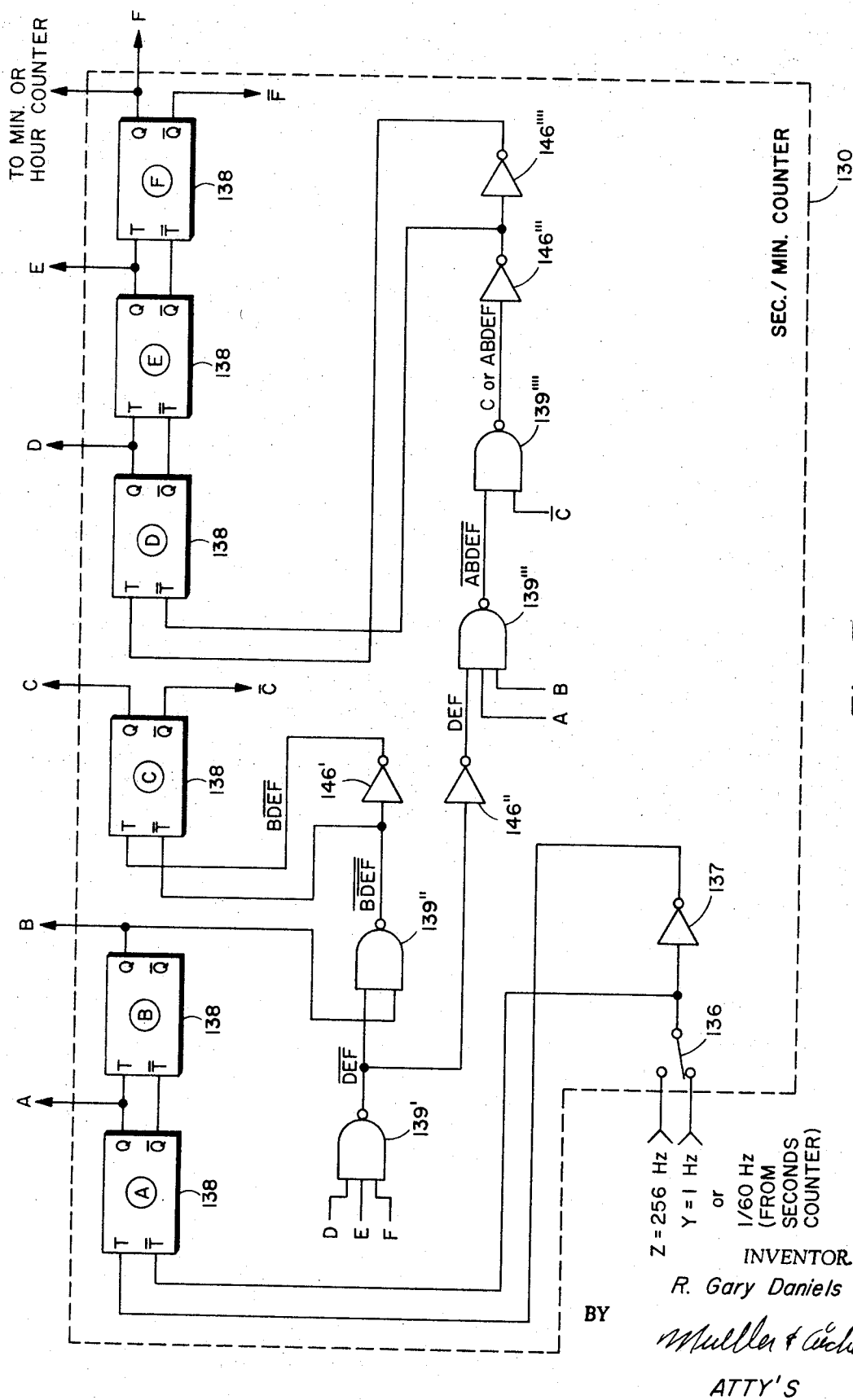


Fig. 7

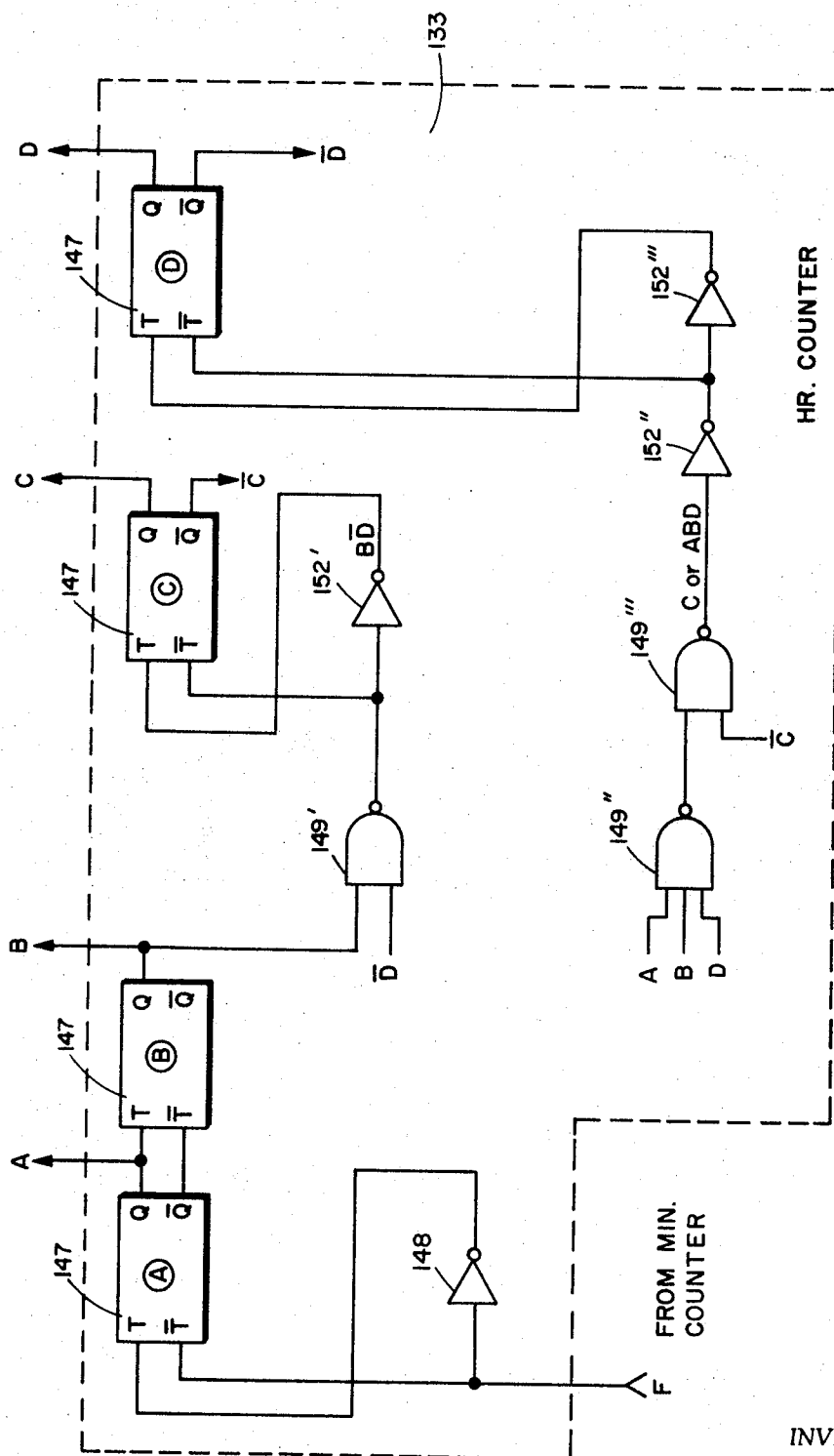


Fig. 8

INVENTOR.

R. Gary Daniels

BY

Mueller & Nichol

ATTY'S.

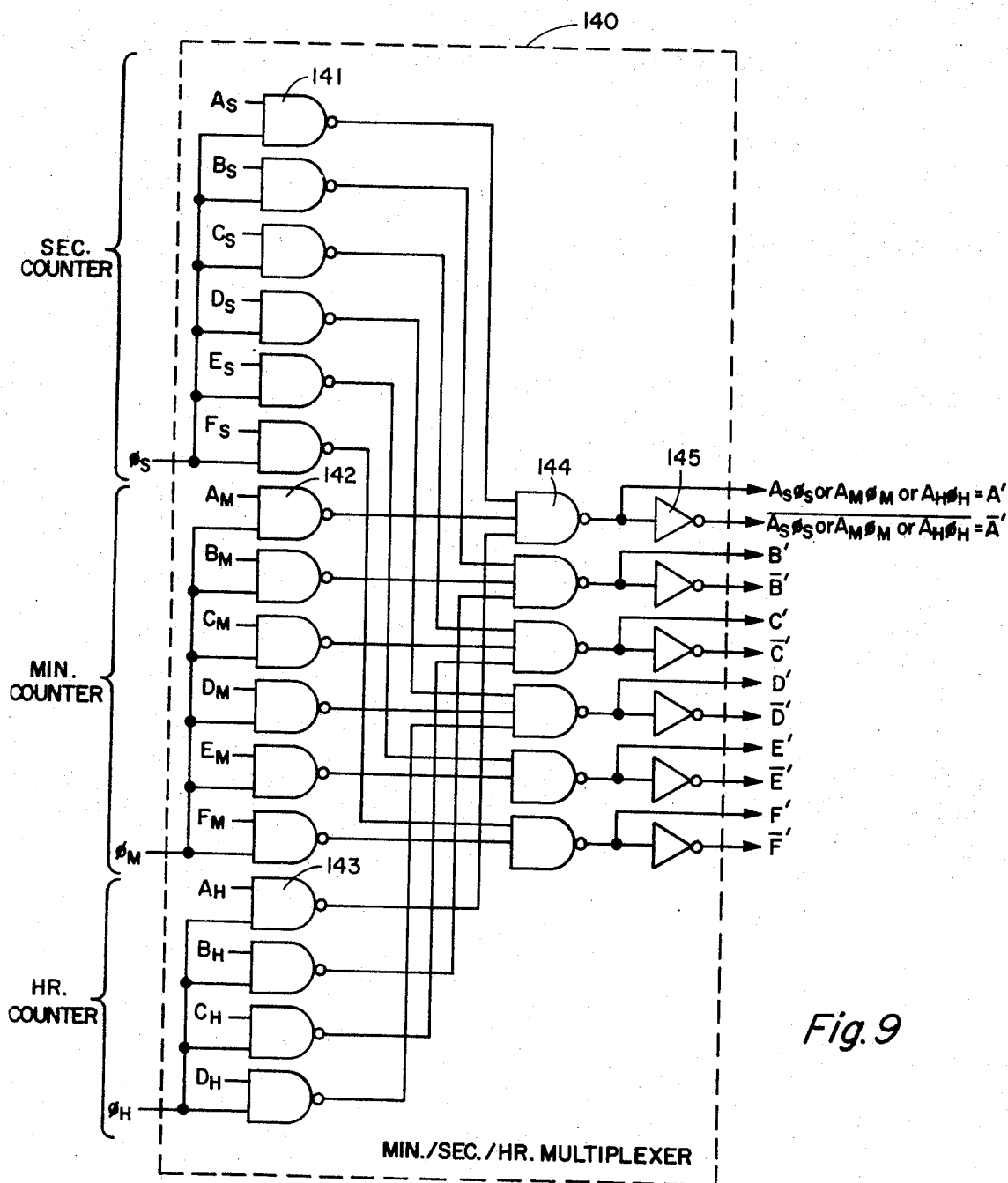


Fig. 9

INVENTOR.
R. Gary Daniels
BY *Mueller & Aichele*
ATTYS.

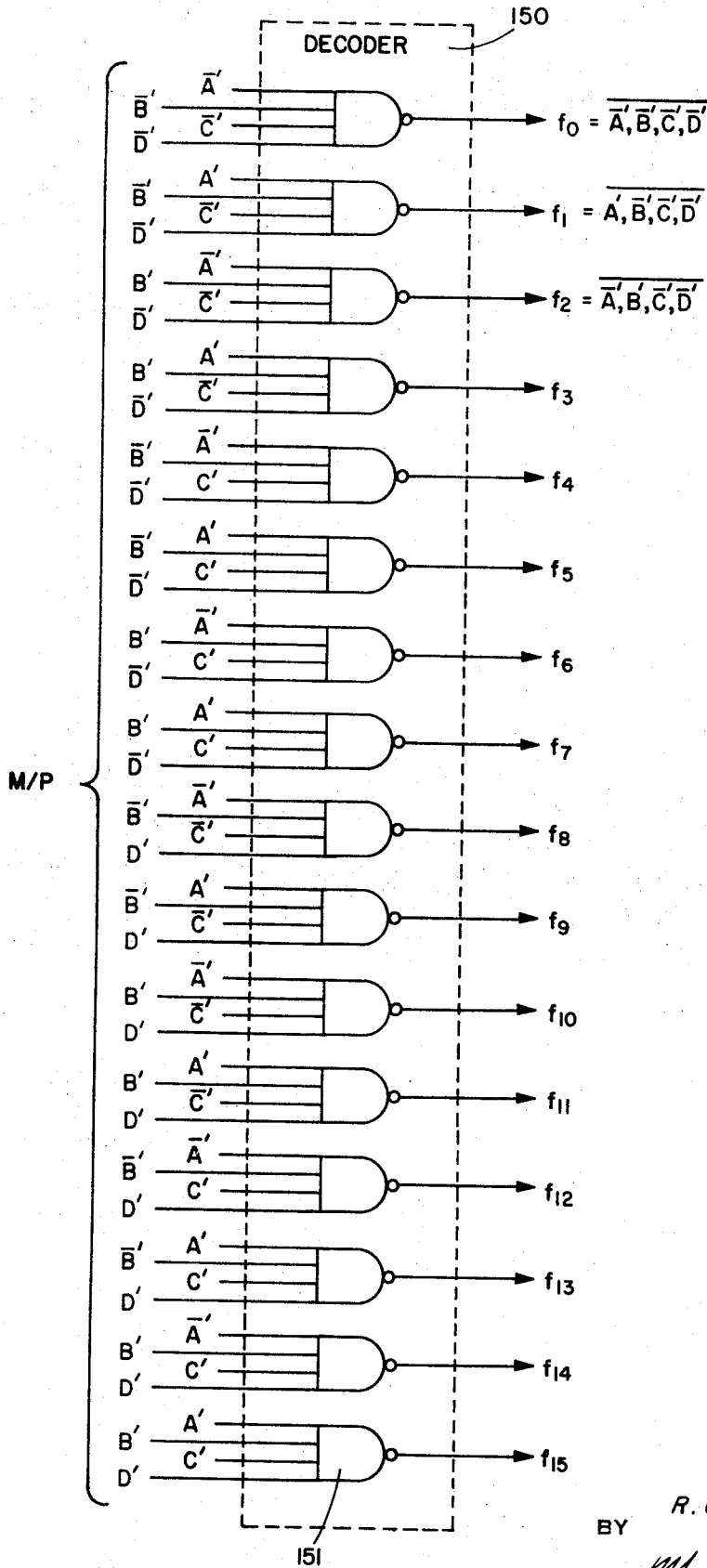


Fig. 10

INVENTOR
 R. Gary Daniels
 BY *Mueller & Nichols*
 ATTY'S.

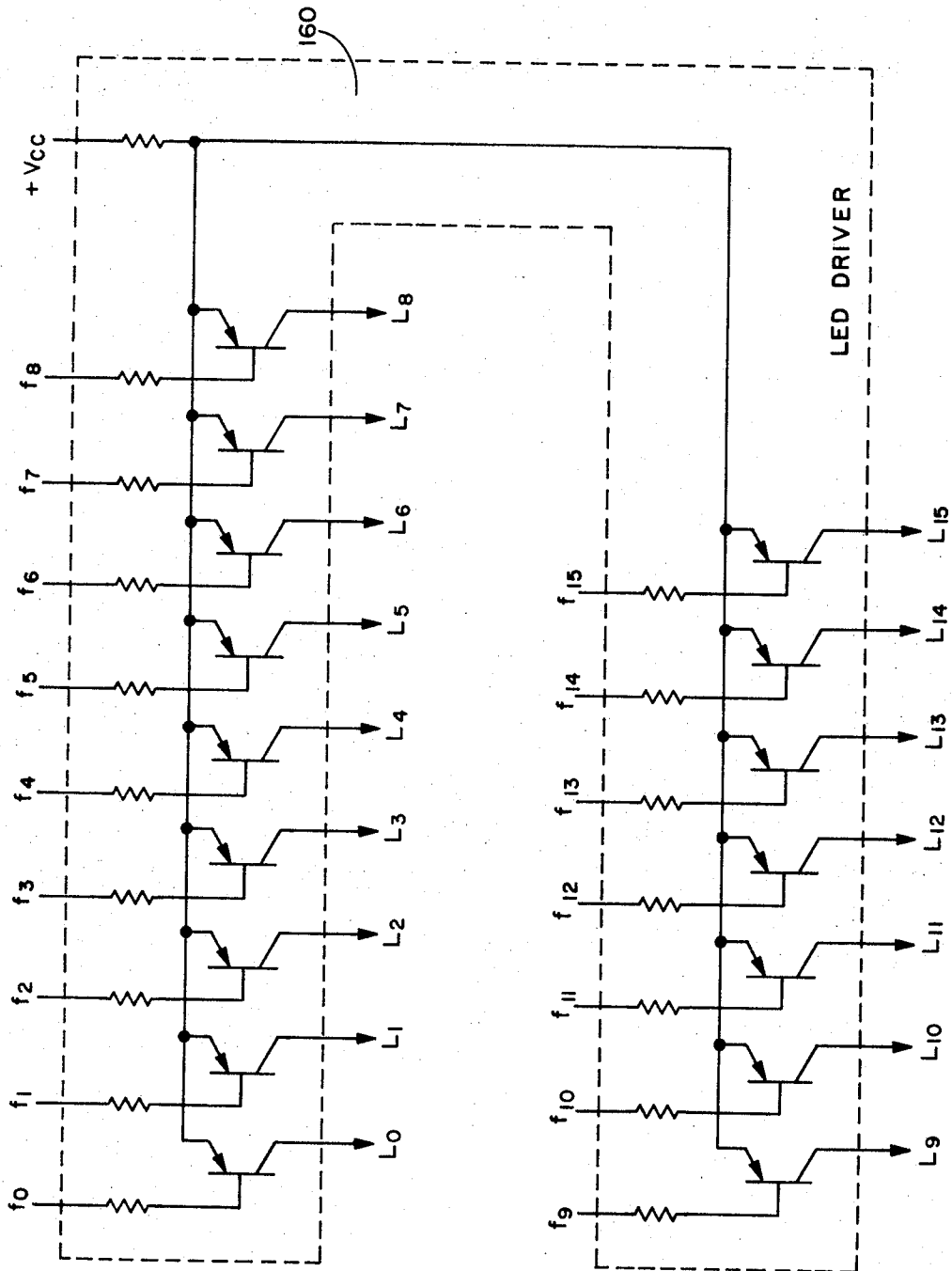


Fig. 11

INVENTOR.
 R. Gary Daniels
 BY *Mueller & Nichols*
 ATTY'S.

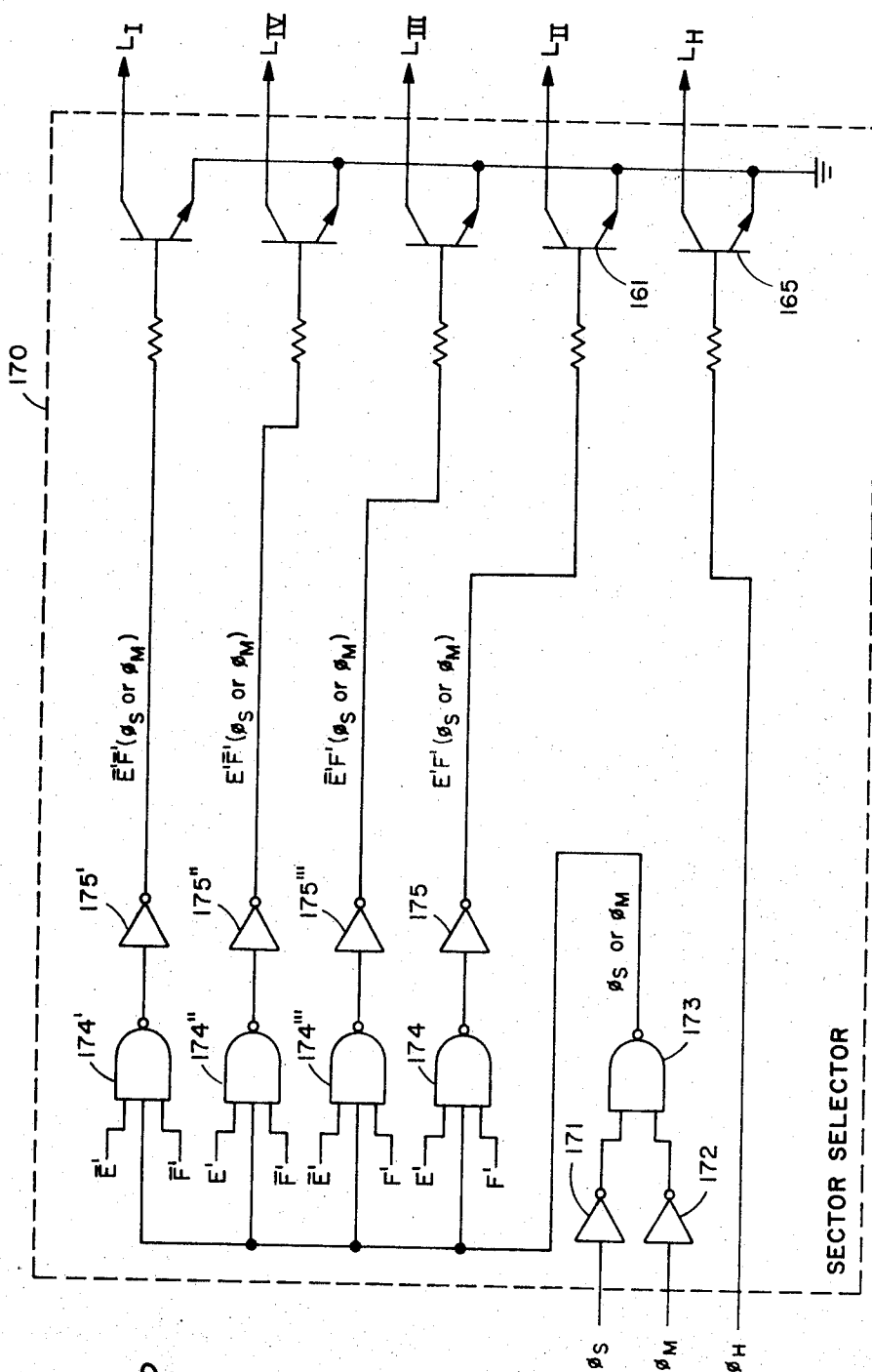


Fig. 12

INVENTOR
 R. Gary Daniels
 BY
Whitler & Archule
 ATTY'S

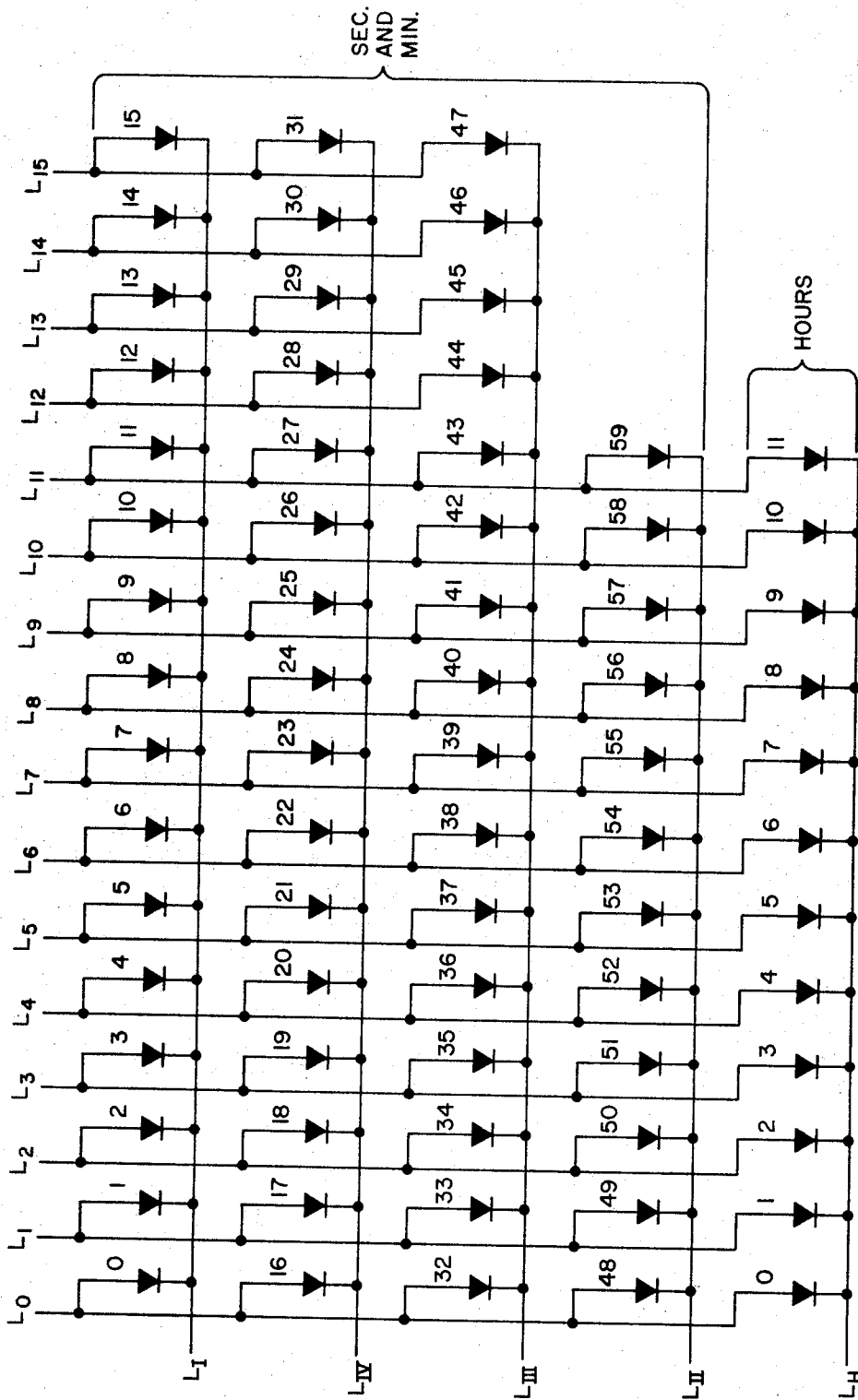


Fig. 13

INVENTOR
R. Gary Daniels
BY *Mueller & Co.*
ATTY'S

APPARATUS FOR DRIVING A LIGHT EMITTING DIODE OF HOROLOGIC DISPLAY

BACKGROUND OF THE INVENTION

This invention relates to horologic displays and more particularly to a system for providing a digital readout for a horologic display in which the minutes and seconds are displayed in a first ring of elements with the hours being displayed in a second ring of elements.

There has in the past been a great deal of interest shown in the provision of a digital readout for wrist watches. Wrist watches utilizing digital readouts have recently been provided with readouts in alpha-numeric form utilizing an XY addressable matrix of individual light emitting diodes. The circuits necessary for driving XY addressable light emitting diode arrays are well known. However, alpha-numeric light emitting diode displays suffer from one major problem when they are utilized to portray the time of day in a wrist watch. This problem is primarily power consumption. Power consumption is so great in wrist watches utilizing alpha-numeric displays that the battery for the wrist watch must be replaced within a matter of weeks if the display is to run continuously. The reason for the amount of power drawn by alpha-numeric display type wrist watches is the number of light emitting elements necessary to portray the time of day. In an effort to increase the lifetime of the wrist watch there is provision for intermittent readout which is activated by the user of the wrist watch. This is both inconvenient and annoying to the user.

The subject system is employed in a time readout of a different character altogether. The time of day is read out by a maximum of three light emitting diodes. In one configuration, 60 light emitting diodes are arranged in a ring and represent both minutes and seconds. An inner concentric ring of 12 light emitting diodes represents the hour of day. The time is read out in this display by providing that the hour diode be substantially continuously lit for the hour it represents. In the outer ring the minute diode remains lit substantially continuously for the minute that it represents. While the minute diode is lit the remaining diodes in the outer ring are lit sequentially so as to represent seconds. Thus, for any given minute all 60 diodes representing seconds are lit sequentially in a clockwise stepping type display. After the seconds have stepped around a full 60 seconds, the next minute diode is activated. It will be appreciated that in this type display the 60 diodes in the outer ring serve both to represent minutes and seconds. It will be further appreciated that the time of day can be read out with a maximum of 3 diodes during any given second. This compares to a maximum of 87 diodes to represent the time of day in alpha-numeric form.

The subject system is one which provides the logic and driving circuits necessary to actuate the above mentioned light emitting diodes in the proper sequence. In the concentric ring display, it is possible to reduce the current drawn by such a display to 5 milliamps or less by reducing what is known as the duty cycle of the display. This refers to the practice of lighting each light emitting diode, not continuously, but in a pulsed manner such that the diode is lit only for a certain percentage of time. The logic portion of the circuit to be described herein in combination with the driving

portion not only actuates the display in proper sequence, but also provides the low duty cycle. The logic and driver portions utilize only an insignificant additional amount of current therefore enabling a light emitting diode horologic display which can be read out in a substantially continuous manner for a period of time exceeding one year without the necessity of providing for intermittent readouts to extend battery lifetime.

Power consumption in the logic and driving circuits are kept to a minimum by the use of several individual concepts. The first of these concepts involves the use of two voltage levels in the operation of the display. For those circuits having a high frequency of operation (i.e., almost continuous operation), a lower voltage such as 1.5 volts is used to minimize power consumption. These type of circuits are the crystal oscillator circuit and the countdown circuit which are utilized in reducing the frequency of the crystal oscillator to 1 Hz. The remainder of the circuit, that is to say the minute, second and hour counting circuits, the multiplexer circuits, the decoding circuits, and the driving circuits, as well as the light emitting diodes themselves, are provided with a 3 volt supply. It will be appreciated that these latter circuits are operated at a considerably lower frequency than the countdown circuitry. Although the higher voltage is desirable in order to drive the light emitting diode elements, power is conserved because both the duty cycle of the light emitting diode elements and the duty cycle of the drive circuitry is reduced to as low as 12.5 percent total "on" time per element. Thus, while it is necessary to increase the voltage to these circuits in order to provide driving power for the light emitting display, this power is utilized over a low duty cycle which corresponds to a lower frequency of operation.

Another power saving portion of the invention involves the use of complementary metal oxide semiconductors (CMOS) as switching elements and in the counters. It will be appreciated that the metal oxide semiconductor devices draw current only when they are switching (i.e., changing state).

In addition to power consumption advantages of the subject circuit, the multiplexing circuit utilized herein eliminates redundancy in the decoder and driver elements necessary for driving the hours, minutes and seconds portions of the display. The numbers of elements are also decreased by provision of a quadrant or sector system of addressing the light emitting diode elements. An additional and a most important function of the multiplexing circuit is to reduce the aforementioned duty cycle. What the multiplexing circuit does is to sample the seconds, minutes, and hour counters at a high repetition rate with a low duty cycle as dictated by sampling pulses of short duration. If the information in the counters is sampled once every one sixty-fourth of a second, the information is actually flowing out of the multiplexer for only a small portion of this one sixty-fourth second time period due to the short sampling pulses. At all other times, the output of the multiplexer is inhibited. Thus the multiplexer in addition to sequentially reading out the information stored in the counters also serves the purpose of reducing the duty cycle ultimately for the light emitting diode in the display. A further advantage occurs with the multiplexing circuit when used in conjunction with a display in which time is displayed by three diodes. Although it looks as if

three diodes are continuously lit during one sampling cycle, this is not so. In any given sampling period only one diode is lit at a time. This is because the seconds, minutes and hours information is not simultaneously read out but rather is read out over mutually exclusive time intervals. This means that peak battery current drain is minimized so that high impedance batteries may be used.

The sampling is accomplished in the subject circuit by coincident gating within the multiplexer circuit. The timing pulses for the sampling are derived from the aforementioned divide-by-two countdown circuit which provides the 1 Hz signal for driving the counters.

In addition, the counters consist of toggle-type flip-flops which are so arranged to have a binary output. These toggle-type flip-flops are utilized rather than JK-type flip-flops because of the aforementioned decrease in number of transistors necessary. While toggle-type flip-flops are usually utilized only in countdown circuits, they are utilized in this application as binary encoders. In the configurations to be described herein the toggle-type counters are easily matched to a NAND-type decoder circuit which is also available in MOS form.

It will be appreciated that the choice of the two level voltage in a strobed multiplexer circuit, MOS type components and the logic to be described are important primarily because of power consumption savings. They are further chosen because of the saving of individual component parts. 11

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide an improved logic and driving system for use in light emitting diode horologic display.

It is a further object of this invention to provide in combination an oscillator circuit; a "divide-by-two" countdown circuit for providing a 1 Hz signal; seconds, minutes and hours counters cascaded to form storage elements having an output in binary form; a multiplexer circuit which provides for sequential readout of the seconds, minutes and hours counters as well as providing for a low duty cycle driving signal; a binary-to-pulse decoder, and a driving circuit which responds to the pulsed output of the decoding circuit for actuating individual light emitting diode elements in the horologic display.

It is a still further object of this invention to provide a horologic display in which the time is represented by an outer ring of elements representing seconds and minutes, and an inner ring of elements representing hours in which the outer ring of elements is divided into sectors such that all the elements are driven by a single driver connected in parallel with the corresponding elements in each sector and is further provided with a sector selector such that only one sector and therefore only one element in each sector is driven at any one given time.

It is a still further object of this invention to provide a driving circuit for a light emitting diode horologic display in which the high frequency circuits are powered by a first voltage while the lower frequency circuits are powered by a second voltage higher than the first voltage such that power consumption is minimized.

It is a still further object of this invention to provide a binary logic system utilizing toggle flip-flops and NAND gate reset logic to provide information which

when decoded and supplied to a driving circuit actuates the light emitting diode display.

It is a still further object of this invention to provide a multiplexed logic and driving circuit for light emitting diode display in which the multiplexing circuit samples seconds, minutes and hour information available in binary form from counters in a sequence and for a sampling duration which minimizes the duty cycle of the light emitting diodes in the display while at the same time conserving on the number of driving elements, thereby conserving greatly on the power dissipated both by the driving circuit and by the light emitting diode display elements.

It is yet another object of this invention to provide logic and drive circuitry for a horologic display utilizing a logic permitting the use of metal oxide semiconductor logic parts.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the logic and driving circuits for a light emitting diode display;

FIG. 2 is a diagrammatic view indicating the manner in which the time of day is read out from the aforementioned light emitting diode display, also indicating an asymmetrical sector arrangement indicating in addition the method of actuation from the output of the driver shown in FIG. 1;

FIG. 3 is a block diagram showing generically the circuit configurations of the multiplexer, the decoder, the sector selector, and the driver circuit, referred to in FIG. 1;

FIG. 4 is a pulse train diagram showing the sampling times and the sampling period of the pulses delivered to the multiplexer which in turn result in the aforementioned low duty cycle;

FIG. 5 is a block and schematic diagram of the frequency dividing circuit utilized to count down the frequency available from a crystal oscillator to 1 Hz also showing a pulse shaper and level translator utilizing in matching the high frequency section of the device to the low frequency section of the device;

FIG. 6 is a pulse train diagram showing the derivation of ϕ_s , ϕ_M and ϕ_H from intermediate outputs of the frequency dividing circuit shown in FIG. 5;

FIG. 7 is a block diagram of a binary seconds or minutes counter utilizing toggle-type flip-flops to indicate a binary number corresponding to integers between 0 and 59;

FIG. 8 is a block diagram of a counter circuit for indicating hours in binary form in which toggle-type flip-flops are utilized to represent in binary form integers between 0 and 11;

FIG. 9 is an expanded diagram of the multiplexer circuit shown in connection with FIG. 3;

FIG. 10 is an expanded diagram of the decoder circuit shown in connection with FIG. 3;

FIG. 11 is an expanded diagram of the driver circuit shown in connection with FIG. 3;

FIG. 12 is an expanded diagram of the sector selector circuit shown in connection with FIG. 3; and

FIG. 13 is a diagram showing the arrangement of the light emitting diodes to be driven by the output of the driver and sector selector circuits shown in connection with FIGS. 11 and 12.

BRIEF DESCRIPTION OF THE INVENTION

There is disclosed a logic and driving circuit for a

light emitting diode type horologic display in which three diodes are read out at any given time to represent the time of day. Power consumption is kept to a minimum by the use of a two voltage level system with the lower voltage supplying those portions of the circuit working at a high frequency while the higher voltage supplies the display and those portions of the driving circuit operating at a considerably lower frequency. In addition to a crystal frequency standard and a "divide-by-two" flip-flop countdown circuit which provides a 1 Hz signal to a series of toggle flip-flop counting circuits which function as the seconds, minutes and hours storage elements, there is provided a multiplexer coupled to the outputs of these counting circuits which is strobed with pulses having a combined duration of only a fraction of the sampling cycle. This results in a low duty cycle for the output of the multiplexer and thus for the display itself which conserves on the power necessary to drive the display. Since hour, minute and second information is sequentially sampled by the multiplexing circuit, multiplexing eliminates decoder and driver redundancy. Provision is made in the multiplexing logic for dividing the horologic display into quadrants or sectors so as to further reduce the number of driver and decoder elements. As a result there is also provided a quadrant selecting circuit. The sampling pulses for the multiplexing circuit are conveniently derived from the frequency standard countdown circuit. The driving system utilizes complementary metal oxide semiconductor (CMOS) components in which power drain is minimized because these elements draw appreciable power only when switching. A further power consumption advantage is obtained by utilizing NAND gate logic to permit the use of these low power CMOS components. Toggle flip-flops are chosen for the counters because they are available in metal oxide semiconductor form and because the total number of transistors utilized is reduced. The logic described herein is used with a horologic display in which the minutes and seconds are displayed in the single ring of elements with the hours being displayed in another single ring of elements.

DETAILED DESCRIPTION OF THE INVENTION

As mentioned hereinbefore the subject logic and driving circuit is tailored to a type of horologic display in which the time of day is read out by three light emitting diode elements. It will be appreciated, however, that many of the concepts utilized in power conservation in the driving of this display can be equally well utilized in the driving of any XY addressable display in which power consumption is a major factor. Thus, although the subject logic and driving circuits are described in connection with the horologic display in which the time of day is represented by two rings of light emitting elements, any system in which pulses are provided on output lines of a driving circuit is within the scope of this invention.

Referring now to FIG. 1, a horologic display 100 is shown with an outer ring 101 of 60 light emitting diodes, and an inner ring 102 of 12 diodes. The time of day in this display is indicated by the sequential activation of the individual light emitting elements. In this display, minutes and seconds are represented by utilizing the same set of light emitting elements. The importance of representing time by using the same light emitting elements for seconds and minutes is the saving of

as many as 60 light emitting elements. The display to which the subject logic is tailored therefore minimizes the number of light emitting elements by portraying minutes and seconds on the same ring by the same set of elements. There are of course other ways of representing time utilizing concentric rings of time indicating elements in which multiplexed readout of counters having binary outputs drives these elements. In addition, for instance additional elements may be added to indicate half hour of 20 minute intervals. In the configuration shown involving a set of 60 elements arranged so as to define a closed geometric curve or ring 101, minutes are portrayed by sequentially actuating successive light emitting elements clockwise around the ring 101 within "on" durations of 1 minute. Simultaneously, each of the elements in this ring are lit sequentially in a clockwise direction for one second such that at any given minute the seconds indications have been stepped around the ring until they reach the 12 o'clock position. At this time the minute indication is stepped ahead so as to indicate the start of a new minute with the second indicator corresponding to the first second of this new minute. The hours are represented by the concentric ring 102 which are actuated sequentially having a 1 hour duration. The time indicated by the display 100 as shown by the darkened light emitting diodes 103, 104 and 105 is 1:12 and 39 seconds.

The driving circuit for display 100 generally consists of a frequency standard indicated by oscillator 110 and countdown circuit 115, which produces a precise 1 Hz signal. This signal is coupled through a level translator 120 to a second series of countdown circuits involving counters 130, 131 and 132 which serve as storage elements for seconds, minutes and hours information. The output of these counters is in binary form such that the information contained in each one of these counters is sequentially read out or sampled by a multiplexing circuit 140. The binary information sampled by the multiplexing circuit is coupled to a decoding circuit 150 which provides a pulse of one of 16 output lines depending on the binary number stored in the particular counter read out by the multiplexing circuit 140. This pulse activates a driver circuit 160 which in turn drives simultaneously all five of the sectors into which the display 100 has been divided. In addition, a portion of the output of the multiplexer circuit drives a sector selector 170 which selects which of the aforementioned five sectors is to be enabled. The enabling of only one of the five sectors results in the activation of only one diode for each sampling pulse to the multiplexer circuit 140. The inner ring 102 of 12 diodes representing hours is in essence one sector which is activated in the timed sequence determined by the multiplexer circuit such that when the hour counter is read out by the multiplexer circuit, the sector selector is directed to enable the hour sector. The minutes-seconds ring 101 is divided into four sectors so that both the sector and the particular element in the sector must be driven to light a particular element.

Referring to the oscillator 110, it is a crystal oscillator with the crystal 111 having a frequency of 65, 636 Hz. This corresponds to 2^{16} Hz. The output of the oscillator is coupled to a "divide-by-two" countdown circuit shown diagrammatically in the dotted box 115. This is composed of a series of flip-flops shown diagrammatically at 116 which basically divide the output of the preceding flip-flop by two. Thus, by the use of 16 indi-

vidual flip-flops, the 2^{16} Hz oscillator output is reduced to 1 Hz. There are however intermediate outputs from the countdown circuit which are utilized for forming the sampling pulses for the multiplexer. These readouts are tapped from the outputs of various of the flip-flops and represent respectively a 256 Hz signal, a 128 Hz signal, and a 64 Hz signal. These intermediate signals are coupled to the pulse shaper and level translator 120 and thence to the multiplexer circuit 140 where they serve to cycle the multiplexer such that a sampling period takes one sixty-fourth of a second with the individual sampling times occupying in one embodiment only 12.5 percent of this one sixty-fourth sampling period. As mentioned hereinbefore, the high frequency circuits are supplied with a lower voltage, thus conserving power. The high frequency circuits are the oscillator circuit 110 and the countdown circuit 115. In order to enable the use of the pulsed signals generated by the countdown and oscillator circuits, there is of necessity a level translator which makes the signals at the output of the countdown circuit compatible with those of the multiplexer and the counter circuits 130, 131 and 132. The 256 Hz signal has a dual purpose insofar as it is utilized in forming the sampling pulses for the multiplexer circuit 140 and as speeds time setting signal. As can be seen, the output of the level translator 120, at least in one configuration, is a 1 Hz signal designated Y, and a 256 Hz signal designated by the letter Z. In ordinary operation the switch 136 is in the position shown coupling the counters 130, 131 and 132 to the 1 Hz signal. If, however, it is desired to change the time displayed by the subject horologic display, switch 136 is coupled to a higher frequency signal, in this case the 256 Hz signal, which speeds up the counting operation until the appropriate time is reached at which point switch 136 is returned to the position shown in FIG. 1. This 1 Hz output signal is coupled directly to the seconds counter 130 which operates in such a manner as to count the number of bits of information delivered thereto between "0" and "59" (i.e., 60 bits). The state of the counter is indicated by a binary output of 6 bits as shown by the output lines 133. In the configuration shown, the state of the counter is changed on the negative going edge of an incoming pulse. What this means is that the flip-flops used in the counters are set by the leading edge of an incoming pulse and are toggled by the trailing edge. After 59 bits have been counted, seconds counter 130 resets and also simultaneously delivers a first pulse to the minutes counter 131. Minutes counter is identical to the seconds counter in that it has 6 flip-flops. Thus its state is also represented by a binary number of 6 bits. The output in binary form of the minutes counter 131 is shown by the output lines 134. Thus, the seconds counter 130 must cycle through all of its 60 bits before the minute counter receives its first pulse. Likewise, the minute counter must cycle through its 60 bits before the hour counter 132 receives its first pulse. The hour counter is provided with four flip-flops and thus its state is represented by the four output lines 135. At the end of 12 bits this counter is reset. It will be appreciated that counters 130 and 131 have six flip-flops each. It is therefore possible for these counters to count up to 63 in binary form. However, these counters are reset after they reach a count of 59 by a logic to be described hereinafter. Likewise, counter 132 can count up to 15. However, this counter is reset after it reaches a count of 11, thus representing 12 bits. These count-

ers, as mentioned hereinbefore, are constructed of toggle-type flip-flops with attendant NAND gate logic circuitry to make the counters operate in the above fashion. They are toggle-type flip-flops rather than JK-type flip-flops because toggle-type flip-flops use less transistors in the form shown than do JK flip-flops. As has been mentioned hereinbefore that the available of these devices in MOS form contribute significantly to power consumption reduction. It will be appreciated that there is an analog in the JK flip-flop counter art to the toggle flip-flop once the NAND gate-inverter logic shown in connection with FIGS. 7 and 8 is known. Also, any binary encoders which count pulses and generate a binary output can be used with the multiplexer.

In the configuration shown, the information in binary form is available at outputs 133, 134 and 135 which are coupled to the multiplexer circuit 140. The multiplexer circuit is basically a coincident gate-type circuit such that when enabling pulses ϕ_S , ϕ_M , or ϕ_H appear, either the seconds counter or the minutes counter or the hours counter is read out to both the decoder unit 150 and the sector selector 170. ϕ_S , ϕ_M , and ϕ_H are generated from outputs of the countdown circuit 115 by the pulse shaping portion of the level translator 120. After ϕ_S , ϕ_M and ϕ_H are generated, they are level translated by level translator 120 so as to be compatible with the multiplexer circuit 140 which generally operates at 3 volt level as opposed to the 1.5 volts supplied to the high frequency circuits mentioned hereinbefore. ϕ_S , ϕ_M and ϕ_H are not however coextensive with the outputs of the various flip-flops from which they are derived. As will be discussed in FIG. 5, the outputs of the three selected flip-flops from which ϕ_S , ϕ_M and ϕ_H are derived are coupled to NAND gate circuitry such that a series of three sequential pulses are produced spaced apart by considerable "dead air time." ϕ_S , ϕ_M and ϕ_H are coupled to the multiplexer 140 to cause the multiplexer to sample the outputs of the counters in mutually exclusive and separated time intervals within the sampling cycle. The sampling takes place only over the time at which ϕ_S , ϕ_M and ϕ_H appear. This results in the seconds counter being read out during the duration of the pulses ϕ_S , the minutes counter being read out during the duration of the pulse ϕ_M , and the hour counter being read out during the duration of the pulse ϕ_H . At all other times the output of the multiplexing circuit is a binary coded set of words which are incapable of actuating any light emitting diodes in the display. Thus when the term "low duty cycle" is used it refers to the fact that the light emitting diodes have a low duty cycle. In actuality none of the other components in the system are inhibited during "dead air time." It is sufficient that only the display has the low duty cycle since it draws the majority of the power. In one embodiment the sampling time for one ϕ pulse is only 12.5 percent of the entire sampling cycle. If three samples (i.e. ϕ_S , ϕ_M and ϕ_H) are made during the sampling cycle the sampling pulses take up only 37.5 percent of the sampling period.

As mentioned hereinbefore the output of the multiplexer in addition to being coupled to the decoder 150 which decodes either the seconds, minutes or hours numbers, is also coupled to the sector selector 170. It will be appreciated that the aforementioned ring of 60 elements is divided into four parts or sectors. These parts are, however, not equal for reasons which will be described hereinafter. At this point it is only necessary

to note that the sector selector is activated by the last two bits of information from either the seconds counter or the minutes counter. The hours sector is activated merely by a pulse appearing on the line ϕ_H since it is completely separate from the other four sectors utilized to activate the outer ring of elements. However, the outer ring of elements being divided into four parts must be actuated in some orderly manner depending on the numbers in the seconds and minutes counters. The sector which these numbers occupy is conveyed to the sector selector as the last two bits of information in each one of these counters. These last two bits of information in conjunction with ϕ_S , ϕ_M and ϕ_H instruct the sector selector in which sector the information being read out by the multiplexer 140 is to be placed. Thus, although there are 60 elements in the outer ring 101, the driver need only have 16 outputs as shown in FIG. 1. These 16 outputs are connected in parallel to corresponding elements in each one of the first three sectors. The fourth and hour sectors however have only 12 elements and therefore only the first 12 of the output lines of the driver are connected in parallel to corresponding elements both in sectors I-III and the fourth and hour sectors. Actually, the fourth sector is designated sector No. II in keeping with "quadrant" designation commonly used in analytic geometry.

Neglecting for the moment the hours activation, the minutes and second activation is accomplished by the use of only 16 driving lines and four "quadrants" making this akin to an XY addressable array. If, for instance, 10 minutes past the hour is to be represented, during the minutes segment of the multiplexing, "quadrant" I is enabled by grounding it, while the binary number corresponding to 10 is decided by the decoder 150. The decoding circuit enables a section of the driver 160 which then connects to V_{CC} one electrode of corresponding elements No. 10 in each of the sectors. Thus V_{CC} is fed in parallel to the element No. 10 in "quadrant" I, the element No. 10 in "quadrant" II, the element No. 10 in "quadrant" III, and the element No. 10 in "quadrant" IV. However, since only "quadrant" I is grounded, diode No. 10 in "quadrant" I is the only diode which is connected between V_{CC} and ground.

Outputs zero through 11 of the driver 160 are also coupled to the inner ring of elements 102 such that the No. 10 element is also connected to V_{CC} via output line 10. However, since only "quadrant" I is activated, the delivery of this pulse to this element has no effect. However, if 10 o'clock is to be represented, then the hour sector is grounded in conjunction with the connection of V_{CC} to the No. 10 element via output line 10. This causes the 10th diode in the inner ring 102 to become lit during that portion of the multiplexer sequence which reads out the number 10 contained in binary form in hour counter 132. Thus, it can be seen that the sector selector 170 is only necessary to distinguish between seconds readouts and minutes readouts with the hours readouts being directly actuated by ϕ_H shown to pass directly through the sector selector 170. As mentioned hereinbefore the minutes and seconds readout is a bit more complicated. During the time when the seconds are read out, the last two bits in the seconds counter instruct the sector selector 170 to actuate the appropriate "quadrant." When it becomes time for the minutes counter to be read out, the multiplexer also instructs sector selector 170 which "quad-

rant" is to be actuated. However, since the hours are not segmented in any form there is no necessity to instruct a sector selector which "quadrant" to actuate because there is only one sector as far as the hour light emitting diodes are concerned. It will be appreciated that there are five sectors, with the first four sectors designated as "quadrants" so as to distinguish outer ring actuation from that of the inner ring.

The matter of actuation of this subject display is described in connection with FIG. 2. In this diagram, the minute-second portion of the display is divided up into four "quadrants" as shown. The first "quadrant" has 16 light emitting diode elements associated with it. These run from positions zero through 15. Going clockwise the fourth "quadrant" also has 16 elements going indicated from positions zero through 15 as does the third "quadrant." The fourth "quadrant" however has only 12 elements which run from positions zero through 11. This asymmetric division of the of the elements is indicated by the particular seconds, minutes and hours counters employed. It is of course possible to use other types of counters such that the "quadrant" representation is made symmetrical. However, if symmetrical "quadrants" are used more complicated decoders and more complicated counters are necessary. It will be appreciated that the asymmetrical division of "quadrants" described is chosen because it greatly simplifies the logic circuitry required. For example, if four equal "quadrants" of 15 elements each are employed with a 6 bit 0-59 counter, counter outputs 16, 31 and 47 would not be decoded although they are states of the counter which exist during each cycle. Thus, an error of 3 units per cycle would be introduced. To circumvent this problem four 0-14 counters could be used instead of one 0-59 counter for seconds and minutes. This would require 16 flip-flops instead of 6 flip-flops as described herein. The outputs from driver 160 of FIG. 1 are shown to the bottom left-hand side of diagram shown in FIG. 2. It will be appreciated that the outputs from the driver 160 are connected in parallel not only to those corresponding elements in each one of the "quadrants," but also to the corresponding element in the hour ring (hour sector). Thus, the zero output line is connected to the "quadrant" I zero, the "quadrant" II zero, the "quadrant" III zero, and the "quadrant" IV zero as well as to the hour sector zero which in this case represents the hour of 12 o'clock. Likewise, for instance, the 11th output is coupled simultaneously to the 11th element in the first "quadrant," the 11th element in the second "quadrant," the 11th element in the third "quadrant," and the 11th element in the fourth "quadrant." It is also connected to the 11th element in the hour ring (hour sector). Output lines 12 through 15 are however only connected to those corresponding elements in "quadrants" I, III and IV. It will be obvious that there is no element for them to be connected to in "quadrant" II or in the hour ring sector. As mentioned hereinbefore, the hour ring is represented by a single sector which is driven or actuated during the hour readout portion, ϕ_H , of the multiplexing cycle. However, for the seconds and minutes readout the "quadrants" I, II, III and IV are read out in accordance with the binary number in the seconds or minutes counter which is activated or read out by the multiplexer 140. Thus, there are only three light emitting diodes read out in a given sampling cycle. In the embodiment shown in the Figures, the minute, second

and hour are read out once every one sixty-fourth of a second or 64 times a second. This provides for a seemingly continuous readout of the light emitting diode display. It is however not continuous since the sampling cycle takes place over one sixty-fourth of a second and the actual readout takes place over only 12.5 percent of the cycle. Thus the diodes in the display are lit for only 12.5 percent of the time. This 12.5 percent figure in conjunction with the one sixty-fourth of a second sampling rate provides the user with what appears to be a continuous readout of a time period in excess of one year. It will be appreciated that other acceptable duty cycles are feasible going as low as 1.56 percent and as high as 25 percent.

The logic involved in the subject system is now described in general. As mentioned hereinbefore, each of the aforementioned counters 130 through 132 have an output in binary form. The output for the seconds counter 130 is in the form of 6 bits designated A_S through F_S . The binary output of the minutes counter 131 is designated A_M through F_M and the output of the hours counter is designated A_H through D_H . For reference the corresponding binary number table of 0 through 63 is now presented.

TABLE I

No.	F	E	D	C	B	A	No.	F	E	D	C	B	A
0	0	0	0	0	0	0	32	1	0	0	0	0	0
1	0	0	0	0	0	1	33	1	0	0	0	0	1
2	0	0	0	0	1	0	34	1	0	0	0	1	0
3	0	0	0	0	1	1	35	1	0	0	0	1	1
4	0	0	0	1	0	0	36	1	0	0	1	0	0
5	0	0	0	1	0	1	37	1	0	0	1	0	1
6	0	0	0	1	1	0	38	1	0	0	1	1	0
7	0	0	0	1	1	1	39	1	0	0	1	1	1
8	0	0	1	0	0	0	40	1	0	1	0	0	0
9	0	0	1	0	0	1	41	1	0	1	0	0	1
10	0	0	1	0	1	0	42	1	0	1	0	1	0
11	0	0	1	0	1	1	43	1	0	1	0	1	1
12	0	0	1	1	0	0	44	1	0	1	1	0	0
13	0	0	1	1	0	1	45	1	0	1	1	0	1
14	0	0	1	1	1	0	46	1	0	1	1	1	0
15	0	0	1	1	1	1	47	1	0	1	1	1	1
16	0	1	0	0	0	0	48	1	1	0	0	0	0
17	0	1	0	0	0	1	49	1	1	1	0	0	1
18	0	1	0	0	1	0	50	1	1	0	0	1	0
19	0	1	0	0	1	1	51	1	1	0	0	1	1
20	0	1	0	1	0	0	52	1	1	0	1	0	0
21	0	1	0	1	0	1	53	1	1	0	1	0	1
22	0	1	0	1	1	0	54	1	1	0	1	1	0
23	0	1	0	1	1	1	55	1	1	0	1	1	1
24	0	1	1	0	0	0	56	1	1	1	0	0	0
25	0	1	1	0	0	1	57	1	1	1	0	0	1
26	0	1	1	0	1	0	58	1	1	1	0	1	0
27	0	1	1	0	1	1	59	1	1	1	0	1	1
28	0	1	1	1	0	0	60	1	1	1	1	0	0
29	0	1	1	1	0	1	61	1	1	1	1	0	1
30	0	1	1	1	1	0	62	1	1	1	1	1	0
31	0	1	1	1	1	1	63	1	1	1	1	1	1

As shown at the bottom on FIG. 3, the outputs of counters 130 and 131 and 132 are coupled to the multiplexer circuit 140. In general, each of the corresponding outputs of each of the counters is connected as shown in the multiplexer circuit to three corresponding NAND gates 141, 142 and 143. The outputs of these NAND gates form the inputs for a further NAND gate 144. "Positive true" logic is used in this system (i.e., a logic "1" is represented by a positive voltage potential approximately equal to the supply voltage whereas a logic "0" is represented by an approximately zero voltage potential). The NAND gate produces a logic high or "1" output if one or more of its inputs are low. A logic low is generated if, and only if, all of the inputs are high. Taking, for instance, the A output from each of the counters (A_S , A_M , A_H), each of these form one of the inputs for the aforementioned NAND gates 141 through 143. The other input for each of the NAND

gates 141 through 143 is the sampling signal which permits readout of the particular counter. For instance, if it is desired that the seconds be read out a logic "1" signal ϕ_S is applied simultaneously with the A_S signal to NAND gate 141. If A_S is a logic "1" signal, the coincidence of the ϕ_S and the A_S signal results in a logic "0" signal $\overline{A_S \phi_S}$. This signal is coupled to NAND gate 144 such that a logic "1" output of gate 144 indicates the simultaneous presence of an A_S logic "1" signal and the ϕ_S signal. NAND gate 144 produces this logic "1" signal because the other signals to this NAND gate will be logic "1" during the presence of a sampling pulse. Thus during sampling only one signal from gates 141-143 will be low. This is the condition of a logic "1" output from NAND gate 144. The same is true for the minutes sampling signal ϕ_M and the hours sampling signal ϕ_H . It can be seen therefore that the multiplexer utilizes coincident-gate sampling. The multiplexer section shown in FIG. 3 is but one of many such sections corresponding to the six outputs from the seconds and minutes counters and the four outputs of the hours counter. The output of gate 144 is a logic level signal which indicates the simultaneous presence of either A_S and ϕ_S or A_M and ϕ_M , or A_H and ϕ_H signals. There is also provided in the multiplexer an inverter circuit 145 which produces the complement of that which is produced at the output gate 144. The analysis of the multiplexer circuit is a direct consequence of demorgan's laws.

The output of the multiplexer circuit is coupled to the decoding circuit 150 which in general is a simple circuit involving 16 NAND gates. One of these gates is represented by the reference character 151 to be that corresponding to the A', B', C', D' outputs of the multiplexer corresponding to the A, B, C and D outputs from a counter. The prime after these letters indicates that these are in fact sampled. In other words, there is either a ϕ_S , a ϕ_M or ϕ_H which enables the information A, B, C, and D to be read out. Referring to Table I, the presence of logic "1's" in A, B, C, and D represent the number 15, the number 31, and the number 47. the selection of which of these numbers is represented by the display is accomplished by the sector selector 170. Ignoring for the moment the hours indications since this number does not exist on the hours ring, the input to the sector selector is two fold. The first inputs are the enable inputs, ϕ_S and ϕ_M . These are coupled to inverters 171 and 172 such that the output thereof is $\overline{\phi_S}$ and $\overline{\phi_M}$ (i.e., logic "0's"). Utilizing a further NAND gate 173 its output is a logic "1" when ϕ_S or ϕ_M are present at inverters 171 and 172. Thus whenever ϕ_S or ϕ_M is present the "quadrant" portion of the sector selector 170 is enabled. This means that there is a logic "1" signal at one of the inputs to NAND gate 174. The output of gate 173 is thus an input to gate 174 which is also a NAND gate. The other two inputs to this gate are the E' and F' outputs from the multiplexer circuit and thus correspond to the sampled E or F outputs from the minutes and seconds counter. In this case the F output of the counter is a logic "0." This is recognized by the multiplexer which generates a logic "1" signal on its F' output line. The multiplexer generates logic "1" signals indicating a logic "0" signal from a counter. Thus all "X" signals referred to herein are available as logic "1" signals from the multiplexer. E' and F' indicate that a logic "1" exists at NAND gate 174. With three logic "1" signals (E', F', ϕ) the output of gate 174 is low.

This is converted to a high signal by inverter 175. This logic high signal then renders NPN transistor 161 conductive. From Table I the presence EF indicates that the number 31 is to be selected over the number 15 and the number 47. To reiterate, the output of the NAND gate 174 in combination with the inverter circuit 175 indicates that there is a sampling of either the seconds or the minutes counter, and that the "quadrant" indicating the number 31 should be activated. This "quadrant," referring to FIG. 2, is "quadrant" IV. A logic "1" signal therefore from the output of inverter 175 is delivered to the base of the NPN transistor 161 in the driver circuit 160. This particular NPN transistor is coupled between one electrode of each of the light emitting diode devices 162 of "quadrant" IV and ground. The other electrode of these light emitting diodes is connected to the collectors of PNP transistors 163 whose emitters are connected to $V_{CC} = 3$ volts. The output of the decoder gate 151 is coupled simultaneously to the base of those transistors coupled to corresponding light emitting diodes in each "quadrant." Thus a logic "0" generated by the presence of A', B', C', D' at NAND gate 151 is coupled to the base of transistor 163' at the same moment that a logic "1" is delivered to the base of transistor 161. Thus the LED 162' is connected to both V_{CC} and ground.

For any given state of the decoder 150 and the sector selector 170, only one diode is actuated or lit. The results in the aforementioned low peak current drain and the feasibility of using low cost high impedance batteries.

Referring now to the hours actuation, the presence of ϕ_H at the base of transistor 165 enables all of the light emitting diodes 166 in the hour ring. If, for instance, the decoder gate corresponding to A', B', C' and D' were actuated, corresponding to a count in the hours counter of 0000, then at sampling time ϕ_H , the diode representing 12 o'clock would be lit. This is because the particular decoder gate produces a logic "0" signal when logic "1" signals $\bar{A}$, $\bar{B}$, $\bar{C}$ and $\bar{D}$ occur at the NAND gate in the decoder. All of the other gates have logic "1" outputs. The gating in the driver circuit simply renders conducting the transistors on either side of the light emitting diode which is to be actuated. The diode is therefore connected between a 3 volt power supply and ground through the NPN and PNP transistor across which it is connected in series. Various biasing resistors 167 are provided to complete the partial schematic diagram of the driver circuit 160 shown in FIG. 3.

Referring now to FIG. 4, it will be apparent that the entire multiplexer circuit operates on the principle of coincident gating. However, the sampling period is dictated by the length of the sampling pulses, ϕ_S , ϕ_M , and ϕ_H . The length of the sampling pulses is considerably reduced by narrowing these pulses. Since the output of the multiplexer circuit 140 actuates the display, only during the presence of a sampling pulse, by narrowing the sampling pulses the output of the multiplexer can be maintained at a zero level for a considerable portion of time. As shown in FIG. 4, in one embodiment the sameplng cycle is one sixty-fourth of a second as shown by the distance between the leading edges of consecutive pulses 180 and 181 of the ϕ_S sampling pulse train. However, the combined widths of pulses 180, 182 and 183 only occupy about 12.5 percent of the one sixty-fourth second time period. The duty cycle

for this logic and driving system is therefore defined to be the combined pulse widths of the seconds, minutes and hours sampling signals as compared with the length of time between the leading edges of two consecutive ϕ_S sampling pulses. Since the output of the multiplexer does not actuate the display for approximately 87.5 percent of the time, the decoder circuit, sector selector circuit and the driver circuit are actuated for only 12.5 percent of the time that the display is running. Thus, the light emitting diodes are actuated for only 12.5 percent of the time that the display is running. Since NAND gate circuitry is utilized, and since complementary metal oxide semiconductor devices are utilized, the power saving with the circuit thus described in general, is considerable.

A more detailed description of the operation of the preferred embodiment of this invention is now described in detail in connection with FIGS. 5 through 13.

Referring now to FIG. 5, an expanded diagram is shown in which the signals ϕ_S , ϕ_M , ϕ_H , Y and Z are derived. Included in dotted box 115 are the last nine of the flip-flops in the countdown circuit 115. As can be seen, these are labeled F/F₁ through F/F₉. Each flip-flop has two outputs. The first being a $\bar{Q}$ output, and the second being the Q output. As mentioned hereinbefore, the output of F/F₁ is a 1 Hz signal. Since the countdown circuit 115 is supplied with a 1.5 volt potential, the output Q₁ must be converted to be compatible with the 3 volt follow-on systems. In order to accomplish this, the Q₁ output is coupled to the base of an NPN transistor 121 in the pulse shaping and level translating circuit 120. When transistor 121 is "off," the voltage at point 122 is high since no current is being pulled through this transistor. This voltage then corresponds to the 3 volt potential at point 123. When, however, Q₁ is applied to the base of transistor 121 as a logic high, transistor 121 goes into conduction pulling the point 122 low by the IR drop across the resistor 124. Thus the output Y is an inverse replica of the output Q₁. This same procedure is used for the time set output Z enclosed in dotted box 125. Here the transistor 121' is coupled to the Q₉ output of F/F₉. When the Q₉ output of F/F₉ is high, 122' is low because of the voltage drop across the resistive element 124'. The time set signal is equal to 256 Hz which in the worse case can reset the clock in about 6 minutes. It will however be appreciated that the tap for the base of transistor 121' can be taken off a higher numbered flip-flop such that the frequency of the signal at Z is increased proportionately thereto. The signals ϕ_S , ϕ_M , and ϕ_H are derived from the Q₉, Q₈, $\bar{Q}_8$, Q₇ and $\bar{Q}_7$ outputs of flip-flops 116 as follows. As shown, the Q₉ output of F/F₉ is coupled to one of the inputs of each of NAND gates 126, 127 and 128. The $\bar{Q}_8$ output of F/F₈ is coupled to another of the inputs to NAND gate 127. The Q₈ output of F/F₈ is coupled to another of the inputs of NAND gates 126 and 128. The $\bar{Q}_7$ output of F/F₇ is coupled to the last of the inputs to NAND gate 128 while the Q₇ output of F/F₇ is coupled to the last of the inputs to NAND gates 126 and 127. The outputs of these NAND gates drive the bases of transistors 121'', 121''', and 121'''' respectively. The boolean algebraic expressions for the outputs of NAND gates 126 through 128 are as shown. By going through demorgan's theorem recognizing the properties of the level shifting transistors 121, ϕ_S , ϕ_M and ϕ_H are generated as shown in FIG. 6 having been derived from the outputs

of F/F_9 , F/F_8 and F/F_7 . The remaining resistors 119 are for biasing purposes. It will be appreciated that the pulse widths of ϕ_S , ϕ_M and ϕ_H are equal to that of Q_9 , but the repetition rate is equal to that of Q_7 . Thus the combined pulse widths of ϕ_S , ϕ_M and ϕ_H are only 37.5 percent of the period of Q_7 .

Referring now to FIG. 7, the seconds/minutes counter is shown in dotted outline. The toggle flip-flops described herein require two "trigger" (or clock) pulses which are out of phase T and $\bar{T}$. The flip-flops trigger (i.e., change state) upon the transition of the T input pulse from a high to a low state. The toggle flip-flops employed require only 17 MOS transistors per flip-flop which is about one-half the transistors required for a JK flip-flop. Thus, while more NAND gates and inverters are necessary to make a counter (0-59) or (0-1) with toggle flip-flops than JK flip-flops, the total numbers of transistors required for a counter may be less with toggle flip-flops. It should be noted through-out the following discussion of the operation of the counters that the first pulse is the "0th" pulse and the 59th pulse therefore represents a count of 60. Likewise, in the hours counter the 11th pulse represents a count of 12. This agrees with the boolean Table I. Taking, for instance, this counter as the seconds counter 130, it is composed of six toggle flip-flops 138 labeled A, B, C, D, E, and F respectively. It is the purpose of this counter to store the number of pulses received of from zero through 59. If it were the purpose of this counter to recognize zero through 63 incoming pulses, the toggle flip-flops would be cascaded in the normal manner, and no additional logic elements (NAND gates and inverters) would be required. However, in order to stop the toggle flip-flop count at a point corresponding to the 59th incoming pulse and to reset it after this 59th incoming pulse requires the use of NAND gate logic coupled with the inverters as shown. This NAND gate logic assures that the outputs of the six flip-flops are all reset to zero on the trailing edge of the 59th pulse. The system for limiting the count of this counter centers around the use of four NAND gates and four inverter circuits. The input to the counter is the 1 Hz Y signal across the switch 136 which goes directly to the T input of flip-flop 138A. The Y signal is inverted by the inverter 137 and is then coupled to the T input of this first toggle flip-flop. The outputs of the first toggle flip-flop (138A) are coupled directly to the inputs of the 138B toggle flip-flop. Thereafter the switching theory becomes indeed complicated. Referring to Table I, and remembering that the flip-flops toggle on the negative going edge of a pulse it will be appreciated that in the seconds/minutes counter, if the counter is allowed to run up past 59 counts, nothing needs to be done about inhibiting the input to flip-flops 138A and 138B because the change from 59 to 60 is the same as a change from 59 to zero (i.e., the outputs of flip-flops 138A and 138B will be the required "zero" after the 59th pulse has passed). The 138C counter after the 59th pulse would ordinarily go to a logic "1." Some type of circuitry is therefore needed to maintain the output of flip-flop 138C at its zero level (no toggle). The inputs to flip-flop 138C are therefore inhibited during the passage of the 59th pulse so that the trailing edge of the 59th pulse does not toggle flip-flop 138C. The passage of the 59th pulse is indicated when D, E and F are all logic "1's" and B goes from a high to a low. D, E, and F are thence the inputs

to a NAND gate as shown by 139'. An output low from gate 139' indicates the presence of D, E and F at its inputs as logic "1's". This output low (i.e., logic "0") is coupled to one of the inputs of a NAND gate 139". The input to flip-flop 138C is ordinarily the B output of flip-flop 138B. What is done in effect is to inhibit this B output of flip-flop 138B from reaching the input to flip-flop 138C when D, E, and F are present at the output of their respective flip-flops and when B goes from a logic "1" to a logic "0." From the first table, D, E, and F are logic "1's" from 56 through 59. However, during this interval B only goes from a high to a low after the 59th pulse. The fact that B goes from a low to a high does not trigger the 138C flip-flop. The toggle flip-flop only changes state when its input goes from a logic high to a logic low (the negative going edge of a pulse). Therefore, the only time at which the input to 138C is inhibited is after the 59th pulse input. The T input to flip-flop 138C is therefore the output of inverter 146' (i.e., $B \overline{DEF}$). The output of gate 139' ($\overline{BDEF}$) is thence coupled to the $\bar{T}$ input of flip-flop 138C to complete the toggling.

At the passage of the 59th pulse flip-flops D, E, and F would not normally change state and would be logic "1." It is therefore necessary in order to return the counter to the 000000 first state to cause flip-flops D, E, and F to toggle. Since these flip-flops are cascaded, it is only necessary to toggle the D flip-flop in order to toggle E and F flip-flops back to the original $D=0$, $E=0$, and $F=0$ state. This is accomplished as follows: Normally flip-flop 138D toggles in response to the output of flip-flop 138C changing from a logic "1" to a logic "0". This is because the output of 139'" goes low on the appearance of a logic "1" pulse at the $\bar{C}$ output of the 138 flip-flop. However, flip-flop 138D is made to toggle either on the $\bar{C}$ input to gate 139'" or on an $\overline{ABDEF}$ condition since the $\overline{ABDEF}$ condition occurs only on the 59th pulse on the 60th pulse. A and B change to a zero which causes the output of 139'" to go high. This causes the output of 139'" to go low, thus toggling the flip-flop 138D. Therefore, flip-flop 138D while not ordinarily being toggled after the 59th pulse is in fact toggled so as to return the counters 138D, 138E, and 138F to a zero state. The $\overline{ABDEF}$ signal is derived as follows: The output of NAND gate 139' is $\overline{DEF}$. This is inverted to DEF by inverter 146''. The output of the inverter 146'' is an input to NAND gate 139''. A and B signals from flip-flops 138A and 138B form the other two inputs to NAND gate 139''. The output of NAND gate 139'' is low when $\overline{ABDEF}$ signals are present at their respective flip-flops. The output of NAND gate 139'' is thus $\overline{ABDEF}$. This is coupled as one of the inputs to NAND gate 139'" along with a $\bar{C}$ input. The $\bar{C}$ input normally toggles flip-flop 138D. The presence of the $\overline{ABDEF}$ condition indicates the passage of the 59th pulse. Since the 59th pulse is indicated by $\overline{ABDEF}$, going from $\overline{ABDEF}$ to $\overline{ABDEF}$ indicates passage of the 59th pulse. The occurrence of $\overline{ABDEF}$ is sensed by an output from gate 139'" which toggles flip-flop 138D. The output of gate 139'" is inverted by inverter 146' to form the $\bar{T}$ input to flip-flop 138D, and is inverted again by inverter 146'" to form the T input for this flip-flop.

The output of the seconds counter (output F from flip-flop 138F) is connected to the input of the minutes counter. The minutes counter operates in precisely the same way as the seconds counter in that both counters

operate as both binary number generators and as countdown circuits such that the minutes counter is actuated by only the trailing edge of the 59th pulse.

Likewise, as shown in FIG. 8, the hours counter utilizes a set of four toggle flip-flops 147 coupled to the flip-flop F output of the minutes counter. A further inverting circuit 148 completes the input to flip-flop 147A. The outputs of flip-flop 147A are coupled directly to the inputs of flip-flop 147B as was the case in the counter circuit shown in FIG. 7. Here, however, the counter would ordinarily count up to 16 incoming pulses. It is desired however that the counter count only 12 input pulses resetting after the 12th pulse. This corresponds to counting from zero through 11. The resetting of the binary counter is also accomplished by NAND gate circuitry in which three NAND gates and three inverter circuits are utilized. The NAND gates are labeled 149'-149''', while the inverters are labeled 152'-152'''. If the counter is connected as shown in FIG. 8, the counter 133 has an output in binary form and counts from zero to 11 at which point it resets. Like resetting conditions hold for the counter shown in FIG. 8. As pointed out hereinbefore, flip-flops 147A and 147B return to the zero state on the trailing edge of the 11th pulse. Therefore no provision is especially necessary in order to return these two flip-flops to the zero state between the 11th and 12th pulse. However, flip-flop 147C would ordinarily change from a logic "0" to a logic "1" between the 11th and 12th pulse because of a pulse from the B output of flip-flop 147B. The B output must therefore be inhibited after the 11th pulse. In counting from zero to 11, flip-flop C only toggles once. The first time it toggles (transition from 3 to 4) it is not inhibited because $\bar{D}$ is a "1" enabling gate 149'. However C would normally toggle on the transition from 11 to 12. This toggling is inhibited by the fact that $\bar{D}$ is a logic "0" at this time which inhibits gate 140'. Thus, $\bar{D}$ is used to inhibit the output B from the 147B flip-flop from reaching the input of flip-flop 147C. There is however a further problem with flip-flop 147D. As before, flip-flop D must be returned to a zero state between the 11th and 12th pulse. This is accomplished as follows. Normally the D flip-flop is driven by the $\bar{C}$ output from the 147C flip-flop. The $\bar{C}$ output is applied to one of the inputs to NAND gate 149''' whose output is inverted once at 152'' and again at 152'''. The outputs of inverters 152'' and 152''' are coupled to the $\bar{T}$ and $\bar{T}$ inputs to flip-flop 147D respectively. Normally between the 11th and 12th pulse to the counter, $\bar{C}$ would not change and therefore the flip-flop would not change its state. Flip-flop 147D at this point is in its pulse high mode. It is necessary therefore to change flip-flop 147D from its pulse high mode to a logic zero. This cannot be done from the $\bar{C}$ output of the 147C flip-flop so it must be done by some other means. This other means is provided by the A, B, and D outputs of the respective counters. If these outputs are coupled to the NAND gate 149'' and the output of the 149'' NAND gate is coupled to the other input of the 149''' NAND gate, then a negative going pulse will appear at the output of the 149''' NAND gate when A, B, and D are all high. This occurs only once during the zero through 11 counting interval. The passage of this pulse therefore toggles the 147D flip-flop from a "1" to a "0" condition when it would not ordinarily have been toggled by the $\bar{C}$ signal from the C flip-flop.

Referring now to FIG. 9, the complete multiplexer circuit 140 is shown. Since the operation of the multiplexer circuit 140 has been analyzed for the A_S , A_M , and A_H signals, it is only necessary to note that a plurality of NAND gates are provided corresponding to the seconds, minutes and hours outputs of the counters. These outputs are derived from the counters shown in FIGS. 7 and 8. As mentioned hereinbefore, the output of the NAND gate 144 indicates that the signals $A_S\phi_S$ or $A_M\phi_M$ or $A_H\phi_H$ are present as a logic "1" as opposed to a logic "0" output. Thus the output of the NAND gate 144 in effect transmits the output of the A output line of the selected counter to the driver circuit shown diagrammatically in FIG. 10.

Referring now to FIG. 10 it will be appreciated that there are 64 separate inputs to the decoder circuit 150. These inputs are derived from combinations of the 12 outputs of the multiplexer circuit. As will be appreciated, there are 16 possible pulsed outputs from the decoder circuit from the 64 inputs. In general, each one of the four inputs to the individual NAND gates shown must be logic "1" pulses before there is a logic low "0" output from the NAND gate. This logic low output removes current from the base of the corresponding PNP transistor in the driver circuit turning it on and firing a corresponding light emitting diode. These logic low outputs are labeled $f_{(0)}$ through $f_{(15)}$, respectively. The outputs $f_{(0)}$ through $f_{(15)}$ are normally high until the right combination appears at the inputs of the corresponding NAND gate. When the inputs thereto are all logic "1's" as indicated by the $A'-F'$ and $\bar{A}'-\bar{F}'$ states of the multiplexer, there appears a pulse low on the various output lines. These output pulses are fed to corresponding bases of the PNP transistors and the driver circuits shown in FIG. 11. The signals $f_{(0)}$ through $f_{(15)}$ turn on or render conductive their respective transistors such that an output L_0 through L_{15} is derived as shown in FIG. 11. The purpose of the driver is to invert the pulse low voltage from the decoder into a pulse high voltage level applied to the light emitting diode devices and to provide the necessary peak current to drive the light emitting diode elements. As can be seen from the circuit in FIG. 11, V_{CC} is directly applied through the various transistors to the light emitting diode elements. The connections to the display are as shown in FIG. 13. Thus, for instance, the signal L_0 is simultaneously coupled to the anode of diodes representing 0, 16, 32 and 48.

The complete sector selector circuit 170 is shown in FIG. 12 which activates either one of the four "quadrants" or the hour sector. Its operation is as described in connection with FIG. 3. Referring to Table I it can be seen that integers zero through 15 have associated with them E's and F's of logic zeros. Thus, $\bar{E}'$ and $\bar{F}'$ are equal to logic "1" which are applied at the inputs to NAND gate 174' to produce a pulse low. This pulse low is inverted by inverter 175' to a pulse high which turns on the NPN transistor associated with the L_1 or the first "quadrant" (sector). This indicates that a first "quadrant" number is occurring in the various counters. For integers from 16 to 31 it will be appreciated that E is a logic "1" and F is a logic "0." Thus by feeding $\bar{E}'$ and $\bar{F}'$ into NAND gate 174'', it will have logic "1's" at its inputs. With the output of gate 174'' coupled to inverter 175'', a positive pulse represents numbers from 16 to 31 and indicates enabling of "quadrant" IV. "Quadrant" IV is the next clockwise "quadrant" to

"quadrant" I. Similarly, for integers from 32 to 47 E is in its logic zero state and F is in its logic one state. Therefore, $\bar{E}$ and F applied to the NAND gate 174''' cause a pulse low condition which when applied to the inverter 175''' result in enabling of the third "quadrant" which is that next to the fourth "quadrant" going in a clockwise direction. The second "quadrant" is that next adjacent to the third "quadrant" in the clockwise direction and is enabled by E' and F'. Therefore, numbers between 48 and 59 are represented by E having a logic state of one and F having a logic state of 1. When these are NANDed and inverted the diodes in "quadrant" II are enabled. As mentioned hereinbefore, it is not necessary to go through the sector selector 170 when actuating the hours sector. However, when seconds and minutes are read out there must concomitantly be the E and F logic "1" states arriving simultaneously at the various of the NAND gates as well as ϕ_s or ϕ_m signal so that the correct counter will be read out to the transistors 161. The output of the sector selector 170 is L_I through L_{IV} plus L_H . These are connected to the diode array as shown in FIG. 13. It will be apparent, therefore, in order to light a given diode that both a sector logic "1" signal and a driver logic "0" signal must simultaneously be applied to the transistors across which the diode is located. This is accomplished in the following manner, for one example. Assuming that it is desirable to represent the time 1:12 and 39 seconds as shown by the time represented in FIG. 2, the counter states would be as follows. Seconds counter in alphabetical order of output

ABCDEF
111001

. Minutes counter,

ABCDEF
001100

. Hours counter,

ABCD
1000

The "seconds" sampling pulse is first. Therefore, at time T_1 , ϕ_s is positive, $A_s=1$, $B_s=1$, $C_s=1$, $D_s=0$, $E_s=0$ and $F_s=1$. From the multiplexing circuit, $A'_s=1$, $B'_s=1$, $C'_s=1$, $D'_s=0$, $E'_s=0$, $F'_s=1$. Going into the decoder circuit that NAND gate which corresponds to A' , B' , C' , $\bar{D}'$, corresponds to $f_{(7)}$. $f_{(7)}$ turns on the transistor associated with the output $1_{(7)}$ which then applies the voltage V_{CC} to "seconds" diodes 7, 23, 39 and 55 and hour diode 7. Concomitantly therewith, since E' is equal to zero and F' is equal to one, we have the situation $\bar{E}'$, F' in the sector selector. Since ϕ_s is now present because we are sampling the "seconds" counter, 174''' goes to a pulse low which when inverted at 175''' actuates "quadrant" L_{III} . The actuation of the transistor connected with "quadrant" L_{III} corresponds to the grounding of elements 32 through 47. However, connection between V_{CC} and ground is only made across element 39.

Turning now to the hours sampling pulse which is the next sampling pulse the output of the hours counter is 1000. Concomitantly, the output of the multiplexer is $A'=1$, $B'=0$, $C'=0$, $D'=0$. There is also no single signal corresponding to E' and F' since the hours counter does not contain these outputs. The output of the multiplexer therefore is A' , B' , C' , $\bar{D}'$. This corresponds to the NAND gate in the decoder which has an output $f_{(1)}$. $f_{(1)}$ is therefore provided to the driver circuit such that V_{CC} is connected to all of those diodes connected to the

output $1_{(1)}$. These are diodes 1, 17, 33, 49 in the seconds and minutes ring and diode 1 in the hours ring. Concomitantly, ϕ_H is supplied to transistor 165 which as shown in FIG. 12 grounds all of those diodes connected to the L_H sector output. These are diodes zero to 11 in the hours ring. Thus, the only diode in the display across which is applied V_{CC} is diode No. 1 in the hours ring.

Finally, minutes are read out by the sampling pulse ϕ_m . The output of the minutes counter is 001100. The output of the multiplexing circuit is therefore $A'=0$, $B'=0$, $C'=1$, $D'=1$, $E'=0$ and $F'=0$. The decoder NAND gate having a $\bar{A}'$, $\bar{B}'$, C' , D' input is that associated with output $f_{(12)}$. Output $f_{(12)}$ then triggers the PNP transistor having the output $L_{(12)}$. V_{CC} is therefore applied to diode elements 12, 28, and 44, in the seconds and minutes ring and to no diodes in "quadrant" II of the seconds and minutes ring and to no diodes in the hours sector. The output $\bar{E}'$, F', is the input to NAND gate 174' of the "quadrant" selector 170. This actuates the NPN transistor associated with the "quadrant" L_I . L_I is connected to diode elements zero through 15 in the seconds and minutes ring. Therefore, the only diode being connected across V_{CC} and ground is diode 12 in "quadrant" I indicating the minutes. It can therefore be seen that the sequential sampling of the counter circuit by the multiplexer has produced the light emitting diode display representing the time 1:12 and 39 seconds.

In summary, there has been described a logic and driving system for an electro-optical display of time which reduces significantly the amount of power necessary to drive the display. In so doing the subject system permits the design of a clock with a light emitting diode readout which runs for over a year on currently available batteries. The system is comprised of the combination of a sectored ring type electro-optical time display, a frequency standard, and a countdown circuit for producing an accurate 1 Hz signal operating on a reduced voltage, a level translator and pulse shaper for providing seconds, minutes and hours storage elements having binary outputs and functioning as pulse to binary encoders, a multiplexing circuit to sample the information in the storage elements over a high sampling rate low duty cycle, a binary-to-pulse decoder to decode the output of the multiplexing circuit, a driver coupled to the output of the decoder and sector selector to select the sector of the display which is to be enabled.

What is claimed is:

1. Apparatus for displaying the time of day comprising:

a time indicating display having a plurality of time indicating elements, each element having two electrodes and being actuated by the application of a potential across these electrodes, said display containing a first number of time indicating elements in a first ring representing both minutes and seconds and a second number of time indicating elements in a second ring representing hours, the elements being divided into groups, one electrode of all the elements in each group being interconnected so as to form a group terminal, the other electrodes of the elements in each group being interconnected with the other electrodes of corresponding elements in the other groups to form a position terminal;

means for generating a pulsed electrical signal;

means responsive to said pulsed electrical signal for generating a binary output representing time;
 means for decoding said binary output and for driving said display in accordance with said decoded output; and

means interposed between said means for generating said binary output and said decoding means, for multiplexing said binary output such that only portions thereof are coupled to said decoding means during any one time, said multiplexing means sampling said binary output portions sequentially over mutually exclusive and spaced time intervals, such that said display is driven only when said binary output is sampled, whereby said multiplexing means not only functions to sequentially sample portions of said binary output, but also serves to drive said display in a low duty cycle mode.

2. Apparatus as recited in claim 1 wherein said binary output contains information concerning the group as well as the position of the element to be actuated, said decoding means decoding this group and position information and causing said driving means to apply said potential across that element which is located at that position in that group that is indicated by that portion of said binary output which is sampled by said multiplexing means.

3. The apparatus as recited in claim 2 wherein said means for generating a pulsed electrical signal is powered with a lower voltage than that of the rest of the apparatus to conserve on power.

4. Apparatus for driving a time display having a number of time indicating elements actuated by the application of a potential across the electrodes thereof, comprising in combination:

means for generating a series of pulsed electrical signals, each signal having a precise frequency, and one of said signals having a frequency of 1 Hz;
 a power supply;

means operative in response to the signals generated by said pulse generating means for generating a series of seconds, minutes and hours sampling pulses in a timed sequence, said series of sampling pulses repeating over a predetermined sampling period and having sampling durations totalling only a fraction of said sampling period;

pulse-to-binary encoding means for storing in binary form information derived from said 1 Hz signal corresponding to seconds, minutes and hours, said encoding means storing said binary information such that said seconds and minutes information has associated with it bits of information indicating that minutes and seconds are divided into a predetermined number of sets each having a number of elements some of which corresponding in position to elements in other of said sets, said encoding means providing binary output signals corresponding to said seconds, minutes and hours information and to the set to which said information belongs;

multiplexing means for coupling said binary output signals to corresponding outputs thereof such that the seconds, minutes, hours and set information stored in said pulse-to-binary encoder is read out in response to the presence of a corresponding sampling pulse at said multiplexing means, said multiplexing means producing signals capable of actuating elements in said display only during the presence of a sampling pulse at the input thereto;

means for decoding the binary output of said multiplexing means so as to form an output signal in one of a predetermined number of output circuits within said decoding means;

means active in response to a signal in one output circuit of said decoding means for selectively connecting one electrode of those time indicating elements having the same position in their respective sets to one terminal of said power supply, the elements to be connected to said one terminal being selected by that binary state of said multiplexing means corresponding to that binary state of said encoding means read out by said multiplexing means during a given sampling pulse interval; and
 means responsive to that information in said encoding means read out by said multiplexing means during said given sampling pulse interval indicating the set to which the encoding means output belongs for connecting to the other of the terminals of said power supply those other electrodes of the time indicating elements corresponding to this set, whereby individual time indicating elements are sequentially actuated in accordance with said series of sampling pulses by being connected across said power supply over a low and therefore power-saving duty cycle determined by said sampling pulse duration in combination with said multiplexing means.

5. The apparatus as recited in claim 4 wherein the same time indicating elements indicate minutes and seconds.

6. The apparatus as recited in claim 4 wherein the number of time indicating elements indicating minutes and seconds exceeds the number of output circuits in said decoding means.

7. Apparatus for driving a time display having a number of time indicating elements actuated by the application of a potential across the electrodes thereof, comprising in combination;

means for generating a series of pulsed electrical signals, each signal having a precise frequency, and one of said signals having a frequency of 1 Hz;

a power supply having a pair of low voltage output terminals and a pair of high voltage output terminals, said low voltage output terminals being coupled to said pulse generating means;

means operative in response to the signals generated by said pulse generating means for level shifting said 1 Hz signal to a level compatible with the remainder of said apparatus and for generating a series of seconds, minutes and hours sampling pulses in a timed sequence, said series of sampling pulses repeating over a predetermined sampling period and having sampling durations totalling only a fraction of said sampling period;

pulse-to-binary encoding means for storing in binary form information derived from said level-shifted 1 Hz signal corresponding to second, minutes and hours, said encoding means storing said binary information such that said seconds and minutes information has associated with its bits of information indicating that minutes and seconds are divided into a predetermined number of sets each having a number of elements some of which corresponding in position to elements in other of said sets, said hour information constituting an undivided further set having a number of elements, said

encoding means providing binary output signals corresponding to said seconds, minutes and hours information and to the set to which said information belongs;

5 multiplexing means for coupling said binary output signals to corresponding outputs thereof such that the seconds, minutes, hours and set information stored in said pulse-to-binary encoder is read out in response to the presence of a corresponding sampling pulse at said multiplexing means, said multi-

10 plexing means producing signals capable of actuating elements in said display only during the presence of a sampling pulse at the input thereto;

means for decoding the binary output of said multiplexing means so as to form an output signal in one 15 of a preselected number of output circuits within said decoding means;

means active in response to a signal in one output circuit of said decoding means for selectively connecting one electrode of those time indicating elements having the same position in their respective sets to one high voltage output terminal of said power supply, the elements to be connected to said one terminal being selected by that binary state of said multiplexing means corresponding to that binary 25 state of said encoding means read out by said multiplexing means during a given sampling pulse interval; and

means responsive to that information in said encoding means read out by said multiplexing means during said given sampling pulse interval indicating the set to which the encoding means output belongs for connecting to the other of the high voltage output terminals of said power supply those time indicating elements corresponding to this set, whereby individual time indicating elements are sequentially 35 actuated in accordance with said series of sampling pulses by being connected across the high voltage terminals of said power supply over a low and therefore power-saving duty cycle determined by said sampling pulse duration in combination with said multiplexing means and whereby only low frequency elements in said apparatus are connected to said pair of high voltage output terminals.

8. The apparatus as recited in claim 7 wherein the same time indicating elements indicate minutes and seconds.

9. The apparatus as recited in claim 7 wherein the number of time indicating elements indicating minutes and seconds exceeds the number of output circuits in 50 said decoding means.

10. The apparatus as recited in claim 7 wherein said binary encoding means is a series of three cascaded counters, the first two of said counters having six toggle flip-flops and the third counter having four toggle flip-flops, the first two of said counters counting from 0 through 59 bits of input information, said first two counters being reset after the 59th bit, said third counter counting from 0 through 11 bits of input infor-

mation and being reset after said 11th bit.

11. The apparatus as recited in claim 10 wherein all switching components in said apparatus are metal oxide semiconductors.

12. The apparatus as recited in claim 11 wherein said counters utilize NAND gate logic for resetting.

13. The apparatus as recited in claim 11 wherein said means for generating sampling pulses, said counters, said multiplexing means, said decoding means, and said means responsive to set information utilize NAND gate logic in performing their various functions.

14. The apparatus as recited in claim 10 wherein said time indicating elements are arranged in two concentric rings with a first number of time indicating elements in a first ring representing both minutes and seconds and with a second number of time indicating elements in a second ring representing hours, the elements being divided into said sets, one electrode of all the elements in each set being interconnected so as to form a set terminal, the other electrodes of corresponding elements in each set being interconnected so as to form a position terminal, said multiplexing means, said means for decoding, said means for selectively connecting one electrode, and said means responsive to set information acting in combination to apply a potential across a selected element by simultaneously applying a potential to a selected set terminal and a selected position terminal so as to successively actuate each of the elements in said first ring during successive seconds, each of the elements in said first ring during successive minutes, and each of the elements in said second ring during successive hours.

15. The apparatus as recited in claim 14 wherein said elements are divided into five sets with three sets having the same number of elements and the remaining sets having a number of elements different from that of said first three sets.

16. The apparatus as recited in claim 14 wherein the sets representing the elements in said first ring correspond to quadrants which are asymmetrical due to the use of said toggle flip-flops in said counters, whereby the total number of transistors in said counters are minimized.

17. The apparatus as recited in claim 14 wherein said time indicating elements are light emitting diodes.

18. The apparatus as recited in claim 14 wherein said means for generating a series of pulsed electrical signals includes a crystal oscillator having a frequency which is some power of 2 and a series of cascaded flip-flops coupled to the output of said oscillator for counting down the output of said oscillator to 1 Hz, intermediate outputs of said cascaded series of flip-flops being used in the generation of said sampling pulses.

19. The apparatus as recited in claim 18 wherein the output of one of said cascaded flip-flops in said means for generating a series of pulsed electrical signals is applied to the input of the first of said three counters to alter the time indicated by said display.

* * * * *