United States Patent

Low et al.

[15] **3,648,250**

[45] **Mar. 7, 1972**

[54] DIGITAL VIDEO DISPLAY SYSTEM USING CATHODE-RAY TUBE

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[22] Filed: **Nov. 13, 1970**

[21] Appl. No.: **89,209**

[52] **U.S. Cl.** .....**340/172.5**, 340/324 A

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** .....340/172.5, 324 A; 315/22

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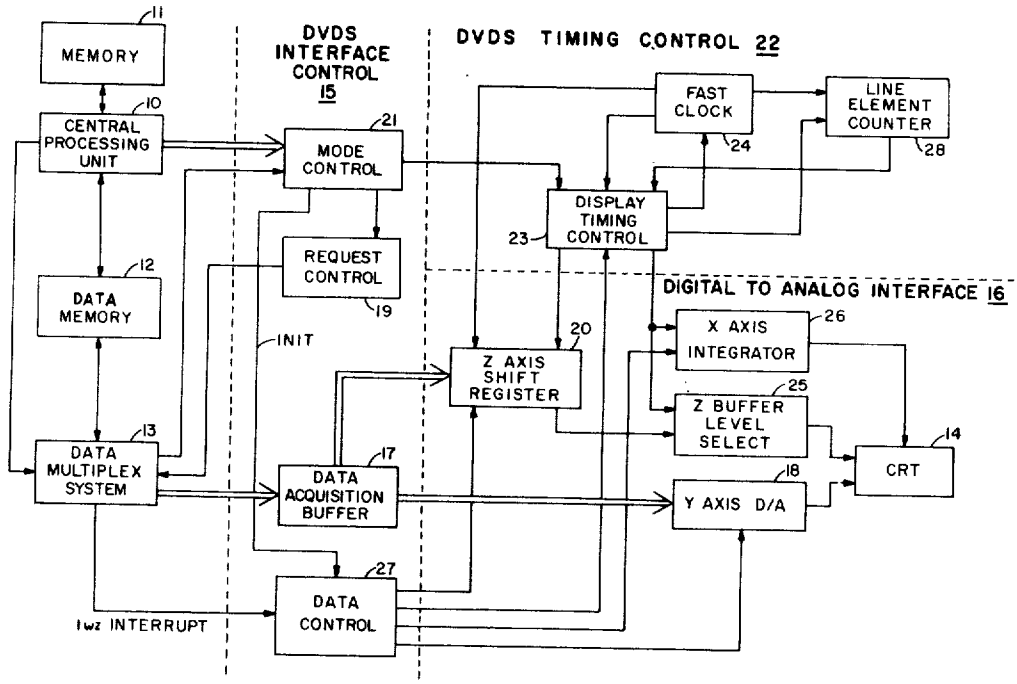
[57] **ABSTRACT**

A digital video display system (DVDS) is disclosed for display of image, alphanumeric and other data on a cathode-ray tube (CRT) with sequential raster scan and two, four or eight gray shades. The DVDS includes a central processing unit for activating the system, selecting the X (horizontal axis) and Z (intensity modulation) modes, and designating the starting location of two successive rasters of data from a memory accessed by a data multiplexer subsystem (DMS). At the end of each raster, the DMS interrupts the computer for a new starting location of a raster of data to follow the next while a DVDS control subsystem is prepared for the next raster. The first word of raster data designates the Y-axis value to be transmitted to the CRT vertical deflection system through a static digital-to-analog converter. Each word thereafter contains a predetermined number n of bits for $n/3$, $n/2$ or $n/1$ display elements (DE) in the respective eight, four and two gray shade modes. DE groups are transmitted to the CRT intensity control through a static digital level select network. As each DE group is read, an X-axis integrator is incremented by one, two or four units depending upon the X-axis mode selected. A counter determines when all DE groups of a word have been displayed in each of the gray shade modes, and resets all of the DVDS, thereby shutting off display after one, two or three DMS-memory cycles in the eight, four and two gray shade modes, respectively, until the next word is automatically read out of memory as a separate counter in the DVDS keeps track of the DMS-memory cycles for the different gray shade modes.

16 Claims, 12 Drawing Figures



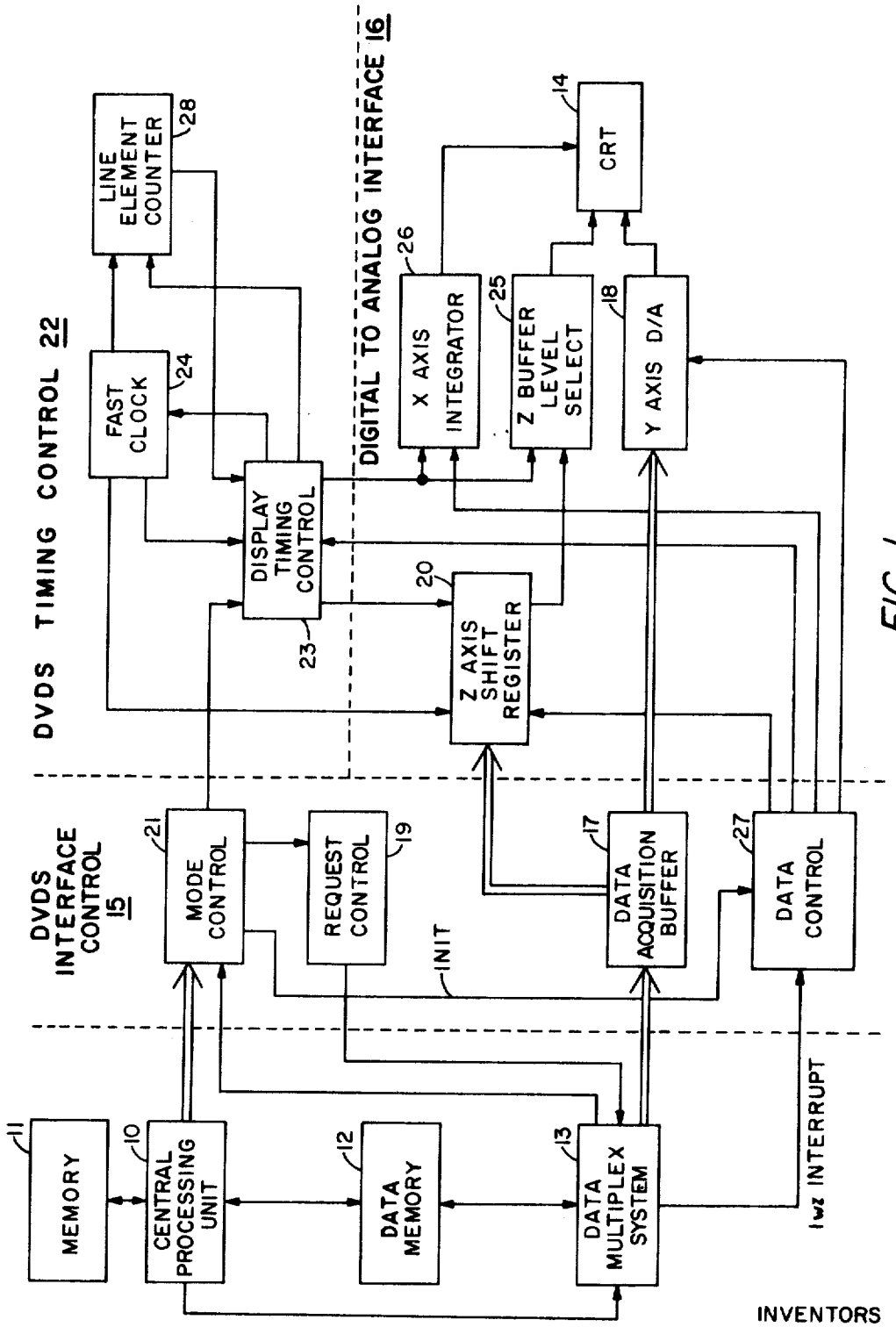


FIG. 1

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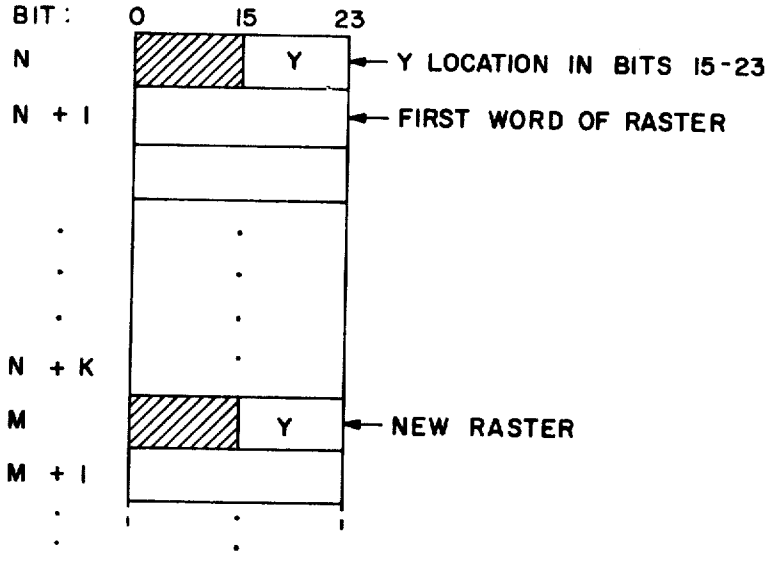

FIG. 2

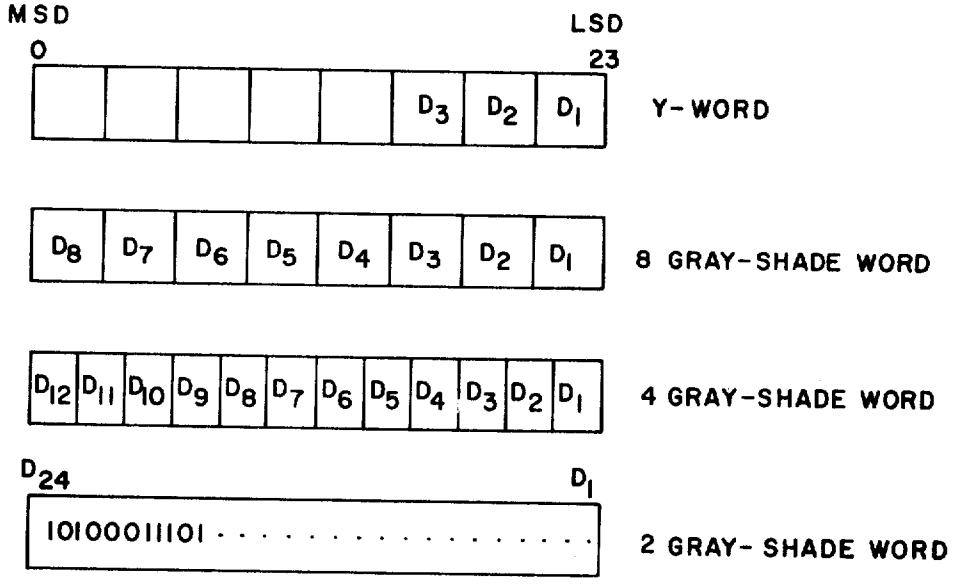

FIG. 3

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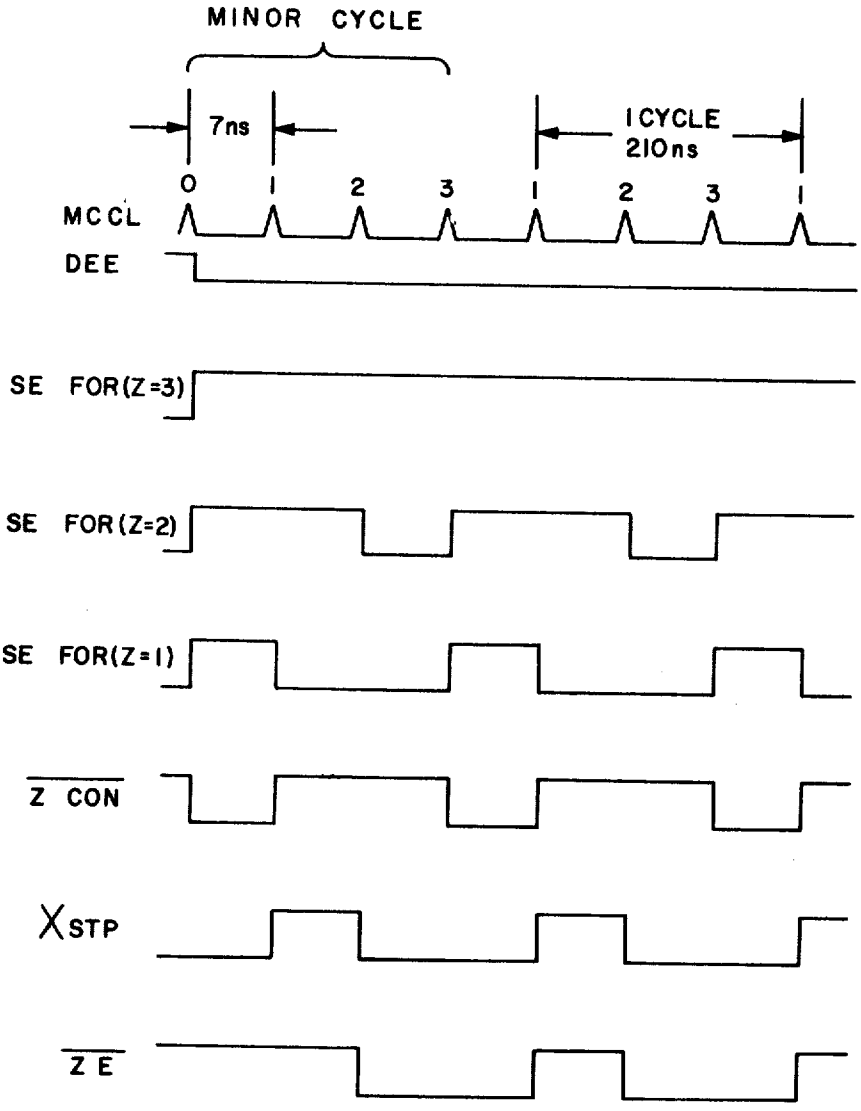

FIG. 4

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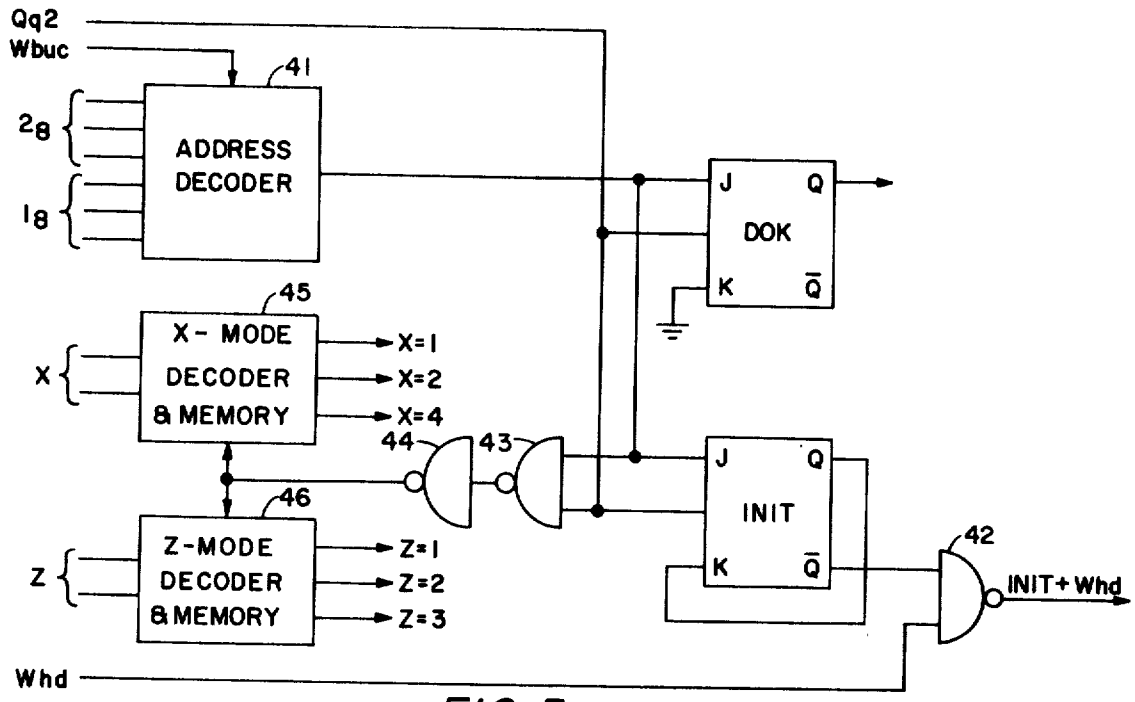
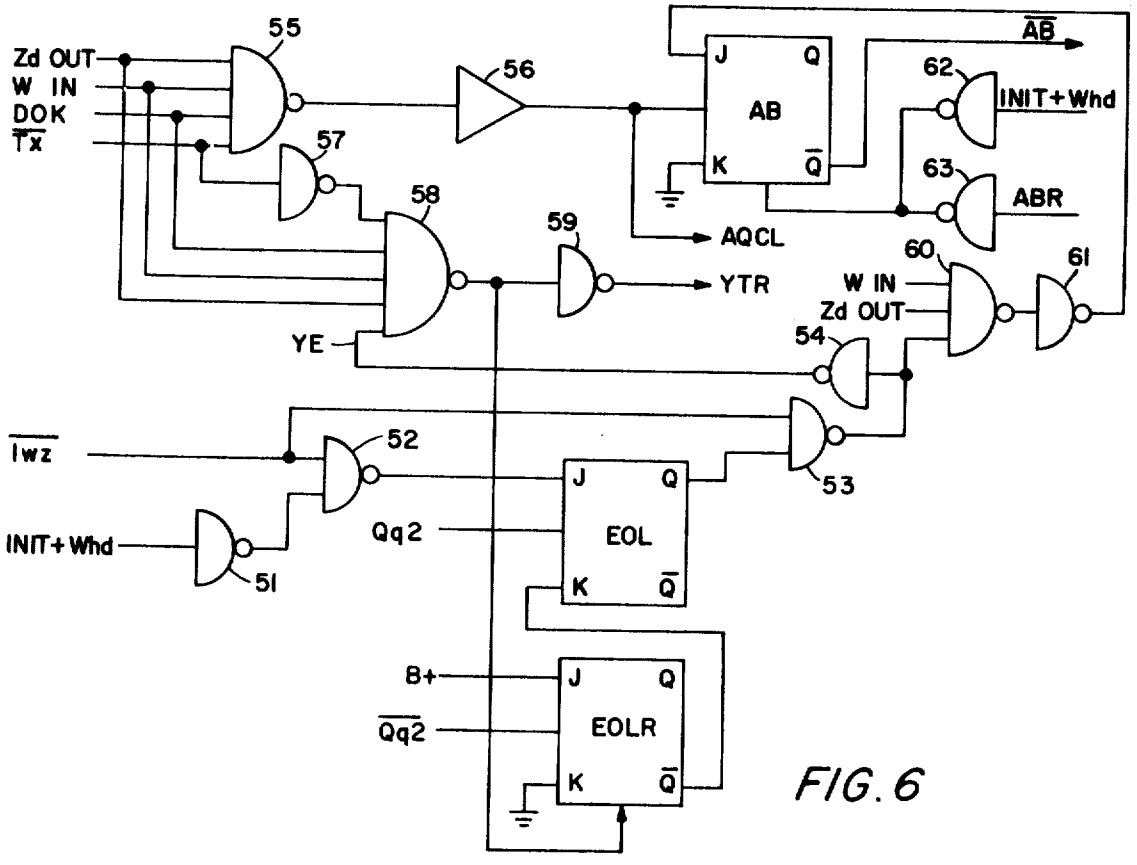

Qq2
Wbuc
41
2₈
1₈
ADDRESS DECODER
J Q
DOK
K Q̄
45
X
X- MODE DECODER & MEMORY
X=1
X=2
X=4
44
43
J Q
INIT
K Q̄
42
INIT+Whd
46
Z
Z-MODE DECODER & MEMORY
Z=1
Z=2
Z=3
Whd

FIG. 5


55
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DOK
T̄x
56
57
58
59
YE
YTR
J Q
AB
K Q̄
AQCL
AB
62
INIT+Whd
63
ABR
60
61
W IN
Zd OUT
54
53
Iwz
52
INIT+Whd
51
Qq2
J Q
EOL
K Q̄
B+
Qq2
J Q
EOLR
K Q̄

FIG. 6

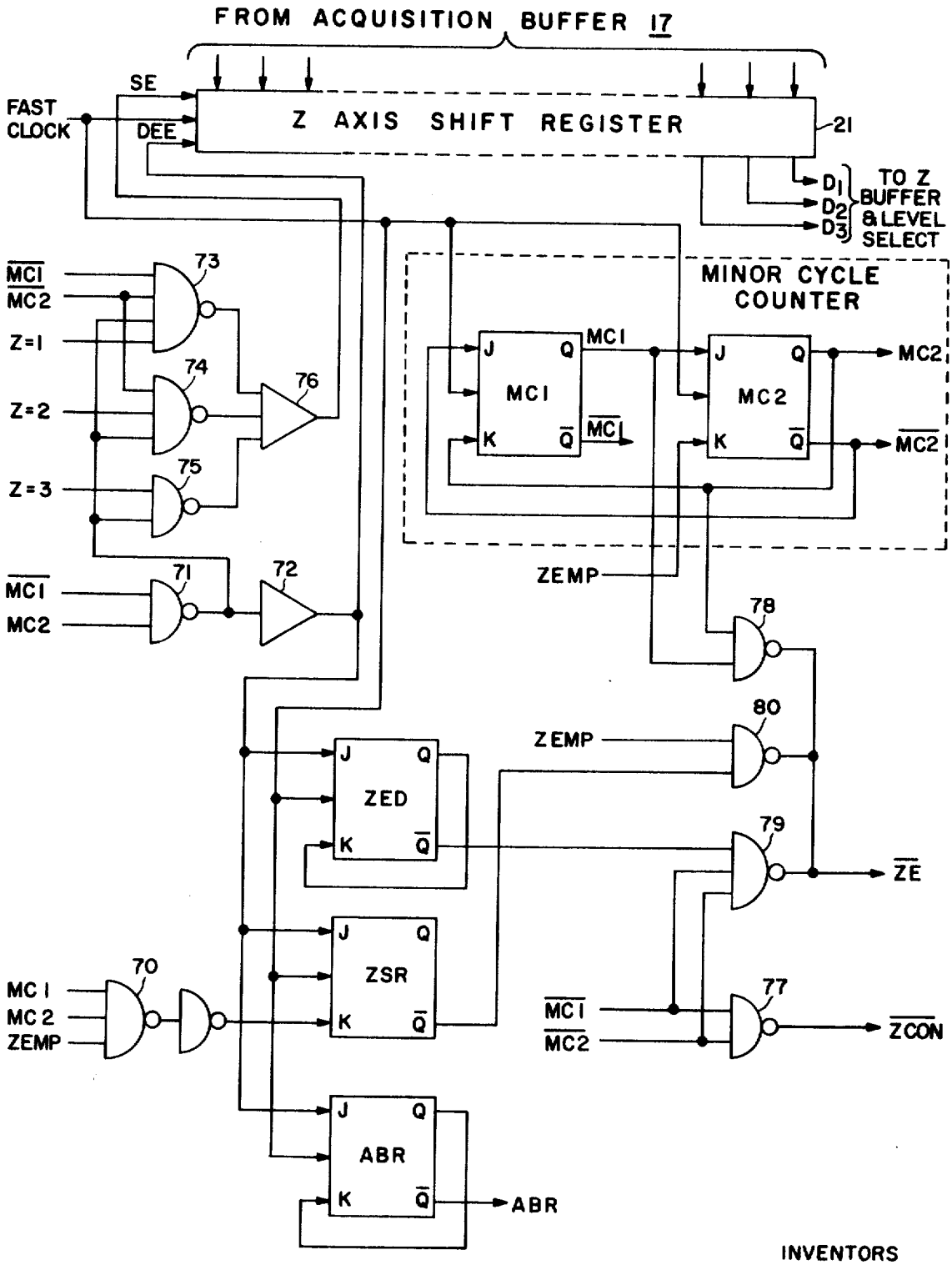

FIG. 7

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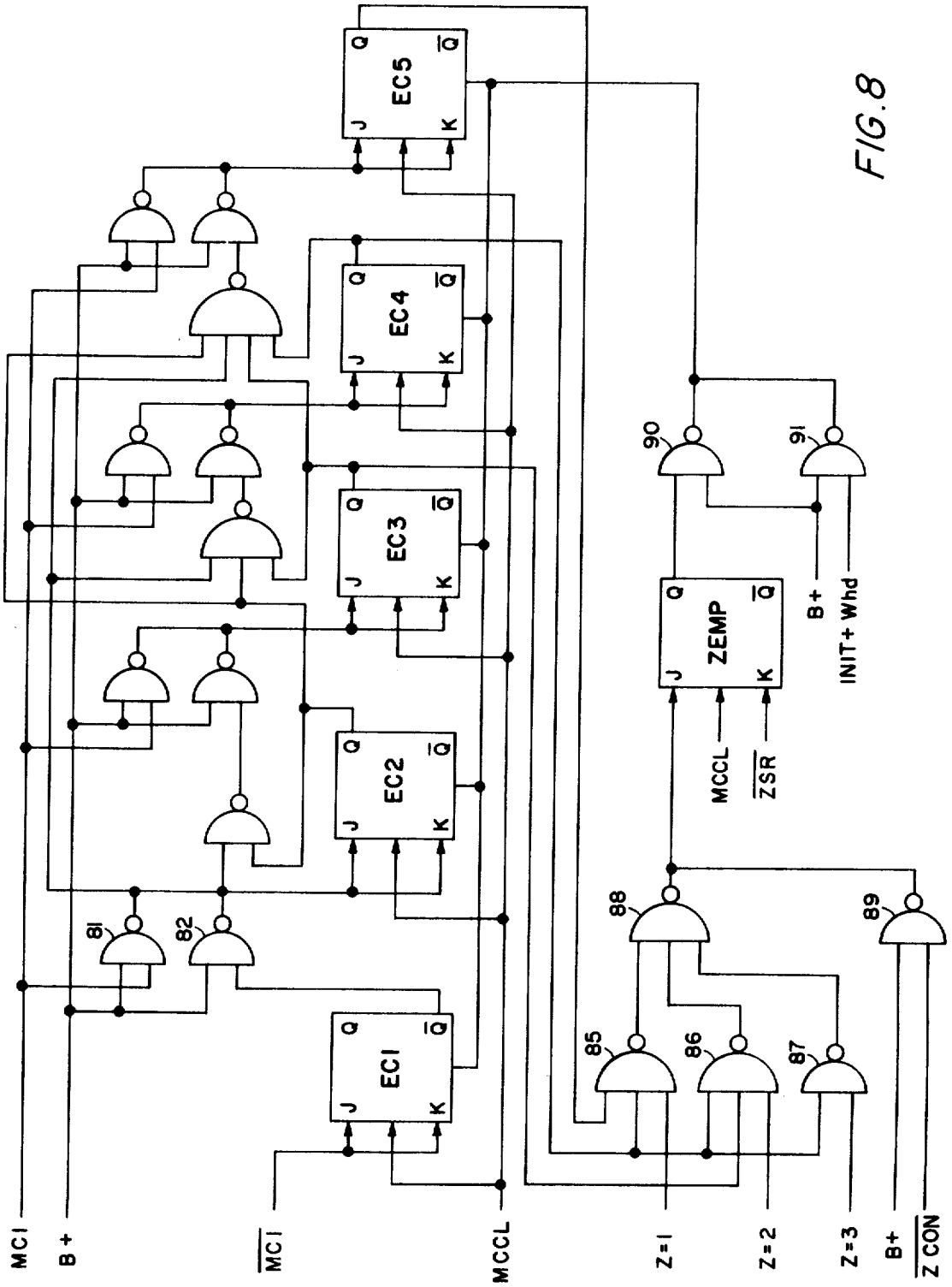
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EC1
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Z=3
B+
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MCCL
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B+
INIT+ Whd

FIG. 8

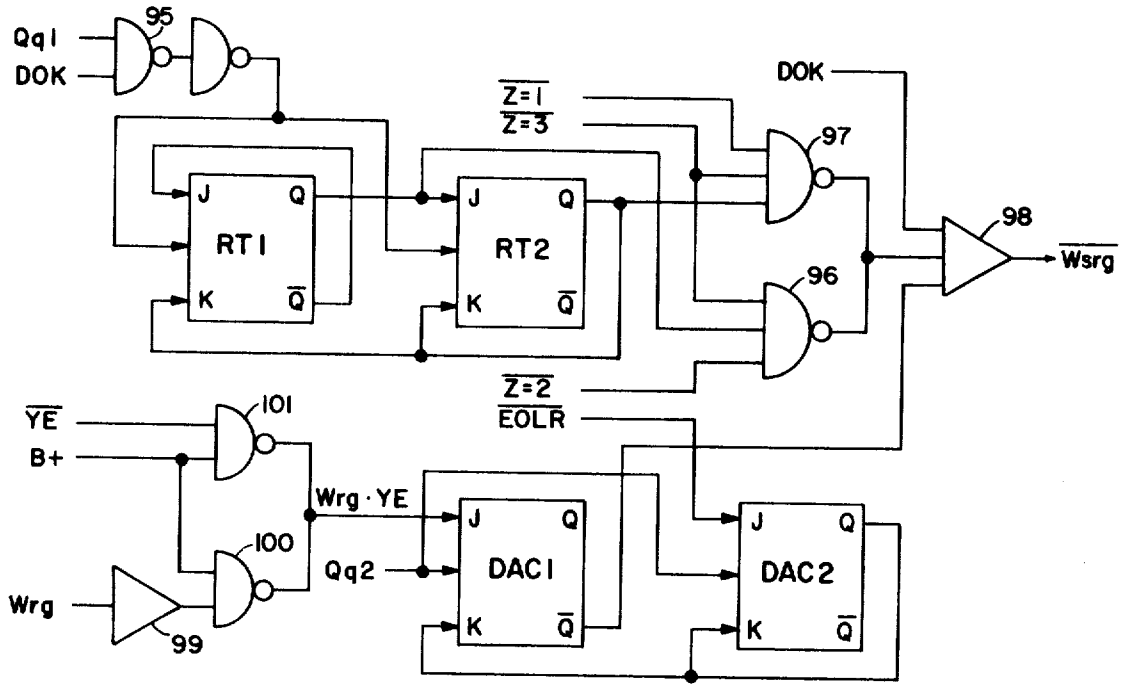

FIG. 9

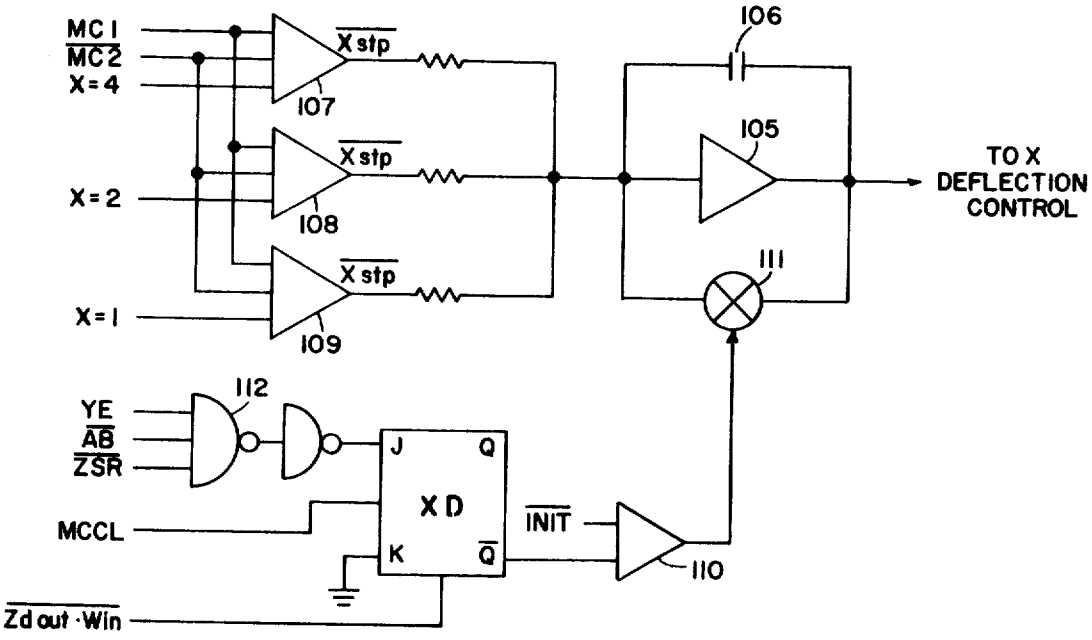

FIG. 10

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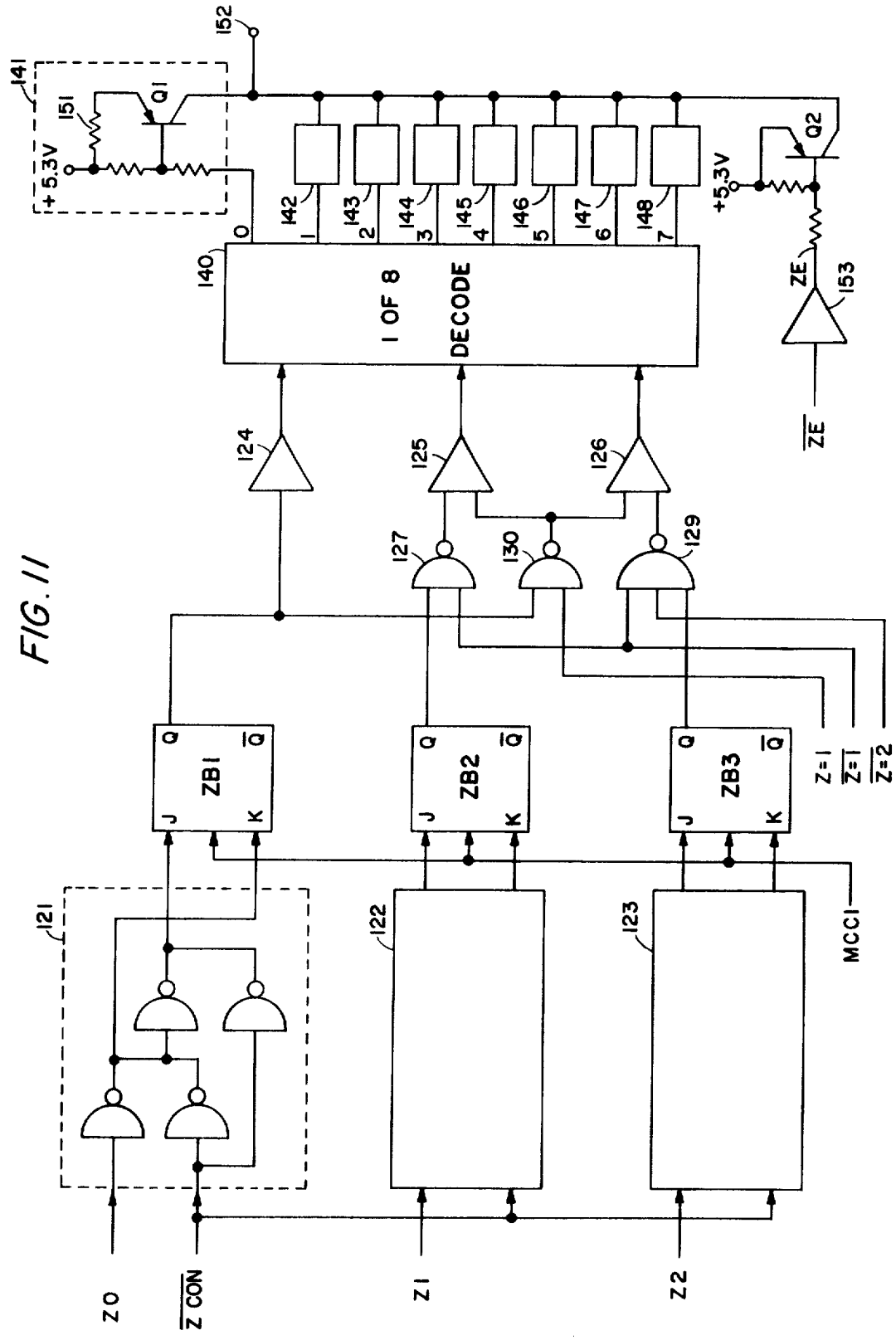
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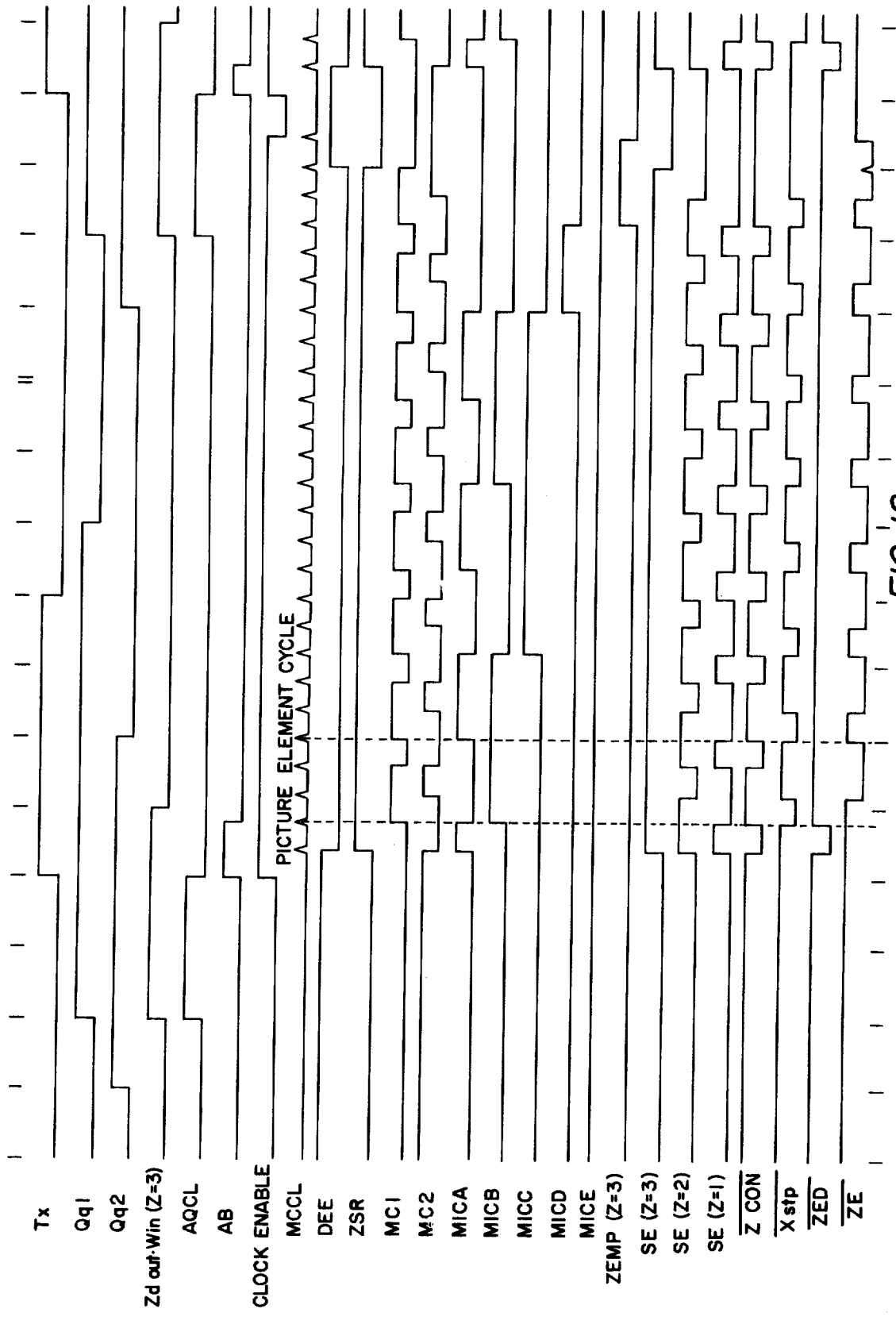
Q2
+5.3V
ZE
153
140
1 OF 8 DECODE
ZE
124
125
126
127
130
129
ZB1
ZB2
ZB3
Q
Q̄
J
K
Z=1
Z=1
Z=2
121
122
123
MCC1
Z0
Z CON
Z1
Z2

FIG. 11


Tx
Qq1
Qq2
Zd out·Win (Z=3)
AQCL
AB
CLOCK ENABLE
MCCL
PICTURE ELEMENT CYCLE
DEE
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MC2
MICA
MICB
MICC
MICD
MICE
ZEMP (Z=3)
SE (Z=3)
SE (Z=2)
SE (Z=1)
Z CON
X stp
ZED
ZE

FIG. 12

DIGITAL VIDEO DISPLAY SYSTEM USING CATHODE-RAY TUBE

ORIGIN OF INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72 Stat. 435; 42 USC 2457).

BACKGROUND OF THE INVENTION

This invention relates to a cathode-ray tube display system, and more particularly to a digital video display system.

In many applications, particularly scientific applications, it is desirable to display image data at a fast rate, sometimes in real time, with high resolution. For example, to display planetary range-doppler radar mapping data, 300 rasters of 400 display elements may be required with as many as eight gray shades, all at a rate of 40 frames per second in order to eliminate flicker. Since three binary digits are required to encode eight gray shades for the display elements, a digital display system would require a capability of processing for display 14.4 megabits of display data alone.

In the past, analog techniques have been employed to display digitally encoded data. As the data was received, or read from memory, one raster at a time, separate but synchronous analog scan generators were relied upon to position the electron beam while the display data was employed to modulate the beam intensity. Accordingly, only the Z axis was digitally controlled. Digital control of X and Y axis would provide not only greater accuracy commensurate with the greater image detail contained in the data, but also faster display. No prior art system has provided display of 4,800,000 display elements per second with a substantial number of gray shades.

OBJECTS AND SUMMARY OF THE INVENTION

A primary object of the invention is to provide a cathode-ray tube display system that is digitally controlled in all three axis of the cathode-ray tube, namely horizontal deflection, vertical deflection and intensity.

Another object of the invention is to provide a stable cathode-ray tube display system.

Still another object is to provide a cathode-ray tube display system that is flexible as to the number of gray shades employed.

Yet another object is to provide a video display system that is flexible as to resolution, i.e., flexible as to the number of picture elements to be displayed in a frame, with independent control over the number of rasters in a frame and the number of elements in a raster.

These and other objects of the invention are achieved by a digital control system for a cathode-ray tube including a central data processing unit, a memory for storing binary data and two independent communications channels from the memory to an external digital video display system which controls the cathode-ray tube, one communications channel for transfer of control words to the digital video display system under control of the central processing unit, and one for asynchronous transfer of display data to the digital video display system independent of the central processing unit once activated under control of the central processing unit.

Data elements to be displayed are stored in the memory as an array of rasters. The asynchronous data channel employs two previously assigned memory locations to store the starting location and number of words of data in blocks for the next two successive rasters, each block containing all elements of a display raster and the Y-axis locations of the raster. The words of a given raster are counted by the DMS as they are read from memory. When all have been read, the next raster is read starting at the location specified by the word in the alternate preassigned memory location, but first the central processing unit is interrupted so that it may insert the starting address and number of words for a raster to follow the next raster to be read.

Each word of a block of data except the first contains a plurality of picture elements, the number depending upon how many shades of gray are initially specified for display by the central processing unit. The first word contains only the Y location of the raster to be displayed. As each element of data is processed, an X-axis integrator is pulsed to advance the cathode-ray beam by a constant increment the magnitude of which is initially specified by the central processing unit. When an interruption occurs at the end of a raster, the integrator is reset. The cathode-ray beam is unblanked a constant period for each display element processed for display. The asynchronous portion of the DVDS counts the number of display elements processed in a word of data, and when all elements have been processed, resets that asynchronous portion. A synchronous counter keeps track of the memory cycles and automatically requests the next word each cycle, two out of three cycles or one out of three cycles for the respective eight, four and two gray shade modes without interrupting the central processing unit.

Since the end of each raster interrupts the central processing unit, and a subroutine must be executed to prepare the DMS for the raster following the next raster to be displayed, an interrupt after the last raster of the frame may be employed to deactivate the digital video display system, or to recycle to the first raster. As the rasters of a given frame are being processed for display, the central processing unit can be updating the data, such as for real time display or for otherwise altering the display as to orientation, size or intensity, in whole or in part, or to display alphanumeric or other symbols by themselves or superimposed on other display data.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention will best be understood from the following description when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the present invention.

FIG. 2 is a diagram illustrating the manner in which data to be displayed is arranged in memory.

FIG. 3 is a diagram illustrating the manner in which data words are coded for selective eight, four or two gray shades.

FIG. 4 is a timing diagram for the system of FIG. 1 for normal video element display.

FIG. 5 is a logic diagram of a mode control section of the system of FIG. 1.

FIG. 6 is a logic diagram of a data control section of the system of FIG. 1.

FIG. 7 is a logic diagram of a display timing control section of the system of FIG. 1.

FIG. 8 is a logic diagram of a line element counter of the system of FIG. 1.

FIG. 9 is a logic diagram of a request control section 19 of the system of FIG. 1.

FIG. 10 is a logic diagram of an X-axis integrator of the system of FIG. 1.

FIG. 11 is a logic diagram of a buffer level select section of the system of FIG. 1.

FIG. 12 is a minor cycle timing diagram for the display system of FIG. 1 implemented as shown in FIGS. 5 to 11.

DESCRIPTION OF PREFERRED EMBODIMENTS

The digital video display system (DVDS) of the present invention was devised to provide display of planetary range doppler data, but is also capable of providing all types of known display functions, such as X-Y plotting, alphanumeric display and image animation, all with online computation capabilities for altering the display point by point. The range doppler data which could be displayed appear as approximately 2 billion bits of binary information recorded serially on magnetic tape. These data are arranged in a $10^4 \times 10^4$ matrix, and then data reduced. Using prior art techniques, the results of changes in the data reduction took one week to become apparent as it

took one week to process a picture. The present invention will supply that picture within several seconds. For observation of experimental data and data processing, it is desirable to be able to see the plot developing such that changes in the data parameters can be made, and the effect of the changes immediately observed on the display.

The DVDS of the present invention comprises a central processing unit **10**, preferably with its own memory **11** for operating as a digital computer in response to a stored program without relying on access to a second memory **12**. Thus, while the central processing unit is communicating with the memory **11**, the DVDS is using the second memory.

The second memory can be accessed by the central processing unit **10** through a second input/output path independent of a first input/output path normally used by the central processing unit for input and output operations, as well as all data processing operations. Thus, while the first path is primarily under control of the central processing unit **10**, the second path can be under the control of either the central processing unit or a data multiplexer subsystem **13** which services a display unit comprising a cathode-ray tube **14** as required in the same manner that the data multiplexer would service any other type of device for input and output operations using the memory **12**.

While data can be transferred between the data multiplexer **13** and the memory **12** in either direction, the DVDS of the present invention employs the data multiplexer **13** only for transfer of data out of the memory **12** for display on the cathode-ray tube (CRT) **14**. By equipping the central processing unit with at least two memories, the central processing unit may carry out its normal data processing functions without interference by the DVDS except for a minimum number of cycles periodically to supervise operation of the data multiplexer. Otherwise, if only one memory were provided, and both the central processing unit and the data multiplexer were to address the one memory, the data multiplexer would have priority.

Computers are commercially available for scientific applications or industrial process control applications having a central processing unit and a data multiplexer with memory as described. One such computer which has been used for implementing the DVDS of the present invention is a model 930 manufactured by Scientific Data Systems, Inc., and described in a Reference Manual published Feb. 1966. Therefore, the description and operation of the central processing unit and data multiplexer of the preferred embodiment will correspond to an SDS 930 system having a data multiplexer with a second memory as optional equipment for transferring data out from the second memory for display. However, it should be appreciated that equivalent computers, having a central processing unit and a data multiplexer for transferring data to an external device can be employed to practice the present invention.

The format of the display data is a two-dimensional array of points. Each point is designated by position and intensity. This format lends itself not only to display by raster scan of the CRT but also to block transfer of data from the memory for deflection and intensity control of a cathode-ray beam to provide digital control of the display involving at least 300 rasters of 400 display elements per raster, each element having as many as eight shades of gray. The preferred embodiment of the present invention was designed to display a matrix or frame of up to 120,000 elements at the rate of at least 40 frames per second for a picture element rate of 4.8 MHz. With the full range of eight gray shades, the digital display must process a total of 14.4 megabits of display data per second. This is made possible by storing one, two or three bit codes for two, four or eight gray shades, respectively, on a point-by-point basis for a given raster, and preceding the display element data for each raster with the raster position in digital form.

As each block of data is read for display along the X axis, the first word of data is decoded to position the electron beam of the tube in the Y axis. That is accomplished through a DVDS interface control **15** communicating directly with the Y deflection circuit of the CRT through a digital-to-analog interface **16**. The DVDS interface control **15** includes a data acquisition buffer **17** which receives successive words in sequence from a block of memory locations for a raster to be displayed. The first word read from a given block is transferred to a Y-axis digital-to-analog (D/A) converter **18** of the digital-to-analog interface. That converter includes a static register to hold the Y-axis address of the cathode-ray beam until it is replaced by another address via the data multiplexer.

The data multiplexer receives from the central processing unit the starting address of the first block of memory locations to be read for display data, the number of words in the block of data, and the starting address of the block of data to follow together with the number of words in that block. As each word of data is transferred to the buffer **17**, the number of remaining words in the block is indicated by decrementing the starting number with the transfer of each word. When a zero word count is reached, the data multiplexer **13** transmits an interrupt signal Iwz to the central processing unit. That unit then replaces the starting address and word count of the block of data just transferred for display with a starting address and the number of words in the block of data to be displayed following the next block. Since the starting address of the next block is already in the data multiplexer, display of the next raster may thereafter be started immediately, again using the first word to position the beam of the CRT through the Y-axis D/A converter.

Since the starting address of each block of data to be displayed is specified by the central processing unit, and the first word of each block specifies the Y-axis position of the raster to be displayed, the raster may be interlaced, as in TV display systems, or arranged in any other order to meet the requirements of particular applications. However, in practice the display is most commonly successive rasters starting with the first displayed horizontally across the top of the face of the CRT.

After the first word of a block of data has been transferred to the Y-axis D/A converter, and sufficient time has been allowed for the electron beam to settle at the new Y-axis position, a request control unit **19** in the DVDS interface control signals the data multiplexer to transfer the next word of data to the data acquisition buffer **17**. From there the next word of data is transferred to a Z-axis shift register **20** to control the intensity of the electron beam for a number of successive points. For example, a 24-bit word read from the memory **12** into the data acquisition buffer **17** by the data multiplexer **13** is transferred in parallel to the Z-axis shift register for intensity control using one bit at a time starting with the most significant bit if only a two gray shade mode of operation has been specified by the central processing unit **10** to a mode control section **21**. If the mode specified is a four gray shade mode, the word in the shift register **20** is used for intensity control two bits at a time starting with the most significant two bits for a display of 12 instead of 24 successive and equally spaced points along the X axis. In an eight gray shade mode, the word in the shift register **20** is used three bits at a time, starting with the most significant three bits.

A DVDS timing control unit **22** includes a display timing control section **23** and a fast clock generator **24** operating at 15 MHz. to shift the Z-axis shift register **20** either one, two or three bit positions per minor cycle for display depending upon the gray shade mode selected. The display timing control **23** also controls the input to a Z buffer level select network **25** for operation with one, two, or three bits per minor cycle of the DVDS.

To position the electron beam for each successive point of a raster, an X-axis integrator **26** receives an increment for each display element processed so that as the Z-axis shift register is shifted one, two or three bits per minor cycle, the X-axis integrator is incremented a predetermined amount during each display minor cycle. The amount by which the X-axis integrator is incremented during each display minor cycle is con-

trolled by the mode control section **21** in accordance with the X-axis mode specified by the central processing unit at the time of activating the DVDS interface control section **15**.

The X-axis modes are three in number for increments of one, two, or four units along the X axis during each minor cycle. The Z-axis modes are also three in number. However, the X-axis mode is selected independently of the Z-axis mode. In other words, any one of the three X-axis modes may be used with anyone of the three Z-axis modes to provide maximum flexibility in the display. That coupled with the freedom of programming in the Y axis will permit optimum use of the DVDS for all display applications.

As noted hereinbefore, the data multiplexer transmits an interrupt signal Iwz when all words of a block have been processed in order to prepare the data multiplexer with the starting address and number of words in the block to follow the next block in the display, each block defining a single display raster. The interrupt signal is also transmitted to a data control section **27** to reset the digital-to-analog interface in preparation for display of the next raster. Needless to say, unblanking of the cathode-ray beam is provided only during point display periods. The beam is automatically blanked while the X-axis integrator is being stepped from one point to the next, and while the Y axis is being set to a new address. Blanking then includes flyback of the cathode-ray beam along the X axis as display progresses from raster to raster.

While the request control section **19** of the DVDS interface control automatically requests the next word of data to be displayed in synchronism with memory access cycles of the central processing unit and the data multiplexer, thus allowing a finite and predetermined time for each word to be processed for display, a display element counter **28** is provided to determine when in fact all 24, 12 or eight display elements of a 24-bit word have been processed in the respective two, four and eight gray shade modes. When the display element counter has determined that all display elements of a word have been processed, it signals the display timing control section **23** to prepare for the next word. The display timing control section **23** then turns off the fast clock generator **24**.

This arrangement may be aptly denominated a synchronous asynchronous display system. It is synchronous in that display words are transferred to the data acquisition buffer **17** in synchronism with memory access cycles. That is assured by the mode control section **21** which receives timing signals from the central processing unit via the data multiplexer to generate request control signals at the proper rate. The system is asynchronous in that the data is processed by the DVDS timing control at a clock rate independent of the central processing unit and the data multiplexer. However, that rate must be selected high enough to assure processing all display elements of a word within one, two or three memory access cycles depending upon the gray shade mode selected.

FIG. **2** illustrates schematically the organization of data for one raster of data to be displayed as stored in the memory **12**. The first word in location N contains the Y-axis position data in bit positions 15 to 23 of a 24-bit word. The Y position of any raster is thus randomly selectable. Following the first (Y) word of a block of data pertaining to one raster, the first word of picture element data is read from location N+1. Successive words of picture element data are then read from successive memory locations N+2 through N+K, where K is the number of words specified by the central processing unit for a block of data following the Y word. A new block of data is then read starting with a memory location M as specified by the central processing unit, where M is normally programmed to be equal to N+(*k*+1).

The data are read out to the DVDS in parallel and processed one, two or three bits at a time starting with the most significant digit (MSD). FIG. **3** illustrates the first word of picture element data in the three alternate forms for the block of data in FIG. **2**. The position of the raster to which the data pertains is specified by the octal number D_3, D_2, D_1 in the least significant nine-bit positions of the first word, i.e., in the three least significant octal digit positions. For an eight gray shade mode of operation, each picture element is specified by eight octal digits D_1 through D_8, each octal digit occupying three bit positions of the word. For the four gray shade mode, the word consists of twelve quaternary digits D_1 through D_{12}, each digit comprising two bits. For the two gray shade modes, each of the 24 bits comprises a binary number specifying the level (off and on) of the electron beam for each of 24 picture elements.

Picture elements are presented for equal periods regardless the gray shade mode selected. Therefore, in the eight gray shade mode, three data bits are read out every minor cycle of the display timing control section **23**. In the four gray shade mode, two data bits are read out during every minor cycle, and in the two gray shade mode, only one bit is read out during every minor cycle. In terms of cycles of the fast clock generator **24**, the bits in the X-axis shift register are shifted one out of every clock cycle for the eight gray shade mode, two out of three clock cycles for the four gray shade mode, and one out of every three clock cycles for the two gray shade mode. A picture element is then displayed for one out of every three clock periods in any one of the three modes.

FIG. **4** is a timing diagram for processing binary digits of a word of display elements in the three gray shade modes. When a word of picture element data is ready for transfer to the Z-axis shift register **20**, a transfer control signal DEE is true (positive) to allow a first clock pulse MCCL from the fast clock generator **24** to transfer in parallel the data word from the buffer **17** to the Z-axis shift register. The same clock also resets the signal DEE and sets a shift enable (SE) signal. Subsequent clock pulses are applied to the shift register in groups of three to define minor cycles of the display timing control section **23**. For the eight gray shade mode, the shift enable signal remains true until all eight display elements have been processed.

The first clock pulse of each minor cycle transfers the most significant three bits of the Z-axis shift register to the Z-buffer level select **26**. This parallel transfer of three bits to the Z buffer is controlled by a signal $\overline{\text{Z CON}}$ from the display timing control section **23**. When that signal is false, the next clock pulse transfers three bits from the most significant three bit positions of the shift register **21** to the buffer **26**. That next clock pulse also sets the signal $\overline{\text{Z CON}}$ true, thereby locking out other data for one complete minor cycle. At the same time, the display element counter **28** is incremented, and a pulse (STP) is applied to the X-axis integrator to step the position of the electron beam along the X-axis a distance of one, two or four units, where the number of units is specified in advance by the central processing unit via the mode control section **21**.

After one clock period of a minor cycle, the intensity control data in the Z buffer has been decoded and the intensity level of the electron bema selected so that during the second and third clock periods of the minor cycle the electron beam of the cathode-ray tube is unblanked by setting a signal $\overline{\text{ZE}}$ false. By the time of the first clock period of the next minor cycle, three new bits will have been shifted into the least significant three bit positions of the Z-axis shift register. Those three new bits are then transferred to the Z buffer, and the sequence just described for the one display element is repeated for the next display element.

In the case of a four gray shade mode of operation, the shift enable signal (SE) is reset for one clock period so that during each minor cycle, only the first and second clock pulses will shift the contents of the Z-axis shift register **21**. In response to the first clock pulse of a given minor cycle, two binary digits are transferred to the Z buffer. For the two gray shade mode, the signal SE is controlled to be true only during the first clock pulse of a minor cycle. One bit of data is shifted to the Z-buffer-level select to set full bright or full off.

In order that the signal SE be true for the first clock pulse of the first minor cycle following a parallel transfer of a data word into the Z-axis shift register, the signal SE is set true in

response to the clock pulse which transfers the data word into the Ztaxis shift register. As noted hereinbefore, the fast clock MCCL is turned on by the display timing control section **23**. The arrangement is for the clock generator to be turned on for one clock period before the processing of data elements is started. That is readily accomplished by employing a modulo-3 counter which has an anomalous fourth state that can be used for the initial clock period preceding the first minor cycle of three clock pulses. The clock pulses MCCL counted by the modulo-3 counter, and the state of that counter are decoded for control of the timing signals described with reference to FIG. **4**.

After a word of display element data has been processed, the modulo-3 counter is set to the anomalous fourth state. This fourth state is decoded to generate the signal DEE for parallel transfer of the data word from the data acquisition buffer into the Z-shift register. Thus, once the fast clock is turned on, the modulo-3 counter in the display timing control section **23** is turned on, and immediately the modulo-3 counter therein allows a word to be transferred from the data acquisition buffer to the Z-shift register in response to the first clock pulse from the fast clock generator **24**. The very next clock pulse initiates the modulo-3 counting sequence to divide the minor cycle into periods of three clock pulses.

After all eight, 12 or 24 display elements of a word have been processed, the modulo-3 counter is reset to its anomalous fourth state in preparation for the next line. Setting the modulo-3 counter in the anomalous fourth state is initially accomplished when the DVDS is activated by the central processing unit by a signal INIT generated for one clock period of 1.75 microseconds timed by clock pulses Qq1 from the central processor.

The data control section **27** is placed in an initial state by the signal INIT for gating of the first word of a block from the memory **12** to the Y-axis digital-to-analog converter **18**. The first word coming from the memory via the data multiplexer **13** is thus put in the data acquisition buffer and then transferred into the Y-axis D/A converter, which includes its own buffer register. The display timing control section **23** inhibits the request control section **19** from making any request for further data words for two memory access cycles (3.5 microseconds) to allow the Y-axis D/A converter to settle before requesting the first word of display element data.

The actual requests for display element data are made automatically by the request control section **19** once the DVDS has been activated and the display timing control section has completed the request control delay. That is accomplished by a second modulo-3 counter which counts memory access cycles. The output of the counter is decoded to allow a new word of display element data to be requested during each memory cycle when operating in the eight gray shade mode, two out of three memory access cycles when operating in the four gray shade mode, and only one out of every three memory access cycles when operating in the two gray shade mode, thus allowing more than the one memory access cycle period for the processing of display element data for the two gray and the four gray shade modes. For the eight gray shade mode, a new word of display element data is requested during each memory access cycle since the binary digits of each word are being used at the maximum rate of three bits per minor cycle of the DVDS. The frequency of the fast clock **25** is selected to be sufficiently high to process one word of display element data and request another word during one memory access cycle in the eight gray shade mode.

The modulo-3 counters employed in the display timing control section and the request control section will be described more fully hereinafter with reference to a logic diagram of the preferred embodiment of the invention. For the present, it is sufficient to understand that the modulo-3 counter in the display timing control section is initially set to its anomalous fourth state in preparation for the first word of display element data, and thereafter set in its anomalous fourth state at the end of each raster or line block of data displayed when the display element counter signals the display timing control **23** that all display elements of a word have been processed. The modulo-3 counter in the request control section is not at any time set in its anomalous fourth state. Thus, as noted hereinbefore, the DVDS is a synchronous asynchronous system in that actual processing of display element data is asynchronous while the request for data words is synchronous with the central processing unit. However, it should be understood that the request for data could also be made asynchronously. A synchronous request is preferred only because the memory **12** is synchronous with the central processing unit. Otherwise the data multiplexer would have to wait and act upon each request for data in synchronism with the next memory access cycle. The request control section of the DVDS interface is made synchronous with the memory access cycles through clock pulses Qq1 from the central processing unit.

The manner in which the central processing unit **10** activates the data multiplexer **13** and the DVDS through the mode control section **21** will now be described with reference to the logic diagram of the mode control section shown in FIG. **5**. But first it is again pointed out that the central processing unit **10** has at least two well defined input/output channels. One channel is through the data multiplexer **13** capable of servicing several data subchannels one of which is here used by the DVDS only for data output. The other input/output channel is for parallel transfer of 24-bit words at slow transfer rates to and from external devices, here used by mode control section of the DVDS interface to receive initiating signal and mode data.

Both input/output channels are controlled directly by the central processing unit. In the case of the data multiplexer, the central processing unit must supply starting location and word count for block transfer of data, after which data is transferred to or from memory upon request of the external device designated to transmit or receive the data. Thus, while the data multiplexer can also be employed to transfer data from the external device to the memory **12**, the DVDS only receives data in memory. Activating the data multiplexer then takes only one form for the DVDS. The mode control section **21** receives predetermined bits of a 24-bit word in parallel to not only activate the DVDS by setting a flip-flop DOK and a flip-flop INIT, but also to decode and store the X (step) and the Z (gray shade) modes of operation for the DVDS.

The data multiplexer has an activation sequence consisting of two control instruction sequences. The first sequence designates the data multiplexer as the channel to have access to the memory **12** and to interrupt the central processing unit. The second sequence activates communication with the DVDS through the multiplexer **13**. In the case of implementation with an SDS 930 computer having a data multiplexing system as optional equipment, the first sequence of instructions consist of an EOM instruction followed by a POT instruction. The EOM (energize output medium) instruction merely designates a data subchannel to communicate with the memory **12** through the data multiplexer **13**. The data subchannel in this case serves the DVDS.

The following POT (parallel output) instruction designates to the data multiplexer that it is to respond to a zero word count interrupt signal Iwz. This first POT instruction also designates to the data multiplexer to start with a word location and count stored in a designated one of adjacent even and odd locations of the memory **12** permanently preassigned to the DVDS, i.e., to the data subchannel addressed by the preceding EOM instruction. It also instructs the data multiplexer to thereafter cycle between the preassigned odd and even memory locations so that having used the starting location and word count from one location, the data multiplexer can continue with its data transfer operation by switching over to the starting address and word count of the other location. But first an interrupt subroutine updates the starting location and word count in the preassigned location which has just been used to provide a starting address and a word count for a subsequent block of data following the next block of data.

The second EOM-POT sequence of instructions is to prepare the DVDS addressed by the first EOM instruction to be activated by allowing transfer to the mode control section of FIG. 5 an enabling signal Wbuc during the succeeding POT instruction. The POT instruction which then follows transmits an octal code 21 to an address decoder 41 enabled by the signal Wbuc to transmit a binary-1 signal to J input terminals of flip-flops DOK and INIT.

A clock pulse Qq2 from the central processing unit sets the flip-flops DOK and INIT, thus allowing the DVDS to become active. The next clock pulse Qq2 resets the flip-flop INIT because its true output terminal is connected to its K input terminal. Thus the flip-flop INIT is turned on for only one clock period of central processing unit. The true output of the flip-flop INIT is transmitted through a NAND-gate 42 to reset all counters and controllers except the flip-flop DOK. It should be noted that all flip-flops of the system are set, or reset, on the trailing (negative going) edge of clock pulses.

The flip-flop DOK remains set until the program turns off the display, at which time a third EOM-POT sequence of instructions is executed by the central processing unit. The EOM instruction addresses the data subchannel of the data multiplexer devoted to the DVDS function, and the POT instruction initiates through the mode control section of FIG. 5 the transmission of a Whd signal to reset the flip-flop DOK and, through the NAND-gate 42, reset all counters and controllers of the system.

The output of the address decoder 41 which operates on designated bit positions of a POT instruction is also transmitted to a NAND-gate 43 which transmits the clock pulse Qq2 via an inverter 44 to an X-mode decoder 45 and a Z-mode decoder 46. The Z and X modes are designated by predetermined octal digits of the POT instruction. Since only three modes are provided for both the X and Z axes, only two binary digits are needed for each of the X and Z octal digits. For the X axis, the octal digits 1, 2 and 3 designate X-step increments of four, two and one units, respectively while the octal digits 1, 2 and 3 for the Z-axis designate two, four and eight gray shade modes, respectively. Each of the decoders 45 and 46 includes as an integral part thereof means for storing the decoded values of X and Z in order to transmit bianry-1 signals from X and Z output terminals corresponding to the values of the X and Z octal digits as shown in FIG. 5.

While all counters and controllers are reset by a signal Whd as just described, the X and Z mode decoders are not because for the system to be used again subsequently, another EOM instruction must be executed to generate a signal Wbuc, and that must be followed by another POT instruction having the address octal code 21 and the Z and X octal codes to be used at that time. When the NAND-gate 43 again transmits a clock pulse Qq2 to the X and Z decoders, they will be set to the proper states.

Referring now to FIG. 6, the data control section shown in logic diagram form is set to an initial state for the first raster display operation by the output of the flip-flop INIT via the NAND-gate 42 (both in FIG. 5), an inverter 51 and a NAND-gate 52 connected to the J input terminal of a flip-flop EOL. The clock Qq2 times the setting of the flip-flop EOL with the resetting of the flip-flop INIT.

The output of the flip-flop EOL generates the Y-enable signal (YE) referred to hereinbefore via NAND-gates 53 and 54. The NAND-gate 53 transmits a complementary signal $\overline{YE}$, and the NAND-gate 54 transmits the signal YE only when an interrupt signal Iwz is not present at the input of the NAND-gate 53. An interrupt signal Iwz present from the data multiplexer 13 (FIG. 1) will allow the flip-flop EOL to be set by the next clock pulse Qq2, but a Y-enable signal and its complement are not transmitted by the respective NAND-gates 54 and 53 until the multiplexer has ceased transmitting the interrupt signal Iwz.

As noted hereinbefore, when the DVDS is activated, two control words are transferred to the data multiplexer from preassigned odd and even memory locations. The interrupt routine replaces the control word just used with a new control word for a block of data to follow the next block. For example, if the odd control word has been used to read out a block of k+1 words starting at a memory location N, and the next k+1 words are to be read out of a block starting at memory location M as specified by the even control word, where M is equal to N+(k+1), the interrupt routine replaces the odd control word already used with a new control word specifying the starting address and word count for the block of data following the word from location M+k. In the SDS 930 system, the starting location is entered as M−1 in the control word because the multiplexer increments the address by one before each word of the block is read, not after it is read.

Once the Iwz interrupt routine has been completed, the data multiplexer 13 will prepare to transfer the first word of the next block of data to the data acquisition buffer 17 (FIG. 1). When the word is ready for transfer to the data acquisition buffer, the data multiplexer transmits two signals both of which must be present. The first signal is Win and the second signal is ZdOUT. These signals, shown in FIG. 12 with others already referred to and others to be referred to hereinafter, are applied to a NAND-gate 55 which also receives a clock pulse Tx from the central processing unit via the data multiplexer and true output of the flip-flop DOK. The output of the NAND-gate 55 is inverted by a power amplifier 56 to transmit a signal AQCL to the clock terminals of the data acquisition buffer. That causes the word read from the memory by the data multiplexer to be entered in the acquisition buffer upon the occurrence of the clock pulse Tx. At the same time the output of an inverter 57 becomes true to enable a NAND-gate 58 to transmit a signal YTR via an inverter 59 to cause the Y-axis value of the next raster to be transferred from bit position 15 to 23 of the acquisition buffer to the Y-axis D/A converter 18 (FIG. 1). That converter has its own input buffer register. There the Y value is converted from digital-to-analog form and applied to the Y-deflection circuits of the CRT.

After two memory cycles the position of the electron beam in the Y axis will be stable. The first word of data to be displayed is then read from memory. The display timing control 23 is employed to cause the request control section 19 to delay requesting another word of data following the first (Y) word for the two memory cycles required for the Y-deflection circuit to settle. Accordingly, each time the first word is transferred from the memory by the data multiplexer following activation of the DVDS and following each Iwz interrupt, the display timing control section delays any further request for words from the request control section for two memory cycles.

It should be noted that clock pulses from the fast clock generator 24 (FIG. 1) are not required for the first (Y) word. The clock pulse Tx from the central processing unit times the transfer of the Y value to the Y-buffer register. Accordingly, the fast clock generator 24 is not turned on for the first word of each block of data.

The signal AQCL which clocks the first (Y) word and the subsequent data words into the acquisition buffer is also applied to the clock input terminal of a flip-flop AB to set it and thereby indicate that a data word is waiting in the acquisition buffer, except for the first (Y) word because its J input terminal receives a binary 0 signal from NAND-gates 60 and 61 while a Y-enable signal $\overline{YE}$ is present at the output of the NAND-gate 54, i.e., while the complement YE is present at the output of a NAND-gate 53.

Upon transferring the first (Y) word to the Y-axis D/A converter in response to the signal YTR from the NAND-gate 59, the complement YTR at the input to the NAND-gate 59 resets the flip-flop EOLR. That flip-flop is continually being set by the clock pulse $\overline{Qq2}$. The false output terminal of the flip-flop EOLR is connected to the K-input terminal of the flip-flop EOL to enable it to be set upon initial activation of the DVDS or upon the occurrence of an interrupt signal Iwz to generate the Y-enable signal. Then when the first (Y) word has been

transferred to the Y-axis digital-to-analog converter (in response to a clock pulse Tx applied to the NAND-gate **58**), the flip-flop EOLR is reset to allow the next clock pulse Qq2 to reset the flip-flop EOL, thereby terminating the Y-enable signal YE as indicated by the timing diagram of FIG. **13**.

The flip-flop AB is initially reset by the output of the flip-flop INIT or a signal Whd (produced by the central processing unit in response to a POT instruction to deactivate the DVDS). Both signals are transmitted from the NAND-gate **42** (FIG. **5**) to the reset terminal of the flip-flop AB by a NAND-gate (inverter) **62**.

After the initial Y word has been read, and the flip-flop AB has been set to indicate a data word is ready in the acquisition buffer, the false output terminal of the flip-flop AB transmits a signal ($\overline{AB}$) to the fast clock generator **24** (FIG. **1**) to turn that clock generator on for one pulse. This first of a series fast clock pulses MCCL transfers the content of the data acquisition buffer to the Z-axis shift register **20** (FIG. **1**) in parallel. It also sets a flip-flop ZSR in the display timing control section **24** shown in FIG. **7**. That flip-flop then keeps the fast clock generator on until the display element counter **28** (FIG. **1**) indicates that all display elements of the word in the Z-axis shift register have been processed. The first of the series of clock pulses also sets a flip-flop ABR to transmit a signal ABR through a NAND-gate **63** (FIG. **6**) to reset the flip-flop AB. Thus, while a word is being transferred from acquisition buffer to the Z-shift register, the flip-flop AB is being reset.

The display timing control section shown in FIG. **7** sequences the actual processing of display element data. The heart of the timing control section is a specially constructed modulo-3 counter having an anomalous fourth state from which it enters the normal modulo-3 counting sequence. This counter comprises two JK flip-flops MC1 and MC2 the true output of which are shown in FIG. **12**. When the DVDS is activated by setting the flip-flop INIT, the output of the NAND-gate **42** (FIG. **5**) sets the modulo-3 counter into is anomalous state by resetting the flip-flops MC1 and MC2. The X-axis integrator (FIG. **1**) is also reset at that time as will be described more fully hereinafter.

After the first word and each subsequent word of a raster has been displayed, a flip-flop ZEMP (FIG. **8**) is set at the end of each word display cycle. The false output signal $\overline{ZEMP}$ (complement of the signal ZEMP shown in FIG. **12**) is then employed to set the modulo-3 counter to its fourth state in response to an extra clock pulse produced to shut the fast clock generator off. The fourth state of the modulo-3 counter is decoded to enable a parallel transfer of these subsequent words of a raster from the data acquisition buffer into the Z-axis shift register. Once a subsequent data word has been transferred into the Z-axis shift register in response to the first fast clock pulse which sets the flip-flop ABR, the modulo-3 counter proceeds to count the fast clock pulses MCCL to define the minor cycles during which the Z-axis register can be shifted one, two or three steps per minor cycle for the respective two, four and eight gray shade modes. When all of the binary digits have thus been shifted out of the Z-axis shift register, the display element counter sets the flip-flop ZEMP as just noted to signify that the Z-axis shift register is empty.

The true output of that flip-flop ZEMP is employed (via a NAND-gate **70** connected to decode the third count of binary 11 in the modulo-3 minor cycle counter) to reset the flip-flop ZSR at the same time that the modulo-3 counter is being set to its fourth state as shown in the timing diagram of FIG. **12**. The signal ZEMP is also employed to enable the fast clock generator to stay on for one extra pulse to shut itself off. That is also shown in FIG. **12**. In this manner, the minor cycle counter is in its fourth state for the operation of transferring a word from the acquisition buffer to the Z-axis shift register when the flip-flop AB (FIG. **6**) is again set. That fourth state is decoded by a NAND-gate **71** which transmits through a power amplifier **72** a transfer control signal DEE to the parallel input control terminals of the Z-axis shift register and to the J-input terminal of the flip-flop ABR to enable it to be set for one fast clock period for the purpose of resetting the flip-flop AB.

Once a data word has been transferred into the Z-axis shift register, NAND-gates **73**, **74** and **75** decode the three states of the minor cycle counter to control one, two or three shifts of the Z-axis shift register during each minor cycle. For an eight gray shade mode, the Z-mode decoder **46** (FIG. **5**) transmits a signal Z=3 to enable the NAND-gate **75** to transmit a shift enable (SE) signal through a power amplifier **76** at all times except when the fourth state of the minor cycle counter is detected by the NAND-gate **71**. For a four gray shade mode, the Z-mode detector transmits a signal (Z=2) to enable the NAND-gate **74** to transmit a shift enable signal through the amplifier **76** at all times when $\overline{MC2}$ is true except when the gate **71** detects a fourth state. SE is true, then, during two out of every three clock periods of each minor cycle. Similarly, for a two gray shade mode, the Z-mode detector transmits a signal (Z=1) which enables the NAND-gate **73** to transmit a shift enable signal SE through the amplifier **76** at all times when either $\overline{MC1}$ or $\overline{MC2}$ is true except when the gate **71** detects a fourth state. SE is true, then only one out of every three clock periods of each minor cycle. All three modes are illustrated in the timing diagram of FIG. **12** by showing in parenthesis the enabling signals Z=1, Z=2 and Z=3 for the signal SE.

As noted hereinbefore with reference to the timing diagram of FIG. **4**, a signal $\overline{Z\ CON}$ enables the transfer of the three most significant (right most) bits of the Z-shift register to the Z buffer and level select section **26** (FIG. **1**). That signal, also shown in the timing diagram of FIG. **12**, is generated by a NAND-gate **77** which decodes the first clock period of each minor cycle by detecting when both of the flip-flops MC1 and MC2 are reset at the same time. The level select portion of the section **26** employs one, two or three bits thus entered into the Z buffer to set the intensity level of the electron beam in the CRT. During the next clock period following the $\overline{Z\ CON}$ period, when the flip-flop MC1 is in the one state and MC2 is in the zero state, the X-axis integrator receives an $\overline{X\ stp}$ signal at one of three terminals and is thus stepped one, two or four units under control of an output signal of the X-mode decoder. For that purpose, the MC1 and $\overline{MC2}$ output terminals of the respective flip-flops MC1 and MC2 are connected to the X-axis integrator. The $\overline{X\ stp}$ signal shown in FIG. **12** is applied to one of the three terminals of the X-axis integrator as shown in FIG. **10**.

At the end of the $\overline{X\ stp}$ period of each minor cycle, the electron beam of the cathode-ray tube is unblanked by a signal $\overline{ZE}$ shown in FIG. **12**. NAND-gates **78**, **79** and **80** generate the unblanking signal $\overline{ZE}$ for **140** ns of each minor cycle during the third and first states of the minor cycle counter, which is when both flip-flops MC1 and MC2 are either true as detected by the NAND-gate **78** or false as detected by the NAND-gate **79**. It should be noted that there is an initial first state (00) in the minor cycle counter immediately after a parallel transfer of a data word to the Z-axis shift register as shown in FIG. **12**. Since binary digits are not transferred to the Z-buffer level select section **26** (FIG. **1**) in response to a signal $\overline{Z\ CON}$ from the NAND-gate **77** until the end of the period of the first state, the unblanking signal $\overline{ZE}$ must be inhibited during that initial first clock period after a word has been transferred into the Z-axis shift register. That is accomplished by the false output terminal of a flip-flop ZED connected to the NAND-gate **79**. The flip-flop ZED is set by the first clock pulse applied to the Z-axis shift register to transfer a word from the acquisition buffer into the Z-axis shift register as shown in the timing diagram of FIG. **12**. Accordingly, the J-input terminal is connected to receive the transfer control signal from the output of the amplifier **72**. Immediately thereafter, the flip-flop ZED is reset since its K-input terminal is connected to its true output terminal, and the signal at the J-input terminal is zero after the first clock pulse.

The display element counter **28** (FIG. **1**) keeps track of the number of Z conversions made. For a 24-bit word of display elements, there may be eight, 12 or 24 conversions according to whether the mode selected by the octal digit applied to the Z-mode decoder **46** (FIG. **5**) is for an eight gray shade mode, a four gray shade mode or a two gray shade mode. Accordingly,

although the display of each element requires the same amount of time (three periods of the fast clock generator regardless of the Z mode selected), a word of data is processed in a period of time which depends upon the Z mode selected. The Z mode selected is stored in the Z-mode decoder **26** throughout the period of time the DVDS is activates so that it is feasible to count the pulses from the fast clock generator to determine when all display elements of a word have been processed, the number being predetermined and different for each mode. However, since there is only one Z conversion for each display element, it is preferred to effectively count the conversions in a five-bit synchronous counter shown in FIG. **8**.

Referring now to FIG. **8**, the five-bit synchronous display element counter comprises five JK flip-flops EC1 through EC5. The flip-flop EC1 for the least significant bit has its J and K input terminals connected to the false output terminal of the flip-flop MC1 so that each time the flip-flop MC1 of the minor cycle counter is zero, the least significant flip-flop will change state in response to a clock pulse from the fast clock generator. Two NAND-gates **81** and **82** are connected to the respective true output of the flip-flop MC1 and the false output of the flip-flop EC1 to function as a NOR-gate in that when the variable inputs to both gates are false, the output of the J and K input terminals of the second stage EC2 is true, thereby causing the second flip-flop EC2 to change state only every other time the flip-flop MC1 is in the false state. Pairs of NAND gates are similarly used to control the inputs to is in the false state. Pairs of NAND-gates are similarly used to control the inputs to the remaining flip-flops EC3, EC4 and EC5 in accordance with the state of the flip-flop MC1, while for a given flip-flop an input to one of the paired NAND-gates is controlled by a third NAND gate as a function of the state of all lower order flip-flops in a conventional manner for synchronous counters.

The respective predetermined counts to be detected for the different Z modes of Z=1, Z=2 and Z=3 are effectively 23, 11 and seven. This is accomplished by allowing the counter to count to one at the initial transfer of data from the acquisition buffer to the Z-axis shift register and then detecting 24, 12 or eight. The count 24 is detected by a NAND-gate **85** having one input terminal connected to receive a mode control signal Z=1 and the remaining two input terminals connected to true output terminals of the two most significant flip-flops EC4 and EC5. The count of 12 is detected by a NAND-gate **86** having one input terminal connected to receive the mode control signal Z=2 and the remaining two input terminals connected to the true output terminals of flip-flops EC3 and EC4. The count of eight is detected by a NAND-gate **87** having one input terminal connected to receive the mode control signals Z=3 and the remaining input terminal connected to the true output terminal of the flip-flop EC4.

The output signals of the NAND-gates **85**, **86** and **87** are ORed by a NAND-gate **88**, and the output of the NAND-gate **88** is ANDed with the signal $\overline{Z\ CON}$ by a NAND-gate **89**. Together, the NAND-gates **88** and **89** function as a NOR gate such that when any input signal to the NAND-gate **88** is false, and the signal $\overline{Z\ CON}$ is also false, the common output of the NAND-gates **88** and **89** will be true.

The common output terminal of the NAND-gates **88** and **89** is connected to the J-input terminal of the flip-flop ZEMP. The K-input terminal of that flip-flop is connected to the false output terminal of the flip-flop ZSR (FIG. **7**). Since the flip-flop ZSR is set, i.e., in the one state, the next pulse MCCL will set the flip-flop ZEMP, thereby allowing the flip-flop ZSR to be reset two clock pulses later when the minor cycle counter is in the third state with MC1 and MC2 both true. The one extra clock pulse produced after the flip-flop ZSR is reset then resets the flip-flop ZEMP as shown in the timing diagram of FIG. **12**. This is so because once the flip-flop ZEMP is set, its true output terminal resets all of the flip-flops of the synchronous display element counter via a NAND-gate **90** which functions simply as an inverter. A second NAND-gate **91** is provided to similarly reset the synchronous display element counter in response to the output signal from the NAND-gate **42** (FIG. **5**) which is true when the flip-flop INIT is set upon activating the DVDS, or when the central processing unit transmits a signal Whd through the data multiplexer to deactivate the DVDS.

Setting the flip-flop ZEMP also causes the minor cycle counter to be set in the fourth anomalous state and causes the fast clock generator to be turned off after one more clock pulse is transmitted, as shown by the waveform "clock enable" which represents a composite of signal ORed to control the fast clock generator, the extra clock pulse serving to reset the flip-flop ZEMP as just described. The fast clock generator remains off until the next display element data word is transferred into the Z-axis shift register. In the meantime, the unblanking signal $\overline{ZE}$ holds the electron beam of the CRT off via the NAND gate **80** (FIG. **7**).

The next word of display element data is requested from the data multiplexer by the request control section shown in FIG. **9** in synchronism with memory cycles of the memory **12**. Thus, although data once entered in the acquisition buffer **17** is processed asynchronously under timing control of the fast clock generator **25** independently of the central processing unit, operation of the request control section **19** is synchronized by the central processing unit in response to the processor clock pulse Qq1 applied to a NAND gate **95** enables by the flip-flop DOK while the DVDS is activated.

The actual requests for data words are made by a synchronous modulo-3 counter comprising flip-flops RT1 and RT2. The true output terminal of the flip-flop RT2 is connected to the K-input terminals of both flip-flops while the J-input terminals of both flip-flops are connected to the respective false and true output terminals of the flip-flop RT1. The flip-flops sequence through three distinct states in response to clock pulses Qq1 in accordance with the following table.

Qq1	RT1	RT2
1	0	0
2	1	0
3	1	1
4	0	0
.	.	.
.	.	.
.	.	.

There is an anomalous fourth state of RT1 reset and RT2 set, but should the counter be turned on in that state when power is initially applied to the DVDS, the first clock pulse Qq1 to occur after the flip-flop DOK is set, will advance the counter to the 10 state. Thereafter, the counter will cycle through the states shown in the foregoing table.

Since the flip-flop RT1 is reset only once for every three clock pulses, its false output may be detected to request a new word of display element data only once for every three memory cycles. That is necessary when the two gray shade mode is selected since each bit of a 24-bit word constitutes a display element thereby taking three times as long as for an eight gray shade mode. It should be noted that the flip-flop RT2 is false for two out of the three states of the counter and thus can be used to select two out of three cycles for the four gray shade mode. The selection logic is $\overline{Wsrq}=(\overline{Z=3})\ (\overline{Z=1})$ RT2++$(\overline{Z=3})\ (\overline{Z=2})$ RT1. Note that if Z=3, $\overline{Wsrq}$ is low for each cycle, thus requesting data each cycle. Therefore, by connecting NAND-gates **96** and **97** to the true output terminals of the respective flip-flops RT1 and RT2, and to mode control signals, new words of display element data can be requested at the required rates for any one of the selected gray shade modes as shown.

A gated power amplifier **98** is connected to a common output terminal of the NAND-gates **96** and **97** transmits word request signals Wsrq to the data multiplexer while the flip-flop DOK is set provided a flip-flop DAC1 is not set. Flip-flops DAC1 and DAC2 delay a request for a new data word for two memory cycles, i.e., for two periods of the clock Qq1, following the acknowledgement (in the form of the signal Wrq) of a request for a first (Y) word of a block to to allow the Y-axis

D/A converter 18 (FIG 1) to settle before acquiring the first word of display element data for processing. When the data multiplexer has received a request signal $\overline{Wsrq}$ and accepted the request for data, it transmits to the DVDS the signal Wrq which sets the flip-flop DAC1 via an inverter 99 and a NAND-gate 100 in response to a clock pulse Qq2 but only if the complement $\overline{YE}$ of the Y-enable signal transmitted by the NAND-gate 53 (FIG. 6) is present indicating either that an end of a line or raster has been reached (so the next word is taken as Y word) or that the DVDS has been activated, in which case the first word is automatically taken as Y word. The signal INIT will set the flip-flop EOL (FIG. 6) to provide the necessary Y-enable signal.

After the EOLR flip-flop has been reset by a signal from the NAND-gate 58 (FIG. 6) upon transfer of the first word to the Y buffer register (FIG. 11), the flip-flop DAC2 is set in response to the next clock pulse Qq2, thereby enabling both of the flip-flops DAC1 and DAC2 to be reset by the following clock pulse Qq2, thereby delaying for two clock pulse periods any further request for a new word of data after receiving a signal Wrq any time a Y word is received. In that manner, the NAND-gate 100 and a NAND-gate 101 effectively AND the signal Wrq and the signal YE to enable the flip-flop DAC1 to be set for two periods of the clock pulse Qq2 after which the flip-flop DAC2 is set so that the next clock pulse Qq2 will reset both flip-flops DAC1 and DAC2. If the signal YE is not true, the flip-flops DAC1 and DAC2 are not set and a request for new data can be made during the next cycle as determined by the NAND-gates 96 and 97.

Referring now to FIG. 10, the X axis integrator is comprised of an operational amplifier 105 which positions the electron beam of the cathode-ray tube according to an accumulated charge on an integrating capacitor 106. For each display element processed, a known pulse $\overline{X\ stp}$ is added to the charge on the capacitor, thus increasing its charge to advance the beam along the X-axis The pulse is applied only when the minor cycle counter is in the second state with the flip-flop MC1 set and the flip-flop MC2 reset. The period of the applied pulse is thus always the period of the fast clock. However, the amplitude of the charge applied to the summing junction of the operational amplifier is programmed by the X-mode decoder 45 (FIG. 5) according to whether the octal digit decoded by the mode controller is equal to 3, 2 or 1 by respective gated amplifiers 107, 108 and 109. A gates amplifier 110 resets the X-axis integrator through a transistor switch 111 when either the DVDS is activated and the flip-flop INIT (FIG. 5) is set, thereby transmitting a signal $\overline{INIT}$ to the amplifier 110, or when the end of a line or raster has been reached such that the flip-flop EOL is set to transmit a Y-enable signal (YE) to a NAND-gate 112. That gate allows a flip-flop XD to be set when the Z shift register is empty and no Z data is left in the acquisition buffer as indicated by both $\overline{ZSR}$ and $\overline{AB}$ both being true. In that manner, after an interrupt signal Iwz, the Y-enable signal YE is generated. That signal prevents the flip-flop AB from being set and enables a Y-transfer control signal to be transmitted by a NAND-gate 58 (FIG. 6) when the next (Y) word, is in the acquisition buffer. The Y-enable signal also causes the X-axis integrator to reset upon setting the flip-flop XD. Following that, the request control section 19 of FIG. 9 requests a new word from memory. Upon acknowledgement by a signal Wrq from the data multiplexer that the request has been received, the flip-flop DAC1 is set, thus initiating a delay in further request of new data for two memory cycles in order to allow the Y-axis D/A converter and X integrator to settle, as noted hereinbefore. The signal $\overline{Zdout}$ Win indicates that the Y word is available from the computer. This resets the flip-flop XD.

Referring now to FIG. 11, as each data element of a word in the Z-axis shift register is processed, the three most significant bits are gated into Z-buffer flip-flops ZB1, ZB2 and ZB3 via groups of NAND-gates 121, 122, and 123 which receive as the transfer control signal the signal $\overline{Z\ CON}$ from the NAND-gate 77 (FIG. 7) where the state 00 of the minor cycle counter is decoded. The groups of gates 121, 122 and 123 transmit the least significant three bits to the J-input terminals of the buffer flip-flops, and complements thereof to the K-input terminals, so that upon the occurrence of the next clock pulse from the fast clock generator, the least significant three digits of the Z-axis shift register are entered in the Z-axis buffer flip-flops.

The most significant bit in the flip-flop ZB1 is applied directly to an amplifiers 124, 125 and 126 since the most significant bit is always used regardless of the gray shade mode selected. This bit therefore adds a seven or zero to the gray shade control. The remaining two bits stored in the flip-flops ZB2 and ZB3 are gated to amplifiers 125 and 126 according to the gray shade mode selected. If it is not a two gray shade mode (Z=1), a NAND-gate 127 is enabled by the Z-mode decoder 46 (FIG. 5) to allow the second most significant bit to be transmitted, and it is neither a 2 gray-shade mode or a four gray shade mode (Z=2), the Z-mode decoder 46 enables a NAND-gate 129 to transmit the third most significant bit form the flip-flop ZB3 via the amplifier 126. In the Z=1 mode, a NAND-gate 130 transmits the most significant bit to all three amplifiers.

A decoder 140 decodes the signals Z1, Z2 and Z3 from the amplifiers 124, 125, and 126 to select one out of eight weighted current sources 141 to 148 where each current source is, as shown for the current source 141, comprised of a transistor Q_1 having a weighted resistor 151 in the emitter circuit. The currents are inversely weighted so that the signal of the output terminal is a maximum positive level for blanking, and a minimum positive level for maximum brightness. For blanking control, the signal $\overline{ZE}$ is inverted by an amplifier 153 and applied to a transistor Q_2 which provides a maximum positive level at the output terminal 152.

It is evident that for flicker-free display, a frame is refreshed from memory at a suitable rate, such as forty times per second. As the rasters of a given frame are being displayed in sequence, the rasters already displayed may be updated or otherwise changed by processing the data for those rasters through the central processing unit.

What is claimed is:

1. In an electronic data processing and display system having a central processing unit, a cathode-ray tube display and an addressable means for storing display data, said display data comprising digital codes of intensity levels for a two-dimensional array of point display elements stored in blocks of words, each word consisting of a plurality of display element codes and each block comprising words for one raster of display elements preceded by one word comprising a digital code defining the position of the raster in the array, the combination comprising:

data-multiplexing means for reading said display data from said memory, one block at a time, successive words of a block of data following the first word being read in response to data request signals,

means connected to said display tube for receiving from said multiplexing means, storing, and converting into an analog signal the first word of a given block of data, whereby the position of an electron beam is controlled for display of a raster;

means including a shift register for receiving from said multiplexing means each subsequent word read in sequence following said first word of a given block, and for shifting each word in a given direction toward one end of said register in response to clock pulses;

means for generating clock pulses;

means connected to said display tube for receiving from said one end of said register data for display elements, and for converting data for each element into an analog signal to control the intensity of said electron beam;

means connected to said display device synchronized with said shift register means for integrating step control pulses, one step control pulse for each display-element conversion to produce an element positioning signal for said electron beam in a direction orthogonal to the direction of control for raster position control;

means synchronized with said first-word receiving means for resetting said step-pulse integrating means whereby, upon starting to process a new raster of display data, said electron beam is returned to the starting side of said display tube for the next raster of display elements; and

means synchronized with said step-pulse integrating means and said resetting means for blanking said electron beam during each step pulse integration period to permit display of an element at a given position only after said beam has reached said given position, and during return periods of said electron beam upon starting a new raster of display.

2. In an electronic data processing and display system, the combination of claim 1 wherein said display data may be for more than two levels of intensity control for each element, and additional levels are specified by codes of more than the one binary digit necessary for the two-level intensity control to a maximum of n bits, whereby a plurality of gray shade modes of display are possible, and wherein said shift register means includes a minor-cycle counting means for counting n clock pulses for each display element cycle of any gray shade mode designated, said combination including:

means for designating a selected one of said gray shade modes of display;

means responsive to said gray shade designating means and said minor-cycle counting means for applying to said shift register during each minor cycle a number of clock pulses corresponding to the number of binary digits necessary for the number of levels of intensity control designated by said gray shade mode designating means; and

wherein said data element converting means is responsive to said minor-cycle counting means to convert data for each element into an analog signal during the first clock period of each minor cycle, said step integrating means is responsive to said minor-cycle counting means to advance the electron beam position during the first clock period of each minor cycle, and said blanking means is responsive to said minor-cycle counting means during the first clock period of each minor cycle whereby each display element is presented for $n-1$ clock periods for any one of said gray shade modes designated.

3. In an electronic data processing and display system, the combination of claim 1 including:

means for designating one of a plurality of different numbers of units of spacing to be provided between elements displayed; and

wherein said step integrating means includes means responsive to said last-named means for weighting said step control pulses to produce deflection control steps in said element-positioning signal of amplitudes corresponding to the number of units of spacing designated.

4. In an electronic data processing and display system, the combination of claim 2 including:

means for designating one of a plurality of different numbers of units of spacing to be provided between elements displayed; and

wherein said step integrating means includes means responsive to said last-named means for weighting said step control pulses to produce deflection control steps in said element-positioning signal of amplitudes corresponding to the number of units of spacing designated.

5. In an electronic data processing and display system, the combination of claim 2 wherein said central processing unit, data-multiplexing means and memory are synchronized by system clock pulses, and said minor-cycle clock pulses are produced at a rate which assures each word of display data to be processed through said shift register during one system clock period for a gray shade mode of a maximum number of levels and minimum number of elements per word, said combination including means responsive to said gray shade designating means and said system clock pulses for generating said data request signals at the rate of $n-k$ request signals out of n cycles of said system clock pulses, where k in an integer from 0 to $n-1$ such that the difference $n-k$ is the number of data bits of each display element, and including buffer storage means for storing words read out of said memory as requested until needed for processing through said register.

6. In an electronic data processing and display system, the combination of claim 5 including:

means for counting display elements processed through said display element converting means; and

means responsive to said gray shade designating means and said display element counting means for resetting said shift register and entering therein a new word of data from said buffer storage means when all display elements of a word have been processed.

7. In an electronic data processing and display system, the combination of claim 6 wherein said minor-cycle counting means comprises a cyclic counter having n stable states and an additional anomalous stable state from which the cycle of said n stable states is entered in response to a clock pulse, said combination including means for setting said cyclic counter into its additional anomalous state upon resetting said shift register, and for preventing clock pulses from being applied to said cyclic counter and shift register until a new new word of data has been entered in said shift register from said buffer storage means.

8. In an electronic data processing and display system, the combination of claim 2 wherein said means for designating a gray shade mode of display operation comprises means for receiving and decoding a group of binary digits transmitted by said data processing unit and for storing a signal indicating the gray shade mode designated by said group of binary digits, whereby said gray shade mode of operation is programmed by said data processing unit.

9. In an electronic data processing and display system, the combination of claim 4 wherein said means for designating a gray shade mode of display operation comprises means for receiving and decoding a group of binary digits transmitted by said data processing unit and for storing a signal indicating the gray shade mode designated by said group of binary digits, whereby said gray shade mode of operation is programmed by said data processing unit; and

wherein said means for designating units of spacing to be provided between elements displayed comprises means for receiving and decoding a second group of binary digits transmitted by said data processing unit, and for storing a signal indicating the stepping mode designated by said second group of binary digits, whereby said stepping mode of operation is programmed by said data processing unit.

10. In an electronic data processing and display system, the combination of claim 9 wherein said data processing unit is a digital computer having a stored program, and said first and second groups of binary digits are transmitted in response to a single programmed instruction executed in preparation for the display of data.

11. A digital video display system for display of data in a two-dimensional array of points, each point being a discrete display element, comprising:

a random access digital memory system having fixed memory access cycles;

a data-multiplexing system for reading data out of said memory in blocks of data words;

a central processing unit responsive to a program stored in said memory system for activating said data-multiplexing unit, selecting the number of interelement spacing units, and one of n gray shade modes for display of each element with units of intensity for the respective modes 2^1 to 2^n of 2^0 to 2^{n-1}, where n is an integer and the exponents are successive integers from 1 to n and 0 to $n-1$;

a cathode-ray tube display unit;

means responsive to the first word of each block for setting the Y-axis position of an electron beam in said cathode-ray tube display unit in accordance with the binary code of said first word;

means responsive to each word of a block following the first for specifying units of intensity for display of elements in sequence, each word having m bits divided into group of bits, each group having a number of bits corresponding to the exponent of the gray shade mode specified;

means responsive to each group of digits specifying the units of intensity for a display element signal of said cathode-ray tube display unit a number of interelement spacing units corresponding to that specified by said central processing unit from a predetermined initial value;

means responsive to said data-multiplexing system for automatically resetting said incrementing means when the reading of a new block of data is initiated; and

means for blanking said electron beam while said incrementing means is being incremented, and while said Y-axis setting means is setting said electron beam to the new Y-axis position specified by the binary code of the first word of said new block of data.

12. A digital video display system as defined by claim **11**, including means for counting said memory access cycles, and means responsive to said counting means for requesting a new word to be read out of said memory system each cycle when the 2^n gray shade mode has been specified, and k out of n cycles when a 2^k gray shade mode has been specified, where k is an integer from 1 to $n-1$.

13. A digital video display system as defined by claim **12** including:

a clock pulse generator;

a counter having n cyclic states and an additional anomalous state from which it enters the regular cycle of counting pulses from said clock generator for controlling display of one display element per cycle;

means for setting said element control counter in said anomalous state at the beginning of each word of display element data to be processed;

clock pulse gating means;

a shift register for receiving each word of display element data in parallel and for shifting a word in a given direction towards one end thereof in response to clock pulses from said gating means;

means for controlling said gating means to transmit to said shift register n out of n clock pulses when the 2^n gray shade mode has been specified and k out of n clock pulses when a 2^k gray shade mode has been specified; and

means responsive to said element control counter for decoding n bits at said one end of said shift register during each cycle of said control counter for control of electron beam intensity when the 2^n gray shade mode has been specified and k bits when a 2^k gray shade mode has been specified.

14. A digital video display system as defined by claim **13** wherein said incrementing means in an integrating operational amplifier which receives a weighted pulse of current once during each cycle of said element control cycle, and wherein the weighting of said pulses is in accordance with the interelement spacing specified.

15. A digital video display system as defined by claim **14** including a display element counting means for counting the number of display element groups of bits decoded from a given word, and means responsive to said display element counting means for effecting transfer of a new word of data into said shift register when a number of group of bits have been counted equal to m divided by n for a 2^n gray shade mode of operation specified and m divided by k for a 2^k gray shade mode of operation specified.

16. A digital video display system as defined in claim **14** including 2^n weighted intensity control signal generators and wherein said decoding means selects one of said 2^n signal generators for maximum intensity selection when k is equal to 1, maximum and intermediate intensity when k is equal to 2, and k equally spaced intensities when k is greater than 2.

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