



(51) International Patent Classification:
H04L 12/715 (2013.01) H04L 12/761 (2013.01)
(21) International Application Number:
PCT/US2016/049315
(22) International Filing Date:
29 August 2016 (29.08.2016)
(25) Filing Language:
English
(26) Publication Language:
English
(30) Priority Data:
62/211,512 28 August 2015 (28.08.2015) US

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(54) Title: NETWORK ADDRESS ASSIGNMENT AND RECLAMATION FOR HIERARCHICAL BASED RPL NETWORKS

(57) Abstract: This invention is an improvement of a Hierarchical Do-Dag based RPL (H-DOC) network configuration where the network address of each node corresponds to its location within the hierarchical network. Network addresses are initialized hierarchically (600). Candidate parent nodes signal availability (602). Candidate child nodes select a candidate parent node (603) and respond with a temporary address (604). The selected candidate parent node acknowledges selection and communicates a hierarchical address for the child node in a transmission to the temporary address (605). The child node changes its address to the hierarchical address from the parent node (606).

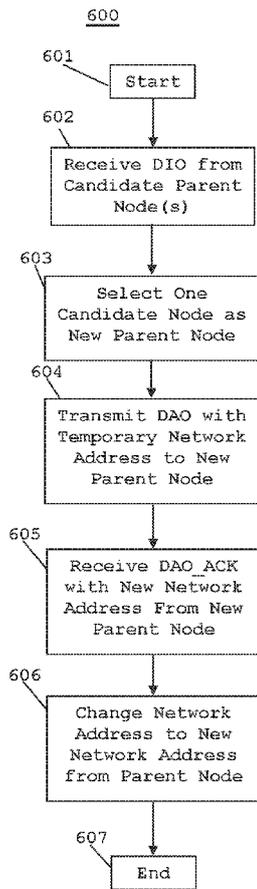


FIG. 6

WO 2017/040425 A1



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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH,

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

NETWORK ADDRESS ASSIGNMENT AND RECLAMATION FOR HIERARCHICAL BASED RPL NETWORKS

[0001] This relates to network communication including nodes having alterable addresses.

BACKGROUND

[0002] Ad hoc wireless communications networks are formed dynamically as nodes come within range of existing network resources. These networks may be utilized in many applications to provide communications between lower level devices on the networks such as sensors and upper tier devices communicating with these sensors. The sensors typically operate with limited processing and memory and are often constrained by various technical limitations. Such limitations may include issues related to power consumption, small form factors and communication challenges (low speed, high error rates, and so forth) used to form the respective networks. The challenges are further complicated as there can be interdependence between the issues. For example, the level of communication within the networks impacts the power consumption in the network devices.

[0003] This disclosure relates to address generation for such ad hoc communications networks. A network includes at least two nodes that employ a routing protocol to communicate across the network. The routing protocol can be a Routing for Low Power (RPL) networks protocol, for example. One of the nodes is a parent node and other nodes are child nodes of the parent node. In some cases, the parent node can be a root node which is at the top of a hierarchical network. In other cases, the parent node can also be an intermediate node that is downstream from the root node yet can have other child nodes, sometimes referred to as leaf nodes, communicating with it.

SUMMARY

[0004] An address generator assigns a unique network address to each node by appending an address value of a number of bits to a parent address of the parent node to create the unique network address for the child node. In this manner, each node in the network can assume its identity in part from its respective parent while creating a unique network address via various assignment protocols disclosed herein. The address assignment protocol allows each node to know which is the next hop in the ad hoc network for message routing since each node can

determine whether to route a message upstream or downstream based on its derived parental address assignment. This alleviates the need for routing tables as with conventional systems and thereby conserves memory in the respective nodes of the system. Moreover, handshaking in the network is reduced since each intermediate node that encounters a new child node does not have to communicate additional address announcements to the network since the incoming node is already a part of the parent's node address. Reducing handshaking communications reduces the power expended in the system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 (prior art) is a block diagram of example node.

[0006] FIG. 2 (prior art) illustrates a hierarchical network of nodes.

[0007] FIG. 3 (prior art) is a view of address segments in a hierarchical network address technique.

[0008] FIG. 4 is a flow chart illustrating message routing when employing the hierarchical network address technique of FIG. 3.

[0009] FIG. 5 is a flow chart illustrating actions of a potential parent node in network address initialization according to this invention.

[0010] FIG. 6 is a flow chart illustrating actions of a potential child node in network address initialization according to this invention.

[0011] FIG. 7 is a flow chart illustrating actions of a chosen parent node in network address initialization according to this invention.

[0012] FIG. 8 is a flow chart illustrating actions of a child node when changing parent nodes according to this invention.

[0013] FIG. 9 is a flow chart illustrating actions of the old parent node when changing parent nodes according to this invention.

[0014] FIG. 10 is a flow chart illustrating actions of the new parent node when changing parent nodes according to this invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0015] FIG. 1 (prior art) is a flow chart of an example node 100. Node 100 is one of a plurality of nodes typically employed. Node 100 includes communications transceiver 101. Communications transceiver 101 enables bi-directional communication with other nodes. In accordance with the known art, each node is provided with a communications address. Node

100 is only responsive to communications having a message header identifying node 100 as the destination node. This identification is typically made by the destination node's communications address. The node communications address is described more fully below. Node 100 illustrated in FIG. 1 is not limited to a particular communications medium. It is typical to provide wireless communication between nodes via low power radio frequency signals.

[0016] Node 100 includes node controller 102. Node controller 102 typically includes a programmable microprocessor. This microprocessor of node controller 102 provides the operating features of node 100. Node controller 102 may exchange messages with other nodes via a bi-directional connection to communications transceiver 101. As known in the art the microprocessor of node controller 102 is programmed by instructions stored in memory 103. Memory 103 typically includes both non-volatile memory, whose contents do not depend upon continual electrical power, such as read only memory (ROM) or FLASH memory, and volatile memory, commonly known as random access memory (RAM), whose contents are lost on interruption of electrical power. Typically program instructions are stored in non-volatile memory and more ephemeral data is stored in volatile memory. Node controller 102 communicates with sensor 105 and actuator 106 (described below) and with other nodes via communications transceiver 101. As illustrated in FIG. 1, memory 103 includes at least a portion 104 devoted to storing a network address assigned to the node 100. As will be described below, node 100 is only responsive to messages having a destination address matching network address 104 stored in memory 103.

[0017] Node 100 optionally includes one or more sensors 105 or actuators 106. Typically plural nodes such as node 100 are employed together. The sensors 105 detect environmental conditions for use by the network of nodes. These environmental conditions could be ambient temperature, wind speed, pressure and the like. The actuators 106 may be used to control the environment according to commands received from the network of nodes. An actuator may include an electrical switch, a fluid valve or control of motive parts of node 100. Any particular example of a node may include one or more sensors and one or more actuators, only one sensor or only one actuator.

[0018] Node 100 includes power supply 107. In the typical application node 100 is designed to employ very little electric power. Power supply 107 may be a small battery. In other applications power supply 107 is designed to scavenge power from the environments. This

could be a solar cell with a back-up capacitor or other power storage for dark intervals. Alternatively, this could be some sort of motion capture device that generates electric power from environmental motion. An example is a weather buoy that generates electric power from wave motion.

[0019] FIG. 2 illustrates a prior art preferred communication among nodes in a network of such nodes. In the preferred embodiment, the nodes are disposed in a hierarchical network. Network 200 illustrates a single Level 0 node N1 also known as the root node. Level 0 node N1 communicates directly with Level 1 nodes N2 and N3. Level 1 node N2 communicates directly with Level 2 nodes N4 and N5. Level 1 node N3 communicates directly with Level 2 nodes N6 and N7. Level N nodes N16 to N63 communicate directly with Level N-1 nodes (not shown). The Top Level node N1 thus directly communicates with only child nodes N2 and N3. Level 1 node N2 communicates with parent node N1 and child nodes N4 and N5. Level 1 node N3 communicates directly with parent node N1 and with child nodes N6 and N7. At the bottom level (Level N) each node N16 to N64 communicates directly its respective parent node (not shown).

[0020] As noted above, a network of nodes according to this invention typically employs wireless communication between nodes via low power radio frequency signals. Thus a parent node is not hardwired to its child nodes. All the wireless communication may share one or just a few radio frequencies. This environment requires some manner for a node to determine whether a communication is intended for it. Such networks typically employ a network address to distinguish communications. Each node in the network is assigned a network address. Each communication in the network includes reference to the network address of the destination node. This destination node network address is typically specified in a message header. Upon receiving a communication, each node extracts the destination node network address from the message. The node compares this destination node network address with its own network address. The node responds to the message if the destination node network address matches its own network address. The node ignores this communication if the destination node network address does not match its own network address. The node may also route the message to its parent node or one of its child nodes in an attempt to reach the destination node. It is typical for a node to handle (service or route) only messages from its parent node or from one of its child nodes.

[0021] Provision of network address for destination nodes identifies the desired node. The destination network address does not automatically provide information on routing. In the preferred embodiment using low power radio frequency signals for communication, not all nodes will be in range of all other nodes. In the preferred embodiment only a parent node and its child node(s) are guaranteed to be in communication. Thus a communication directed to another node must either be sent up the hierarchy to the parent node or down the hierarchy to an appropriate child node.

[0022] The communications between parent and child nodes occur according to a network routing protocol. The routing protocol can be Routing for Low Power Networks (RPL) protocol, for example. The parent node can be a root node or an intermediate node and the child node can be a leaf node to the root node or the intermediate node in a destination oriented directed acyclic graph (DODAG) configuration. The DODAG consists of at least one root node and at least one leaf node.

[0023] In order to properly route a communications directed to another node, each node must access routing information for the destination node. The RPL routing protocol has two modes of operation. The first mode is the storing mode. The second mode is the non-storing mode. In the RPL protocol storing mode, each node stores information for routing to all other nodes in memory 103. Upon receipt a communication node controller 102 extracts the destination node address. If this address matches the node address, the node responds to the communication. If this destination node address does not match the node address, the node must route the communication to another node. Node controller 102 consults the stored routing information to determine the routing of the communication. The routing table need only indicate whether the communication is to be routed up the hierarchical network or down the hierarchical network to one of the node's child nodes. This technique is disadvantageous because it requires storing a routing table at each node. This is a burden on hardware because it requires memory and power at each node to store the routing table. The routing table size is linearly proportional to the number of child nodes for that node plus one additional entry for the parent. This is disadvantageous for low cost, low power nodes. In the RPL protocol non-storing mode, only the root node stores information for routing. All communications between any pair of nodes must first be routed up the root node. The root node routes the communication to the appropriate child and grandchild nodes based upon its routing table. This technique eliminates the requirement for

storing a routing table at each node. However, this technique increases the communications traffic due because all communications must pass through the root node.

[0024] The network configuration illustrated in FIG. 2 is known as a directed acyclic graph (DODAG) configuration. As shown in FIG. 2, the DODAG consists of at least one root node and at least one leaf node. Candidate parent nodes transmit DODAG information object request (DIO) signals indicating their availability as a parent node. Candidate child nodes respond with a Destination Advertisement Object (DAO) signal to their preferred parent node in response to a DIO.

[0025] FIG. 3 illustrates features of a prior art hierarchical Do_Dag based RPL network (H-DOC) addressing technique advantageously used with the hierarchical network illustrated in FIG. 2. For each node network address 300 includes prefix bits 301, level 1 bits 302, level 2 bits 303 ... level N bits 309. Prefix bits 301 includes bits common to all nodes in the network and bits associated with the root node. All nodes within the hierarchical network include the bits in prefix bits 301. For the root node of the network all other bit fields (302, 303 ... 309) have a predetermined null value such as all 0s. Each node at level 1 includes prefix bits 301 having the same value as the root node and a unique value within the level 1 bits 302 from all other level 1 nodes. For level 1 nodes all other bit fields (303 ... 309) have the predetermined null value. Each node at level 2 includes prefix bits 301 having the same value as the root node, level 1 bits 302 having the same value as its parent node and a unique value within the level 2 bits 302 from among all other level 2 nodes having the same parent level 1 node. For level 2 nodes all other bit fields (... 309) have the predetermined null value. The number of address bits assigned to each level field is a design choice dependent upon the desired parent-child fan out. Note that the order of the level fields within the network address is arbitrary. That is, the level fields can be in any order and not just the high bits to low bits order illustrated in FIG. 3. It is merely required that all nodes within the network employ the same level field order.

[0026] One feature of this hierarchical network address technique is that the network address of each node corresponds to its location within the hierarchical network. Each node has a network address dependent upon its parent node and all intermediate nodes up the hierarchy to the root node. This simplifies the routing decision made at each node.

[0027] FIG. 4 illustrates a flow chart of the process 400 for handling message routing when employing hierarchical addresses. In the preferred embodiment, memory 103 at each node stores

instructions causing node controller 102 to perform this process. There are three routing possibilities. The message may need to be routed the parent of the current node up the hierarchy. The message may be intended for the current node. The message may need to be routed to a child node of the current node down the hierarchy. A message received from the parent node of the current node may be directed to the current node or need to be routed to a down hierarchy node. A message from a child node may need to be routed to the parent node up the hierarchy, may be directed to the current node or need to be routed to a down hierarchy to another child node.

[0028] Process 400 begins upon receipt of a message from another node (block 401). The node extracts the destination address from the message header (block 402). The routing of the message depends upon the relationship of the destination address to the node address of the current node.

[0029] Test block 403 determines if the destination address matches higher level address slots of the current node address and does not match current level address of the current node address. If so (Yes at test block 403), then the message should be routed up the hierarchy. Block 404 routes the message to the parent node of the current node. Following this routing of the message in block 404, process 400 ends at end block 405. If not so (No at test block 403), then flow passed to test block 406.

[0030] Test block 406 determines if the destination address matches the address of the current node including predetermined null values for level fields below the current node level. If the destination address matches the address of the current node including predetermined null values for level fields below the current node level (Yes at test block 406), then the current node is the intended destination. Accordingly, block 407 services the message. The exact manner of servicing the message depends upon the intended use of the network. The message could be a request for data from a sensor 104 at the current node. The message could be a command to take some action via actuator 105 the current node. The exact nature of servicing this message is beyond the scope of this invention. Following service of the message in block 407, process 400 ends at end block 408.

[0031] If the destination address does not match the address of the current node including predetermined null values for level fields below the current node level (No at test block 406), then the current node is not the intended destination. Test block 409 determines if the

destination node address matches the fields of the current node address and further includes significant lower level address fields. If this is true (Yes at test block 409), then the message is routed to a child node of the current node. Block 410 routes the message down hierarchy to an appropriate child node. The appropriate child node is determined by the level address field one level below the level of the current node. Following this routing of the message in block 410, process 400 ends at end block 411.

[0032] If none of these conditions are met (No at test block 403, No at test block 406 and No at test block 409), then there is an error in the destination address. Error handling block 412 handles this error. This is beyond the scope of this invention.

[0033] There are serious limitations in practical implementation of the H-DOC technique. There is no clean way to assign node addresses in the network. There is no provision for reassigning node address. It is complicated or impossible for a node to change its parent node. Such a change may be needed if the nodes are mobile. This invention, addresses the limitations of the H-DOC technique for address assignment and reassignment for mesh networks. This invention slightly modifies two messages used in RPL networks employing the H-DOC technique. In the prior art, a node sends a DODAG information object request (DIO) message to its potential child nodes. A child node desiring to connect to that node responds with a Destination Advertisement Object (DAO) message. In general, each node connects with its parent node before attempting to connect with a child node. This invention provides better assignment of network addresses in the hierarchical network.

[0034] FIGS. 5 to 7 together illustrate hierarchical address initialization according to this invention. FIG. 5 illustrates process 500 taking place on candidate parent nodes. FIG. 6 illustrates process 600 taking place on candidate child nodes. FIG. 7 illustrates process 700 taking place on a chosen parent node.

[0035] FIG. 5 illustrates process 500 on a candidate parent node beginning at start block 501. In the preferred embodiment, memory 103 at each node stores instructions causing node controller 102 to perform this process. The candidate parent node broadcasts a DIO signal at block 502. The DIO signal is similar to the prior art. The DIO signal announces the transmitting node's availability as a parent node and its network address. This DIO signal is typically broadcast to all candidate child nodes of the transmitting node. Such a broadcast is possible in the typical network using wireless communication. The initialization process preferably starts

with the root node and proceeds down the hierarchy. The root node is assumed to know it is the root node and begins initialization. A node cannot transmit a DIO signal to connect to child nodes until it has been attached to a parent node. Transmission of a DIO signal indicates that the current node can accept at least one node as a child. Thus this guarantees that the current node has fewer than the maximum number of child nodes assigned as limited by the size of the next level field in FIG. 3. Process 500 ends with end block 503.

[0036] FIG. 6 illustrates process 600 of a candidate child node. In the preferred embodiment, memory 103 at each node stores instructions causing node controller 102 to perform this process. Process 600 begins at start block 601. The candidate child node receives at least one DIO signal from a candidate parent node at block 602. The candidate child node selects a parent node from among the received DIO signals. The manner of this selection is not important to this invention. This selection includes identifying the network address of the selected parent node from the received DIO signal. In block 604 the node transmits a DAO signal to the selected parent node. This DAO signal is directed to the selected parent node via a destination network address matching the network address of the selected parent node extracted from the DIO signal. In accordance with this invention, this DAO signal includes information regarding a temporary network address to which the transmitting node will be responsive. This temporary node address may be an address selected from a set of node addresses set aside for this purpose.

[0037] FIG. 7 illustrates process 700 taken by a selected parent node. In the preferred embodiment, memory 103 at each node stores instructions causing node controller 102 to perform this process. Process 700 begins with start block 701. The selected parent node receives a DAO signal in block 702. As noted above this DAO signal is directed to the current node by destination address and includes an indication of the temporary address of the child node. In block 703 the process 700 selects an available network address to assign to the requesting node. As noted above, this node transmitted a DIO signal (block 502) indicating availability as a parent node. This guarantees that the current node can accept another child node. This node stores an indication of the network addresses of currently assigned child nodes. Process 700 then transmits a DAO_ACK signal back to the requesting node (block 704). This DAO_ACK signal is transmitted to the temporary address of the received DAO signal (block 702). This DAO_ACK signal includes a payload indicating the network address assigned to this child node in block 703. As indicated in conjunction with FIG. 3, according to the hierarchical

address technique this assigned address includes high level fields down to the level of the parent node identical to the network address of the parent node. The field one level below the level of the parent node is set to an unused address from among currently assigned child nodes, if any. Process 700 ends with end block 705.

[0038] Process 600 (FIG. 6) continues at block 604. The node receives a DIA_ACK signal from the selected parent node (block 605). As noted above this DAO_ACK signal includes a child network address assigned by the selected parent node. The child node then changes its network address to the assigned address included in payload of the DAO_ACK transmission (block 606). The current node then is responsive to this newly assigned child address in a manner described above. Process 600 ends with end block 607. As previously described, upon this assignment of network address this child node may transmit a DIO signal indicating it can be a parent node to other nodes.

[0039] The prior art hierarchical address technique did not provide a manner of rearranging the network once initialized. If the network includes mobile nodes, a node may move to a location where its current parent node is more accessible. Due to the hierarchical nature of the address, this requires reassignment of the address of the child node. FIGS. 8 to 10 illustrated this process. FIG. 8 illustrates process 800 taking place on the moving child node. FIG. 9 illustrates process 900 taking place on the old parent node. FIG. 10 illustrates process 1000 taking place on the new parent node.

[0040] FIG. 8 illustrates process 800 taking place on the moving child node. In the preferred embodiment, memory 103 at each node stores instructions causing node controller 102 to perform this process. Process 800 begins at start block 801. It is assumed that the child node has determined to change parent nodes and that it has selected the identity (and hence the network address) of the new parent node. Process 800 transmits a new signal DAO_NO_PATH to the old parent node. The child node directs this transmission to the network address of the old parent node. This DAO_NO_PATH signal also identifies the transmitting node preferably by the old network address.

[0041] FIG. 9 illustrates process 900 taking place on the old parent node. In the preferred embodiment, memory 103 at each node stores instructions causing node controller 102 to perform this process. Process 900 begins with start block 901. The old parent node receives a DAO_NO_PATH signal at block 902. In response to the DAO_NO_PATH signal the old parent

node deallocates the address assigned to the transmitting node (block 903). Thus the old parent node is no longer the parent of the transmitting node. Process 900 ends at end block 904.

[0042] Returning to FIG. 8, following transmission of the DAO_NO_PATH signal the moving child node transmits a DAO signal to the selected new parent node (block 803). This process is similar block 604 described above. The DAO signal includes a destination node indicating the selected new parent node. The DAO signal also includes a temporary node address for reply. This temporary node address may be the prior address. Note the old parent node has deallocated this node address and will not attempt to communicate with the moving child node via this address. This temporary node address may be an address selected from a set of node addresses set aside for this purpose.

[0043] FIG. 10 illustrates process 1000 taking place on the new parent node. In the preferred embodiment, memory 103 at each node stores instructions causing node controller 102 to perform this process. Process 1000 begins with start block 1001. At block 1002 the new parent node receives a DAO signal which includes an indication of the temporary address of the child node. In test block 1003 process 1000 determines whether a network address is available for a new child node. This slightly differs from process 700 illustrated in FIG. 7. In process 700 the node has transmitted a DIO signal indicating availability to accept a new child node. In process 1000 the selected parent node may not have a network address available to allocate to another child node. If the new parent node has an available network for allocation to a new child node (Yes at test block 1003), the process 1000 selects an available network address for allocation to the requesting node in block 1004. Process 1000 then transmits a DAO_ACK signal back to the requesting node (block 1006). This DAO_ACK signal is transmitted to the temporary address of the received DAO signal (block 1002). This DAO_ACK signal includes a payload indicating the network address selected for this child node in block 1004. Process 1000 ends with end block 1006.

[0044] If the new parent node does not have an available network for allocation to a new child node (No at test block 1003), the process 1000 begins error handling in block 1007. This error handling may be failing to respond to the DAO signal. This relies upon the requesting child node to note the lack of response (via a time out for example) and select another new parent node. This may be by sending a not acknowledge (NAK) signal to the requesting node. The requesting node responds to the NAK signal by selecting another new parent node and

transmitting a new DAO signal. Following error handling, process 1000 ends with end block 1006.

[0045] Returning to FIG. 8, following transmission of the DAO signal (block 804), process 800 continues at block 804 by receiving the DIA_ACK signal from the new parent node. As noted above this DAO_ACK signal includes a network address assigned by the new parent node. The child node then changes its network address to the assigned address included in the DAO_ACK transmission (block 807). The current node then is responsive to this newly assigned child address in a manner described above. Process 800 ends with end block 806.

[0046] This invention may be practiced employing a MAC_ACK signal rather than the DAO_ACK signal. This MAC_ACK signal similarly is directed to the temporary address of the requesting child node and includes the newly assigned network address as part of the payload.

[0047] This invention has the following advantages in network address assignment and reclamation. This invention is a simple and elegant solution for network address assignment, reclamation and reassignment. This invention uses the same underlying principles for all three aspects of address management. This invention is fully compliant with existing standards by using payload network address information. This invention does not incur any additional implementation overhead. This invention ensures that the hierarchical Do_Dag based RPL network (H-DOC) operates with a routing table size of 1 (corresponding to the node network address).

CLAIMS

What is claimed is:

1. A method of network address initialization in a directed acyclic graph (DODAG) network configuration including a plurality of nodes including a root node, the network address having predetermined level subsets corresponding to plural hierarchical levels of the nodes, the method comprising:

the root node broadcasting a DODAG information object request (DIO) signal to at least one candidate child node indicating availability as a parent node and a root node address including a first level address subset having a predetermined root node set of bits and at least one additional level of address subsets each having a predetermined set of null bits;

receiving the DIO signal at a candidate child node;

transmitting from the candidate child node to the root node at the root node address a Destination Advertisement Object (DAO) signal indicating a desire to become a child node of the root node and a temporary network address to which the child node will be responsive;

receiving the DAO signal at the root node;

selecting at the root node a hierarchical address for the candidate child node consisting of the first level address subset, a second level address subset selected to be unique to the candidate child node and each of the additional level of address subsets having the predetermined null set of bits;

transmitting from the root node to the child node at the temporary address a DAO_ACK signal including an indication of the hierarchical address;

receiving the DAO_ACK signal at the child node; and

changing at the child node the address to which it is responsive from the temporary address to the hierarchical address included in the DAO_ACK signal.

2. The method of claim 1 further comprising: upon confirmation as a child node by changing the address to which it is responsive,

each node broadcasting a DODAG information object request (DIO) signal to at least one candidate child node indicating availability as a parent node and a node address level address subsets equal to its address and at least one additional level of address subsets each having a predetermined set of null bits,

receiving the DIO signal at a candidate child node,

transmitting from the candidate child node to the node at the node address a Destination Advertisement Object (DAO) signal indicating a desire to become a child node of the node and a temporary network address to which the child node will be responsive,

receiving the DAO signal at the node,

selecting a hierarchical address for the candidate child node consisting of the first level address subset, a second level address subset selected to be unique to the candidate child node and each of the additional level of address subsets having the predetermined null set of bits,

transmitting from the node to the child node at the temporary address a DAO_ACK signal including an indication of the hierarchical address,

receiving the DAO_ACK signal at the child node, and

changing at the child node the address to which it is responsive from the temporary address to the hierarchical address included in the DAO_ACK signal.

3. A method of changing a hierarchical network address in a directed acyclic graph (DODAG) network configuration including a plurality of nodes organized as parent nodes and child nodes, the method comprising:

determining at a child node to change network address;

determining at the child node a preferred new parent node;

transmitting from the child node to an old parent node a DAO_NO_PATH signal indicating determination to no longer be a child node of the old parent node;

receiving the DAO_NO_PATH signal at the old parent node;

deallocating at the old parent node the child status of a node transmitting the DAO_NO_PATH signal;

transmitting from the child node to a selected candidate parent node a Destination Advertisement Object (DAO) signal indicating a desire to become a child node of the node and a temporary network address to which the child node will be responsive;

receiving the DAO signal at the candidate parent node;

selecting at the candidate parent node a hierarchical address for the child node consisting of at least one level address subset corresponding to a network address of the candidate parent node, a second level address subset selected to be unique to the candidate child node and each of the additional level of address subsets having the predetermined null set of bits;

transmitting from the candidate parent node to the child node at the temporary address a

DAO_ACK signal including an indication of the selected hierarchical address;

receiving the DAO_ACK signal at the child node; and

changing at the child node the address to which it is responsive from the temporary address to the hierarchical address included in the DAO_ACK signal.

4. The method of claim 3, wherein the temporary address of the child node is a prior address of the child node.

5. The method of claim 3, wherein the temporary address of the child node is an address selected from a set of addresses set aside for temporary addresses.

6. A method of network communication in a directed acyclic graph (DODAG) network configuration including a plurality of hierarchically disposed nodes including a root node, the network address having predetermined level subsets corresponding to plural hierarchical levels of the nodes, the method comprising:

comparing a destination address of a communication received at a node to the network address of the node;

routing the communication to a parent node if the subset of the destination address corresponding to the hierarchical level of the network address of the node does not match the subset of that hierarchical level of the network address of the node;

receiving the communication for service at the node if the destination address matches the network address of the node; and

routing the communication to a child node if the destination node address of the hierarchical level of the node and all higher hierarchical levels matches the subset of the network address of the node and the destination node address further includes significant lower level address fields, the child node to which the communication is routed having a subset network address one hierarchical level below the level of the current node matching the destination address.

7. A node for use in a directed acyclic graph (DODAG) network configuration including a plurality of nodes, comprising:

a communication transceiver operable to communicate with at least a parent node and at least one child node;

a node controller connected to the communication transceiver for control of functions of the node;

a memory connected to the node controller storing a control program and a network address for the node controller, the control program operable to cause the node controller to: receive a DODAG information object request (DIO) from a candidate parent node; determine whether to connect as a child node to the candidate parent node; transmit to the candidate parent node a Destination Advertisement Object (DAO) signal indicating a desire to become a child node of the candidate parent node and a temporary network address to which the node will be responsive; receive a DAO_ACK signal from the candidate parent node including a selected hierarchical network address; and change the network address stored in the memory from the temporary address to the hierarchical address included in the DAO_ACK signal.

8. The node of claim 7, wherein the control program stored in the memory is further operable to cause the node controller to: determine whether to change a current parent node to a new parent node; and upon determining to change the current parent node to a new parent node, transmit a DAO_NO_PATH signal indicating determination to no longer be a child node of the current parent node to the current parent node.

9. The node of claim 8, wherein the control program stored in the memory is further operable following transmission of DAO_NO_PATH signal to cause the node controller to: select another node in the acyclic graph (DODAG) network configuration to be a parent node of the current node; and transmit to the selected parent node a Destination Advertisement Object (DAO) signal indicating a desire to become a child node of the selected parent node and a temporary network address to which the node will be responsive.

10. A node for use in a directed acyclic graph (DODAG) network configuration including a plurality of nodes, comprising:

a communication transceiver operable to communicate with at least a parent node and at least one child node;

a node controller connected to the communication transceiver for control of functions of the node;

a memory connected to the node controller storing a control program and a network address for the node controller, the control program operable upon receiving a Destination Advertisement Object (DAO) signal indicating a desire to become a child node of the node and a temporary network address to which the child node will be responsive to cause the node controller to: select a hierarchical address for the child node consisting of the first level address

subset, a second level address subset selected to be unique to the candidate child node and each of the additional level of address subsets having the predetermined null set of bits; and transmit to the child node at the temporary address a DAO_ACK signal including an indication of the selected hierarchical address.

11. The node of claim 10, wherein the control program stored in the memory is further operable following receiving a DAO_NO_PATH signal to cause the node controller to: deallocate the child status of a node transmitting the DAO_NO_PATH signal.

12. A node for use in a directed acyclic graph (DODAG) network configuration including a plurality of nodes, each node except a root node having a parent node, comprising:

- a communication transceiver operable to communicate with at least a parent node and at least one child node;

- a node controller connected to the communication transceiver for control of functions of the node;

- a memory connected to the node controller storing a control program and a network address for the node controller, the control program operable to cause the node controller to:

- compare a destination address of a communication received at the node to the network address of the node;

- route the communication to a parent node if the subset of the destination address corresponding to the hierarchical level of the network address of the node does not match the subset of that hierarchical level of the network address of the node;

- receive the communication for service at the node if the destination address matches the network address of the node; and

- route the communication to a child node if the destination node address of the hierarchical level of the node and all higher hierarchical levels matches the subset of the network address of the node and further includes significant lower level address fields, the child node to which the communication is routed having a subset network address one hierarchical level below the level of the current node matching the destination address.

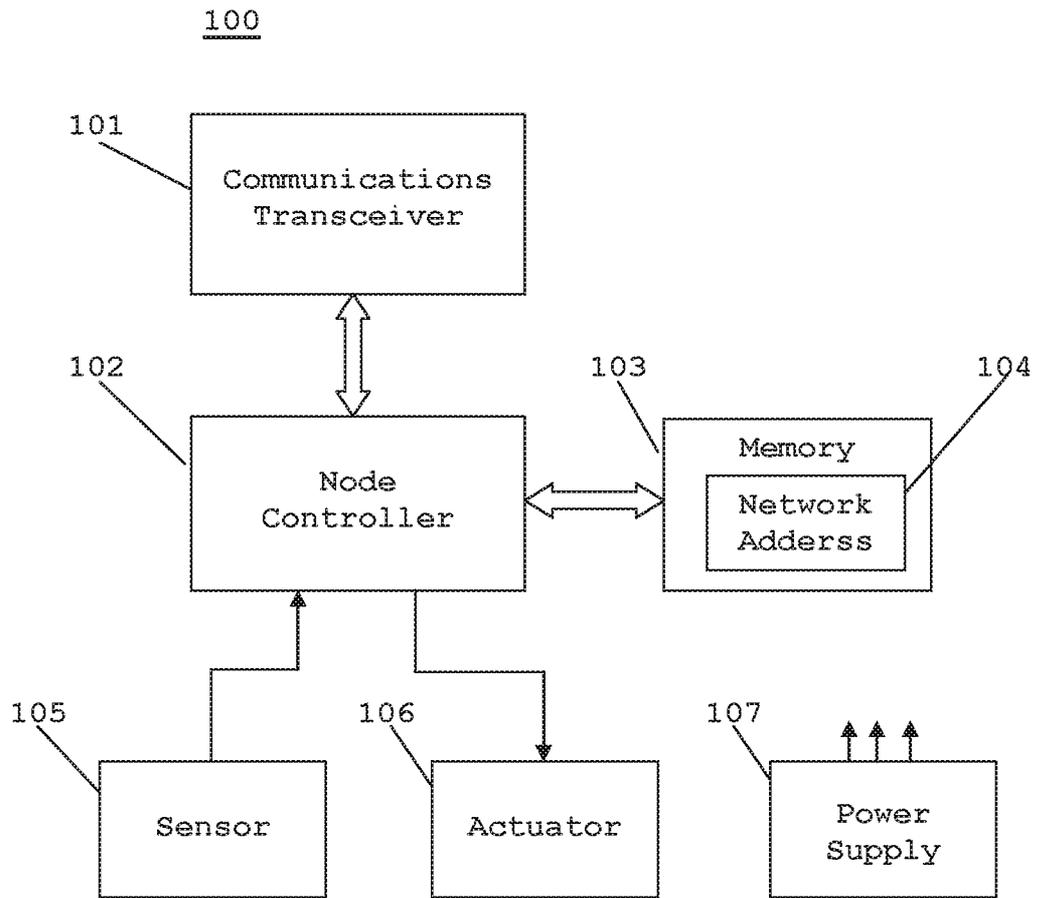


FIG. 1
(Prior Art)

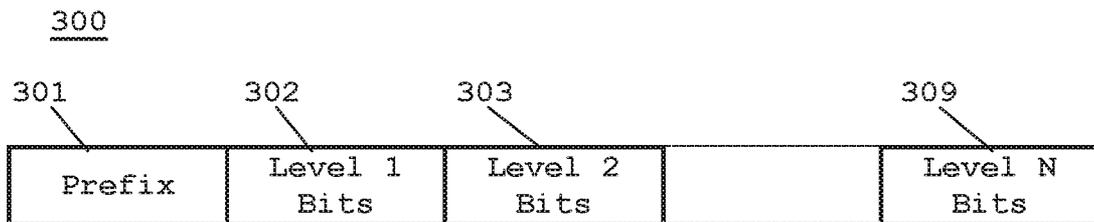


FIG. 3
(Prior Art)

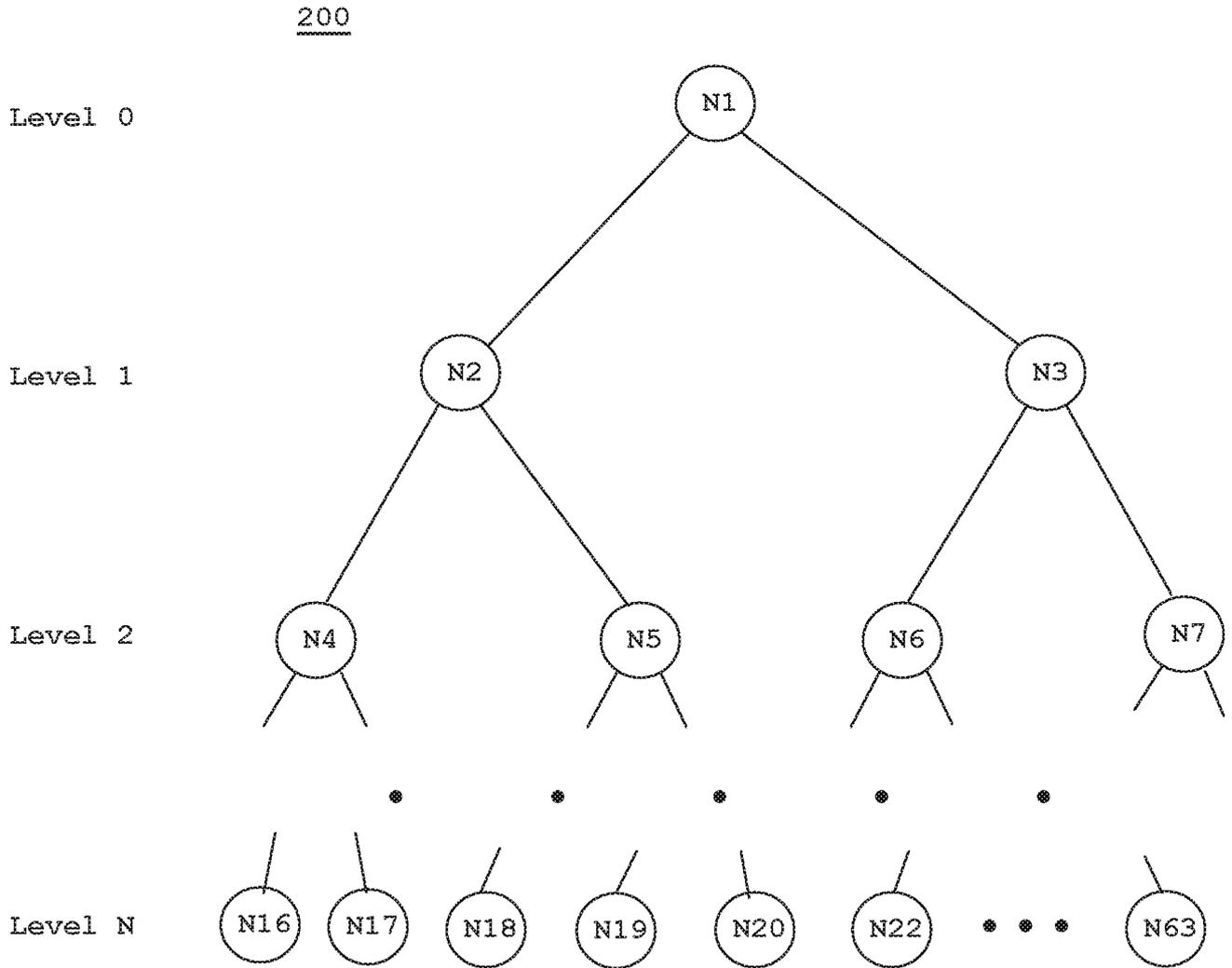


FIG. 2
(Prior Art)

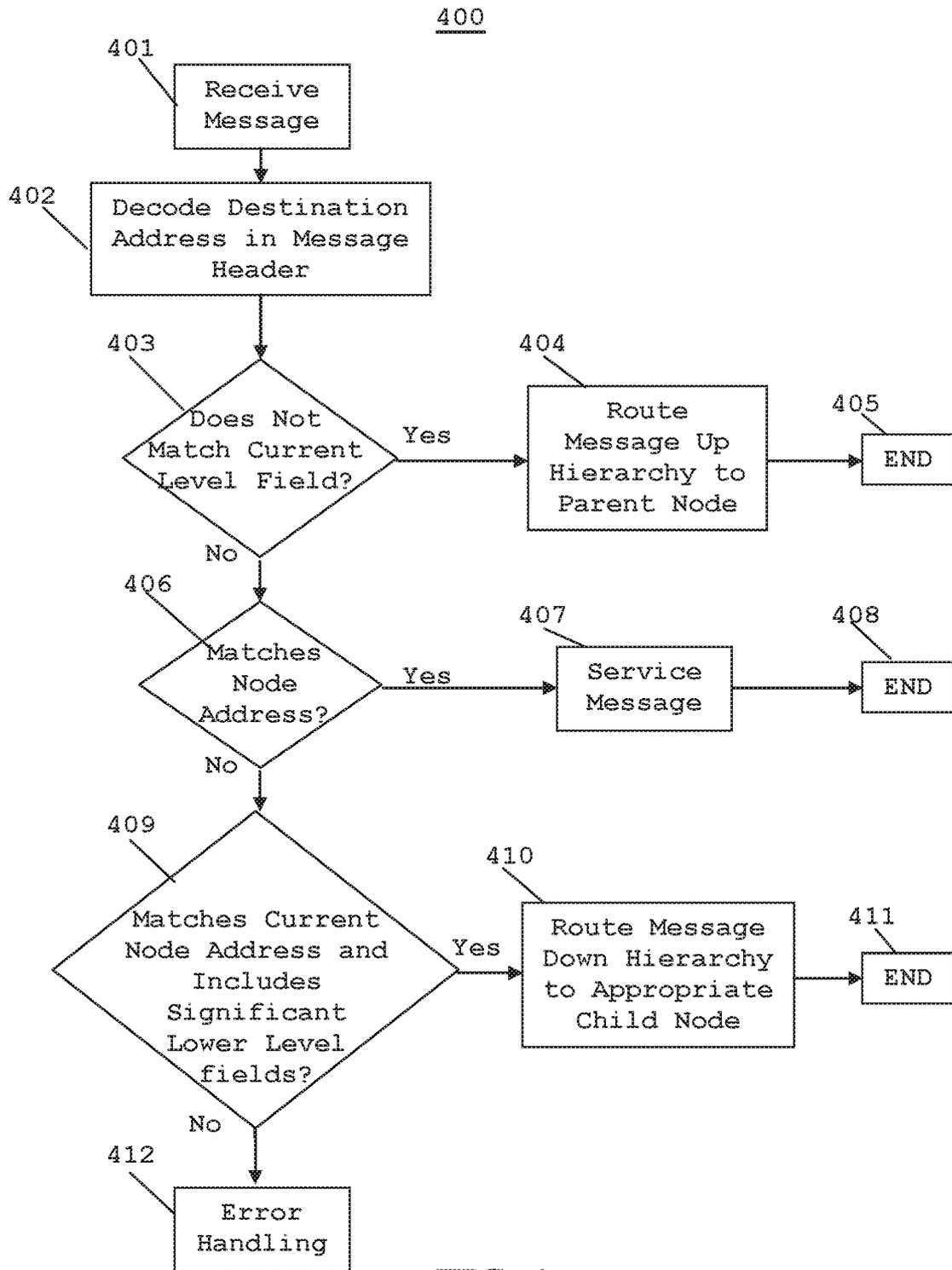


FIG. 4

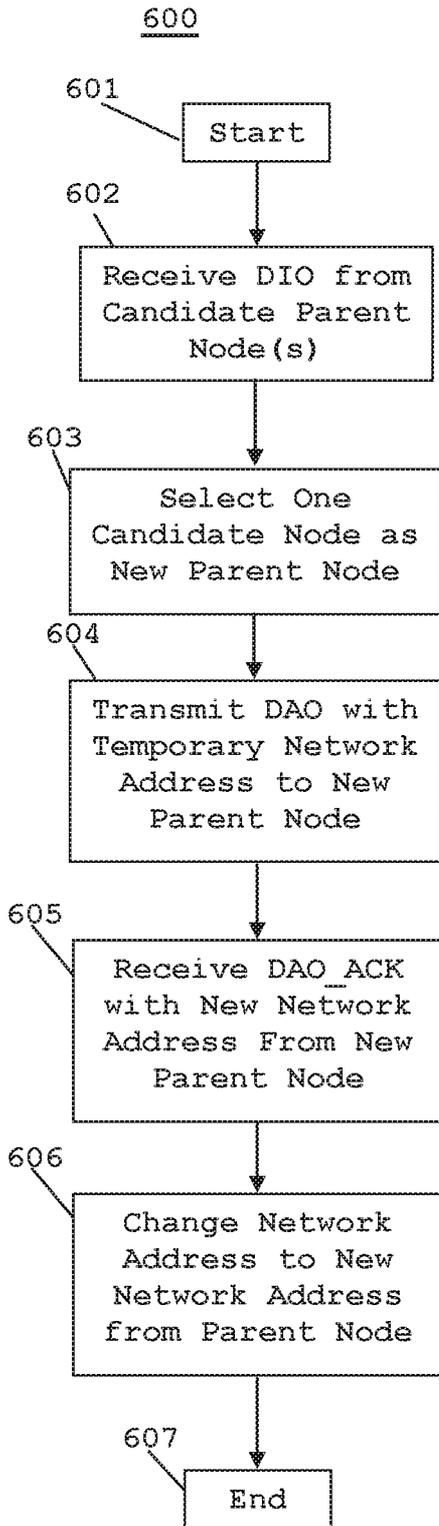


FIG. 6

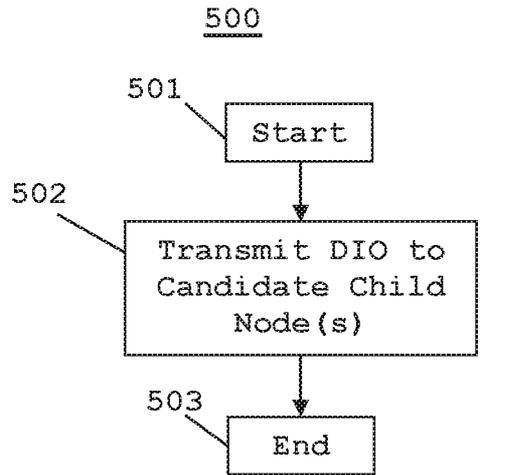


FIG. 5

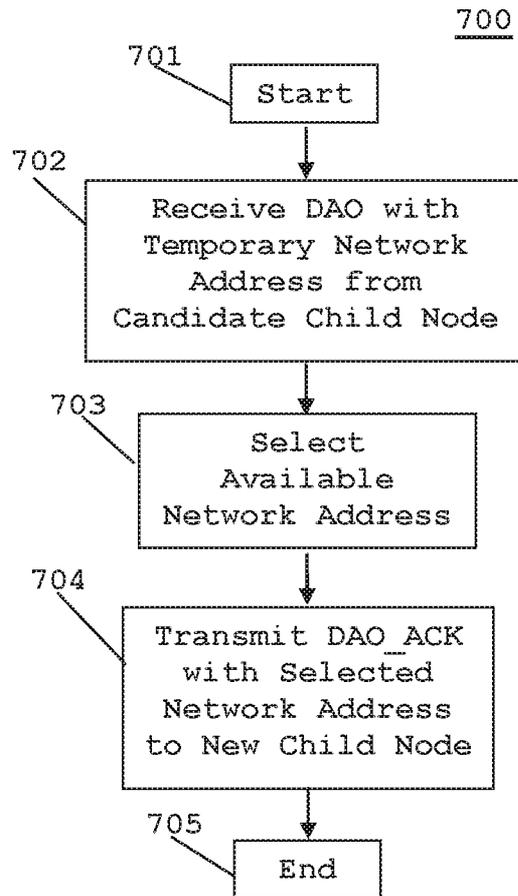


FIG. 7

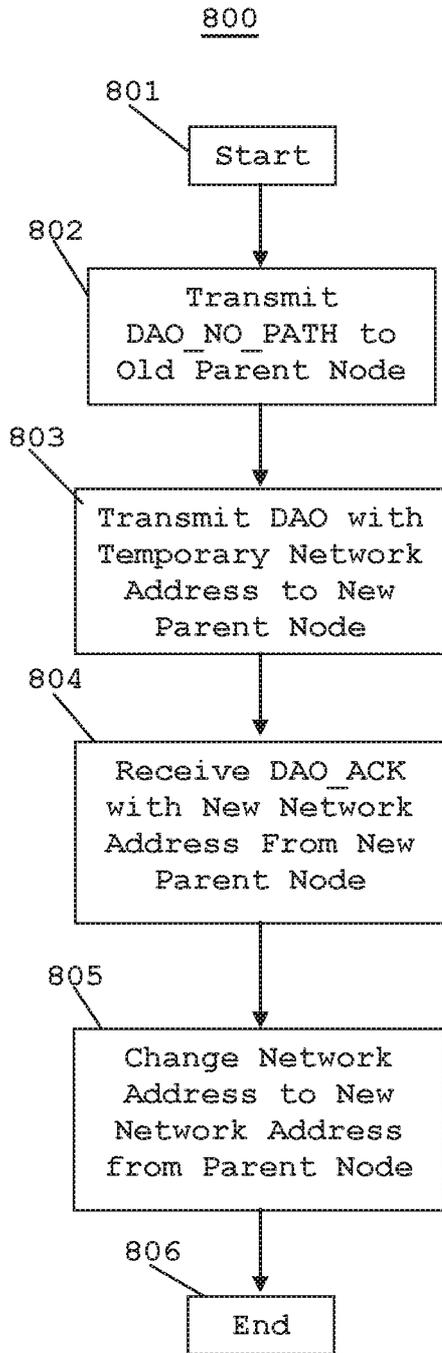


FIG. 8

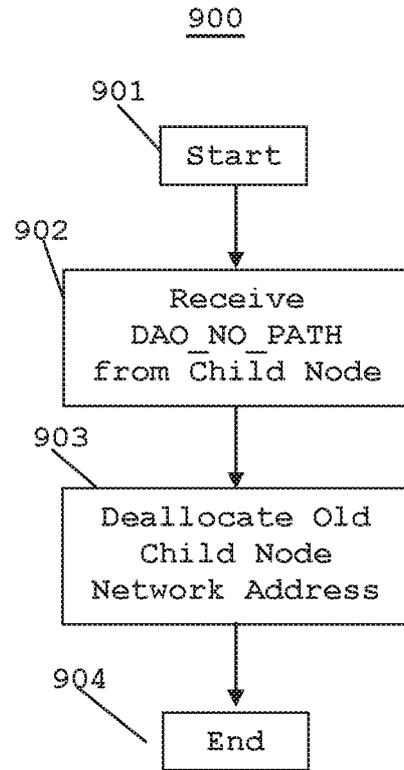


FIG. 9

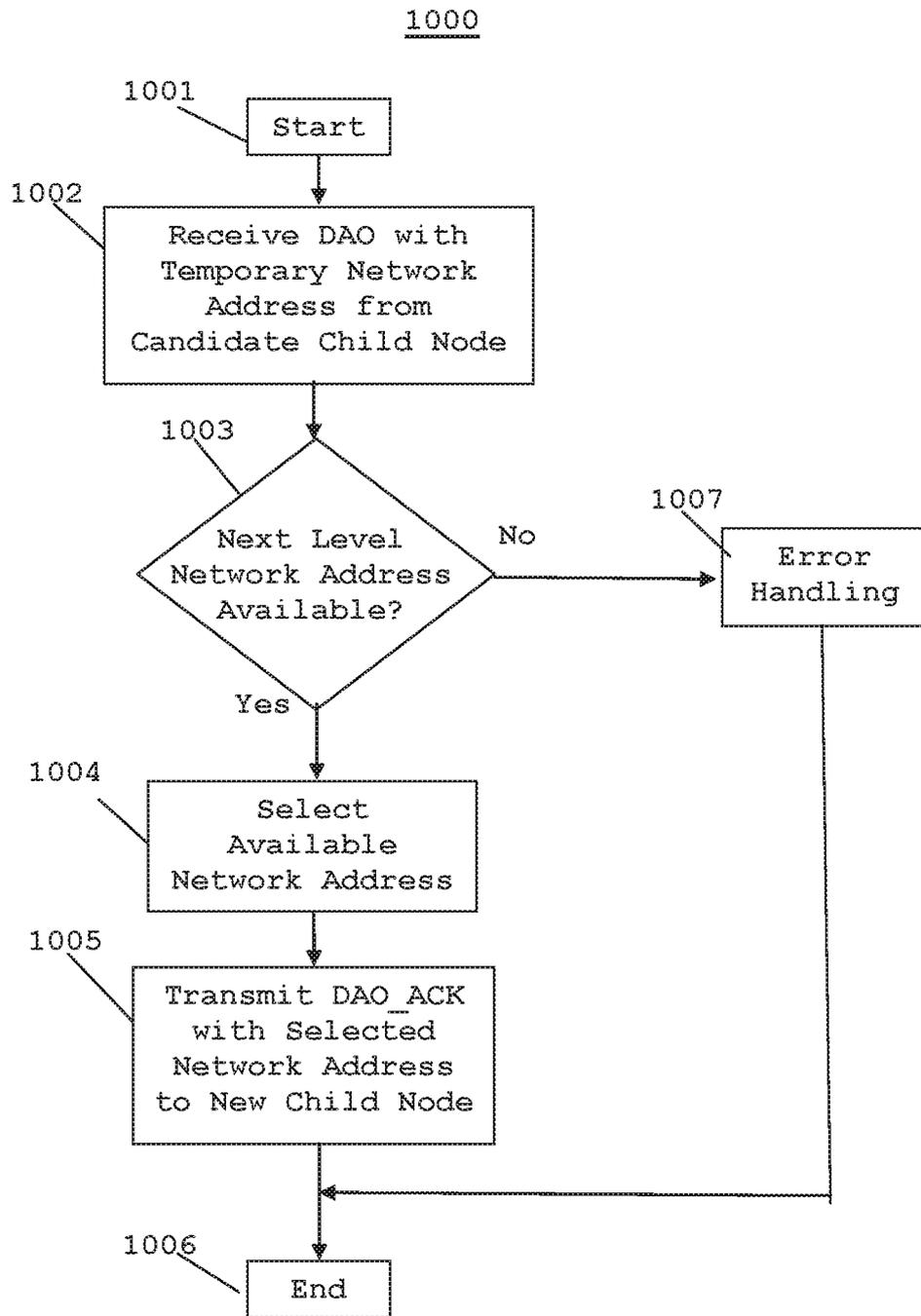


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/049315

A. CLASSIFICATION OF SUBJECT MATTER		
H04L 12/715 (2013.01) H04L 12/761 (2013.01)		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H04L 1/00, 1/02, 1/16, 1/18, 12/00, 12/02, 12/16, 12/18, 12/70, 12/701, 12/715, 12/751, 12/753, 12/761, G06F 11/00, 11/07, 11/14, 15/00, 15/16, 15/177		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/0228788 A1 (CISCO TECHNOLOGY, INC.) 22.09.2011, paragraphs [0021], [0023], [0027], [0028], [0039], [0043]-[0045], [0051], [0052]	1-12
A	WO 2013/131867 A1 (COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES) 12.09.2013, p. 18, lines 24-29	1-12
A	WO 2012/083134 A1 (CISCO TECHNOLOGY, INC.) 21.06.2012	1-12
A	US 2012/0117208 A1 (CISCO TECHNOLOGY, INC.) 10.05.2012	1-12
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
*	Special categories of cited documents:	"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
"A"	document defining the general state of the art which is not considered to be of particular relevance	
"E"	earlier document but published on or after the international filing date	
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	
"O"	document referring to an oral disclosure, use, exhibition or other means	
"P"	document published prior to the international filing date but later than the priority date claimed	
Date of the actual completion of the international search		Date of mailing of the international search report
17 October 2016 (17.10.2016)		17 November 2016 (17.11.2016)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer P. Volkov Telephone No. (495) 531-64-81