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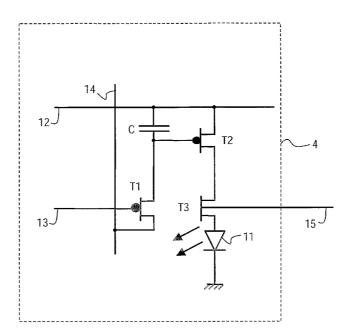
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#### **Declaration under Rule 4.17:**

as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ,

[Continued on next page]

(54) Title: ELECTROLUMINESCENT DISPLAY DEVICE WITH DUTY CYCLE CONTROL



(57) Abstract: The display device comprises a display panel (2) having a plurality of display pixels (4) with emissive display elements (11). The display device further comprises duty cycle control means (15, T3) for varying a fraction of the frame period during which the display pixels (4) emit light in dependence on an overall brightness level of an image to be displayed on the display panel. In order to vary the duty cycle a switch, e.g. a power transistor (T3) is connected between the drive transistor (T2) and the light emitting element (11) of each pixel (4) each pixel in a row may be connected to a single duty cycle select line (15).



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IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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ELECTROLUMINESCENT DISPLAY DEVICE WITH DUTY CYCLE CONTROL

The invention relates to a display device comprising a display panel having a plurality of display pixels with emissive display elements, an integrated circuit and a method for controlling such a display.

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Although new display technologies rapidly emerge, people are still used to cathode ray tube (CRT) displays as e.g. employed for conventional TV-sets or monitors. One of the effects people are familiar with and appreciate in CRT displays is the 'sparkling effect' or 'peak white', i.e. the effect of more brightness for bright areas in otherwise dim images. In a CRT display this effect occurs by the electron gun providing more beam current (and hence more brightness) if only a part of the display shows a bright area. Indeed if the electron gun provides a large bright area, the beam current of the electron gun has to be limited resulting in a reduction of the brightness. However, if only a small area is bright in an otherwise dark scene, there is no need for limiting the beam current.

electroluminescent light emitting elements deposited on or over a substrate, are becoming increasingly popular. These light emitting elements may be light emitting diodes (LED's), incorporated in or forming display pixels that are arranged in a matrix of rows and columns. The materials employed in such LED's are suitable to generate light if a current is driven through these materials, such as particular polymeric (PLED) or small molecule organic

(SMOLED) materials. Accordingly the LED's have to be arranged such that current can flow

Display devices employing display elements, such as emissive display

through these light emitting materials.

Typically passively and actively driven matrix displays are distinguished. For active matrix PLED (AMPLED) displays, the display pixels themselves comprise active circuitry such as one or more transistors. This active circuitry generates the current driven through the PLED material to generate or emit light. Such a display is addressed row at a time and the light emitting elements emit light during the remainder of the frame period. It is a disadvantage that new display technologies lack the sparkling effect of CRT-displays.

It is therefore an object of the invention to provide a display device comprising a plurality of display pixels having emissive display elements that is adapted to generate the sparkling effect. The invention is defined by the independent claims. The dependent claims define advantageous embodiments.

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The object is achieved by providing a display device that comprises a display panel having a plurality of display pixels with emissive display elements and duty cycle control means for varying a fraction of a frame period during which said display pixels emit light in dependence on an overall brightness level of an image to be displayed on said display panel. By determining the overall brightness level for each frame period, the occurrence of a dim frame is detected and as a result the effective brightness of the display pixels in the dim frame can be boosted by increasing the fraction of the frame period during which the display pixels emit light. When the overall brightness level is high, the effective brightness of the display pixels can be dimmed by decreasing the fraction of the frame period during which the display pixels emit light. Consequently the sparkling effect can be obtained for the dim frames. Furthermore the power consumption of the display device is reduced for images with high overall brightness levels. Also, the range of available grey scale levels is not influenced by varying the above indicated fraction.

In an embodiment of the invention the display device comprises a a frame memory for storing input signals, representing said image, during a frame period for enabling a determination of the overall brightness level of the image during the frame period. This memory provides the possibility to determine the overall brightness level per frame or per set of frames. The frame memory allows to store the input signals for one frame period before providing the signals to the display panel. During this frame period the overall brightness level of the image corresponding to this frame may be determined. Based on this overall brightness level the fraction can be determined which should be applied during this frame period.

The device may further comprise a look up table for determining the fraction corresponding with the determined overall brightness level. This look-up table may contain data relating to the appropriate fraction for a particular overall brightness level for a frame.

In an embodiment of the invention the display pixels comprise a switch coupled to said control means for enabling light emission by said corresponding emissive display element for said fraction of said frame period. Such a switch preferably comprises a

transistor connected in series to the electroluminescent element such that the current flow through the electroluminescent elements can be controlled by means of the transistor.

The invention further relates to a method for controlling a display panel having a plurality of display pixels with emissive display elements comprising the steps of:

- determining an overall brightness level of an image to be displayed in a frame period on said display, and
  - controlling a fraction of said frame period during which said display pixels (4) emit light in dependence on said overall brightness level.

US 5,451,979 discloses a display sign comprising a plurality of lights that are separately energized to produce an image. The display sign comprises a processor for controlling the duration of a duty cycle for energizing said lights. The processor includes means for determining the number of lights to be energized and means for reducing the duty cycle when the number of lights drops below a determined number. The display sign is neither arranged nor has as a purpose to cause the sparkling effect as the processor does not determine the overall brightness level for a frame, thus lacking the means for detecting a dim frame.

The non-prepublished patent application GB 0220512 ("Electroluminescent display devices") of the applicant describes an active matrix electroluminescent display device comprising means for determining an overall brightness level of an image to be displayed in a frame period and means for controlling a drive transistor in dependence on a respective input signal providing a drive level for a display pixel and in dependence on the overall brightness level. According to the present invention the drive transistor is not controlled by the control means.

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The invention will be further illustrated with reference to the attached drawings, in which:

Fig. 1 shows a display device according to an embodiment of the invention; and

Fig. 2 shows a display pixel according to an embodiment of the invention.

Fig. 1 shows a schematic illustration of a display device 3. The display device 3 comprises the PLED display panel 2 having a plurality of display pixels 4 arranged in a

matrix of rows and columns. It should be appreciated that Fig. 1 shows only a few display pixels 4. In practice there may be several hundreds of rows and columns with display pixels 4.

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The display device 3 further comprises a driver circuitry arrangement 5 for addressing and data provision of the individual display pixels 4. The driver circuitry arrangement 5 comprises a data-input 6 for receiving a signal representing a video image to be displayed on the display panel 2. The image load or overall brightness level of the image received at the data-input 6 is determined by duty cycle control means 7. The control means 7 may consist of an adder 10, a memory 8, a loop-up table 9, herein after-also called a LUT, and other logic circuitry (not shown). Alternatively the control means may be a processor with associated memory and software performing the functions of adding, storing and other logic functions. The control means 7 may also comprise a combination of hardware and software to perform the mentioned functions, or be completely realized by software. The adder adds the values of the grey levels of each display pixel 4 for a frame. The total of the values of the grey levels may be stored in the memory and used as a measure of the image load for the display pixels 4 for that particular frame. Alternatively an average value of the values of the grey levels of the pixels 4 within a frame may be used as the measure of the image load.

Alternatively, if the color components red R, green G and blue B of the video image are available, the luminance values of these signals may be added.

As a further alternatively, the total luminance value of each of the color components may be determined.

A combination of the respective total luminance value of the color components may be used to represent the image load.

In the example of Fig. 1, the memory 3 comprises the total of the values of the grey levels for a current frame being displayed.

The LUT 9 comprises a list of duty cycle values to be selected as function of the total of the grey level values. The duty cycle is defined as a percentage, indicating the fraction of the frame period of the input signal, during which a display pixel 4 is driven to emit light.

Below an example of the contents of a LUT 9 is depicted for use with a display panel 2 providing a nominal brightness of 100% at a duty cycle of 50%.

OBV (%)	DC (%)	EPB (%)	
100	35	70	
90	35	70	
80	35	70	-
70	35	70	
60	35	70	*
50	40	80	
40	45	90	
30	50	100	
20	55	110	
15	60	120	
10	65	130	
5	75	150	

TABLE 1

Table 1 illustrates that when the video image has an overall brightness level (OBV) of 5%, the duty cycle (DC) is increased to 75% via the driver circuitry arrangement 5 by control means 7 of the display device 3. This results in a boost by a factor 1.5 of the effective pixel brightness (EPB) compared to the nominal brightness. Thus the peak brightness is substantially increased for video images having a relatively low overall brightness level. This provides the desired sparkling effect.

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The control means 7 may determine the image load and the corresponding duty cycle of a current frame of the video image while the image load and the corresponding duty cycle of a previous frame is used to display the current video image.

Alternatively a frame memory (not shown) may be applied to delay the video image with a frame period prior to supplying the video image received at the data input 6 to the drive circuitry arrangement 5. This enables the control means 7 to determine the duty cycle to be applied to a current frame prior to displaying this current frame.

The increase of the duty cycle may induce sample/hold artifacts for the display panel 2. Sample/hold artefacts arise from the fact that in every frame period, a new image may be displayed at the start of the frame period (sample), whilst in remainder of the frame period (typically 16msec for 60Hz operation) the image remains visible on the screen (hold). For moving video images, the eye tries to follow the image across the screen of the display

panel 2, whilst, due to the sample/hold nature of the addressing, the image is physically stationary. The user interprets this effect as a blurred image. However, users generally prefer the sparkling effect over moving image quality. Furthermore, when the duty cycle has low values (e.g. DC<50%) a small increase of the duty cycle will result in a large brightness increase without increasing the motion blurring effect noticeably.

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The display device may be a display module for incorporating in a display product. The display device may also be a product like a television set, monitor, personal digital assistant, camera, computer, phone or any other product having a display screen. Such a product includes next to the display module also a housing and other features like, for example, controls and a power supply.

Fig. 2 shows an example of a display pixel 4 arranged to enable control of the duty cycle. The display pixel 4 is a voltage controlled display pixel comprising an addressing transistor T1, a storage capacitor C and a drive transistor T2 for driving an electroluminescent display element 11. T2 may be a p-Si thin film transistor (TFT) and light emitting element 11 may be a light emitting diode, such as a polymer or small molecule OLED. One of the plates of the capacitor C and the source electrode of T2 are connected to a voltage supply line 12. Addressing of the display pixel 4 is performed via line 13, while the data received via the data-input 6 is transmitted via data line 14.

It is noted that the duty cycle may be varied in various ways. In a preferred embodiment a switch T3, such as a power transistor, is applied. The switch T3 can be addressed over a duty cycle select line 15 that is controlled by the control means 7. Thus, in operation, the control means 7 determine the overall brightness level for a particular frame and vary the duty cycle in dependence on the determined overall brightness level, for example, according to the LUT 9, via the duty cycle select line 15. The switches T3 of each display pixel 4 in a row may be connected to a single duty cycle select line 15, such that all display pixels 4 of a particular row are subject to the same duty cycle. Two or more select line 15 may be combined in groups of select lines 15 in order to reduce the number of connections to be made to the display panel 2.

The invention is not restricted to the above described embodiments which can be varied in a number of ways within the scope of the claims, e.g. by arranging the switch T3 between the display element 11 and ground. Several different display pixels 4 can be envisaged incorporating the invention. The invention can also be applied to other matrix displays that are driven with a duty cycle and have emissive display elements like active matrix field emission displays.

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It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. Use of the verb "comprise" and its conjugations does not exclude the presence of elements or steps other than those stated in a claim. The article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention may be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means may be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

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### **CLAIMS:**

- 1. Display device (3) comprising a display panel (2) having a plurality of display pixels (4) with emissive display elements (11); and duty cycle control means (7) for varying a fraction of a frame period during which said display pixels (4) emit light in dependence on an overall brightness level of an image to be displayed on said display panel (2).
- 2. Display device (3) according to claim 1, wherein said control means (7) are adapted to increase said fraction if a decrease of said overall brightness level is determined.
- Display device (3) according to claim 1 wherein said control means (7) are adapted to decrease said fraction if an increase of said overall brightness level is determined.
  - 4. Display device (3) according to claim 1, further comprising a frame memory for storing input signals, representing said image, during a frame period for enabling a determination of the overall brightness level of the image during the frame period.
  - 5. Display device (3) according to claim 1, wherein the control means (7) are adapted to determine the fraction of the frame period in dependence on the overall brightness level of the image during a previous frame period.

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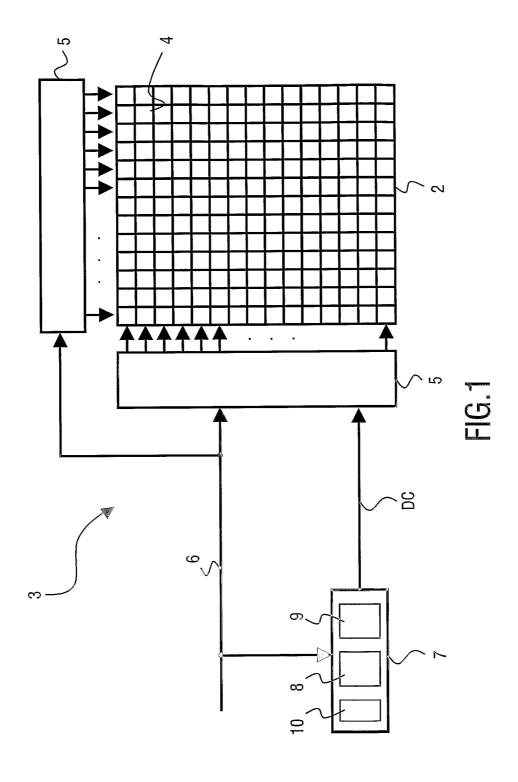
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- 6. Display device (3) according to claim 1, wherein the control means (7) further comprise a look-up table (9) for determining said fraction corresponding with said determined overall brightness level.
- 7. Display device (3) according to claim 1, wherein said display pixels (4) comprise a switch (T3) coupled to said control means (7) for enabling light emission by said corresponding emissive display element (11) for said fraction of said frame period.

- 8. Method for controlling a display panel (2) having a plurality of display pixels (4) with emissive display elements (11) comprising the steps of:
- determining an overall brightness level of an image to be displayed in a frame period on said display, and
- 5 controlling a fraction of said frame period during which said display pixels (4) emit light in dependence on said overall brightness level.
- 9. Integrated circuit for controlling a display panel (2) having a plurality of display pixels (4) with emissive display elements (11), the integrated circuit comprising a duty cycle control arrangement (7) for varying a fraction of a frame period during which said display pixels (4) emit light in dependence on an overall brightness level of an image to be displayed on said display panel (2).

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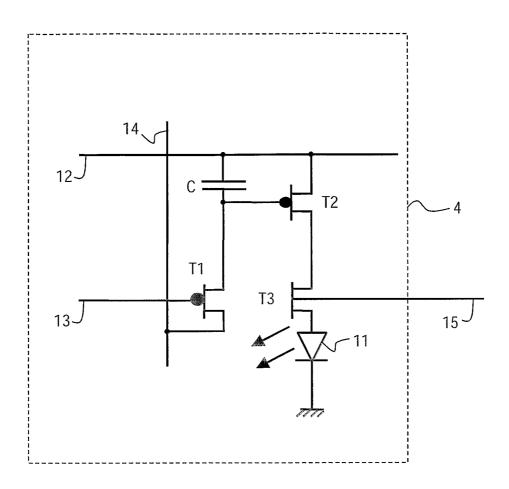


FIG.2

# INTERNATIONAL SEARCH REPORT

International Application No

A. CLASSI IPC 7	G09G3/32		
According to	International Patent Classification (IPC) or to both national classification	ation and IPC	
B. FIELDS			<u></u>
IPC 7	cumentation searched (classification system followed by classification $6096$	on symbols)	
Documentat	on searched other than minimum documentation to the extent that s	uch documents are included in the fields se	arched
	ata base consulted during the international search (name of data base	se and, where practical, search terms used	
EPO-In	cernal		
C. DOCUME	NTS CONSIDERED TO BE RELEVANT	· · · · · · · · · · · · · · · · · · ·	
Category °	Citation of document, with indication, where appropriate, of the rele	evant passages	Relevant to claim No.
χ	US 5 757 343 A (NAGAKUBO TETSURO) 26 May 1998 (1998-05-26)		1-6,8,9
Υ	column 2, line 4 - column 2, line	60;	7
	figures 1,2,3a,3b column 5, line 57 - column 6, lin	19٠ م	
	figure 7		
	column 8, line 61 - column 10, li figure 10	ne 7;	
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	er documents are listed in the continuation of box C.	Y Patent family members are listed in	a appey
		Patent family members are listed in	raimex.
-,	egories of cited documents:  nt defining the general state of the art which is not	"T" later document published after the inter or priority date and not in conflict with	the application but
consid	ered to be of particular relevance	cited to understand the principle or the invention	,,
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which i citation	s cited to establish the publication date of another or other special reason (as specified)	"Y" document of particular relevance; the cl cannot be considered to involve an inv	entive step when the
other n		document is combined with one or mo ments, such combination being obviou in the art.	re other such docu- is to a person skilled
"P" docume later th	nt published prior to the international filing date but an the priority date claimed	*&" document member of the same patent f	amily
Date of the	ctual completion of the international search	Date of mailing of the international sear	ch report
20	5 October 2004	05/11/2004	
Name and n	ailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2	Authorized officer	
	NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,	Morris, D	ļ
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# **INTERNATIONAL SEARCH REPORT**

International Application No

C.(Continuation	) DOCUMENTS CONSIDERED TO BE RELEVANT	102004/ 031093	
	ation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	
	HONG Y ET AL: "NOVEL POLY-SI TFT PIXEL ELECTRODE CIRCUITS AND CURRENT PROGRAMMED ACTIVE-MATRIX DRIVING METHODS FOR AM-OLEDS" 2002 SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS. BOSTON, MA, MAY 21 - 23, 2002, SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, SAN JOSE, CA: SID, US, vol. Vol. 33 / 1, 21 May 2002 (2002-05-21), pages 618-621, XP001134284 page 619, right-hand column, paragraph 1 - page 621, right-hand column, paragraph 2; figures 2,3	7	
	US 5 451 979 A (LEVAC RONALD A) 19 September 1995 (1995-09-19) column 1, line 49 - column 1, line 61 column 3, line 52 - column 4, line 13; figures 2a,2b column 4, line 53 - column 5, line 17; figure 4	1-9	
	US 2003/063078 A1 (HANARI JUN ET AL) 3 April 2003 (2003-04-03) paragraph '0048! - paragraph '0055!; figures 1-4 paragraph '0060! - paragraph '0061!; figure 7 paragraph '0069! - paragraph '0076!; figures 12-14 paragraph '0092! - paragraph '0101!; figures 18-21,22a-22c paragraph '0112! - paragraph '0114!	1-9	
	US 2003/122759 A1 (ABE NAOTO ET AL) 3 July 2003 (2003-07-03) paragraph '0312! - paragraph '0321!; figures 14,20a,20b paragraph '0472! - paragraph '0487!; figure 26	1-9	

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No IB2004/051093

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 5757343	A	26-05-1998	JP	8286636 A	01-11-1996
US 5451979	Α	19-09-1995	NONE		
US 2003063078	A1	03-04-2003	JP JP TW	2003108073 A 2003108075 A 574529 B	11-04-2003 11-04-2003 01-02-2004
US 2003122759	A1	03-07-2003	CN JP	1424707 A 2003255884 A	18-06-2003 10-09-2003