

Nov. 6, 1962

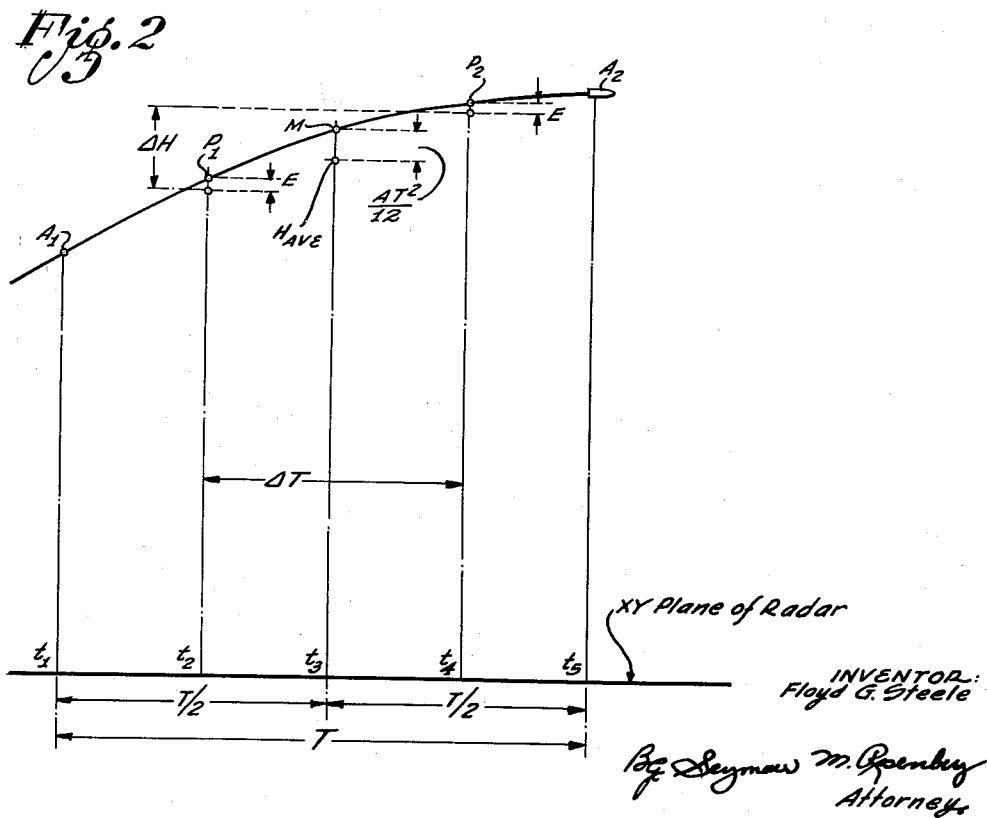
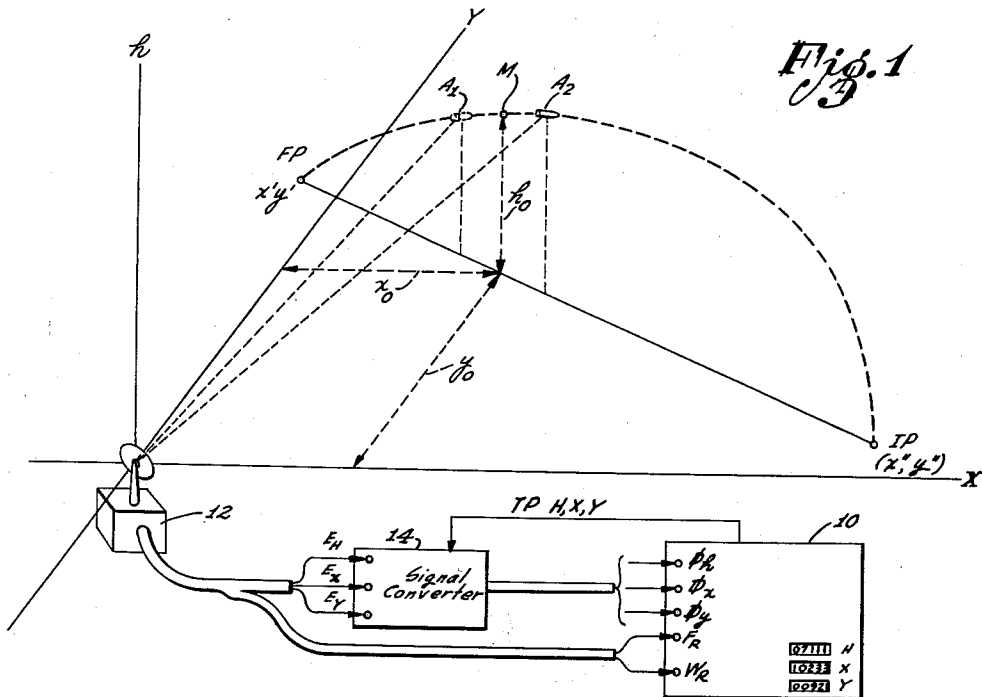
F. G. STEELE

3,063,047

FIRING POINT LOCATOR SYSTEM

Filed Jan. 23, 1957

6 Sheets-Sheet 1



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FIRING POINT LOCATOR SYSTEM

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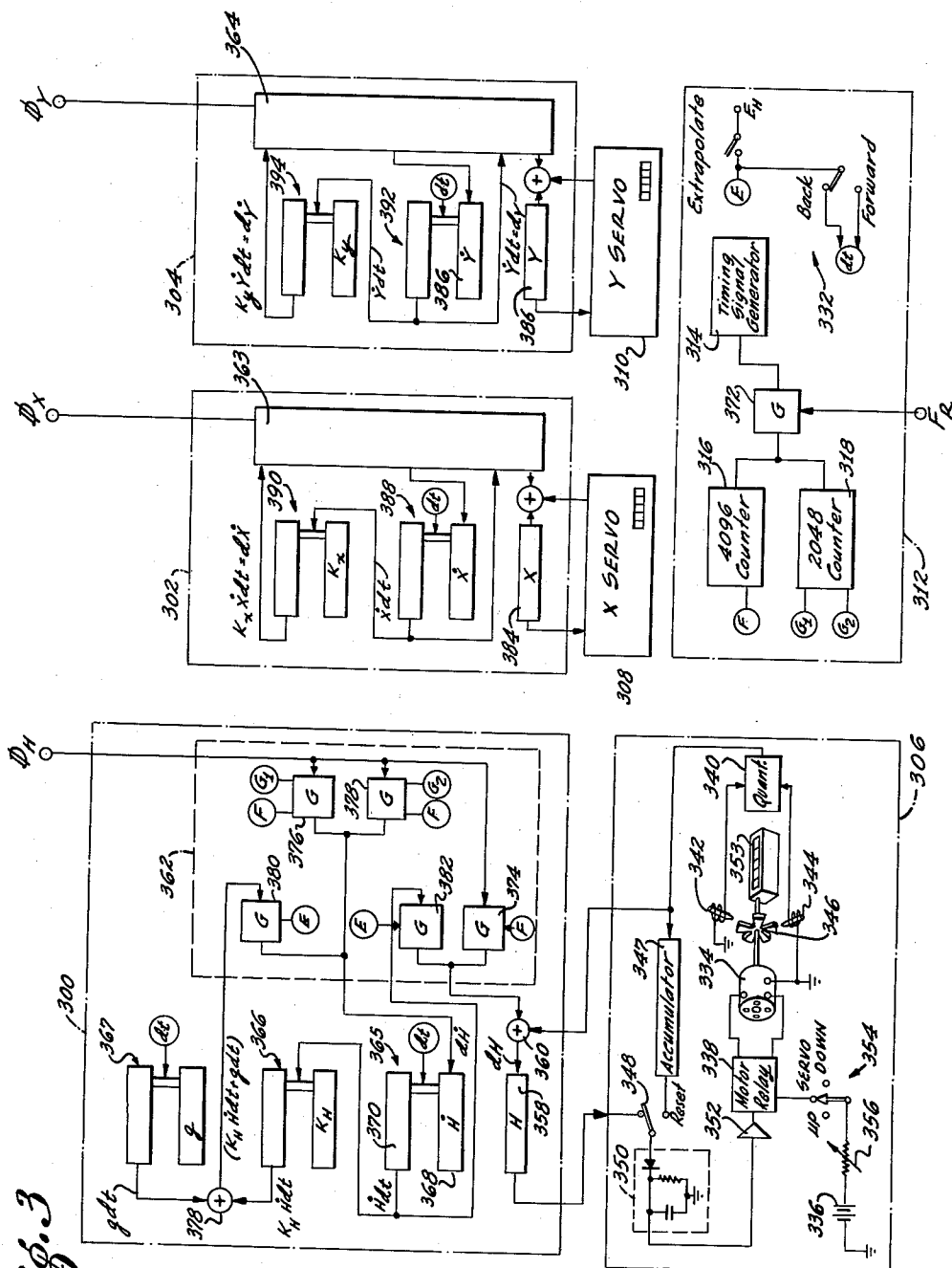


Fig. 3

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Fig. 4

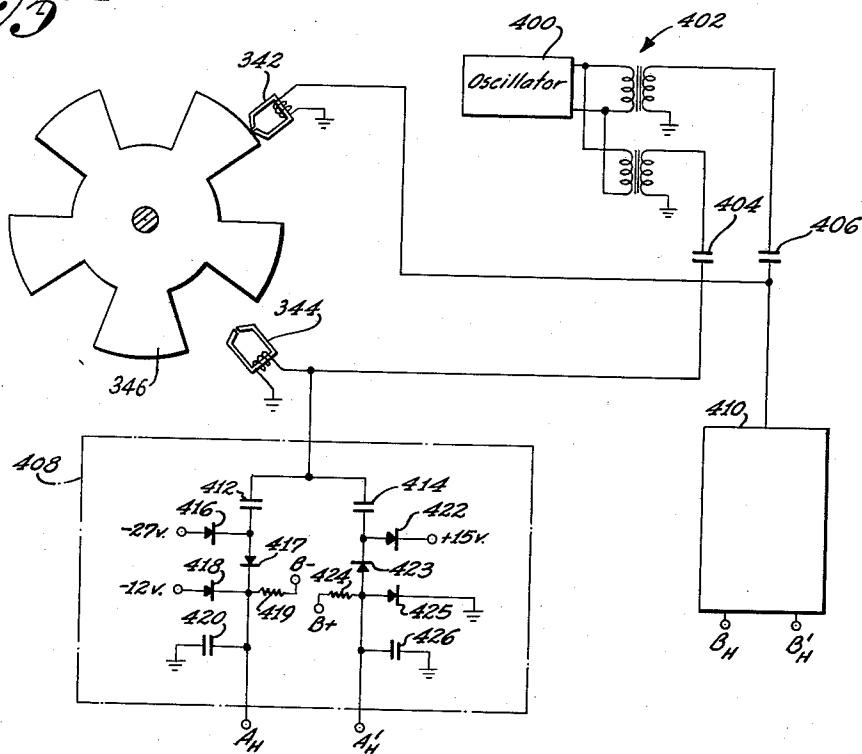


Fig. 5a

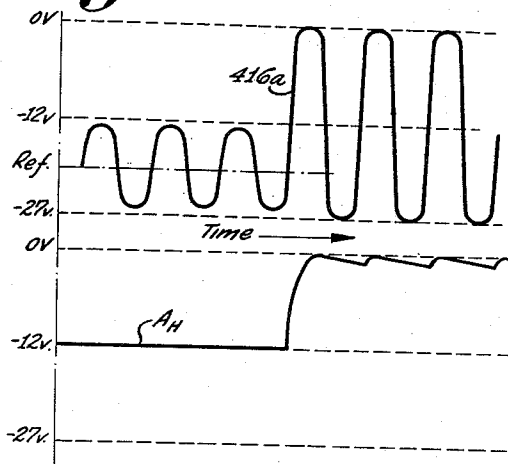
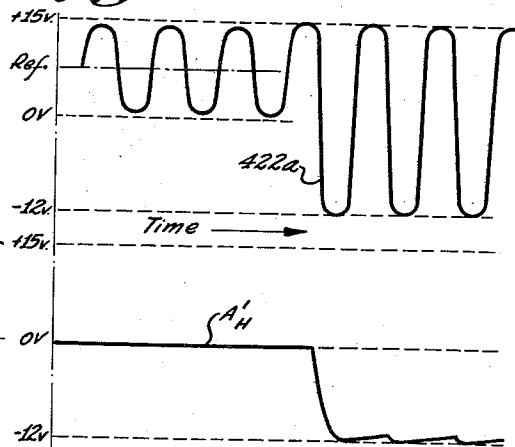


Fig. 5b



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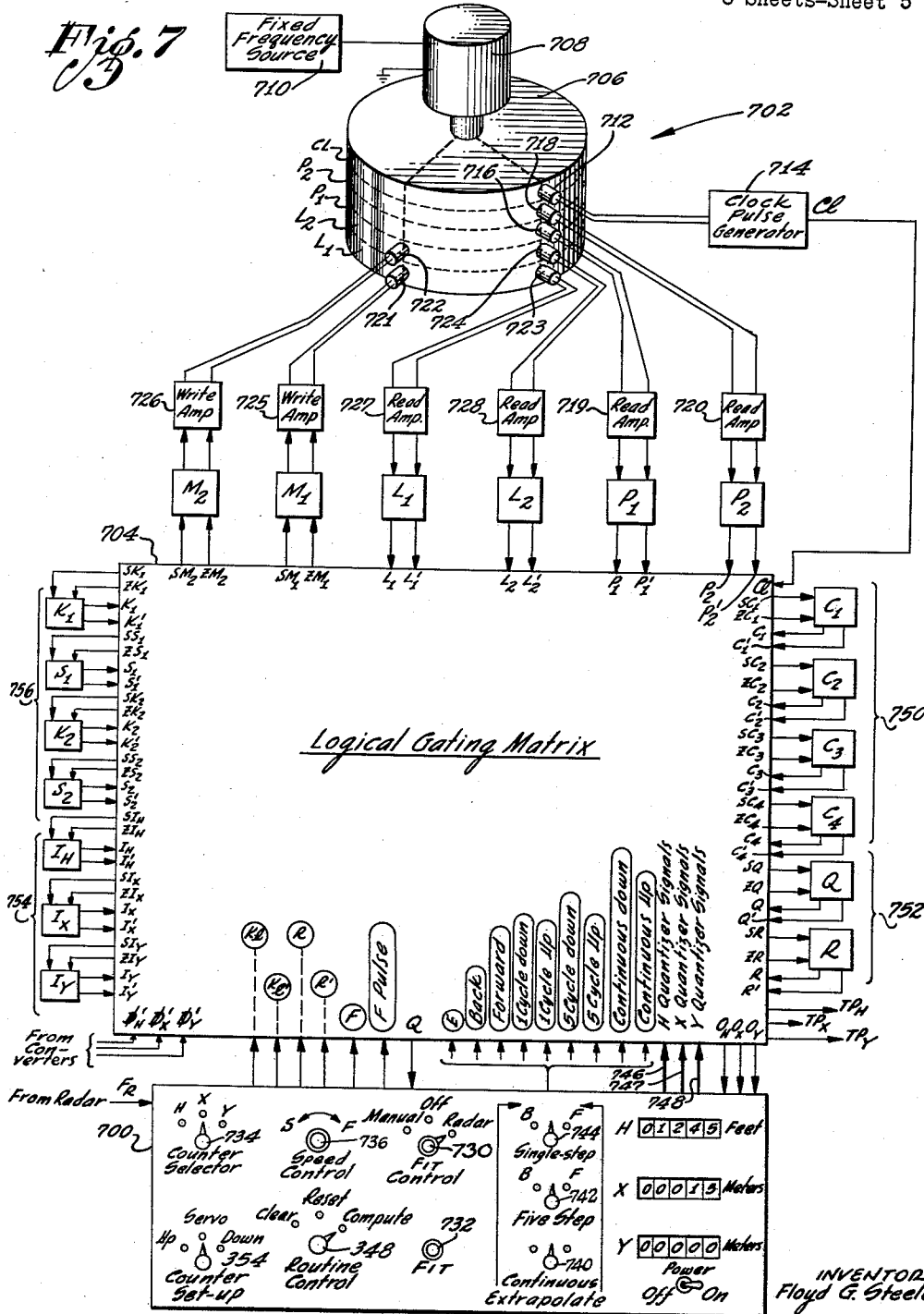
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Filed Jan. 23, 1957

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Fig. 7



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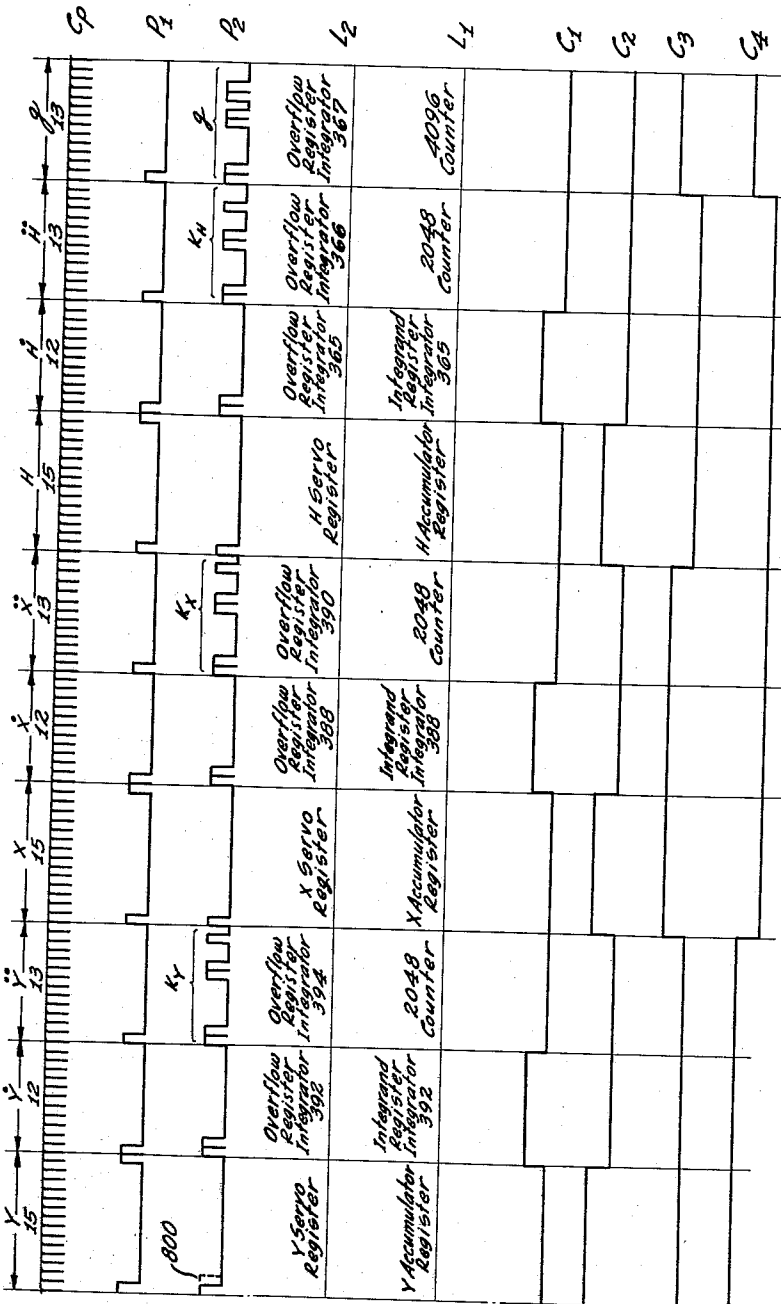
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FIRING POINT LOCATOR SYSTEM

Filed Jan. 23, 1957

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Fig. 8
C3



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FIRING POINT LOCATOR SYSTEM

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Filed Jan. 23, 1957, Ser. No. 635,916
28 Claims. (Cl. 343-7)

This invention relates to a firing point locator system for determining the firing point of a projectile, and more particularly to a firing point locator system which utilizes a digital computer for determining the position and velocity of a projectile at a point on its trajectory, and which is thereafter operable to iteratively extrapolate the trajectory equations of the projectile to determine the firing point thereof.

It has long been recognized that the effectiveness of artillery and mortar fire would be sharply reduced if there was some manner to accurately and rapidly locate the firing point of the projectiles fired thereby. Following the development of accurate tracking radars which are capable of tracking a projectile through at least a portion of its trajectory, various attempts have been made to construct firing point locators by utilizing the data produced by the radar during its tracking mode to simulate the earlier portion of the trajectory and thereby indicate the projectile's firing point.

One of the first firing point locator systems suggested in the prior art included a plotting board which was utilized to plot the trajectory of a projectile while it was being tracked, after which the operator manually extrapolated the curve backward to indicate the projectile's firing point. The principal disadvantage of this system is that it is subject to human error and produces results which are grossly inaccurate when compared with the degree of accuracy necessary to reasonably insure subsequent destruction of the enemy weapon by friendly fire.

In still other prior art firing point locator systems analog computing elements have been utilized which are responsive to the intelligence data produced by the radar for predicting the location of the firing point by extrapolating simplified equations which roughly define the ballistics of the projectile. One example of this type of prior art system is disclosed in U.S. Patent 2,761,129, issued August 28, 1956, to E. G. Hills for "Apparatus for Locating a Missile Projecting Device," wherein a trigonometric solution of a missile's trajectory in a polar coordinate system is utilized to present the approximate firing point location on an associated plotting board, the solution of the trajectory equations being accomplished through the addition of analog signals representative of position and the time rate of change of position.

Although analog systems which operate in the foregoing or similar manner have been constructed and tested, their utility is inherently restricted by several important factors. Firstly, the accuracy provided by these systems is frequently inferior to that provided by the manual plotting method described previously owing to the fact that the error contributed by each analog element in the system, when compounded with the errors contributed by the other elements, produces an intolerable system error. In addition, the systems are extremely complex, bulky and expensive, and great care must be exercised in adjusting the various analog elements to provide even a slight degree of accuracy and reliability.

The present invention, on the other hand, overcomes the above and other disadvantages of the prior art firing point locator systems by providing a system in which a digital computer is utilized to determine first the position and velocity of a projectile at a point on its trajectory, and which is thereafter operable to iteratively extrapolate the trajectory equations of the projectile to determine the firing point thereof. In accordance with the basic con-

cept of the present invention, the firing point locator system herein disclosed comprises a radar operable to track a projectile through at least a portion of its trajectory to produce output signals representative of the instantaneous coordinate position of the projectile along each of the coordinates of a three dimensional coordinate system in space, an analog-to-digital converter for converting the radar output signals to electrical signals digitally representative of the position and time rate of change of position of the projectile at substantially the midpoint of a sampled portion of the projectile's trajectory, and an electronic digital computer operative to extrapolate the trajectory equations of the projectile utilizing as initial conditions the known position and velocity of the projectile at a point on its trajectory.

More specifically, in the preferred embodiment of the invention herein disclosed the analog-to-digital converter functions to generate three difunction signal trains corresponding to the X, Y and H coordinates of an orthogonal coordinate system and representative of the instantaneous position of the projectile as it is being tracked, each train including a predetermined number of sequential difunction signals. These signals are then applied to associated binary accumulators which function to determine the average coordinate position of the projectile during the interval through which the signals are generated, and which also function to determine the coordinate velocities of the projectile by differencing the average positions of the projectile during the first and second halves of the interval.

In order to most clearly comprehend the invention it should be here pointed out that the term difunction signal train refers to a train of signals each having a fixed period and having either a high level representing a first quantity or a low level representing a second quantity, the average values of the quantities represented by the signals occurring over a given interval corresponding to the average value of the physical quantity represented by the train during the given interval. For example, if it is assumed that the first and second quantities represented by the signals in a train are the maximum range of the system along the corresponding coordinate axis expressed positively and negatively, respectively, then the average value of the signals occurring over a given interval represents the average coordinate position of the projectile during the interval. In accordance with the invention, therefore, the average position of the projectile along each coordinate may be determined by actuating an associated binary accumulator to increase its count in one direction in response to each high level signal in the train and in the opposite direction in response to each low level signal, the binary number stored in the accumulator at the end of the operation corresponding to the coordinate position of the projectile at the midpoint of the sampled portion of its trajectory.

In a similar manner the coordinate velocity is determined by separating each train into a first group of signals and a second group of signals, and thereafter inverting the signals in one group and sequentially applying the inverted signals and the remaining uninverted signals to an associated accumulator. The resultant binary number in the accumulator is then representative of the difference between the average position of the projectile during the first half of the sampled portion of its trajectory and the average position during the second half of the sampled portion of its trajectory, or in other words, the time rate of change of the projectile's position at the midpoint of the sampled portion of the trajectory.

In accordance with the invention the coordinate positions and velocities derived in the foregoing manner are entered as the initial conditions in a plurality of digital integrators which are interconnected to selectively extrapolate

olate the trajectory equations for the projectile, either forward or backward in time, to produce output signals representative of the changes in the projectile's coordinate positions as the extrapolation process is carried out. These signals are then combined with the initial position signals which are in turn utilized to actuate three digital servos which are operative to drive three respectively associated mechanical counters to present a visual indication of the coordinates of the point of the projectile's trajectory to which the trajectory equations have been extrapolated.

Among the novel features of the present invention there is also disclosed a bidirection digital position servo operable to drive a positionable element to a position corresponding to the coordinate position of a point on a projectile's trajectory in a three dimensional coordinate system in space. Still another novel feature of the invention herein disclosed is the utilization in the associated digital servos of a bidirectional quantizer which senses incremental rotational changes in the position of a shaft by sensing changes in the inductive reactances presented by a pair of ferromagnetic core inductors positioned adjacent the periphery of a toothed ferromagnetic disk which rotates in accordance with shaft rotation. A further novel feature of the quantizer is the detection of incremental changes in the shaft position by generating first and second bilevel signal trains one of which leads the other by 90° when the shaft is rotated at a fixed rate in one direction and which lags the other by 90° when the shaft is rotated at a fixed rate in the opposite direction, a change in the level of the first train signifying an incremental change in rotational position while the polarity of the change is indicated by the level of the second train when the first train is changing levels.

It is, therefore, an object of the invention to provide a firing point locator system which functions to determine first the position and velocity of a projectile at a point on its trajectory and which is thereafter operable to iteratively extrapolate the trajectory equations of the projectile to determine the firing point thereof.

Another object of the invention is to provide a firing point locator system which utilizes a digital computer to incrementally extrapolate the trajectory equations of a projectile either forward or backward in time to either verify the projectile's impact point or ascertain its firing point.

A further object of the invention is to provide a firing point locator system which utilizes a plurality of digital integrators interconnected in accordance with the trajectory equations of a projectile to extrapolate the trajectory backward in time to determine the projectile's firing point, the digital integrators utilizing as initial conditions the known coordinate positions of the midpoint of a sampled portion of the projectile's trajectory.

Still another object of the invention is to provide a system for digitally determining the coordinates of the midpoint of a sampled portion of the trajectory of a projectile moving in a three dimensional coordinate system.

An additional object of the invention is to provide a system for determining the coordinates of the midpoint of a sampled portion of the path traveled by an object moving in space by generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates in a rectangular coordinate system, and accumulating the individual difunction signals in the trains to produce electrical signals representative of the average coordinate positions of the object during the interval it was traversing the sampled portion of its path in space.

It is another object of the invention to provide a system for digitally determining the coordinate velocities of a projectile moving in an orthogonal coordinate system in space at the midpoint of a sampled portion of the projectile's trajectory.

It is also an object of the invention to provide a system

for determining the velocity of an object moving in an orthogonal coordinate system in space at the midpoint of a sampled portion of the object's trajectory by generating a plurality of difunction signal trains each including N signals and representative of the instantaneous position of the object along a corresponding plurality of coordinates which define the coordinate system, and accumulating the signals in each train to present signals representative of the numerical difference between the summation of the first N/2 signals in each train and the summation of the last N/2 signals in each train.

Still a further object of the invention is to provide an input conversion apparatus for rotating a shaft to a position corresponding to the average value of an applied analog signal over a predetermined period by generating a difunction signal train including N difunction signals during the period, each signal having either a first value representing a predetermined maximum value of the analog signal or a second value representing a predetermined minimum value of the analog signal, the average value of the N signals being proportional to the analog signal over the period, and rotating the shaft through an incremental rotational angle proportional to the maximum or minimum value over N in response to each first or second valued difunction signal, respectively.

Another object of the invention is to provide a bidirectional digital position servo operable to drive a positionable element to a position corresponding to the coordinate position of a point on a projectile's trajectory in a three dimensional coordinate system in space.

A further object of the invention is to provide a bidirectional digital quantizer which senses incremental rotational changes in the position of a shaft by sensing changes in the inductive reactances presented by a pair of ferromagnetic core inductors positioned adjacent the periphery of a toothed ferromagnetic disk which rotates in accordance with shaft rotation.

Still another object of the invention is to provide a bidirectional digital quantizer for detecting incremental changes in the rotational position of a shaft by producing first and second bilevel signal trains one of which leads the other by 90° when the shaft is rotated at a fixed rate in one direction and which lags the other by 90° when the shaft is rotated at a fixed rate in the opposite direction, a change in the level of the first train signifying an incremental rotational change, while the level of the second train at the same instant signifies the sense of the change.

The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages thereof, will be better understood from the following description considered in connection with the accompanying drawings in which several embodiments of the invention are illustrated by way of example. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only, and are not intended as a definition of the limits of the invention.

FIG. 1 is a block diagram of a firing point locator system, in accordance with the invention;

FIG. 2 is a graph illustrating the manner in which the firing point locator system of the invention determines the coordinates and coordinate velocities of a projectile at a point in the projectile's trajectory;

FIG. 3 is a block diagram, partly in schematic form, of a digital projectile tracking computer, in accordance with the invention, which has been employed in the system of FIG. 1;

FIG. 4 is a schematic diagram of a quantizer, in accordance with the invention, which may be utilized in the digital servos in the computer of FIG. 3;

FIGS. 5a and 5b are waveforms of signals appearing at various points in the circuit of FIG. 4;

FIGS. 6a and 6b are waveforms of the output signals

produced by the circuit of FIG. 4 illustrating the manner in which the quantizers of the invention convey output intelligence;

FIG. 7 is a detailed block diagram, partly in schematic form, illustrating the principal physical components of the computer shown in FIG. 3;

FIG. 8 is a word diagram illustrating the manner in which intelligence is stored and processed in the computer of FIG. 7; and

FIG. 9 is a schematic diagram illustrating the manner in which the logical gating circuits are mechanized within the computer of FIG. 7 to perform logical and arithmetic functions.

Referring now to the drawings, wherein like or corresponding parts are now designated by the same reference characters throughout the several views, there is shown in FIG. 1 a firing point locator system, in accordance with the invention, which includes a projectile tracking computer 10 operative in conjunction with a tracking radar 12 and a plurality of signal converters 14 for determining either the firing point FP or impact point IP of a projectile shown at A_2 . Before describing the manner in which the projectile tracking computer of the invention performs its computational function, consideration will be given first to the coordinates in which the system is operative and the manner in which tracking of the projectile is accomplished.

More specifically, in setting up the system shown in FIG. 1, tracking radar 12 is placed at a selected point on the topography and thereafter serves as the origin of an orthogonal coordinate system x, y, h in which the computer operates, the computed coordinates of the projectile's firing point or impact being displayed by the computer in a plurality of registers X, Y and H . As will be described in more detail hereinafter, by merely pre-setting registers, X, Y and H to numbers representing the map coordinates of the tracking radar location, the display in the output registers after a projectile tracking operation may be utilized to present the actual map coordinates of the firing point or impact point.

In the operation of the system, radar 12 is normally operative in a scanning mode during which time the radar is utilized to scan for projectiles which have been fired. When a projectile is detected, the operation of the radar is changed, either manually or automatically, to a tracking mode in which the radar locks on and tracks the projectile through at least a portion of its trajectory; at the start of the tracking mode the radar also transmits directly to the computer an electrical start signal F_R indicating that the computer should initiate a routine termed Fit, which will be described in detail hereinafter.

In addition to the aforementioned start signal, the radar also makes available to converter 14 three analog signals E_X, E_Y and E_H whose voltages are respectively representative of the instantaneous position of the projectile being tracked in the coordinate system x, y, h . It will be recognized, of course, that in a conventional radar the target position is presented basically in terms of range, elevation angle and azimuth angle. However, since there are numerous techniques available for resolving this information into an orthogonal coordinate system, further description of the structure of radar 10 is considered unnecessary.

As set forth hereinbefore, the projectile tracking computer of the invention is basically a digital device which receives its input intelligence information in the form of bilevel signal trains which represent the input intelligence digitally. Although the computer of the invention may be readily adapted for operation upon a number of different forms of digital input signal trains without departing from the invention, it will be assumed hereinafter that the computer receives its input information in the form of three difunction input signal trains $\bar{P}_X, \bar{P}_Y, \bar{P}_H$ which are produced by converter 14 in response to the analog signals E_X, E_Y and E_H , respectively.

One form of structure which is available for converting an applied analog signal to a corresponding difunction signal train is disclosed in co-pending U.S. patent application Serial No. 540,699, filed October 17, 1955, by Siegfried Hansen, for "Analog-to-Difunction Converters," now U.S. Patent No. 2,885,662. Still another structure which represents an improved version of the foregoing device is disclosed in co-pending U.S. patent application Serial No. 592,963, filed June 21, 1956, for "Apparatus for Analog-to-Difunction Conversion," by Daniel L. Curtis, now U.S. Patent No. 2,885,663. In mechanizing converter 14, of course, either a single time-shared converter or three separate converters may be employed for operating on the three input signals E_X, E_Y and E_H to generate the three output difunction signals $\bar{P}_X, \bar{P}_Y$ and $\bar{P}_H$, respectively. It should also be noted from FIG. 1 that converter 14 also receives signals TP_H, TP_X and TP_Y from computer 10; these signals, as will be described in detail hereinafter, are timing pulse signals each of which divides time into what will hereinafter be termed "difunction signal intervals," the timing signals being applied to converter 14 so that each of the difunction signal trains $\bar{P}_X, \bar{P}_Y$ and $\bar{P}_H$ is synchronized with the computer to present one difunction output signal during each operational cycle of the computer as hereinafter described.

Before continuing with the general description of operation of the projectile tracking computer of the invention, the manner in which input intelligence is conveyed by a difunction signal should first be discussed in more detail. It will be recalled that a difunction signal train may be defined as a series of bivalued signals, each signal having either a first value or a second value, the average of the signals in the train representing the average value of the quantity being conveyed. Thus, for example, if the difunction signals represent either a plus or a minus one, the average value of the train over a given interval is obtained by adding the number of plus ones, subtracting the number of minus ones, and dividing the difference by the total number of signals occurring within the interval. Consequently, a difunction train wherein the pattern $+1, +1, -1$ is cyclically repetitive represents

$$\frac{+3-1}{4} = +\frac{1}{2}$$

whereas a train wherein the pattern $+1, -1, -1$ is cyclically repetitive represents

$$\frac{+1-2}{3} = -\frac{1}{3}$$

If now the analog signal E_H representing height, for example, has a voltage range from $-E$ to $+E$ representing the height range from $-20,000$ feet to $+20,000$ feet, then a difunction pattern of $+1, +1, +1, -1$ represents $+10,000$ feet with respect to the radar, while a difunction repetitive pattern of $+1, -1, -1$ represents a $-\frac{1}{3}$ of the range in the negative direction, or $-6,667$ feet with respect to the radar.

Returning now to the description of FIG. 1, when the projectile tracking computer receives signal F_R indicating that the radar is tracking a projectile, and that consequently difunction signals $\bar{P}_X, \bar{P}_Y$ and $\bar{P}_H$ are available for sampling, appropriate gate circuits are opened within the computer to receive a predetermined number of difunction signals in each of the input trains. More specifically, if it is assumed that the particular embodiment of the invention here shown starts accepting difunction signals when the projectile is at point A_1 in FIG. 1, it will accept precisely 4096 difunction signals in each of the input trains, at the end of which time the projectile is at a point A_2 in its trajectory, and the computer will accept no further input information. With this information the computer is then operative, as described hereinafter, to compute the coordinates X_0, Y_0 and H_0 of the midpoint

M by averaging the difunction on signals received, and to selectively extrapolate either forward or backward along the projectile's trajectory to compute the coordinates of either the firing point FP or the impact point IP.

It should be noted that although the firing and impact points are shown in FIG. 1 to lie in plane XY, in practice the elevation of these points will depend upon the terrain; consequently, when the computer extrapolates forward or backward, the location of the impact and firing points is determined by referring to a topographical map of the area, the impact and firing points being given by the X, Y and H register readings when these readings coincide with a corresponding set of values defining actual points on the associated map.

The X and Y registers preferably represent their respective coordinates in meters owing to the fact that topographic maps customarily are plotted in meters. In particular, in the specific embodiment of the invention to be shown and described each +1 difunction signal in difunction trains $\mathcal{D}_X$ and $\mathcal{D}_Y$ preferably has a physical significance of $+2\frac{1}{2}$ meters and each -1 difunction a physical significance of $-2\frac{1}{2}$ meters. Consequently, the X and Y coordinates have a range of $\pm 4096 \times 2\frac{1}{2}$ or $\pm 10,240$ meters, the X coordinate for example, having a value of -10,240 meters if all 4096 difunction signals received are at their low level, and a value of +10,240 meters if all 4096 difunction signals are at their high levels.

In a similar manner, the individual difunction signals in height difunction train $\mathcal{D}_H$ are preferably scaled to have a significance of +5 feet or -5 feet, depending upon whether the signal is high or low, respectively. Thus the maximum height capable of being represented by difunction input train $\mathcal{D}_H$ is 4096×5 or 20,480 feet, the use of feet being preferred because topographical maps show elevation in feet.

Before setting forth in greater detail the structure and detailed operation of the invention, consideration will be given to the mathematical concepts involved in the operation of the computer and the equations which are mechanized therein.

MATHEMATICAL ANALYSIS

The height coordinate of a specified point on the trajectory of a projectile traveling in space may be expressed as the algebraic sum of the known height H_0 of a known point in the projectile's trajectory, and the sum of the incremental changes in the height of the projectile during the interval required for the projectile to travel between the known point and the specified point, this latter term constituting the integral with respect to time of the vertical velocity $\dot{H}$. Thus the height coordinate may be written as:

$$H = H_0 + \int \dot{H} dt \quad (1)$$

The vertical velocity term $\dot{H}$ may be expressed as the sum of the projectile's vertical velocity V_H at the known point and the sum of the incremental changes in velocity during the previously mentioned interval, this latter term being the integral with respect to time of the vertical acceleration $\ddot{H}$. Consequently, the vertical velocity may be written as:

$$\dot{H} = V_H + \int \ddot{H} dt \quad (2)$$

The vertical accelerating forces operating on the projectile in space are the acceleration of gravity g , and atmospheric drag. While gravity is independent of velocity, drag is a function of velocity and may be expressed, within the projectile speeds of interest, as the product of a constant K_H and the velocity. Thus the vertical acceleration of the projectile may be expressed as:

$$\ddot{H} = -(g + K_H \dot{H}) \quad (3)$$

Substituting Equation 3 in Equation 2 then gives:

$$\dot{H} = V_H - \int (g + K_H \dot{H}) dt \quad (4)$$

In a similar manner, the X and Y coordinates of the projectile at any instant may be found from the equations:

$$X = X_0 + \int \dot{X} dt \quad (5)$$

and

$$Y = Y_0 + \int \dot{Y} dt \quad (6)$$

where X_0 and Y_0 are the coordinates of a known point on the trajectory of the projectile and $\dot{X}$ and $\dot{Y}$ represent the velocity vectors of the projectile along the X and Y coordinate axis.

Although the velocity vectors $\dot{X}$ and $\dot{Y}$ are of course independent of gravity, they are effected by atmospheric drag. Accordingly the velocity vectors may be expressed as:

$$\dot{X} = V_X - \int K_X \dot{X} dt \quad (7)$$

and

$$\dot{Y} = V_Y - \int K_Y \dot{Y} dt \quad (8)$$

where K_X and K_Y again represent constant drag factors, and V_X and V_Y are the velocities at the known point on the trajectory.

Referring once more to FIG. 1, it will be recalled that the computer of the invention is operative to compute the average values of the difunction signals transmitted to the computer during the interval in which the projectile moves from point A_1 to point A_2 , and that these average values when multiplied times the full scale range correspond to the coordinates X_0 , Y_0 and H_0 of the midpoint M of the tracking interval. In addition, as will be described hereinbelow with respect to FIG. 2, the intelligence information conveyed to the computer through the difunction signal trains may be utilized to determine the velocities V_X , V_Y and V_H of the projectile at the midpoint M. It will be recognized, therefore, that since the acceleration of gravity g and the drag factors are constants, the computer of the invention has all of the information necessary to extrapolate Equations 1, 5 and 6 backward to find the coordinates of firing point FP, or to extrapolate the equations forward to determine the coordinates of impact point IP.

Consider now the manner in which the difunction signals transmitted to the computer during the tracking interval A_1 to A_2 may be employed for computing the velocities V_H , V_X and V_Y of midpoint M. With reference now to FIG. 2, there is shown a plot of the trajectory in the plane of the trajectory for illustrating the manner in which the height coordinate H_0 of the midpoint M is produced, and the manner in which the vertical or height velocity V_H is determined.

It will be noted first that the trajectory does not have a uniform slope, but instead follows a roughly parabolic curve as it moves from point A_1 to point A_2 through the interval T during which time, as aforesaid, the computer receives 4096 difunction signals in the train $\mathcal{D}_H$. Recall now that the average value of a difunction signal train multiplied by the full scale range corresponds to the average value of the variable position which the train represents. Accordingly, it will be recognized that the height represented by the average of the train is that of the point designated H_{AVE} in FIG. 2, and not the actual height of the midpoint M above the XY plane of the radar. It may be shown, however, that the difference between the computer height H_{AVE} and the actual height of midpoint M is

$$\frac{AT^2}{12}$$

as indicated in the drawing, where A is equal to one-half the acceleration of gravity, or approximately 16 feet per second, and T equals the duration of the tracking interval.

Inasmuch as the interval T is a constant, it follows, therefore, that the value of

$$\frac{AT^2}{12}$$

is also a constant which represents a constant error in height of the computed midpoint, the height error being, for example, approximately 80 feet for a computer embodiment each of whose 4096 iterations is precisely 2 milliseconds in duration.

It should be pointed out at this time that a correction for this error in height is made when the computer is first set up for operation at a particular point, and that the error is thenceforth completely compensated. More specifically, when the X, Y and H registers shown in the computer of FIG. 1 are adjusted to the radar coordinates during system set up, the H register is set to a value corresponding to the actual height of the radar above sea level, plus eighty feet. Thereafter, it follows from the above description, the height coordinate H_0 of point M can be obtained by merely averaging input difunction train $\mathcal{P}_H$ between the times t_1 and t_5 in FIG. 2, the function being expressible by the following equation:

$$H_0 = \frac{\text{Max range} \times \sum_{t_1}^{t_5} \mathcal{P}_H}{T} = \frac{20,480 \sum_{t_1}^{t_5} \mathcal{P}_H}{4096} = 5 \sum_{t_1}^{t_5} \mathcal{P}_H \text{ feet} \quad (9)$$

Continuing now with the description of FIG. 2, the vertical velocity component V_H is obtained by determining the first difference between the average height of the projectile during the interval t_1 to t_3 and the interval t_3 to t_5 . More particularly, the 4096 difunction signals generated in the interval T may be separated into two groups of signals each including 2048 difunction signals, the first group representing the average height of the projectile between times t_1 and t_3 , and the second group representing the average height of the projectile in the interval between points t_3 and t_5 .

Again, as in the valuation of the height of midpoint M hereinabove, the average values represented by the two groups of difunction signals do not represent the true altitudes of midpoints P_1 and P_2 in the two signal intervals, but are smaller than the true altitudes by the error signal ϵ which may be shown to be equal to

$$\frac{AT^2}{48}$$

at both P_1 and P_2 . Inasmuch as the change in height or altitude ΔH of the projectile between points P_1 and P_2 represents an incremental change in height about the midpoint M during the incremental time ΔT between times t_2 and t_4 , it is clear that vertical velocity vector of the projectile at midpoint M may be expressed by the following difference equation:

$$V_H = \frac{\Delta H}{\Delta T} = \frac{HP_2 - HP_1}{\Delta T} = \frac{\left[\frac{\text{Max range} \times \sum_{t_3}^{t_5} \mathcal{P}_H + \epsilon}{\Delta T} \right] - \left[\frac{\text{Max range} \times \sum_{t_1}^{t_3} \mathcal{P}_H + \epsilon}{\Delta T} \right]}{\Delta T} \quad (10)$$

or

$$V_H = \frac{10 \left[\sum_{t_3}^{t_5} \mathcal{P}_H - \sum_{t_1}^{t_3} \mathcal{P}_H \right]}{\Delta T} = - \frac{10 \left[\sum_{t_1}^{t_3} \mathcal{P}_H - \sum_{t_3}^{t_5} \mathcal{P}_H \right]}{\Delta T} \text{ feet per difunction interval} \quad (11)$$

This last equation will be recognized as stating that the

vertical velocity V_H at the midpoint M may be obtained by summing the first 2048 difunction signals in difunction train $\mathcal{P}_H$, subtracting the result from the sum of the second group of 2048 difunction signals in train $\mathcal{P}_H$, and dividing the difference by the incremental time ΔT which in turn represents 2048 difunction signal intervals.

Through a similar analysis, the position coordinates X_0 and Y_0 of midpoint M, and the associated midpoint velocities V_X and V_Y may be shown to be derivable by operating upon the input difunction signal trains $\mathcal{P}_X$ and $\mathcal{P}_Y$ in accordance with the following equations:

$$X_0 = \frac{\text{Max range} \sum_{t_1}^{t_5} \mathcal{P}_X}{T} = \frac{10,240 \sum_{t_1}^{t_5} \mathcal{P}_X}{4096} = 2 \frac{1}{2} \sum_{t_1}^{t_5} \mathcal{P}_X \text{ meters} \quad (12)$$

$$Y_0 = 2 \frac{1}{2} \sum_{t_1}^{t_5} \mathcal{P}_Y \text{ meters} \quad (13)$$

$$V_X = \frac{-5 \left[\sum_{t_1}^{t_3} \mathcal{P}_X - \sum_{t_3}^{t_5} \mathcal{P}_X \right]}{\Delta T} \text{ meters per difunction interval} \quad (14)$$

$$V_Y = \frac{-5 \left[\sum_{t_1}^{t_3} \mathcal{P}_Y - \sum_{t_3}^{t_5} \mathcal{P}_Y \right]}{\Delta T} \text{ meters per difunction interval} \quad (15)$$

It should be noted that the derivation of these equations is simplified by the fact that there is no gravity force to be considered. It also will be recognized by those familiar with digital computational techniques that Equations 9 through 15 indicate that the initial conditions required to solve Equations 1 and 4 through 8 may be derived by simple accumulation processes performed upon the difunction signal trains received by the projectile tracking computer of the invention during the tracking operation.

Consideration will now be given to the general manner in which the computer operates, including the technique utilized for deriving the requisite initial conditions from the difunction signal trains, and the general manner in which the computer then functions to solve the trajectory equations.

GENERAL DESCRIPTION OF COMPUTER OPERATION

The operation of the computer, including the initial setting up of the system, as described hereinbefore, may be broken down into the routines listed in the following table:

Table 1

Routine	Function
60 Clear.....	Clear computer in preparation for computation.
Fit.....	Set X, Y and H registers to radar coordinates. Derive from difunction signal trains the initial conditions expressed in Equations 9 through 15.
Extrapolate:	
Forward.....	Solve trajectory equations for impact point.
Backward.....	Solve trajectory equations for firing point.
65 Reset.....	Prepares computer for Fit Routine on the next tracking operation.

70 The general operation of the computer in carrying out the foregoing routines will be described with reference to FIG. 3 which is a block diagram of the computer.

Referring now to FIG. 3, the computer includes three computing sections 300, 302 and 304 which are employed in conjunction with three respectively associated

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digital servos 306, 308 and 310 for performing the computational functions of the computer during the Fit and Extrapolate routines, the entry of the difunction signal trains $\bar{V}_H$, $\bar{V}_X$ and $\bar{V}_Y$ during the Fit routine being controlled by a combined timing and gating circuit 312. As shown in FIG. 3, timing and gating circuit 312 includes a timing signal generator 314 which generates the standard timing pulse signal T_P referred to previously hereinabove, each signal marking off one difunction signal interval at the input converters.

The timing and gating circuit also includes a pair of counters 316 and 318 which are actuable by start pulse F_R received from the radar to respectively count off 4096 difunction signal intervals and 2048 difunction signal intervals. In operation, counter 316 is used to generate a signal representing the duration of the Fit subroutine, this signal being utilized to control the transmission of precisely 4096 difunction signals in the difunction trains $\bar{V}_H$, $\bar{V}_X$ and $\bar{V}_Y$ to the computing sections 300, 302 and 304. The 2048 counter 318, on the other hand, is utilized for separating the first group of 2048 difunction signals in each of the input trains from the second group, to thereby enable the derivation of the velocity vectors defined by Equations 11, 14 and 15.

In addition to the foregoing elements, timing and gating circuit 312 also includes an extrapolate control circuit generally designated 332 which is employed to initiate the extrapolate routine of the computer and to selectively signal extrapolation in either the forward direction to determine the projectile's impact point, or in the reverse or backward direction to determine the projectile's firing point. As will be described below in more detail, the direction of extrapolation is determined by controlling the mathematical operations performed by the computing elements within computing sections 300, 302 and 304.

Referring once more to FIG. 3 each of digital servos 308 and 310 is similar structurally to height servo 306, which will now be described in detail. Basically the servo is similar to the digital servo shown and described in copending U.S. patent application Serial No. 525,148, filed on July 29, 1955 for "Bidirectional Digital Rate Servo System," by the present inventor, now U.S. Patent No. 2,829,323. As shown in FIG. 3 the servo includes: a reversible motor 334 which is selectively energizable from a source 336 of direct-current potential under the control of a motor relay circuit 338; a digital quantizer 340 which is operative in conjunction with a pair of pick-off heads 342 and 344 for generating an output signal train which indicates incremental rotational movements of a toothed disc 346 attached to the shaft of motor 334; an accumulator register 347 for receiving and accumulating the quantizer output signals; and feedback means, including a switch 348, a low pass filter 350 and a buffer amplifier 352, for controlling the direction of energization of motor 334 in accordance with the value of the signals stored in register 347.

In addition to the foregoing elements, the height servo 306 also includes a mechanical shaft revolution counter 353 which presents a visual indication of the rotational position of the shaft of motor 334, a control switch 354 which is utilized for initially setting into the mechanical counter the height coordinate of the radar, and a variable resistor 356 which is utilized for controlling the response of the servo. It should also be noted from FIG. 3 that the digital servo has an alternate feedback circuit through switch 348 and a servo register 358 which constitutes part of computing section 309 to be described hereinafter, the output train from quantizer 340 being applied to the input circuit of servo register 358 through an adder circuit 360.

Accumulator register 347 and servo register 358 are both basically electronic digital accumulators, or more specifically, binary count-up count-down counters, each

counter having a predetermined number of binary bit places and being responsive to an applied train of bi-valued signals for increasing the count stored therein by one digit each time a signal representing one value is received, and for decreasing by one digit the count stored therein each time a signal of the opposite value is received. In the operation of the servo, the most significant digit of the binary number stored in one of the registers 347 and 358 is employed to control the energization of motor 334, servo register 358 being utilized when switch 348 is in its normal position, which represents the compute operation, whereas accumulator 347 is utilized to control the motor energization when switch 348 is in its reset position.

Considering the operation of the accumulator and servo register with more particularity, assume that in the null condition accumulator 347 is normally cleared or in other words, contains all zeros, and that switch 348 is in the reset position. Assume also that a binary one in the most significant digit, when presented as a low level signal and passed by filter 350, energizes relay 338 to drive motor 334 in a clockwise direction, while a binary zero in the most significant digit, when presented as a high level signal and filtered, energizes relay 338 to drive the motor in the counter-clockwise direction. If then an incremental unit of clockwise or counter-clockwise rotation of the motor shaft causes the quantizer to put out either a -1 or a $+1$ representing signal, respectively, it will be seen that the servo register oscillates back and forth between a binary number in which all digits are zeroes and a binary number in which all digits are ones. Accordingly, mechanical counter 353 will present a stabilized output display in which the least significant digit oscillates in amplitude in accordance with the scaled significance of the quantizer output signals.

Assume now, however, that a relatively large binary number is placed in accumulator 347, the only limitation imposed being that the most significant digit of the number is zero if the number is positive or one if the number is negative. When this is done the servo motor will be energized to drive the mechanical counter in the appropriate direction until the quantizer feedback to the accumulator causes the number to be reduced so that the most significant digit changes from zero to plus one, or vice versa. Thereafter the servo register will oscillate for a short period and finally stabilize in its null condition as described hereinafter. It should be noted here that variable resistor 356 in the motor supply voltage permits the servo motor to operate at full energizing torque until the null point is passed, after which it enables rapid damping of any oscillations which might occur.

At the conclusion of the servo operation, therefore, the count presented by the mechanical counter has been changed by the magnitude of the binary number which was stored in the servo register and in a sense corresponding to the sign of the number; accordingly the mechanical counter has been servoed digitally in accordance with the binary number which was entered in the accumulator. The manner in which the servo operates in conjunction with the remainder of the computer will be described hereinafter after a brief discussion of the structure of computing sections 300, 302 and 304.

Referring once more to FIG. 3, computing sections 300, 302 and 304 are shown to include program sequencing gating networks 362, 363 and 364, respectively, and a plurality of digital integrators which are interconnected therewith. Although the gating networks are shown in FIG. 3 as three separate entities, it should be pointed out that in the detailed embodiment of the invention to be described hereinafter a single gating network is time-shared by all three computing sections.

With reference now to computing section 300 in particular, the computational processes are performed by servo register 358 and three digital integrators 365, 366 and 367, respectively. Register 358, which will herein-

after be termed the H servo register, is utilized to control the operation of the associated height servo 306 as previously described.

With respect to the structure of digital integrators 365, 366 and 367, a complete and rigorous discussion of their basic functioning, from both electronic and mathematical standpoints, is set forth in detail in copending U.S. patent applications, Serial No. 388,780, filed October 28, 1953, for "Electronic Digital Differential Analyzer," and Serial No. 564,683, filed February 10, 1956, for "Electronic Digital Differential Analyzer," both by the same inventor. As illustrated by integrator 365, a digital integrator comprises two registers termed the integrand register and overflow register, here designated 368 and 370, which are operative to store digital information in the form of signals representing binary numbers, and a transfer network interconnecting the two registers. In addition the integrator includes an output circuit for presenting a train of bivalued signals representing the integral generated, and a pair of input circuits one of which is coupled to register 368 for receiving a train of bivalued signals representing the integrand or the quantity to be operated upon, while the other input circuit is employed for applying to the transfer network a train of bivalued signals representing the operand.

In operation, integrand register 368 is operable as an accumulator for summing the signals in the applied signal train, while register 370 is utilized as an overflow register into which the binary number in register 368 is cyclically either added or subtracted once each signal interval, the particular operation performed depending upon the value of the operand signal received during the interval. The overflow digits resulting from each of the additive transfers to the upper register 370 are then extracted during successive intervals to produce the output train representative of the integral.

To more succinctly point out the operation of an integrator, consider the application to register 368 of a difunction integrand signal $d\dot{H}$ representing the time rate of change of velocity, and the application to the transfer network of an operand signal dt representing time. It is apparent that register 368, operating as an accumulator, will produce a binary number representing the vertical velocity $\dot{H}$ by summing the signals in the train $d\dot{H}$. It may be shown, then, that the output train generated by the integrator represents the function $\dot{H}dt$, as indicated in the drawing.

It should be noted from FIG. 3 that integrators 366 and 367 in computing section 300 do not include input circuits for receiving an integrand signal train, but instead have constants stored in their lower registers, the height drag factor K_H being stored in integrator 366 whereas integrator 367 stores the acceleration constant g . Thus these two integrators operate in essence as constant multipliers, their output signal trains representing the products of the operand times the constants stored in their lower registers. It should be noted, however, that the projectile tracking computer of the invention operates in real time, and that the operand signal dt applied to integrator 367 represents either a +1 or -1, depending upon whether the computer is extrapolating forward in time or backward in time.

Consider now the operation of the computer in carrying out in sequence the routines set forth in Table I above. The computer Clear routine is carried out when the radar is first set up at the desired map coordinates, and is utilized to clear accumulator 347, servo register 358, the upper and lower registers in integrator 365, and the upper register in integrators 366 and 367 so that their contents represent zero, the mechanism for accomplishing this routine not being shown in FIG. 3. It will be appreciated of course that a similar routine is carried out simultaneously in computing sections 302 and 304. It should also be noted that those integrator registers carry-

ing constants, such as the lower registers in integrators 365 and 367, remain unaffected by the Clear routine.

In addition to clearing the computer, the Clear routine also permits a set-up subroutine to be carried out to enter into the mechanical counters the coordinates of the radar. More specifically, during the Clear routine switch 354 is switched from its servo position, as shown in FIG. 3, to either the Up or Down position, to thereby energize motor 334 to rotate counter 353 to present the corresponding map coordinate of the radar. This operation is carried out for each of the three coordinates, it being remembered that the height visually displayed by the H counter should be set to a quantity equal to the true altitude of the radar plus the previously discussed constant of 80 feet. It should also be noted that variable resistor 356 may be utilized to control the motor speed, and that while the set-up subroutine is being carried out, energy is removed from the motor relay 338 in each of the digital servos.

After the Clear routine has been completed, the servo register in each of the computer sections is coupled to its associated digital servo and a start signal is awaited from the associated radar indicating that a tracking operation has commenced and to initiate the Fit routine. In this routine, the receipt of the Start signal F_R , as shown in FIG. 3, opens a gate 372 in timing and gating circuit 312 to initiate the counting operations within counters 316 and 318, counter 316 in turn functioning to open a gate 374 in program sequencing circuit 362 to thereby pass to servo register 358 the next 4096 difunction signals in input train $\dot{P}_H$.

During the period of the first 2048 difunction intervals in the sampling interval, 4096 counter 316 functions to open a gate 376 in the program sequencing circuit to thereby accumulate the first group of 2048 difunction signals in register 368 of integrator 365 to present a number representing the average position of the projectile during the first half of the counting interval. At the conclusion of this period 2048 counter 318 functions to close gate 376 and to open an inverting gate 378 to thereby apply to $\dot{H}$ register 368 the second group of 2048 signals in the difunction train $\dot{P}_H$, these signals being inverted or complemented. In this manner, the final number standing in $\dot{H}$ register 368 represents the summation of the first 2048 signals minus the summation of the second group of 2048 signals. In other words, the final number in the register represents a solution to Equation 11 and is the value of the vertical velocity V_H of the midpoint of the projectile's sampled trajectory.

It should be apparent that the number standing in servo register 358, if digital servo 306 was not permitted to operate, would represent the height coordinate H_0 of the projectile at the midpoint in its sampled trajectory, or in other words a solution to Equation 9. As a practical matter, however, as soon as servo register 358 starts to accumulate signals in the difunction input signal train, digital servo 306 is unbalanced and motor 338 starts driving counter 353 in a restoring direction, the output signals from quantizer 340 being applied to adder 360, along with the signals from gate 374, so that the servo register maintains accurate position follow-up of counter 353.

At the conclusion of the Fit routine, gates 378 and 376 in program sequencing current 362 are both closed and, consequently, no further difunction input signals are accepted. It should be pointed out that as a rule digital servo 306 will not yet have reached its null positions, and will therefore continue to drive mechanical counter 353 in a restoring direction. It should be recognized however, that if the servo is permitted to drive to its null position, then the count visually displayed by counter 353 will represent the altitude of the midpoint M in FIG. 2. After the operator of the computer has received a signal indicating that the Fit routine has been terminated, he

may energize extrapolation circuit 332 to cause the computing sections to extrapolate the trajectory equations either backward to evaluate the firing point or forward to evaluate the impact point.

Consider now the manner in which the various integrators are interconnected to solve the trajectory equations. It should be noted first that if the trajectory equations are to be extrapolated forward in time, a signal dt representing a continuous train of plus one difunction signals is applied to the transfer networks of integrators 365 and 367 so that the contents of the associated lower register are added to the contents of the upper register once per iteration. Conversely, if the equations are to be extrapolated backward, a signal dt representing a continuous train of minus one difunction signals is applied to the transfer networks of these integrators so that the contents of the lower register are subtracted from the contents of the upper register once per computational iteration.

Turning then to the elements of computing section 300, if it is assumed that the number stored in $\dot{H}$ register 368 represents the vertical velocity $\dot{H}$, then the output train presented by integrator 365 represents the quantity $\dot{H}dt$. If this output train is applied to the transfer network of integrator 366 to control its additive transfers, it will be recognized that the output train from this integrator will be $K_H \dot{H}dt$, since the constant drag factor K_H is stored in the lower register. In a similar manner, the output train from integrator 367 may be shown to be gdt since the gravity acceleration constant g is stored in its lower register. By combining the output trains from integrators 366 and 367 in an adding network 378, a resultant sum signal train is produced representative of the quantity $(K_H \dot{H}dt + gdt)$ as indicated in the drawing, or stated differently, is representative of the velocity derivative $d\dot{H}$ as may be verified by differentiating Equation 4 set forth above.

The resultant sum train is then passed by gate 380, which is opened during the extrapolate routine, to the $\dot{H}$ register of integrator 365 which accumulates the signals in the train $d\dot{H}$ to modify the original velocity vector V_H stored therein during the Fit routine. Accordingly it will be recognized that integrators 365, 366 and 367 provide an iterative solution of trajectory Equation 4.

The output train $\dot{H}dt$ from integrator 365 is also applied to servo register 358 through a gate 382, which is opened during the extrapolate routine, and through adder 360. It will be appreciated that the quantity $\dot{H}dt$ corresponds to the height derivative dH , as may be verified by differentiating Equation 1, the servo register functioning to accumulate the difunction signals in the input train and to further energize the digital servo system in accordance with the summation of the received signals.

Before completing the generalized description of operation of the projectile tracking computer of the invention, it should first be pointed out that during the Fit and Extrapolate routines identical processes are carried out substantially simultaneously in X and Y computing sections 302 and 304 and their associated digital servos. More specifically, it will be recalled that program sequencing circuit 362 of H computing section 300 is actually a gating matrix which is time-shared with computing sections 302 and 304, the sequencing circuit first being utilized to perform a single iteration for vertical velocity and height, then for X velocity and X coordinate, then for Y velocity and Y coordinate, and then back to vertical velocity and height.

With respect to the computational elements employed in computing sections 302 and 304, each includes a servo register and two integrators which function in the same manner as servo register 358 and integrators 365 and 366 in computing section 300, the only distinction being that

computing sections 302 and 304 have no equivalent to integrator 367 in computing section 300 since the acceleration of gravity is not a function of the X and Y coordinates of trajectory. The servo registers are designated 384 and 386, respectively, while the X coordinate velocity and acceleration integrators are designated 388 and 390 and the Y coordinate velocity and acceleration integrators are designated 392 and 394. Thus, in the Extrapolate routine the output trains from the acceleration integrators in the X and Y computing sections are merely reapplied to the integrand registers of the associated velocity integrators to thereby solve Equations 7 and 8, respectively, while the output trains of the velocity integrators are applied to the associated servo registers in their associated computer section to provide a solution to differential Equations 5 and 6, respectively.

Continuing now with the description of the Extrapolate routine, all three computing sections are operable in synchronism to selectively extrapolate either forward or backward by successive iterations. Although not disclosed in detail in FIG. 3, the specific embodiment of the invention to be shown and described in detail hereinbelow provides controls for either continuous extrapolation in the desired direction, extrapolation in groups of five iterations, or extrapolation by utilizing only a single iteration at a time. Inasmuch as the digital servos are operative continuously throughout both the Fit and Extrapolate routines, the choice of the extrapolate control to be employed is determined by how close the position coordinates visually displayed in the mechanical counters of the digital servos approach the coordinates of a point on the associated terrain map.

For example, assume that the coordinates displayed on the counters at the conclusion of the Fit routine are those of a point high in the projectile's trajectory, and that it is desired to evaluate the projectile's firing point. The computer is then placed in continuous extrapolation in the backward direction until the servo counters indicate that the map coordinates of a point on the terrain are being approached. The continuous extrapolation is then stopped to permit the digit servos to null, after which the five-step or single-step extrapolation switches are selectively energized in the appropriate direction until the coordinates presented in the mechanical counters are identical with the map coordinates of a point on the terrain. These coordinates then represent the firing point. By applying a similar technique of extrapolation in the opposite direction, on the other hand, the impact point of the projectile may be ascertained.

Having obtained the desired information the computer must now be reset to prepare for a subsequent tracking operation on another projectile. In order to fully comprehend the manner in which the Reset routine is accomplished, it should first be understood that throughout the complete running of the Fit and Extrapolate routines, the signals generated by the quantizer in each of the digital servos are applied not only to the associated servo register of the computing section, but also to the associated accumulator register within each of the digital servos. Consequently when the projectile's impact or firing point has been determined, accumulator register 347 in digital servo 306, for example, contains a number whose magnitude and sign are representative of the amplitude and sense of the numerical change of the count in counter 353 in going from the original coordinates of the radar to the coordinates of the firing point or impact point.

In carrying out the Reset routine, the servo loop in the digital servo is changed by switch 348 so that motor 333 is energized from accumulator 347, thereby driving the digital servo to a null whereat the accumulator is emptied and the height counter again presents a visual indication of the radar altitude. Meanwhile similar operations carried out concomitantly in digital servos 308 and 310

return to their respectively associated output registers to the coordinates of the radar. In addition, the Reset routine is also employed to again clear the servo register and the integrators in each of the computing sections in the same manner as described previously for the Clear routine. The computer is then ready to again perform the Fit routine of its computational operations whenever the radar again signals that a projectile is being tracked.

It should be here pointed out that the diagrammatic view of the invention as shown in FIG. 3 illustrates the basic mode of operation of the projectile tracking computer, but does not necessarily show each element of the computer in its optimum form. For example, although switches are shown to be utilized for controlling the Reset operation, in practice the output of either the servo register or accumulator is selectively gated electronically to control the energization of the associated servomotor. In a similar manner, each of the accumulators, servo registers and integrators, shown as separate physical entities in FIG. 3 may be carried as words in a magnetic drum recirculating memory, as will be described in detail hereinbelow.

DETAILED DESCRIPTION OF OPERATION

In order to fully comprehend the operation of the specific embodiment of the invention described in detail hereinbelow, it is first essential to understand the operation of the quantizers in the individual digital servos, the type and nature of the signals produced thereby, and the intelligence information conveyed by these signals. With reference then to FIG. 4, there is shown a schematic diagram of a quantizer which may be utilized in height servo 306 for presenting output signals representative of changes in the rotational position of toothed disk 346 as detected by the previously described pick-off heads 342 and 344.

As shown in FIG. 4, the quantizer includes an oscillator 400 which produces a sine wave output signal which in turn is applied through a transformer 402 to a pair of series L-C circuits, one circuit including a capacitor 404 and the inductance of pick-off head 344 while the other circuit comprises a similar capacitor 406 and the inductance of pick-off head 342. In addition, the quantizer includes a pair of detection circuits 408 and 410 respectively associated with pick-off heads 344 and 342, respectively, each detection circuit in turn including a plurality of rectifiers and capacitors for producing a pair of complementary voltage level output signals representative of the position of its associated pick-off relative to the teeth on toothed disk 346.

Both of pick-off heads 342 and 344 are fixed relative to each other and are positioned adjacent the outer periphery of toothed disk 346, each head comprising a horseshoe shaped ferromagnetic core which presents through its associated winding a variable inductance whose magnitude is dependent upon whether a tooth of disk 346 is beneath the air gap in its core. More specifically, the inductance presented by each head is at a maximum when a tooth of disk 346 is adjacent its air gap, and is at a minimum when the air gap in its core is the space between adjacent teeth.

The value of the capacitor in each L-C circuit is selected to provide an L-C series circuit resonant at the frequency of the applied signal when the inductance is at its maximum value. Consequently, when a tooth is adjacent the gap in a pick-off head a relatively large alternating current signal is presented across the head, whereas a relatively small alternating current signal is presented across the head when the inductance of the head is at its minimum value.

As further illustrated in FIG. 4, each detection circuit is connected across its associated pick-off head and includes two parallel paths to which the signal appearing across the head is applied by a pair of coupling capacitors 412 and 414, respectively, the parallel paths in detection

circuit 408 functioning to produce a pair of complementary output signals A_H and A'_H representative of the relative position of head 344 with respect to the teeth of disk 346, while similar paths in circuit 410 function to produce a pair of complementary output signals B_H and B'_H representative of the relative position of head 342. The left-hand path, as viewed in FIG. 4, includes a reference diode 416 having its anode connected to a -27 volt source, not shown, and its cathode connected to capacitor 412 and to the anode of a blocking diode 417, the other end of this diode being connected, in turn, to the cathode of a clamping diode 418, to one end of a pull down resistor 419, and to one terminal of an output capacitor 420. The other terminal of capacitor 420 is grounded while the second end of resistor 419 and the anode of diode 418 are connected respectively to a source of B- and to a source of -12 volts, either of which source is here shown.

The right-hand path in the detection circuit, in a similar manner, includes a reference diode 422 having its cathode connected to a +15 volt source, not shown, and its anode connected to capacitor 414 and to the cathode of a blocking diode 423. The anode of diode 423 is then coupled to a B+ source, not shown, by a pull-up resistor 424, to the anode of a clamping diode 425 whose cathode is connected to ground, and to one terminal of an output capacitor 426 whose other terminal is grounded.

In the absence of an applied alternating current signal, the voltage across capacitor 420 is normally -12 volts since the pull-down resistor renders diode 418 conductive, whereas the voltage across capacitor 426 is at ground potential owing to the fact that diode 425 is rendered conductive from the B+ source through resistor 424. It also follows, therefore, that the junction of diodes 416 and 417 is floating midway between -12 volts and -27 volts owing to the fact that diodes 416 and 417 are both back-biased, while the junction of diodes 422 and 423 is floating midway between ground and +15 volts since these two diodes are back-biased.

With reference now to FIGS. 5a and 5b, there are shown the waveforms appearing at various points in the detection circuit as toothed disk 346 is rotated from its position as shown, relative to head 344, to a position where one of the teeth is adjacent the gap in head 344. As shown by the left-hand portion of the waveforms in FIGS. 5a and 5b, when the head is adjacent a space in the disk a relatively small alternating current signal is applied to the junction of diodes 416 and 417 and to the junction of diodes 422 and 423 as shown by waveforms 416a and 422a, the peak-to-peak amplitude of the signal being less than 15 volts so that all four of these diodes remain back-biased. Accordingly, the output signals A_H and A'_H across capacitors 420 and 426 are at -12 volts and ground potential, respectively.

Assuming then that disk 346 rotates so that a tooth is adjacent pick-off head 344, a signal of relatively large amplitude is impressed across the junctions of diodes 416 and 417 and of diodes 422 and 423 as illustrated by waveforms 416a and 422a, the signal causing diode 417 to conduct as the signal raises the junction of diodes 416 and 417 above -12 volts and causing diode 423 to conduct when its negative going portion falls below ground potential. Consequently diodes 418 and 425 become back-biased, and the voltage across capacitors 420 and 426 tends to follow the signals passed by diodes 417 and 423.

As shown by the waveforms A_H and A'_H , respectively, when the signal thereafter goes through regions of negative slope and positive slope, respectively, the voltage across capacitors 420 and 426 does not follow the waveforms 416a and 422a, but instead provides a form of envelope detection analogous to the detection of the modulating signal in an amplitude modulated carrier signal. This result is produced by the fact that diodes 418 and 425 remain back-biased while the input signal is large, and that diodes 417 and 423 are front-biased only when

charge is being added to the capacitors and are back-biased as soon as the alternating current signal goes below the voltage on the associated output capacitor. Consequently capacitors 420 and 426 have only a high impedance discharge path during those portions of the input signal cycle when they are not being charged from the input signal.

The structure and function of detection circuit 410 are identical to the structure and function of circuit 408 described hereinabove, circuit 410 being operable to produce a pair of complementary output signals B_H and B'_H representative of the position of pick-off head 342 relative to disk 346. For purposes of discussion hereinbelow, a high level or ground potential in signal A_H or B_H will be termed a one-representing signal, while a -12 volt or low level voltage will be termed a zero-representing signal. Conversely, complementary signals A'_H and B'_H present a one-representing signal as a low level voltage and a zero-representing signal as a high level voltage.

Consider next then the manner in which the quantizer, including its two detection circuits, indicates a change in the rotational position of toothed disk 346. With reference once more to FIG. 4, if each tooth on disk 346 and an adjacent space are considered to be one cycle or one increment of rotation, then pick-off heads 342 and 344 are 90° out of phase with respect to each other. Referring then to FIGS. 6a and 6b, there are shown the waveforms of signals A_H and B_H as they appear when disk 346 is rotated at a constant speed, the waveforms of FIG. 6a representing clockwise rotation of disk 346 while the waveforms of FIG. 6b represent counterclockwise rotation of the disk. It will be seen that waveform B_H leads waveform A_H by 90° when the disk is rotating in a clockwise direction, and lags waveform A_H by 90° when the disk is rotating in a counterclockwise direction.

Assume now that one complete revolution of disk 346 actuates the mechanical counter to produce a change of 100 feet in the altitude visually displayed in the counter. Assume also that the maximum rate of rotation of the toothed disk is one-twentieth of a revolution per difunction interval, or in other words, is of 18° per iteration of the computer. It follows then that the maximum rate of change of the altitude presented by the counter is 5 feet per difunction interval.

It will be apparent from the description set forth below, however, that for a five-toothed disk such as is utilized in the height servo, the quantizer is only capable of distinguishing between ten foot increments of altitude, inasmuch as the quantizer can respond only to such movement of the disk as will produce a change in the output signals A_H and B_H , as previously described with regard to FIGS. 5a and 5b. Thus at the end of a difunction interval the quantizer output signals presented may be identical to those presented at the end of the previous interval, and will therefore indicate that no change has taken place in the counter-reading. On the other hand, if the quantizer signals are different from those presented at the end of the previous difunction interval, then a change of either plus ten feet or minus ten feet is indicated.

In the operation of the quantizer a change in the signal A_H at the end of successive difunction intervals is utilized to indicate that the reading has changed by either plus ten feet or minus ten feet, whereas if the A_H signal remains at the same level as before a zero change is indicated. The B_H signal, on the other hand, is utilized to indicate whether a change in altitude of ten feet is positive or negative, since as pointed out previously, the signal B_H either leads or lags the signal A_H depending upon whether the rotation of the counter is clockwise or counterclockwise, respectively.

More specifically, it will be noted from FIG. 6a that the disk is rotating in a clockwise direction if signal A_H goes from its one-representing value or high level to its zero-representing value or low level and signal B_H is at its zero-representing value or low level, whereas FIG. 6b

illustrates that a high level for signal B_H when signal A_H changes from its high level to its low level indicates an increment of rotation in the counterclockwise direction. In a similar manner these figures illustrate that a change in signal A_H from its low level to its high level represents an increment of clockwise rotation when signal B_H is at its high level, and an increment of counterclockwise rotation when signal B_H is at its low voltage level. All of the foregoing conditions and their operation significance are correlated by the following table, Table II.

Table II

Possible conditions	Prior A_H	Present A_H	Present B_H	Change in H
1.-----	0	0	0	0 No change.
2.-----	0	0	1	Do.
3.-----	0	1	0	-10 feet.
4.-----	0	1	1	+10 feet.
5.-----	1	0	0	Do.
6.-----	1	0	1	-10 feet.
7.-----	1	1	0	0 No change
8.-----	1	1	1	Do.

It will be recognized from the foregoing table that it is necessary to store signal A_H at the end of each difunction signal interval so that it may be compared with the signal A_H as it is presented at the conclusion of the following interval to determine if there has been a change in its voltage level. As will be disclosed in more detail hereinbelow, the storage of signal A_H is accomplished in the detailed computer to be hereinafter described by magnetizing a predetermined spot or cell in a recirculating magnetic memory in accordance with the level of the signal.

The structure and operation of the quantizers in the X and Y digital servos are substantially identical with that of the height servo described hereinabove, the only material distinction being that these quantizers operate in conjunction with toothed disks which have ten teeth in lieu of five as in the height servo. More specifically, it will be recalled that the difunction altitude or height is represented by a difunction train wherein each signal represents ± 5 feet, whereas the height quantizer produces output signals representing either zero or ± 10 feet, thereby setting up a 2:1 scale factor between the signals. Assume now that one turn of the X and Y mechanical counters represents 100 meters instead of 100 feet, and that the 2:1 scale factor between quantizer output signals and difunction input signals is to be maintained in order to simplify the computer's circuitry as described hereinafter. Inasmuch as each signal in the input difunction trains ϕ_X and ϕ_Y has a significance of $\pm 2\frac{1}{2}$ meters as discussed previously, it follows therefore that the quantizers in the X and Y servos must produce signals representing zero or ± 5 meters. Accordingly it will be recognized that ten teeth must be provided in the disks utilized in the X and Y servos to provide the 20 detectable transitions in rotational position which are required to detect an incremental change of 5 meters in the rotation of a shaft where a complete revolution of the shaft signifies 100 meters.

The manner in which the X and Y quantizers present their output signals is identical with that previously discussed for the height servo, the X quantizer generating output signals A_X , A'_X , B_X and B'_X while the Y quantizer generates output signals A_Y , A'_Y , B_Y and B'_Y . Thus Table II, set forth hereinabove, is equally applicable to the X and Y quantizers with the exception that changes in the X and Y coordinates presented by the associated counters are represented by changes of ± 5 meters instead of ± 10 feet.

With reference now to FIG. 7 there is shown in more detail the computational elements employed in a specific projectile tracking computer which has been constructed in accordance with the teachings of the present invention. As shown in FIG. 7 the computer includes a front panel 700 on which are mounted the various computer controls and the mechanical counters for displaying the results of the computation, a recirculating memory system including a magnetic drum unit generally designated 702 for storing applied electrical signals as magnetic cells on a magnetizable medium, a plurality of flip-flops or bistable storage elements which are designated by alphabetical characters, and a logical gating matrix 704 which is operable under the control of the various flip-flops for transferring intelligence information between the panel controls and magnetic drum unit 702, and for performing electrically the computational processes carried out within the computer.

In the particular embodiment of the invention shown in FIG. 7, magnetic drum unit 702 comprises a rotatable drum 706 having a magnetizable periphery, a synchronous motor 708 energizable from a fixed frequency source 710 for rotating the drum at a constant speed, and a plurality of magnetic transducers some of which are utilized for writing applied electrical signals as magnetized cells on the drum periphery and others of which are employed for reading the magnetization of cells on the drum periphery to present electrical output signals representative of the magnetization. The utilization of synchronous motor 708 and fixed frequency source 710 is dictated by the fact that the computer must perform its Fit routine in real time, and must therefore rotate drum 706 through a predetermined angle during each difunction interval. It should be noted, however, that it is not essential to employ a synchronous motor, since an induction motor energized from a servo having precision follow-up may also be utilized to provide synchronous memory operation.

As indicated in FIG. 7 by the dotted lines on the periphery of drum 706, the drum surface is divided into five channels or tracks designated C1, P₁, P₂, L₁ and L₂, each of which has one or more magnetic transducers permanently associated therewith. More specifically, channel C1 is a clock or timing signal channel on which a predetermined number of alternately polarized magnetic cells are permanently recorded, the magnetic pattern on this track being employed to energize an associated reading transducer 712 which in turn is coupled to a clock pulse generator 714 which produces a continuous train of high frequency pulses for synchronizing the operation of the computer through gating matrix 704. In a similar manner channels P₁ and P₂ are also utilized to store permanent predetermined patterns of magnetic cells; these two channels will be termed the first and second marking channels and are operable in conjunction with a pair of respectively associated reading transducers 716 and 718 and a pair of reading amplifiers 719 and 720 for energizing a pair of channel reading flip-flops P₁ and P₂ in accordance with the magnetization of channels P₁ and P₂. Thus each of flip-flops P₁ and P₂ presents at its output terminals a pair of complementary signal trains which are cyclically repetitive with each drum revolution and whose sequential signals correspond to the magnetization of the successive cells on their associated tracks. As will become more apparent from the description of FIG. 8 hereinbelow, channel P₁ is utilized both alone and in conjunction with channel P₂ to separate or distinguish different pieces of intelligence information stored in channels L₁ and L₂. Channel P₂, on the other hand, is also utilized to store signals representing the constant acceleration factor g and the drag constants K_H , K_X and K_Y required to solve the trajectory equations previously described.

As shown in FIG. 7, channels L₁ and L₂ are different

from the permanently recorded channels described hereinabove in that they each operate in conjunction with a pair of magnetic transducers. More particularly, channels L₁ and L₂ are recirculating registers utilized to store serially the results of the computational processes carried out within the computer, and are operable in conjunction with a pair of writing transducers 721 and 722 and a pair of reading transducers 723 and 724, respectively, the writing transducers being energized from a pair of writing flip-flops M₁ and M₂ through a pair of respectively associated writing amplifiers 725 and 726. The reading transducers, in turn, are employed to energize a pair of channel reading flip-flops L₁ and L₂ through a respectively associated pair of reading amplifiers 727 and 728.

In the operation of the computer intelligence information is stored on the surface of drum 706 in a serial fashion and in the form of binary bits, that is, as either a binary one or a binary zero. Stated differently, each track may be considered as an endless chain of magnetic cells each of which may be magnetized in one sense to represent a binary one or in the opposite sense to represent a binary zero, each cell having a circumferential length about the drum equal to the length of each recorded clock pulse in channel C1. Accordingly, the reading amplifiers and their associated output flip-flops present a different binary information bit for each successive clock pulse interval, while the writing amplifiers and flip-flops M₁ and M₂ function to sequentially record in channels L₁ and L₂ a separate and distinct binary information bit during each successive clock pulse interval.

Consider now the relative positions of writing transducers 721 and 722 with respect to reading transducers 723 and 724. As will be disclosed in more detail hereinbelow, the computer performs one complete computational iteration by operating on the H, X and Y coordinates serially or in sequence during the interval required to present in read flip-flops L₁ and L₂ the binary bits previously stored in flip-flops M₁ and M₂. Accordingly, the recirculating time of the L₁ and L₂ channels is precisely one difunction time interval since it will be recalled that during the Fit routine one difunction input signal is received by the computer during each computational iteration.

Owing to the fact that permanent marking channels P₁ and P₂ are continuous around the drum while channels L₁ and L₂ are relatively short recirculating registers, it will also be recognized that the length of the drum periphery must be an integral multiple of the length of the recirculating registers so that the marks in the marking channels always occur concomitantly with predetermined intelligence bits in the recirculating registers. In the particular embodiment of the invention here shown and described, the periphery of drum 706 is precisely five times the length of the recirculating registers; the reason for choosing a one to five ratio, as will be discussed more thoroughly hereinbelow, is to permit extrapolation of the trajectory equations in groups of five iterations at a time, or in other words, to permit the computer to extrapolate through one entire drum revolution.

Consider now the rotational speed of drum 706 in a practical embodiment of the invention, and the number of clock pulses stored around the drum. It will be recalled from the description of FIGS. 1 and 2 that the duration of each difunction signal interval is 2 milliseconds; accordingly, one revolution of the drum then consumes ten milliseconds, since there are five difunction intervals per revolution. It follows, therefore, that the drum speed is 6,000 r.p.m., which may be obtained for example, by driving an eight pole synchronous motor from a 400 cycle per second source.

With respect to the number of clock pulses recorded around the drum periphery, it will be apparent from the description of FIG. 8 set forth hereinafter that there are 133 bit spaces in each of the recirculating channels for

performing the requisite computational functions. Consequently the drum has $5 \times 133 = 665$ clock pulses recorded around its periphery. It should be noted here, incidentally, that the reading and writing heads on the recirculating channels are separated by a distance equal to the length of 131 magnetizable cells, rather than 133, owing to the fact that read flip-flops L_1 and L_2 and write flip-flops M_1 and M_2 provide a memory for two of the binary bits in each of these channels.

With reference once more to FIG. 7, control panel 700 includes a plurality of switches for controlling the operation of the computer, some of these switches having been described previously with respect to FIG. 3. For example, switch 348 in FIG. 3 is also shown on control panel 700 and is designated the routine control switch, this switch having three switching points designated Clear, Reset and Compute. When the switch is set to the Clear position, a high level signal is presented to logical gating matrix on the conductor designated (K) and a low level signal on conductor (K') to indicate that the Clear routine is being carried out, while low and high level signals are presented on conductors (R) and (R') , respectively, to indicate that the Reset routine is not being carried out. Conversely, when switch 348 is set to its Reset position high level signals are presented on conductors (R) and (K') and low level signals on conductors (R') and (K) to indicate that the Reset routine is being carried out and not the Clear routine. On the other hand when switch 348 is in its Compute position, low level signals are presented on both the (R) and (K) conductors while high level signals are presented on conductors (R') and (K') to indicate that neither the Clear nor Reset routine is being carried out. It should be here pointed out that when switch 348 is set to the Clear position, a biasing voltage is removed from certain flip-flops in the computer, as described in more detail hereinbelow, to force these flip-flops to their zero-representing conduction states.

Continuing with the description of control panel 700, when switch 348 is in its Compute position start signal F_R from the radar for initiating the Fit routine is passed on to a Fit control switch 730, this switch having three switch points designated Manual, Off and Radar. When switch 730 is in the Radar position the F_R signal from the radar actuates a relay, not shown, which transmits a high level signal to the logical gating matrix over the conductor designated (P) and a pulse signal over the conductor designated $(F\text{-pulse})$; in addition the relay energizes the signal lamp 732 indicating that the Fit routine is taking place. On the other hand, if switch 730 is in the Off position, the radar start signal F_R merely energizes lamp 732, the computer operator thereby being notified that he can manually initiate the Fit routine by switching to the manual position, at which time a high level signal is presented over conductor (P) . It should be pointed out here that the conductor designated E is complementary to conductor (P) in that a high level signal is presented on conductor E at all times except during the Fit routine when conductor (P) presents a high level signal.

As shown in FIG. 7 the control panel also includes the counter set-up switch 354 previously described with respect to FIG. 3, and in addition a counter selector switch 734 which has three switch positions designated H, X and Y and which is utilized in conjunction with switch 354. More specifically, it will be recalled that in describing FIG. 3 hereinabove, it was assumed that for illustrative purposes that switch 354 was associated with the height servo alone. In practice, however, a single switch is utilized in conjunction with counter selector switch 734 to selectively set-up the initial coordinates in each of H, X and Y counters while the Clear routine is

being carried out; thus while routine control switch 348 is in the Clear position, counter selector switch is moved sequentially to its H position; then to its X position, and finally to its Y position, in each of which positions switch 354 is selectively moved to either its up position or down position to change the coordinates visually presented by the correspondingly designated mechanical counter.

It should be noted here that the computer also includes a single speed control knob 736 which corresponds to the variable resistor designated 356 in the height servo of FIG. 3, the speed control being utilized to control the speed of all of the servomotors when switch 354 is in its servo position, and being utilized to energize the single servo motor designated by the setting of counter selector switch 734 during the clear routine when switch 354 is switched to its up or down position.

In addition to the foregoing control elements, panel 700 also includes three different extrapolate control switches respectively designated 740, 742 and 744 for providing either continuous extrapolation of the trajectory equations after the conclusion of the Fit routine, extrapolation by five iterations or steps, or extrapolation by a single iteration or step. As shown in the drawing, each switch has a normal position from which it can be moved to either the left or right to extrapolate the trajectory equations backward or forward, respectively.

Consider next the signals transmitted to logical gating matrix 704 by the extrapolate control switches. When all three switches are in their normal positions, low level signals are transmitted to the matrix on the conductors designated (Back) , (Forward) , (1 cycle-down) , (5 cycle-down) , and (continuous down) , while high level signals are transmitted to the matrix on the conductors designated (1 cycle-up) , (5 cycle-up) , and (continuous up) . Upon actuation of any of the three switches from its normal position, a high level signal is presented on either conductor (Back) or the conductor (Forward) , depending upon whether the switch is moved to the left to extrapolate backwards or to the right to extrapolate forward. In addition, the voltage states normally presented are reversed on the pair of conductors associated with the particular switch which has been actuated. For example, if the single-step switch 744 is moved to the left to extrapolate backwards by one iteration, high level signals are presented on conductors (Back) and on (1 cycle-down) , whereas a low level signal is presented on conductor (1 cycle-up) ; the remaining conductors, on the other hand, remain at their normal voltage levels. During the Extrapolation routine, of course, conductor (P) presents its afore-mentioned high level signal.

As indicated by the busses designated 746, 747 and 748 in FIG. 7, the three quantizer output signals from each of the digital servos previously described are also transmitted to logical gating matrix 704, while the matrix transmits three output signals O_H , O_X and O_Y back to the control panel. These latter three signals represent the output signals from the computer and are utilized to control the direction of energization of the servomotors in the digital servos during the Fit, Extrapolate and Reset routines. In terms of the digital servo structure previously described with respect to FIG. 3, signal O_H is applied to filter 350 in the height servo 306, while signals O_X and O_Y are applied to similar filters in digital servos 308 and 310, respectively.

Continuing now with the description of the basic elements of the specific projectile tracking computer shown in FIG. 7, the computer as shown includes nineteen flip-flops or bistable storage elements which are operative in conjunction with memory unit 702, gating matrix 704, and the input control switches to provide temporary storage for intelligence information, to control the sub-

routines carried out within the computer, to control the mathematical operations carried on within the computer, and to transfer intelligence information to and from the memory unit.

Before describing the functions performed by the individual flip-flops, consideration will be given first to the designation of the input and output conductors of the various flip-flops shown in FIG. 7. Each flip-flop may comprise either vacuum tubes, transistors, magnetic cores, or any other elements suitable for providing bistable operation, and includes a pair of input conductors which are designated the S input conductor and Z input conductor, respectively, each conductor being further designated by an alphabetical postscript corresponding to the alphabetical designation of its associated flip-flop. In addition, each flip-flop includes a pair of output conductors one of which is designated by the same alphabetical designation as the flip-flop from which it is taken, while the other is designated by the prime of the alphabetical designation of the flip-flop. Thus, for example, flip-flop K_1 has both SK_1 and ZK_1 input conductors and K_1 and K'_1 output conductors.

In operation each flip-flop will be assumed to be responsive to the application of an input signal to its S input conductor for setting to a conduction state corresponding to the binary value one, and to the application of an input signal to its Z input conductor for setting to the opposite conduction state, which corresponds to the binary value zero. In addition it will be assumed that when a flip-flop is in its one-representing state the voltage presented on its correspondingly designated output conductor has a relatively high level value while the voltage presented on its prime output conductor has a relatively low level value. Conversely, when a flip-flop is in its zero-representing state, the voltage presented on its correspondingly designated output conductor has a low level value whereas a high level voltage is presented on its prime output conductor. For example, when flip-flop K_1 is in its one-representing state, high and low level signals are presented on output conductors K_1 and K'_1 , respectively, whereas these voltage levels are reversed when flip-flop K_1 is in its zero-representing conduction state.

Returning now to the description of FIG. 7, the flip-flops there shown may be classified in six groups according to the functions they perform, two of these groups having been discussed previously with regard to the description of memory unit 702. More specifically, flip-flops L_1 , L_2 , P_1 and P_2 may be termed the memory reading group and function as electrical windows for the correspondingly designated channels on drum 706 by sequentially presenting as output signal trains the magnetization of sequential cells in the memory, each flip-flop assuming its one-representing state when a binary one is read by its associated reading transducer and its zero-representing state when a binary zero is read. Flip-flops M_1 and M_2 , on the other hand constitute a memory writing flip-flop group for recording information bits in channels L_1 and L_2 .

The remaining four groups of flip-flops are bracketed in FIG. 7 and are termed counting group 750, program control group 752, temporary memory group 754, and computational group 756. The counting group designated 750 comprises four flip-flops C_1 , C_2 , C_3 and C_4 which are operable as a scale-of-ten binary counter for distinguishing between or separating the various intelligence words stored in channels L_1 , L_2 , P_1 and P_2 , as will be illustrated more fully with respect to the description of FIG. 8 hereinbelow. Program control group 752, on the other hand, includes two flip-flops Q and R which function to provide signals to indicate whether a computational function is being carried out, and to prevent re-actuating the computer falsely when a computational func-

tion has been carried out and the panel control switch which initiated the function has not yet been released.

The temporary memory flip-flop group including flip-flops I_H , I_X and I_Y is utilized to store certain operational results produced during one pass of the recirculating memories so that these results may be utilized in the succeeding computational iteration. More specifically, it will be recalled from FIG. 3 that during the extrapolate routine the output signal from integrator 365 is applied to integrator 366 to control its additive transfers, a similar operation being carried out in computing sections 302 and 304 as well. However, as will be shown in detail in FIG. 8, integrator 366 is operated upon in the serial recirculating memories before integrator 365 is operated upon; consequently flip-flop I_H is utilized to store the output signal from integrator 365 until it can be utilized for operating on integrator 366 during the subsequent memory pass, while flip-flops I_X and I_Y perform the identical function for the integrators in computing sections 302 and 304.

The functions performed by the computational flip-flop group 756 are relatively complex and will be more clearly understood from the detailed description set forth hereinafter. Briefly, however, this flip-flop group includes flip-flops S_1 , K_1 , S_2 and K_2 which are operable in conjunction with read flip-flops L_1 and L_2 and write flip-flops M_1 and M_2 for changing the magnitudes of the numbers stored in the various integrators and registers in accordance with the values of the input received, for making additive transfers between the integrator registers, and for controlling the operation of the 4096 counter and the 2048 counter described hereinabove.

Finally, it should be noted that the three timing pulse signals TP_H , TP_X and TP_Y utilized for interrogating the difunction converters described in connection with FIG. 1 are transmitted to the associated analog-to-difunction converter from gating matrix 704, while the three input difunction signals from the converters are applied to the gating matrix. It will be noted that the three difunction trains are designated $\mathcal{P}'_H$, $\mathcal{P}'_X$ and $\mathcal{P}'_Y$ in FIG. 7; the reason for utilizing the complementary difunction signals in this specific embodiment of the invention is that it simplifies the solution of the difference Equations 11, 14 and 15 as will be described more fully below.

In order to comprehend more fully the detailed operation of the projectile tracking computer of the invention, the arrangement of intelligence information in the memory unit will now be described; it should be noted that in computed parlance the sequence and arrangement of intelligence in the memory is termed the "word structure," and is utilized frequently to teach the sequence of operation of the computer.

With reference now to FIG. 8, there is shown in graphic form the word structure of the computer as it appears at the reading flip-flops during one difunction time interval, the sequence of appearance being from right to left. As shown in FIG. 8, there are 133 clock pulses (C_p) presented during one pass of the recirculating register, the 133 digit time intervals defined by these clock pulses being divided into ten "words" of varying length and designated g through Y . For purposes of simplicity, the g word will henceforth be termed the gravity word, while the words designated $\ddot{H}$, $\ddot{X}$, and $\ddot{Y}$ will be termed the acceleration words. In a similar manner the words designated $\dot{H}$, $\dot{X}$ and $\dot{Y}$ will be termed the velocity words, whereas the words designated H , X and Y will be termed the position words.

It will be noted from the word diagram that each of the position words includes 15 binary information bits, each of the velocity words 12 binary information bits, and each of the acceleration words, including the gravity word, 13 binary information bits. The selection of the number of bits used to represent each word is made in view of the accuracy required of the system, and the

fact that the various integrators to be described hereinbelow must be scaled with respect to each other to permit proper communication between integrators and provide a resultant output signal scaled to actuate the servos described hereinabove.

With reference once more to FIG. 8 it will be noted that marker channel P_1 has a binary value of one recorded in the last digit place of each word for demarking the end of each word, and a binary value of one recorded in the first digit place of each position word, the remainder of the digit places in the P_1 marking channel having binary zeros recorded therein. These marks, as will be seen from the description below, are utilized to change the operations performed by the various flip-flops in carrying out the computer's computational processes, and for sequencing the counting flip-flops C_1 through C_4 in flip-flop group 750 in FIG. 7. In a similar manner, marker channel P_2 also includes a binary one in the last digit place of each word, and in addition, has a binary value of one recorded in the next to the last digit place of each velocity word. Ignoring for a moment the remaining digits stored in the acceleration words of channel P_2 , it will be noted that the next to last digit place in each of the velocity words has a binary one recorded therein while the next to last digit place in each of the position words has a binary zero recorded therein.

Recall now that channels P_1 and P_2 extend around the entire memory drum, and are five times as long as the L_1 and L_2 recirculating channels, or in other words, the word structure of FIG. 8. In each of the P_1 and P_2 channels, therefore, the recording pattern shown in FIG. 8 is repeated precisely five times so that the proper marks are presented in channels P_1 and P_2 during each recirculation of channels L_1 and L_2 . It will be recognized, however, that the computational processes carried out by the computer must be initiated at a predetermined instant in order for the intelligence stored in the memory to be processed in the proper sequence and for the specified number of iterations. The marker bit utilized for initiating the computational processes is termed the origin mark, and is represented by a binary value of one permanently recorded in the next to last digit place of one of the five Y position words which occur in a complete revolution of channel P_2 , the origin mark being indicated in FIG. 8 by the dotted line 800. It will be recognized, therefore, that once during each complete revolution of the memory drum, flip-flop P_2 will present a one-representing signal which corresponds to the origin mark and signifies that the gravity word is about to be presented to be operated upon.

Consider now the remaining binary bits stored in the acceleration words of channel P_2 . It will be remembered from the description of FIG. 7 that the constants g , K_H , K_X and K_Y are essential for extrapolating the trajectory equations which are stored in the P_2 channel. As shown in FIG. 8, the constant g is stored in the first twelve digit places of the gravity word sector of channel P_2 , while the constants K_H , K_X and K_Y are stored in the first twelve digit places of the H , X and Y acceleration words, respectively, of channel P_2 . It will be recognized, therefore, that marker channel P_2 serves as the integrand registers for integrators 367, 366, 390 and 394 in FIG. 3. The values of the constants stored in these registers and their representation will be discussed more fully below.

As pointed out hereinbefore, the markers at the end of the various words in the P_1 and P_2 channels are utilized in conjunction with counter flip-flops C_1 through C_4 to distinguish between the different words. It will also be recalled that these flip-flops operate as a scale-of-ten counter for demarking the words, the output waveforms of flip-flops in performing their counter function being shown in FIG. 8 by the waveforms C_1 , C_2 , C_3 and C_4 . The conduction states of the flip-flops for the various words are correlated by the following truth table.

Table III

Word	Counter flip-flop states			
	C_1	C_2	C_3	C_4
5 g -----	0	0	1	1
$\ddot{H}$ -----	0	0	0	0
10 $\dot{H}$ -----	1	0	0	0
$\ddot{X}$ -----	0	1	0	0
$\dot{X}$ -----	0	0	1	0
$\ddot{Y}$ -----	1	0	1	0
$\dot{Y}$ -----	0	1	1	0
15 Y -----	0	0	0	1
$\ddot{Y}$ -----	1	0	0	1
$\dot{Y}$ -----	0	1	0	1

It will be noted from this table that the Y coordinate words $\ddot{Y}$, $\dot{Y}$ and Y are specified by the conduction states C_3C_4 , the X coordinate words by the conduction states C_3C_4 , the g word by C_3C_4 , and the remainder of the H coordinate words by C_3C_4 . It will also be noted that within each group of words associated with each coordinate, the acceleration words are identified by conduction states C_1C_2 , the velocity words by the conduction state C_1 , and the position words by the conduction state C_2 .

Consider next the intelligence information stored in channels L_1 and L_2 . As shown in FIG. 8 the computer has a single 4096 counter whose count is stored in the gravity word of channel L_1 to control the duration of the Fit routine, and three 2048 counters whose counts are stored in the acceleration words of channel L_1 . It will be recalled that only a single 2048 counter was shown in FIG. 3 for controlling the inputs to the velocity registers. In practice, however, it has been found preferable to employ three separate 2048 counters located immediately preceding the three velocity words for controlling the velocity word inputs during the Fit routine, since it is then unnecessary to utilize an additional flip-flop for holding throughout the three velocity words to indicate whether the first or second group of 2048 difunction input signals is being received. It is clear, of course, that each of these three counters operate in an identical manner and store the same numerical count.

Continuing with the description of FIG. 8, channel L_2 is utilized as a composite register channel which functions as the overflow registers for all of the various integrators and also functions as the servo registers. More specifically, the gravity word sector of channel L_2 represents the overflow register of integrator 367 in FIG. 3, while the acceleration words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ represent the overflow registers of integrators 366, 390 and 394 in FIG. 3. In a similar manner, the overflow registers of velocity integrators 365, 388 and 392 in FIG. 3 are represented by the velocity words $\dot{H}$, $\dot{X}$ and $\dot{Y}$ in channel L_2 , while the position words H , X and Y function as servo registers 358, 384 and 386, respectively. The remaining words in channel L_1 are also utilized in a manner analogous to the use of channel L_2 , the integrand registers of velocity integrators 365, 388 and 392 in FIG. 3 being represented by the $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ words of channel L_1 , while the H , X and Y words of the L_1 channel function as the accumulator registers in the digital servos 306, 308 and 310, respectively.

Consider now the scaling of the various registers, or in other words, the physical significance of a binary one stored in the various binary digit spaces of the servo registers, accumulators, and the integrator registers. It will be recalled that each $+1$ difunction signal in the input difunction train $\mathcal{D}_H$ has a scaled significance of $+5$ feet and each -1 difunction signal has a scaled sig-

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nificance of -5 feet, whereas the signals in the trains ψ_x and ψ_y have a scaled significance of $\pm 2\frac{1}{2}$ meters. Since these signals are applied to the first significant digit place of the associated servo register, it will be recognized that the least significant digit of the height servo register must have a significance of 5 feet, while the least significant digit of the accumulator register and servo register in each of the X and Y computing sections is $2\frac{1}{2}$ meters. Inasmuch as the digits of the servo registers represent distance or position, it follows that the applied difunction input signals which are accumulated must represent rates or velocities. Accordingly the input signals to the height servo register represents ± 5 feet per difunction interval, whereas the input signals to the X and Y coordinate servo registers represent $\pm 2\frac{1}{2}$ meters per difunction interval.

The accumulator registers, on the other hand, do not receive the input difunction signals nor do they receive the output trains from either integrators; instead the accumulator registers receive only the quantizer output signals which have a significance of zero or ± 10 feet for the height servo, and zero or ± 5 meters for the K and Y servos. Accordingly the least significant digit of the height accumulator has a scaled weight of 10 feet, whereas the least significant digits of the K and Y coordinate accumulators have a scaled weight of 5 meters.

Consider next the significance of the last significant digit of the velocity word registers which form the integrators which feed to the servo registers during the extrapolate routine. Although each velocity word has twelve bits, it will be recalled that the last bit space is reserved for marking purposes; hence only the first eleven bits of the velocity words are utilized in the integrators. It may be shown that for a digit integrator which produces its output signal as a difunction signal and which has n digit places, the least significant digit represents

$$\frac{1}{2^{n-1}}$$

of the value of the integrator output signal scaling, the loss of one binary digit being due to the fact that to produce an output train in difunction form, the binary integrand members are stored as

$$\frac{2^n + Z}{2^n}$$

where Z is the integrand intelligence information. Accordingly, the least significant digit of the height velocity integrator represents

$$\frac{5}{2^{10}}$$

feet per difunction interval, while the least significant

$$\frac{2\frac{1}{2}}{2^{10} \times 2^{11}} \text{ meters per difunction interval per difunction interval}$$

digits of the X and Y velocity integrators represent $2\frac{1}{2}$ meters per difunction interval or $\frac{1}{2^{10} \times 2^{11}}$ per difunction interval which in turn simplifies to

$$\frac{2\frac{1}{2}}{2^{10}}$$

meters per difunction interval.

It follows then that the input difunction signals to the integrand registers of the velocity integrators have a significance of

$$\pm \frac{5}{2^{10}}$$

feet per difunction interval per difunction interval for the height coordinate, and a significance of

$$\pm \frac{2\frac{1}{2}}{2^{10}}$$

meters per difunction interval per difunction interval for the X and Y coordinates. The scaling and units of the

30

input signals may be verified by looking to the significance of each of the difunction signals applied to the integrand registers of the velocity integrators during the Fit routine. It may be shown that each difunction signal utilized in the determination of the velocity V_H in accordance with Equation 11 has a significance of

$$\pm \frac{10}{2^{11}}$$

feet per difunction interval per difunction interval which of course simplifies to

$$\pm \frac{5}{2^{10}}$$

feet per difunction interval per difunction interval. In a similar manner each difunction signal utilized to determine V_x and V_y in accordance with Equations 14 and 15 has a significance of

$$\pm \frac{5}{2^{11}}$$

meters per difunction interval per difunction interval, which simplifies to

$$\pm \frac{2\frac{1}{2}}{2^{10}}$$

meters per difunction interval per difunction interval.

Consider next the scaling of the acceleration integrators. It will be assumed at the outset that the value of the constant of gravity is 32.2 feet per second per second, while the constants K_H , K_x and K_y have a value of .012 per second representing the drag factor on some preselected form of projectile. It should also be noted here again that although each acceleration word is thirteen binary digits in length as shown in FIG. 8, only the first twelve digits are utilized in the acceleration integrators, the last digit space in each acceleration word occurring during the marking interval.

In view of the scaling rules discussed hereinabove with respect to the scaling of the velocity words, it follows that the least significant digits of the overflow registers in the X and Y acceleration words in channel L_2 have a significance of

$$\frac{2\frac{1}{2}}{2^{10} \times 2^{11}}$$

meters per difunction interval per difunction interval. It will be recalled however, that the X and Y acceleration integrators receive the output signals from the associated velocity integrators as operand signals. Accordingly, the least significant digits of the integrand registers of the X and Y acceleration integrators is

50

per second, since there are 500 difunction intervals per second. The units of the constants K_x and K_y may be verified by differentiating Equations 7 and 8 and solving for the constants.

Recall now that the true value of the constants K_x and K_y is .012 per second. It will be seen, therefore, that the number stored in the integrand registers should be

$$\frac{.012}{500/2^{10} \times 2^{11}} = 50.3$$

expressing this quantity to the nearest integer as a binary number, the constants K_x and K_y are each included in channel P_2 as the binary number 100000110010 where the binary stored in the most significant digit place is

65

60

70

75

utilized to generate the integrator's output signals in difunction form.

Insofar as the storage of the constants g and K_H are concerned, however, it will be recalled from FIG. 3 that the output trains from the two height acceleration integrators 366 and 367 are added together in adder 378 before being applied to the integrand register 368 of velocity integrator 365. As will be shown in more detail hereinafter, the addition of two difunction trains produces an output difunction train whose value is equal to the sum of the values of the two input difunction trains divided by two. Inasmuch as the difunction adder is interposed between the height acceleration integrators and the height velocity integrator, it therefore follows that the constants stored as g and K_H should be twice as large as they would normally be if there were no difunction adder in the circuit; thus the least significant digit of the overflow registers for both of the height acceleration integrators in the $\ddot{H}$ and $\dot{g}$ words is

$$\frac{5}{2^{10} \times 2^{12}}$$

feet per difunction interval per difunction interval, while the least significant digit of the integrand register of integrator 366 has a scaled value of

$$\frac{500}{2^{10} \times 2^{12}}$$

per second. Consequently the constant K_H , which is equal to .012 per second, should be stored as the number

$$\frac{.012}{500/2^{10} \times 2^{12}} = 100$$

As shown in FIG. 8 by markings appearing in the P_2 channel during the acceleration word $\ddot{H}$, the constant K_H is thus represented by the binary number 100001100100.

Finally, recalling that the least significant digit of the overflow register of integrator 367 has a scaled value of

$$\frac{5}{2^{10} \times 2^{12}}$$

feet per difunction interval per difunction interval, and since the operand signal to this integrator merely represents time, the least significant digit of the integrand register in the g word of channel P_2 in FIG. 8 has a scaled value of

$$\frac{5 \times 500 \times 500}{2^{10} \times 2^{12}}$$

feet per second per second. Since gravity is assumed equal to 32.2 feet per second per second, the binary number to be stored in channel P_2 is equal to

$$\frac{32.2}{5 \times 500 \times 500 / 2^{10} \times 2^{12}} = 108$$

which is expressed in binary form as 100001101100, where the first binary one again represents the conversion digit for permitting binary notation to apply to the numbers in the integrator registers and difunction notation to apply to the integrator output signal train.

Returning now to the description of FIG. 8, before describing the detailed operation of the computer and the functioning of its flip-flops and gating matrix, the basic sequence of operations will first be described with reference to the word diagram. During the initial Clear routine, channels L_1 and L_2 are cleared by recording the number zero in each of the word spaces in each of the channels; in all of the word spaces with the exception of the velocity words of channel L_1 the Clear function is performed by writing a binary zero in each binary digit space of the registers. In the integrand registers of the velocity words, however, a zero is represented by writing binary zeroes in all digit positions from the least significant to the next to the most significant digit of the number,

and writing a binary one in the most significant digit of the number. As will be recognized by those skilled in the computer art and especially those familiar with the operation of digital integrators, a binary one in the most significant digit of the integrand is utilized to permit storage in the registers of binary numbers while still providing a difunction output train rather than a train of binary signals. Thus a binary one in the most significant digit followed by all zeros will cause the associated overflow register to produce a difunction output signal having alternately high and low levels, which as previously described, is representative of the quantity zero. It should be noted here again that the most significant digit of each register's number is actually stored in the next to last digit place of the word owing to the fact that the last digit place of each word is utilized for advancing the computer sequence in response to the marker signals generated by channels P_1 and P_2 . It should also be recalled that during the Clear routine the mechanical counters in the digital servo are set up in the manner previously described, and that the output signals from the quantizers are not utilized within the computer at this time.

After the Clear routine has been terminated, the computer functions to recirculate the zeroes stored in all but the position words of channels L_1 and L_2 pending the start of the Fit routine when a projectile is being tracked. During this waiting period the position words are not merely recirculated, but instead receive any positive or negative signals from the associated quantizers to modify the numbers stored in the associated servo register and accumulator. Recalling first that the digital servos are by nature oscillatory in their response to the most significant digits stored in the servo register, assume for purposes of illustration, that on one pass of the L_1 and L_2 channels an increase of +10 feet is received from the height quantizer, a decrease of -5 meters is received from the X quantizer, and a change of zero meters is received from the Y quantizer. In this recirculation of the memory the binary number 10 is then added to the H servo register number, since the least significant digit of this register represents 5 feet, a binary number of 10 is subtracted from the X servo register number, where the least significant digit is scaled to represent $2\frac{1}{2}$ meters, and no change is made in the numbers stored in the Y accumulator and in the Y servo register.

Correlatively, at the end of each of the position words the carry from the last or most significant digit of each of the servo registers is picked off and transmitted to the associated digital servo for energizing the servomotor in a direction corresponding to the sign of the carry. As will be seen from the description set forth below, the foregoing operations in conjunction with the quantizers are carried out at all times except during the Clear routine.

Upon receipt of a signal from the radar that a projectile is being tracked, the Fit routine is initiated upon the next appearance of the origin mark. Thereafter the 4096 counter is sequenced through 4096 difunction intervals to control the length of the Fit routine, while the 2048 counters are also sequenced through a count of 4096, means being provided for distinguishing between counts of 2048 or less and counts of 2049 or more to thereby control the entry of the input difunction signals in the integrand registers of the velocity words. These same difunction signals are thereafter also added into the servo register numbers along with the quantizer output signals as the position word intelligence is processed.

After the Fit routine is completed the computer idles until the Extrapolate routine is initiated; when this occurs the constant stored in the g word of channel P_2 is either added to or subtracted from the overflow number stored in channel L_2 , depending upon whether extrapolation is forward or backward in time. The difunction output signal from the integrator is then temporarily stored.

In a similar manner, during the $\ddot{H}$ word the constant

K_H in channel P_2 is arithmetically combined with the overflow number in channel L_2 under the control of the difunction output signal product by the $\bar{H}$ word integrator on the preceding memory recirculation. The difunction output signal from integrator 366 at the end of the $\bar{H}$ word is then added to the previously stored output signal from integrator 367, the result being added to the integrand number of integrator 365 which follows immediately.

Simultaneously, the integrand number of integrator 365 is arithmetically combined with the overflow number in channel L_2 , the operation of addition or subtraction again being determined by whether the extrapolation is forward or backward in time. At the end of the $\bar{H}$ word the difunction output signal from integrator 365 is then stored to be utilized as the operand signal on integrator 366 on the next memory recirculation, and is also arithmetically combined, along with the height quantizer output signals, with the servo register number stored in the H position word.

The operation of the computer during the X coordinate words and Y coordinate words while the extrapolate routine is being carried out is similar to the operation on the height coordinate words, the only significant distinction being that the difunction output signals generated from integrators 390 and 394 at the end of the $\bar{X}$ and $\bar{Y}$ words are entered at once in the integrand registers of integrators 388 and 392 which follow immediately during the $\bar{X}$ and $\bar{Y}$ words, respectively. Having thus described the basic manner in which intelligence information is processed and sequenced within the computer, the detailed operation of the computer in carrying out these processes will now be described.

Considering first the manner in which logical gating matrix 704 in FIG. 7 functions to control and actuate the various flip-flops which cooperate therewith, it is well known to those skilled in the art of digital computers that the complete mechanization of the gate circuits which generate the input functions to a flip-flop may be specified by what are termed Boolean or logical equations. For purposes of clarity and simplicity, the logical equations which specify the input signals to all of the flip-flops with the exception of the channel reading flip-flops will first be given. The gate mechanization of the input functions to several exemplary flip-flops will then be considered with reference to the specific gating structures shown in FIG. 9, after which the detailed operational description will be set forth with reference to the logical equations.

$$SC_1 = P_1 P_2 C'_2 (C'_3 + C'_4) \quad (16)$$

$$ZC_1 = P_1 \quad (17)$$

$$SC_2 = P_1 C_1 + P_1 P'_2 = P_1 (C_1 + P'_2) \quad (18)$$

$$ZC_2 = P_1 P_2 \quad (19)$$

$$SC_3 = P_1 P_2 C'_1 C_2 \quad (20)$$

$$ZC_3 = P_1 P_2 C_2 + P_1 C_4 + P_1 P'_2 C'_2 \quad (21)$$

$$SC_4 = P_1 P_2 C_2 C_3 \quad (22)$$

$$ZC_4 = P_1 P_2 C_3 + P_1 P'_2 C'_2 \quad (23)$$

$$SQ = R' P'_1 P_2 C_2 \left[\frac{F\text{-pulse}}{52} + \frac{E}{121} (1\text{-cycle down}) + \frac{5\text{-cycle down}}{121} + \frac{\text{continuous down}}{121} \right] \quad (24)$$

$$ZQ = R P_2 C_2 C_4 \left[\frac{F}{81} + \frac{5\text{-cycle up}}{121} + \frac{\text{continuous up}}{121} \right] + \frac{E}{121} P'_1 P_2 C_2 \frac{5\text{-cycle down}}{121} \quad (25)$$

$$SR = P_1 C'_1 C'_2 Q M'_1 K_1 + \frac{E}{120} Q \quad (26)$$

$$ZR = \frac{F}{82} Q' + \frac{E}{122} (1\text{-cycle up}) + \frac{5\text{-cycle up}}{122} + \frac{\text{continuous up}}{122} \quad (27)$$

$$O_H = \frac{R'}{49} P_2 C_2 C'_3 C'_4 M'_2 + \frac{R}{123} P_2 C_2 C'_3 C'_4 M'_1 \quad (28)$$

$$O_X = \frac{R'}{50} P_2 C_2 C'_3 C'_4 M'_2 + \frac{R}{124} P_2 C_2 C'_3 C'_4 M'_1 \quad (29)$$

$$O_Y = \frac{R'}{51} P_1 P_2 C'_3 C'_4 M'_2 + \frac{R}{125} P_1 P_2 C'_3 C'_4 M'_1 \quad (30)$$

$$SM_1 = \frac{K_1}{14} P'_1 P_2 C_1 + \frac{K'_1}{15} Q' L_1 C'_1 + \frac{P_1 C_1 S_1}{26} + \frac{K'_1}{36} P'_1 (C_2 + Q) (L_1 + S_1) (L'_1 + S'_1) \quad (31)$$

$$ZM_1 = \frac{K_1}{13} + \frac{P'_1 C'_2 Q' L'_1}{16} + \frac{P_1 C_1 S'_1}{27} + \frac{P'_1 (C_2 + Q) (L_1 + K'_1) (L'_1 + K_1)}{37} \quad (32)$$

$$SK_1 = P_1 C_1 (L_1 + S_1) (L_1 + S'_1) + \frac{F}{53} P_2 C_2 Q + \frac{F}{54} P_1 C'_1 C'_2 Q + \frac{E}{91} P_1 C_3 C_4 (K_2 + S'_2) (K'_2 + S_2) + \frac{E}{99} P_1 C'_1 C'_2 Q C'_3 C'_4 (K'_2 + S'_2) (K_2 + S_2) + \frac{E}{103} P_1 C'_1 C'_2 Q (C_2 + C'_4) (C_3 + C_4) \quad (33)$$

$$ZK_1 = P'_1 P_2 C_1 + \frac{E}{25} P'_1 (C_1 + C_2) (L_1 + S_1) (L'_1 + S'_1) + \frac{E}{38} P_2 C_2 + \frac{E}{52} P'_1 (L_1 + S_1) (L'_1 + S'_1) + \frac{E}{56} P_1 C'_1 C'_2 C'_3 C'_4 (K'_2 + S'_2) (K_2 + S_2) \quad (34)$$

$$\begin{aligned}
 SS_1 = & P'_1 P_2 C_1 C'_3 C'_4 A_H \\
 & + P'_1 P_2 C_1 C'_3 C'_4 A_X \\
 & + P'_1 P_2 C_1 C'_3 C'_4 A_Y \\
 & + P_1 C_1 C'_3 C'_4 B'_H + P_1 C_1 C'_3 C'_4 B'_X + P_1 C_1 C'_3 C'_4 B'_Y \\
 & + P_2 C_2 Q + \textcircled{E} C'_1 C'_2 (K_2 + S_2) (K'_2 + S'_2) \\
 & + P_1 C_1 L'_1 \\
 & + P_2 C_2 Q + \textcircled{E} C'_1 C'_2 (K_2 + S_2) (K'_2 + S'_2)
 \end{aligned}
 \tag{35}$$

$$\begin{aligned}
 ZS_1 = & P'_1 P_2 C_1 C'_3 C'_4 A'_H \\
 & + P'_1 P_2 C_1 C'_3 C'_4 A'_X \\
 & + P'_1 P_2 C_1 C'_3 C'_4 A'_Y \\
 & + P_1 C_1 C'_3 C'_4 B'_H L'_1 \\
 & + P_1 C_1 C'_3 C'_4 B'_X L'_1 \\
 & + P_1 C_1 C'_3 C'_4 B'_Y L'_1 \\
 & + \textcircled{E} P_1 C'_1 C'_2 (C'_3 + C'_4) (M_1 + S_2 + K'_2) (M_1 + S'_2 + K_2) (M'_1 + S_2 + K_2) (M'_1 + S'_2 + K'_2) \\
 & + \textcircled{E} C'_1 C'_2 (K_2 + S'_2) (K'_2 + S_2)
 \end{aligned}
 \tag{36}$$

$$\begin{aligned}
 SM_2 = & C'_2 Q' L_2 + P_1 Q' L_2 = (P_1 + C'_2) Q' L_2 \\
 & + P'_1 C_2 (L_2 + K_2) (L'_2 + K'_2) \\
 & + P_1 P'_2 Q L'_2 \\
 & + \textcircled{E} Q C'_1 C'_2 P_2 (L_2 + K'_2) (L'_2 + K_2) \\
 & + \textcircled{E} Q C'_1 C'_2 P'_2 (L_2 + K_2) (L'_2 + K'_2) \\
 & + \textcircled{E} Q P'_1 C_1 L_1 (L_2 + K'_2) (L'_2 + K_2) \\
 & + \textcircled{E} Q P'_1 C_1 L'_1 (L_2 + K_2) (L'_2 + K'_2)
 \end{aligned}$$

$$\begin{aligned}
 ZM_2 = & C'_2 Q' L'_2 + P_1 Q' L'_2 = (P_1 + C'_2) Q' L'_2 \\
 & + P'_1 C_2 (L_2 + K'_2) (L'_2 + K_2) \\
 & + P_1 P'_2 Q L'_2 \\
 & + \textcircled{E} Q C'_1 C'_2 P_2 (L_2 + K_2) (L'_2 + K'_2) \\
 & + \textcircled{E} Q C'_1 C'_2 P'_2 (L_2 + K'_2) (L'_2 + K_2) \\
 & + \textcircled{E} Q P'_1 C_1 L_1 (L_2 + K_2) (L'_2 + K'_2) \\
 & + \textcircled{E} Q P'_1 C_1 L'_1 (L_2 + K'_2) (L'_2 + K_2)
 \end{aligned}$$

$$\begin{aligned}
 SS_2 = & P_1 C_1 \\
 & + C_2 K_2 L_2 \\
 & + \textcircled{E} C'_1 C'_2 K_1 \\
 & + P'_1 C_2 K'_2 S_1 \\
 & + \textcircled{E} P_2 C_2 C'_3 C'_4 \textcircled{\text{Forward}} \\
 & + \textcircled{E} P_1 C_3 C_4 I_H \\
 & + \textcircled{E} P_2 C_2 C'_3 C'_4 I_X \\
 & + \textcircled{E} P_2 C_2 C'_3 C'_4 I_Y \\
 & + \textcircled{E} P_1 C'_1 C'_2 \textcircled{\text{Forward}}
 \end{aligned}
 \tag{39}$$

$$\begin{aligned}
 ZS_2 = & P_1 P'_2 S'_1 Q' + P_1 P'_2 S'_1 (K'_2 + L'_2) = P_1 P'_2 S'_1 (Q' + K'_2 + L'_2) \\
 & + \textcircled{E} C'_1 C'_2 K'_1 \\
 & + P_1 P'_2 Q L'_2 K'_1 K'_2 \\
 & + P_1 P'_2 Q L_2 K_1 K_2 \\
 & + \textcircled{E} P_2 C_2 C'_3 C'_4 \textcircled{\text{Back}} \\
 & + \textcircled{E} P_1 C_3 C_4 I'_H \\
 & + \textcircled{E} P_2 C_2 C'_3 C'_4 I'_X \\
 & + \textcircled{E} P_2 C_2 C'_3 C'_4 I'_Y \\
 & + \textcircled{E} P_1 C'_1 C'_2 \textcircled{\text{Back}}
 \end{aligned}
 \tag{40}$$

$$\begin{aligned}
 SK_2 = & P_1 P'_2 K_1 Q' + P_1 P'_2 K_1 L_2 = P_1 P'_2 K_1 (Q' + L_2) \\
 & + \textcircled{E} P'_1 P_2 C'_1 C'_2 C'_3 C'_4 \textcircled{\text{H}} \\
 & + \textcircled{E} P'_1 P_2 C'_1 C'_2 C'_3 C'_4 \textcircled{\text{X}} \\
 & + \textcircled{E} P'_1 P_2 C'_1 C'_2 C'_3 C'_4 \textcircled{\text{Y}} \\
 & + \textcircled{E} P'_1 P_2 C_1 \\
 & + P_1 P'_2 Q K'_1 L'_2 \\
 & + P'_1 C_2 S'_2 \\
 & + \textcircled{E} P'_1 C'_1 C'_2 Q P_2 (L_2 + S'_2) (L'_2 + S_2) \\
 & + \textcircled{E} P'_1 C_1 Q L_1 (L_2 + S'_2) (L'_2 + S_2) \\
 & + \textcircled{E} P_1 C_1 S'_2
 \end{aligned}
 \tag{41}$$

$$ZK_2 = P_1 P_2 Q' K'_1$$

$$+ P'_1 C_2 (L_2 + S_2) (L'_2 + S'_2)$$

$$+ P_2 C_2 Q$$

$$+ \oplus P'_1 P_2 C_1$$

$$+ P_1 P'_2 Q K'_1 L'_2$$

$$+ P_1 P'_2 K_1 L_2$$

$$+ \oplus C'_1 C'_2 Q P'_2 (L_2 + S_2) (L'_2 + S'_2)$$

$$+ \oplus P_1 C'_1 C'_2$$

$$+ \oplus P'_1 C_1 Q L'_1 (L_2 + S_2) (L'_2 + S'_2)$$

$$+ \oplus P_1 C_1 S'_2$$

(42)

$$TP_H = P_2 C_2 C'_3 C_4$$

(43)

$$TP_X = P_1 C_1 C'_3 C'_4$$

(44)

$$TP_Y = P_1 C_1 C_3 C'_4$$

(45)

$$SI_H = P_1 P'_2 C'_3 C'_4 Q K_2$$

(46)

$$ZI_H = P_1 C'_1 C'_2 C'_3 C'_4 Q$$

(47)

$$SI_X = P_1 P'_2 C_2 C'_3 C'_4 Q K_2$$

(48)

$$ZI_X = P_1 C'_1 C'_2 C_3 C'_4 Q$$

(49)

$$SI_Y = P_1 P'_2 C'_3 C_4 Q K_2$$

(50)

$$ZI_Y = P_1 C'_1 C'_2 C'_3 C_4 Q$$

(51)

Before considering the logical significance of the various terms in the foregoing equations, consideration will be given first to the manner in which these terms specify in detail the mechanization of the logical gating matrix 704 in FIG. 7. For purposes of simplicity and clarity, the mechanization of the input signals to flip-flops C_1 and C_2 will be described with particularity and with reference to Equations 16 and 17 for flip-flop C_1 , and to Equations 18 and 19 for flip-flop C_2 . With the understanding of gating techniques thereby gained the mechanization of the remaining logical equations will be readily apparent to those skilled in the art.

Referring now to FIG. 9, the logical gates which mechanize the input functions to flip-flops C_1 and C_2 comprise a plurality of logical "and" gates and logical "or" gates, each logical "and" gate being represented by a semicircular hood with a dot (.) in the center thereof, while each logical "or" gate is represented by a semicircular hood with a plus sign (+) in its center. The "and" and "or" gates may utilize either vacuum tubes, transistors or crystal rectifiers, and are preferably similar to the gating circuits shown and described in connection with FIGS. 3 and 4 of the article entitled "An Algebraic Theory for Use in Digital Computer Design," by Eldred C. Nelson, on page 12 of the September 1954 issue of the Transactions of the IRE Professional Group on Electronic Computers.

Briefly stated, an "and" gate includes two or more input terminals and a single output terminal and is responsive to the voltage levels of two-level signals applied

to its input terminals for producing a high level output signal at its output terminal only when all of the input signals are at their high level values. Each "or" gate, on the other hand, includes two or more input terminals and a single output terminal and is responsive to the voltage levels of two-level signals applied to its input terminals for producing a high-level output signal at its output terminal whenever one or more of the input signals is at its high level value.

It should be pointed out that the "and" gates which are connected directly to the input terminal to each flip-flop will hereinafter be termed "clock pulse and" gates. Structurally a "clock pulse and" gate and a conventional "and" gate, as described hereinabove, are identical, the difference between these gates being in their operational significance. More specifically, it has been pointed out above that an "and" gate in the conventional sense is responsive to what are known to the art as voltage-level input signals to produce a voltage-level output signal. It will be recognized by those skilled in the art, however, that flip-flops are generally triggered with a clock pulse signal which has a relatively short time duration as contrasted with the time duration of each voltage-level signal, which has a minimum interval of one digit time interval. In order to provide a means for triggering the flip-flops, each input terminal to each flip-flop has associated therewith a multiple-input-terminal "and" gate, one of whose input terminals receives a periodically recurring clock pulse which divides real time into clock pulse intervals, or as they are more familiarly termed, digit time intervals. The clock pulse signal by definition, therefore, presents a pulse once per digit time interval, which pulse is preferably of relatively short duration.

If now the clock pulse signal is normally at a relatively high level voltage corresponding to the high level voltage of the voltage-level signals produced at the output circuits of the flip-flops, and if each clock pulse results in a brief negative excursion of the clock pulse signal to the low level voltage of the voltage-level signals applied to the gates, it will be recognized that an applied clock pulse signal will be passed by a "clock pulse and" gate to its associated flip-flop input terminal only when a clock pulse is received and the voltage-levels of any other signals applied to the gate are at their high level voltage.

Referring once more to FIG. 9, Equations 16 and 17 which define the input signals to flip-flop C_1 are mechanized by a pair of two-input terminal "clock pulse and" gates 900 and 902 each of which has one input terminal connected to a clock pulse bus 904, a four-input terminal "and" gate 906, and a two-input terminal "or" gate 908. More specifically, "or" gate 908 receives the signals C'_3 and C'_4 and thereby generates an output signal ($C'_3 + C'_4$) which is applied to one input terminal of "and" gate 906, the other three input terminals of this latter gate being utilized for receiving signals P_1 , P_2 and C'_2 . Consequently the output signal from "and" gate 906 represents the function $P_1 P_2 C'_2 (C'_3 + C'_4)$, this signal being applied to the remaining input terminal of "clock pulse and" gate 900 which functions to pass the applied clock pulse signal whenever a high level output signal is presented by gate 906. Considering then the logical significance of both Equation 16 and its gate mechanization, it will be recognized that flip-flop C_1 receives a set-to-one signal whenever flip-flop P_1 is in its one-representing state "and" flip-flop P_2 is in its one-representing state "and" flip-flop C_2 is in its zero-representing state "and" either flip-flop C_3 is in its zero-representing state "or" flip-flop C_4 is in its zero-representing state.

The remaining input terminal of "clock pulse and" gate 902, on the other hand, is connected directly to the conductor designated P_1 and thus provides a set-to-zero signal to flip-flop C_1 whenever flip-flop P_1 is in its one-representing state. It should be noted here that any time flip-flop C_1 receives a set-to-one signal from gate 900, it also receives a set-to-zero signal from gate

902 since the sole logical condition P_1 in the zero setting function is also one of the several prerequisite conditions in the one setting function. In the digital computer art whenever input signals are received simultaneously by both flip-flop input circuits, the signal combination is termed a triggering function and operates to reverse the state of the flip-flop from what it was prior to the receipt of the input signals.

The input functions to flip-flop C_2 are in turn mechanized by a pair of "clock pulse and" gates 910 and 912, a pair of two input terminal "and" gates 914 and 916, and a two-input terminal "or" gate 918. As shown in FIG. 9, gate 918 receives input signals C_1 and P'_2 to produce the function $(C_1 + P'_2)$ which is applied to "and" gate 914 along with signal P_1 , thereby generating the output function $P_1(C_1 + P'_2)$ which corresponds to logical Equation 18 as set forth above. This signal is then utilized to control the setting of flip-flop C_2 through the operation of gate 910. In a similar manner, "and" gate 916 combines the signals P_1 and P_2 and thus mechanizes Equation 9.

It will be recognized by those skilled in the art that the specific mechanizations shown are merely exemplary and are not the only mechanizations which could be utilized for generating the input functions to flip-flops C_1 and C_2 . For example, Equation 18 may be mechanized as shown in FIG. 9, or by mechanizing the alternate equation form $P_1C_1 + P_1P'_2$ with two two-terminal "and" gates feeding a two-terminal "or" gate. In a similar manner, Equation 19 could be mechanized by utilizing a single three-input terminal "clock pulse and" gate instead of the structure shown in FIG. 9.

It should also be recognized that each of the flip-flop input functions set forth hereinabove in equation form should include an additional logical condition which is not shown, namely, the clock pulse signal C_p which is utilized as described with regard to FIG. 9 to perform the actual switching of the flip-flop. Since this clock pulse signal is uniformly employed only as an actuating signal which is selectively passed or rejected, for purposes of simplicity only the logical conditions controlling the passage or rejection of the clock pulse are set forth.

Consider now the detailed operation of the particular projectile tracking computer exemplified by the drawings. In order to best describe the functioning of the computer, the various operations of the computer will be described with reference to detailed FIGS. 3, 7 and 8.

Assuming that the computer is now being put into service at a new projectile tracking site, the first thing that occurs which is of significance is the synchronization of the scale-of-ten counter comprising flip-flops C_1 through C_4 , and its continued operation thereafter in the proper sequence. The sequencing of the counter is specified by terms 1 through 9 in Equations 16 through 23, while the initial synchronization is assured by terms 10, 11 and 12 in Equations 18, 21 and 23, respectively. Inasmuch as it is possible for flip-flops C_1 through C_4 to assume the proper state initially so that no initial synchronization is required, the regular count sequencing terms will be discussed first.

With reference now to the count sequence set forth in Table III hereinabove and to the waveforms of FIG. 8, it will be noted that flip-flop C_1 is set to its one-representing state at the end of each of the acceleration words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$, and that during these acceleration words flip-flop C_2 is always in its zero-representing state and either one or both of flip-flops C_3 and C_4 is in its zero-representing state. Recalling that the last digit time interval of each word is identified by flip-flops P_1 and P_2 both being in their one-representing state, it follows that term 1 of Equation 16 will set flip-flop C_1 to one at the beginning of the velocity words as desired.

With respect to the zeroing of flip-flop C_1 at the end of the $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ words, the mere signal P_1 is sufficient, as specified by term 2 of Equation 17. It should be noted that this term will also apply a zero setting signal to flip-flop C_1 at the end of the position words H , X and Y , and again at the end of the acceleration words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ and g . At the end of the H , X , Y and g words this has no significance whatsoever since the flip-flop is already in its zero state. In a similar manner, the zero set signal at the end of the $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ words will not keep flip-flop C_1 from going to its one-representing state in response to term 1 of Equation 16, since it will be recalled that the application of signals to both inputs of a flip-flop simultaneously triggers the flip-flop, or in other words, makes it reverse its conduction state.

Continuing, in normal counting operation flip-flop C_2 is set to its one-representing state at the end of the velocity words $\dot{H}$, $\dot{X}$ and $\dot{Y}$, the end of these words being defined by the logical condition P_1C_1 as shown by term 3 of Equation 18 where the condition C_1 denotes the acceleration words as aforesaid while condition P_1 denotes the last digit space of the words. In a manner analogous to the zeroing of flip-flop C_1 , the flip-flop C_2 is zeroed by the term P_1P_2 as indicated by term 4 of Equation 19.

It should be noted here that the condition P_1 alone is not sufficient to zero flip-flop C_2 as it was in term 2 above, since a high level P_1 signal is presented during the first digit time interval of each of the position words H , X and Y when flip-flop C_2 must remain in its one-representing state. Consequently, the condition P_1P_2 is utilized to define the mark in channel P_1 occurring at the end of the position words. It should also be noted that the condition P_1P_2 applies a zero set signal to the flip-flop at the end of each word; however, the application of the signal has no effect on the flip-flop except at the end of the position words, since term 3 overrides term 4 in a triggering function when the C_2 flip-flop is set to one at the end of the velocity words.

As shown in FIG. 8, in its normal counting sequence, flip-flop C_3 is set to its one-representing state at the end of the position word H and at the end of the position word Y , and is set to zero at the end of the g acceleration word and at the end of the position word X . The set to one function of flip-flop C_3 at the end of the H word and Y word is specified by term 5 of Equation 20; it should be noted that this term also provides a set to one signal at the end of the X position word as well, at which time the flip-flop should be zeroed. The zeroing is accomplished at this time by the triggering function $P_1P_2C_2$ specified by term 6 of Equation 21, the passage of both signals to the flip-flop functioning to reverse its conduction state or in other words to restore the flip-flop to its zero state. The zeroing of the C_3 flip-flop at the end of the g word, on the other hand, is accomplished by term 7 of Equation 21 which specifies that a zeroing signal should be applied to flip-flop C_3 whenever flip-flop C_4 is in its one-representing state and a marker pulse appears in flip-flop P_1 . It should be noted that term 7 will apply a zeroing signal to flip-flop C_3 at the end of the $\ddot{Y}$ word when C_3 is already zero, at the beginning of the Y word when C_3 is still zero, and at the end of the Y word at which time term 5 of Equation 20 serves as a triggering function to set the flip-flop to its one state. Consequently term 7 assures that C_3 is zeroed throughout the $\ddot{H}$, $\dot{H}$ and $\ddot{H}$ words, so that at the end of H word the flip-flop will be trig-

gered to one even though term 6 as well as term 5 passes a clock pulse signal to the flip-flop.

In a similar manner flip-flop C_4 is normally set to one at the end of the X position word by term 8 of Equation 22 which specifies set flip-flop C_4 to one at the end of any word in which both flip-flops C_2 and C_3 are in their one-representing states; as shown by the waveforms of FIG. 8, this condition is satisfied only at the end of the X word. Insofar as the zeroing of flip-flop C_4 is concerned, term 9 of Equation 23 specifies that C_4 should be zeroed at the end of every word during which C_3 has been in its one-representing state. During the $\bar{X}$, $\bar{X}$ and X words when C_3 is in its one state this term has no effect, since C_4 is already in its zero state; accordingly term 9 is only operative at the end of the g word, at which time flip-flop C_3 is again in its one-representing state.

As indicated previously, the terms 1 through 9 define the normal sequencing of the counting flip-flops once the counter has been synchronized. Assuming, however, that the counter is not initially synchronized with the sequential appearance of the words stored in channels L_1 and L_2 , the counter is forced into synchronization by terms 10, 11 and 12 in Equations 18, 21 and 23, and by term 2 in Equation 17. More specifically, it will be noted from FIG. 8 that a marker signal occurs in channel P_1 during the first digit time interval of each of the position words, this digit time interval being identified by the condition $P_1P'_2$ since no marker occurs in channel P_2 at this time. It will also be recognized that each time the condition $P_1P'_2$ is satisfied flip-flop C_1 should be in its zero state and flip-flop C_2 should be in its one-representing state.

It is apparent that if flip-flop C_1 is falsely in its one-representing state at the beginning of one of the position words, it will be set to zero at the end of the first digit time interval of the word by term 2 of Equation 17 in the manner previously described. Simultaneously, flip-flop C_2 is also forced to its proper state by term 10 in Equation 18; consequently during the latter part of each position word flip-flops C_1 and C_2 are forced to the proper conduction states. In particular, flip-flops C_1 and C_2 will be forced to their proper states at the beginning of the position word Y. If flip-flops C_3 and C_4 are then in their zero and one states, respectively, the counter is synchronized and will thereafter count in the manner described previously.

If however the conduction states of flip-flops C_3 and C_4 are improper, at the end of the Y position word flip-flop C_2 will be zeroed by term 4 of Equation 19, while flip-flops C_3 and C_4 will assume some combination of states other than both being high, or in their one-representing states. At the end of the g word then, flip-flop C_1 will be set to its one-representing state by term 1 of Equation 16, which is obviously erroneous. So also, at the end of the H word the condition C'_1C_2 will be set up since term 2 will zero flip-flop C_1 while term 3 will set flip-flop C_2 to its one-representing state. This combination of states is also erroneous for the $\bar{H}$ velocity word. At the end of the $\bar{H}$ word flip-flop C_2 will again be zeroed by term 4 leaving both of flip-flops C_1 and C_2 in their zero states.

During the following digit time interval then flip-flop C_2 is again set to its proper state by the $P_1P'_2$ mark combination as given by term 10 of Equation 18, this same mark being utilized simultaneously to zero flip-flops C_3 and C_4 , as specified by terms 11 and 12 in Equations 21 and 23, respectively. Thus all four of the flip-flops C_1 through C_4 are now in their proper states

for the H position word, and the counter has been synchronized.

After the scale-of-ten counter has been synchronized, the computer clear routine may be initiated at any time for preparing the computer for its subsequent operations. Although various portions of the computer are operative prior to the initiation of the clear routine, the functions performed are of no significance at this time; accordingly these portions of the computer will be described after the clear routine has been described.

When the routine control switch 348 on the front panel shown in FIG. 7 is switched to the clear routine several different operations take place. Firstly a number of the computer flip-flops including flip-flops Q, R, K_1 , S_1 , K_2 , M_2 , I_H , I_X and I_Y are forced into their zero states, while flip-flop S_2 is forced into its one-representing state.

Although the signal (K_1) , described heretofore with respect to FIG. 7 as the clear signal, could be utilized as a logical gating condition for forcing the flip-flops specified above to the desired states, in the particular embodiment of the invention here under consideration, the forcing of the flip-flops is accomplished by removing the pull down grid biasing voltage from one side of the flip-flop. Since this technique is well known to the computer art and merely involves opening of a biasing voltage with the routine control switch when it is set to the clear position, further description of the structure for performing this function is considered unnecessary.

The zeroing of flip-flop M_2 at this time is especially important since this causes a continuous chain of binary zeroes to be written into all of the digit spaces in channel L_2 . This same technique cannot be utilized, however, for writing zeroes in the L_1 channel owing to the fact that a binary one must be written in the most significant digit space of the integrand numbers in the velocity words $\bar{H}$, $\bar{X}$ and $\bar{Y}$; it will be recalled that these binary ones are recorded in the next to last digit space of these words, and are utilized to represent an integrand binary number representing zero. All of the remaining digit spaces in the L_1 channel, on the other hand, are filled with binary zeroes.

With reference now to the equations, term 13 of Equation 32 specifies that flip-flop M_1 receives a set to zero signal every digit time interval, thereby assuring that flip-flop M_1 is normally maintained in its zero-representing state. At the end of the next to last digit time interval of each velocity word ($P'_1P_2C_1$) the M_1 flip-flop is then set to one by term 14 of Equation 31, this latter term being effective as a triggering function even though a zeroing signal is simultaneously applied by term 13 of Equation 32. It should be noted here that the binary one is written in the next to last digit space of the velocity word even though the condition P'_1P_2 in term 14 specifies that flip-flop M_1 should contain a binary one during the last digit time interval of the word; the reason for this apparent discrepancy is that the time flow of the information bits shown in FIG. 8 is taken with respect to read flip-flops L_1 , L_2 , P_1 and P_2 whereas term 14 sets flip-flop M_1 which is the write flip-flop on channel L_1 and is thus effectively one digit delayed from flip-flop L_1 . Consequently during the last digit time interval of any word the L_1 flip-flop holds the contents of the last digit space of the word while flip-flop M_1 holds the bit stored in the next to last digit space.

The purpose of setting flip-flops S_1 , K_1 , K_2 , I_H , I_X and I_Y to zero during the clear routine is to assure that erroneous computations are not carried out by the computer when the clear routine is terminated, while flip-flops Q and R are zeroed to assure that the computer is not falsely actuated to enter either the Fit or Extrapolate routines. It will be remembered that while the clear routine is being carried out the counters in the digital servos also are set up

in the manner described previously to present the radar coordinates. After this has been done the routine control switch on the computer is returned to its compute position, and a low level signal is once more presented to the gating matrix on conductor (K1) and a high level signal on conductor (K1).

Consider now the various operations which take place within the computer while it is awaiting the start of the Fit routine. It should be pointed out that the computer is now in what will hereinafter be termed its idle condition, the idle condition being distinguished from two other conditions termed dawdle and compute by the states of the Q and R flip-flops. The following Table IV correlates the conduction states of these flip-flops with the conditions they represent.

Table IV

Flip-flop Q	Flip-flop R	
0-----	0-----	Idle.
1-----	0 or 1-----	Compute [represents both the Fit and Extrapolate routine].
0-----	1-----	Dawdle.

As will be shown in more detail, the dawdle routine is utilized as an intermediate step to return the computer from its compute condition to the idle condition at the end of the Extrapolate routine.

Consider now the idle condition which is assured by virtue of the fact that flip-flops Q and R were zeroed automatically during the clear routine. The binary zeroes which have been stored in the acceleration words and velocity words must be recirculated during this period, terms 15 and 16 of Equations 31 and 32, respectively, specifying this function in the L_1 channel. These terms specify that the recirculation should occur by transferring into the M_1 flip-flop the contents of flip-flop L_1 , but only when Fit or Extrapolate are not taking place as specified by Q' , and only during the velocity and acceleration words, as specified by the condition C'_2 . In addition term 16 includes the logical condition P'_1 which states that during the last digit time interval of the velocity and acceleration words a zero should not be recirculated. The purpose in withholding this term, it will be seen, is to permit storage of the A signals from the H, X and Y quantizers in the last digit space of the associated velocity words.

In channel L_2 , on the other hand, the recirculation of the acceleration and velocity words is accomplished by terms 17 and 18 of Equations 37 and 38. In these terms the conditions $Q'C'_2$ again specify that L_2 should be transferred to M_2 during all times when the machine is not in the Fit or Extrapolate routine and a position word is not being processed.

The reason why the contents of the position words are not recirculated, it will be remembered, is that the accumulator registers and servo-registers accept the output signals from their associated quantizers at all times following the clear routine. Recall now from the description of Table II hereinabove that the height quantizer output signals may represent zero or $\pm$ ten feet, while the X and Y quantizer output signals may represent zero or $\pm$ five meters; it will also be recalled that a change of ten feet or five meters, as the case may be, is determined by whether the signals A_H , A_X or A_Y have been changed from a high level to a low level or vice versa, the signals B_H , B_X and B_Y indicating the direction of the servo's rotational changes.

The sequence in which the functions outlined in Table II are entered into the computer will now be considered. At the end of the next to last digit time interval of the velocity words, as specified by the condition $P'_1P_2C_1C'_3C'_4$ for the height coordinate, by $P'_1P_2C_1C'_3C'_4$ for the X co-

ordinate, and by $P'_1P_2C_1C'_3C'_4$ for the Y coordinate, the S_1 flip-flop is set to its one-representing state if the associated quantizer A signal is at its high level value, and to its zero state if the quantizer A' signal is at its high level value. These operations are specified by terms 19 and 20 of Equations 35 and 36 for the height coordinate, by terms 21 and 22 for the X coordinate, and by terms 23 and 24 for the Y coordinate. Thus during the last digit time interval of each velocity word, flip-flop S_1 holds the A output of the quantizer associated with the particular coordinate being operated upon.

At the same times that the S_1 flip-flop receives the new A_H , A_X and A_Y from the quantizers, namely at the end of the next to last digit time interval of the velocity words, flip-flop K_1 is zeroed by term 25 in Equation 34 preparatory to being utilized for comparing the new A signal stored in flip-flop S_1 and the old A signal, which as will be seen below, is stored in the last digit space of the associated velocity word.

At the end of the last digit time interval of each of the three velocity words H, X and Y, three functions are carried out simultaneously. Firstly, the new A signal is stored in the last digital place of the velocity word in channel L_1 so that it can be used as the old A signal on the next recirculation of the L_1 and L_2 channels. Secondly, flip-flop K_1 is utilized to compare the old A signal which is in flip-flop L_1 and the new A signal which is in flip-flop S_1 , the K_1 flip-flop being set to one if the signals are different indicating an incremental change in the quantizer's rotational position during the preceding difunction interval. Thirdly, at the end of the velocity words the S_1 flip-flop receives the sign of any change set up in flip-flop K_1 in order to indicate whether the rotational increment was clockwise or counter-clockwise.

Consider now the logical terms which specify the mechanization of the foregoing functions. Terms 26 and 27 of Equations 31 and 32, respectively, specify the transfer into write flip-flop M_1 , at the end of each velocity word, of the new A signal stored in flip-flop S_1 , thereby writing in the last digit space of the velocity words H, X and Y, respectively, the latest signals A_H , A_X and A_Y received from the quantizers. At the very same time, term 28 of Equations 33 specifies that the previously zeroed flip-flop K_1 should be set to its one-representing state if the contents of flip-flops S_1 and L_1 are different indicating that the old and new A signals from the particular quantizer are different, as discussed hereinabove with respect to Table V.

Finally, at the end of the velocity words H, X and Y the sign of the servo change entered in flip-flop K_1 is in turn entered in flip-flop S_1 , this operation being specified by terms 29, 30, 31 and 32 in Equations 35 and by terms 33, 34 and 35 in Equations 36. To better understand these terms consider the setting of flip-flops S_1 and K_1 with reference to Table V which is in essence a restatement of Table II in terms of flip-flop conduction states.

Table V

Situation	Old A_H flip-flop L_1	New A_H flip-flop S_1	New B_H from quantizer	S_1	K_1	Significance
1-----	0	0	0	1	0	Zero.
2-----	0	0	1	1	0	Do.
3-----	0	1	0	0	1	-10 feet.
4-----	0	1	1	1	1	+10 feet.
5-----	1	0	0	1	1	Do.
6-----	1	0	1	0	1	-10 feet.
7-----	1	1	0	1	0	Zero.
8-----	1	1	1	1	0	Do.

It will be noted from Table V that a change in the height

coordinate is indicated only by the situations 3 through 6. In situations 1, 2, 7 and 8 however, the signal flip-flop S_1 must be set to one, the reason for this requirement being that flip-flop S_2 must subsequently receive the contents of flip-flop S_1 , as will be described below, and a zero in flip-flop S_1 would lead to a logical error in the machine.

From Table V it will be seen that flip-flop S_1 should be set to one under the logical conditions

$$L_1'S_1B'_H + L_1S_1B_H + L_1S_1B_H + L_1S_1B'_H + L_1S_1B'_H + L_1S_1B'_H + L_1S_1R_H$$

these conditions simplifying to $L_1 + B'_H$. In a similar manner, the S_1 flip-flop should be zeroed under the logical conditions $L_1S_1B'_H + L_1S_1B_H$ which simplifies under the rules of Boolean algebra to $L_1B'_H$. By adding the conditions which specify the time interval during which these changes occur, the terms $P_1C_1C'_3C'_4B'_H + P_1C_1L'_1$ are specified for setting the flip-flop S_1 to its one state, and the term $P_1C_1C'_3C'_4B'_HL'_1$ is specified for setting flip-flop S_1 to zero. These logical terms will be recognized as terms 29, 32 and 33 in Equations 35 and 36.

The reason why no specific position word is specified by term 32 is that this term is operative during the first digit of position words X and Y as well as for word H. During the position words X and Y, however, quantizer signals B'_X and B'_Y are utilized in lieu of signal B'_H . Accordingly, terms 30 and 34 operate during the X position word to perform the same function as terms 29 and 33, while terms 31 and 35 are operative during the Y position words.

Consider now the function performed by terms 29, 32 and 33 of Equations 35 and 36 in setting up the flip-flops for the height coordinate. Whenever a change of either plus ten feet or minus ten feet is indicated, flip-flop K_1 is set to one by term 28 of Equation 33 as aforesaid. At this time, flip-flop S_1 should take its one-representing state when the quantizer feeds back to the computer a plus ten foot signal, and should take its zero-representing state when a minus ten foot indication is conveyed to the computer.

Recalling now that the new or present A_H signal is stored in flip-flop S_1 up until the end of the last digit of the velocity word H, it will be seen from Table V that for conditions 4 and 6, flip-flop S_1 is already in the proper state to represent the sign since the sign in these two situations is the same as the present A_H signal which is already stored in S_1 . Conversely, for conditions 3 and 5 the sign to be placed in flip-flop S_1 is represented by precisely the opposite conduction state utilized for representing the new A_H signal. In addition it will be noted further that conditions 3 and 5 are distinguishable from 4 and 6 in that B_H represents a zero during the former; since this in turn implies that the quantizer output signal B_H is at its high level, this signal may be utilized as a trigger function to reverse the state of flip-flop S_1 , as specified by terms 29 and 33. It should be noted, however, that term 33 includes the additional condition L'_1 which operates in conjunction with term 32 to assure that flip-flop S_1 is set to one under situations 2 and 7 when no change in coordinate is communicated from the quantizer.

Having set forth the manner in which the quantizer signals are set up in flip-flops K_1 and S_1 , consideration will now be given to the manner in which these signals are added to or subtracted from the binary numbers stored in the accumulator and servo registers in the position words H, X and Y. It will be recalled that the least significant digit of the accumulator has a scaled significance of 10 feet for the height coordinate and 5 meters for the X and Y coordinates. Accordingly, if K_1 is in its zero state at the start of the position word,

the accumulator number should be recirculated without modification; on the other hand if K_1 is in its one-representing state corresponding to a quantizer change of ± 10 feet or ± 5 meters, depending on the coordinate, then the contents of flip-flop K_1 should be either added to or subtracted from the number stored in the accumulator starting with the least significant digit, the operation of either addition or subtraction being specified by the state of the sign flip-flop S_1 .

It may be shown that the result of both binary addition and subtraction is specified by an identical logical equation for actuating a result flip-flop which stores the result, and that the difference in the two arithmetic operations is determined by controlling the state of the carry flip-flop utilized to store the carry of the operation. More specifically, the result of either adding or subtracting the digit stored in carry flip-flop K_1 from the sequential accumulator number digits presented by flip-flop L_1 is specified by terms 36 and 37 of Equations 31 and 32, respectively, the conditions $(L_1 + K_1)(L'_1 + K'_1)$ in term 36 and $(L_1 + K'_1)(L'_1 + K_1)$ in term 37 specifying that flip-flop M_1 which takes the result of the operation should be set to zero in flip-flops L_1 and K_1 are both in either their zero states or one states, and should be set to one if either flip-flop L_1 or flip-flop K_1 alone is in its one state. It should be noted here that the condition Q in terms 36 and 37 is not operative here since the computer is not engaged in either the Fit or Extrapolate routine, the terms being satisfied instead by the condition C_2 which specifies that the terms are operative during the position words even though neither Fit nor Extrapolate is being carried out. It should also be pointed out that the condition P'_1 in these terms specifies that no arithmetic operation is performed on the last bit of the word, while the condition K_1' in term 36 specifies that the arithmetic operation is suspended during the clear routine at which time it will be recalled, the M_1 flip-flop operates under the control of terms 14 and 13 in Equations 31 and 32, respectively.

Consider next the operation of carry flip-flops K_1 and the manner in which it is controlled for the operation of addition and the operation of subtraction. When the order is add, as specified by flip-flop S_1 being in its one state, it may be shown that the K_1 flip-flop will stay in its one state as the L_1 flip-flop presents the successive digits of the accumulator number until a binary digit of zero appears in the number. The first binary zero appearing in L_1 may of course be the least significant digit or a higher order digit; consequently the zeroing of flip-flop S_1 during addition may be expressed logically as $S_1L'_1$. Conversely, when the order is subtract as specified by flip-flop S_1 being in its zero state, the K_1 flip-flop should stay in its one state only until the first binary one is presented by flip-flop L_1 as the successive digits of the accumulator number appear; thus in subtract the zeroing of flip-flop K_1 may be expressed logically as S'_1L_1 . Combining terms from both add and subtract operations then gives the "or" function $S_1L'_1 + S'_1L_1$, which may be transformed according to the rules of logical algebra to the form $(S_1 + L_1)(S'_1 + L'_1)$. With reference then to term 38 of Equation 34 it will be seen that the foregoing condition specifies the mechanization for zeroing the carry flip-flop. It should be pointed out that of the other logical conditions in term 38, condition ⑥ specifies that this term is operative at all times except during the Fit routine, condition P'_1 specifies that it is not operative during the last digit interval of each word, and $(C_1 + C_2)$ specifies that the zeroing operation may take place during both the velocity word and position words. Since the velocity word in the L_1 channel at this time contains all zeroes, however, only condition C_2 which specifies the position words is of present interest.

At the same time that the quantizer output signals set

up in flip-flops S_1 and K_1 are being entered in the accumulator numbers, the same information is also being entered into the servo registers, as discussed previously with respect to FIG. 3. In adding the quantizer signal intelligence in the servo register number stored in channel L_2 , flip-flop K_2 functions as the carry flip-flop, flip-flop S_2 as the sign flip-flop, and flip-flop L_2 as the flip-flop which presents the successive digits of the servo register number.

The combining of the quantizer signals with the servo register number is complicated by one factor, namely, that the least significant digit of the servo register number has a scaled weight of 5 feet for the height coordinate and $2\frac{1}{2}$ meters for the X and Y coordinate, whereas the quantizer indicates a change in height as either ± 10 feet and a change in the X and Y coordinates as either ± 5 meters. It follows, therefore, that a change in coordinate position as indicated by the quantizer output signals must be added to or subtracted from the servo register number by operating upon the next to least significant digit of the servo register's binary number rather than upon the least significant digit as in the modification of the accumulator numbers described hereinbefore. Accordingly, at the beginning of the position words H, X and Y, the read flip-flop L_2 contains the least significant digit of the servo register number, which is merely shifted into flip-flop M_2 and re-recorded, as specified by terms 39 and 40 in Equations 37 and 38 respectively, the condition Q' specifying that neither Fit nor Extrapolate is being carried out while the condition P_1 represents the marker bit which occurs during the first digit of the position words.

At the same time that the foregoing operation takes place the contents of flip-flops S_1 and K_1 are shifted into flip-flops S_2 and K_2 respectively, these latter two flip-flops then performing the identical function in channel L_2 as is performed by flip-flops S_1 and K_1 in channel L_1 in controlling the arithmetic operation on the accumulator number. The reason for the shift into flip-flops S_2 and K_2 is that the information is not utilized in channel L_2 until the end of the second digit time interval of the position word, whereas the information is first utilized in channel L_1 during the first digit place of the position word and the K_1 flip-flop's contents may be erased at the end of the first digit time interval of the word.

The shift of this information occurs substantially as follows. Flip-flop S_2 is set to one at the end of the velocity words by term 41 of Equation 39. At the end of the following digit time interval, which is the first digit time interval of the position words, flip-flop S_2 is zeroed if flip-flop S_1 is zero, by term 42 of Equation 40; if flip-flop S_1 is in its one representing state, on the other hand, flip-flop S_2 is merely left in its one-representing state. The shift of the contents of flip-flop K_1 into flip-flop K_2 , in turn, is accomplished by terms 43 and 44 of Equations 41 and 42, respectively.

It will be recognized, therefore, that as the end of the second digit time interval of the position words H, X and Y approaches, flip-flops S_2 and K_2 contain the sign and change value from the appropriate quantizer while flip-flop L_2 now presents the next to least significant digit of the servo register number. Since this digit is scaled to the same value as the scaling of the quantizer signals, that is, 10 feet for the height servo register and 5 meters for the X and Y servo register, a straightforward binary addition or subtraction of the K_2 flip-flop contents may now be made with the L_2 flip-flop contents under the control of sign flip-flop S_2 which determined whether the operation is add or subtract.

Again as in the above-described arithmetic operation upon the accumulator number, the result signal of the arithmetic operation upon the servo register number may be specified by identical logical expressions regardless of whether the operation is add or subtract, the distinction between these operations being taken into account in con-

trolling the future behavior of the carry flip-flop K_2 . Thus whether the operation is add or subtract, terms 45 and 46 of Equations 37 and 38 specify the generation of the arithmetic result and the storing of the result in the L_2 channel. It will be noted that terms 45 and 46 are similar to terms 36 and 37 in Equations 31 and 32 described hereinabove, the condition P_1C_2 in terms 45 and 46 specifying that the arithmetic operation is carried out only after the first digit interval of the position word has been passed; thus the normal operation of terms 39 and 40 of Equations 37 and 38 in merely rewriting the first digit of the servo register numbers is assured.

The control of carry flip-flop K_2 at this time is also analogous to the control of the L_1 channel flip-flop K_1 described above, the K_2 flip-flop being zeroed if the order is add, as specified by the condition S_2 , and flip-flop L_2 presents a zero binary digit, or if the order is subtract as specified by the condition S'_2 and a one-representing signal is stored in flip-flop L_2 . These two situations are again expressible by the logical expression $(L'_2S_2 + L_2S'_2)$ which may be transformed to the logical expression

$$(L_2 + L_2)(L'_2 + S'_2)$$

This condition then is utilized to zero flip-flop K_2 , as specified by term 47 in Equation 42.

Another significant distinction between the arithmetic operations on the accumulator number and servo register number should also be mentioned at this time. More specifically, in the operation upon the accumulator number, flip-flop S_1 stays in its one or zero state representing add or subtract, respectively, throughout the operation upon the entire number. In operating upon the servo register number, however, flip-flop S_2 stays in its zero state representing subtract only so long as flip-flop K_2 is in its one state signifying there is still a carry digit to be subtracted. At the time that flip-flop K_2 is zeroed during the subtract operation by term 47 of Equation 42, the sign flip-flop S_2 is set to one as specified by term 48 of Equation 39, the remaining digits of the servo register number being processed as though the operation is add rather than subtract. Inasmuch as flip-flop K' has been zeroed, however, the digits presented by flip-flop L_2 are merely passed on to flip-flop M_2 without alteration and are re-recorded. The reason for switching the arithmetic control provided by flip-flop S_2 will be described in more detail hereinbelow with respect to the operation of the computer during the Fit routine. Briefly stated, however, this function is carried out to permit entry of an initial carry signal into the third digit of the servo register number under certain conditions when either the Fit or Extrapolate routine is being carried out.

Having thus described the manner in which the quantizer signals are entered arithmetically into the accumulators and servo registers, consideration will next be given to the operations which take place within the computer when the end of the position words H, X and Y are reached. During the last digit time interval of the position words, the most significant digits of the accumulator number and servo register number are stored in flip-flops M_1 and M_2 , respectively, and are being written into channels L_1 and L_2 . At this time during all routines except the reset routine the most significant digit of the servo register number is also picked off flip-flop M_2 and is communicated to the corresponding digital servo for controlling the direction of energization of its associated servomotor. The logical expressions which specify this transfer are given by terms 49, 50 and 51 of Equations 28, 29 and 30, respectively, representing the signals O_H , O_X and O_Y which are supplied to the digital servos as discussed hereinbefore with respect to FIGS. 3 and 7. In these terms the conditions setting up the conduction states of

flip-flops C_2 , C_3 and C_4 identify the three position words, the condition $\textcircled{R}$ identifies all time except the Reset routine, and the condition P_2 identifies the last digit time interval of the H and X words. The Y word, on the other hand, has its last digit time interval identified by the condition P_1P_2 in order to distinguish the origin mark interval, which occurs once every five difunction intervals, from the last digit interval.

At the same time that the servo output signals are generated by terms 49 through 51, the carry flip-flop K_1 in channel L_1 receives a zeroing signal as specified by term 52 in Equation 34; this term is utilized at all times except during the Fit routine to zero flip-flop K_1 if it has not been zeroed previously by term 38, the zoning assuring that a carry digit of one is not entered in the 2048 counters which follow position words H and X or the 4096 counter which follows position word Y.

The foregoing description of operation applies to the idle condition of the computer as identified by flip-flops Q and R being in their zero states, and to the dawdle condition identified by a zero stored in flip-flop Q and a one in flip-flop R. It will be seen from the description set forth hereinbelow that the dawdle condition of the computer is encountered after the Fit routine before the Extrapolate routine is initiated, and after the Extrapolate routine before the Reset routine is initiated.

Consider next the operation of the computer when the associated radar signals that a projectile is being tracked. It will be recalled from FIG. 7 that the receipt of signal F_R by the front panel controls results in a high level voltage being placed on conductor $\textcircled{R}$, a low level signal being placed on conductor $\textcircled{S}$, and a pulse signal being transmitted to the logical gating network on conductor $(F\text{-pulse})$. It should be noted here that this pulse lasts for more than one drum revolution and thus is present during the occurrence of at least one origin pulse.

Upon receipt of the $(F\text{-pulse})$ indicating that a projectile is being tracked, the computer remains in its idle condition until the origin mark 800 in FIG. 8 is presented by the P_2 flip-flop. At this time flip-flop Q is set to its one-representing state by term 52 of Equation 24, the conditions $P_1P_2C_2$ defining the origin pulse while the condition R' defines that the computer is not in its dawdle state. The final "or" condition in term 52 is not utilized or necessary at this time.

The setting of flip-flop Q to its one-representing state thus initiates the Fit routine which is utilized as described hereinbefore for processing precisely 4096 difunction signals for each coordinate. In order to accomplish this function, the three 2048 counters and the 4096 counter are all rendered operative on the memory recirculation immediately following the setting of flip-flop Q. More specifically, at the end of the last digit time interval of the Y position word immediately following the origin mark, flip-flop K_1 is set to its one-representing state by term 53 of Equation 33, this term being operative at the end of each position word thereafter throughout the Fit routine to set up a binary one in flip-flop K_1 so that it may be added into the count stored in the counter which follows immediately, to thereby increase its count. Thus term 53 sets up an "add one" signal for the 4096 counter and for the 2048 counters which follow the H and X position words. The "add one" signal for the 2048 counter in the $\ddot{H}$ acceleration word, on the other hand, is furnished by term 54 of Equation 33 which sets flip-flop K_1 to one at the end of the g word. As will be disclosed below, term 54 also sets flip-flop K_1 to one at the end of

the acceleration words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ in preparation for entering the difunction signals from the radar into the velocity word integrators.

Continuing with the description of the counter operation, it will be recognized that sign flip-flop S_1 should be set to one for the operation on each counter since the binary one stored in flip-flop K_1 is always added to the count in the counters; the entry of the sign also occurs automatically at the end of the H, X and Y position words, and is specified by term 55 of Equation 35. It should be noted here that term 55, unlike term 53 for flip-flop K_1 , is sufficient to provide the addition signal for the 2048 counter in the $\ddot{H}$ word as well as for the other counters, the reason being that during the Fit routine the sign stays in flip-flop S_1 each time it is set to one until the end of the following velocity word when it is again employed to receive the sign of the associated quantizer input signals as previously described.

Continuing, as the successive digits of the numerical counts stored in the counters appear in flip-flop L_1 they are combined with the signal stored in carry flip-flop K_1 and are then returned to flip-flop M_1 to be re-recorded, the entry of the result in flip-flop M_1 being specified by the previously described terms 36 and 37 of Equations 31 and 32. It will be appreciated, however, that the condition in these terms which enables their operation is the condition Q, since an arithmetic operation is taking place in all words of channel L_1 and not merely the position words.

As in the previous situations where addition or subtraction is carried out, means are also provided for zeroing the L_1 channel carry flip-flop as soon as no carry is to be propagated to a higher digit in the number being operated upon. The zeroing of the K_1 flip-flop is thus specified by term 56 of Equation 34. Two factors about this term should be noted, namely, that it includes subtractor logic as well as adder logic even though the counters only use the addition function, and secondly, that this term is operative in all words and takes the place of the previously described term 38 for operating on the position and velocity words during the Fit routine. It is in its operation during the position words as previously described, and during the velocity words as described below, that the subtractor logic of term 56 becomes operative.

Consider next the operation of the computer during the velocity words of the Fit routine, and the manner in which the 2048 counters control the entry of the difunction signals into the integrand registers of the velocity integrators. It will be recalled from the derivation of difference Equations 11, 14 and 15 set forth hereinbefore that the velocity V_H , V_X and V_Y may be obtained by scanning the second group of 2048 signals in each input difunction train and subtracting therefrom the sum of the first group of 2048 signals in the train. Owing to the fact that the first group of signals are received before the second group, however, it was necessary to transform the initial form of Equations 11, 14 and 15 into the their final form where velocity is expressed negatively, so as to utilize the groups of difunction signals as they become available. In the specific embodiment of the invention here being described it has been found preferable to solve the difference equations by utilizing the complements of the difunction signal trains, since the solutions may then be obtained by summing the complements of the first group of 2048 difunction signals, and subtracting therefrom the sum of the complements of the second group of difunction signals. Since subtracting the complement of a signal is identical with adding the signal, the computer herein disclosed functions in reality to first sum the complements of the first 2048 difunction signals, and then to add to this sum the sum of the second group of 2048 uncomplemented difunction signals.

The timing pulses TP_H , TP_X and TP_Y which are utilized for actuating the analog-to-difunction converters

to produce the difunction input signal trains are generated continuously within the logical gating matrix, but of course create no useful intelligence feedback to the computed until the Fit routine is carried out. The timing pulses for each coordinate are generated by mechanizations of terms 57, 58 and 59 of Equations 43, 44 and 45, respectively, the pulses generated by term 57 being transmitted to the height converter at the end of the position word Y while the pulses generated by terms 58 and 59 are transmitted to the X and Y coordinate converters at the very end of the velocity words H and X. It should be pointed out that the use of three different timing pulses is not necessary essential, since a single timing pulse could be used with three analog-to-difunction converters of the type shown in FIG. 2 of the aforementioned U.S. patent application Serial No. 540,699 to Hansen; if however the converters are similar in operation to that shown in Hansen's FIG. 4, three different timing signals should be transmitted to the converters.

Returning now to the manner in which difference Equations 11, 14 and 15 are mechanized, the individual difunction signals are entered into flip-flop K₂ during the next to last bit of the acceleration words H, X and Y as specified by terms 60, 61 and 62 of Equation 41 the flip-flop being set to one if the difunction complement signal being entered represents -1 and remaining in its zero state if the input difunction signal is at its low level representing a +1. That flip-flop K₂ will be in its zero state at the time the difunction signal is entered in flip-flop K₂ is assured by term 63 of Equation 42 which specifies that the flip-flop should be zeroed at the end of each of the position words H, X and Y when the computer is in its compute condition as signified by flip-flop Q being in its one-representing state. It will be recognized that term 63 is operative at the very beginning of the Fit routine and first applies a zeroing signal to flip-flop K₂ in the digit time interval immediately following the initial setting of flip-flop Q at the start of the Fit routine.

In entering the difunction signals into the velocity word it will be appreciated from what has been said before that the sign of the arithmetic operation is determined not only by the sign of the difunction signal, but whether the 2048 counter immediately preceding the velocity word specifies that the first 2048 signals are being received or whether the last group of 2048 signals are being received. More specifically, the sign of flip-flop S₁ is set up at the end of the acceleration words H, X and Y one digit time interval after the appropriate difunction signal has been entered in flip-flop K₂, by term 64 of Equation 36 which if satisfied specifies that flip-flop S₁ should be zeroed to subtract a binary one from the integrand number, and if unsatisfied leaves flip-flop S₁ in its one state to which it was set by term 55 at the end of the prior position word, thereby specifying that a binary one should be added. At the same time that term 64 is operative, namely at the last digit of the acceleration words, term 54 of Equation 33 is operative as described previously to set flip-flop K₁ to its one-representing state to provide the binary one which is either added or subtracted from the velocity word integrand number whose least significant digit appears in flip-flop L₁ during the following digit time interval.

The logical conditions expressed in term 64 will be more fully understood from Table VI below which indicates the count stored in the 2048 counters at the end of the various difunction intervals and the manner in which it is used to control the sign flip-flop. In this operation the count is determined by looking at the most significant digit of the newly formed count when it is stored in flip-flop M₁ to be re-recorded at the end of the accelera-

tion words, and by looking at the contents of flip-flop S₂ which is utilized as a one-digit delay for storing the successive carry digits set up in flip-flop K₁ during the count operation. The logical functions which specify the shift from flip-flop K₁ to S₂ are set forth in terms 65 and 66 of Equations 39 and 40, respectively.

Table VI

Difunction interval count	Binary change during difunction interval	M ₁	S ₂	K ₂	S ₁
1-----	0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0 (Sub).
	to				
15-----	0 0 0 0 0 0 0 0 0 0 0 1			1	1 (Add).
2048-----	0 1 1 1 1 1 1 1 1 1 1 1	1	1	0	0 (Sub).
	to				
20-----	1 0 0 0 0 0 0 0 0 0 0 0			1	1 (Add).
2049-----	1 0 0 0 0 0 0 0 0 0 0 0			0	1 (Add).
	to				
25-----	1 0 0 0 0 0 0 0 0 0 0 1	1	0	1	0 (Sub).
4096-----	1 1 1 1 1 1 1 1 1 1 1 1			0	1 (Add).
	to				
	0 0 0 0 0 0 0 0 0 0 0 0	0	1	1	0 (Sub).

As pointed out above, flip-flop S₁ is already in its one-representing state at the end of the acceleration words owing to the operation of term 55 of Equation 35, and hence only a zeroing signal is required to set the flip-flop to its proper state when the order is subtract. From Table VI the subtract conditions are given as

$$M'_1 S'_2 K'_2 + M_1 S_2 K'_2 + M'_1 S'_2 K_2 + M'_1 S_2 K_2$$

which may be rewritten in the form

$$(M'_1 + S'_2 + K'_2)(M_1 + S_2 + K'_2) \\ (M_1 + S'_2 + K_2)(M'_1 + S_2 + K_2)$$

Combining this logic with the condition

$$\bar{P} P_1 C'_1 C'_2 (C'_3 + C'_4)$$

which specifies the last digit of the acceleration words H, X and Y during the Fit routine, thereby gives term 64 of Equation 36.

Having thus set up the sign in flip-flop S₁ and a binary one in the carry flip-flop K₁, the individual difunction signals are entered into the velocity word integrand registers by the previously described term 56 in Equation 34 and terms 36 and 37 in Equations 31 and 32. Consequently the control of sign flip-flop S₁ and its reversal after the count 2048 has been passed assures that difference Equations 11, 14 and 15 are solved in the computer during the Fit routine.

Consider now the operation on the accumulator numbers and servo register numbers during the Fit routine. It will be recalled from the description of FIG. 3 hereinabove that the difunction signals from the radar are entered into the appropriate servo registers in order to set up the three midpoint position coordinates defined by Equations 10, 12 and 13. It will also be recalled, however, that the complement of each difunction signal rather than the signal itself was stored in flip-flop K₂ at the end of the acceleration words. Since the difunction signal's complement is no longer required after being utilized in the solution of Equations 11, 14 and 15, the first operation performed in preparing for entry of the difunction signal into the associated servo register is to trigger flip-flop K₂ so that it reverses its state and thus presents the difunction signal rather than its complement. The triggering of flip-flop K₂ takes place at the end of the next to last digit space of the velocity words when the difunc-

tion signal complement is no longer needed to control sign flip-flop S_1 , and is specified by the identical terms 67 and 68 in Equations 41 and 42, respectively.

It will be remembered from the description of FIG. 3 hereinabove that the output signals from the quantizers are also arithmetically entered into the servo registers at the same time that the difunction signals are entered. In this respect it will be recalled from the description of the computer's idle condition that the quantizer signals are entered in flip-flops S_1 and K_1 at the end of the velocity words. As previously mentioned, this operation is continuous throughout all routines including Fit and Extrapolate, as is the operation of entering the quantizer signals into the accumulator registers. In entering these signals into the accumulator there is one slight variation in the logic employed, namely, term 56 of Equation 34 is utilized for zeroing the K_1 flip-flop instead of term 38. The operation performed, however, is identical.

Returning now to the entry of the quantizer signals and difunction signals into the servo registers, the following Table VII is a corollary of Table V set forth above and indicates the manner in which flip-flops S_2 , K_2 and M_2 are set up during Ft and Extrapolate when flip-flop Q is in its one-representing state and flip-flop K_2 includes input signals to be entered in the registers.

Table VII

[Compute = Q]

Situation	S_1	K_1	Signif., ft.	K_2	Signif., ft.	L_2	Signif., ft.	S_2	K_2	M_2	Total signif., ft.
1	1	0	0	0	-5	0	0	0	1	1	-5
2	1	0		0		1	+5	1	0	1	0
3	1	0		1		0	0	1	0	1	+5
4	1	0		1		1	+5	1	0	1	+10
5	0	1	-10	0	-5	0	0	0	1	0	-15
6	0	1		0		1	+5	0	1	0	-10
7	0	1		1		0	0	0	1	1	-5
8	0	1		1		1	+5	0	1	1	-5
9	1	1	+10	0	-5	0	0	1	0	0	0
10	1	1		0		1	+5	1	0	1	+5
11	1	1		1		0	0	1	1	1	+10
12	1	1		1		1	+5	1	1	1	+15
								0	0	0	+20

It should be noted first that although the foregoing table refers to the height coordinate and expresses distance in integral multiples of 5 feet, the same table applies equally well to the X and Y coordinates except that $2\frac{1}{2}$ meters, 5 meters, $7\frac{1}{2}$ meters and 10 meters then have the same significance as 5 feet, 10 feet, 15 feet and 20 feet in Table VII.

In mechanizing the functions set forth in the above truth table it will be recognized that flip-flop M_2 is always set to the conduction state opposite to that of flip-flop L_2 , to thereby record the least significant digit of the new servo register number. This operation is specified by terms 69 and 70 of Equations 37 and 38, respectively.

The mechanization for setting up flip-flop K_2 , on the other hand, is different in that for situations 2, 4, 5, 7, 9 and 11 in Table VII the flip-flop may be left alone since the flip-flop's final state during the second digit interval of the position word is identical to its state during the first digit interval of the word. For situations 1 and 3, however, when flip-flops K_1 and L_2 are both in their zero states, the state of flip-flop K_2 is reversed, this operation being specified by the identical triggering terms 71 and 72 in Equations 41 and 42, respectively. Similarly, when situations 6, 8, 10 and 12 are presented, flip-flop K_2 should be triggered to reverse its conduction state, these four situations being distinguishable from all of the rest by the fact that flip-flops K_1 and L_2 both are in their one-representing states; the mechanization of this function is specified by terms 73 and 74 of Equations 41 and 42.

Flip-flop S_2 , on the other hand, is preset to its one-representing state during the last digit time interval of the

velocity words by term 41 of Equation 39 as previously described, and is zeroed when situations 1, 5, 6, 7 and 12 of Table VII are presented, and is left in its one-representing state for all other situations. It will be noted that situations 1, 5, 6 and 7 all signify a subtract operation whereby the servo register number is to be decreased by a predetermined amount, while situation 12 signifies the addition of 20 feet if it occurs when operating on the height coordinate or 10 meters when operating on the X or Y coordinates. It will also be noted that situation 1 is distinguished by flip-flops L_2 , K_1 and K_2 all being in their zero states, that situations 5, 6 and 7 are distinguishable by the fact that flip-flop S_1 is zeroed when either flip-flop K_2 or flip-flop L_2 is zeroed, and that situation 12 is distinguishable by the fact that flip-flop K_1 , K_2 and L_2 are all in their one-representing states. Thus in the mechanization of the computer, term 75 of Equation 40 specifies the zeroing of flip-flop S_2 for situation 1, term 76 specifies the zeroing for situations 5, 6 and 7, and term 77 specifies the zeroing for situation 12.

After flip-flops S_2 , K_2 and M_2 have been set up at the end of the first digit interval of the position words, as specified above, the contents of carry flip-flop K_2 are added to or subtracted from the successive digits presented by flip-flop L_2 under the control of the sign stored in sign flip-flop S_2 . For situations 1 through 11 of Table VII the arithmetic operation is carried out in the same manner described hereinabove with respect to the computer's idle conditions, terms 45 and 46 of Equation 37 and 38 specifying the result digits, while term 47 of Equation 42 specifies the zeroing of the carry flip-flop K_2 for both add and subtract operations. It should also be recalled that when the operation is subtract, then flip-flop S_2 is normally zero but is returned to its one-representing state by term 48 of Equation 39 at the same time that flip-flop K_2 is zeroed by term 47. The purpose of this operation will be understood from the description below of the computer's operation when situation 12 of Table VII is presented.

When situation 12 is presented, input signals totaling 15 feet are to be added to a servo register number whose least significant digit is a binary one representative of 5 feet. Consequently the addition process must present a carry digit of one to be added into the third digit of the zero register number, since this digit has a scaled significance of 20 feet. In same operation, of course, the binary one in the least significant digit of the servo register is rewritten as a zero, as set forth in Table VII by the fact that flip-flop M_2 is set to zero. The second digit of the servo register number is then merely re-recorded unaltered by the action of terms 45 and 46 of Equations 37 and 38 since flip-flop K_2 is zeroed in situation 12 of Table VII.

At the end of the second digit time interval of the position word, however, flip-flops S_2 and K_2 must be set to one when situation 12 of Table VII is presented to thereby add a binary one into the third digit of the servo register number. The setting of flip-flop S_2 to its one-representing state is specified by term 78 of Equation 39 which stipulates that S_2 should be set to one during the position words whenever carry flip-flop K_2 is zero following the operation on the first digit of the servo register number and the L_1 channel sign flip-flop S_1 is in its one-representing state.

At the same time the carry flip-flop K_2 is set to its one-representing state by term 79 of Equation 41 which stipulates that flip-flop K_2 should be set to one during the position words whenever sign flip-flop S_2 is zero following the operation on the first digit of the servo register number. It is at this time that the true significance of term 48 of Equation 39 can be appreciated, since term 48 forces flip-flop S_2 to its one-representing state during sub-

tract operations when flip-flop K_2 is being zeroed by term 47. If this were not done, then term 79 of Equation 14 would be operative falsely to reset flip-flop K_2 to its one state whenever it was zeroed during a subtract operation on the servo register number.

After flip-flops K_2 and S_2 are set to one the conventional additive process previously described is carried out to add the contents of flip-flop K_2 into the third digit of the servo register number, the K_2 flip-flop thereafter being utilized to propagate any carry digits produced to the next higher digit of the number. It is important to note at this point that the aforementioned operations on the position word servo registers are not restricted to the Fit routine, but are operative during both the Fit and Extrapolate routines as identified by flip-flop Q being in its one-representing state. As will be described in more detail below, the one basic distinction in the application of Table VII to the Extrapolate routine in lieu of the Fit routine is that flip-flop K_2 there initially holds the overflow difunction signals from the preceding integrator rather than the difunction input signals from the radar.

It should be understood, of course, that terms 49, 50 and 51 of Equations 28 through 30 continue to supply the appropriate digital servos with the output signals from the servo registers during the Fit routine in the same manner as previously described for the computer's idle condition. Moreover, the various operations outlined above continue to be performed once per recirculation of the L_1 and L_2 channels until the 4096 counter indicates that 4096 recirculations have occurred and that consequently the Fit routine should be terminated.

Considering now the termination of the Fit routine, as the L_1 and L_2 channels start their 4096th recirculation, the 4096 counter contains twelve consecutive binary ones representative of the number 4095 corresponding to the number of difunction intervals which have elapsed since the Fit routine was initiated. During this final recirculation of the Fit routine, therefore, the carry digit initially set up in flip-flop K_1 by term 53 of Equation 33 is propagated throughout the count and manifests itself finally as a carry digit of one from the most significant digit of the count; stated differently, the arrival at the count of 4096 is indicated by the fact that flip-flop K_1 is still in its one-representing state during the last digit time interval of the g acceleration word. This condition is then utilized to set flip-flop R to its one-representing state as specified by term 80 of Equation 26.

Thereafter the computer continues to operate in the Fit routine for the remainder of the difunction time interval until the end of the Y position word at which time the Q flip-flop is zeroed by term 81 of Equation 25 which specifies that Q should be zeroed when the routine is Fit and the end of the Y position word is reached. This in turn returns the interval operation of the computer to the dawdle condition since flip-flop Q is returned to its zero state, the R flip-flop being zeroed during the following digit time interval by term 82 of Equation 27. Accordingly, as the L_1 and L_2 channels are recirculated during the following difunction interval the computer is returned once more to the idle condition previously described. In addition, the zeroing of flip-flop Q is transmitted to the computer's front panel controls wherein it functions to release the Fit relay and to once more place a high level voltage on conductor ⑤ and a low level voltage on conductor ⑥.

It will be recognized that the velocities V_H , V_X and V_Y have now been determined from the evaluation of the difference equations and are now stored in the integrand registers in channel L_1 in the words H , X and Y , respectively. In addition, the coordinates of the projectile's midpoint M in FIG. 1 have been entered in the servo registers of the position words, it being understood that this particular intelligence is being utilized continuously to control the digital servos so that the feedback from

the servos reduces the magnitude of the numbers stored in the servo registers. While this is being done, it will be remembered, the feedback from the digital servos is also being stored simultaneously in the appropriate accumulator registers so that there is always an inherent memory of how far the servo counters have been driven from the initial radar coordinates stored therein.

At the conclusion of the Fit routine the release of the Fit relay in the front panel controls as above-described provides a visual indication through Fit lamp 732 in FIG. 7 that the Fit routine has been completed and that the Extrapolate routine may be commenced at any time to extrapolate the trajectory equations to determine either the projectile's firing point or impact point. It should be pointed out here that the Extrapolate routine may be initiated at once without waiting until the servo register numbers have served the servo counters to the coordinates of the midpoint of the projectile during the Fit interval.

Recall now that the Extrapolate routine is initiated by switching one of the three extrapolate switches in FIG. 7 to either its forward or back position. When this is done, flip-flop Q is set to one upon the next appearance of the origin mark 800 in FIG. 8, this operation being specified by term 52 of Equation 24 where the condition $R'P_1P_2C_2$ represents the appearance of the origin mark during idle and the condition ③

$$(1\text{-cycle down}) + (5\text{-cycle down}) + (\text{continuous down})$$

represents the actuation of an extrapolate switch when the computer is not in the Fit routine.

Consider now the operations carried out during the various word times during a recirculation of the L_1 and L_2 channels in the Extrapolate routine. During the last digit time interval of the Y position word, or in other words, immediately following the setting of flip-flop Q to its one-representing state, sign flip-flop S_2 for channel L_2 is set to one if the Extrapolate is to be forward in time to determine impact point, and is set to zero if Extrapolation is to be backward in time to determine the projectile's firing point, these functions being specified by terms 83 and 84 of Equations 39 and 40, respectively. Thus the S_2 flip-flop is set to control the arithmetic transfer of the constant g stored in channel P_2 to the overflow register of integrator 367 in channel L_2 , the operation being add if S_2 is in its one-representing state and subtract if S_2 is in its zero state. At the same time that flip-flop S_2 is set by terms 83 and 84, carry flip-flop K_2 is zeroed by the previously described term 63 of Equation 42.

As the g word is thereafter processed, the constant g is either added to or subtracted from the overflow register number appearing in flip-flop L_2 , the operation being controlled by sign flip-flop S_2 while the result of the operation is stored in flip-flop M_2 . This operation will be recognized by those familiar with digital computers as being one of either full addition or full subtraction in which two binary numbers are either added or subtracted and in which carry flip-flop K_2 is utilized to store the carry from the operation on each of the successively weighted digits of the binary number.

It is well known in the digital computer art that the logical functions specifying addition or subtraction may be expressed by the same logical equations, the difference in the operations being controlled by varying the input functions to the carry flip-flop. Thus for both addition and subtraction, where the result is to be put in flip-flop M_2 to be recorded in channel L_2 , it may be shown that flip-flop M_2 should be set to one for the logical conditions $L_2P_2K'_2 + L_2P_2K_2 + L_2P'_2K_2 + L_2P_2K_2$, and should be zeroed for the logical conditions

$$L'_2P_2K_2 + L_2P'_2K_2 + L_2P_2K'_2 + L'_2P'_2K'_2$$

Simplifying these expressions then gives the function

$P_2(L_2+K_2)(L_2+K_2)+P_2'(L_2+K_2)(L_2+K_2)$ for the set to one operation, and the function

$$P_2(L_2+K_2)(L_2+K_2)+P_2'(L_2+K_2)(L_2+K_2)$$

for the zeroing operation. Adding then to each of these terms the logical condition $\textcircled{B} QC_1C_2$ which specifies all four acceleration words during the Extrapolate routine thus derives terms 85 and 86 of Equation 37 and terms 87 and 88 of Equation 38.

It is important to note here that the logical condition C_1C_2 defines all four acceleration words, and not merely the g word. The reason for not specifically identifying the g word is that these same terms 85 through 88 are also utilized in acceleration words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ for respectively arithmetically transferring the drag constants K_H , K_X and K_Y to the overflow registers of integrators 366, 390 and 394.

In a similar manner the logical functions which control the operation of carry flip-flop K_2 are identical for all four acceleration words, the carry functions being specified by terms 89 and 90 of Equations 41 and 42, respectively, wherein the condition $\textcircled{B} P_1C_1C_2Q$ identifies all digit time intervals but the first in each of the acceleration words during the extrapolate routine. The remaining logical conditions of terms 89 and 90 specify the actual arithmetic operations when flip-flop K_2 should be set to one or zeroed; for example, the condition

$$P_2(L_2+S_2)(L_2+S_2)$$

of term 89 may be transformed to $P_2L_2S_2+P_2L_2S_2'$ which signifies that K_2 should receive a set to one signal whenever the operation is add and both the L_2 and P_2 flip-flops contain binary ones, or when the operation is subtract and flip-flops P_2 and L_2 contain a binary one and zero, respectively. Conversely, the remainder of term 90 transforms to $P_2'L_2S_2+P_2'L_2S_2'$ which specifies that flip-flop K_2 should be zeroed whenever flip-flops L_2 and P_2 both contain zeroes and the order is add, or when flip-flop P_2 contains a zero and flip-flop L_2 a binary one and the order is subtract. It will be recognized by those familiar with digital computational techniques, therefore, that terms 89 and 90 specify the complete logic for controlling the carry flip-flop K_2 for both full addition and full subtraction.

Considering next the operation of the computer at the end of the g word, it will be recalled from FIG. 3 that the overflow from integrator 367 is one of two input signals applied to integrator 365. It is obvious from FIG. 8, however, that the integrand registers of integrator 365 is not available to receive an input signal until the $\ddot{H}$ word is reached, and that means must be provided for storing the difunction output signal from integrator 367 throughout the $\ddot{H}$ word. In the particular embodiment of the computer here shown this is accomplished by storing the difunction output signal in flip-flop K_1 at the end of the g word, flip-flop K_1 being set to one by term 91 of Equation 33 if the difunction signal represents a plus one, and being left in its zero state to which it has been preset by terms 52 of Equation 34 if the difunction output signal from integrator 367 represents a minus one. Term 91 will be recognized as specifying that a plus one difunction output signal is produced whenever the order is add (S_2) and a carry is propagated from the overflow register (K_2), or the order is subtract (S_2') and no carry is propagated from the overflow register (K_2').

At the time that the K_1 flip-flop is set up to take the overflow difunction from the g word integrator, carry flip-flop K_2 is again zeroed preparatory to being utilized in the arithmetic transfer in the $\ddot{H}$ word integrator, this operation being specified by term 92 of Equation 42. It should be noted that this term will also be operative at

the end of the H , X and Y words to zero flip-flop K_2 for operating upon the integrators in velocity words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$. The zeroing of flip-flop K_2 preparatory to operating on the acceleration words $\ddot{X}$ and $\ddot{Y}$, however, is provided by the previously described term 63 which also zeroed flip-flop K_2 prior to the start of the g word.

It will be recalled from FIG. 3 that the operand signals which control the arithmetic transfer in integrators 366, 390 and 394 are taken from the associated velocity word integrators 365, 388 and 392, respectively. It is apparent from FIG. 8, however, that the integrators which provide the operand signals occur later in time than the acceleration word integrators, and that it is therefore necessary to store the difunction output signals from the velocity word integrators in some manner so that they may be utilized as operand input signals to the acceleration word integrators during the succeeding difunction interval. In the particular embodiment of the invention herein disclosed in detail flip-flops I_H , I_X and I_Y are utilized for performing this function, and as will be disclosed hereinbelow, are set to one when its associated velocity word integrator produces a plus one difunction output signal and are left at zero if a minus one difunction output signal is received.

At the end of the g word and at the end of position words H and X , therefore, the contents of flip-flops, I_H , I_X and I_Y are utilized to set the sign flip-flop S_2 to control the arithmetic operations on the $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ acceleration word integrators. With reference now to Equations 39 and 40, terms 93 and 94 specify the setting up of flip-flop S_2 at the end of the g word in preparation for operation on the $\ddot{H}$ word integrator, terms 95 and 96 specify the setting up of sign flip-flop S_2 at the end of the H position word preparatory to operating on the $\ddot{X}$ word integrator and terms 97 and 98 specify the setting up of sign flip-flop S_2 at the end of the X position word preparatory to operating on the $\ddot{Y}$ word integrator. As the acceleration word are thereafter processed, terms 85 through 88 function in the manner previously described to store the result of the arithmetic operation in flip-flop M_2 , while terms 89 and 90 of Equations 41 and 42 function to control the carry flip-flop K_2 under the control of the sign flip-flop S_2 as previously described.

The operation of the specific computer herein disclosed at the end of the $\ddot{H}$ acceleration word differs from the operation at the end of the $\ddot{X}$ and $\ddot{Y}$ acceleration words owing to the fact that the overflow difunction signals from both the g word integrator and $\ddot{H}$ word integrator must be combined before being entered into the integrand register of the $\ddot{H}$ velocity word integrator. It will be remembered that at the end of the g word flip-flop K_1 was set to one if the overflow difunction from integrator 367 was a plus one, and was left in its zero state if the overflow difunction represented a minus one. The manner in which the difunction overflow from the $\ddot{H}$ word integrator is combined with the previously stored overflow from the g word integrator will now be described with reference to the following Table VIII.

Table VIII

Output integrator 367	Flip- flop, K_1	Output integrator 366	Flip-flops		Sum result	Flip-flops	
			K_2	S_2		K_1	K_1
+1	1	+1	1	1	+1	1	0
+1	1	-1	0	0	0	0	-----
-1	0	+1	0	1	0	0	-----
-1	0	-1	1	0	-1	1	1

As shown in Table VIII, if the output difunction signals from integrators 366 and 367 both represent +1, a binary one is subtracted from the H word integrand register by setting flip-flops K_1 and S_1 to their one and zero representing states respectively, whereas a binary one is added to the integrand register by setting flip-flop K_1 and flip-flop S_1 to one when both of the acceleration word integrators present signals representing -1. Conversely, when the output difunction signals are different, flip-flop K_1 is zeroed so that nothing is added to the integrand register, the sign stored in flip-flop S_1 being immaterial at these times. The reason for subtracting when the acceleration word integrator produces a plus one output signal and for adding in response to a minus one output signal is the fact that drag and gravity are both negative accelerations, the foregoing complementing operation thus being utilized to provide the negative signs which appear in Equations 3, 7 and 8.

From the foregoing table the set to one function of flip-flop K_1 may be expressed as

$$K_1(K_2S_2 + K'_2S'_2) + K'_1(K'_2 + K_2S'_2)$$

which simplifies to $K'_2S_2 + K_2S'_2$, or stated differently, $(K_2 + S_2)(K'_2 + S'_2)$. In a similar manner the zeroing function for flip-flop K_1 may be expressed as

$$K_1(K_2S'_2 + K'_2S_2) + K'_1(K_2S_2 + K'_2S'_2)$$

which also simplifies to $K'_2S_2 + K_2S'_2$, or in other words $(K_2 + S_2)(K'_2 + S'_2)$. The two foregoing simplified logical conditions are set forth in terms 99 and 100 of Equations 33 and 34, respectively, which in essence function to leave flip-flop K_1 alone when the contents of flip-flops K_2 and S_2 are the same, and to trigger flip-flop K_1 to reverse its state when the contents of flip-flops K_2 and S_2 are different.

In an analogous manner it may be seen from Table VIII that the proper sign will be set up in flip-flop S_1 if it is set to one when the contents of flip-flops K_2 and S_2 are different and zeroed when the contents are the same. This operation is in turn specified by terms 101 and 102 of Equations 35 and 36, respectively.

It should be noted here that terms 101 and 102 apply to all acceleration words since all drag factors are negative, and are thus utilized to enter into the integrand registers in velocity words $\ddot{X}$ and $\ddot{Y}$ the complement of the sign of the overflow difunctions from the integrators in acceleration words $\ddot{X}$ and $\ddot{Y}$. That this may be done is also apparent from Table VIII which shows that the sign set up in flip-flop S_1 for the $\ddot{H}$ velocity word operation is independent of the prior contents of flip-flop K_1 . It should also be apparent that since a plus one or minus one entry is always made in the integrand registers in velocity words $\ddot{X}$ and $\ddot{Y}$ during the Extrapolate routine, carry flip-flop K_1 is merely set to one at the end of acceleration words $\ddot{X}$ and $\ddot{Y}$ and does not require a complex equation such as is required at the end of the height acceleration word $\ddot{H}$. Thus term 103 of Equation 33 specifies the setting of the S_1 flip-flop to one during the Extrapolate routine during the last digit time interval of acceleration words $\ddot{X}$ and $\ddot{Y}$.

It will be recalled that the operand signal for operating on the integrators in the velocity words is merely a $\pm dt$ for extrapolating forward or backward in time. Thus flip-flop S_2 is actuated in the same manner for the velocity words as it was for the acceleration word g , namely, by being set to one if the extrapolation is to be forward in time, and to zero if the extrapolation is backward in time. Looking then to the equations, this function of flip-flop S_2 is entered by terms 104 and 105 of Equations 39 and 40, respectively, which specify that the S_2 flip-flop should be set up during the last digit time interval of the accel-

eration words. It should be noted that these terms are not restricted to just the $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ acceleration words, but could also operate at the end of the g word when, it will be remembered, flip-flop S_2 is set up by terms 93 and 94. Terms 104 and 105 are ineffective at this time, however, owing to the fact that the state specified by the operative one of these terms is already preexisting in flip-flop S_2 by virtue of the action of terms 83 and 84 at the end of the previous Y position word. Hence terms 93 and 94 alone function to set up flip-flop S_2 at the end of the g word, while terms 104 and 105 are inherently restricted to setting up flip-flop S_2 at the end of acceleration words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$. Consider now the arithmetic processes carried out during the Extrapolate routine on the velocity $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$. The entry of the integrand input signals set up in carry flip-flop K_1 and sign flip-flop S_1 are accomplished by terms 36 and 37 in Equations 31 and 32 and by term 38 of Equation 34 in the same manner described for the computer's idle condition, the only difference being that the condition, C_1 in term 38 is the condition which enables its operation during the velocity words. The arithmetic transfers performed in the velocity words, on the other hand, are slightly different from those performed during the acceleration words owing to the fact that the integrand registers for the velocity word integrators are stored in channel L_1 instead of channel P_2 as in the case of the acceleration word integrators. Thus the full adder and full subtractor result terms specified by terms 85 through 88 of Equations 37 and 38 are replaced during the velocity words by terms 106 through 109. It will be recognized that these latter terms identify the velocity words instead of the acceleration words, and that the conditions P_2 and P'_2 in terms 85 through 88 are replaced by the conditions L_1 and L'_1 , respectively, in terms 106 through 109. The manner in which these velocity word terms are derived is identical with that discussed hereinabove for terms 85 through 88.

In a similar manner, the control of carry flip-flop K_2 for the full addition or subtraction during the Extrapolate routine on the velocity words is provided by terms 110 and 111 of Equations 41 and 42 instead of terms 89 and 90. Again the principal distinction between terms 110 and 111 and terms 89 and 90 is in the fact that terms 110 and 111 specify the velocity words and in addition, utilize the conditions L_1 and L'_1 in lieu of P_2 and P'_2 since the associated integrand registers are now stored in the L_1 channel.

Continuing, at the end of the arithmetic operations on $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ velocity words, two functions must be performed, namely, the overflow difunction signal from the integrators must be entered in flip-flops I_H , I_X and I_Y to be stored for the following iteration of the computer, and in addition, flip-flop K_2 must be set up with the overflow difunction so that this intelligence can be arithmetically combined with the servo register number in the manner described with respect to Table VII. As will be shown below, these functions are carried out by first setting up the difunction output signal in flip-flop K_2 , so that it may be utilized in the ensuing position word servo register, and then shifting the contents of flip-flop K_2 into the appropriate one of flip-flops I_H , I_X and I_Y .

It will be recalled that a plus one difunction output signal is produced by an integrator when its operand signal is add and a carry is propagated from the most significant digit in flip-flop K_2 , or when the operand signal is subtract and no carry is propagated into flip-flop K_2 from the most significant digit of the integrator's overflow

register. Consequently, when the operand signal is add, as indicated by a binary one stored in flip-flop S_2 , flip-flop K_2 presents the difunction output signal in its proper form, that is, a plus one being represented by flip-flop K_2 being in its one state and a minus one being represented by a zero for flip-flop K_2 . When the operand signal is subtract as indicated by flip-flop S_2 containing a zero, on the other hand, flip-flop K_2 presents the complement of the difunction output signal at the end of the velocity word; in other words, a plus one difunction output signal is represented by a zero stored in flip-flop K_2 whereas a binary one in the flip-flop represents a minus one difunction signal. It will be recognized, therefore, that at the end of the velocity words $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ the K_2 flip-flop may be made to present the output difunction signal in its proper form, regardless of whether the operand signal was add or subtract, by merely triggering the K_2 flip-flop to reverse its state at that time when the operand signal was subtract. This triggering function is specified by the identical terms 112 and 113 in Equations 41 and 42, respectively.

In the immediately following digit time interval then, which is the first digit time interval of the position words, flip-flop K_2 is available for use in the mechanization of Table VII above, the arithmetic operations upon the servo register number being identical with those previously described for the Fit routine except that flip-flop K_2 now initially contains the overflow difunction signals from the preceding velocity word integrator rather than the input difunction signals from the radar. Thereafter the difunction signal from each velocity word integrator is shifted into the appropriate I flip-flop at the end of the first digit time interval of each position word, terms 114, 115 and 116 of Equations 46, 48 and 50 specifying the shift at the beginning of the position words H , X and Y , respectively. In performing this shift function only the foregoing set-to-one functions are required owing to the fact that flip-flops I_H , I_X and I_Y have been preset to zero at the end of the last digit time interval of the preceding acceleration word, as specified by terms 117, 118 and 119 of Equations 47, 49 and 51, respectively. It will be recognized that these latter terms are effective to zero the associated flip-flops only after the contents of the flip-flops have been utilized to set up the operand signal for the $\ddot{H}$, $\ddot{X}$ and $\ddot{Y}$ acceleration integrators in sign flip-flop S_2 as previously described.

Having thus described the various operations which take place within the computer during the Extrapolate routine, consideration will now be given to the manner in which the Extrapolate routine is terminated. Recall now that the Extrapolate routine may be initiated to make a single iteration, a group of five iterations, or to iterate continuously until the continuous extrapolate switch in the front panel controls is released. It will also be recalled from Table II hereinabove that the dawdle condition of the computer is utilized to prevent a false recirculation of the computer at the end of the Extrapolate routine.

As soon as the Extrapolate routine is initiated and flip-flop Q is set to its one-representing state, flip-flop R is also set to its one-representing state as specified by term 120 of Equation 26. This does not affect the compute condition of the computer, however, since as set forth in Table IV the compute condition is specified by flip-flop Q being in its one-representing state regardless of the state of flip-flop R .

Assuming now that the Extrapolate routine was initiated by depressing the 5-cycle switch in the front panel controls. Remembering that the routine is initiated by the origin mark in channel P_2 , and that the origin mark occurs once every five iterations or difunction intervals, it will be recognized that flip-flop Q should be zeroed to place the computer in its dawdle condition on the next

appearance of the origin mark. This operation is specified by term 121 of Equation 25, thus terminating the Extrapolate routine in the event a 5-cycle extrapolation is utilized.

If on the other hand a single extrapolation operation is initiated by actuation of the 1-cycle switch in the front panel controls, the Extrapolation routine is terminated at the end of the position word Y following the setting of flip-flop Q to its one-representing state, or in other words, after only one difunction interval. This operation is specified by a portion of the previously described term 81 of Equation 25, the conditions operative in this instance being $P_1P_2C_2C_4[(5\text{-cycle up})(\text{continuous up})]$. It will be noted that this logical expression stipulates that the Q flip-flop should be zeroed at the end of the first Y position word when both the 5-cycle switch and the continuous extrapolate switch are in their normal positions. It therefore follows that although this function is the normal zeroing function for a one cycle Extrapolation, it also provides the means for ending continuous Extrapolation, and also for 5-cycle Extrapolation if the 5-cycle switch is released prematurely before four iterations have taken place.

After the Q flip-flop has been zeroed to end the Extrapolate routine, the R flip-flop remains in its one-representing state until all three Extrapolate switches in the front panel controls are returned to their normal positions, at which time the R flip-flop is zeroed by term 122 of Equation 27. Thus the R flip-flop holds the computer in its dawdle condition and prevents the resetting of flip-flop Q to its one state falsely by failure of the operator to release one of the Extrapolate control switches after the Extrapolate routine has been carried out.

After the Q and R flip-flops are returned to their zero states the computer is once more in its idle condition and continues to operate in the manner described originally hereinabove. It is clear of course, that the Extrapolate routine may be initiated and terminated any desired number of times until the coordinates visually presented by the digital servo coincide with those of a point on the associated map, at which time these coordinates represent either the projectile's firing point or impact point depending upon whether the Extrapolation was carried out backward in time or forward in time.

Having ascertained the desired information concerning the projectile's trajectory, the Reset routine is then initiated by switching the routine control switch on the computer's front panel to the Reset position to thereby prepare the computer for its computational operations when another projectile is subsequently tracked by the radar. In the Reset position, it will be recalled, the computer receives a low level signal on the conductor $\textcircled{R}$ and a high level signal on the conductor designated $\textcircled{R}$. Within the computer this has the effect of rendering terms 49, 50 and 51 of Equations 28, 29 and 30 inoperative, and substituting therefore terms 123, 124 and 125 of these same equations. These terms, in turn, specify that the digital servos should be energized in accordance with the values of the most significant digits of the binary numbers stored in the accumulator registers, which numbers, it will be recalled, represent the amount which the coordinates visually displayed by the servo counters have changed from the original radar coordinates. Consequently the Reset routine functions to restore the servo counters to the radar coordinates, at which time the accumulator registers are once more empty.

Following the Reset routine the routine control switch on the computer's front panel is then switched briefly to its clear position, and then back to its compute position, the clear routine being utilized in the manner previously described to clear channels L_1 and L_2 of all prior intelligence and to preset the necessary operational flip-flops to

zero. Accordingly, the computer is now completely restored to its original idle condition and is fully prepared for another projectile tracking operation.

Having thus described in detail the projectile tracking computer of the invention and its various novel features, it is to be expressly understood that numerous details of the computer may be modified without departing from the spirit and scope of the invention. For example, in mechanizing the logical equations set forth above the gating structure may be utilized to combine several terms into a single term, as shown in Equations 18, 37, 38 and 40 by the fact that terms 3 and 10, terms 17 and 39, terms 18 and 40, and terms 42 and 76, respectively, may be expressed by an equivalent single term. In a similar manner it will be appreciated that although three 2048 counters are included in channel L₁, a single 2048 counter could be utilized in conjunction with all three computing sections. Moreover, if desired the computer could include additional memory space in which a plurality of different drag factors could be stored so that different drag factors could be utilized in solving the trajectory equations for projectiles having widely different ballistics characteristics. In view of the fact that the computer of the invention and its various novel features are thus modifiable in numerous particulars without departing from the basic concepts herein disclosed, it is to be expressly understood that the spirit and scope of the invention is limited only by the spirit and scope of the appended claims.

What is claimed as new is:

1. A projectile tracking system for determining the coordinates of either the firing point or impact point of a projectile in an X, Y, H orthogonal coordinate system, said tracking system comprising: a radar operable to track a projectile through at least a portion of its trajectory, said radar being oriented with respect to the coordinate system to produce output signals representative of the instantaneous coordinate position of the projectile along each of the three coordinate axes while the projectile is being tracked; an electronic digital computer operable to solve the trajectory equations of a projectile moving in space to produce successive output signals representative of the coordinate positions of successive points on a projectile's trajectory, said computer requiring as initial conditions the coordinate positions and velocities of the projectile at a point on its trajectory; and means operable in conjunction with said computer for sampling said radar output signals over a fixed predetermined time interval to apply to said compute as said initial conditions electrical signals representative of the coordinate positions and velocities of the projectile at substantially the midpoint of that portion of the projectile's trajectory traversed by the projectile during said time interval.

2. The system defined in claim 1 wherein said last-named means includes conversion means responsive to said radar output signals for generating three difunction signal trains corresponding respectively to X, Y and H coordinate axes of the coordinate system and representative of the instantaneous position of the projectile as it is being tracked, each of said trains including N difunction signals each having a fixed period T/N where T is the period of said fixed predetermined interval, each signal in said difunction signal trains having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each of said difunction signal trains corresponding to the average position of the projectile along the corresponding coordinate during said fixed time interval.

3. A projectile tracking system for determining the coordinates of either the firing point or impact point of a projectile in an X, Y, H orthogonal coordinate system, said tracking system comprising: a radar operable to track a projectile through at least a portion of its trajectory, said radar being oriented with respect to the coordinate

system to produce output signals representative of the instantaneous coordinate position of the projectile along each of the three coordinate axes while the projectile is being tracked; an electronic digital computer selectively actuatable to iteratively extrapolate the trajectory equations of a projectile moving in space to produce successive output signals representative of the coordinate positions of successive spaced points on a projectile's trajectory, said computer requiring as initial conditions the known coordinate positions and velocities of the projectile at a point on its trajectory; means operable in conjunction with said computer for sampling said radar output signals over a fixed predetermined time interval to apply to said computer as said initial conditions electrical signals representative of the coordinate positions and velocities of the projectile at substantially the midpoint of that portion of the projectile's trajectory traversed by the projectile during said time interval; and means for selectively actuating said computer to extrapolate said trajectory equations either forward or backward.

4. A projectile tracking system for determining the coordinates of either the firing point or impact point of a projectile in an X, Y, H orthogonal coordinate system, said tracking system comprising: a radar operable to track a projectile through at least a portion of its trajectory, said radar being oriented with respect to the coordinate system to produce output signals representative of the instantaneous coordinate position of the projectile along each of the three coordinate axes while the projectile is being tracked; converter means responsive to said radar output signals for producing three difunction signal trains corresponding to X, Y and H axes of the coordinate system and representative of the instantaneous position of the projectile along the coordinate axis, each signal in said trains having either a high level representative of a first quantity or a low level representative of a second quantity, the average value of the quantities represented by N successive signals in each train being representative of the average position of the projectile along the corresponding axis during the period that the signals are generated; and an electronic digital computer operable to solve the trajectory equations of a projectile moving in space to produce output signals representative of the coordinates of any point on the projectile's trajectory, said computer requiring as initial conditions the known coordinate positions and velocities of the projectile at a point in its trajectory, said computer including accumulator means for receiving N successive difunction signals in each of said trains to produce electrical signals representative of the coordinate positions and velocities of the projectile at substantially the midpoint of that portion of the projectile's trajectory traversed by the projectile during the period that said N successive signals in each train are generated.

5. A projectile tracking computer for determining the coordinates of the firing point of a projectile a portion of whose trajectory in an orthogonal coordinate system has been tracked by an associated radar, said computer comprising: a plurality of digital integrators interconnected to solve the trajectory equations for the projectile along each of the coordinate axes of the coordinate system, said digital integrators including means for storing as initial conditions in the solution of said equations the position and velocity of the projectile along the coordinate axis of the coordinate system and at a point in its trajectory; means for generating a plurality of difunction signal trains corresponding respectively to the coordinate axes of the coordinate system and representative of the instantaneous position of the projectile along the corresponding coordinate axes and over a preselected portion of its trajectory, each of said trains including N sequential signals, each signal in each train having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each train repre-

senting the average position of projectile along the corresponding coordinate axis; means for receiving said difunction signal trains to generate electrical signals representative of the position and velocity of the projectile along the coordinate axes of the coordinate system and at a point corresponding substantially to the midpoint of said preselected portion of the trajectory; and means for entering said electrical signals into said plurality of integrators.

6. A projectile tracking computer for determining the coordinates of the firing point of a projectile a portion of whose trajectory in an orthogonal coordinate system has been tracked by an associated radar, said computer comprising: a plurality of digital integrators interconnected in accordance with the trajectory equations for the projectile along each of the coordinate axes of the coordinate system, said digital integrators including means for storing as initial conditions the coordinate positions and velocities of the projectile at a preselected point in its trajectory, and being selectively actuatable to extrapolate said equations backward in time to produce output signals representative of the coordinate positions of points in the projectile's trajectory other than said preselected point; means for generating a plurality of difunction signal trains corresponding respectively to the coordinate axes of the coordinate system and representative of the instantaneous position of the projectile along the corresponding coordinate axes and over a preselected portion of its trajectory, each of said trains including N sequential signals, each signal in each train having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each train representing substantially the average position of the projectile along the corresponding coordinate axis; means responsive to said difunction signal trains for storing in said digital integrators electrical signals representative of the position and velocity of the projectile along the coordinate axes of the coordinate system and at a point corresponding substantially to the midpoint of said preselected portion of the trajectory; and means for selectively actuating said integrators to extrapolate said trajectory equations backward in time to produce said output signals.

7. The projectile tracking computer defined in claim 6 which further includes a plurality of mechanical counters corresponding respectively to the coordinate axes of the coordinate system, each of said counters having an input shaft and being operable to present a visual numerical display representative of the total rotation imparted to said shaft, and digital servo means intercoupling said plurality of integrators with said counters and responsive to said output signals for rotating said counter shafts to positions corresponding to the extrapolated coordinate positions represented by said output signals whereby said counters visually display the corresponding coordinates of any point on the projectile's trajectory to which said trajectory equations have been extrapolated.

8. A projectile tracking computer for determining the coordinates of the firing point of a projectile a portion of whose trajectory in an XYH orthogonal coordinate system has been tracked by an associated radar, said computer comprising: means for generating three difunctional signal trains corresponding respectively to the X, Y and H coordinate axes of the coordinate system and representative of the instantaneous position of the projectile along the corresponding coordinate axes and over a preselected portion of its trajectory, each of said trains including N sequential signals, each signal in each train having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each train representing substantially the average position of the projectile along the corresponding coordinate axis; binary accumulator means responsive to said difunction signal trains for generating electrical signals representative of

the position and velocity of the projectile along the coordinate axes of the coordinate system and at a point corresponding substantially to the midpoint of said preselected portion of the trajectory; a plurality of digital

5 integrators interconnected in accordance with the trajectory equations for the projectile along each of the three coordinate axes of the coordinate system, said digital integrators including means for storing as initial conditions the electrical signals representing the coordinate positions and velocities of the projectile at said midpoint, and being selectively actuatable to extrapolate said equations backward in time to produce output signals representative of the coordinate positions of points in the projectile's trajectory other than said midpoint; and means for selectively actuating said integrators to extrapolate said trajectory equations backward in time to produce said output signals.

9. The projectile tracking computer defined in claim 8 wherein said binary accumulator means includes a first group of three binary accumulators corresponding respectively to the X, Y, and H coordinate axes, each accumulator in said first group being operable to accumulate the signals in the corresponding signal train to generate signals representative of the numerical difference between the summation of the first N/2 signals in the train and the summation of the remaining N/2 signals in the train, and a second group of three binary accumulators corresponding respectively to the X, Y and H coordinate axes, each accumulator in said second group being operable to accumulate the signals in the corresponding signal train to generate signals representative of the summation of the N signals in the train, whereby the signals generated in said first and second groups of accumulators are respectively representative of the coordinate velocity and position of the projectile along each of the coordinate axes.

10. A projectile tracking computer for determining the coordinates of the firing point of a projectile a portion of whose trajectory in an XYH orthogonal coordinate system has been tracked by an associated radar, said computer comprising: a plurality of digital integrators interconnected to produce output signals representative of the coordinate positions of points in the projectile's trajectory, said integrators being interconnected in accordance with the equations

$$H = H_0 + \int \dot{H} dt$$

$$X = X_0 + \int \dot{X} dt$$

$$Y = Y_0 + \int \dot{Y} dt$$

50 where H_0 , X_0 and Y_0 are initial conditions corresponding to the coordinates of a known point in the projectile's trajectory and where $\dot{H}$, $\dot{X}$ and $\dot{Y}$ are velocities along the corresponding coordinate axes and are described by the equations

$$\dot{H} = V_H - \int (g + K_H \dot{H}) dt$$

$$\dot{X} = V_X - \int K_X \dot{X} dt$$

$$\dot{Y} = V_Y - \int K_Y \dot{Y} dt$$

60 where g , K_H , K_X and K_Y are constants stored in said integrators and V_H , V_X and V_Y are initial conditions corresponding to the coordinate velocities of the projectile at said known point; means for generating a plurality of difunction signal trains corresponding respectively to the three coordinate axes of the coordinate system and representative of the instantaneous position of the projectile along the corresponding coordinate axes and over a preselected portion of its trajectory, each of said trains including N sequential signals, each signal in each train having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each train representing substantially the average position of the projectile along the corresponding coordinate axis

over the selected portion of the trajectory; and means responsive to said difunction signal trains for storing as the initial conditions in said digital integrators electrical signals representative of the position and velocity of the projectile along the coordinate axes of the coordinate system and at a point corresponding substantially to the midpoint of said preselected portion of the trajectory.

11. In a digital computer, a system for determining the coordinates of the midpoint of a sampled portion of the path traveled by an object moving in space, said system comprising: means for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates in a rectangular coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each train occurring over a given interval representing substantially the average position of the object along the associated coordinate during the interval; sampling means for abstracting N signals from each of said difunction signal trains; and a plurality of digital binary accumulators corresponding respectively to said plurality of difunction signal trains representative of said corresponding coordinates, each of said accumulators being operable to receive and accumulate the signals abstracted by said sampling means from the corresponding difunction signal train to average the values represented by the abstracted signals.

12. The combination defined in claim 11 which further includes a corresponding plurality of digital servo systems coupled to said accumulators for visually presenting an indication of the average coordinate positions of the object during the interval in which said sampling means abstracts said difunction signal trains, each of said servo systems comprising a bidirectional counter having means for presenting a visual display of the counter position, drive means for driving the counter in one direction when the binary number stored in the corresponding accumulator is above a predetermined value and in the opposite direction when the binary number stored in the accumulator is below said predetermined value, quantizer means coupled to said counter for producing signals representative of each incremental change in the count presented in said counters and the direction of the change, and means for applying the signals generated by said counter to said accumulator to change the number stored in the accumulator by an amount corresponding to the incremental changes made in the counter position and in a sense opposite to the sense of the incremental changes.

13. In a digital computer, a system for determining the coordinates of the midpoint of a sampled portion of the path traveled by an object moving in space, said system comprising: means selectively actuable for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates in a rectangular coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals in each train occurring over a given interval representing substantially the average position of the object along the associated coordinate during the interval; means for actuating said selectively actuable means to produce said difunction signal trains each including N sequential difunction signals; a plurality of digital binary accumulators corresponding respectively to said plurality of coordinates, each of said accumulators being operable to count in one direction in response to each high level signal applied thereto and in the opposite direction in response to each applied low level signal;

and means for applying each of said difunction signal trains to said respectively corresponding accumulator.

14. In a digital computer, a system for determining the velocity of an object moving in an orthogonal coordinate system in space at the midpoint of a sampled portion of the object's trajectory, said system comprising: selectively actuable means for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates which define the coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals occurring in each train over a given time interval representing substantially the average position of the object along the corresponding coordinate during the interval; means for selectively actuating said selectively actuable means to generate said plurality of difunction trains, each of said trains comprising N sequential signals; a plurality of digital binary accumulators corresponding respectively to said plurality of difunction signal trains representative of said corresponding plurality of coordinates, each of said accumulators being operable to change the count stored therein in one sense in response to each high level difunction signal applied thereto and in the opposite sense in response to each low level difunction signal applied thereto; means for separating the N difunction signals in each of said difunction signal trains into a first group of N/2 signals and a second group of N/2 signals; means for inverting the signals in one of said groups in each of said trains; and means for applying to the corresponding accumulator the inverted signals in said one group of signals and the signals in the other group of said first and second groups of signals whereby the binary numbers stored in said accumulators represent the midpoint velocities of the object along the corresponding coordinates of the coordinate system.

15. In a digital computer, a system for determining the velocity of an object moving in an orthogonal coordinate system in space at a predetermined point in the object's trajectory, said system comprising: selectively actuable means for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates which define the coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals occurring in each train over a given time interval representing substantially the average position of the object along the corresponding coordinate during the interval; means for selectively actuating said selectively actuable means to generate simultaneously said plurality of difunction trains, each of said trains comprising N sequential signals, the first group of N/2 signals in each train being generated before the object reaches said predetermined point and the second group of N/2 signals being generated after the object has passed said predetermined point; a plurality of digital binary accumulators for storing binary numbers and corresponding respectively to said plurality of difunction signal trains representative of said corresponding plurality of coordinates, each of said accumulators being operable to change the number stored therein in one sense in response to each high level difunction signal applied thereto and in the opposite sense in response to each low level difunction signal applied thereto; means for inverting the signals in one of said groups of N/2 signals in each of said trains; and means for applying to the corresponding accumulator the inverted signals in said one group of signals and the signals in the other group of said first and second signals whereby the binary number stored in said accumulators represent the mid-

point velocities of the object along the corresponding coordinates of the coordinate system.

16. In a digital computer, a system for determining the velocity of an object moving in an orthogonal coordinate system in space at the midpoint of a sampled portion of the object's trajectory, said system comprising: selectively actuable means for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates which define the coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals occurring in each train over a given time interval representing substantially the average position of the object along the corresponding coordinate during the interval; means for selectively actuating said selectively actuable means to generate said plurality of difunction trains, each of said trains comprising N sequential signals; and a corresponding plurality of accumulator means for receiving the corresponding difunction signal trains, each of said accumulator means being operable to accumulate the signals in the applied signal train to present signals representative of the numerical difference between the summation of the first N/2 signals in the applied train and the summation of the remaining N/2 signals in the applied train.

17. In a digital computer, a system for determining the time rate of change of a quantity represented by an applied analog signal whose value is changing substantially uniformly with time, said system comprising: selectively actuable means for generating a difunction train representative of the instantaneous value of the analog signal, each signal in said train having a predetermined period and having either a high level value representing the maximum value of the quantity or a low level value representing the minimum value of the quantity, the average value of the quantities represented by the signals over a given time interval representing substantially the average value of the quantity represented by the analog signal; means for selectively actuating said selectively actuable means to generate a difunction train including N sequential difunction signals; a binary accumulator for storing electrical signals representative of a binary number, said accumulator being operable to change the number stored therein in one sense in response to each high level difunction signal applied thereto and in the opposite sense in response to each low level signal applied thereto; means for separating said N difunction signals into a first group of N/2 signals and a second group of N/2 signals; means for inverting the inverting the signals in one of the said groups of signals; and means for applying to said accumulator the inverted signals in said one group of signals and the difunction signals in the other group of signals.

18. In a digital computer, a system for determining the position and velocity of an object moving in an orthogonal coordinate system in space at the midpoint of a sampled portion of the object's trajectory, said system comprising: selectively actuable means for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates which define the coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals occurring in each train over a given time interval representing substantially the average position of the object along the corresponding coordinate during the interval; means for selectively actuating said selectively actuable means to generate said plurality of difunction trains, each of said trains comprising N sequential signals;

a first plurality of binary accumulators corresponding respectively to said plurality of difunction signal trains, each accumulator in said first plurality of accumulators being operable to accumulate the signals in the corresponding difunction signal train to present signals representative of the numerical difference between the summation of the first N/2 signals in the train and the summation of the remaining N/2 signals in the train; and a second plurality of binary accumulators corresponding respectively to said plurality of difunction signal trains, each accumulator in said second plurality being operable to accumulate the signals in the corresponding difunction signal train to present signals representative of the summation of the N signals in the train, whereby the accumulators in said first and second pluralities present signals representative of the velocity and position, respectively, of the object along the corresponding coordinates.

19. In a digital computer, a system for determining the position and velocity of an object moving in an orthogonal coordinate system in space at the midpoint of a sampled portion of the object's trajectory, said system comprising: selectively actuable means for generating a plurality of difunction signal trains representative of the instantaneous position of the object along a corresponding plurality of coordinates which define the coordinate system, each signal in said trains having a predetermined period and having either a high level representing a first quantity or a low level representing a second quantity, the average value of the quantities represented by the signals occurring in each train over a given time interval representing substantially the average position of the object along the corresponding coordinate during the interval; means for selectively actuating said selectively actuable means to generate said plurality of difunction trains, each of said trains comprising N sequential signals; first and second groups of digital binary accumulators, each group including a plurality of accumulators corresponding respectively to said plurality of difunction signal trains, each accumulator in each group being operable to change the count stored therein in one sense in response to each high level difunction signal applied thereto and in the opposite sense in response to each low level difunction signal applied thereto; means for applying said N signals in each of said difunction signal trains to the corresponding accumulators in said first group of accumulators; means for separating the N difunction signals in each of said difunction signal trains into a first group of N/2 signals and a second group of N/2 signals and for inverting the signals in one of said groups of signals in each difunction train; and means for applying the inverted signals in said one group of signals and the difunction signals in the other group of signals to the corresponding accumulators in said second group of accumulators.

20. In a digital computer, an input conversion apparatus for rotating a shaft to represent an applied analog signal, the total rotation imparted to the shaft being proportional to the average value of the analog signal, said apparatus comprising: first means responsive to the applied analog signal over a period T for producing a difunction input signal train including N difunction signals, each signal having either a first value representing a predetermined maximum value of the analog signal or a second value representing a predetermined minimum value of the analog signal, the average value of said difunction signals over the period T being proportional to the average value of the analog signal over said period; and second means responsive to each first or second valued difunction signal for rotating the shaft through an incremental rotational angle proportional to said maximum or minimum value divided by N, respectively, whereby in response to said N signals, the shaft is rotated a total amount proportional to the average value of the analog signal.

21. The input conversion apparatus defined in claim 20

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wherein said second means includes a binary accumulator for storing electrical signals representing a binary number; drive means responsive to the most significant digit of the number stored in said accumulator for rotating the shaft in one direction when the most significant digit is a binary one and in the opposite direction when the most significant digit is a binary zero; quantizer means coupled to the shaft and operative to produce a first difunction output signal for indicating each time the shaft has rotated through said predetermined incremental rotational angle and a second difunction output signal train for indicating the direction in which the shaft has rotated through each of said incremental rotational angles; and means for combining said input difunction signal train and said first and second difunction signal trains with said signals stored in said accumulator to store in said accumulator signals representative of the algebraic sum of the quantities represented by the signals combined.

22. In a digital computer, an input conversion apparatus for rotating a shaft to represent an applied analog signal, the total rotation imparted to the shaft being proportional to the average value of the analog signal, said apparatus comprising: conversion means responsive to the applied analog signal over a period T for producing an input difunction train consisting of N difunction signals, each signal having either a first value representing a predetermined maximum value of the analog signal or a second value representing a predetermined minimum value of the analog signal, the average value of said difunction signals over the period T being proportional to the average value of the analog signal over said period; accumulator means responsive to said N difunction signals for generating electrical signals representative of the numerical difference between the number of first valued signals in said train and the number of second valued signals in said train; and servo means coupled to said accumulator and operative to rotate the shaft through a total rotational angle proportional to said numerical difference, whereby in response to said N signals, the shaft is rotated a total amount proportional to the average value of the analog signals.

23 An input conversion apparatus for rotating a shaft to represent an applied analog signal, the total rotation imparted to the shaft being proportional to the average value of the analog signal, said apparatus comprising: first means responsive to the applied analog signal over a period T for producing a difunction input signal train including N difunction signals, each signal having either a first value representing a predetermined maximum value of the analog signal or a second value representing a predetermined minimum value of the analog signal, the average value of said difunction signals over the period T being proportional to the average value of the analog signal over said period; accumulator means for storing signals representative of a binary number, said accumulator means being responsive to said input difunction signal train for increasing said binary number by unity in response to each difunction signal having said first value and for decreasing said binary number by unity in response to each difunction signal having said second value; means for rotating the shaft in one direction when the most significant digit of said binary number is zero and in the opposite direction when the most significant digit of said number is one; and quantizer means for increasing or decreasing said number by unity each time the shaft is rotated in said one direction or said other direction, respectively, through an incremental angle proportional to said predetermined maximum value divided by N.

24. A bidirectional digital position servo system operable to drive a positionable element to a position corresponding to the position of an object along a preselected coordinate of a coordinate system in space, said system comprising: converter means for generating a difunction signal train representative of the position of the object along the preselected coordinate in space, each signal in said train hav-

ing a predetermined period; digital storage means including recording means for recording at a first point applied electrical signals representative of the successive digits of a binary number and reading means for presenting at a second point the signals applied to said recording means, the time required for a signal applied to said recording means to be presented at said reading means being substantially said predetermined period; drive means actuable for driving the positionable element selectively forward or backward; means coupled to said reading means and to said drive means and operative in response to the signals representing the most significant digit of the binary number for actuating said drive means to drive the positionable element in one direction when the most significant digit is a binary one and in the opposite direction when the digit is a binary zero; quantizer means coupled to said positionable element and operative to generate a first output signal train for indicating each incremental change in the position of the positionable element and a second output signal train representative of the complement of the sense of the positional changes indicated by said first output signal train; and control means coupled to said quantizer means, said converter means, and to said recording and reading means, said control means being operative to combine the signals representing the binary number, the difunction signal train and the first and second output signal trains from the quantizer to apply to said recording means signals representing the algebraic sum of the positions and incremental changes of position represented by the signals combined thereby.

25. A bidirectional digital position servo system operable to drive a positionable element to a position corresponding to the average position represented by an applied difunction signal train composed of 2^n sequential difunction signals, each signal in said train having a predetermined period, said digital servo system comprising: digital storage means including recording means for recording at a first point applied electrical signals representative of the successive digits of a binary number, and reading means for presenting at a second point the signals applied to said recording means, the time required for a signal applied to said recording means to be presented at said reading means being substantially said predetermined period; drive means actuable for driving the positionable element selectively forward or backward; means coupled to said reading means and to said drive means and operative in response to the signals representing the most significant digit of the binary number for actuating said drive means to drive the positionable element in one direction when the most significant digit is a binary one and in the opposite direction when the digit is a binary zero; quantizer means coupled to said positionable element and operative to generate a first output signal train for indicating each incremental change in the position of the positionable element and a second output signal train representative of the complement of the sense of the positional changes indicated by said first output signal train; control means coupled to said quantizer means, and to said recording and reading means, said control means being normally operable to combine the signals representing the binary number and the first and second output signal trains from the quantizer to apply to said recording means signals representing the binary sum of the quantities represented by the signals combined; and means for applying the difunction signal train to said control means, said control means being operable in response to said difunction signal train for applying to said recording means signals representing the binary sum of the quantities represented by the difunction signals, said first and second output signals from said quantizer, and the signals received from said reading means.

26. A bidirectional digital position servo system operable to drive a positionable element to a position corresponding to the average position of a moving object as

represented by an applied difunction signal train composed of 2^n sequential difunction signals, each signal in said train having a predetermined period, said digital servo system comprising: digital storage means including recording means for recording at a first point applied electrical signals representative of the successive digits of a binary number, and reading means for presenting at a second point the signals applied to said recording means, the time required for a signal applied to said recording means to be presented at said reading means being substantially said predetermined period; drive means actuable for driving the positionable element selectively forward or backward; means coupled to said reading means and to said drive means and operative in response to the signals representing the most significant digit of the binary number for actuating said drive means to drive the positionable element in one direction when the most significant digit is a binary one and in the opposite direction when the digit is a binary zero; quantizer means coupled to said positionable element and operative to generate a first output signal train for indicating each incremental change in the position of the positionable element and a second output signal train representative of the complement of the sense of the positional changes indicated by said first output signal train; and electronic arithmetic means coupled to said quantizer means, said converter means, and to said recording and reading means, said arithmetic means being normally operative to combine said first and second output signals and the signals presented by said reading means to apply to said writing means signals representing the algebraic sum of the quantities represented by the signals combined, and being responsive to the application of the signals in the difunction signal train to combine said first and second output signals, the difunction signals and the signals received from said reading means to apply to said writing means signals representative of the algebraic sum of the quantities represented by the signals which have been combined.

27. In a digital computer, a bidirectional quantizer for generating electrical output signals representative of each incremental change in the rotational position of a shaft and the sense of the positional change, said quantizer comprising: first means responsive to each revolution of the shaft for producing a first bilevel signal train composed of a plurality of high-level signals separated by a corresponding plurality of low-level signals; second means responsive to each revolution of the shaft for producing a second bilevel signal train composed of a corresponding plurality of high-level signals separated by a corresponding plurality of low-level signals, said second signal train leading said first signal train by approximately 90° when said shaft is rotated at a fixed rate in one direction, and lagging said first signal train by approximately 90° when said shaft is rotated at a fixed rate in the opposite direction; means for periodically sampling said first signal train at a predetermined frequency and responsive to a change in the signal levels for producing a first output signal indicating that an incremental change has been made in the rotational position of the shaft; third means for periodically sampling said first signal train at a predetermined rate; fourth means for storing the sampled signal and for presenting the stored signal when said third

means again samples said first output signal train; and comparator means responsive to the signal sampled by said fourth means and the signal presented by said fifth means for generating an output signal representing an incremental unit of rotation of the shaft whenever the values represented by said sampled and stored signals are different; and means responsive to said sampled signal, said stored signal and the level of said second output signal for indicating the sense of the rotational change of the shaft.

28. A bidirectional quantizer for periodically indicating whether an incremental change has taken place in the rotational position of a shaft and the direction of the rotational change, said quantizer comprising: first means coupled to said shaft for dividing the rotational positions of said shaft into first and second groups of n angular sectors each, where n is an integer and the sectors in each group define substantially the same arcuate angle, the sectors in each group being interplexed with the sectors of the other group; second means coupled to said first means and responsive to rotation of the shaft for producing a first bilevel output signal train having a relatively high level value when a first fixed reference point adjacent said shaft lies within the angle defined by a sector in said first group of sectors and a relatively low level value when said first fixed reference point lies within the angle defined by a sector in said second group of sectors; third means coupled to said first means and responsive to rotation of the shaft for producing a second bilevel output signal train having a high level value when a second fixed reference point adjacent said shaft lies within the angle defined by a sector in said first group of sectors and a low level value when said second reference point lies within a sector in said second group of sectors, said first and second reference points being spaced from each other circumferentially about the shaft by an angle such that one of said points falls substantially in the middle of a sector when the other point is on the borderline between any two adjacent sectors; fourth means for periodically sampling said first output signal train at a predetermined rate; fifth means for storing the sampled signal and for presenting the stored signal when said fourth means again samples said first output signal train; comparator means responsive to the signal sampled by said fourth means and the signal presented by said fifth means for generating an output signal representing an incremental unit of rotation of the shaft whenever the values represented by said sampled and stored signals are different; and means responsive to said sampled signal, said stored signal and the level of said second output signal for indicating the sense of the rotational change of the shaft.

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