(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 August 2011 (18.08.2011)

PCT

(10) International Publication Number
WO 2011/099335 A1

(51) International Patent Classification:
H01L 21/8234 (2006.01) *H01L 27/10* (2006.01)
H01L 21/02 (2006.01) *H01L 27/108* (2006.01)
H01L 21/336 (2006.01) *H01L 27/115* (2006.01)
H01L 21/8242 (2006.01) *H01L 27/12* (2006.01)
H01L 21/8247 (2006.01) *H01L 29/786* (2006.01)
H01L 27/00 (2006.01) *H01L 29/788* (2006.01)
H01L 27/06 (2006.01) *H01L 29/792* (2006.01)
H01L 27/088 (2006.01)

(21) International Application Number:
PCT/JP2011/050791

(22) International Filing Date:
12 January 2011 (12.01.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2010-029278 12 February 2010 (12.02.2010) JP

(71) Applicant *(for all designated States except US)*: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.** [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa 2430036 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **YAMAZAKI, Shunpei** [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP). **FUJII, Teruyuki. IMAHAYASHI, Ryota. SASAGAWA, Shinya. KURATA, Motomu. TAGUCHI, Fumika.**

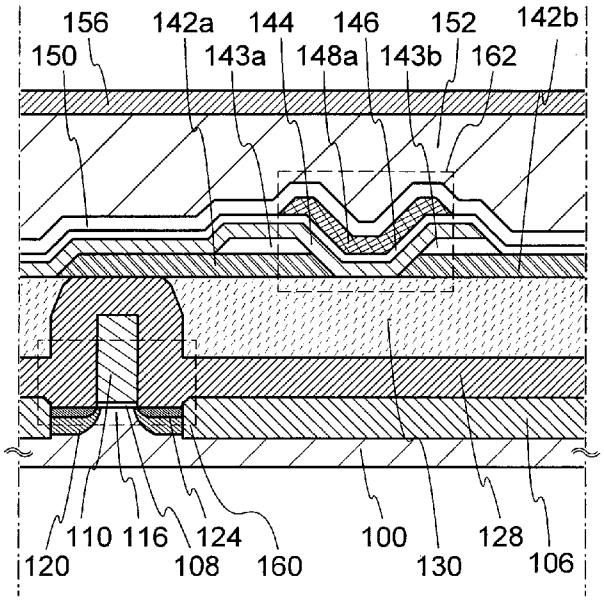
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

FIG. 1



(57) Abstract: An object is to provide a semiconductor device having a novel structure in which a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor are stacked. The semiconductor device includes a first transistor, an insulating layer over the first transistor, and a second transistor over the insulating layer. In the semiconductor device, the first transistor includes a first channel formation region, the second transistor includes a second channel formation region, the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region, and the insulating layer includes a surface whose root-mean-square surface roughness is less than or equal to 1 nm.

WO 2011/099335 A1

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

TECHNICAL FIELD

[0001]

The technical field of the present invention relates to a semiconductor device and a method for manufacturing the semiconductor device. Note that here, semiconductor devices refer to general elements and devices which function utilizing semiconductor characteristics.

BACKGROUND ART

[0002]

There are a wide variety of metal oxides and such metal oxides are used for various applications. Indium oxide is a well-known material and has been used for transparent electrodes required in liquid crystal display devices or the like.

[0003]

Some metal oxides have semiconductor characteristics. The examples of such metal oxides having semiconductor characteristics are, for example, tungsten oxide, tin oxide, indium oxide, zinc oxide, and the like. A thin film transistor in which a channel formation region is formed using such metal oxides is already known (for example, see Patent Documents 1 to 4, Non-Patent Document 1, and the like).

[0004]

As metal oxides, not only single-component oxides but also multi-component oxides are known. For example, $InGaO_3(ZnO)_m$ (m: a natural number) having a homologous phase is known as a multi-component oxide semiconductor including In, Ga, and Zn (for example, see Non-Patent Documents 2 to 4 and the like).

[0005]

Furthermore, it is confirmed that an oxide semiconductor including such an

In-Ga-Zn-based oxide is applicable to a channel formation region of a thin film transistor (for example, see Patent Document 5, Non-Patent Documents 5 and 6, and the like).

[Reference]

[Patent Documents]

[0006]

[Patent Document 1] Japanese Published Patent Application No. S60-198861

[Patent Document 2] Japanese Published Patent Application No. H8-264794

[Patent Document 3] Japanese Translation of PCT International Application No. H11-505377

[Patent Document 4] Japanese Published Patent Application No. 2000-150900

[Patent Document 5] Japanese Published Patent Application No. 2004-103957

[Non-Patent Documents]

[0007]

[Non-Patent Document 1] M. W. Prins, K. O. Grosse-Holz, G. Muller, J. F. M. Cillessen, J. B. Giesbers, R. P. Weening, and R. M. Wolf, "A ferroelectric transparent thin-film transistor", *Appl. Phys. Lett.*, 17 June 1996, Vol. 68 pp. 3650-3652

[Non-Patent Document 2] M. Nakamura, N. Kimizuka, and T. Mohri, "The Phase Relations in the In_2O_3-Ga_2ZnO_4-ZnO System at 1350 °C", *J. Solid State Chem.*, 1991, Vol. 93, pp. 298-315

[Non-Patent Document 3] N. Kimizuka, M. Isobe, and M. Nakamura, "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System", *J. Solid State Chem.*, 1995, Vol. 116, pp. 170-178

[Non-Patent Document 4] M. Nakamura, N. Kimizuka, T. Mohri, and M. Isobe, "Homologous Series, Synthesis and Crystal Structure of $InFeO_3(ZnO)m$ (m: natural number) and its Isostructural Compound", *KOTAI BUTSURI (SOLID STATE PHYSICS)*, 1993, Vol. 28, No. 5, pp. 317-327

[Non-Patent Document 5] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide

semiconductor", *SCIENCE*, 2003, Vol. 300, pp. 1269-1272

[Non-Patent Document 6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *NATURE*, 2004, Vol. 432 pp. 488-492

DISCLOSURE OF INVENTION

[0008]

A transistor including an oxide semiconductor with a wide band gap has a characteristic of a significantly small off current. On the other hand, the operation speed of a transistor including an oxide semiconductor is not sufficiently high as compared to that of a transistor including a semiconductor material other than an oxide semiconductor, such as single crystal silicon.

[0009]

In addition, although a transistor including a semiconductor material other than an oxide semiconductor, such as single crystal silicon, has high mobility and is capable of sufficiently high-speed operation, the off current thereof is not low enough to be regarded as substantially zero. Therefore, a slight amount of current flows regardless of the operation state of the semiconductor device, and thus it has been difficult to ensure a sufficient charge holding period in the case of fabrication of a charge-holding semiconductor device such as a memory device or a liquid crystal display device.

[0010]

Thus, an object of an embodiment of the disclosed invention is to provide a semiconductor device having a novel structure in which a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor are stacked.

[0011]

An embodiment of the present invention is a semiconductor device in which a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor are stacked.

[0012]

An embodiment of the present invention is a semiconductor device in which a transistor whose transistor characteristics are improved by forming an oxide semiconductor layer over a surface with favorable planarity is stacked over a transistor including a semiconductor material other than an oxide semiconductor. The following structures can be employed, for example.

[0013]

An embodiment of the present invention is a semiconductor device including a first transistor, an insulating layer over the first transistor, and a second transistor over the insulating layer. In this structure, the first transistor includes a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode overlapping with the first channel formation region, over the first gate insulating layer, and a first source electrode electrically connected to the first channel formation region and a first drain electrode electrically connected to the first channel formation region, and the second transistor includes a second channel formation region including an oxide semiconductor, a second source electrode electrically connected to the second channel formation region and a second drain electrode electrically connected to the second channel formation region, a second gate electrode overlapping with the second channel formation region, and a second gate insulating layer provided between the second channel formation region and the second gate electrode. In this structure, the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region, and the insulating layer includes a surface whose root-mean-square surface roughness is less than or equal to 1 nm.

[0014]

Note that it is preferable that a top surface of the first gate electrode be exposed to be included in the same surface as the insulating layer, and that the first gate electrode and the second source electrode or the second drain electrode be in contact with each other on the top surface of the first gate electrode.

[0015]

In addition, another embodiment of the present invention is a method for manufacturing a semiconductor device comprising the steps of forming a first transistor including a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode overlapping with the first channel formation region over the first gate insulating layer, a first source electrode layer electrically connected to the first channel formation region, and a first drain electrode electrically connected to the first channel formation region; forming an insulating layer over the first transistor; planarizing the insulating layer so that a surface of the insulating layer has a root-mean-square surface roughness of less than or equal to 1 nm; and forming a second transistor including a second channel formation region including an oxide semiconductor, a second source electrode electrically connected to the second channel formation region, a second drain electrode electrically connected to the second channel formation region, a second gate electrode overlapping with the second channel formation region, and a gate insulating layer provided between the second channel formation region and the second gate electrode, so as to be in contact with the insulating layer. In this structure, the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region.

[0016]

Further, another embodiment of the present invention is a method for manufacturing a semiconductor device, comprising the steps of forming a first transistor including a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode which overlaps with the first channel formation region and is provided over the first gate insulating layer, a first source electrode electrically connected to the first channel formation region, and a first drain electrode electrically connected to the first channel formation region; forming an insulating layer over the first transistor; planarizing the insulating layer so that a surface of the insulating layer has a root-mean-square roughness of less than or equal to 1 nm and a top surface of the first gate electrode is exposed to be included in the same surface as the insulating layer; and over the insulating layer,

forming a second transistor including a second channel formation region including an oxide semiconductor, a second source electrode electrically connected to the second channel formation region, a second drain electrode electrically connected to the second channel formation region, a second gate electrode provided to overlap with the second channel formation region, a second gate insulating layer provided between the second channel formation region and the second gate electrode. In this structure, the second source electrode or the second drain electrode are provided to be in contact with a top surface of the first gate electrode, and the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region.

[0017]

Note that the second channel formation region is preferably formed over the surface of the insulating layer. In addition, the surface of the insulating layer is preferably planarized by chemical mechanical polishing (CMP) treatment. Further, the first transistor preferably includes impurity regions with the first channel formation region provided therebetween.

[0018]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode. Moreover, the terms such as "over" and "below" are only used for convenience of description and can include the case where the relation of components is reversed, unless otherwise specified.

[0019]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term “electrode” or "wiring" can include the case where a plurality of "electrodes" or "wirings" is formed in an integrated manner.

[0020]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be used to denote the drain and the source, respectively, in this specification.

[0021]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between components that are connected through the object.

[0022]

Examples of an “object having any electric function” are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0023]

An embodiment of the present invention provides a semiconductor device in which a transistor including a semiconductor material other than an oxide semiconductor is included in a lower portion and a transistor including an oxide semiconductor is included in an upper portion.

[0024]

With a combination of a transistor including a semiconductor material other than an oxide semiconductor and a transistor including an oxide semiconductor as described above, a novel semiconductor device making use of advantages of characteristics of the respective transistors can be realized.

[0025]

In addition, a semiconductor device in which a transistor whose transistor characteristics are improved by forming an oxide semiconductor layer over a surface with favorable planarity is stacked over a transistor including a semiconductor

material other than an oxide semiconductor can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0026]

In the accompanying drawings:

FIG. 1 is a cross-sectional view of a semiconductor device;

FIGS. 2A to 2D are cross-sectional views according to a process for manufacturing a semiconductor device;

FIGS. 3A to 3C are cross-sectional views according to the process for manufacturing a semiconductor device;

FIGS. 4A to 4C are cross-sectional views according to the process for manufacturing a semiconductor device;

FIGS. 5A to 5C are cross-sectional views according to the process for manufacturing a semiconductor device;

FIGS. 6A and 6B are a cross-sectional view and a plan view of a semiconductor device;

FIGS. 7A and 7B are a cross-sectional view and a plan view of a semiconductor device;

FIGS. 8A and 8B are a cross-sectional view and a plan view of a semiconductor device;

FIGS. 9A and 9B are a cross-sectional view and a plan view of a semiconductor device;

FIGS. 10A to 10D are cross-sectional views according to a process for manufacturing a semiconductor device;

FIGS. 11A to 11C are cross-sectional views according to the process for manufacturing a semiconductor device;

FIGS. 12A to 12D are cross-sectional views according to the process for manufacturing a semiconductor device;

FIGS. 13A to 13C are cross-sectional views according to the process for manufacturing a semiconductor device;

FIGS. 14A and 14B are a cross-sectional view and a plan view of a semiconductor device;

FIGS 15A to 15H are cross-sectional views according to a process for manufacturing a semiconductor substrate used for manufacturing a semiconductor device;

FIGS. 16A to 16E are cross-sectional views according to a process for manufacturing a semiconductor device;

FIGS. 17A-1, 17A-2, and 17B are circuit diagrams of semiconductor devices;

FIGS. 18A and 18B are circuit diagrams of semiconductor devices;

FIGS. 19A to 19C are circuit diagrams of semiconductor devices;

FIGS. 20A to 20F are diagrams for illustrating electronic appliances using semiconductor devices;

FIG. 21 shows an AFM image of Example 1; and

FIG. 22 shows an AFM image of Example 1.

BEST MODE FOR CARRYING OUT THE INVENTION

[0027]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the invention should not be construed as being limited to the description in the following embodiment modes.

[0028]

Note that the position, the size, the range, or the like of each structure illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like.

[0029]

In this specification and the like, ordinal numbers such as "first", "second",

and "third" are used in order to avoid confusion among components, and the terms do not mean limitation of the number of components.

[0030]

[Embodiment 1]

A structure of a semiconductor device according to an embodiment of the disclosed invention and a method for manufacturing the semiconductor device will be described in this embodiment with reference to FIG. 1, FIGS. 2A to 2D, FIGS. 3A to 3C, FIGS. 4A to 4C, and FIGS. 5A to 5C.

[0031]

<Cross-sectional Structure of Semiconductor Device>

FIG. 1 is a cross-sectional view of an example of a structure of a semiconductor device. In the semiconductor device illustrated in FIG. 1, a transistor 160 including a first semiconductor material is included in a lower portion, and a transistor 162 including a second semiconductor material is included in an upper portion. Here, the first semiconductor material is preferably different from the second semiconductor material. For example, a semiconductor material other than an oxide semiconductor can be used as the first semiconductor material, and an oxide semiconductor can be used as the second semiconductor material. As the semiconductor material other than an oxide semiconductor, for example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used. In addition, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material other than an oxide semiconductor can operate at high speed easily. On the other hand, in a transistor including an oxide semiconductor, off current can be sufficiently reduced.

[0032]

For example, with the transistor 160 in the lower portion which includes the semiconductor material other than an oxide semiconductor, a logic circuit or driver circuit which needs high-speed operation can be formed. In addition, with the transistor 162 in the upper portion which includes an oxide semiconductor, a memory

circuit or a display element of a liquid crystal display device which needs sufficient charge holding period can be formed. When the transistors are provided in combination, a novel semiconductor device making use of advantages of characteristics of the respective transistors can be obtained.

[0033]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. The technical nature of the disclosed invention is that a transistor including an oxide semiconductor with sufficiently reduced off current and a transistor including a semiconductor material other than an oxide semiconductor which is capable of sufficiently high-speed operation are provided in combination; thus, it is not necessary to limit specific conditions, such as a material used for the semiconductor device or a structure of the semiconductor device, to the structure described here.

[0034]

The transistor 160 illustrated in FIG. 1 includes a channel formation region 116 provided in a substrate 100 including a semiconductor material (e.g., silicon), impurity regions 120 with the channel formation region 116 provided therebetween, metal compound regions 124 in contact with the impurity regions 120, a gate insulating layer 108 provided over the channel formation region 116, and a gate electrode 110 provided over the gate insulating layer 108. Note that a transistor whose source electrode and drain electrode are not illustrated in a drawing may be referred to as a transistor for the sake of convenience. Further, in such a case, in description of a connection of a transistor, a source region and a source electrode are collectively referred to as a "source electrode," and a drain region and a drain electrode are collectively referred to as a "drain electrode". In other words, in this specification, the term "source electrode" may include a source region and the term "drain electrode" may include a drain region.

[0035]

Further, an element isolation insulating layer 106 is provided over the substrate 100 so as to surround the transistor 160, and an insulating layer 128 and an

insulating layer 130 are provided over the transistor 160. Although not shown, part of the metal compound region 124 of the transistor 160 is connected to a wiring via an electrode functioning as a source electrode or a drain electrode. Note that in order to obtain high integration, the transistor 160 preferably does not have a sidewall insulating layer as illustrated in FIG. 1. On the other hand, in the case where characteristics of the transistor 160 are emphasized, a sidewall insulating layer may be provided on a side surface of the gate electrode 110 and the impurity regions 120 may include an impurity region having a different impurity concentration provided in a region overlapping with the sidewall insulating layer.

[0036]

The transistor 162 in FIG. 1 includes a source or drain electrode 142a and a source or drain electrode 142b which are provided over the insulating layer 130; an oxide semiconductor layer 144 electrically connected to the source or drain electrode 142a and the source or drain electrode 142b; a gate insulating layer 146 covering the source or drain electrode 142a, the source or drain electrode 142b, and the oxide semiconductor layer 144; a gate electrode 148a provided to overlap with the oxide semiconductor layer 144 over the gate insulating layer 146; an insulating layer 143a provided in a region between the source or drain electrode 142a and the oxide semiconductor layer 144, which overlaps with the gate electrode 148a; and an insulating layer 143b provided in a region between the source or drain electrode 142b and the oxide semiconductor layer 144, which overlaps with the gate electrode 148a. Note that in order to reduce capacitance between the source electrode or the drain electrode and the gate electrode, it is preferable to provide the insulating layer 143a and the insulating layer 143b. However, alternatively, a structure without the insulating layer 143a and the insulating layer 143b may be employed.

[0037]

Here, the oxide semiconductor layer 144 is preferably a highly-purified oxide semiconductor layer by sufficiently removing impurities such as hydrogen or sufficiently supplying oxygen. Specifically, the hydrogen concentration of the oxide semiconductor layer 144 is less than or equal to 5×10^{19} atoms/cm^3, preferably less

than or equal to 5×10^{18} atoms/cm^3, more preferably less than or equal to 5×10^{17} atoms/cm^3. Note that the hydrogen concentration of the oxide semiconductor layer 144 is measured by secondary ion mass spectrometry (SIMS). In the oxide semiconductor layer 144 which is highly purified by sufficiently reducing the hydrogen concentration and in which a defect level in an energy gap due to oxygen deficiency is reduced by supplying a sufficient amount of oxygen, the carrier concentration resulted from hydrogen, an oxygen deficiency, or the like is less than 1×10^{12} /cm^3, preferably less than 1×10^{11} /cm^3, or more preferably less than 1.45×10^{10} /cm^3. It is possible to sufficiently reduce off current in the transistor including the oxide semiconductor layer 144. For example, in a transistor in which the oxide semiconductor layer 144 has a thickness of 30 nm and a channel length is 2 μm, off current (a gate bias: −3 V) per channel length of 1 μm at room temperature (25 °C) is less than or equal to 100 zA (1 zA (zeptoampere) is equal to 1×10^{-21} A), or preferably less than or equal to 10 zA. In this manner, by using the highly-purified oxide semiconductor (hereinafter, which is referred to as an i-type (intrinsic) or substantially-i-type oxide semiconductor in this specification), the transistor 162 with excellent off-current characteristics can be obtained.

[0038]

Here, the oxide semiconductor layer 144 is provided over the insulating layer 130 including a surface whose root-mean-square (RMS) roughness is less than or equal to 1 nm, preferably less than or equal to 0.5 nm. In this manner, by providing the oxide semiconductor layer 144 over the surface with favorable planarity, the oxide semiconductor layer 144 can have favorable planarity and uniformity. Note that at least a portion including the channel formation region of the oxide semiconductor layer may have favorable planarity and uniformity. In addition, by using the oxide semiconductor layer 144 with favorable planarity and uniformity, transistor characteristics of the transistor 162 can be improved. In particular, in the case where the thickness of the oxide semiconductor layer 144 is approximately 10 nm or less, when the oxide semiconductor layer 144 is provided over such a surface with favorable planarity, breaking of the oxide semiconductor layer 144 or the like can be

prevented.

[0039]

By using the oxide semiconductor layer 144 with favorable planarity and uniformity, carrier scattering can be prevented and an interface level can be reduced at an interface with the oxide semiconductor layer. Accordingly, improvement in mobility, reduction in an S-value and off current, and improvement in transistor characteristics are possible in the transistor 162. In addition, improvement in the planarity of the oxide semiconductor layer 144 leads to reduction in gate leakage current of the transistor 162.

[0040]

Note that in this specification and the like, root-mean-square (RMS) roughness is measured using an atomic force microscope (AFM) with a measurement area of 1 μm × 1 μm.

[0041]

In addition, in this specification and the like, an RMS roughness is obtained by three-dimensionally expanding the RMS roughness of a cross section curve so as to be able to apply to the measurement surface. The RMS can be expressed as the square root of the average value of squares of deviations from the reference surface to the specific surface, and can be obtained by the following formula.

[0042]

[FORMULA 1]

$$R_{ms} = \sqrt{\frac{1}{S_0}\int_{Y_1}^{Y_2}\int_{X_1}^{X_2}\{F(X,Y) - Z_0\}^2 dXdY}$$

[0043]

Note that the measurement surface is a surface which is shown by all the measurement data, and is represented by the following formula.

[0044]

[FORMULA 2]

$$Z = F(X,Y)$$

[0045]

The specific surface is a surface which is an object of roughness measurement, and is a rectangular region which is surrounded by four points represented by the coordinates (X_1, Y_1), (X_1, Y_2), (X_2, Y_1), and (X_2, Y_2). The area of the specific surface when the specific surface is flat ideally is denoted by S_0. Note that S_0 is obtained by the following formula.

[0046]

[FORMULA 3]

$$S_0 = |X_2 - X_1| \cdot |Y_2 - Y_1|$$

[0047]

In addition, the reference surface refers to a surface parallel to an X-Y surface at the average height of the specific surface. In short, when the average value of the height of the specific surface is denoted by Z_0, the height of the reference surface is also denoted by Z_0. Note that Z_0 can be obtained by the following formula.

[0048]

[FORMULA 4]

$$Z_0 = \frac{1}{S_0}\int_{Y_1}^{Y_2}\int_{X_1}^{X_2} F(X, Y)dXdY$$

[0049]

Although the oxide semiconductor layer 144 which is processed to have an island shape is used in order to suppress leakage current generated between elements due to miniaturization in the transistor 162 of FIG. 1, a structure including the oxide semiconductor layer 144 which is not processed to have an island shape may be employed. In the case where the oxide semiconductor layer is not processed to have an island shape, contamination of the oxide semiconductor layer 144 due to etching in the processing can be prevented.

[0050]

Note that in the transistor 162, edge portions of the source or drain electrode 142a and the source or drain electrode 142b are preferably tapered. The end portions

of the source or drain electrode 142a and the source or drain electrode 142b are tapered, whereby coverage of the oxide semiconductor layer 144 can be improved and breaking can be prevented. Here, a taper angle is, for example, greater than or equal to 30° and less than or equal to 60°. Note that the "taper angle" means an inclination angle formed by a side surface and a bottom surface of a layer (for example, the source or drain electrode 142a) having a tapered shape when being observed in a direction perpendicular to the cross-section (a plane which is perpendicular to the surface of the substrate).

[0051]

Further, an insulating layer 150 is provided over the transistor 162 and an insulating layer 152 is provided over the insulating layer 150. A wiring 156 connected to the transistor 160 or the transistor 162 is provided over the insulating layer 152.

[0052]

<Method for manufacturing semiconductor device>

Next, an example of a method for manufacturing the semiconductor device will be described. First, a method for manufacturing the transistor 160 in the lower portion will be described below with reference to FIGS. 2A to 2D and FIGS. 3A to 3C, and then a method for manufacturing the transistor 162 in the upper portion will be described with reference to FIGS. 4A to 4C and FIGS. 5A to 5C.

[0053]

<Method for manufacturing transistor in lower portion>

First, the substrate 100 including a semiconductor material is prepared (see FIG. 2A). As the substrate 100 including a semiconductor material, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like; a compound semiconductor substrate made of silicon germanium or the like; an SOI substrate; or the like can be used. Here, an example of using a single crystal silicon substrate as the substrate 100 including a semiconductor material is described. Note that in general, the term "SOI substrate" means a substrate where a silicon semiconductor layer is provided on an insulating

surface. In this specification and the like, the term "SOI substrate" also includes a substrate where a semiconductor layer formed using a material other than silicon is provided over an insulating surface in its category. That is, a semiconductor layer included in the "SOI substrate" is not limited to a silicon semiconductor layer. Moreover, the SOI substrate can be a substrate having a structure in which a semiconductor layer is provided over an insulating substrate such as a glass substrate, with an insulating layer provided therebetween.

[0054]

The case where a single crystal semiconductor substrate such as a single crystal silicon substrate is used as the substrate 100 including a semiconductor material is preferable because the transistor 160 can be operated at higher speed.

[0055]

A protective layer 102 serving as a mask for forming an element isolation insulating layer is formed over the substrate 100 (see FIG. 2A). As the protective layer 102, for example, an insulating layer formed using silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, or the like can be used. Note that before or after this step, an impurity element imparting n-type conductivity or an impurity element imparting p-type conductivity may be added to the substrate 100 in order to control the threshold voltage of the transistor. When the semiconductor is formed using silicon, phosphorus, arsenic, or the like can be used as the impurity imparting n-type conductivity. Boron, aluminum, gallium, or the like can be used as the impurity imparting p-type conductivity.

[0056]

Next, part of the substrate 100 in a region that is not covered with the protective layer 102 (i.e., an exposed region) is removed by etching with the use of the protective layer 102 as a mask. Thus, a semiconductor region 104 which is apart from another semiconductor region is formed (see FIG. 2B). As the etching, dry etching is preferably performed, but wet etching can be performed. An etching gas and an etchant can be selected as appropriate depending on a material of layers to be etched.

[0057]

Next, an insulating layer is formed so as to cover the semiconductor region 104 and a region of the insulating layer which overlaps with the semiconductor region 104 is selectively removed, so that the element isolation insulating layer 106 is formed (see FIG. 2C). The insulating layer is formed using silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, or the like. As a method for removing the insulating layer, polishing treatment such as chemical mechanical polishing (CMP), etching treatment, or the like can be given, and any of the above treatment may be used or a combination thereof may be used. Note that the protective layer 102 is removed after the formation of the semiconductor region 104 or after the formation of the element isolation insulating layer 106.

[0058]

Note that as a method for forming the element isolation insulating layer 106, a method in which an insulating region is formed by introduction of oxygen, or the like can be used instead of the method in which the insulating layer is selective etched.

[0059]

Next, an insulating layer is formed over a surface of the semiconductor region 104, and a layer including a conductive material is formed over the insulating layer.

[0060]

The insulating layer is to be a gate insulating layer later and can be formed by performing heat treatment (e.g., thermal oxidation treatment or thermal nitridation treatment) on the surface of the semiconductor region 104, for example. Instead of heat treatment, high-density plasma treatment may be employed. The high-density plasma treatment can be performed using, for example, a mixed gas of a rare gas such as He, Ar, Kr, or Xe and any of oxygen, nitrogen oxide, ammonia, nitrogen, and hydrogen. Needless to say, the insulating layer may be formed using a CVD method, a sputtering method, or the like. The insulating layer preferably has a single-layer structure or a stacked structure using a film including any of silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium

silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, and the like. The thickness of the insulating layer can be, for example, greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0061]

The layer including a conductive material can be formed using a metal material such as aluminum, copper, titanium, tantalum, or tungsten. The layer containing a conductive material may be formed using a semiconductor material such as polycrystalline silicon. There is no particular limitation on the method for forming the layer containing a conductive material, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, or a spin coating method can be used. Note that this embodiment describes an example of the case where the layer containing a conductive material is formed using a metal material.

[0062]

After that, the insulating layer and the layer including a conductive material are selectively etched, so that the gate insulating layer 108 and the gate electrode 110 are formed (see FIG. 2C).

[0063]

Next, phosphorus (P), arsenic (As), or the like is added to the semiconductor region 104, so that the channel formation region 116 and the impurity regions 120 are formed (see FIG. 2D). Note that phosphorus or arsenic is added here in order to form an n-channel transistor, an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. Here, the concentration of the impurity added can be set as appropriate; the concentration is preferably increased when the size of a semiconductor element is extremely decreased.

[0064]

Note that a sidewall insulating layer may be formed in the periphery of the gate electrode 110 so that an impurity region to which an impurity element is added at

a different concentration may be formed.

[0065]

Next, a metal layer 122 is formed so as to cover the gate electrode 110, the impurity regions 120, and the like (see FIG. 3A). A variety of deposition methods such as a vacuum evaporation method, a sputtering method, or a spin coating method can be employed for forming the metal layer 122. The metal layer 122 is preferably formed using a metal material that reacts with a semiconductor material contained in the semiconductor region 104 to be a low-resistance metal compound. Examples of such metal materials include titanium, tantalum, tungsten, nickel, cobalt, and platinum.

[0066]

Next, heat treatment is performed so that the metal layer 122 reacts with the semiconductor material. Thus, the metal compound regions 124 that are in contact with the impurity regions 120 are formed (see FIG. 3A). Note that when the gate electrode 110 is formed using polycrystalline silicon or the like, a metal compound region is also formed in a region of the gate electrode 110 in contact with the metal layer 122.

[0067]

As the heat treatment, irradiation with a flash lamp can be employed, for example. Although it is needless to say that another heat treatment method may be used, a method by which heat treatment for an extremely short time can be achieved is preferably used in order to improve the controllability of chemical reaction in formation of the metal compound. Note that the metal compound regions are formed by reaction of the metal material and the semiconductor material and have sufficiently high conductivity. The formation of the metal compound regions can properly reduce the electric resistance and improve element characteristics. Note that the metal layer 122 is removed after the metal compound regions 124 are formed.

[0068]

Then, the insulating layer 128 and the insulating layer 130 are formed so as to cover the components formed through the above steps (see FIG. 3B). The insulating

layer 128 and the insulating layer 130 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, or aluminum oxide. In particular, the insulating layer 128 and the insulating layer 130 are preferably formed using a low dielectric constant (low-k) material, whereby capacitance caused by an overlap of electrodes or wirings can be sufficiently reduced. Note that a porous insulating layer including these materials may be used for the insulating layer 128 and the insulating layer 130. Since the porous insulating layer has low dielectric constant as compared to a dense insulating layer, capacitance due to electrodes or wirings can be further reduced.

[0069]

In addition, a layer including an inorganic material containing a large amount of nitride, such as silicon nitride oxide or silicon nitride, may be included in the insulating layer 128 or the insulating layer 130. Thus, the impurity such as water or hydrogen contained in the material included in the transistor 160 in the lower portion can be prevented from entering the oxide semiconductor layer 144 of the transistor 162 in the upper portion that is formed later. Note that in this case, it is difficult to remove the layer including an inorganic insulating material containing a large amount of nitrogen only by CMP treatment performed in a later step; therefore, CMP treatment and etching treatment are preferably performed in combination.

[0070]

For example, silicon oxynitride and silicon oxide are used for forming the insulating layer 128 and the insulating layer 130, respectively. In this manner, only an inorganic insulating material containing a large amount of oxygen, such as silicon oxynitride or silicon oxide, is used for the insulating layer 128 and the insulating layer 130, whereby CMP treatment can be easily performed on the insulating layer 128 and the insulating layer 130 in a later step.

[0071]

Note that a stacked structure of the insulating layer 128 and the insulating layer 130 is employed here; however, one embodiment of the disclosed invention is not limited to this. A single-layer structure or a stacked structure including three or

more layers can also be used. For example, the following structure may be employed: silicon oxynitride and silicon oxide are used for the insulating layer 128 and the insulating layer 130, respectively, and a silicon nitride oxide film is formed between the insulating layer 128 and the insulating layer 130.

[0072]

Note that in this specification, "silicon oxynitride" contains more oxygen than nitrogen, and "silicon nitride oxide" contains more nitrogen than oxygen.

[0073]

Through the above steps, the transistor 160 using the substrate 100 including a semiconductor material is formed (see FIG. 3B). Such a transistor 160 is capable of high-speed operation.

[0074]

After that, as treatment before formation of the transistor 162, chemical mechanical polishing (CMP) treatment is performed on the insulating layer 128 and the insulating layer 130, so that surfaces of the insulating layer 128 and the insulating layer 130 are planarized (see FIG. 3C). Here, the CMP treatment is treatment of planarizing a surface of an object to be processed by a combination of chemical and mechanical actions using the surface as a reference. In general, the CMP treatment is treatment in which a polishing cloth is attached to a polishing stage, the polishing stage and the object to be processed are each rotated or swung while a slurry (an abrasive) is supplied between the object to be processed and the polishing cloth, and the surface of the object to be processed is polished by chemical reaction between the slurry and the surface of the object to be processed and by action of mechanical polishing of the object to be processed with the polishing cloth.

[0075]

The CMP treatment may be performed once or plural times. When the CMP treatment is performed plural times, first polishing is preferably performed with a high polishing rate followed by final polishing with a low polishing rate. By combining polishing with different polishing rates, planarity of the surfaces of the insulating layer 128 and the insulating layer 130 can be further improved.

[0076]

As the treatment for planarizing the insulating layer 128 and the insulating layer 130, etching treatment or the like can be performed instead of CMP treatment, and planarization is preferably performed so that each of the surfaces of the insulating layer 128 and the insulating layer 130 has an RMS roughness of less than or equal to 1 nm, or preferably less than or equal to 0.5 nm in order to improve the planarity and the uniformity of the oxide semiconductor layer 144 and improve characteristics of the transistor 162.

[0077]

In addition, when the stacked layer structure of the insulating layer 128 and the insulating layer 130 includes an inorganic insulating material containing a large amount of nitrogen, such as silicon nitride or silicon nitride oxide, since it is difficult to remove the inorganic insulating material containing a large amount of nitrogen only by the CMP treatment, CMP treatment and etching treatment are preferably performed in combination. As the etching treatment for the inorganic insulating material containing a large amount of nitrogen, either dry etching or wet etching may be used. However, in view of miniaturization of elements, dry etching is preferably used. In addition, it is preferable that etching conditions (an etching gas, an etchant, an etching time, a temperature, or the like) be set appropriately so that etching rates of the respective insulating layers are equal to each other. In addition, as an etching gas for dry etching, for example, a gas containing fluorine (trifluoromethane (CHF_3)), a gas to which a rare gas such as helium (He) or argon (Ar) is added, or the like can be used.

[0078]

Note that before or after the above steps, a step for forming an additional electrode, wiring, semiconductor layer, or insulating layer may be performed. For example, a multilayer wiring structure in which an insulating layer and a conductive layer are stacked is employed as a wiring structure, so that a highly-integrated semiconductor device can be provided.

[0079]

<Method for manufacturing transistor in upper portion>

A conductive layer is formed over the gate electrode 110, the insulating layer 128, the insulating layer 130, and the like, and the conductive layer is etched selectively, so that the source or drain electrode 142a and the source or drain electrode 142b are formed (see FIG. 4A).

[0080]

The conductive layer can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. As a material for the conductive layer, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of these elements as a component; or the like can be used. Any of manganese, magnesium, zirconium, beryllium, neodymium, and scandium or a material including any of these in combination may be used.

[0081]

The conductive layer can have a single-layer structure or a stacked structure including two or more layers. For example, a single-layer structure of a titanium film or a titanium nitride film, a single-layer structure of an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given. Note that in the case where the conductive layer has a single-layer structure of a titanium film or a titanium nitride film, there is an advantage that the conductive layer is easily processed into the source or drain electrode 142a and the source or drain electrode 142b having tapered shapes.

[0082]

The conductive layer may also be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), an indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials in which silicon or silicon oxide is included can be used.

[0083]

The conductive layer is preferably etched so that edge portions of the source or drain electrode 142a and the source or drain electrode 142b are tapered. Here, the tapered angle is preferably greater than or equal to 30° and less than or equal to 60°, for example. The edge portions of the source or drain electrode 142a and the source or drain electrode 142b are etched so as to be tapered; accordingly, the coverage with the gate insulating layer 146 to be formed later is improved and breaking can be prevented.

[0084]

The channel length (*L*) of the transistor in the upper portion is determined by a distance between a lower edge portion of the source or drain electrode 142a and a lower edge portion of the source or drain electrode 142b. Note that for light exposure for forming a mask used in the case where a transistor with a channel length (*L*) of less than 25 nm is formed, it is preferable to use extreme ultraviolet rays whose wavelength is as short as several nanometers to several tens of nanometers. In the light exposure by extreme ultraviolet light, the resolution is high and the focus depth is large. For these reasons, the channel length (*L*) of the transistor to be formed later can be in the range of greater than or equal to 10 nm and less than or equal to 1000 nm (1 μm), and the circuit can operate at higher speed. Moreover, miniaturization can lead to low power consumption of a semiconductor device.

[0085]

Note that an insulating layer functioning as a base may be provided over the insulating layer 128 and the insulating layer 130. The insulating layer can be formed by a PVD method, a CVD method, or the like. In this case, the formed insulating layer preferably includes a surface having an RMS roughness of less than or equal to 1 nm, or preferably less than or equal to 0.5 nm.

[0086]

Next, the insulating layer 143a and the insulating layer 143b are formed over the source or drain electrode 142a and the source or drain electrode 142b, respectively (see FIG. 4B). The insulating layer 143a and the insulating layer 143b can be formed in such a manner that an insulating layer covering the source or drain electrode 142a

and the source or drain electrode 142b is formed, and then the insulating layer is selectively etched. In addition, the insulating layer 143a and the insulating layer 143b are formed so as to overlap with part of the gate electrode formed later. By providing such an insulating layer, capacitance between the gate electrode and the source or drain electrode can be reduced.

[0087]

The insulating layer 143a and the insulating layer 143b can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, or aluminum oxide. In particular, it is preferable that the insulating layer 143a and the insulating layer 143b are formed using a low dielectric constant (low-k) material, because capacitance between the gate electrode and the source or drain electrode can be sufficiently reduced. Note that a porous insulating layer including any of these materials may be used for the insulating layer 143a and the insulating layer 143b. Since the porous insulating layer has low dielectric constant as compared to a dense insulating layer, capacitance between the gate electrode and the source or drain electrode can be further reduced.

[0088]

Note that in view of reduction in the capacitance between the gate electrode and the source or drain electrode, the insulating layer 143a and the insulating layer 143b are preferably formed; however, a structure without the insulating layer 143a and the insulating layer 143b may be employed.

[0089]

Next, an oxide semiconductor layer is formed so as to cover the source or drain electrode 142a and the source or drain electrode 142b, and then the oxide semiconductor layer is selectively etched, so that the oxide semiconductor layer 144 is formed (see FIG. 4C).

[0090]

As the oxide semiconductor layer can be used using an In-Sn-Ga-Zn-O-based oxide semiconductor which is a four-component metal oxide; an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an

In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, or a Sn-Al-Zn-O-based oxide semiconductor which are three-component metal oxides; an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, or an In-Mg-O-based oxide semiconductor which are two-component metal oxides; an In-O-based oxide semiconductor; a Sn-O-based oxide semiconductor; or a Zn-O-based oxide semiconductor.

[0091]

In particular, an In-Ga-Zn-O-based oxide semiconductor material has sufficiently high resistance when there is no electric field and thus off current can be sufficiently reduced. In addition, with high field-effect mobility, the In-Ga-Zn-O-based oxide semiconductor material is suitable for a semiconductor device.

[0092]

As a typical example of the In-Ga-Zn-O-based oxide semiconductor material, one represented by $InGaO_3(ZnO)_m$ ($m>0$) is given. Using M instead of Ga, there is an oxide semiconductor material represented by $InMO_3(ZnO)_m$ ($m > 0$). Here, M denotes one or more metal elements selected from gallium (Ga), aluminum (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), and the like. For example, *M* may be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the above-described compositions are derived from the crystal structures that the oxide semiconductor material can have and are mere examples.

[0093]

As a target for forming the oxide semiconductor layer by a sputtering method, a target having a composition ratio of In:Ga:Zn = 1:x:y (x is 0 or more and y is more than or equal to 0.5 and less than or equal to 5) is preferably used. For example, a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio], or the like can be used. Alternatively, a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio], a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:4

[molar ratio], or a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:0:2 [molar ratio] can be used.

[0094]

In this embodiment, the oxide semiconductor layer is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target.

[0095]

The relative density of a metal oxide in the metal oxide target is 80% or more, preferably 95% or more, more preferably 99.9% or more. The use of a metal oxide target having high relative density makes it possible to form the oxide semiconductor layer with a dense structure.

[0096]

The atmosphere in which the oxide semiconductor layer is formed is preferably a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas (typically argon) and oxygen. Specifically, it is preferable to use a high-purity gas atmosphere from which impurities such as hydrogen, water, hydroxyl, and hydride are removed so that the concentration thereof is decreased to 1 ppm or less (preferably, 10 ppb or less).

[0097]

In forming the oxide semiconductor layer, the object is held in a treatment chamber that is maintained at reduced pressure and is heated so that the temperature of the object is higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of the object in the formation of the oxide semiconductor layer may be room temperature (25 °C ± 10 °C). Then, a sputtering gas from which hydrogen, water, and the like are removed is introduced into the treatment chamber while moisture in the treatment chamber is removed, whereby the oxide semiconductor layer is formed using the above target. By forming the oxide semiconductor layer while heating the object, impurities in the oxide semiconductor layer can be reduced. In addition, damage due to the sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For

example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. A turbo pump provided with a cold trap may be used. By performing evacuation with the use of a cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber; thus, the impurity concentration in the oxide semiconductor layer can be reduced.

[0098]

The oxide semiconductor layer can be formed under the following conditions, for example: the distance between the object and the target is 170 mm, the pressure is 0.4 Pa, the direct current (DC) power is 0.5 kW, and the atmosphere is an oxygen (oxygen: 100%) atmosphere, an argon (argon: 100%) atmosphere, or a mixed atmosphere including oxygen and argon. Note that a pulsed direct-current (DC) power source is preferably used because dust (such as powder substances formed at the time of the film formation) can be reduced and the film thickness can be uniform. The thickness of the oxide semiconductor layer is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 1 nm and less than or equal to 30 nm, more preferably greater than or equal to 1 nm and less than or equal to 10 nm. With the oxide semiconductor layer having such a thickness, a short-channel effect which occurs along with miniaturization can be suppressed. Note that the appropriate thickness varies depending on the material for the oxide semiconductor, the usage of the semiconductor device, or the like, and thus the thickness can be selected as appropriate depending on the material, the usage, or the like.

[0099]

Here, the oxide semiconductor layer 144 is provided over the insulating layer 130 including the surface having an RMS roughness of less than or equal to 1 nm, or preferably less than or equal to 0.5 nm. When the oxide semiconductor layer 144 is provided over the surface having favorable planarity in this manner, favorable planarity and uniformity of the oxide semiconductor layer 144 can be obtained. Further, by using the oxide semiconductor layer 144 with favorable planarity and uniformity, transistor characteristics of the transistor 162 can be improved.

[0100]

Note that before the oxide semiconductor layer is formed by a sputtering method, reverse sputtering in which plasma is generated with an argon gas introduced is preferably performed, so that dust attached to a surface on which the oxide semiconductor layer is formed (e.g., a surface of the insulating layer 130) is removed. Here, the reverse sputtering is a method by which ions collide with a surface to be processed of a substrate so that the surface is modified, in contrast to normal sputtering by which ions collide with a sputtering target. An example of a method for making ions collide with a surface to be processed is a method in which high-frequency voltage is applied to the surface in an argon atmosphere so that plasma is generated near an object. Note that an atmosphere of nitrogen, helium, oxygen, or the like may be used instead of an argon atmosphere.

[0101]

After that, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer. Excessive hydrogen (including water and hydroxyl group) in the oxide semiconductor layer is removed by the first heat treatment and a structure of the oxide semiconductor layer is improved, so that a defect level in energy gap of the oxide semiconductor layer can be reduced. The temperature of the first heat treatment is set to higher than or equal to 300 °C and lower than 550 °C, or higher than or equal to 400 °C and lower than or equal to 500 °C.

[0102]

The heat treatment can be performed in such a way that, for example, an object is introduced into an electric furnace in which a resistance heating element or the like is used and heated, in a nitrogen atmosphere at 450 °C for one hour. During the heat treatment, the oxide semiconductor layer is not exposed to the air to prevent the entry of water and hydrogen.

[0103]

The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object by thermal conduction or thermal radiation from a medium such as a heated gas. For example, an RTA (rapid thermal anneal) apparatus such as a GRTA (gas rapid thermal anneal) apparatus or an LRTA (lamp rapid thermal

anneal) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0104]

For example, as the first heat treatment, a GRTA process may be performed as follows. The object is put in an inert gas atmosphere that has been heated, heated for several minutes, and taken out from the inert gas atmosphere. The GRTA process enables high-temperature heat treatment for a short time. Moreover, the GRTA process can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas may be switched to a gas including oxygen during the process. This is because defect level in energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere including oxygen.

[0105]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into the heat treatment apparatus is greater than or equal to 6N (99.9999%), preferably greater than or equal to 7N (99.99999%) (that is, the impurity concentration is less than or equal to 1 ppm, preferably less than or equal to 0.1 ppm).

[0106]

In any case, the i-type (intrinsic) or substantially i-type oxide semiconductor layer in which impurities are reduced by the first heat treatment is formed, which enables a transistor having excellent characteristics to be realized.

[0107]

The above heat treatment (the first heat treatment) can be referred to as dehydration treatment, dehydrogenation treatment, or the like because of its effect of removing hydrogen, water, and the like. The dehydration treatment or dehydrogenation treatment can be performed, for example, after the oxide semiconductor layer is formed, after the gate insulating layer is formed, or after the gate electrode is formed. Such dehydration treatment or dehydrogenation treatment may be conducted once or also plural times.

[0108]

The oxide semiconductor layer may be etched either before or after the heat treatment. In view of miniaturization of elements, dry etching is preferably used; however, wet etching may be used. An etching gas and an etchant can be selected as appropriate depending on a material of layers to be etched. Note that in the case where leakage current in an element does not cause a problem, the oxide semiconductor layer may be used without being processed to have an island shape.

[0109]

Next, the gate insulating layer 146 in contact with the oxide semiconductor layer 144 is formed, and then the gate electrode 148a is formed in a region overlapping with the oxide semiconductor layer 144, over the gate insulating layer 146 (see FIG. 5A).

[0110]

The gate insulating layer 146 can be formed by a CVD method, a sputtering method, or the like. The gate insulating layer 146 is preferably formed so as to include silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, tantalum oxide, hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, or the like. Note that the gate insulating layer 146 may have a single-layer structure or a stacked structure. There is no particular limitation on the thickness thereof; however, in the case where the semiconductor device is miniaturized, the thickness is preferably small for ensuring operation of the transistor. For example, in the case where silicon

oxide is used, the thickness can be set to greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0111]

When the gate insulating layer is thin as in the above description, a problem of gate leakage due to a tunnel effect or the like is caused. In order to solve the problem of gate leakage, it is preferable that the gate insulating layer 146 be formed using a high dielectric constant (high-k) material such as hafnium oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, or hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added. By using a high-k material for the gate insulating layer 146, electrical characteristics can be ensured and the thickness can be large to prevent gate leakage. Note that a layered structure of a film containing a high-k material and a film containing any one of silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, and the like may be employed.

[0112]

After the gate insulating layer 146 is formed, second heat treatment is desirably performed in an inert gas atmosphere or an oxygen atmosphere. The heat treatment is performed at a temperature higher than or equal to 200 °C and lower than or equal to 450 °C, or preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for one hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electrical characteristics of the transistor. Further, in the case where the gate insulating layer 146 contains oxygen, oxygen is supplied to the oxide semiconductor layer 144 to cover oxygen deficiency in the oxide semiconductor layer 144, so that an i-type (intrinsic semiconductor) or substantially i-type oxide semiconductor layer can be formed.

[0113]

Note that in this embodiment, the second heat treatment is performed after the gate insulating layer 146 is formed; the timing of the second heat treatment is not

limited thereto. For example, the second heat treatment may be performed after the gate electrode is formed. Alternatively, the second heat treatment may be performed following the first heat treatment, the first heat treatment may double as the second heat treatment, or the second heat treatment may double as the first heat treatment.

[0114]

As described above, at least one of the first heat treatment and the second heat treatment is performed, so that the oxide semiconductor layer 144 can be highly purified so as to contain impurities which are not main components as little as possible.

[0115]

The gate electrode 148a can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then selectively etched. The conductive layer to be the gate electrode 148a can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source or drain electrode 142a or the like; thus, the description thereof can be referred to.

[0116]

Next, the insulating layer 150 and the insulating layer 152 are formed over the gate insulating layer 146 and the gate electrode 148a (see FIG. 5B). The insulating layer 150 and the insulating layer 152 can be formed by a PVD method, a CVD method, or the like. The insulating layer 150 and the insulating layer 152 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, hafnium oxide, or aluminum oxide.

[0117]

Note that a low dielectric constant material or a structure having a low dielectric constant (e.g., a porous structure) is preferably employed for the insulating layer 150 and the insulating layer 152 because when the insulating layer 150 and the insulating layer 152 each have a low dielectric constant, capacitance generated between wirings, electrodes, or the like can be reduced and thus, high-speed operation

can be obtained.

[0118]

Note that a stacked structure of the insulating layer 150 and the insulating layer 152 is used in this embodiment, but an embodiment of the disclosed invention is not limited thereto. A single-layer structure or a stacked structure including three or more layers can also be used. Alternatively, the insulating layer may be omitted.

[0119]

Note that the insulating layer 152 is preferably formed so as to have a planarized surface. By forming the insulating layer 152 so as to have a planarized surface, an electrode, a wiring, or the like can be favorably formed over the insulating layer 152 even in the case where the semiconductor device is miniaturized, for example. The insulating layer 152 can be planarized using a method such as CMP.

[0120]

An electrode (not shown) for electrically connecting the transistor 160 or the transistor 162 and the wiring 156 is formed, and then the wiring 156 is formed over the insulating layer 152 (see FIG. 5C). Needless to say, all of these elements are not electrically connected to each other necessarily. An element independent of the other elements may be included.

[0121]

The wiring 156 is formed in such a manner that a conductive layer is formed using a PVD method including a sputtering method or a CVD method such as a plasma CVD method and then the conductive layer is patterned. As a material of the conductive layer, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy containing any of these elements as a component; or the like can be used. Moreover, one or more materials selected from manganese, magnesium, zirconium, beryllium, neodymium, or scandium may be used. The details are similar to those of the source or drain electrode 142a or the like.

[0122]

Through the above steps, the transistor 162 using the highly-purified oxide semiconductor layer 144 is completed (see FIG. 5C).

[0123]

With the use of the highly-purified intrinsic oxide semiconductor layer 144, off current of the transistor 162 can be sufficiently reduced.

[0124]

As described above, the semiconductor device can be provided, in which the transistor including a semiconductor material other than an oxide semiconductor is included in the lower portion and the transistor including an oxide semiconductor is included in the upper portion.

[0125]

With a combination of the transistor including a semiconductor material other than an oxide semiconductor and the transistor including an oxide semiconductor as described above, a novel semiconductor device making use of advantages of characteristics of the respective transistors can be realized.

[0126]

In addition, the semiconductor device can be provided, in which the transistor whose transistor characteristics are improved by providing the oxide semiconductor layer over the surface with favorable planarity is stacked over the transistor including a semiconductor material other than an oxide semiconductor.

[0127]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0128]

[Embodiment 2]

In this embodiment, a structure and a method for manufacturing a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 6A and 6B, FIGS. 7A and 7B, FIGS. 8A and 8B, FIGS. 9A and 9B, FIGS. 10A to 10D, FIGS. 11A to 11C, FIGS. 12A to 12D, and FIGS. 13A to 13C. In particular, an example of a structure of a semiconductor device which can be used as a memory device will be described in this embodiment.

[0129]

<Cross-sectional structure and planar structure of semiconductor device>

FIGS. 6A and 6B illustrate an example of a structure of a semiconductor device. FIG. 6A illustrates a cross section of the semiconductor device, and FIG. 6B illustrates a plan view of the semiconductor device. Here, FIG. 6A corresponds to a cross section along line A1-A2 and line B1-B2 in FIG. 6B. In the semiconductor device illustrated in FIGS. 6A and 6B, a transistor 260 including a first semiconductor material is provided in a lower portion, a transistor 262 including a second semiconductor material is provided in an upper portion, and a gate electrode 210 of the transistor 260 and a source or drain electrode 242a of the transistor 262 are directly connected to each other. Here, the first semiconductor material is preferably different from the second semiconductor material. For example, a semiconductor material other than an oxide semiconductor can be used as the first semiconductor material and an oxide semiconductor can be used as the second semiconductor material. Note that as the semiconductor material other than an oxide semiconductor, for example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material may be used. The transistor 260 including such a semiconductor material can be operated at high speed easily. On the other hand, the transistor 262 including an oxide semiconductor has off current which is sufficiently reduced, so that the transistor 262 can hold charge for a long time.

[0130]

Therefore, when the transistor 262 is in an off state, the potential of the gate electrode 210 of the transistor 260 can be held for an extremely long time. When a capacitor 264 is provided, electric charge supplied to the gate electrode 210 of the transistor 260 can be held easily and reading of held data can be performed easily. In addition, since the transistor 260 including such a semiconductor material is capable of operating at sufficiently high speed, reading speed of data can be improved.

[0131]

Although all the transistors are n-channel transistors here, it is needless to say

that p-channel transistors can be used. The technical nature of the disclosed invention is that a transistor including an oxide semiconductor with sufficiently reduced off current and a transistor including a semiconductor material other than an oxide semiconductor which is capable of sufficiently high-speed operation are provided in combination; thus, it is not necessary to limit specific conditions, such as a material used for the semiconductor device or a structure of the semiconductor device, to the structure described here.

[0132]

The transistor 260 illustrated in FIGS. 6A and 6B includes a channel formation region 216 provided in a substrate 200 including a semiconductor material (e.g., silicon), impurity regions 220 with the channel formation region 216 provided therebetween, metal compound regions 224 in contact with the impurity regions 220, a gate insulating layer 208 provided over the channel formation region 216, and the gate electrode 210 provided over the gate insulating layer 208. In short, the structure of the transistor 260 is similar to that of the transistor 160 described in Embodiment 1. Note that a transistor whose source electrode and drain electrode are not illustrated in a drawing may be referred to as a transistor for the sake of convenience.

[0133]

Further, an element isolation insulating layer 206 is provided over the substrate 200 so as to surround the transistor 260, and an insulating layer 228 and an insulating layer 230 are provided over the transistor 260. Although not shown, part of the metal compound region 224 of the transistor 260 is connected to a wiring 256 or another wiring via electrodes functioning as a source electrode and a drain electrode. Note that in order to obtain high integration, the transistor 260 preferably does not have a sidewall insulating layer as illustrated in FIGS. 6A and 6B. On the other hand, in the case where characteristics of the transistor 260 are emphasized, a sidewall insulating layer may be provided on a side surface of the gate electrode 210 and the impurity regions 220 may include an impurity region having a different impurity concentration provided in a region overlapping with the sidewall insulating layer.

[0134]

The transistor 262 in FIGS. 6A and 6B includes the source or drain electrode 242a and a source or drain electrode 242b which are provided over the insulating layer 230; an oxide semiconductor layer 244 electrically connected to the source or drain electrode 242a and the source or drain electrode 242b; a gate insulating layer 246 covering the source or drain electrode 242a, the source or drain electrode 242b, and the oxide semiconductor layer 244; a gate electrode 248a provided to overlap with the oxide semiconductor layer 244, over the gate insulating layer 246; an insulating layer 243a provided in a region between the source or drain electrode 242a and the oxide semiconductor layer 244, which overlaps with the gate electrode 248a; and an insulating layer 243b provided in a region between the source or drain electrode 242b and the oxide semiconductor layer 244, which overlaps with the gate electrode 248a. Note that in order to reduce capacitance between the source electrode or the drain electrode and the gate electrode, it is preferable to provide the insulating layer 243a and the insulating layer 243b. However, alternatively, a structure without the insulating layer 243a and the insulating layer 243b may be employed. In short, the structure of the transistor 262 is similar to that of the transistor 162 described in Embodiment 1.

[0135]

In a similar manner to the oxide semiconductor layer 144 described in Embodiment 1, the oxide semiconductor layer 244 is preferably a highly-purified oxide semiconductor layer by sufficiently removing impurities such as hydrogen or sufficiently supplying oxygen. In this manner, by using a highly-purified oxide semiconductor, the transistor 262 with excellent off-current characteristics can be obtained. Embodiment 1 can be referred to for the details of the oxide semiconductor layer 244.

[0136]

Here, the oxide semiconductor layer 244 is provided over the insulating layer 230 including a surface whose RMS roughness is less than or equal to 1 nm, preferably less than or equal to 0.5 nm. In this manner, by providing the oxide semiconductor layer 244 over the surface with favorable planarity, favorable planarity

and uniformity of the oxide semiconductor layer 244 can be obtained.

[0137]

By using the oxide semiconductor layer 244 with favorable planarity and uniformity, carrier scattering can be prevented and an interface level can be reduced at an interface with the oxide semiconductor layer. Accordingly, improvement in mobility, reduction in an S-value and off current, and improvement in transistor characteristics are possible in the transistor 262. In addition, improvement in the planarity of the oxide semiconductor layer 244 leads to reduction in gate leakage current of the transistor 262.

[0138]

Although the oxide semiconductor layer 244 which is processed to have an island shape is used in order to suppress leakage current generated between elements due to miniaturization in the transistor 262 in FIG. 6, a structure including the oxide semiconductor layer 244 which is not processed to have an island shape may be employed. In the case where the oxide semiconductor layer is not processed to have an island shape, contamination of the oxide semiconductor layer 244 due to etching in processing can be prevented.

[0139]

A difference between the semiconductor device in FIGS. 6A and 6B and the semiconductor device in FIG. 1 is whether or not the gate electrode of the transistor in the lower portion is directly connected to the source or drain electrode of the transistor in the upper portion. As in the semiconductor device in FIGS. 6A and 6B, when the gate electrode 210 whose top surface is exposed from the insulating layer 230 and the source or drain electrode 242a are directly connected to each other, higher integration of the semiconductor device can be achieved as compared to the case where an opening and an electrode for connection are separately formed so that the gate electrode 210 is connected to the source or drain electrode 242a because a contact area can be reduced. In addition, a step necessary for forming an opening and an electrode which are separately formed for the contact can be omitted; therefore, a process for manufacturing a semiconductor device can be simplified.

[0140]

In addition, a difference between the semiconductor device in FIG. 1 and the semiconductor device in FIGS. 6A and 6B is whether the capacitor 264 is provided or not. The capacitor 264 in FIGS. 6A and 6B includes the source or drain electrode 242a, the oxide semiconductor layer 244, the gate insulating layer 246, and an electrode 248b. That is, the source or drain electrode 242a functions as one electrode of the capacitor 264, and the electrode 248b functions as the other electrode of the capacitor 264.

[0141]

Note that in the capacitor 264 in FIGS. 6A and 6B, insulating properties between the source or drain electrode 242a and the electrode 248b can be adequately secured by stacking the oxide semiconductor layer 244 and the gate insulating layer 246. Needless to say, the capacitor 264 may employ a structure without the oxide semiconductor layer 244 in order to secure sufficient capacitance. Further, the capacitor 264 having a structure including an insulating layer formed in a similar manner to the insulating layer 243a may be employed. In the case where a capacitor is not needed, it is possible to employ a structure without the capacitor 264.

[0142]

Note that in the transistor 262 and the capacitor 264, edge portions of the source or drain electrode 242a and source or drain electrode 242b are preferably tapered. This is because when the edge portions of the source or drain electrode 242a and the source or drain electrode 242b are tapered, the coverage with the oxide semiconductor layer 244 can be improved and breaking can be prevented. Here, a taper angle is, for example, greater than or equal to 30° and less than or equal to 60°. Note that the taper angle is a tilt angle formed by a side surface and a bottom surface of a layer having a tapered shape (e.g., the source or drain electrode 242a) in the case where the layer is observed from a direction perpendicular to a cross section (a plane perpendicular to the surface of a substrate).

[0143]

In this embodiment, the transistor 262 and the capacitor 264 are provided so

as to overlap with the transistor 260. By employing such a planar layout, high integration is possible. For example, given that the minimum processing dimension is F, the area occupied by a memory cell can be $15F^2$ to $25F^2$ by devising a connection between a wiring and an electrode.

[0144]

Further, an insulating layer 250 is provided over the transistor 262 and the capacitor 264, and an insulating layer 252 is provided over the insulating layer 250. An electrode 254 is provided in an opening formed in the gate insulating layer 246, the insulating layer 250, the insulating layer 252, and the like, and the wiring 256 connected to the electrode 254 is provided over the insulating layer 252. Here, a difference between the semiconductor device in FIG. 1 and the semiconductor device in FIGS. 6A and 6B is whether the electrode 254 is provided or not. Note that the source or drain electrode 242b and the wiring 256 are connected to each other with the electrode 254 in FIGS. 6A and 6B; however, the disclosed invention is not limited thereto. For example, the wiring 256 may be directly in contact with the source or drain electrode 242b.

[0145]

In addition, an electrode (not shown) connected to the metal compound region 224 may be connected to the source or drain electrode 242b. In this case, the electrode connected to the metal compound region 224 and the electrode 254 connecting the source or drain electrode 242b and the wiring 256 are preferably provided so as to be overlap with each other. By employing such a layout, high integration of the semiconductor device can be obtained.

[0146]

Note that a top-gate transistor in which an oxide semiconductor layer is provided over source and drain electrodes is used as the transistor 262 in the semiconductor device of FIGS. 6A and 6B; however, the structure of the semiconductor device according to this embodiment is not limited thereto. For example, the semiconductor device may have any of structures illustrated in FIGS. 7A and 7B, FIGS. 8A and 8B, and FIGS. 9A and 9B.

[0147]

FIGS. 7A and 7B illustrate an example of the structure of the semiconductor device. FIGS. 7A and 7B illustrate a cross-sectional view and a plan view of the semiconductor device, respectively. Here, FIG. 7A corresponds to a cross section along line A1-A2 and line B1-B2 in FIG. 7B.

[0148]

The semiconductor device in FIGS. 7A and 7B is different from the semiconductor device in FIGS. 6A and 6B in that the source or drain electrode 242a and the source or drain electrode 242b are provided over the oxide semiconductor layer 244. Accordingly, the structures of the transistor 272 and the capacitor 274 in the semiconductor device in FIGS. 7A and 7B are different from those of the transistor 262 and the capacitor 264 in the semiconductor device in FIG. 6A and 6B.

[0149]

The transistor 272 in FIGS. 7A and 7B includes the oxide semiconductor layer 244 provided over the insulating layer 230, the source or drain electrode 242a and the source or drain electrode 242b which are provided over and electrically connected to the oxide semiconductor layer 244; the gate insulating layer 246 covering the source or drain electrode 242a, the source or drain electrode 242b, and the oxide semiconductor layer 244; the gate electrode 248a provided to overlap with the oxide semiconductor layer 244, over the gate insulating layer 246; the insulating layer 243a provided in a region between the source or drain electrode 242a and the gate insulating layer 246, which overlaps with the gate electrode 248a; and the insulating layer 243b provided in a region between the source or drain electrode 242b and the gate insulating layer 246, which overlaps with the gate electrode 248a.

[0150]

The capacitor 274 in FIGS. 7A and 7B includes the source or drain electrode 242a, the gate insulating layer 246, and the electrode 248b. That is, the source or drain electrode 242a functions as one electrode of the capacitor 274, and the electrode 248b functions as the other electrode of the capacitor 274.

[0151]

The structures other than those described above in the semiconductor device in FIGS. 7A and 7B are the same as those in the semiconductor device in FIG. 6A and 6B, and therefore, the semiconductor device in FIGS. 6A and 6B can be referred to.

[0152]

FIGS. 8A and 8B illustrate an example of the structure of the semiconductor device. FIGS. 8A and 8B illustrate a cross-sectional view and a plan view of the semiconductor device, respectively. Here, FIG. 8A corresponds to a cross section along line A1-A2 and line B1-B2 in FIG. 8B.

[0153]

The semiconductor device in FIGS. 8A and 8B is different from the semiconductor device in FIGS. 6A and 6B in that the gate insulating layer 246, the oxide semiconductor layer 244, the source or drain electrode 242a, and the source or drain electrode 242b are provided over the gate electrode 248a. In other words, a transistor 282 in the semiconductor device in FIGS. 8A and 8B is a bottom-gate transistor. Accordingly, the structures of the transistor 282 and a capacitor 284 in the semiconductor device in FIGS. 8A and 8B are different from those of the transistor 262 and the capacitor 264 in the semiconductor device in FIGS. 6A and 6B.

[0154]

The transistor 282 in FIGS. 8A and 8B includes the gate electrode 248a provided over the insulating layer 230, the gate insulating layer 246 covering the gate electrode 248a, the source or drain electrode 242a and the source or drain electrode 242b which are provided over the gate insulating layer 246, and the oxide semiconductor layer 244 which is provided over and electrically connected to the source or drain electrode 242a and the source or drain electrode 242b. Note that the transistor 282 does not include the insulating layer 243a and the insulating layer 243b.

[0155]

The capacitor 284 in FIGS. 8A and 8B includes the source or drain electrode 242a, the gate insulating layer 246, and the electrode 248b. That is, the source or drain electrode 242a functions as one electrode of the capacitor 284, and the electrode 248b functions as the other electrode of the capacitor 284.

[0156]

The structures other than those described above in the semiconductor device in FIGS. 8A and 8B are the same as those in the semiconductor device in FIG. 6A and 6B, and therefore, the semiconductor device in FIGS. 6A and 6B can be referred to.

[0157]

FIGS. 9A and 9B illustrate an example of the structure of the semiconductor device. FIGS. 9A and 9B illustrate a cross-sectional view and a plan view of the semiconductor device, respectively. Here, FIG. 9A corresponds to a cross section along line A1-A2 and line B1-B2 in FIG. 9B.

[0158]

The semiconductor device in FIGS. 9A and 9B is different from the semiconductor device in FIGS. 6A and 6B in that the gate insulating layer 246, the oxide semiconductor layer 244, the source or drain electrode 242a, and the source or drain electrode 242b are provided over the gate electrode 248a. In other words, a transistor 292 in the semiconductor device in FIGS. 9A and 9B is a bottom-gate transistor. Accordingly, the structures of the transistor 292 and a capacitor 294 in the semiconductor device in FIGS. 9A and 9B are different from those of the transistor 262 and the capacitor 264 in the semiconductor device in FIGS. 6A and 6B. The semiconductor device in FIGS. 9A and 9B is different from the semiconductor device in FIGS. 8A and 8B in that the source or drain electrode 242a and the source or drain electrode 242b are provided over the oxide semiconductor layer 244.

[0159]

The transistor 292 in FIGS. 9A and 9B includes the gate electrode 248a provided over the insulating layer 230, the gate insulating layer 246 covering the gate electrode 248a, the oxide semiconductor layer 244 provided over the gate insulating layer 246, the source or drain electrode 242a and the source or drain electrode 242b which are provided over and electrically connected to the oxide semiconductor layer 244. Note that the transistor 292 does not include the insulating layer 243a and the insulating layer 243b.

[0160]

The capacitor 294 in FIGS. 9A and 9B includes the source or drain electrode 242a, the gate insulating layer 246, and the electrode 248b. That is, the source or drain electrode 242a functions as one electrode of the capacitor 294, and the electrode 248b functions as the other electrode of the capacitor 294.

[0161]

The structures other than those described above in the semiconductor device in FIGS. 9A and 9B are the same as those in the semiconductor device in FIG. 6A and 6B, and therefore, the semiconductor device in FIGS. 6A and 6B can be referred to.

[0162]

<Example of method for manufacturing semiconductor device>

Next, an example of a method for manufacturing the semiconductor device will be described. First, a method for manufacturing the transistor 260 in the lower portion will be described below with reference to FIGS. 10A to 10D and FIGS. 11A to 11C, and then a method for manufacturing the transistor 262 and the capacitor 264 in the upper portion will be described with reference to FIGS. 12A to 12D and FIGS. 13A to 13C.

[0163]

<Method for manufacturing transistor in lower portion>

First, the substrate 200 including a semiconductor material is prepared, and a protective layer 202 serving as a mask for forming an element isolation insulating layer is formed over the substrate 200 (see FIG. 10A).

[0164]

Here, the same material as that of the substrate 100 in Embodiment 1 can be used for the substrate 200. In addition, the same material as that of the protective layer 102 in Embodiment 1 can be used for the protective layer 202. Embodiment 1 can be referred to for the details thereof.

[0165]

Note that it is preferable that a single crystal semiconductor substrate of silicon or the like be used as the substrate 200 including a semiconductor material because high-speed reading operation in the semiconductor device is possible.

[0166]

Next, part of the substrate 200 in a region that is not covered with the protective layer 202 (i.e., an exposed region) is removed by etching with the use of the protective layer 202 as a mask. Thus, a semiconductor region 204 which is apart from another semiconductor region is formed (see FIG. 10B). As the etching, dry etching is preferably performed, but wet etching can be performed. An etching gas and an etchant can be selected as appropriate depending on a material of layers to be etched.

[0167]

Then, an insulating layer is formed so as to cover the semiconductor region 204, and the insulating layer in a region overlapping with the semiconductor region 204 is selectively removed, so that the element isolation insulating layer 206 is formed (see FIG. 10C). The element isolation insulating layer 206 can be formed using a material and a method similar to those of the element isolation insulating layer 106 in Embodiment 1. Therefore, Embodiment 1 can be referred to for the details thereof.

[0168]

Next, an insulating layer is formed over a surface of the semiconductor region 204, and a layer containing a conductive material is formed over the insulating layer. After that, the insulating layer and the layer containing a conductive material are selectively etched, so that the gate insulating layer 208 and the gate electrode 210 are formed (see FIG. 10C). The gate insulating layer 208 and the gate electrode 210 can be formed using materials and methods similar to those of the gate insulating layer 108 and the gate electrode 110 in Embodiment 1. Therefore, Embodiment 1 can be referred to for the details thereof.

[0169]

Next, phosphorus (P), arsenic (As), or the like is added to the semiconductor region 204, so that the channel formation region 216 and the impurity regions 220 are formed (see FIG. 10D). Note that phosphorus or arsenic is added here in order to form an n-channel transistor; an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. Here, the concentration

of the impurity added can be set as appropriate; the concentration is preferably increased when the size of a semiconductor element is extremely decreased.

[0170]

Note that a sidewall insulating layer may be formed in the periphery of the gate electrode 210 so that an impurity region to which an impurity element is added at a different concentration may be formed.

[0171]

Next, a metal layer 222 is formed so as to cover the gate electrode 210, the impurity regions 220, and the like. Then, heat treatment is performed so that the metal layer 222 and a semiconductor material react to each other, whereby the metal compound regions 224 in contact with the impurity regions 220 are formed (see FIG. 11A). The metal layer 222 and the metal compound regions 224 can be formed using materials and methods similar to those of the metal layer 122 and the metal compound regions 124 in Embodiment 1. Therefore, Embodiment 1 can be referred to for the details thereof. The formation of the metal compound regions can properly reduce the electric resistance and improve element characteristics.

[0172]

Then, the insulating layer 228 and the insulating layer 230 are formed so as to cover the components formed in the above steps (see FIG. 11B). The insulating layer 228 and the insulating layer 230 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, or aluminum oxide. In particular, the insulating layer 228 and the insulating layer 230 are preferably formed using a low dielectric constant (low-k) material, whereby capacitance caused by an overlap of electrodes or wirings can be sufficiently reduced. Note that a porous insulating layer including these materials may be used for the insulating layer 228 and the insulating layer 230. Since the porous insulating layer has low dielectric constant as compared to a dense insulating layer, capacitance due to electrodes or wirings can be further reduced.

[0173]

In addition, a layer including an inorganic material containing a large amount

of nitride, such as silicon nitride oxide or silicon nitride, may be included in the insulating layer 228 or the insulating layer 230. Thus, the impurity such as water or hydrogen contained in the material included in the transistor 260 in the lower portion can be prevented from entering the oxide semiconductor layer 244 of the transistor 262 in the upper portion that is formed later. Note that in this case, it is difficult to remove the layer including an inorganic insulating material containing a large amount of nitrogen only by CMP treatment performed in a later step; therefore, CMP treatment and etching treatment are preferably performed in combination.

[0174]

For example, silicon oxynitride and silicon oxide are used for forming the insulating layer 228 and the insulating layer 230, respectively. In this manner, only an inorganic insulating material containing a large amount of oxygen, such as silicon oxynitride or silicon oxide, is used for the insulating layer 228 and the insulating layer 230, whereby CMP treatment can be easily performed on the insulating layer 228 and the insulating layer 230 in a later step.

[0175]

Note that a stacked structure of the insulating layer 228 and the insulating layer 230 is employed here; however, one embodiment of the disclosed invention is not limited to this. A single-layer structure or a stacked structure including three or more layers can also be used. For example, the following structure may be employed: silicon oxynitride and silicon oxide are used for the insulating layer 228 and the insulating layer 230, respectively, and a silicon nitride oxide film is formed between the insulating layer 228 and the insulating layer 230.

[0176]

Through the above steps, the transistor 260 using the substrate 200 including a semiconductor material is formed (see FIG. 11B). Such a transistor 260 is capable of high-speed operation. Therefore, when the transistor 260 is used as a reading transistor, data can be read out at high speed.

[0177]

After that, as treatment before formation of the transistor 262, CMP treatment

is performed on the insulating layer 228 and the insulating layer 230, so that surfaces of the insulating layer 228 and the insulating layer 230 are planarized and a top surface of the gate electrode 210 is exposed (see FIG. 11C).

[0178]

The CMP treatment may be performed once or plural times. When the CMP treatment is performed plural times, first polishing is preferably performed with a high polishing rate followed by final polishing with a low polishing rate. By combining polishing with different polishing rates, planarity of the surfaces of the insulating layer 228 and the insulating layer 230 can be further improved.

[0179]

As the treatment for planarizing the insulating layer 228 and the insulating layer 230, etching treatment or the like can be performed instead of CMP treatment, and planarization is preferably performed so that each of the surfaces of the insulating layer 228 and the insulating layer 230 has an RMS roughness of less than or equal to 1 nm, or preferably less than or equal to 0.5 nm in order to improve the planarity and the uniformity of the oxide semiconductor layer 244 and improve characteristics of the transistor 262.

[0180]

In addition, when the stacked layer structure of the insulating layer 228 and the insulating layer 230 includes an inorganic insulating material containing a large amount of nitrogen, such as silicon nitride or silicon nitride oxide, since it is difficult to remove the inorganic insulating material containing a large amount of nitrogen only by the CMP treatment, CMP treatment and etching treatment are preferably performed in combination. As the etching treatment for the inorganic insulating material containing a large amount of nitrogen, either dry etching or wet etching may be used. However, in view of miniaturization of elements, dry etching is preferably used. In addition, it is preferable that etching conditions (an etching gas, an etchant, an etching time, a temperature, or the like) be set appropriately so that etching rates of the respective insulating layers are equal to each other and high etching selectivity with the gate electrode 210 can be obtained. In addition, as an etching gas for dry etching,

for example, a gas containing fluorine (trifluoromethane (CHF_3)), a gas to which a rare gas such as helium (He) or argon (Ar) is added, or the like can be used.

[0181]

In addition, when the top surface of the gate electrode 210 is exposed from the insulating layer 230, the top surface of the gate electrode 210 and a surface of the insulating layer 230 are included in the same surface.

[0182]

Note that before or after the above steps, a step for forming an additional electrode, wiring, semiconductor layer, or insulating layer may be performed. For example, an electrode which is connected to part of the metal compound region 224 and functions as a source or drain electrode of the transistor 260 may be formed. In addition, a multilayer wiring structure in which an insulating layer and a conductive layer are stacked is employed as a wiring structure, so that a highly-integrated semiconductor device can be provided.

[0183]

<Method for manufacturing transistor in upper portion>

Then, a conductive layer is formed over the gate electrode 210, the insulating layer 228, the insulating layer 230, and the like, and the conductive layer is selectively etched, so that the source or drain electrode 242a and the source or drain electrode 242b are formed (see FIG. 12A). The source or drain electrode 242a and the source or drain electrode 242b can be formed using a material and a method similar to those of the source or drain electrode 142a and the source or drain electrode 142b in Embodiment 1. Therefore, Embodiment 1 can be referred to for the details thereof.

[0184]

Here, the edge portions of the source or drain electrode 242a and the source or drain electrode 242b are etched so as to be tapered; accordingly, the coverage of the gate insulating layer 246 to be formed later is improved and breaking can be prevented.

[0185]

The channel length (L) of the transistor in the upper portion is determined by

a distance between a lower edge portion of the source or drain electrode 242a and a lower edge portion of the source or drain electrode 242b. Note that for light exposure for forming a mask used in the case where a transistor with a channel length (L) of less than 25 nm is formed, it is preferable to use extreme ultraviolet rays whose wavelength is as short as several nanometers to several tens of nanometers. In the light exposure by extreme ultraviolet light, the resolution is high and the focus depth is large. For these reasons, the channel length (L) of the transistor to be formed later can be in the range of greater than or equal to 10 nm and less than or equal to 1000 nm (1 μm), and the circuit can operate at higher speed. Moreover, miniaturization can lead to low power consumption of a semiconductor device.

[0186]

Here, the source or drain electrode 242a of the transistor 262 and the gate electrode 210 of the transistor 260 are directly connected to each other (see FIG. 12A). When the gate electrode 210 and the source or drain electrode 242a are directly connected to each other, higher integration of the semiconductor device can be achieved as compared to the case where an opening and an electrode for connection are separately formed so that the gate electrode 210 is connected to the source or drain electrode 242a because a contact area can be reduced. Accordingly, a storage capacity per unit area of the semiconductor device which can be used as a memory device can be increased. In addition, a step necessary for forming an opening and an electrode which are separately formed for the contact can be omitted; therefore, a process for manufacturing a semiconductor device can be simplified.

[0187]

Then, the insulating layer 243a and the insulating layer 243b are formed over the source or drain electrode 242a and the source or drain electrode 242b, respectively (see FIG. 12B). The insulating layer 243a and the insulating layer 243b can be formed using a material and a method similar to those of the insulating layer 143a and the insulating layer 143b in Embodiment 1. Accordingly, Embodiment 1 can be referred to for the details thereof. By providing the insulating layer 243a and the insulating layer 243b, capacitance between the gate electrode and the source or drain

electrode can be reduced.

[0188]

Note that in view of reduction in the capacitance between the gate electrode and the source or drain electrode, the insulating layer 243a and the insulating layer 243b are preferably formed; however, a structure without the insulating layer 243a and the insulating layer 243b may be employed.

[0189]

Next, an oxide semiconductor layer is formed so as to cover the source or drain electrode 242a and the source or drain electrode 242b, and then the oxide semiconductor layer is selectively etched, so that the oxide semiconductor layer 244 is formed (see FIG. 12C). The oxide semiconductor layer 244 can be formed using a material and a method similar to those of the oxide semiconductor layer 144 described in Embodiment 1. Embodiment 1 can be referred to for the details.

[0190]

Here, the oxide semiconductor layer 244 is provided over the insulating layer 230 including a surface whose RMS roughness is less than or equal to 1 nm, preferably less than or equal to 0.5 nm. In this manner, by providing the oxide semiconductor layer 244 over the surface with favorable planarity, favorable planarity and uniformity of the oxide semiconductor layer 244 can be obtained. In addition, by using the oxide semiconductor layer 244 with favorable planarity and uniformity, transistor characteristics of the transistor 262 can be improved.

[0191]

Note that, as described in Embodiment 1, before the oxide semiconductor layer is formed by a sputtering method, reverse sputtering in which plasma is generated with an argon gas introduced is preferably performed, so that dust attached to a surface on which the oxide semiconductor layer is formed (e.g., the surface of the insulating layer 230) is removed.

[0192]

After that, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer. The heat treatment (the first heat treatment) can be

performed in a similar manner to that in Embodiment 1.

[0193]

Impurities are reduced by the first heat treatment so that the i-type (intrinsic) or substantially i-type oxide semiconductor layer is obtained. Accordingly, a transistor having significantly excellent characteristics can be realized.

[0194]

Note that the oxide semiconductor layer may be etched either before or after the heat treatment. In view of miniaturization of elements, dry etching is preferably used; however, wet etching may be used. An etching gas and an etchant can be selected as appropriate depending on a material of layers to be etched. Note that in the case where leakage current in an element does not cause a problem, the oxide semiconductor layer may be used without being processed to have an island shape.

[0195]

Next, the gate insulating layer 246 in contact with the oxide semiconductor layer 244 is formed, and then the gate electrode 248a and the electrode 248b are formed in regions overlapping with the oxide semiconductor layer 244 and the source or drain electrode 242a, respectively, over the gate insulating layer 246 (see FIG. 12D). The gate insulating layer 246 can be formed using a material and a method similar to those of the gate insulating layer 146 in Embodiment 1.

[0196]

After the gate insulating layer 246 is formed, second heat treatment is desirably performed in an inert gas atmosphere or an oxygen atmosphere. The second heat treatment can be performed in a similar manner to that in Embodiment 1. The second heat treatment can reduce variation in electrical characteristics of the transistor. Further, in the case where the gate insulating layer 246 contains oxygen, oxygen is supplied to the oxide semiconductor layer 244 to cover oxygen deficiency in the oxide semiconductor layer 244, so that an i-type (intrinsic semiconductor) or substantially i-type oxide semiconductor layer can be formed.

[0197]

Note that in this embodiment, the second heat treatment is performed after the

gate insulating layer 246 is formed; the timing of the second heat treatment is not limited thereto. For example, the second heat treatment may be performed after the gate electrode is formed. Alternatively, the second heat treatment may be performed following the first heat treatment, the first heat treatment may double as the second heat treatment, or the second heat treatment may double as the first heat treatment.

[0198]

As described above, at least one of the first heat treatment and the second heat treatment is performed, so that the oxide semiconductor layer 244 can be highly purified so as to contain impurities which are not main components as little as possible.

[0199]

The gate electrode 248a can be formed using a material and a method similar to those of the gate electrode 148a in Embodiment 1. In addition, the electrode 248b can be formed by selectively etching the conductive layer, at the same time as the formation of the gate electrode 248a. Embodiment 1 can be referred to for the details thereof.

[0200]

Next, the insulating layer 250 and the insulating layer 252 are formed over the gate insulating layer 246, the gate electrode 248a, and the electrode 248b (see FIG. 13A). The insulating layer 250 and the insulating layer 252 can be formed using materials and methods similar to those of the insulating layer 150 and the insulating layer 152 in Embodiment 1. Accordingly, Embodiment 1 can be referred to for the details thereof.

[0201]

Next, an opening which reaches the source or drain electrode 242b through the gate insulating layer 246, the insulating layer 250 and the insulating layer 252 is formed (see FIG. 13B). The opening is formed by selective etching with the use of a mask or the like.

[0202]

Then, the electrode 254 is formed in the opening, and the wiring 256 in

contact with the electrode 254 is formed over the insulating layer 252 (see FIG. 13C).

[0203]

For example, the electrode 254 can be formed in the following manner: a conductive layer is formed in a region including the opening by a PVD method, a CVD method, or the like, and then, the conductive layer is partly removed by etching treatment, CMP, or the like.

[0204]

Specifically, it is possible to employ a method, for example, in which a thin titanium film is formed in a region including the opening by a PVD method and a thin titanium nitride film is formed by a CVD method, and then, a tungsten film is formed so as to be embedded in the opening. Here, the titanium film formed by a PVD method has a function of reducing an oxide film (e.g., a natural oxide film) formed on a surface over which the titanium film is formed, to decrease the contact resistance with the lower electrode (here, the source or drain electrode 242b) or the like. The titanium nitride film formed after the formation of the titanium film has a barrier function of preventing diffusion of the conductive material. A copper film may be formed by a plating method after the formation of the barrier film of titanium, titanium nitride, or the like.

[0205]

Note that in the case where the electrode 254 is formed by removing part of the conductive layer, it is preferable that a surface thereof be processed to be flat. For example, when a thin titanium film or a thin titanium nitride film is formed in a region including the opening and then a tungsten film is formed so as to be embedded in the opening, excess tungsten, titanium, titanium nitride, or the like can be removed and the planarity of the surface can be improved by subsequent CMP treatment. The surface including the surface of the electrode 254 is planarized in such a manner, whereby an electrode, a wiring, an insulating layer, a semiconductor layer, and the like can be favorably formed in later steps.

[0206]

The wiring 256 can be formed using a material and a method similar to those

of the wiring 156 in Embodiment 1. Accordingly, Embodiment 1 can be referred to for the details thereof.

[0207]

Through the above steps, the transistor 262 including the highly-purified oxide semiconductor layer 244 and the capacitor 264 are completed (see FIG. 13C).

[0208]

With the use of the highly-purified intrinsic oxide semiconductor layer 244, the off current of the transistor can be sufficiently reduced. Then, by using such a transistor, a semiconductor device in which stored data can be held for an extremely long time can be obtained.

[0209]

In this manner, the semiconductor device in which the transistor including a semiconductor material other than an oxide semiconductor is included in the lower portion and the transistor including an oxide semiconductor is included in the upper portion, and which can be used as a memory device can be provided.

[0210]

With a combination of the transistor including an oxide semiconductor and the transistor including a semiconductor material other than an oxide semiconductor, the semiconductor device capable of holding data for a long time and reading data at high speed, which can be used as a memory device, can be obtained.

[0211]

In addition, by providing the oxide semiconductor layer over a surface with favorable planarity, the semiconductor device in which the transistor whose transistor characteristics are improved is stacked over the transistor including a semiconductor material other than an oxide semiconductor can be provided.

[0212]

When the gate electrode 210 and the source or drain electrode 242a are directly connected to each other, higher integration of the semiconductor device can be achieved because a contact area can be reduced. Accordingly, a storage capacity per unit area of the semiconductor device which can be used as a memory device can be

increased.

[0213]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0214]

[Embodiment 3]

In this embodiment, a structure and a manufacturing method of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 14A and 14B, FIGS. 15A to 15H, and FIGS. 16A to 16E. In particular, an example of a structure of a semiconductor device which can be used as a memory device will be described in this embodiment.

[0215]

<Cross-sectional structure and planar structure of semiconductor device>

FIGS. 14A and 14B illustrate an example of a structure of the semiconductor device according to this embodiment. FIGS. 14A and 14B illustrate a cross-sectional view and a plan view of the semiconductor device, respectively. Here, FIG. 14A corresponds to a cross section along line C1-C2 and line D1-D2 in FIG. 14B. In the semiconductor device illustrated in FIGS. 14A and 14B, a transistor 560 including a first semiconductor material is provided in a lower portion, a transistor 562 including a second semiconductor material is provided in an upper portion, and a gate electrode 524a of the transistor 560 and a source or drain electrode 542a of the transistor 562 are directly connected to each other. Here, the first semiconductor material is preferably different from the second semiconductor material. For example, a semiconductor material other than an oxide semiconductor (e.g., silicon), can be used as the first semiconductor material and an oxide semiconductor can be used as the second semiconductor material. The transistor 560 including a semiconductor material other than an oxide semiconductor can operate at high speed easily. On the other hand, the transistor 562 including an oxide semiconductor has off current which is sufficiently reduced, so that the transistor 562 can hold charge for a long time.

[0216]

Therefore, when the transistor 562 is in an off state, the potential of the gate electrode 524a of the transistor 560 can be held for an extremely long time. When a capacitor 564 is provided, electric charge supplied to the gate electrode 524a of the transistor 560 can be held easily and reading of held data can be performed easily. In addition, since the transistor 560 including such a semiconductor material is capable of operating at sufficiently high speed, reading speed of data can be improved.

[0217]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. The technical nature of the disclosed invention is that a transistor including an oxide semiconductor with sufficiently reduced off current and a transistor including a semiconductor material other than an oxide semiconductor which is capable of sufficiently high-speed operation are provided in combination; thus, it is not necessary to limit specific conditions, such as a material used for the semiconductor device or a structure of the semiconductor device, to the structure described here.

[0218]

The transistor 560 illustrated in FIGS. 14A and 14B includes a channel formation region 526 provided in a semiconductor layer over a base substrate 500, impurity regions 528 with the channel formation region 526 provided therebetween, a gate insulating layer 522a provided over the channel formation region 526, and the gate electrode 524a provided over the gate insulating layer 522a. That is, a difference between the transistor 560 in FIGS. 14A and 14B and the transistor 260 in FIGS. 6A and 6B is whether or not the channel formation region of the transistor is formed in the semiconductor layer over the base substrate. It can also be said that the difference lies in the use of a semiconductor substrate or an SOI substrate. Note that a transistor whose source electrode and drain electrode are not illustrated in a drawing may be referred to as a transistor for the sake of convenience.

[0219]

In addition, an insulating layer 532 and an insulating layer 534 are provided

so as to cover the transistor 560. Although not shown, part of the impurity region 528 of the transistor 560 is connected to a wiring 556 or another wiring via electrodes functioning as a source electrode and a drain electrode. Note that in order to obtain high integration, the transistor 560 preferably does not have a sidewall insulating layer as illustrated in FIGS. 14A and 14B. On the other hand, in the case where characteristics of the transistor 560 are emphasized, a sidewall insulating layer may be provided on a side surface of the gate electrode 524a and the impurity regions 528 may include an impurity region having a different impurity concentration provided in a region overlapping with the sidewall insulating layer.

[0220]

The transistor 562 in FIGS. 14A and 14B has the same structure as the transistor 262 in FIGS. 6A and 6B. In other words, the transistor 562 in FIG. 14A and 14B includes the source or drain electrode 542a and a source or drain electrode 542b which are provided over the insulating layer 534; an oxide semiconductor layer 544 electrically connected to the source or drain electrode 542a and the source or drain electrode 542b; a gate insulating layer 546 covering the source or drain electrode 542a, the source or drain electrode 542b, and the oxide semiconductor layer 544; a gate electrode 548a provided to overlap with the oxide semiconductor layer 544, over the gate insulating layer 546; an insulating layer 543a provided in a region between the source or drain electrode 542a and the oxide semiconductor layer 544, which overlaps with the gate electrode 548a; and an insulating layer 543b provided in a region between the source or drain electrode 542b and the oxide semiconductor layer 544, which overlaps with the gate electrode 548a. Note that in order to reduce capacitance between the source electrode or the drain electrode and the gate electrode, it is preferable to provide the insulating layer 543a and the insulating layer 543b. However, alternatively, a structure without the insulating layer 543a and the insulating layer 543b may be employed. The above embodiments can also be referred to for the other details.

[0221]

Here, the oxide semiconductor layer 544 is provided over the insulating layer

534 including a surface whose RMS roughness is less than or equal to 1 nm, preferably less than or equal to 0.5 nm. In this manner, by providing the oxide semiconductor layer 544 over the surface with favorable planarity, favorable planarity and uniformity of the oxide semiconductor layer 544 can be obtained.

[0222]

By using the oxide semiconductor layer 544 with favorable planarity and uniformity, carrier scattering can be prevented and an interface level can be reduced at an interface with the oxide semiconductor layer. Accordingly, improvement in mobility, reduction in an S-value and off current, and improvement in transistor characteristics are possible in the transistor 562. In addition, improvement in the planarity of the oxide semiconductor layer 544 leads to reduction in gate leakage current of the transistor 562.

[0223]

Further, the capacitor 564 in FIGS. 14A and 14B has the same structure as the capacitor 264 in FIGS. 6A and 6B. In other words, the capacitor 564 in FIGS. 14A and 14B includes the source or drain electrode 542a, the oxide semiconductor layer 544, the gate insulating layer 546, and an electrode 548b. That is, the source or drain electrode 542a functions as one electrode of the capacitor 564, and the electrode 548b functions as the other electrode of the capacitor 564. The above embodiments can also be referred to for the other details.

[0224]

The following structures in FIGS. 14A and 14B are also similar to those in FIGS. 6A and 6B: an insulating layer 550 is provided over the transistor 562 and the capacitor 564; an insulating layer 552 is provided over the insulating layer 550; an electrode 554 is provided in an opening formed in the gate insulating layer 546, the insulating layer 550, the insulating layer 552, and the like; and the wiring 556 connected to the electrode 554 is provided over the insulating layer 552.

[0225]

Note that the structure of the semiconductor device according to this embodiment is not limited to that of the semiconductor in FIGS. 14A and 14B. For

example, instead of the transistor 562 and the capacitor 564, the transistor 272 and the capacitor 274 illustrated in FIGS. 7A and 7B may be used, the transistor 282 and the capacitor 284 illustrated in FIGS. 8A and 8B may be used, or the transistor 292 and the capacitor 294 illustrated in FIGS. 9A and 9B may be used.

[0226]

<Method for manufacturing SOI substrate>

Next, an example of a method for manufacturing an SOI substrate used for manufacturing the semiconductor device will be described with reference to FIGS. 15A to 15H.

[0227]

First, the base substrate 500 is prepared (see FIG. 15A). As the base substrate 500, a substrate formed using an insulator can be used. Specific examples thereof are as follows: a variety of glass substrates used in the electronics industry, such as substrates of aluminosilicate glass, aluminoborosilicate glass, and barium borosilicate glass; a quartz substrate; a ceramic substrate; and a sapphire substrate. Further, a ceramic substrate which contains silicon nitride and aluminum nitride as its main components and whose coefficient of thermal expansion is close to that of silicon may be used.

[0228]

Alternatively, a semiconductor substrate such as a single crystal silicon substrate or a single crystal germanium substrate may be used as the base substrate 500. In the case of using such a semiconductor substrate as the base substrate 500, the temperature limitation for heat treatment can be raised compared with the case of using a glass substrate or the like; thus, a high-quality SOI substrate is easily obtained. Here, as a semiconductor substrate, a solar grade silicon (SOG-Si) substrate or the like may be used. Alternatively, a polycrystalline semiconductor substrate may be used. In the case of using a SOG-Si substrate, a polycrystalline semiconductor substrate, or the like, manufacturing cost can be reduced as compared to the case of using a single crystal silicon substrate or the like.

[0229]

Note that in this embodiment, a description is given of the case where a glass substrate is used as the base substrate 500. Cost reduction can be achieved when a glass substrate which can have a larger size and is inexpensive is used as the base substrate 500.

[0230]

A surface of the base substrate 500 is preferably cleaned in advance. Specifically, the base substrate 500 is subjected to ultrasonic cleaning with a hydrochloric acid/hydrogen peroxide mixture (HPM), a sulfuric acid/hydrogen peroxide mixture (SPM), an ammonium hydrogen peroxide mixture (APM), diluted hydrofluoric acid (DHF), FPM (a mixed solution of hydrofluoric acid, hydrogen peroxide water, and pure water), or the like. Through such cleaning treatment, the surface planarity of the base substrate 500 can be improved and abrasive particles left on the surface of the base substrate 500 can be removed.

[0231]

Then, a nitrogen-containing layer 502 (e.g., a layer including an insulating film containing nitrogen, such as a silicon nitride (SiN_x) film or a silicon nitride oxide (SiN_xO_y ($x > y$)) film) is formed over the surface of the base substrate 500 (see FIG. 15B). The nitrogen-containing layer 502 can be formed by a CVD method, a sputtering method, or the like.

[0232]

The nitrogen-containing layer 502 formed in this embodiment corresponds to a layer for bonding a single crystal semiconductor layer (a bonding layer). The nitrogen-containing layer 502 also functions as a barrier layer for preventing impurity contained in the base substrate, such as sodium (Na), from diffusing into the single crystal semiconductor layer.

[0233]

As described above, since the nitrogen-containing layer 502 is used as the bonding layer in this embodiment, it is preferable that the nitrogen-containing layer 502 be formed to have a certain level of surface planarity. Specifically, the nitrogen-containing layer 502 is formed such that it has an average surface roughness

(Ra, which is also referred to as arithmetic mean deviation) of 0.5 nm or less and an RMS roughness of 0.60 nm or less, preferably Ra of 0.35 nm or less and an RMS of 0.45 nm or less. Note that for the above average surface roughness or the root-mean-square surface roughness, for example, a value obtained by the measurement performed on a region of 10 μm × 10 μm can be used. The thickness is in the range of from 10 nm to 200 nm, preferably, from 50 nm to 100 nm. With the surface planarity improved as described above, the bonding defect of the single crystal semiconductor layer can be prevented.

[0234]

Next, a bonding substrate is prepared. Here, a single crystal semiconductor substrate 510 is used as the bonding substrate (see FIG. 15C). Note that although a substrate whose crystallinity is single crystal is used as the bonding substrate here, the crystallinity of the bonding substrate is not necessarily limited to single crystal.

[0235]

For example, as the single crystal semiconductor substrate 510, a single crystal semiconductor substrate formed using an element of Group 14, such as a single crystal silicon substrate, a single crystal germanium substrate, or a single crystal silicon germanium substrate, can be used. Further, a compound semiconductor substrate using gallium arsenide, indium phosphide, or the like can be used. Typical examples of commercially available silicon substrates are circular silicon substrates which are 5 inches (125 mm) in diameter, 6 inches (150 mm) in diameter, 8 inches (200 mm) in diameter, 12 inches (300 mm) in diameter, and 16 inches (400 mm) in diameter. Note that the shape of the single crystal semiconductor substrate 510 is not limited to circular, and the single crystal semiconductor substrate 510 may be a substrate which has been processed into, for example, a rectangular shape or the like. Further, the single crystal semiconductor substrate 510 can be formed by a Czochralski (CZ) method or a floating zone (FZ) method.

[0236]

An oxide film 512 is formed over a surface of the single crystal semiconductor substrate 510 (see FIG. 15D). In view of removal of contamination, it

is preferable that the surface of the single crystal semiconductor substrate 510 be cleaned with a hydrochloric acid/hydrogen peroxide mixture (HPM), a sulfuric acid/hydrogen peroxide mixture (SPM), an ammonium hydrogen peroxide mixture (APM), diluted hydrofluoric acid (DHF), FPM (a mixed solution of hydrofluoric acid, hydrogen peroxide water, and pure water), or the like before the formation of the oxide film 512. Alternatively, diluted hydrofluoric acid and ozone water may be discharged alternately to clean the surface of the single crystal semiconductor substrate 510.

[0237]

The oxide film 512 can be formed with, for example, a single layer or a stacked layer of a silicon oxide film, a silicon oxynitride film, and the like. As a method for forming the oxide film 512, a thermal oxidation method, a CVD method, a sputtering method, or the like can be used. When the oxide film 512 is formed by a CVD method, a silicon oxide film is preferably formed using organosilane such as tetraethoxysilane (abbreviation: TEOS) (chemical formula: $Si(OC_2H_5)_4$), so that favorable bonding can be achieved.

[0238]

In this embodiment, the oxide film 512 (here, a SiO_x film) is formed by performing thermal oxidation treatment on the single crystal semiconductor substrate 510. The thermal oxidation treatment is preferably performed in an oxidizing atmosphere to which a halogen is added.

[0239]

For example, thermal oxidation treatment of the single crystal semiconductor substrate 510 is performed in an oxidizing atmosphere to which chlorine (Cl) is added, whereby the oxide film 512 can be formed through chlorine oxidation. In this case, the oxide film 512 is a film containing chlorine atoms. By such chlorine oxidation, heavy metal (e.g., Fe, Cr, Ni, or Mo) that is an extrinsic impurity is trapped and chloride of the metal is formed and then removed to the outside; thus, contamination of the single crystal semiconductor substrate 510 can be reduced. Moreover, after the bonding to the base substrate 500, impurity from the base substrate, such as Na, can be

fixed, so that contamination of the single crystal semiconductor substrate 510 can be prevented.

[0240]

Note that the halogen atoms contained in the oxide film 512 are not limited to chlorine atoms. A fluorine atom may be contained in the oxide film 512. As a method for fluorine oxidation of the surface of the single crystal semiconductor substrate 510, a method in which the single crystal semiconductor substrate 510 is soaked in an HF solution and then subjected to thermal oxidation treatment in an oxidizing atmosphere, a method in which thermal oxidation treatment is performed in an oxidizing atmosphere to which NF_3 is added, or the like can be used.

[0241]

Next, ions are accelerated by an electric field and the single crystal semiconductor substrate 510 is irradiated and added with the ions, whereby an embrittled region 514 where the crystal structure is damaged is formed in the single crystal semiconductor substrate 510 at a predetermined depth (see FIG. 15E).

[0242]

The depth at which the embrittled region 514 is formed can be controlled by the kinetic energy, mass, charge, or incidence angle of the ions, or the like. The embrittled region 514 is formed at approximately the same depth as the average penetration depth of the ions. Therefore, the thickness of the single crystal semiconductor layer to be separated from the single crystal semiconductor substrate 510 can be adjusted with the depth at which the ions are added. For example, the average penetration depth may be controlled such that the thickness of a single crystal semiconductor layer is approximately 10 nm to 500 nm, preferably, 50 nm to 200 nm.

[0243]

The above ion irradiation treatment can be performed with an ion-doping apparatus or an ion-implantation apparatus. As a typical example of the ion-doping apparatus, there is a non-mass-separation apparatus in which plasma excitation of a process gas is performed and an object to be processed is irradiated with all kinds of ion species generated. In this apparatus, the object to be processed is irradiated with

ion species of plasma without mass separation. In contrast, an ion-implantation apparatus is a mass-separation apparatus. In the ion-implantation apparatus, mass separation of ion species of plasma is performed and the object to be processed is irradiated with ion species having predetermined masses.

[0244]

In this embodiment, an example will be described in which an ion-doping apparatus is used to add hydrogen to the single crystal semiconductor substrate 510. A gas containing hydrogen is used as a source gas. As for ions used for the irradiation, the proportion of H_3^+ is preferably set high. Specifically, it is preferable that the proportion of H_3^+ be set 50% or higher (more preferably, 80% or higher) with respect to the total amount of H^+, H_2^+, and H_3^+. With a high proportion of H_3^+, the efficiency of ion irradiation can be improved.

[0245]

Note that ions to be added are not limited to ions of hydrogen. Ions of helium or the like may be added. Further, ions to be added are not limited to one kind of ions, and plural kinds of ions may be added. For example, in the case of performing irradiation with hydrogen and helium concurrently using an ion-doping apparatus, the number of steps can be reduced as compared with the case of performing irradiation of hydrogen and helium in different steps, and an increase in surface roughness of a single crystal semiconductor layer to be formed later can be suppressed.

[0246]

Note that heavy metal may also be added when the embrittled region 514 is formed with the ion doping apparatus; however, the ion irradiation is performed through the oxide film 512 containing halogen atoms, whereby contamination of the single crystal semiconductor substrate 510 due to the heavy metal can be prevented.

[0247]

Then, the base substrate 500 and the single crystal semiconductor substrate 510 are disposed to face each other and a surface of the nitrogen-containing layer 502 and a surface of the oxide film 512 are disposed in close contact with each other.

Thus, the base substrate 500 and the single crystal semiconductor substrate 510 are bonded to each other (see FIG. 15F).

[0248]

When bonding is performed, it is preferable that a pressure greater than or equal to 0.001 N/cm^2 and less than or equal to 100 N/cm^2, e.g., a pressure greater than or equal to 1 N/cm^2 and less than or equal to 20 N/cm^2, be applied to one part of the base substrate 500 or one part of the single crystal semiconductor substrate 510. When the bonding surfaces are made close to each other and disposed in close contact with each other by applying a pressure, a bonding between the nitrogen-containing layer 502 and the oxide film 512 is generated at the part where the close contact is made, and the bonding spontaneously spreads to almost the entire area. This bonding is performed under the action of the Van der Waals force or hydrogen bonding and can be performed at room temperature.

[0249]

Note that before the single crystal semiconductor substrate 510 and the base substrate 500 are bonded to each other, surfaces to be bonded to each other are preferably subjected to surface treatment. Surface treatment can improve the bonding strength at the interface between the single crystal semiconductor substrate 510 and the base substrate 500.

[0250]

As the surface treatment, wet treatment, dry treatment, or a combination of wet treatment and dry treatment can be used. Alternatively, wet treatment may be used in combination with different wet treatment or dry treatment may be used in combination with different dry treatment.

[0251]

Note that heat treatment for increasing the bonding strength may be performed after bonding. This heat treatment is performed at a temperature at which separation at the embrittled region 514 does not occur (for example, a temperature higher than or equal to room temperature and lower than 400 °C). Alternatively, bonding of the nitrogen-containing layer 502 and the oxide film 512 may be

performed while heating them at a temperature in this range. The heat treatment can be performed using a diffusion furnace, a heating furnace such as a resistance heating furnace, a rapid thermal annealing (RTA) apparatus, a microwave heating apparatus, or the like. The above temperature condition is merely an example, and an embodiment of the disclosed invention should not be construed as being limited to this example.

[0252]

Next, heat treatment is performed for separation of the single crystal semiconductor substrate 510 at the embrittled region, whereby a single crystal semiconductor layer 516 is formed over the base substrate 500 with the nitrogen-containing layer 502 and the oxide film 512 provided therebetween (see FIG. 15G).

[0253]

Note that the temperature for heat treatment in the separation is preferably as low as possible. This is because as the temperature in the separation is low, generation of roughness on the surface of the single crystal semiconductor layer 516 can be suppressed. Specifically, the temperature for the heat treatment in the separation may be higher than or equal to 300 °C and lower than or equal to 600 °C and the heat treatment is more effective when the temperature is higher than or equal to 400 °C and lower than or equal to 500 °C.

[0254]

Note that after the single crystal semiconductor substrate 510 is separated, the single crystal semiconductor layer 516 may be subjected to heat treatment at 500 °C or higher so that concentration of hydrogen remaining in the single crystal semiconductor layer 516 is reduced.

[0255]

Next, a surface of the single crystal semiconductor layer 516 is irradiated with laser light, whereby a single crystal semiconductor layer 518 in which the planarity of the surface is improved and the number of defects is reduced is formed (see FIGS. 15H). Note that instead of the laser light irradiation treatment, heat treatment may be

performed.

[0256]

Although the irradiation treatment with the laser light is performed just after the heat treatment for separation of the single crystal semiconductor layer 516 in this embodiment, one embodiment of the disclosed invention is not construed as being limited to this. Etching treatment may be performed after the heat treatment for separation of the single crystal semiconductor layer 516, to remove a region where there are many defects on the surface of the single crystal semiconductor layer 516, and then the laser light irradiation treatment may be performed. Alternatively, after the surface planarity of the single crystal semiconductor layer 516 is improved, the laser light irradiation treatment may be performed. Note that the etching treatment may be either wet etching or dry etching. Further, in this embodiment, a step of reducing the thickness of the single crystal semiconductor layer 516 may be performed after the laser light irradiation. In order to reduce the thickness of the single crystal semiconductor layer 516, any one or both of dry etching and wet etching may be employed.

[0257]

Through the above steps, an SOI substrate including the single crystal semiconductor layer 518 with favorable characteristics can be obtained (see FIG. 15H).

[0258]

<Method for manufacturing semiconductor device>

Next, a method for manufacturing a semiconductor device with the use of the SOI substrate, in particular, a method for manufacturing the transistor 560 will be described with reference to FIGS. 16A to 16E. Note that FIGS. 16A to 16E illustrate part of the SOI substrate formed by the method illustrated in FIGS. 15A to 15H, and are cross-sectional views corresponding to FIG. 14A.

[0259]

First, the single crystal semiconductor layer 518 is patterned to have an island shape so that a semiconductor layer 520 is formed (see FIG. 16A). Note that before

or after this step, an impurity element imparting n-type conductivity or an impurity element imparting p-type conductivity may be added to the semiconductor layer in order to control the threshold voltage of the transistor. In the case where silicon is used as the semiconductor, phosphorus, arsenic, or the like can be used as an impurity element imparting n-type conductivity. On the other hand, boron, aluminum, gallium, or the like can be used as an impurity element imparting p-type conductivity.

[0260]

Next, an insulating layer 522 is formed so as to cover the semiconductor layer 520, and a conductive layer 524 is formed in a region overlapping with the semiconductor layer 520 over the insulating layer 522 (see FIG. 16B).

[0261]

The insulating layer 522 is to be a gate insulating layer later. The insulating layer 522 can be formed, for example, by performing heat treatment (thermal oxidation treatment, thermal nitridation treatment, or the like) on a surface of the semiconductor layer 520. Instead of heat treatment, high-density plasma treatment may be employed. The high-density plasma treatment can be performed using, for example, a mixed gas of a rare gas such as He, Ar, Kr, or Xe and a gas such as oxygen, nitrogen oxide, ammonia, nitrogen, or hydrogen. Needless to say, the insulating layer may be formed using a CVD method, a sputtering method, or the like. The insulating layer preferably has a single-layer structure or a stacked structure using a film including any of silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, and the like formed by a CVD method, a sputtering method, or the like. The thickness of the insulating layer can be, for example, greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm. Here, a single-layer insulating layer containing silicon oxide is formed using a plasma CVD method.

[0262]

The conductive layer 524 is to be a gate electrode later. The conductive layer 524 can be formed using a metal material such as aluminum, copper, titanium, tantalum, or tungsten. The layer containing a conductive material may be formed using a semiconductor material such as polycrystalline silicon. There is no particular limitation on the method for forming the layer containing a conductive material, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, or a spin coating method can be employed. Note that this embodiment shows an example of the case where the layer containing a conductive material is formed using a metal material.

[0263]

Next, the insulating layer 522 and the conductive layer 524 are selectively etched, so that the gate insulating layer 522a and the gate electrode 524a are formed above the semiconductor layer 520 (see FIG. 16C). As the etching, dry etching is preferably performed, but wet etching can be performed. An etching gas and an etchant can be selected as appropriate depending on a material of layers to be etched.

[0264]

Then, the gate electrode 524a is used as a mask, and an impurity element imparting one conductivity type is added to the semiconductor layer 520, so that the channel formation region 526 and the impurity regions 528 are formed (see FIG. 16D). Note that phosphorus (P) or arsenic (As) is added here in order to form an n-channel transistor; an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. Here, the concentration of impurity to be added can be set as appropriate. In addition, after the impurity element is added, heat treatment for activation is performed.

[0265]

Note that when the semiconductor layer 520 is formed using a material containing silicon, a silicide region may be formed by forming silicide in part of the semiconductor layer 520 in order to further reduce the resistance of the source region and the drain region. The silicide region is formed in such a manner that metal is brought into contact with the semiconductor layer, and silicon in the semiconductor

layer is made to react with the metal by heat treatment (e.g., a GRTA method, an LRTA method, or laser irradiation). For the silicide region, for example, cobalt silicide, nickel silicide, or the like may be formed. In the case where the semiconductor layer 520 is thin, silicide reaction may proceed to a bottom of the semiconductor layer 520. As a metal material used for forming silicide, titanium, tungsten, molybdenum, zirconium, hafnium, tantalum, vanadium, neodymium, chromium, platinum, palladium, and the like can be given in addition to cobalt and nickel.

[0266]

Next, the insulating layer 532 and the insulating layer 534 are formed so as to cover the components formed in the above steps (see FIG. 16D). The insulating layer 532 and the insulating layer 534 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, or aluminum oxide. In particular, the insulating layer 532 and the insulating layer 534 are preferably formed using a low dielectric constant (low-k) material, whereby capacitance caused by an overlap of electrodes or wirings can be sufficiently reduced. Note that a porous insulating layer including these materials may be used for the insulating layer 532 and the insulating layer 534. Since the porous insulating layer has low dielectric constant as compared to a dense insulating layer, capacitance due to electrodes or wirings can be further reduced.

[0267]

In addition, a layer including an inorganic material containing a large amount of nitride, such as silicon nitride oxide or silicon nitride, may be included in the insulating layer 532 or the insulating layer 534. Thus, the impurity such as water or hydrogen contained in the material included in the transistor 560 in the lower portion can be prevented from entering the oxide semiconductor layer 544 of the transistor 562 in the upper portion that is formed later. Note that in this case, it is difficult to remove the layer including an inorganic insulating material containing a large amount of nitrogen only by CMP treatment performed in a later step; therefore, CMP treatment and etching treatment are preferably performed in combination.

[0268]

For example, silicon oxynitride and silicon oxide are used for forming the insulating layer 532 and the insulating layer 534, respectively. In this manner, only an inorganic insulating material containing a large amount of oxygen, such as silicon oxynitride or silicon oxide, is used for the insulating layer 532 and the insulating layer 534, whereby CMP treatment can be easily performed on the insulating layer 532 and the insulating layer 534 in a later step.

[0269]

Note that a stacked structure of the insulating layer 532 and the insulating layer 534 is employed here; however, one embodiment of the disclosed invention is not limited to this. A single-layer structure or a stacked structure including three or more layers can also be used. For example, the following structure may be employed: silicon oxynitride and silicon oxide are used for the insulating layer 532 and the insulating layer 534, respectively, and a silicon nitride oxide film is formed between the insulating layer 532 and the insulating layer 534.

[0270]

Through the above steps, the transistor 560 including the SOI substrate is formed (see FIG. 16D). Since the transistor 560 including a semiconductor material other than an oxide semiconductor is capable of high-speed operation, when the transistor is used as a reading transistor, high-speed reading operation is possible. Further, a logic circuit (also referred to as an arithmetic circuit) or the like can be formed using the transistor 560.

[0271]

Then, the insulating layer 532 and the insulating layer 534 are subjected to CMP treatment, so that a top surface of the gate electrode 524a is exposed (see FIG. 16E). Instead of CMP treatment, etching treatment or the like can be used as the treatment for exposing the top surface of the gate electrode 524a, and it is preferable that surfaces of the insulating layer 532 and the insulating layer 534 be as planar as possible in order that characteristics of the transistor 562 to be formed later are improved.

[0272]

After that, as treatment before formation of the transistor 562, CMP treatment is performed on the insulating layer 532 and the insulating layer 534, so that surfaces of the insulating layer 532 and the insulating layer 534 are planarized and a top surface of the gate electrode 524a is exposed (see FIG. 16E).

[0273]

The CMP treatment may be performed once or plural times. When the CMP treatment is performed plural times, first polishing is preferably performed with a high polishing rate followed by finishing polishing with a low polishing rate. In this manner, by combining polishing with different polishing rates, the planarity of the surfaces of the insulating layer 532 and the insulating layer 534 can be further improved.

[0274]

As the treatment for planarizing the insulating layer 532 and the insulating layer 534, etching treatment or the like can be performed instead of CMP treatment, and planarization is preferably performed so that each of the surfaces of the insulating layer 532 and the insulating layer 534 has an RMS roughness of less than or equal to 1 nm, or preferably less than or equal to 0.5 nm in order to improve the planarity and the uniformity of the oxide semiconductor layer 544 and improve characteristics of the transistor 562.

[0275]

In addition, when the stacked layer structure of the insulating layer 532 and the insulating layer 534 includes an inorganic insulating material containing a large amount of nitrogen, such as silicon nitride or silicon nitride oxide, since it is difficult to remove the inorganic insulating material containing a large amount of nitrogen only by the CMP treatment, CMP treatment and etching treatment are preferably performed in combination. As the etching treatment for the inorganic insulating material containing a large amount of nitrogen, either dry etching or wet etching may be used. However, in view of miniaturization of elements, dry etching is preferably used. In addition, it is preferable that etching conditions (an etching gas, an etchant, an etching time, a temperature, or the like) be set appropriately so that etching rates of the

respective insulating layers are equal to each other and high etching selectivity with the gate electrode 524a can be obtained. In addition, as an etching gas for dry etching, for example, a gas containing fluorine (trifluoromethane (CHF_3)), a gas to which a rare gas such as helium (He) or argon (Ar) is added, or the like can be used.

[0276]

In addition, when the top surface of the gate electrode 524a is exposed from the insulating layer 534, the top surface of the gate electrode 524a and a surface of the insulating layer 534 are included in the same surface.

[0277]

Note that before or after the above steps, a step for forming an additional electrode, wiring, semiconductor layer, or insulating layer may be performed. For example, an electrode which is connected to part of the metal compound region 528 and functions as a source or drain electrode of the transistor 560 may be formed. In addition, a multilayer wiring structure in which an insulating layer and a conductive layer are stacked is employed as a wiring structure, so that a highly-integrated semiconductor device can be provided.

[0278]

After that, the transistor 562 and the capacitor 564 which are electrically connected to the transistor 560 are manufactured (FIG. 14A). Since manufacturing methods of the transistor 562 and the capacitor 564 are the same as those of the transistor 262 and the capacitor 264, the description of the manufacturing methods are omitted here. The above embodiment can be referred to for the details of the manufacturing methods.

[0279]

Through the above steps, the semiconductor device in which the transistor including a semiconductor material other than an oxide semiconductor is included in the lower portion and the transistor including an oxide semiconductor is included in the upper portion, and which can be used as a memory device can be provided.

[0280]

With a combination of the transistor including a semiconductor material other

than an oxide semiconductor and the transistor including an oxide semiconductor, the semiconductor device capable of holding data for a long time and reading data at high speed, which can be used as a memory device, can be obtained.

[0281]

In addition, by providing the oxide semiconductor layer over a surface with favorable planarity, the semiconductor device in which the transistor whose transistor characteristics are improved is stacked over the transistor including a semiconductor material other than an oxide semiconductor can be provided.

[0282]

When the gate electrode 524a and the source or drain electrode 542a are directly connected to each other, higher integration of the semiconductor device can be achieved because a contact area can be reduced. Accordingly, a storage capacity per unit area of the semiconductor device which can be used as a memory device can be increased.

[0283]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0284]

[Embodiment 4]

In this embodiment, application examples of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 17A-1, 17A-2, and 17B. Here, an example of a memory device will be described. Note that in a circuit diagram, "OS" is written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0285]

In the semiconductor device illustrated in FIG. 17A-1, a first wiring (a 1st Line) is electrically connected to a source electrode of a transistor 700, and a second wiring (a 2nd Line) is electrically connected to a drain electrode of the transistor 700. A gate electrode of the transistor 700 and one of a source electrode and a drain

electrode of a transistor 710 are electrically connected to one of electrodes of a capacitor 720. A third wiring (a 3rd Line) is electrically connected to the other of the source electrode and the drain electrode of the transistor 710, and a fourth wiring (a 4th Line) is electrically connected to a gate electrode of the transistor 710. A fifth wiring (a 5th Line) is electrically connected to the other electrode of the capacitor 720.

[0286]

Here, a transistor including an oxide semiconductor is used as the transistor 710. Here, as the transistor including an oxide semiconductor, for example, the transistor 262, the transistor 272, the transistor 282, the transistor 292, or the transistor 562 described in the above embodiments can be used. A transistor including an oxide semiconductor has a characteristic of a significantly small off current. Therefore, when the transistor 710 is turned off, the potential of the gate electrode of the transistor 700 can be held for a very long time. By providing the capacitor 720, holding of charge given to the gate electrode of the transistor 700 and reading of held data can be easily performed. Here, as the capacitor 720, for example, the capacitor 264, the capacitor 274, the capacitor 284, the capacitor 294, or the capacitor 564 described in the above embodiments can be used.

[0287]

In addition, a transistor including a semiconductor material other than an oxide semiconductor is used as the transistor 700. Note that as the semiconductor material other than an oxide semiconductor, for example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material may be used. A transistor including such a semiconductor material can be operated at high speed easily. Here, as the transistor including a semiconductor material other than an oxide semiconductor, for example, the transistor 260 or the transistor 560 described in the above embodiments can be used.

[0288]

Alternatively, a structure without the capacitor 720 as illustrated in FIG. 17B can be employed.

[0289]

The semiconductor device illustrated in FIG. 17A-1 utilizes a characteristic in which the potential of the gate electrode of the transistor 700 can be held, thereby writing, holding, and reading data as follows.

[0290]

Firstly, writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 710 is turned on, so that the transistor 710 is turned on. Accordingly, the potential of the third wiring is supplied to the gate electrode of the transistor 700 and the capacitor 720. That is, predetermined charge is given to the gate electrode of the transistor 700 (writing). Here, one of charges for supply of two different potentials (hereinafter, a charge for supply of a low potential is referred to as a charge Q_L and a charge for supply of a high potential is referred to as a charge Q_H) is given to the gate electrode of the transistor 700. Note that charges giving three or more different potentials may be applied to improve a storage capacity. After that, the potential of the fourth wiring is set to a potential at which the transistor 710 is turned off, so that the transistor 710 is turned off. Thus, the charge given to the gate electrode of the transistor 700 is held (holding).

[0291]

Since the off current of the transistor 710 is significantly low, the charge of the gate electrode of the transistor 700 is held for a long time.

[0292]

Secondly, reading of data will be described. By supplying an appropriate potential (reading potential) to the fifth wiring while a predetermined potential (a constant potential) is supplied to the first wiring, the potential of the second wiring varies depending on the amount of charge held in the gate electrode of the transistor 700. This is because in general, when the transistor 700 is an n-channel transistor, an apparent threshold voltage V_{th_H} in the case where Q_H is given to the gate electrode of the transistor 700 is lower than an apparent threshold voltage V_{th_L} in the case where Q_L is given to the gate electrode of the transistor 700. Here, an apparent threshold

voltage refers to the potential of the fifth wiring, which is needed to turn on the transistor 700. Thus, the potential of the fifth wiring is set to a potential V_0 intermediate between V_{th_H} and V_{th_L}, whereby charge given to the gate electrode of the transistor 700 can be determined. For example, in the case where Q_H is given in writing, when the potential of the fifth wiring is set to V_0 ($> V_{th\_H}$), the transistor 700 is turned on. In the case where Q_L is given in writing, even when the potential of the fifth wiring is set to V_0 ($> V_{th\_L}$), the transistor 700 remains in an off state. Therefore, the held data can be read by the potential of the second wiring.

[0293]

Note that in the case where memory cells are arrayed to be used, only data of desired memory cells is needed to be read. Thus, in order that data of a predetermined memory cell is read and data of the other memory cells is not read, in the case where the transistors 700 are connected in parallel between the memory cells, potential at which the transistor 700 is turned off regardless of a state of the gate electrode, that is, potential lower than V_{th_H} may be supplied to fifth wirings of the memory cells whose data is not to be read. In the case where the transistors 700 are connected in series between the memory cells, potential at which the transistor 700 is turned on regardless of the state of the gate electrode, that is, potential higher than V_{th_L} may be supplied to the fifth wirings of the memory cells whose data is not to be read.

[0294]

Thirdly, rewriting of data will be described. Rewriting of data is performed in a manner similar to that of the writing and holding of data. That is, the potential of the fourth wiring is set to a potential at which the transistor 710 is turned on, so that the transistor 710 is turned on. Accordingly, the potential of the third wiring (potential related to new data) is supplied to the gate electrode of the transistor 700 and the capacitor 720. After that, the potential of the fourth wiring is set to a potential which the transistor 710 is turned off, so that the transistor 710 is turned off. Accordingly, charge related to new data is given to the gate electrode of the transistor 700.

[0295]

In the semiconductor device according to the disclosed invention, data can be directly rewritten by another writing of data as described above. Therefore, extracting of charge from a floating gate with the use of high voltage needed in a flash memory or the like is not necessary and thus, reduction in operation speed, which is attributed to erasing operation, can be suppressed. In other words, high-speed operation of the semiconductor device can be realized.

[0296]

Note that the source electrode or the drain electrode of the transistor 710 is electrically connected to the gate electrode of the transistor 700, thereby having an effect similar to that of a floating gate of a floating gate transistor used for a nonvolatile memory element. Therefore, a portion in the drawing where the source electrode or the drain electrode of the transistor 710 is electrically connected to the gate electrode of the transistor 700 is called a floating gate portion FG in some cases. When the transistor 710 is off, the floating gate portion FG can be regarded as being embedded in an insulator and thus charge is held in the floating gate portion FG. The amount of off current of the transistor 710 including an oxide semiconductor is smaller than or equal to one hundred thousandth of the amount of off current of a transistor including a silicon semiconductor or the like; thus, lost of the charge accumulated in the floating gate portion FG due to leakage current of the transistor 710 is negligible. That is, with the transistor 710 including an oxide semiconductor, a nonvolatile memory device which can hold data without being supplied with power can be realized.

[0297]

For example, when the off current of the transistor 710 is less than or equal to 10 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) at room temperature and the capacitance value of the capacitor 720 is approximately 10 fF, data can be held for 10^4 seconds or longer. It is needless to say that the holding time depends on transistor characteristics and the capacitance value.

[0298]

Further, in that case, the problem of deterioration of a gate insulating film (tunnel insulating film), which is pointed out in a conventional floating gate transistor, does not exist. That is, the deterioration of a gate insulating film due to injection of an electron into a floating gate, which has been traditionally regarded as a problem, can be solved. This means that there is no limit on the number of times of writing in principle. Furthermore, high voltage needed for writing or erasing in a conventional floating gate transistor is not necessary.

[0299]

The components such as transistors in the semiconductor device in FIG. 17A-1 can be regarded as including a resistor and a capacitor as shown in FIG. 17A-2. That is, in FIG. 17A-2, the transistor 700 and the capacitor 720 are each regarded as including a resistor and a capacitor. R1 and C1 denote the resistance value and the capacitance value of the capacitor 720, respectively. The resistance R1 corresponds to the resistance of the insulating layer included in the capacitor 720. R2 and C2 denote the resistance value and the capacitance value of the transistor 700, respectively. The resistance value R2 corresponds to the resistance value which depends on a gate insulating layer at the time when the transistor 700 is on. The capacitance value C2 corresponds to the capacitance value of so-called gate capacitance (capacitance formed between the gate electrode and each of the source electrode and the drain electrode and capacitance formed between the gate electrode and the channel formation region).

[0300]

An electron holding period (also referred to as a data holding period) is determined mainly by the off current of the transistor 710 under the conditions that gate leakage of the transistor 710 is sufficiently small and that $R1 \geq ROS$ and $R2 \geq ROS$ are satisfied, where the resistance value (also referred to as effective resistance) between the source electrode and the drain electrode in the case where the transistor 710 is off is ROS.

[0301]

On the other hand, when the conditions are not satisfied, it is difficult to

sufficiently secure the holding period even if the off current of the transistor 710 is small enough. This is because a leakage current other than the off current of the transistor 710 (e.g., a leakage current generated between the source electrode and the gate electrode) is large. Thus, it can be said that the semiconductor device disclosed in this embodiment desirably satisfies the above relation.

[0302]

It is preferable that $C1 \geq C2$ be satisfied. This is because when C1 is large, the potential of the fifth wiring can be supplied to the floating gate portion FG efficiently at the time of controlling the potential of the floating gate portion FG by the fifth wiring, and a difference between potentials (e.g., the reading potential and a non-reading potential) supplied to the fifth wiring can be reduced.

[0303]

When the above relation is satisfied, a more preferable semiconductor device can be realized. Note that R1 and R2 are controlled by the gate insulating layer of the transistor 700 and the insulating layer of the capacitor 720. The same relation is applied to C1 and C2. Therefore, the material, the thickness, and the like of the gate insulating layer are desirably set as appropriate to satisfy the above relation.

[0304]

In the semiconductor device described in this embodiment, the floating gate portion FG has an effect similar to a floating gate of a floating gate transistor of a flash memory or the like, but the floating gate portion FG of this embodiment has a feature which is essentially different from that of the floating gate of the flash memory or the like. In the case of a flash memory, since a voltage applied to a control gate is high, it is necessary to keep a proper distance between cells in order to prevent the potential from affecting a floating gate of the adjacent cell. This is one of factors inhibiting high integration of the semiconductor device. The factor is attributed to a basic principle of a flash memory, in which a tunneling current flows in applying a high electrical field.

[0305]

Further, because of the above principle of a flash memory, deterioration of an

insulating film proceeds and thus another problem of the limit on the number of times of rewriting (approximately 10^4 to 10^5 times) occurs.

[0306]

The semiconductor device according to the disclosed invention is operated by switching of a transistor including an oxide semiconductor and does not use the above-described principle of charge injection by a tunneling current. That is, high electrical field for charge injection is not necessary unlike a flash memory. Accordingly, it is not necessary to consider an influence of a high electrical field from a control gate on an adjacent cell, which facilitates high integration.

[0307]

Further, charge injection by a tunneling current is not utilized, which means that there is no cause for deterioration of a memory cell. In other words, the semiconductor device according to the disclosed invention has higher durability and reliability than a flash memory.

[0308]

In addition, it is also advantageous that a high electrical field is unnecessary and a large supplemental circuit (such as a booster circuit) is unnecessary as compared to a flash memory.

[0309]

In the case where the dielectric constant εr1 of the insulating layer included in the capacitor 720 is different from the dielectric constant εr2 of the insulating layer included in the transistor 700, it is easy to satisfy $C1 \geq C2$ while $2 \cdot S2 \geq S1$ (desirably, $S2 \geq S1$) is satisfied where S1 is the area of the insulating layer included in the capacitor 720 and S2 is the area of the insulating layer forming the gate capacitance of the transistor 700. That is, it is easy to satisfy $C1 \geq C2$ while it is satisfied that the area of the insulating layer included in the capacitor 720 is small. Specifically, for example, a film formed of a high-k material such as hafnium oxide or a stack of a film formed of a high-k material such as hafnium oxide and a film formed of an oxide semiconductor is used for the insulating layer included in the capacitor 720 so that εr1 can be set to 10 or more, preferably 15 or more, and silicon oxide is used for the

insulating layer forming the gate capacitance so that εr2 can be set to 3 to 4.

[0310]

Combination of such structures enables higher integration of the semiconductor device according to the disclosed invention.

[0311]

Note that an n-channel transistor in which electrons are majority carriers is used in the above description; it is needless to say that a p-channel transistor in which holes are majority carriers can be used instead of the n-channel transistor.

[0312]

As described above, a semiconductor device according to an embodiment of the disclosed invention has a nonvolatile memory cell including a writing transistor where a leakage current (off current) between a source and a drain in an off state is small, a reading transistor including a semiconductor material different from that of the writing transistor, and a capacitor.

[0313]

The off current of the writing transistor is preferably less than or equal to 100 zA (1×10^{-19} A), more preferably less than or equal to 10 zA (1×10^{-20} A), still more preferably less than or equal to 1 zA (1×10^{-21} A) at ambient temperature (e.g., 25 °C). In the case of general silicon, it is difficult to achieve such small off current. However, in a transistor obtained by processing an oxide semiconductor under an appropriate condition, a small off current can be achieved. Therefore, a transistor including an oxide semiconductor is preferably used as the writing transistor.

[0314]

In addition, a transistor including an oxide semiconductor has a small subthreshold swing (S-value), so that the switching rate can be sufficiently high even if mobility is comparatively low. Therefore, by using the transistor as the writing transistor, rising of a writing pulse given to the floating gate portion FG can be very sharp. Further, an off current is small and thus, the amount of charge held in the floating gate portion FG can be reduced. That is, by using a transistor including an oxide semiconductor, rewriting of data can be performed at high speed.

[0315]

As for the reading transistor, although there is no limitation on off current, it is desirable to use a transistor which is operated at high speed in order to increase the reading rate. For example, a transistor with a switching rate of 1 nanosecond or lower is preferably used as the reading transistor.

[0316]

In this manner, when a transistor including an oxide semiconductor is used as a writing transistor, and a transistor including a semiconductor material other than an oxide semiconductor is used as a reading transistor, a semiconductor device capable of holding data for a long time and reading data at high speed, which can be used as a memory device, can be obtained.

[0317]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0318]

[Embodiment 5]

In this embodiment, application examples of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 18A and 18B and FIGS. 19A to 19C.

[0319]

FIGS. 18A and 18B are examples of circuit diagrams of semiconductor devices each including a plurality of semiconductor devices (hereinafter also referred to as memory cells 750) illustrated in FIG. 17A-1. FIG. 18A is a circuit diagram of a so-called NAND semiconductor device in which the memory cells 750 are connected in series, and FIG. 18B is a circuit diagram of a so-called NOR semiconductor device in which the memory cells 750 are connected in parallel.

[0320]

The semiconductor device in FIG. 18A includes a source line SL, a bit line BL, a first signal line S1, a plurality of second signal lines S2, a plurality of word lines WL,

and the plurality of memory cells 750. In FIG. 18A, one source line SL and one bit line BL are provided, but this embodiment is not limited to this. A plurality of source lines SL and a plurality of bit lines BL may be provided.

[0321]

In each of the memory cells 750, a gate electrode of a transistor 700, one of a source electrode and a drain electrode of a transistor 710, and one of electrodes of a capacitor 720 are electrically connected to one another. The first signal line S1 and the other of the source electrode and the drain electrode of the transistor 710 are electrically connected to each other, and the second signal line S2 and the gate electrode of the transistor 710 are electrically connected to each other. The word line WL and the other of the electrodes of the capacitor 720 are electrically connected to each other.

[0322]

Further, the source electrode of the transistor 700 included in the memory cell 750 is electrically connected to the drain electrode of the transistor 700 in the adjacent memory cell 750. The drain electrode of the transistor 700 included in the memory cell 750 is electrically connected to the source electrode of the transistor 700 in the adjacent memory cell 750. Note that the drain electrode of transistor 700 included in the memory cell 750 of the plurality of memory cells connected in series, which is provided at one end, and the bit line are electrically connected to each other. The source electrode of the transistor 700 included in the memory cell 750 of the plurality of memory cells connected in series, which is provided at the other end, and the source line are electrically connected to each other.

[0323]

In the semiconductor device in FIG. 18A, writing operation and reading operation are performed in each row. The writing operation is performed as follows. A potential at which the transistor 710 is turned on is applied to the second signal line S2 of a row where writing is to be performed, whereby the transistor 710 of the row where writing is to be performed is turned on. Accordingly, the potential of the first signal line S1 is supplied to the gate electrode of the transistor 700 of the specified

row, so that a predetermined charge is given to the gate electrode. Thus, data can be written to the memory cell of the specified row.

[0324]

Further, the reading operation is performed as follows. First, a potential at which the transistor 700 is turned on regardless of charge given to the gate electrode thereof is supplied to the word lines WL of the rows other than the row where reading is to be performed, so that the transistors 700 of the rows other than the row where reading is to be performed are turned on. Then, a potential (reading potential) at which an on state or an off state of the transistor 700 is determined depending on charge in the gate electrode of transistor 700 is supplied to the word line WL of the row where reading is to be performed. After that, a constant potential is supplied to the source line SL so that a reading circuit (not shown) connected to the bit line BL is operated. Here, the plurality of transistors 700 between the source line SL and the bit line BL are on except the transistors 700 of the row where reading is to be performed; therefore, conductance between the source line SL and the bit line BL is determined by a state (an on state or an off state) of the transistor 700 of the row where reading is to be performed. The conductance of the transistors 700 in the rows where which reading is performed depends on charge in the gate electrodes thereof. Thus, a potential of the bit line BL varies accordingly. By reading the potential of the bit line with the reading circuit, data can be read from the memory cells of the specified row.

[0325]

The semiconductor device in FIG. 18B includes a plurality of source lines SL, a plurality of bit lines BL, a plurality of first signal lines S1, a plurality of second signal lines S2, a plurality of word lines WL, and a plurality of memory cells 750. The gate electrode of the transistor 700, one of the source electrode and the drain electrode of the transistor 710, and one of electrodes of the capacitor 720 are electrically connected to one another. The source line SL and the source electrode of the transistor 700 are electrically connected to each other. The bit line BL and the drain electrode of the transistor 700 are electrically connected to each other. The first signal line S1 and the other of the source electrode and the drain electrode of the

transistor 710 are electrically connected to each other, and the second signal line S2 and the gate electrode of the transistor 710 are electrically connected to each other. The word line WL and the other electrode of the capacitor 720 are electrically connected to each other.

[0326]

In the semiconductor device in FIG. 18B, writing operation and reading operation are performed in each row. The writing operation is performed in a manner similar to that of the semiconductor device in FIG. 18A. The reading operation is performed as follows. First, a potential at which the transistor 700 is turned off regardless of charge given to the gate electrode of the transistor 700 is supplied to the word lines WL of the rows other than the row where reading is to be performed, so that the transistor 700 of the rows other than the row where reading is to be performed are turned off. Then, a potential (reading potential) at which an on state or an off state of the transistor 700 is determined depending on charge in the gate electrode of the transistor 700 is supplied to the word line WL of the row where reading is to be performed. After that, a constant potential is supplied to the source line SL so that a reading circuit (not shown) connected to the bit line BL is operated. Here, conductance between the source lines SL and the bit lines BL is determined by a state (an on state or an off state) of the transistor 700 of the row where reading is performed. That is, a potential of the bit lines BL depends on charge in the gate electrodes of the transistors 700 of the row where reading is performed. By reading the potential of the bit line with the reading circuit, data can be read from the memory cells of the specified row.

[0327]

Although the amount of data which can be held in each of the memory cells 750 is one bit in the above description, the structure of the memory device of this embodiment is not limited to this. The amount of data which is held in each of the memory cells 750 may be increased by preparing three or more potentials to be supplied to the gate electrode of the transistor 700. For example, in the case where the number of potentials to be supplied to the gate electrode of the transistor 700 is

four, data of two bits can be stored in each of the memory cells.

[0328]

Next, examples of reading circuits which can be used for the semiconductor devices in FIGS. 18A and 18B, or the like will be described with reference to FIGS. 19A to 19C.

[0329]

FIG. 19A illustrates a schematic of the reading circuit. The reading circuit includes a transistor and a sense amplifier circuit.

[0330]

At the time of reading of data, a terminal A is connected to a bit line to which a memory cell from which data is read is connected. Further, a bias potential V_{bias} is applied to a gate electrode of the transistor so that a potential of the terminal A is controlled.

[0331]

The resistance of the memory cell 750 varies depending on stored data. Specifically, when the transistor 700 in a selected memory cell 750 is on, the memory cell has a low resistance; whereas when the transistor 700 in a selected memory cell 750 is off, the memory cell has a high resistance.

[0332]

When the memory cell has a high resistance, a potential of the terminal A is higher than a reference potential V_{ref} and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A. On the other hand, when the memory cell has a low resistance, the potential of the terminal A is lower than the reference potential V_{ref} and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A.

[0333]

Thus, by using the reading circuit, data can be read from the memory cell. Note that the reading circuit of this embodiment is one of examples. Another circuit may be used. The reading circuit may further include a precharge circuit. Instead of the reference potential V_{ref}, a reference bit line may be connected to the sense

amplifier circuit.

[0334]

FIG. 19B illustrates a differential sense amplifier which is an example of sense amplifier circuits. The differential sense amplifier has an input terminal $V_{in}(+)$ and an input terminal $V_{in}(-)$, and an output terminal V_{out}, and amplifies the difference between $V_{in}(+)$ and $V_{in}(-)$. V_{out} is approximately high output when $V_{in}(+) > V_{in}(-)$, and is approximately low output when $V_{in}(+) < V_{in}(-)$. In the case where the differential sense amplifier is used for the reading circuit, one of V_{in} (+) and V_{in} (−) is connected to the input terminal A, and the reference potential V_{ref} is supplied to the other of V_{in} (+) and V_{in} (−).

[0335]

FIG. 19C illustrates a latch sense amplifier which is an example of sense amplifier circuits. The latch sense amplifier has input-output terminals V1 and V2 and input terminals of control signals Sp and Sn. First, the control signals Sp and Sn are set to a signal High and a signal Low, respectively, and a power supply potential (V_{dd}) is interrupted. Then, potentials to be compared are applied to V_1 and V_2. After that, the control signals Sp and Sn are set to a signal Low and a signal High, respectively, and a power supply potential (V_{dd}) is supplied. If $V_{1in} > V_{2in}$ is satisfied for the potentials for comparison V_{1in} and V_{2in}, an output from V_1 is a signal High and an output from V_2 is a signal Low, whereas an output from V_1 is a signal Low and an output from V_2 is a signal High if $V_{1in} < V_{2in}$ is satisfied. By utilizing such a relation, the difference between V_{1in} and V_{2in} can be amplified. In the case where the latch sense amplifier is used for the reading circuit, one of V_1 and V_2 is connected to the terminal A and the output terminal through a switch, and the reference potential V_{ref} is supplied to the other of V_1 and V_2.

[0336]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0337]

[Embodiment 6]

In this embodiment, application of the semiconductor device described in any of the above embodiments to an electronic device is described with reference to FIGS. 20A to 20F. In this embodiment, the case where the above semiconductor device is applied to an electronic device such as a computer, a mobile phone (also referred to as a mobile telephone or a mobile telephone device), a portable information terminal (including a portable game machine, an audio reproducing device, and the like), a digital camera, a digital video camera, an electronic paper, or a television device (also referred to as a television or a television receiver) will be described.

[0338]

FIG. 20A illustrates a laptop personal computer which includes a housing 601, a housing 602, a display portion 603, a keyboard 604, and the like. In the housing 601 and the housing 602, the semiconductor device of any of the above embodiments which is provided with a combination of a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor is provided. Therefore, the laptop personal computer capable of holding data for a long time and reading data at high speed can be obtained.

[0339]

FIG. 20B illustrates a portable information terminal (personal digital assistance (PDA)) which includes a main body 611 provided with a display portion 613, an external interface 615, operation buttons 614, and the like. In addition, a stylus 612 which controls the portable information terminal and the like are provided. In the main body 611, the semiconductor device of any of the above embodiments which is provided with a combination of the transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor is provided. Therefore, the portable information terminal capable of holding data for a long time and reading data at high speed can be obtained.

[0340]

FIG. 20C illustrates an electronic book reader 620 which is mounted with electronic paper and includes two housings, a housing 621 and a housing 623. The

housing 621 and the housing 623 are respectively provided with a display portion 625 and a display portion 627. The housing 621 is combined with the housing 623 by a hinge 637, so that the electronic book reader 620 can be opened and closed using the hinge 637 as an axis. The housing 621 is provided with a power button 631, operation keys 633, a speaker 635, and the like. In at least one of the housing 621 and the housing 623, the semiconductor device of any of the above embodiments which is provided with a combination of a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor is provided. Therefore, the electronic book reader capable of holding data for a long time and reading data at high speed can be obtained.

[0341]

FIG. 20D illustrates a mobile phone which includes two housings, a housing 640 and a housing 641. Moreover, the housing 640 and the housing 641 in a state where they are developed as illustrated in FIG. 20D can be slid so that one is lapped over the other. Therefore, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried around. The housing 641 includes a display panel 642, a speaker 643, a microphone 644, a pointing device 646, a camera lens 647, an external connection terminal 648, and the like. The housing 640 includes a solar cell 649 for charging the mobile phone, an external memory slot 650, and the like. The display panel 642 is provided with a touch-panel function. A plurality of operation keys 645 which are displayed as images is illustrated by dashed lines in FIG. 20D. In addition, an antenna is incorporated in the housing 641. In at least one of the housing 640 and the housing 641, the semiconductor device of any of the above embodiments which is provided with a combination of a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor is provided. Therefore, the mobile phone capable of holding data for a long time and reading data at high speed can be obtained.

[0342]

FIG. 20E illustrates a digital camera which includes a main body 661, a display portion 667, an eyepiece portion 663, an operation switch 664, a display

portion 665, a battery 666, and the like. In the main body 661, the semiconductor device of any of the above embodiments which is provided with a combination of a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor is included. Therefore, the digital camera capable of holding data for a long time and reading data at high speed can be obtained.

[0343]

FIG. 20F illustrates a television device 670 which includes a housing 671, a display portion 673, a stand 675, and the like. The television device 670 can be operated with an operation switch of the housing 671 or a remote controller 680. In the housing 671 and the remote controller 680, the semiconductor device of any of the above embodiments which is provided with a combination of a transistor including an oxide semiconductor and a transistor including a semiconductor material other than an oxide semiconductor is provided. Therefore, the television device capable of holding data for a long time and reading data at high speed can be obtained.

[0344]

As described above, the electronic devices described in this embodiment are each mounted with the semiconductor device according to any of the above embodiments. Therefore, an electronic device having characteristics of being small, high-speed operation, and low power consumption can be realized.

[Example 1]

[0345]

In this example, the following steps were performed: a transistor was manufactured using an SOI substrate, an interlayer insulating layer was formed over the transistor, CMP treatment was performed on the interlayer insulating layer, and the planarity of the interlayer insulating layer before and after the CMP treatment was evaluated.

[0346]

Steps for manufacturing the transistor and the interlayer insulating layer formed over the transistor, which are employed in this example, will be described.

[0347]

First, an SOI substrate including a glass substrate, a thermal oxide film (the thickness: 100 nm) provided over the glass substrate, and a single crystal silicon layer (the thickness: 60 nm) provided over the thermal oxide film was prepared. Then, the single crystal silicon layer formed over the glass substrate with the thermal oxide film provided therebetween was patterned using dry etching.

[0348]

Next, a silicon oxynitride film (the thickness: 20 nm) was deposited using a CVD method so as to cover the single crystal silicon layer and the glass substrate, so that a gate insulating layer was formed.

[0349]

Then, a tantalum nitride film (the thickness: 30 nm) was deposited over the gate insulating layer using a sputtering method, and then a tungsten film (the thickness: 370 nm) was deposited using a sputtering method. After that, a stacked layer of the tantalum nitride film and the tungsten film was patterned using dry etching, so that a gate electrode was formed.

[0350]

As described above, a top-gate transistor in which the single crystal silicon layer was provided over the glass substrate with the thermal oxide film provided therebetween, the gate insulating layer was provided over the single crystal silicon layer, and the gate electrode was provided over the gate insulating layer could be manufactured.

[0351]

Next, a silicon oxynitride film (the thickness: 50 nm) was deposited using a plasma CVD method so as to cover the transistor. The silicon oxynitride film functions as a protective insulating layer for the transistor. After that, heat treatment was performed at 550 °C for one hour. Further, heat treatment was performed at 450 °C for one hour in a hydrogen atmosphere.

[0352]

Further, a silicon oxide film (the thickness: 500 nm) was deposited using a

sputtering method so as to cover the protective insulating layer. The silicon oxide film functions as an interlayer insulating layer.

[0353]

Finally, the interlayer insulating layer formed using a silicon oxide film was subjected to CMP treatment so that the polished interlayer insulating layer over the gate electrode has a thickness of 340 nm. At this time, a polyurethane polishing cloth was used, and silica slurry (the grain size: 150 nm) was used as a chemical solution for supplying slurry. The other CMP conditions are as follows: the slurry flow rate was 150 ml/min, the polishing pressure was 0.03 MPa, the spindle rotation speed was 20 rpm, the table rotation speed was 20 rpm, and processing time was 3 min.

[0354]

Next, an evaluation method of the planarity of the interlayer insulating layer performed before and after the CMP treatment will be described.

[0355]

In this example, the planarity of the interlayer insulating layer was evaluated by measuring the RMS roughness of a surface of the interlayer insulating layer with an atomic force microscope (AFM). As the AFM, SPA-500 manufactured by SII NanoTechnology Inc. was used. Conditions of the measurement were as follows: the scan rate was 1.0 Hz, the measurement area was 1 μm × 1 μm, and the measurement points were 4.

[0356]

An AFM image of the interlayer insulating layer before the CMP treatment is shown in FIG, 21, and an AFM image of the interlayer insulating layer after the CMP treatment is shown in FIG. 22. As is found in the comparison between FIG. 21 and FIG. 22, the planarity of the surface of the interlayer insulating layer is largely improved by the CMP treatment, and the RMS roughness thereof is reduced from 2.33 nm to 0.37 nm.

[0357]

By providing an oxide semiconductor layer over the interlayer insulating layer

having such a favorable planarity, the planarity and uniformity of the oxide semiconductor layer can be favorable. Here, as for the planarity and uniformity of the oxide semiconductor layer, at least a portion including a channel formation region of the oxide semiconductor layer may have favorable planarity and uniformity. In addition, by using the oxide semiconductor layer with favorable planarity and uniformity, characteristics of a transistor can be improved.

This application is based on Japanese Patent Application serial No. 2010-029278 filed with Japan Patent Office on February 12, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising

a first transistor;

an insulating layer over the first transistor; and

a second transistor over the insulating layer,

wherein the first transistor comprises:

a first channel formation region;

a first gate insulating layer provided over the first channel formation region;

a first gate electrode overlapping with the first channel formation region, over the first gate insulating layer; and

a first source electrode electrically connected to the first channel formation region and a first drain electrode electrically connected to the first channel formation region,

wherein the second transistor comprises:

a second channel formation region including an oxide semiconductor;

a second source electrode electrically connected to the second channel formation region and a second drain electrode electrically connected to the second channel formation region;

a second gate electrode overlapping with the second channel formation region; and

a second gate insulating layer provided between the second channel formation region and the second gate electrode,

wherein the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region, and

wherein the insulating layer includes a surface whose root-mean-square surface roughness is less than or equal to 1 nm.

2. The semiconductor device according to claim 1,

wherein a top surface of the first gate electrode is exposed to be included in a same surface as the insulating layer, and

wherein the first gate electrode and the second source electrode or the second drain electrode are in contact with each other on the top surface of the first gate electrode.

3. The semiconductor device according to claim 1, wherein a top surface of the first gate electrode is aligned with the surface of the insulating layer.

4. The semiconductor device according to claim 1, wherein the surface of the insulating layer is formed through a CMP treatment.

5. The semiconductor device according to claim 1, further comprising impurity regions with the first channel formation region provided therebetween.

6. The semiconductor device according to claim 1, wherein the semiconductor device is incorporated in one selected from the group consisting of a computer, a personal digital assistance, an electronic book, a mobile phone, a camera and a television device.

7. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first transistor including a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode overlapping with the first channel formation region over the first gate insulating layer, a first source electrode layer electrically connected to the first channel formation region, and a first drain electrode electrically connected to the first channel formation region;

forming an insulating layer over the first transistor;

planarizing the insulating layer so that a surface of the insulating layer has a

root-mean-square surface roughness of less than or equal to 1 nm; and

forming a second transistor including a second channel formation region including an oxide semiconductor, a second source electrode electrically connected to the second channel formation region, a second drain electrode electrically connected to the second channel formation region, a second gate electrode overlapping with the second channel formation region, and a gate insulating layer provided between the second channel formation region and the second gate electrode,

wherein the channel formation region including the oxide semiconductor is in contact with the insulating layer, and

wherein the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region.

8. The method for manufacturing a semiconductor device according to claim 7, wherein a top surface of the first gate electrode is aligned with the surface of the insulating layer.

9. The method for manufacturing a semiconductor device according to claim 7, wherein the second channel formation region is formed over the surface of the insulating layer.

10. The method for manufacturing a semiconductor device according to claim 7, wherein the semiconductor device is incorporated in one selected from the group consisting of a computer, a personal digital assistance, an electronic book, a mobile phone, a camera and a television device.

11. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first transistor including a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode which overlaps with the first channel formation region and is provided over

the first gate insulating layer, a first source electrode electrically connected to the first channel formation region, and a first drain electrode electrically connected to the first channel formation region;

forming an insulating layer over the first transistor;

planarizing the insulating layer so that a surface of the insulating layer has a root-mean-square roughness of less than or equal to 1 nm and a top surface of the first gate electrode is exposed to be included in a same surface as the insulating layer; and

forming a second transistor including a second channel formation region including an oxide semiconductor over the insulating layer, a second source electrode electrically connected to the second channel formation region, a second drain electrode electrically connected to the second channel formation region, a second gate electrode provided to overlap with the second channel formation region, a second gate insulating layer provided between the second channel formation region and the second gate electrode,

wherein the second source electrode or the second drain electrode are provided to be in contact with the top surface of the first gate electrode, and

wherein the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region.

12. The method for manufacturing a semiconductor device according to claim 11, wherein the top surface of the first gate electrode is aligned with the surface of the insulating layer.

13. The method for manufacturing a semiconductor device according to claim 11, wherein the second channel formation region is formed over the surface of the insulating layer.

14. The method for manufacturing a semiconductor device according to claim 11, wherein the semiconductor device is incorporated in one selected from the group consisting of a computer, a personal digital assistance, an electronic book, a mobile

phone, a camera and a television device.

15. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first transistor including a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode overlapping with the first channel formation region over the first gate insulating layer, a first source electrode layer electrically connected to the first channel formation region, and a first drain electrode electrically connected to the first channel formation region;

forming an insulating layer over the first transistor;

planarizing the insulating layer by a CMP treatment; and

forming a second transistor including a second channel formation region including an oxide semiconductor, a second source electrode electrically connected to the second channel formation region, a second drain electrode electrically connected to the second channel formation region, a second gate electrode overlapping with the second channel formation region, and a gate insulating layer provided between the second channel formation region and the second gate electrode,

wherein the channel formation region including the oxide semiconductor is in contact with the insulating layer,

wherein the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region.

16. The method for manufacturing a semiconductor device according to claim 15, wherein a top surface of the first gate electrode is aligned with a surface of the insulating layer.

17. The method for manufacturing a semiconductor device according to claim 15, wherein the second channel formation region is formed over a surface of the insulating layer.

18. The method for manufacturing a semiconductor device according to claim 15, wherein the semiconductor device is incorporated in one selected from the group consisting of a computer, a personal digital assistance, an electronic book, a mobile phone, a camera and a television device.

19. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first transistor including a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode which overlaps with the first channel formation region and is provided over the first gate insulating layer, a first source electrode electrically connected to the first channel formation region, and a first drain electrode electrically connected to the first channel formation region;

forming an insulating layer over the first transistor;

planarizing the insulating layer by a CMP treatment so that a top surface of the first gate electrode is exposed to be included in a same surface as the insulating layer; and

forming a second transistor including a second channel formation region including an oxide semiconductor over the insulating layer, a second source electrode electrically connected to the second channel formation region, a second drain electrode electrically connected to the second channel formation region, a second gate electrode provided to overlap with the second channel formation region, a second gate insulating layer provided between the second channel formation region and the second gate electrode,

wherein the second source electrode or the second drain electrode are provided to be in contact with the top surface of the first gate electrode, and

wherein the first channel formation region includes a semiconductor material different from a semiconductor material of the second channel formation region.

20. The method for manufacturing a semiconductor device according to claim 19, wherein the top surface of the first gate electrode is aligned with the surface of the insulating layer.

21. The method for manufacturing a semiconductor device according to claim 19, wherein the second channel formation region is formed over the surface of the insulating layer.

22. The method for manufacturing a semiconductor device according to claim 19, wherein the semiconductor device is incorporated in one selected from the group consisting of a computer, a personal digital assistance, an electronic book, a mobile phone, a camera and a television device.

FIG. 1

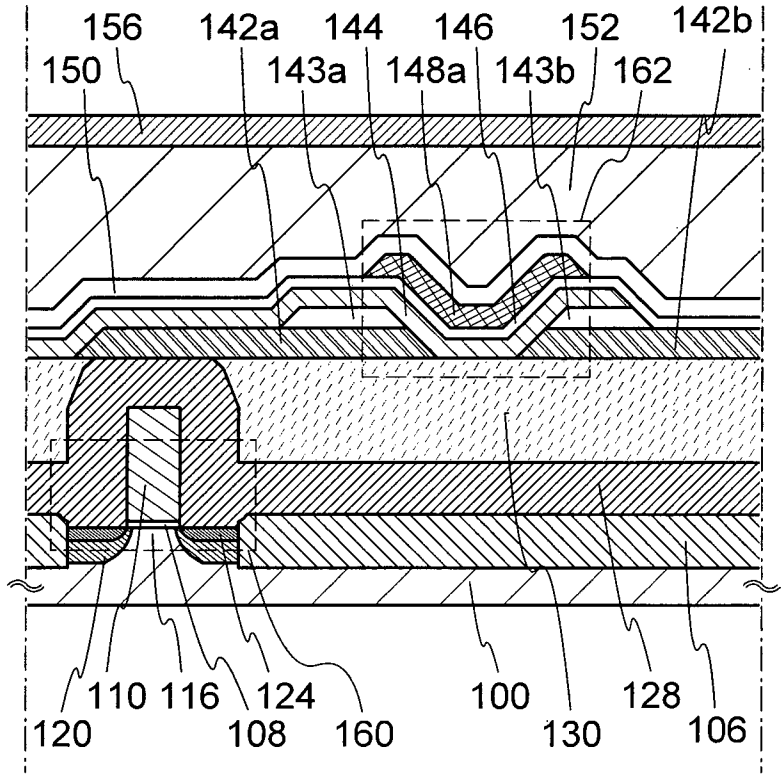

156
142a
144
146
152
142b
150
143a
148a
143b
162
110
116
124
100
128
120
108
160
130
106

FIG. 2A

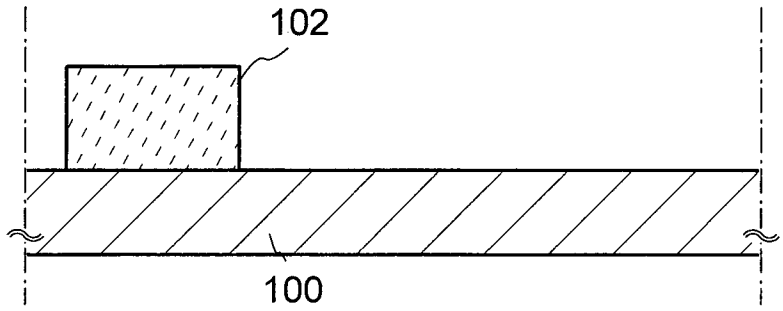


FIG. 2B

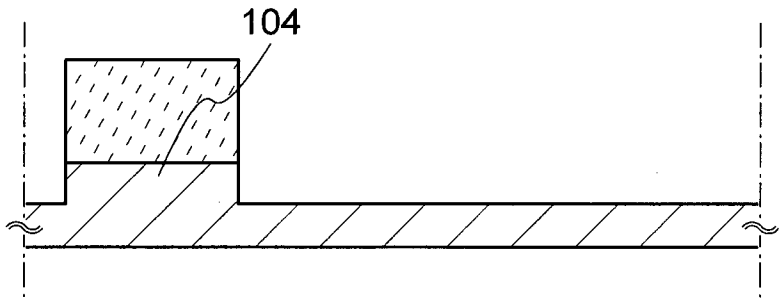


FIG. 2C

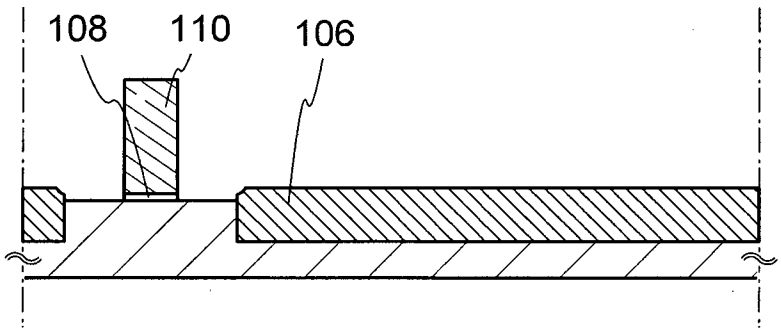


FIG. 2D

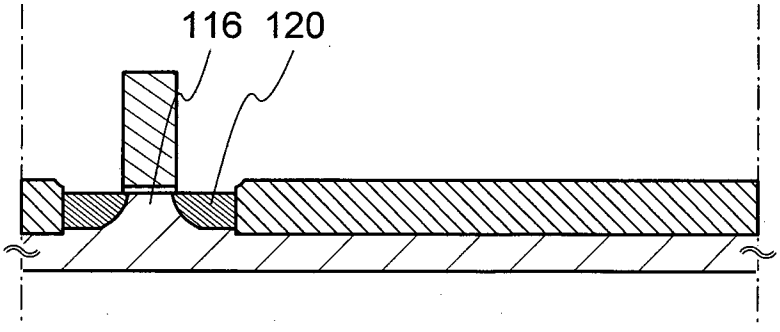


FIG. 3A

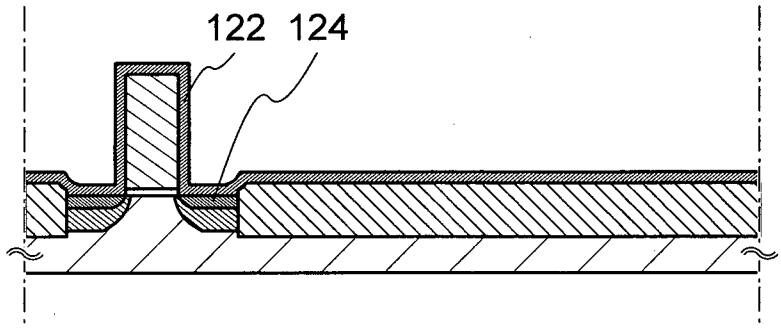


FIG. 3B

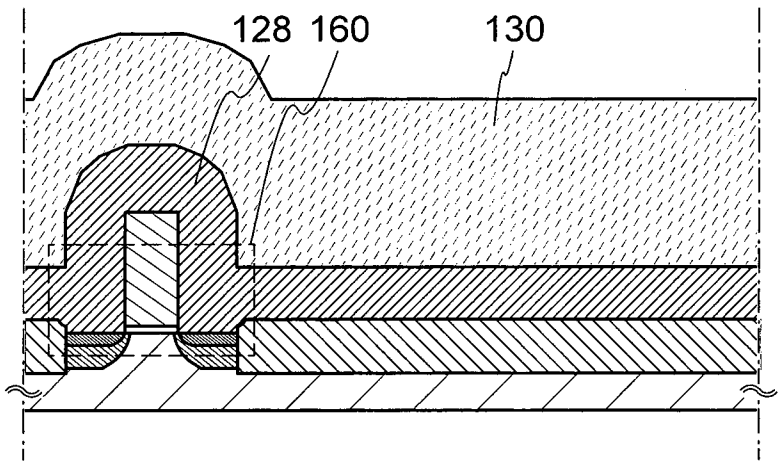


FIG. 3C

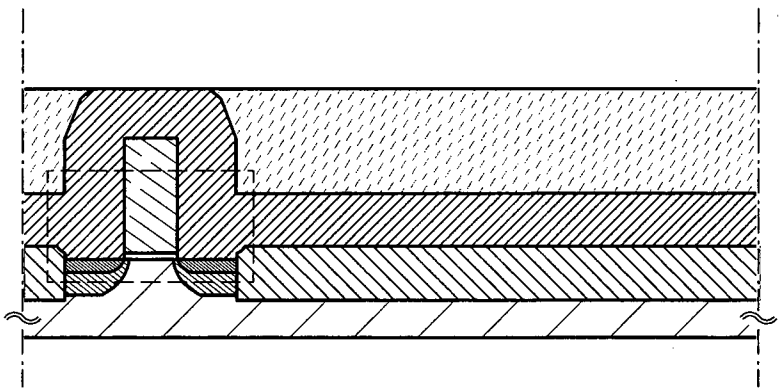


FIG. 4A

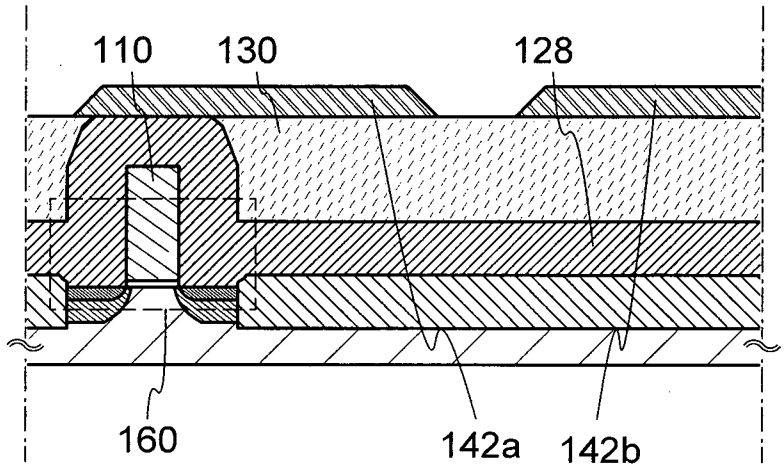


FIG. 4B

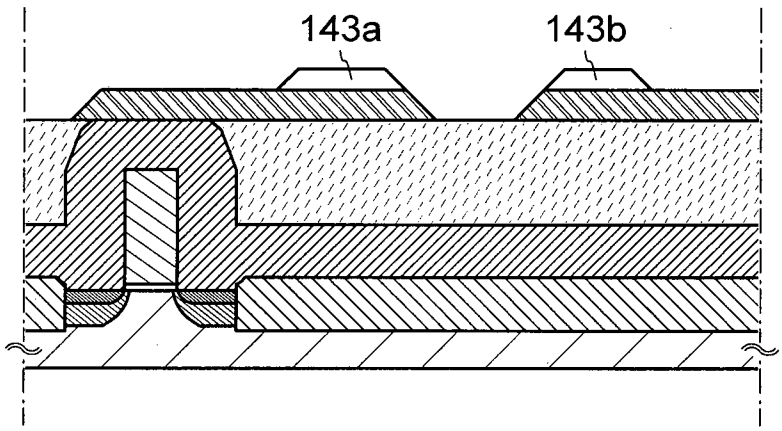


FIG. 4C

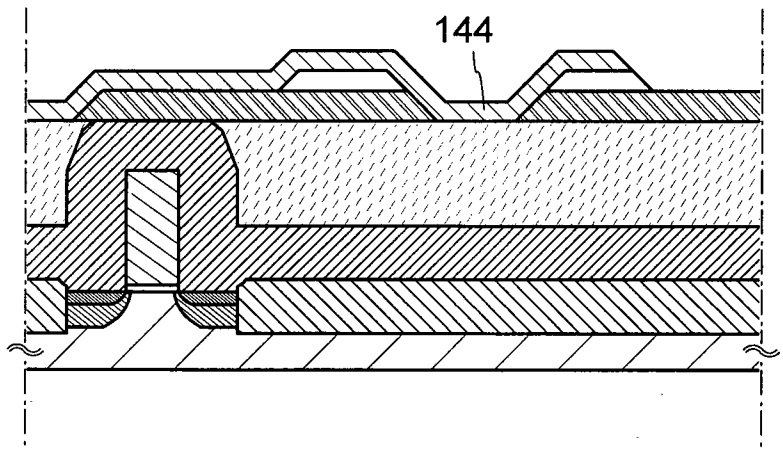


FIG. 5A

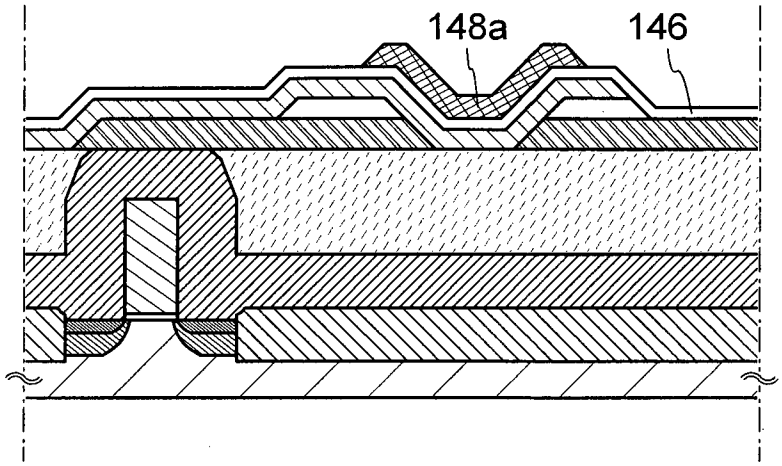


FIG. 5B

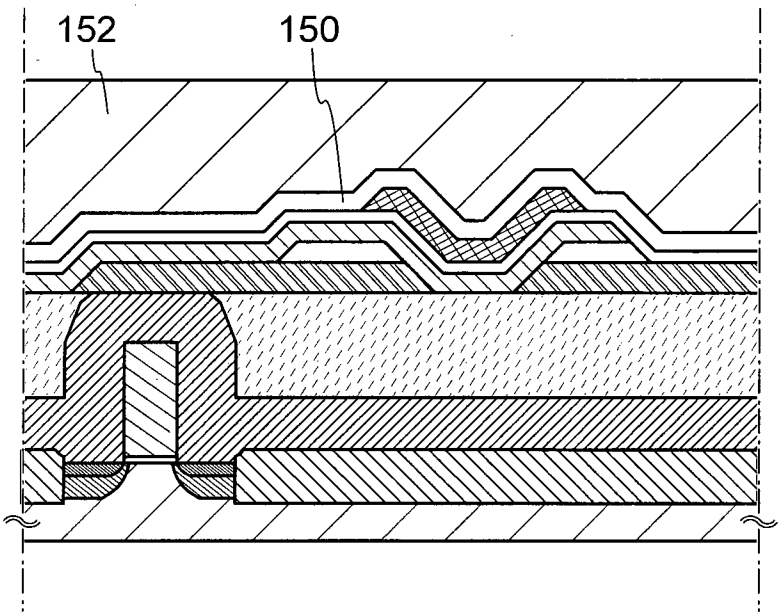


FIG. 5C

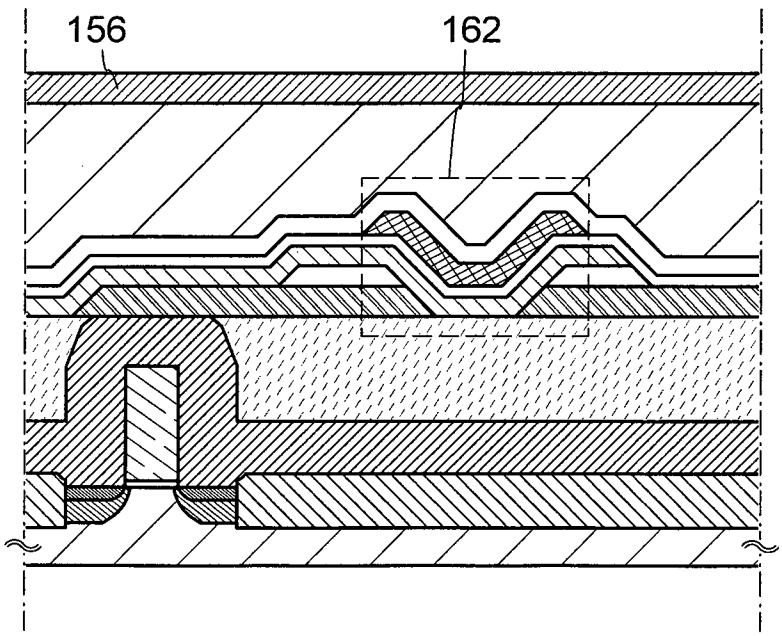


FIG. 6A

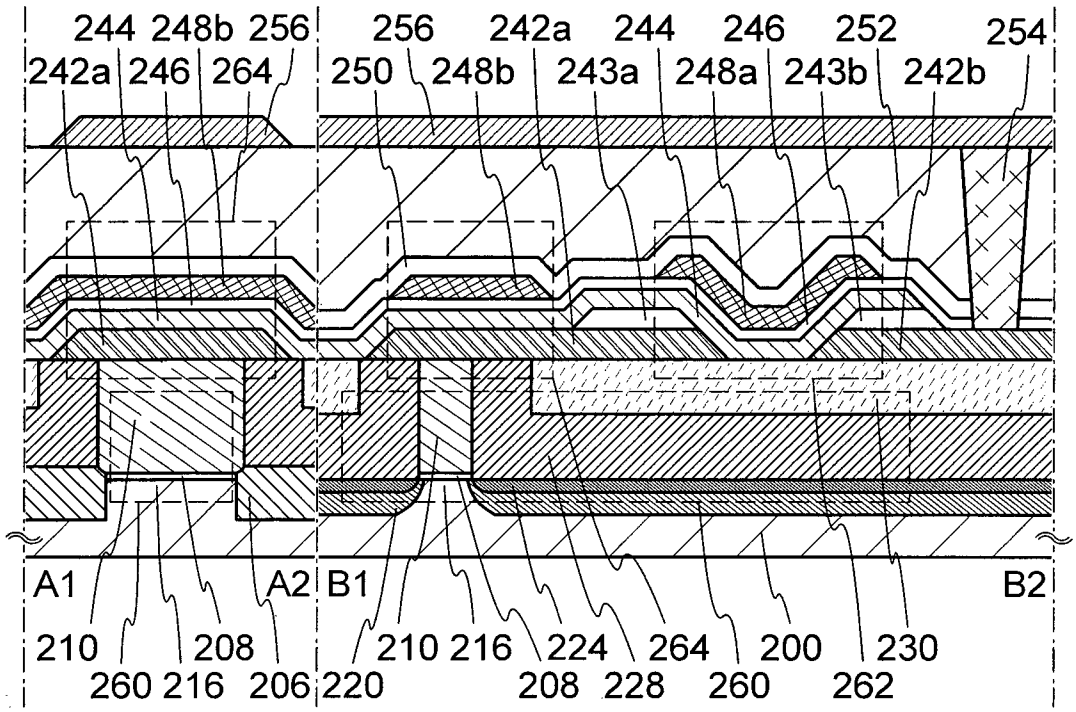

244
248b
256
242a
246
264
256
242a
244
246
252
254
250
248b
243a
248a
243b
242b
A1
A2
B1
B2
210
260
216
208
206
220
210
216
224
208
228
264
260
200
230
262

FIG. 6B

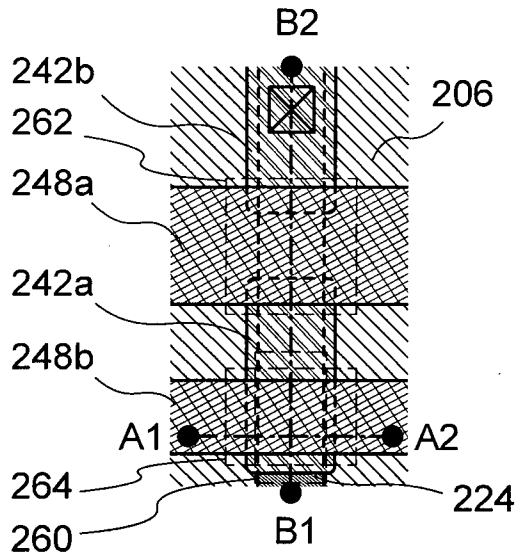

B2
242b
262
206
248a
242a
248b
A1
A2
264
260
224
B1

FIG. 7A

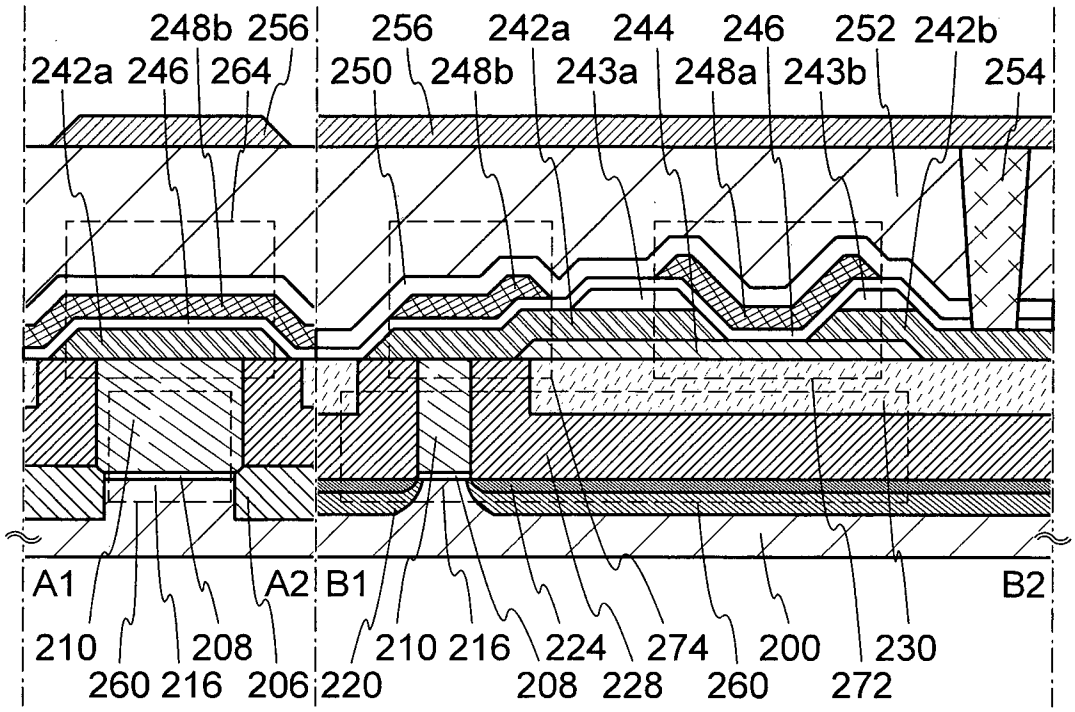

248b 256
242a 246 264
256
250 248b
242a
244
243a
246
248a
252
243b
242b
254
A1
A2
B1
B2
210
260
216
208
206
220
210
216
224
208
274
228
200
260
230
272

FIG. 7B

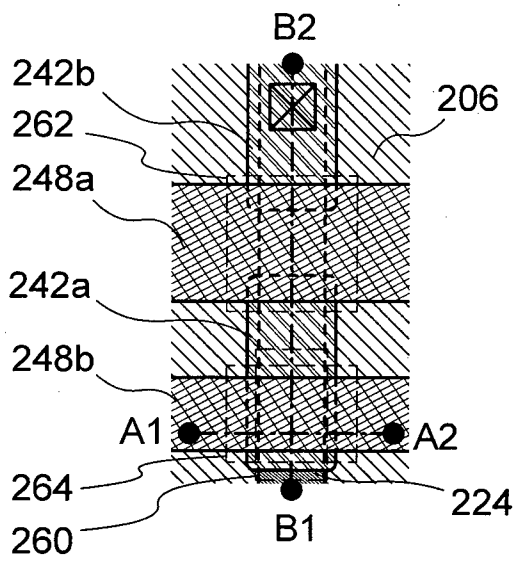

B2
242b
262
248a
242a
248b
A1
A2
264
260
B1
206
224

FIG. 8A

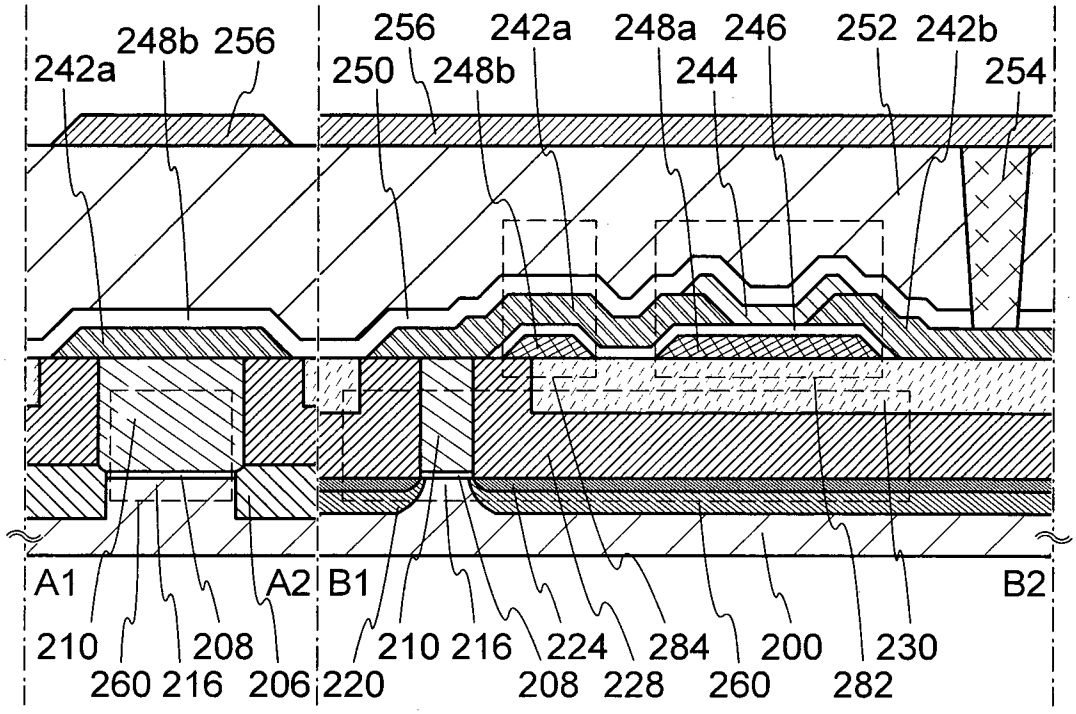

248b 256
242a
256
250
242a
248b
248a
246
244
252
242b
254
A1
A2
B1
B2
210
208
260
216
206
210
216
220
224
208
284
228
260
200
230
282

FIG. 8B

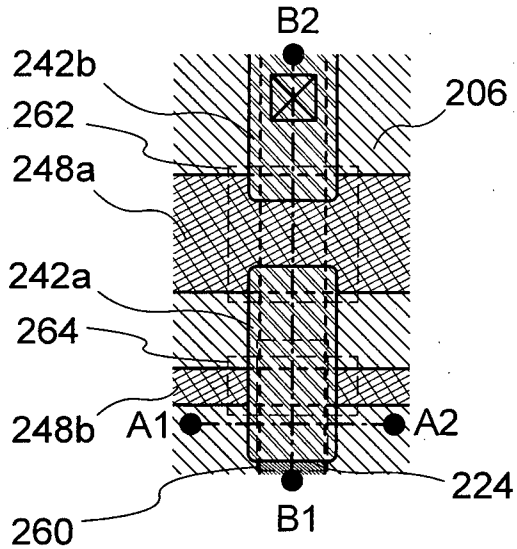

B2
242b
262
248a
242a
264
248b
A1
A2
206
224
260
B1

FIG. 9A

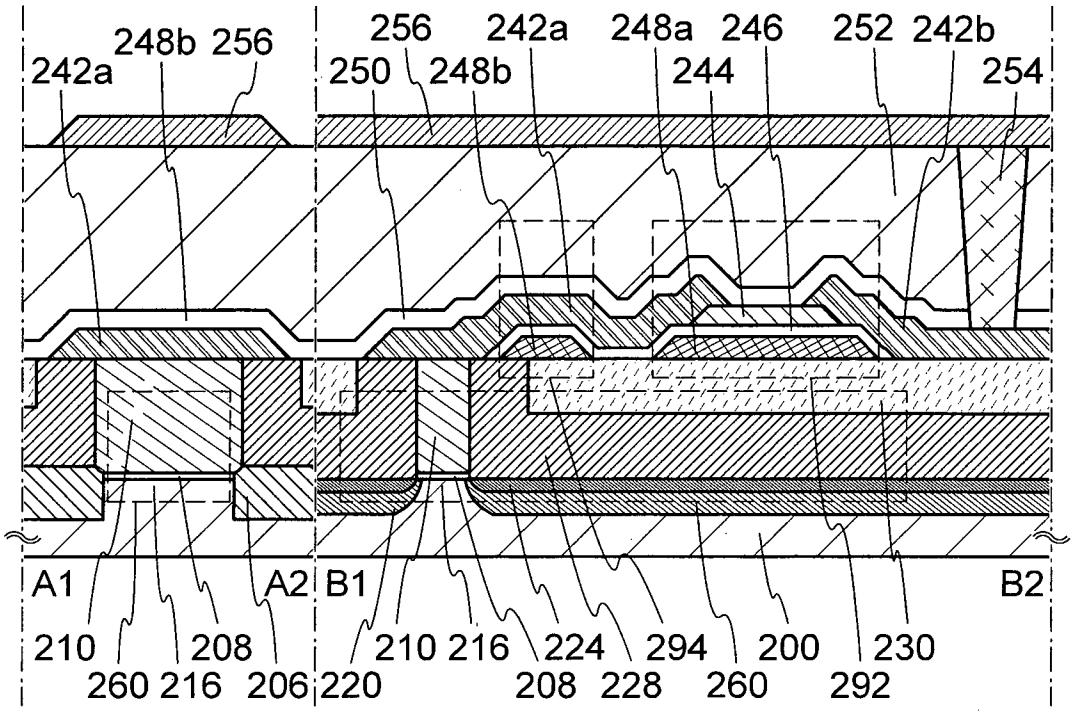

248b 256
242a
256 242a 248a 246 252 242b
250 248b 244 254
A1 A2 B1 B2
210 260 216 208 206
210 216 220 224 208 294 228 200 260 230 292

FIG. 9B

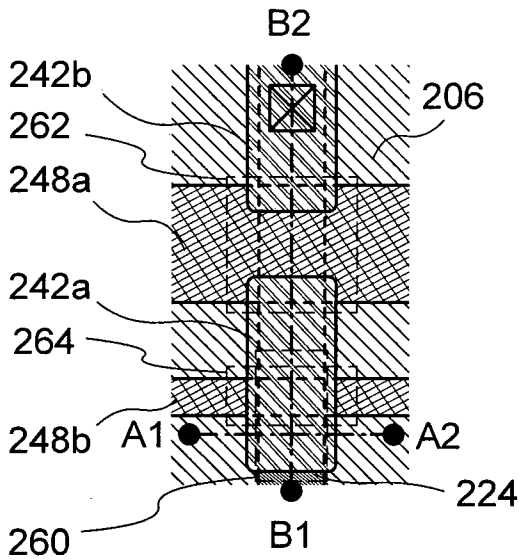

B2
242b
262
248a
242a
264
248b
A1
A2
206
224
260
B1

FIG. 10A

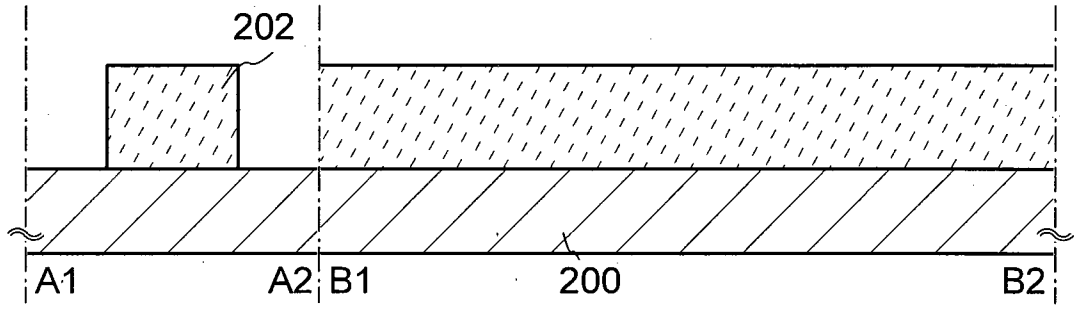


FIG. 10B

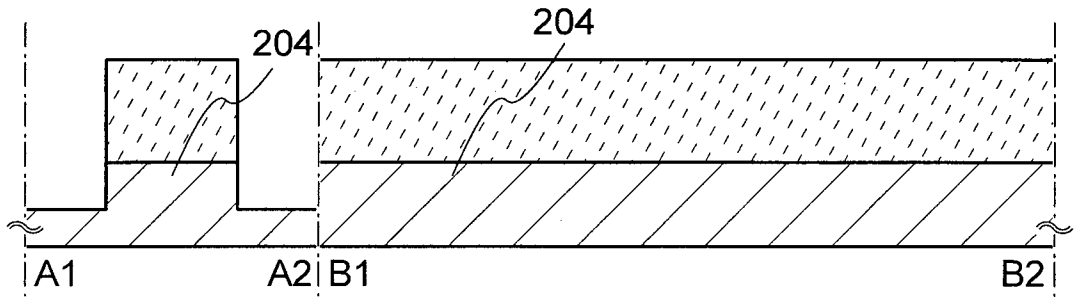


FIG. 10C

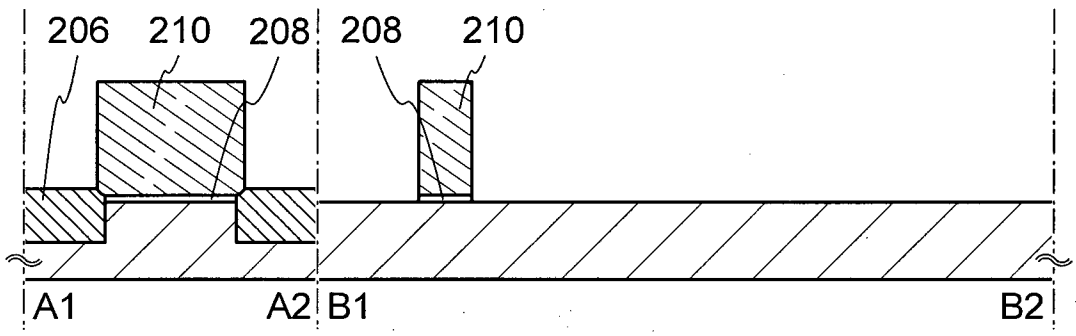


FIG. 10D

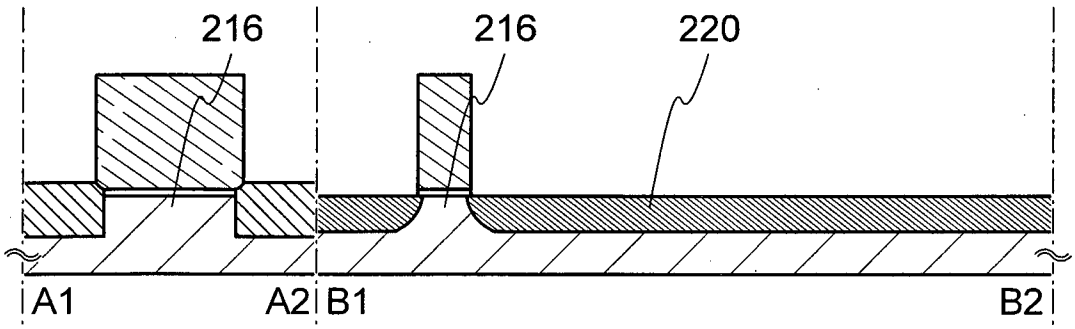


FIG. 11A

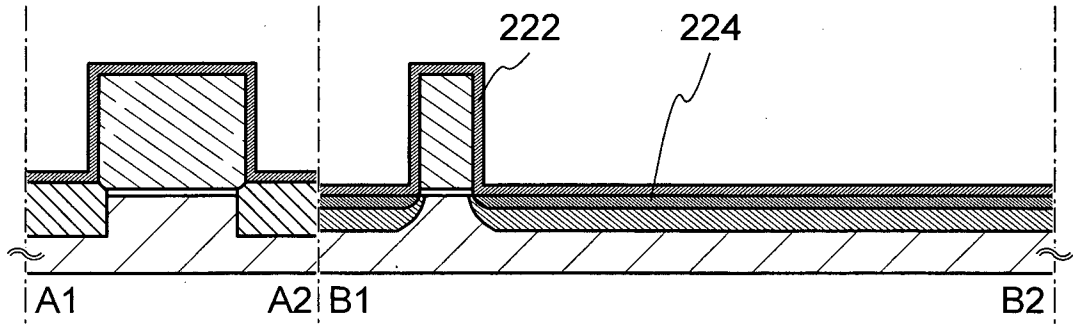


FIG. 11B

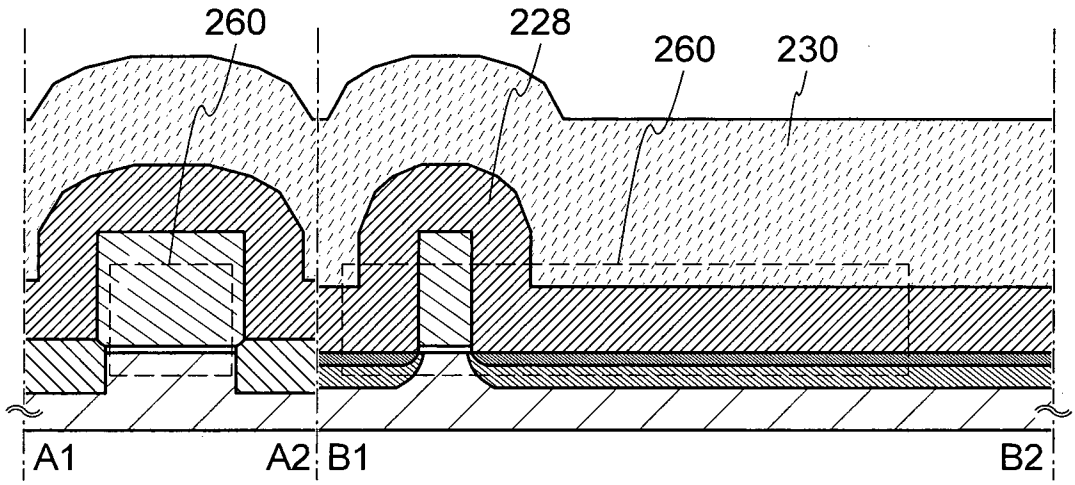


FIG. 11C

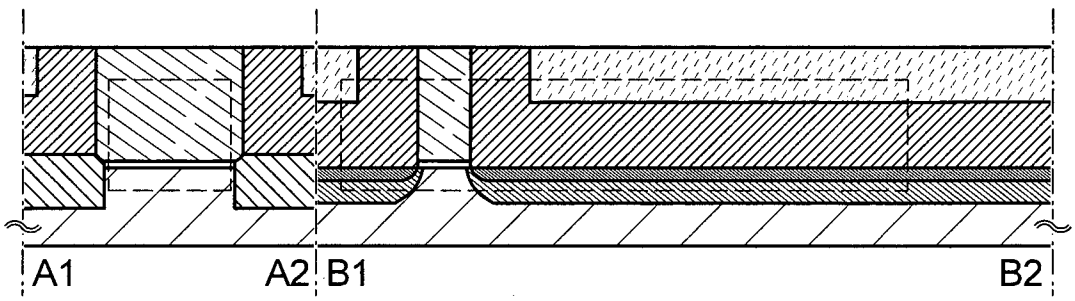


FIG. 12A

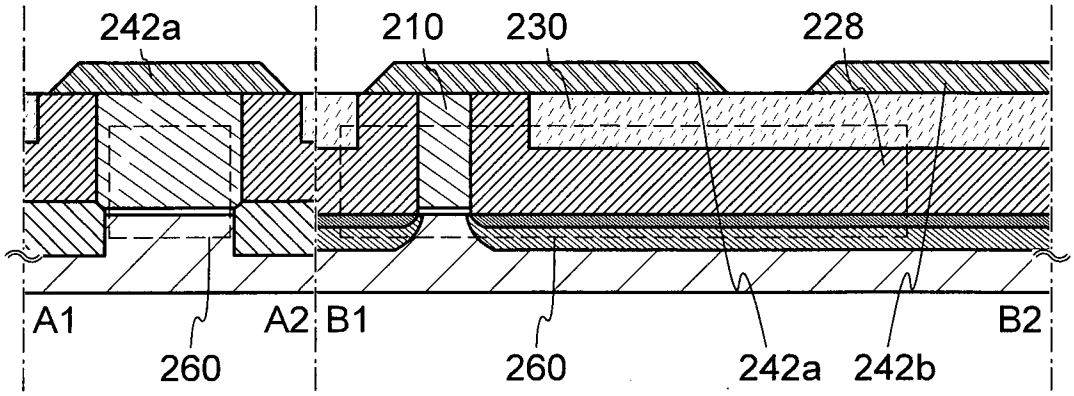


FIG. 12B

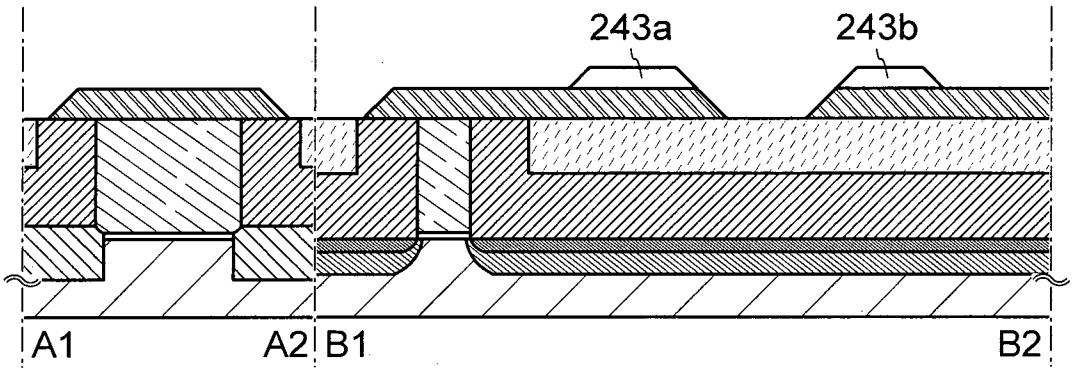


FIG. 12C

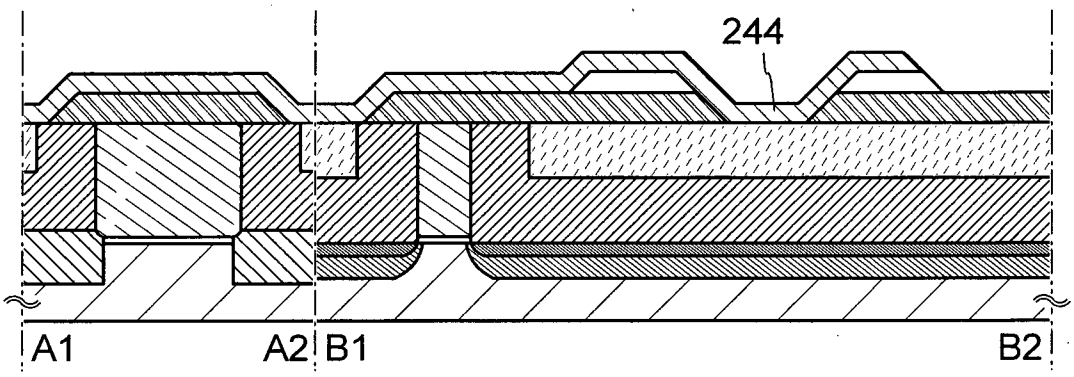


FIG. 12D

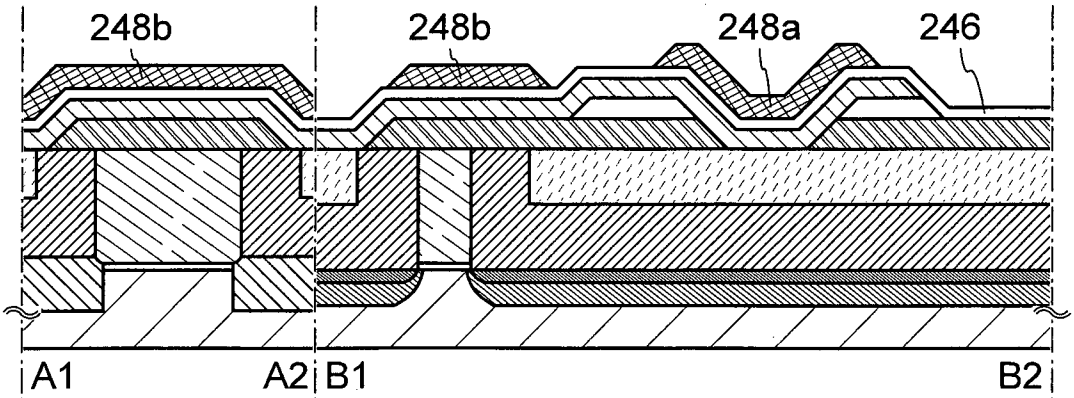


FIG. 13A

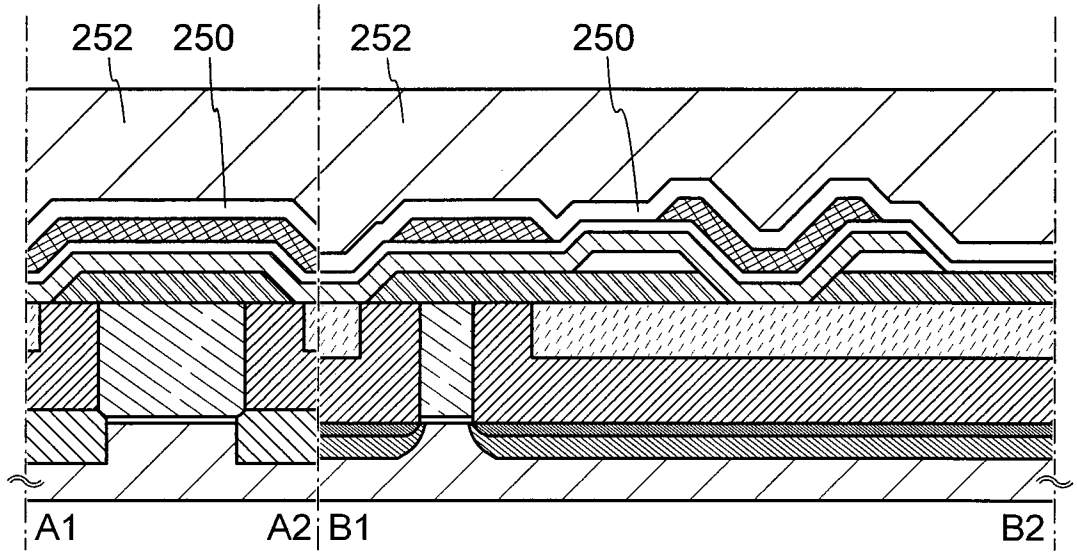


FIG. 13B

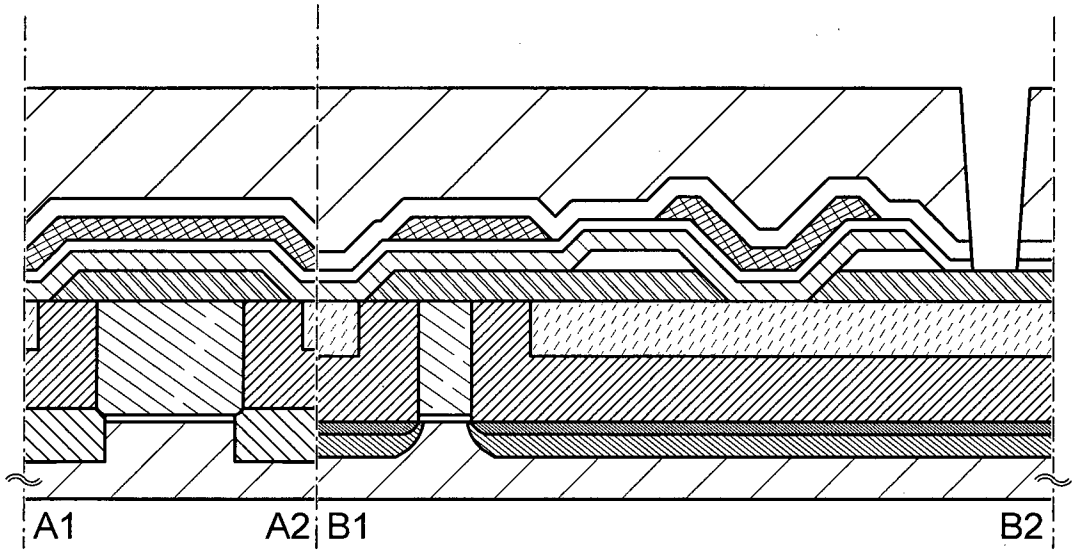


FIG. 13C

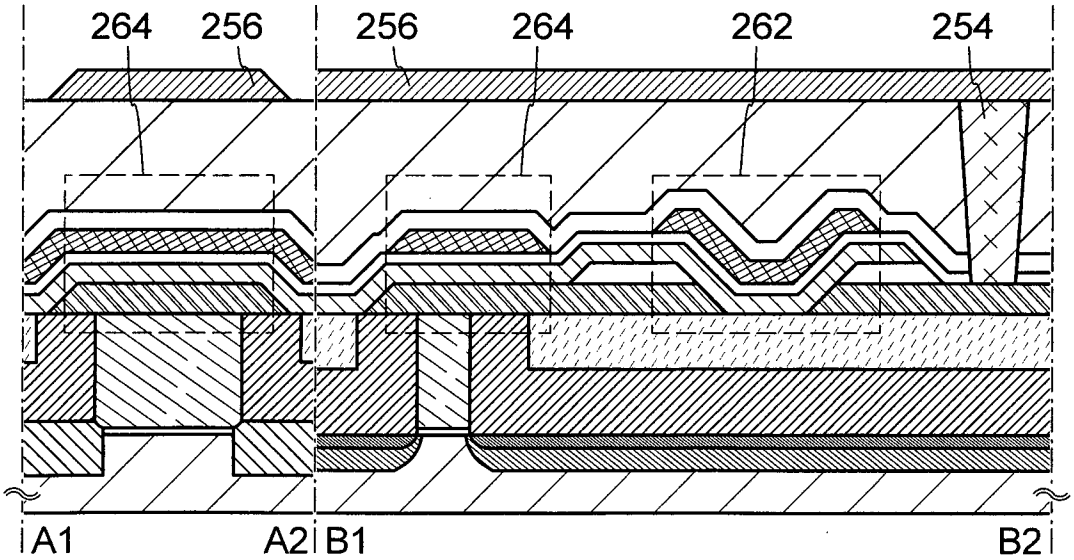


FIG. 14A

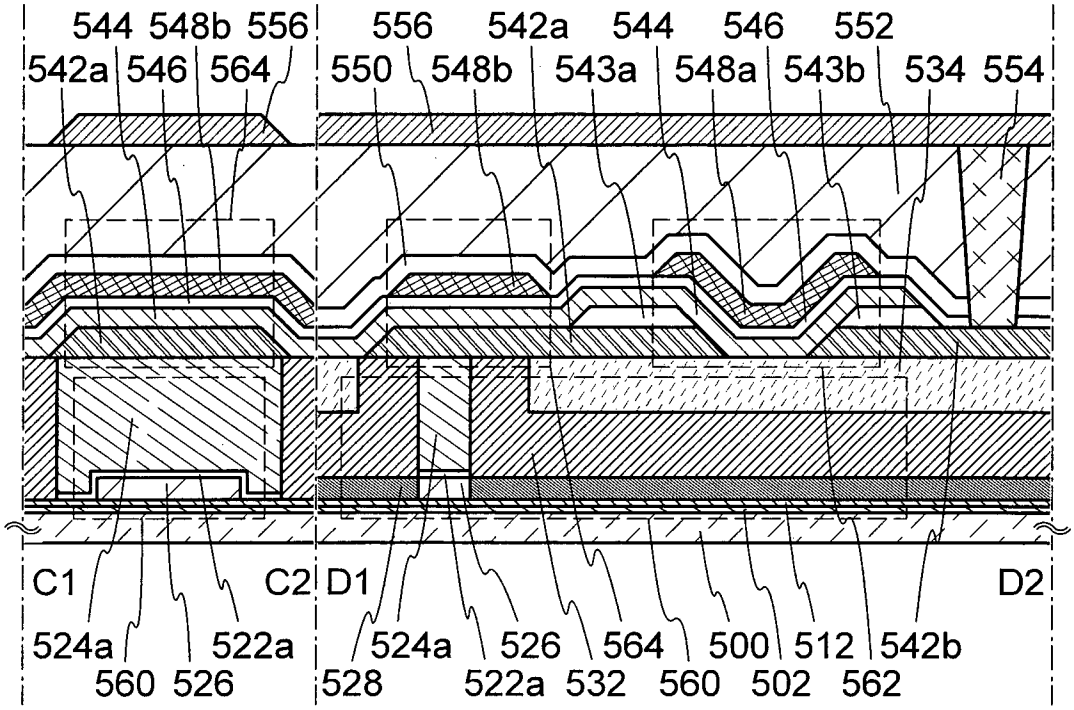


FIG. 14B

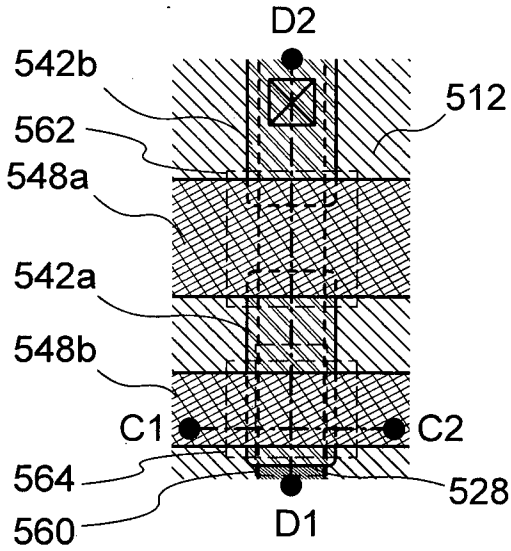


FIG. 15A

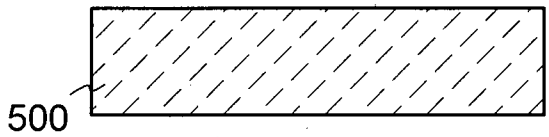


FIG. 15B

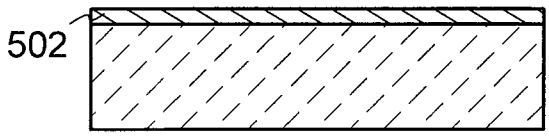


FIG. 15C

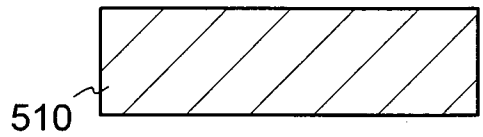


FIG. 15D

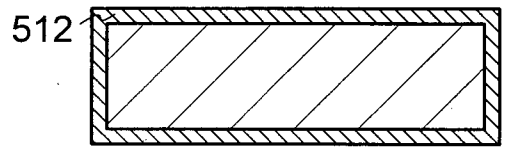


FIG. 15E

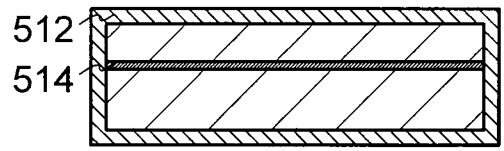


FIG. 15F

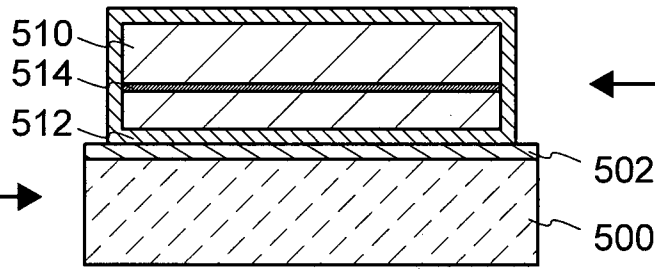


FIG. 15G

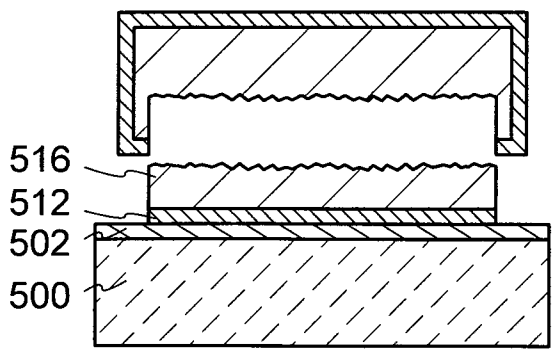


FIG. 15H

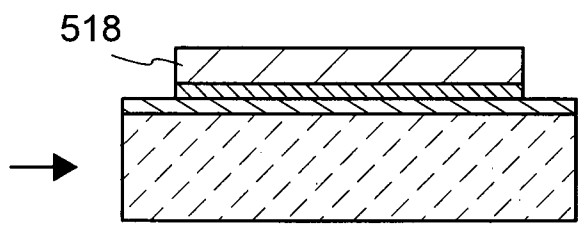


FIG. 16A

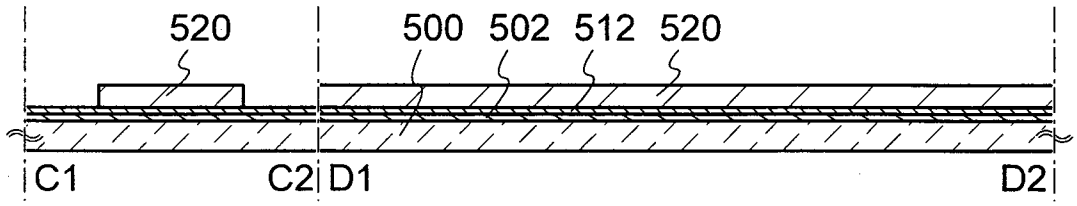


FIG. 16B

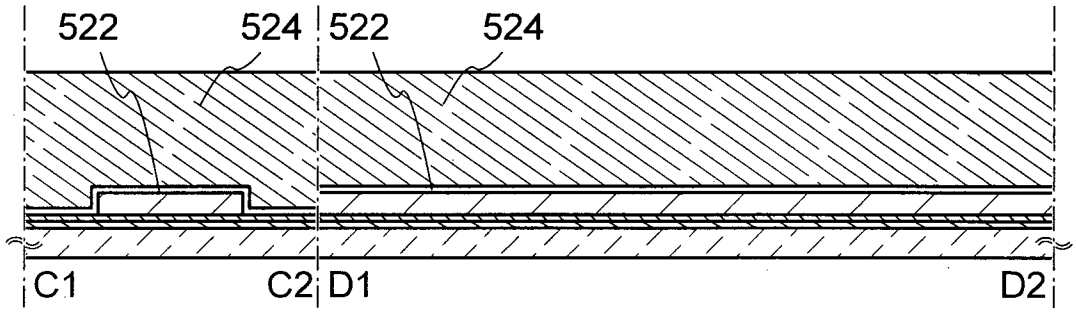


FIG. 16C

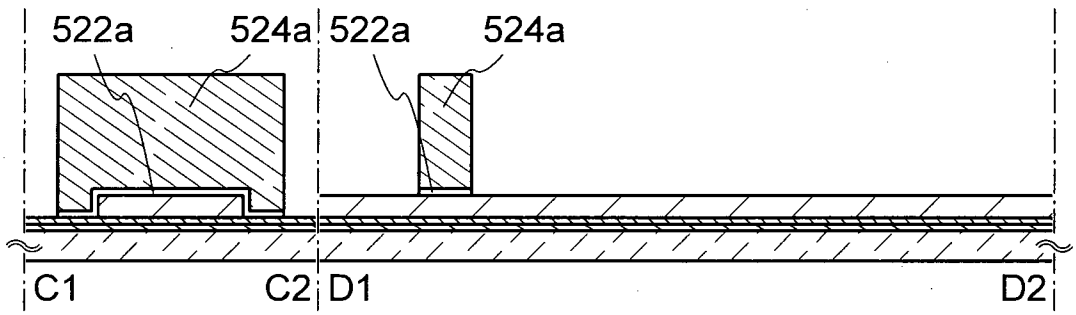


FIG. 16D

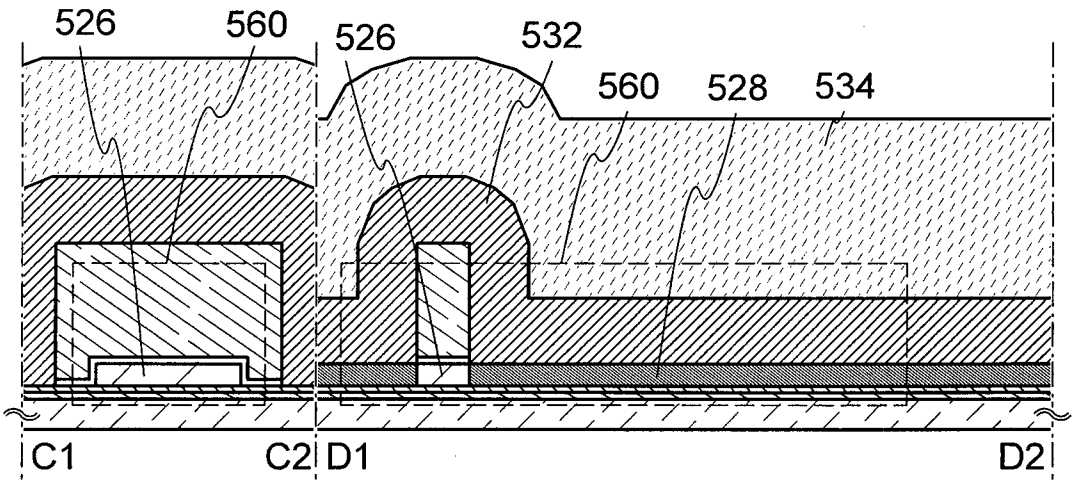


FIG. 16E

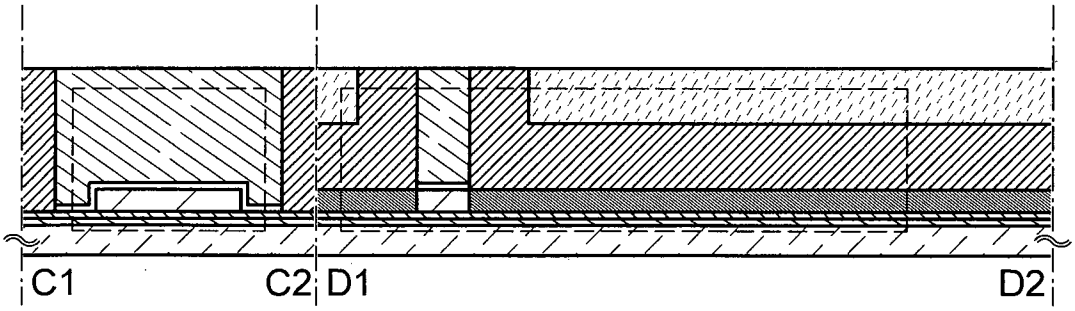


FIG. 17A-1

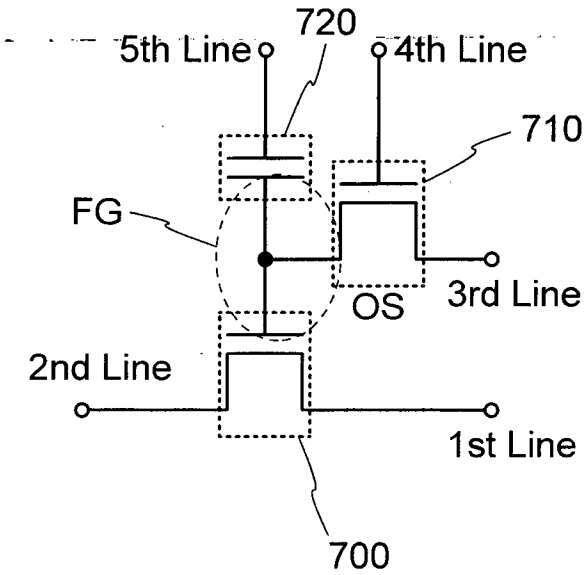


FIG. 17B

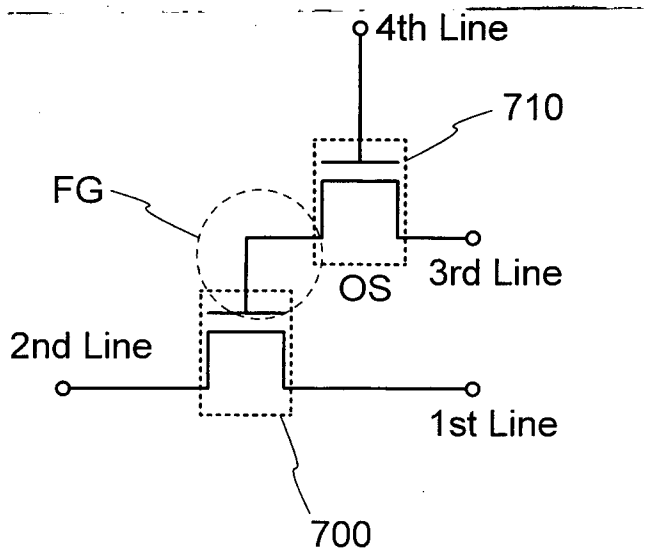


FIG. 17A-2

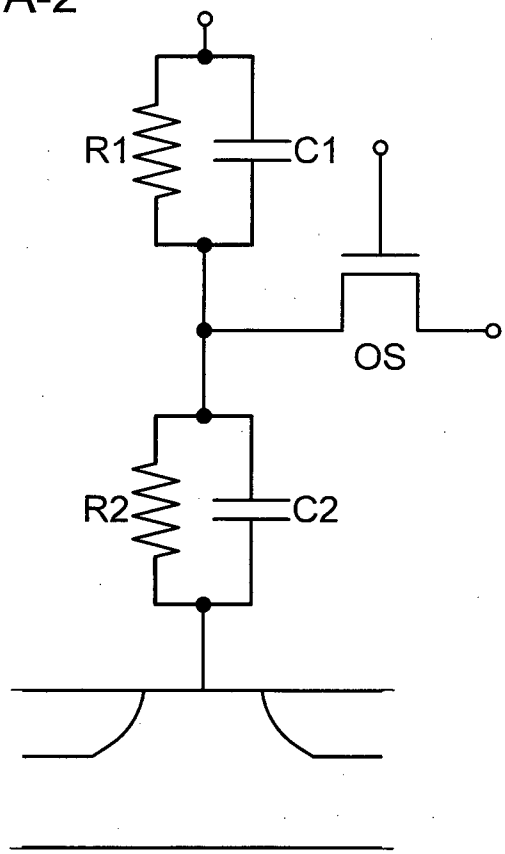


FIG. 18A

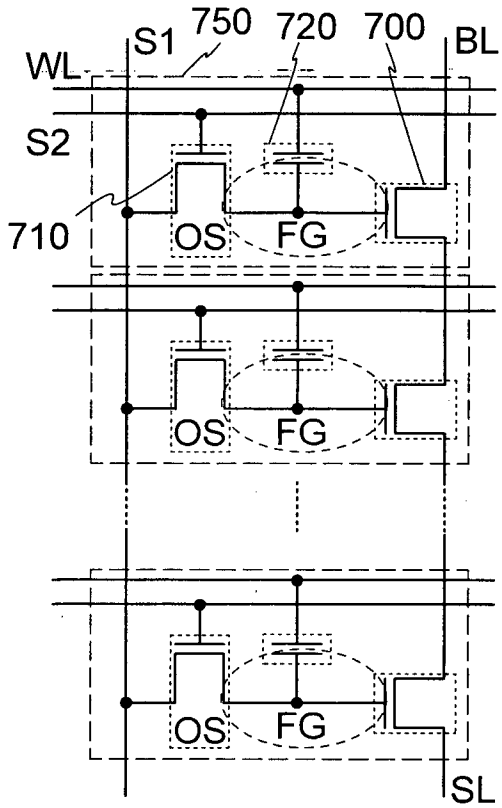


FIG. 18B

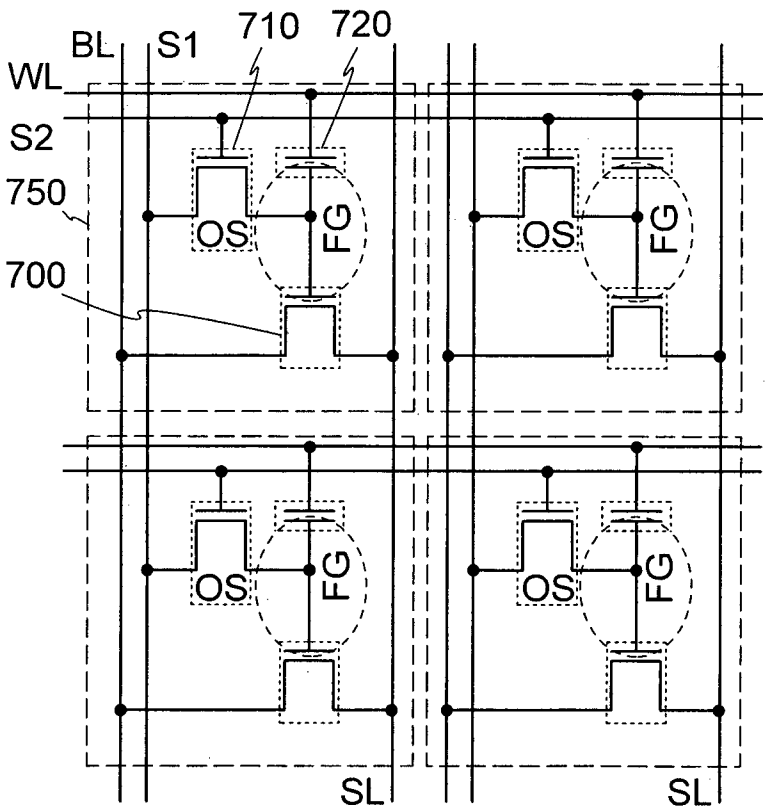


FIG. 19A

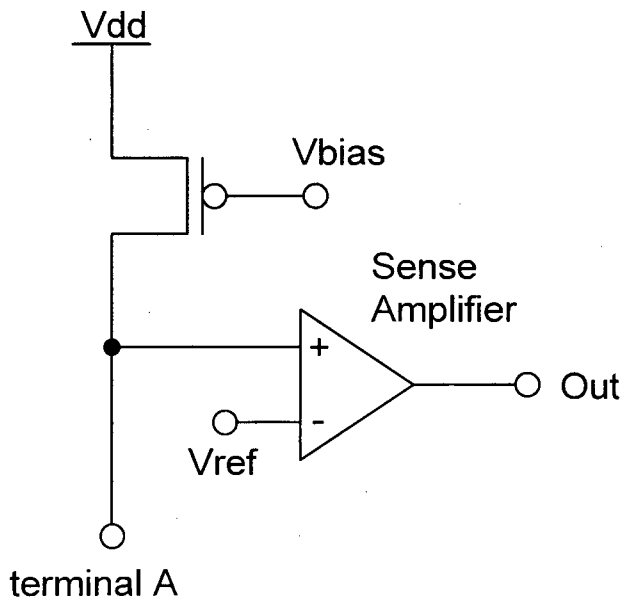


FIG. 19B

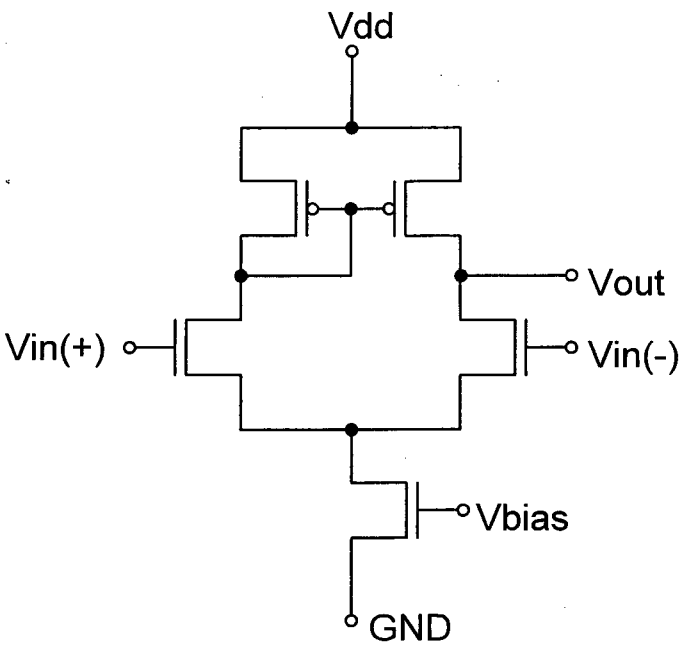


FIG. 19C

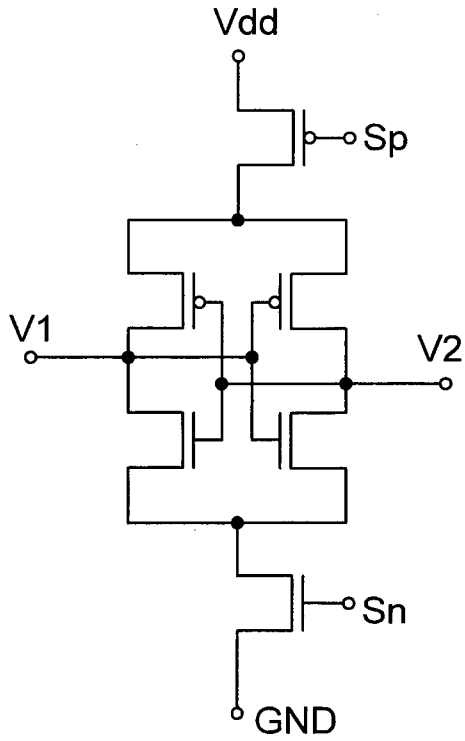


FIG. 20A

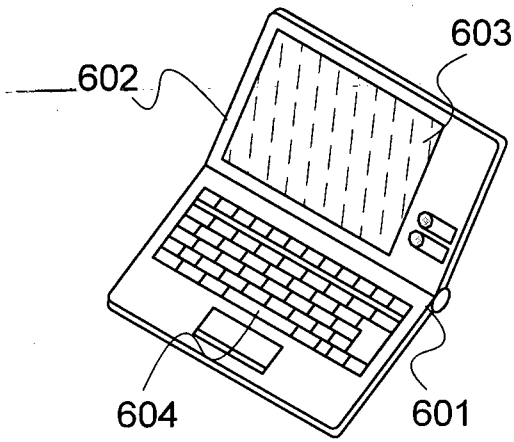


FIG. 20B

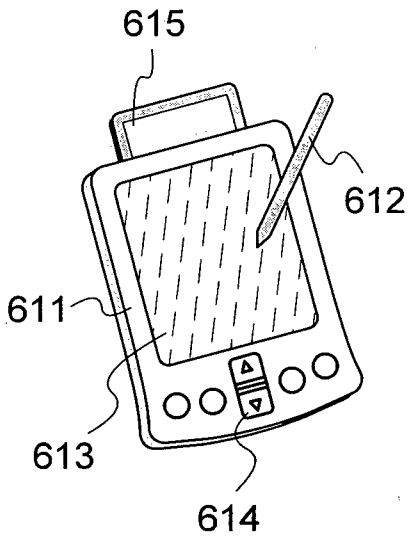


FIG. 20C

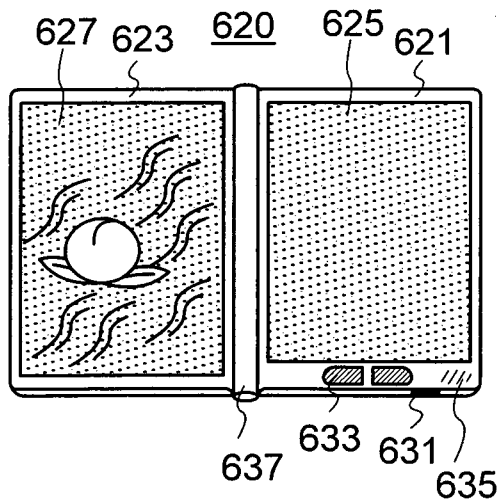


FIG. 20D

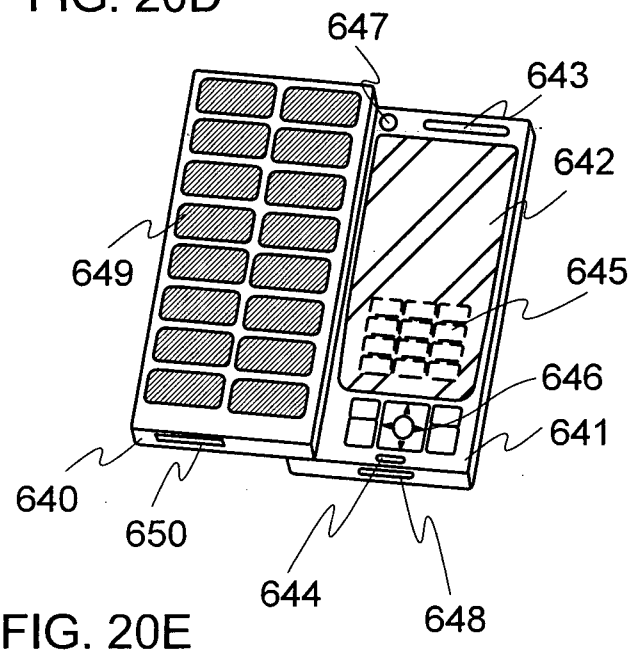


FIG. 20E

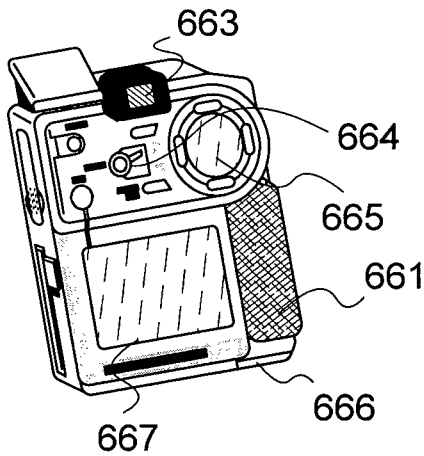


FIG. 20F

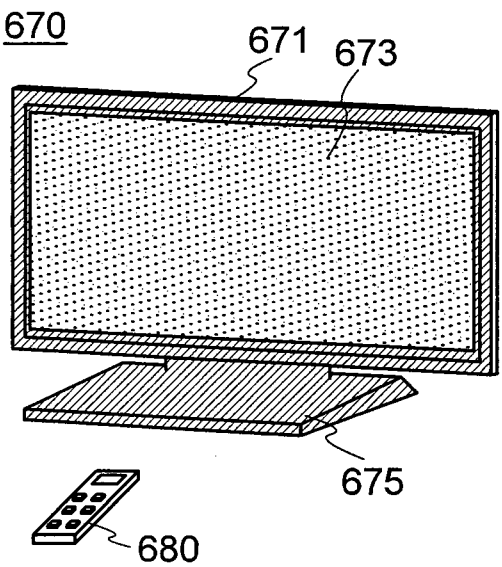


FIG. 21

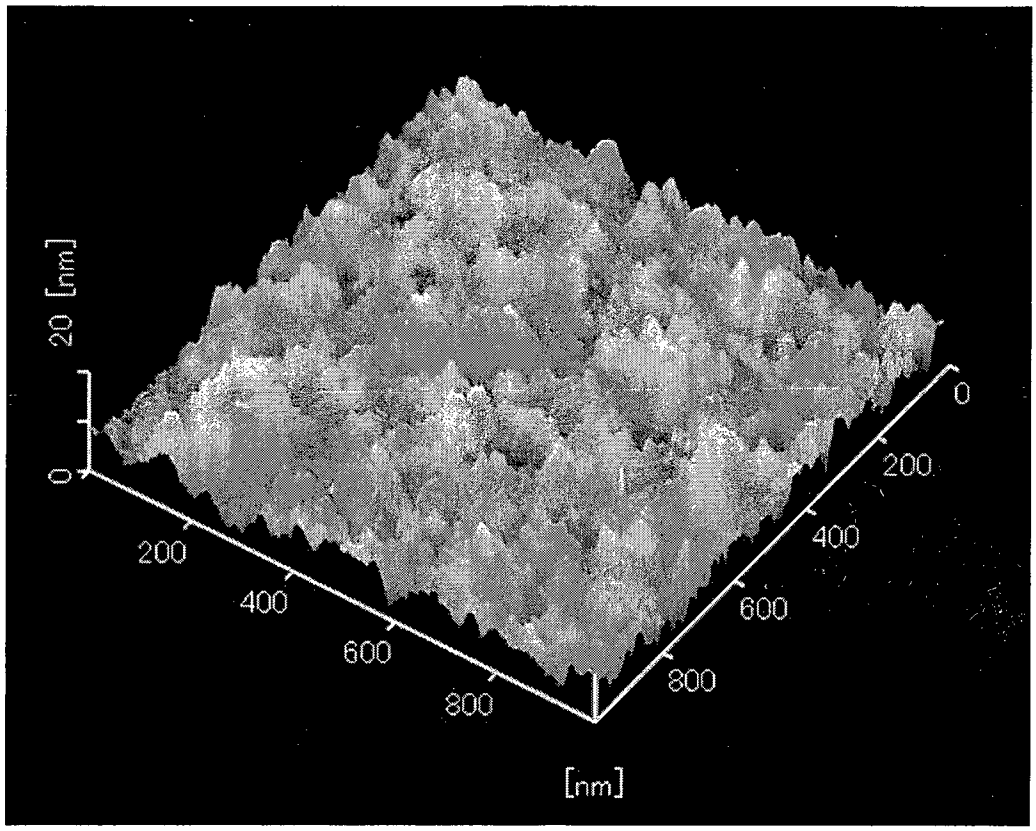
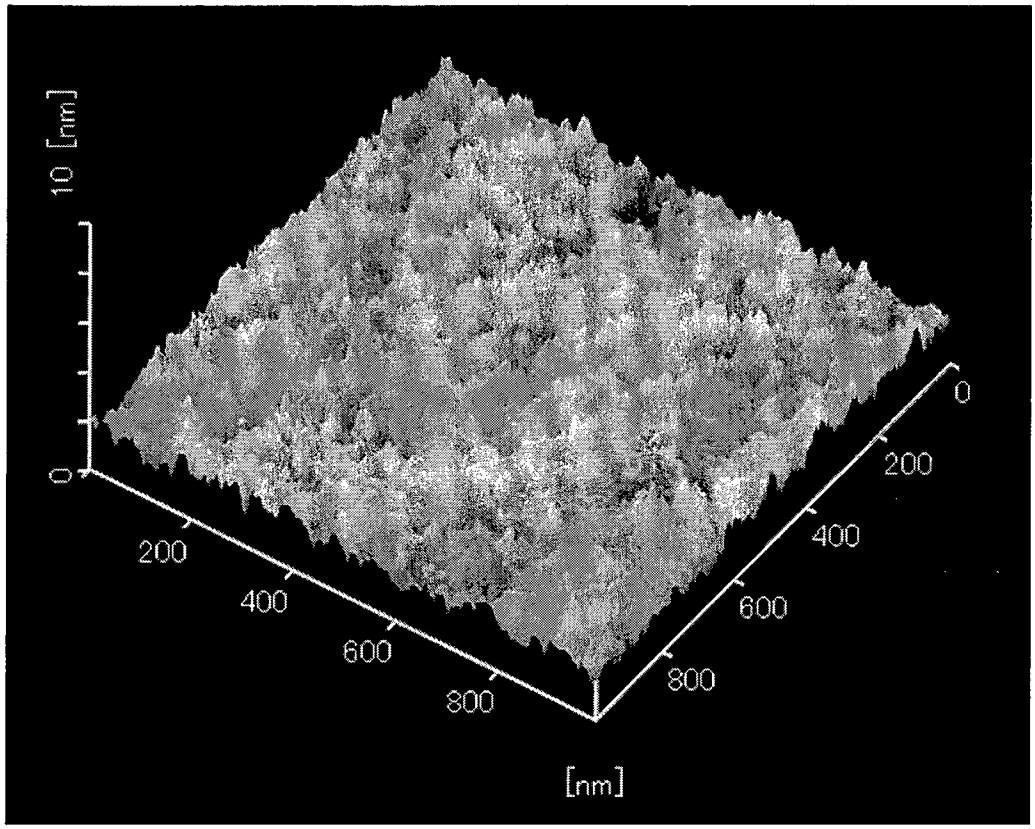


FIG. 22



[EXPLANATION OF REFERENCES]

100: substrate; 102: protective layer; 104: semiconductor region; 106: element isolation insulating layer; 108: gate insulating layer; 110: gate electrode; 116: channel formation region; 120: impurity region; 122: metal layer; 124: metal compound region; 128: insulating layer; 130: insulating layer; 142a: source electrode or drain electrode; 142b: source electrode or drain electrode; 144: oxide semiconductor layer; 143a: insulating layer; 143b: insulating layer; 146: gate insulating layer; 148a: gate electrode; 150: insulating layer; 152: insulating layer; 156: wiring; 160: transistor; 162: transistor; 200: substrate; 202: protective layer; 204: semiconductor region; 206: element isolation insulating layer; 208: gate insulating layer; 210: gate electrode; 216: channel formation region; 220: impurity region; 222: metal layer; 224: metal compound region; 228: insulating layer; 230: insulating layer; 242a: source electrode or drain electrode; 242b: source electrode or drain electrode; 244: oxide semiconductor layer; 243a: insulating layer; 243b: insulating layer; 246: gate insulating layer; 248a: gate electrode; 248b: electrode; 250: insulating layer; 252: insulating layer; 254: electrode; 256: wiring; 260: transistor; 262: transistor; 264: capacitor; 272: transistor; 274: capacitor; 282: transistor; 284: capacitor; 292: transistor; 294: capacitor; 500: base substrate; 502: nitrogen-containing layer; 510: single crystal semiconductor substrate; 512: oxide film; 514: embrittled region; 516: single crystal semiconductor layer ; 518: single crystal semiconductor layer; 520: semiconductor layer; 522: insulating layer; 522a: gate insulating layer; 524: conductive layer; 524a: gate electrode; 526: channel formation region; 528: impurity region; 532: insulating layer; 534: insulating layer; 542a: source electrode or drain electrode; 542b: source electrode or drain electrode; 543a: insulating layer; 543b: insulating layer; 544: oxide semiconductor layer; 546: gate insulating layer; 548a: gate electrode; 548b: electrode; 550: insulating layer; 552: insulating layer; 554: electrode; 556: wiring; 560: transistor; 562: transistor; 564: capacitor; 601: housing; 602: housing; 603: display portion; 604: keyboard; 611: main body; 612: stylus; 613: display portion; 614: operation button; 615: external interface; 620: electronic book reader; 621: housing; 623: housing; 625: display portion; 627: display portion; 631: power button; 633: operation key; 635: speaker; 637: hinge; 640: housing; 641: housing; 642: display panel; 643: speaker; 644: microphone; 645: operation key; 646: pointing device; 647: camera lens; 648: external connection terminal; 649: solar cell ; 650: memory slot; 661: main body; 663: eyepiece portion; 664: operation switch; 665: display portion; 666: battery; 667: display portion; 670: television device; 671: housing; 673: display portion; 675: stand; 680: remote controller ; 700: transistor; 710: transistor; 720: capacitor; 750: memory cell.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/050791

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. See extra sheet

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 63-40343 A (Fujitsu Limited) 1988.02.20, Fig.3 (No Family)	1-22
Y	JP 2007-220816 A (Kochi Industrial Promotion Center) 2007.08.30, Whole document (No Family)	1-22
Y	JP 07-193188 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 1995.07.28, Par. No.【0008】 (No Family)	1-22
Y	JP 2009-141342 A (FUJIFILM CORPORATION) 2009.06.25, Whole document & US 2009/0127551 A1,Whole document & EP 2061087 A2 & KR 10-2009-0050971 A	1-14

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30.03.2011	12.04.2011

Name and mailing address of the ISA/JP
Japan Patent Office
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer
Tsutomu Utagawa
4L 3125
Telephone No. +81-3-3581-1101 Ext. 3498

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/050791

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 09-283751 A (Kabushiki Kaisha Toshiba) 1997.10.31, Fig.1-3 & US 6018195 A, Fig.1-3 & KR 10-0243936 B	2,3,8,11-14, 16,19-22
Y	JP 10-209389 A (Samsung Electronics Co.,Ltd.) 1998.08.07, Fig.1 & US 5940705 A,Fig.1 & KR 10-0219519 B1	2,11-14,19-22,
A	JP 11-233789 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 1999.08.27, Whole document (No Family)	1-22
A	JP 2001-230326 A (NEC CORPORATION) 2001.08.24, Whole document & US 2001/0015450 A1, Whole document	1-22
A	JP 2008-166802 A (Samsung Electronics Co.,Ltd.) 2008.07.17, Whole document & US 2008/0160726 A1,Whole document & DE 102007063551 A & KR 10-0829616 B1 & CN 101256960 A	1-22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/050791

CLASSIFICATION OF SUBJECT MATTER
H01L21/8234(2006.01)i, H01L21/02(2006.01)i, H01L21/336(2006.01)i,
H01L21/8242(2006.01)i, H01L21/8247(2006.01)i, H01L27/00(2006.01)i,
H01L27/06(2006.01)i, H01L27/088(2006.01)i, H01L27/10(2006.01)i,
H01L27/108(2006.01)i, H01L27/115(2006.01)i, H01L27/12(2006.01)i,
H01L29/786(2006.01)i, H01L29/788(2006.01)i, H01L29/792(2006.01)i

Minimum documentation searched

H01L21/8234, H01L21/02, H01L21/336, H01L21/8242, H01L21/8247, H01L27/00, H01L27/06, H01L27/088, H01L27/10, H01L27/108, H01L27/115, H01L27/12, H01L29/786, H01L29/788, H01L29/792