March 10, 1970 D. E. BUCHHOLZ ET AL 3,500,397

RAID ANALYSIS COMPUTER

Filed Sept. 16, 1968 2 Sheets-Sheet 1

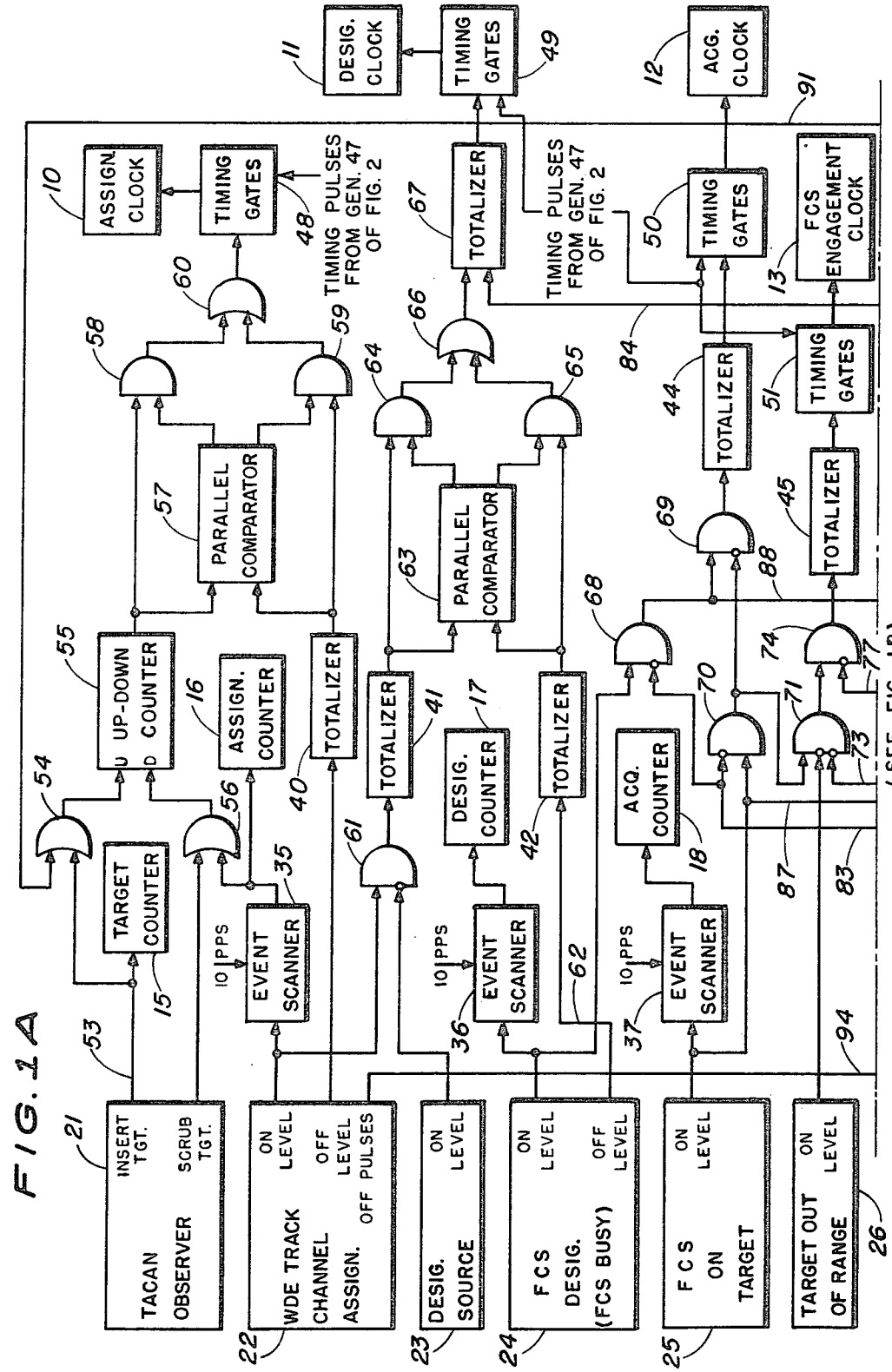


FIG. 1A

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RAID ANALYSIS COMPUTER

Filed Sept. 16, 1968 2 Sheets-Sheet 2

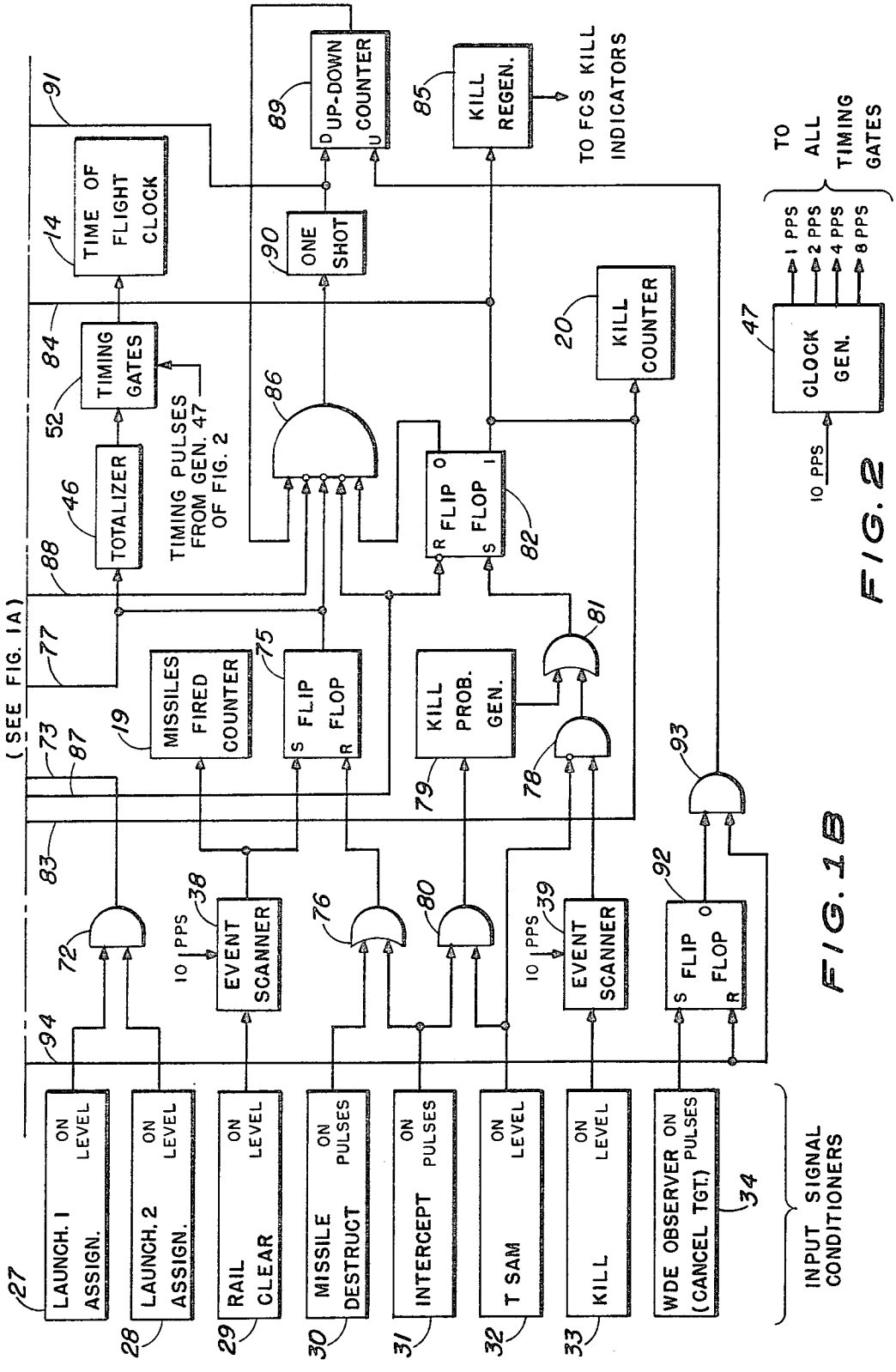


FIG. 2

FIG. 1B

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RAID ANALYSIS COMPUTER

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U.S. Cl. 343—7 8 Claims

ABSTRACT OF THE DISCLOSURE

The present invention relates to raid analysis computer circuitry capable of evaluating and providing an accurate indication of the effectiveness of a shipboard guided missile weapon system during an exercise, by measuring the time utilized by the individual elements of the shipboard weapon system, while engaging or processing attacking aircraft targets, and providing immediate readout of the results. More specifically, a plurality of counters totalize the number of occurrences of specific weapon system events; a plurality of clocks totalize the time between successive events; and, logic circuitry controls the clocks to run at a rate determined by a comparison between the number of system elements which are available for use at a particular time and the number of targets then being processed. Consequently, the clocks provide an accurate indication of the effectiveness of both the overall weapon system and its various sub-system elements.

BACKGROUND OF THE INVENTION

A weapon control system for a guided missile ship includes certain weapon direction equipment, known as WDE, and the fire control equipment. Generally speaking, the weapon direction equipment (WDE) provides the displays and control apparatus required for proper utilization of the ship's weapons, which utilization requires: full evaluation of targets; assignment of missile directors to the proper targets; proper selection of missiles and loading of launchers; tactical evaluation prior to firing; and finally, continued evaluation to ascertain that targets are effectively encountered and that target priorities remain as first evaluated. For these purposes, the weapon direction equipment (WDE) includes a plurality of tracking channels assignable to the various targets being encountered. On the other hand, the fire control equipment is subdivided into a plurality of fire control systems (FCS) which supply the basic intelligence and control functions for effective engagement of targets by the ship's weapons. For example, when controlling guided missiles, there is a need to solve the launcher and inflight guidance orders for the missile.

As additional background information, well-known to those skilled in the art, the normal cycle of operation for a shipboard guided missile control system, during an anti-aircraft warfare exercise, is as follows:

(1) The target reaches the search radar detection range;
(2) The target is detected;
(3) The target reaches the maximum display range for the weapons direction equipment;
(4) The target is entered into the weapons direction equipment by its assignment to a selected tracking channel;
(5) The target is designated to a fire control system;
(6) The target is acquired by the tracking radar of the fire control system;
(7) The target enters the missile engagement range, if not already engageable;
(8) A launcher is assigned;
(9) A missile is fired;
(10) The missile intercepts the target; and
(11) The director is assigned a new target.

DESCRIPTION OF THE INVENTION

It is proposed in accordance with the present invention to provide raid analysis computer apparatus capable of registering the times utilized by the individual elements of a shipboard guided missile weapon system, while engaging attacking aircraft, and providing immediate readout of the results. In this way, problem areas within the weapon system can be quickly identified so that better training of the personnel can be provided, for example, if necessary.

More specifically, it is proposed in accordance with the present invention to utilize counters (electronic or electromechanical) for totalizing the number of occurrences of predetermined weapon system events and pulse counting means or clocks which totalize time between successive system events to provide an accurate indication of the target processing effectiveness of the weapon system. These clocks are controlled, by suitable logic circuitry, in accordance with a comparison made by the circuitry between the number of system elements available for use at a particular time and the number of targets then being processed. In other words, the weapon system evaluation provided by the proposed apparatus takes into account whether or not a system element is busy; i.e. already processing a target, when a new target is ready to be processed. Although the apparatus of the present invention can be utilized during an actual aircraft attack, to score the effectiveness of the guided missile weapon system, the proposed apparatus may also be used during a training exercise, with friendly aircraft or where the targets are manually simulated.

In view of the foregoing, one object of the present invention is to provide apparatus for evaluating the target processing effectiveness of a shipboard weapon system.

A further object of the present invention is to provide apparatus for evaluating the effectiveness of a shipboard weapon system, for example, in accordance with the time required by the various system elements to process targets during an exercise, either actual or simulated.

A further object of the present invention is to provide apparatus for evaluating a shipboard guided missile weapon system, said evaluating apparatus containing timing means which provide an indication of the time elapsing between the processing of a target by the successive elements of the weapon system and wherein the timing means are controlled to operate at a rate determined by a comparison between the number of system elements which are available for use at a particular time and the number of targets then being processed by the over-all system, so as to provide an accurate indication of the weapon system effectiveness.

Other objects, purposes and characteristic features of the present invention will in part be pointed out as the description of the invention progresses and in part be obvious from the accompanying drawings wherein:

FIGS. 1A and 1B illustrate a simplified block diagram of one embodiment of the present invention; and

FIG. 2 illustrates a clock generator for generating certain timing pulses employed in the illustrated embodiment of FIGS. 1A and 1B.

With reference to FIGS. 1A and 1B of the drawings, the proposed raid analysis computer apparatus of the present invention includes: five clocks or timing pulse counters **10** through **14** which register the times between predetermined successive weapon system events; six event counters **15** through **20** each of which totalizes the number of occurrences of an associated weapon system event; and, logic circuitry which control the clocks to run or operate at a rate determined by a comparison between the number of the system elements which are available for use at a particular time and the number of targets then being processed by the system.

For example, in a typical aircraft attack, the engagement is started when the targets cross the maximum range for the weapon direction equipment (WDE) and are disclosed to the weapon system. The targets are then each assigned to a separate WDE tracking channel. In accordance with the present invention, the proposed raid analysis computer apparatus counts all of the targets within the maximum WDE range (on counter **15**) and continuously compare this count with the number of WDE tracking channels available for use. The lesser number (channels or targets) determines the counting rate of the clock which indicates the total elapsed time between target disclosure and tracking channel assignment. In FIG. 1A, this clock is referred to as the assignment clock and is designated by the reference character **10**. The counting rate of the assignment clock **10** is thus greatest when all channels are unassigned and at least as many targets are awaiting assignments. As will be described in more detail hereinafter, similar logic processes are used to control: the designation clock **11** which provides an indication of the cumulative time required for designation of each WDE tracking channel to an appropriate fire control system; the acquisition clock **12** which indicates the time required for each fire control system to acquire a target after receiving a designation; the engagement clock **13** which provides an indication of the engagement time required by the assigned fire control system, from acquisition of the target until a missile is fired; and, the time of flight clock **14** which provides an indication of the total time of flight of each missile fired.

The proposed raid analysis computer apparatus of the present invention also includes a plurality of event counters **15** through **20**, in FIGS. 1A and 1B, which provide a total count of the occurrences of specified events within the weapon system operation. More specifically, the target counter **15** of FIG. 1A counts the total number of targets disclosed to the weapons direction equipment; the assignment counter **16** registers a count of the number of WDE tracking channels assigned; the designation counter **17** registers the number of target designations made to the fire control systems; the acquisition counter **18** registers the total number of target acquisitions made by the fire control systems; the missiles fired counter **19**, in FIG. 1B, registers a count of the number of actual or simulated missile firing; and the kill counter **20** registers a count of targets destroyed.

Thus, the raid analysis computer apparatus of the present invention is designed to register and provide a direct display of the number of selected weapon system events that occur during an anti-aircraft warfare exercise and a total time count, in seconds, of the time spent between consecutive events. This information is an indication of the quality of the weapon system performance during the engagement exercise. More specifically, for any given exercise, the following average time delays can be computed in accordance with the system event and time count registrations provided by the apparatus of the present invention:

$$t_0=\frac{\text{Accumulated time from the assigment clock 10}}{\text{Total number from assignment counter 16}}$$

$$t_1=\frac{\text{Accumulated time from the designation clock 11}}{\text{Total number from designation counter 17}}$$

$$t_2=\frac{\text{Accumulated time from acquisition clock 12}}{\text{Total number from acquisition counter 18}}$$

$$t_3=\frac{\text{Accumulated time from engagement clock 13}}{\text{Total number from missiles fired counter 19}}$$

The sum of these four times; i.e., $t_0+t_1+t_2+t_3$, is the average delay time from target entry into a WDE track channel until missile firing. Based upon the assumption there is a loss in system effectiveness due to excessive time delays and using n seconds as a norm for maximum

effectiveness, the following scoring system might, for example, be employed for any calculated average delay time:

$t_0+t_1+t_2+t_3$ (seconds):	Score (%)
Less than n	100
Less than 1.3 n	75
Less than 1.6 n	50
Less than 2.0 n	25
Greater than 2 n	0

As represented in FIGS. 1A and 1B of the drawings, at blocks **21** through **34**, fourteen distinct weapon system events (actual or simulated) are inputted to the raid analysis computer circuitry of the present invention, for the purpose of evaluating weapon system performance. More specifically, the various input events are in the form of DC relay control and switching signals which are applied to and conditioned by input signal conditioning circuits **21** through **26** of FIG. 1A and **27** through **34** of FIG. 1B.

These signals conditioning circuits **21** through **34** can be of any conventional design for converting the input relay control and switching signals to a level compatible with the integrated logic circuitry utilized in the raid analysis computer circuitry of the present invention. For example, if necessary to isolate the raid analysis computing circuitry ground from the weapons system DC power supply, the DC input voltage signals can be used to energize an oscillator (not shown) within each of the input signal conditioning circuits and whose output is transformer coupled to the remaining portion of the signal conditioning circuitry. Moreover, it may also be necessary that the DC voltage input signals be applied for a predetermined minimum of time and the oscillator output be rectified and integrated, in order to eliminate the effects of noise pulses, AC pickup, and/or relay bounce on the various counters **15** through **20** previously described. The various input signal conditioning circuits **21** through **34** might also contain, for example, level sensing circuitry which responds to the integrated oscillator signal and produces a step voltage with a very fast rise time, to demarcate the occurrence of each input system event.

Since the time interval between the input events within the weapons system can often occur faster than the maximum counting rate of mechanical counters, if these are used in the proposed raid analysis computer, it is preferable to provide certain event scanners **35**, **36** and **37** (FIG. 1A) and **38** and **39** (FIG. 1B). Each of these event scanners produces a train of output pulses numerically equal to the number of times that the associated event has occurred within the weapon system. For example, each of the event scanners **35** through **39** might include flip-flop circuits which are set by the event voltage steps, from the input signal conditioners, and whose outputs are gated sequentially by a 10 pulse per second clock frequency. Each time a flip-flop circuit has been set, a pulse is produced which drives or advances the connected counter and then resets the flip-flop circuit.

The illustrated raid analysis computing apparatus of the present invention also includes a plurality of totalizer circuits **40** through **45** in FIG. 1A and **46** in FIG. 1B which derive binary numbers equal to the total number of associated event occurrences. For example, these totalizer circuits might include decimal to binary converter logic circuitry comprised of half-adder circuits and OR gates, well-known to those skilled in the art.

Moreover, and as mentioned previously when discussing the event scanners, the illustrated raid analysis computing apparatus utilizes a clock rate or frequency of 10 pulse per second which may either be generated internally or be provided by an external source. As shown in FIG. 2, this basic clock rate is applied to a combination divider-counter circuit designated as clock generator **47** which, by means of gating, provides timing pulse out-

puts of 1, 2, 4, and 8 pulses per second. These timing pulse outputs are, in turn, applied to timing gate circuits **48** through **51** of FIG. 1A and **52** of FIG. 1B which generate pulse rates, variable from 0 to 8 pulses per second, as selected by and numerically equal to an input binary number applied to the timing gates. These output pulses from the timing gates **48** through **52** are then applied to and control the various clocks or time counter circuits **10** through **14** in FIGS. 1A and 1B.

ASSIGNMENT LOGIC

To start the raid analysis problem, each raid aircraft participating in the exercise, for example, periodically reports (to the exercise referee or supervisor) its position relative to the exercise ship at prescribed intervals. As each aircraft crosses the WDE maximum display range, or a range calculated to be detectable by the search radar if it is less than the WDE maximum range, a target insertion switch is operated manually by an observer stationed at the ship's TACAN equipment. This switch closure is represented in FIG. 1A at the signal conditioner circuit **21** and causes a voltage signal to appear on line **53**, to operate the counter **15** which maintains a cumulative count of the number of targets inserted. Also, this switch closure is effective, via OR gate **54**, to start the timing sequence for the illustrated raid analysis computing apparatus, by increasing the count of an up-down binary counter **55** used in monitoring the time required for WDE tracking channel assignment. More specifically, the assignment time count registered by clock **10** is defined as:

> The time spent by the ship (for equipment and/or operator response) for each target inserted which has not been assigned to a WDE tracking channel. The counting rate is controlled by the number of targets not assigned or by the number of channels available for assignment, whichever is less. The counting rate cannot exceed the total number of tracking channels not assigned to targets.

As previously mentioned, each time a WDE tracking channel is assigned to a target, a DC signal demarcating this system event is inputted to the illustrated apparatus at conditioner circuit **22** where it is transformed into a so-called ON voltage level, and is registered by counter **16**, in FIG. 1A. Each assignment also is effective, via OR gate **56**, to down-count the binary counter **55**. In other words, the counter **55** maintains a running total of the number of targets inserted but not yet assigned to WDE tracking channels. For example, the counter **55** might be capable of providing a maximum count of thirty-one unassigned targets at any one time.

The binary count of the up-down counter **55** is used to control or select the timing rate of assignment clock **10**, as long as this number is less than the number of tracking channels then available. Whenever the reverse is true; i.e., the number of channels available is less than the number of targets not assigned, the timing rate of clock **10** is controlled by the number of channels available. More specifically, the number of tracking channels available is converted to a binary number by totalizer **40** whose output is applied to parallel comparator **57**, along with the target count from counter **55**. The comparator **57**, of well-known construction, compares these two binary numbers and selectively opens the AND gate, **58** or **59**, for the lesser of the two. This binary number is then applied, through OR gate **60**, to the timing gates **48** where it selects an equivalent output pulse rate, between 0 and 8 pulses per second, to control the assignment clock **10**. As previously mentioned, the clock **10** provides an accumulated count of the time spent for all targets from insertion by the TACAN observer until assignment to a WDE tracking channel, and, its counting rate will be greatest when all WDE channels are unassigned and at least as many targets are awaiting assignment.

DESIGNATION LOGIC

The ON voltage level signal from input signal conditioner **22**, denoting assignment of a WDE tracking channel is also applied to an AND gate **61** to start the designation timing sequence, for which the designation time count registered by clock **11** may be defined as:

> The time spent from assignment of each WDE tracking channel to a target, until that target (channel) has been designated to a fire control system (FCS). The counting rate is controlled by the number of tracking channels assigned, or by the number of fire control systems not actively engaging targets, whichever is less. The counting rate cannot exceed the total number of fire control systems not actively engaging targets.

More specifically, each WDE tracking channel which is assigned, but not yet designated to a fire control system, is counted by totalizer circuit **41**; i.e., selection and designation of a tracking channel to a fire control system produces an output signal level, at conditioner circuit **23**, which inhibits the AND gate **61** and, in effect, reduces the count at totalizer **41** by one. This yields a binary number from the totalizer **41** representing the number of WDE tracking channels which have been assigned to targets, but, not yet been designated to a fire control system. On the other hand, a fire control system which is not active is indicated by the absence of a FCS busy signal or ON level, at conditioner **24**, and the presence of an OFF signal level on line **62** which is applied to another totalizer circuit **42** to provide a binary registration of the number of fire control systems not then in use.

A parallel compartor **63** compares the registrations of totalizers **41** and **42** and selects the lower binary number for transfer, through AND gate **64** or **65** and OR gate **66**, to the timing gates **49**. This binary input to timing gates **49** is effective, as previously discussed, to select a timing control rate, between 0 and 8 pulses per second, for the designation clock **11**. It should also be noted that the binary output of OR gate **66** is applied to timing gates **49** via the totalizer **67** which is included to provide for additional time accounting following missile-target intercept and prior to FCS reassignment, as will be described in more detail hereinafter. It is sufficient at this point to note that the designation time clock **11** will provide an indication of the accumulated time spent from the assignment of each WDE tracking channel until that channel has been designated to an available fire control system. The FCS busy signal level, applied to counter **17** by scanner **36**, is presumed to denote that the associated fire control system has been designated to a target for the purpose of raid analysis. This signal has been selected in order to cover not only WDE tracking channel designations, but also so-called inter-director (IDD) and Target Data Transmitter (TDT) designations.

ACQUISITION LOGIC

The FCS busy level signal from signal conditioner **24** is also applied to an AND gate **68** to start the acquisition timing sequence for which the acquisition time count registered by clock **12** may be defined as:

> The time spent from each designation of a target to a fire control system, until that fire control system has acquired the designated target. The counting rate is controlled by the number of fire control systems which have received target designation but have not yet acquired the target. The counting rate cannot exceed the number of fire control systems.

More particularly, each FCS busy signal level is gated through AND gates **68** and **69** and applied to a totalizer circuit **44**. When an ON signal level is produced at the output of conditioner circuit **25**, to indicate that the selected fire control system has definitely acquired its desig-

nated target, the acquisition counter 18 registers this event and the binary number registration of totalizer 44 is, in effect, reduced by one. The totalizer 44 thus provides a binary registration of the number of designated, but as yet unacquired, targets and selects the output pulse rate of timing gates 50 and the time count registration at acquisition clock 12. More specifically, the FCS on target signal level, from condititioner circuit 25 is gated through AND gate 70 and functions as an inhibit signal at AND gate 69, to prevent the FCS busy signal level from increasing the binary registration at totalizer 44. As will be appreciated by those skilled in the art, the signal level demarcating the FCS on target event has been selected for the purpose of registering target acquisitions since this choice prevents momentary acquisitions from increasing the acquisition count, at 18, and also prevents increasing the acquisition time count, at 12, whenever the radar loses track and a coast condition results after a missile has been fired. This is because the on target signal level appears after the FCS has established a target track and is "locked up" at missile firing until the FCS has been re-set.

FCS ENGAGEMENT LOGIC

The acquisition of a target by a fire control system, as indicated by an FCS on target signal level at circuit 25, starts the FCS engagement time sequence for which the FCS engagement time count is defined as:

The time spent from acquisition of a target until a missile has been fired, less the time during which the target is out of range of the missile and the time that a launcher is assigned to another fire control system and is not available for use.

Each FCS on target signal level from the input signal conditioner 25 is applied, after AND gate 70, as input to a multiple input AND gate 71 for each fire control system. Gate 71 provides an output signal whenever: the fire control system is on target; the target is not out of range of the missile, as indicated by the inhibiting output from conditioner circuit 26; and, the launcher(s) is (are) not assigned to another fire control system, as indicated by the inhibiting signal applied, via AND gate 72 and line 73 (see FIG. 1B), from conditioning circuits 27 and 28. The output of the AND gate 71 is then sent through another gate AND 74 which is inhibited while a salvo (missile) assigned to that fire control system is in flight, as will be described in more detail hereinafter. The outputs from gate 74 are totalized at 45 and its resulting binary number is used to control timing gates 51 and select the clock pulse rate (between 0 and 8 pulses per second) for the FCS engagement time clock counter 13. For those ships having forward and aft launchers which may be assigned to any fire control system, the illustrated logic circuitry is arranged to inhibit the on target signal whenever the forward *and* aft launchers are assigned to any of the other fire control systems.

TIME OF FLIGHT LOGIC

The indication that a missile has been fired is the so-called rail clear signal received from the launcher. This signal, which must be simulated by a manual switch operation when a simulated missile firing occurs, is conditioned at circuit 29 (FIG. 1B) and produces an on signal level which is counted at counter 19 and also used to set a flip-flop 75 for each fire control system. The time duration of the output from flip-flop 75 is controlled, to demarcate the time of flight of the missile, by either of the signals from the conditioner circuits 30 and 31, as applied through OR gate 76, when either a missile destruct or target intercept event occurs. The output signal from the flip-flop 75 is subsequently applied, along line 77 in FIGS. 1A and 1B, to inhibit AND gate 74 and thereby stop the FCS engagement sequence for each fire control system and is also registered at totalizer 46. This registration at 46 controls the timing gates 52 and selects the proper counting rate for the missile time of flight clock 14.

KILL LOGIC

Following the occurrence of an intercept signal from the fire control system, the raid analysis computing apparatus of the present invention awaits an indication of a target kill, from conditioner 33, and although the FCS engagement clock 13 reverts to counting time during the period between intercept and a kill indication, the time increment is usually very short and produces no appreciable affect on the count. In addition, this delay only occurs when a live missile is fired.

During simulated missile firings, employing an inert or Trainer Surface to Air Missile (TSAM), the conditioner circuit 32 produces an output and the kill signal from conditioner 33 is thereby inhibited at AND gate 78. In its place, the proposed apparatus selects the output of an electronic probability-of-kill pulse generator 79 which is activated by receipt of an intercept pulse. More specifically, the conditioner circuit block designated at 32 contains a free running multivibrator circuit, for example, whose output pulses are applied, together with the intercept signal from circuit 31, to AND gate 80. If the intercept pulse occurs in time coincidence with the logical "one" state of this multivibrator, a kill pulse is generated at the output of generator 79. By varying the time that the free-running multivibrator output remains in the logical "one" state, a wide range of kill probabilities may be generated.

The receipt or simulated generation, at 79, of a kill indication from the fire control system opens the OR gate 81 and sets a flip-flop 82 which prevents counting on the acquisition and FCS engagement clocks 12 and 13 respectively, by inhibiting their input clock pulses until that fire control system has been reset and the target processing sequence is resumed. More specifically, the flip-flop 82, in its logical "one" state, applies an inhibiting signal along line 83 (FIGS. 1A and 1B) to the AND gates 68 and 70, in the control logic of the clocks 12 and 13 respectively. The kill signal indication from flip-flop 82 is also fed to event counter 20 in FIG. 1B and, via line 84 in FIGS. 1A and 1B, to totalizer 67 in the designation time counter logic circuit, where it is added to the number of WDE tracking channels assigned but not designated. The output of this totalizer 67, as mentioned previously, controls timing gates 49 which select the counting rate for the designation clock 11. The kill signal also is sent to a kill regenerator circuit 85 which restores the signal to the fire control system voltage level and distributes it to all shipboard kill indicator lights.

TARGET REGENERATION

If no kill indication is received from circuit 33 or generated at generator circuit 79, the flip-flop 82 will not be set. In this case, with the fire control system not reset, the logical "zero" output of the flip-flop 82 is AND gated, at gate 86, with signals indicating respectively: that a missile is not in flight (from flip-flop 75); the fire control system is not on target (line 87 in FIGS. 1A and 1B); the fire control system is not designated (line 88 in FIGS. 1A and 1B); and, an output from up-down counter 89. The output of gate 86 controls a one-shot multivibrator 90 and causes it to regenerate a target input signal and apply it, via line 91 in FIGS. 1A and 1B, to the target up-down counter 55 in the WDE tracking channel assignment timing logic. This assures that all targets not killed are recycled to the earliest point in the raid analysis.

The up-down counter 89 which controls generation of a target, for reinsertion into the timing sequence, is included for the purpose of registering that a WDE tracking channel has been assigned and then released or, for example, that more than one tracking channel has been released during the time period that the fire control system is engaging a target. On the other hand, generation of a target, at

90, and its reinsertion decreases the stored count at counter 89.

To prevent a target recycle operation from occurring once it (the target) has been fired upon, the reset side of flip-flop 92 and AND gate 93 are supplied, via line 94 in FIGS. 1A and 1B, with an output signal from conditioner circuit 22 indicating the release of a WDE tracking channel. This flip-flop 92 can be set by a cancel target signal from conditioner circuit 34, under the control of the WDE observer, for the purpose of inhibiting AND gate 93 and thereby preventing the tracking channel release signal (line 94) from increasing the count at counter 89. The tracking channel release signal resets the flip-flop 92 so that only one target at a time may be inhibited.

The various raid analysis computer timing sequences mentioned above are stopped, at the completion of a raid analysis, by terminating the generation of the 10 pulse per second input clock pulses for the clock generator 47 of FIG. 2; thus preventing further time and events from accumulating.

What is claimed is:

1. Apparatus for evaluating the performance of a guided missile weapon system during an exercise comprising:

means for registering the occurrence of predetermined weapon system events during said exercise and including counter means for totalizing the number of targets awaiting processing by particular elements of said weapon system and the number of said system elements then available for use,

timing means responsive to the event registration provided by said registering means for registering the time interval between successive events in said system exercise,

said timing means including clock means for measuring the time between successive weapon system events, and

logic circuit means responsive to said event registration for causing said clock means to operate at a variable timing rate dependent upon a comparison between said number of targets awaiting processing and said number of weapon system elements then available for use.

2. The apparatus specified in claim 1 wherein the timing rate of said clock means is determined by the lesser of said numbers.

3. The apparatus specified in claim 1 wherein:

said logic circuit means includes comparator means operably connected to said counter means to have a first input signal indicative of said number of targets awaiting processing by particular elements of said weapon system and a second input signal indicative of said number of system elements then available for use,

clock control means operably connected to said clock means for selecting the timing rate of said clock means, in accordance with the value of an input signal applied to said clock control means and

gating means operably connected between said counter means and said clock control means and controlled by said comparator means to cause whichever of said first and second input signals is indicative of a lesser number to be applied as input to said clock control, for selecting the timing rate of said clock means.

4. The apparatus specified in claim 3 wherein:

said clock means is a pulse counter, and

said clock control means is a source of pulses having variable pulse repetition rates.

5. Apparatus for evaluating the performance of a shipboard guided missile weapon system comprising weapon direction equipment including a plurality of target tracking channels and a plurality of fire control systems, said apparatus comprising:

means for registering the occurrence of predetermined weapon system events, and

timing means responsive to the event registration provided by said registering means for registering the following time intervals:

the time interval between disclosure of a target to the weapon system and the assignment of a tracking channel to said target;

the time interval between said assignment of a tracking channel to said target and the designation of said target to a fire control system;

the time interval between said designation of said target to a fire control system and the acquisition of said target by said fire control system;

the time interval between said acquisition of said target and the firing of a missile at said target; and

the time of flight of said missile.

6. The apparatus specified in claim 5 and further including means for generating a target kill indication of predetermined probability during a test exercise.

7. The apparatus specified in claim 6 and further including means responsive to the kill indication of said generating means for causing a reprocessing of a target in the event no kill indication is generated for said target.

8. The apparatus specified in claim 5 and further including manually operated means for cancelling a target subsequent to its disclosure to said weapon system.

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RODNEY D. BENNETT, JR., Primary Examiner

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89—1.8, 41; 343—5