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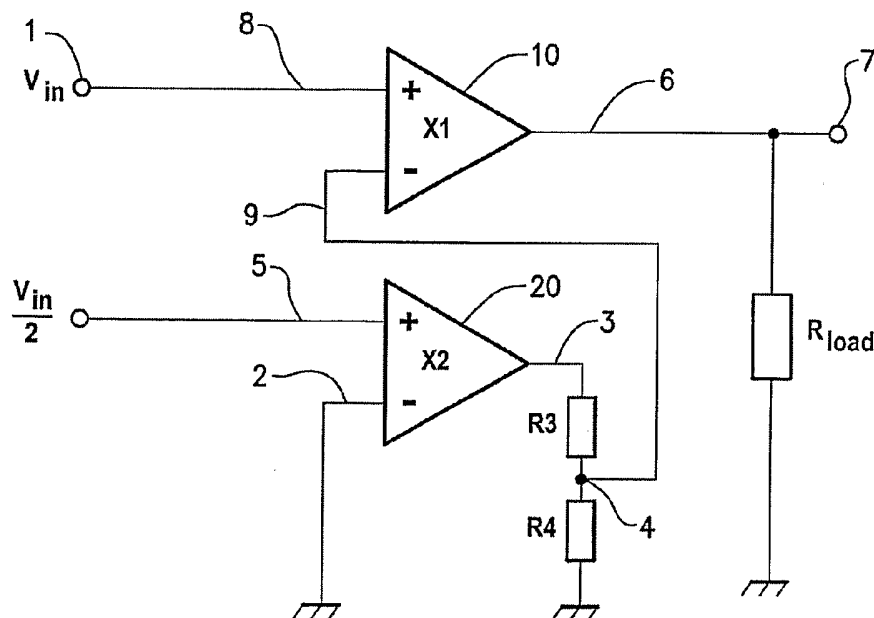
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(54) Title: AN AMPLIFIER APPARATUS AND METHOD



(57) Abstract: An amplifier apparatus comprises a first amplifier arranged to receive an input signal and a second amplifier arranged to receive a proportion of the input signal. A first potential divider is arranged to receive the output signal of the second amplifier and to feed a proportion of the output signal to the first amplifier. The first amplifier is arranged to subtract the proportion of the output signal of the second amplifier from the input signal to produce a difference signal for amplification by the first amplifier. There is also disclosed a method of amplifying a signal.

-An Amplifier Apparatus and Method

Field of the Invention

The present invention relates generally to an amplifier apparatus and method and more particularly to such an apparatus and method suitable for use in the field of high fidelity audio amplifiers.

Background of the Invention

High quality sound systems require amplifiers which produce good sound quality. Sound quality is not something that may easily be measured and an amplifier which may have good physical characteristics such as a wide frequency response at both low and high frequencies, low phase shift and low distortion, may not necessarily produce good quality sound. The reason for this appears to be due to errors or distortions which are not obvious from studying the amplifier's physical characteristics. These distortions may be reduced by applying overall negative feedback.

For audio applications, it is believed that amplifiers without feedback may have desirable characteristics that are good for sound. However, amplifiers without feedback usually do not have good measurement characteristics, such as total harmonic distortion (THD) measurements, when compared to amplifiers that utilise feedback.

There is therefore a need for amplifiers which have improved measurement characteristics and therefore improved performance, irrespective of whether or not feedback is applied.

Summary of the Invention

In general terms, the invention provides an amplifier apparatus and method in which errors in two or more amplifiers in the apparatus are cancelled by subtraction.

According to a first aspect of the invention there is provided an amplifier apparatus comprising:

- a first amplifier arranged to receive an input signal;
 - a second amplifier arranged to receive a proportion of said input signal, said second amplifier having an output signal; and
 - a first potential divider arranged to receive said output signal of said second amplifier and to feed a proportion of said output signal to said first amplifier;
- wherein said first amplifier is arranged to subtract said proportion of said output signal of said second amplifier from said input signal to produce a difference signal amplifiable by said first amplifier.

The amplifier apparatus may further comprise a second potential divider arranged to receive said input signal and feed said proportion of said input signal to said second amplifier.

The amplifier apparatus may further comprise a third potential divider arranged to receive said input signal and feed a proportion of said input signal to said first amplifier.

Preferably, said proportion of said input signal received by said second amplifier is approximately 50% of the proportion of said signal received by said first amplifier.

Preferably, said first amplifier has an output and said apparatus further comprises a resistive element connected between the output of said first amplifier and ground, said resistive element being arranged to reduce variation in the loading of said first amplifier.

In one embodiment, said first and second amplifiers each have a negative input and an output and said apparatus further comprises a first resistive element connected between the negative input of the second amplifier and ground, and

a second resistive element connected between the output of the second amplifier and the negative input of the second amplifier to set the gain of the second amplifier by feedback.

The amplifier apparatus may further comprise a third resistive element connected between the negative input of the first amplifier and the junction of the resistors forming the first potential divider, and a fourth resistive element connected between the output of the first amplifier and the negative input of the first amplifier to set the gain of the first amplifier by feedback.

Said first and second amplifiers may be substantially identical.

In one embodiment, said first and said second amplifiers have substantially identical errors generated therein, said errors being substantially cancelled by the error generated in said second amplifier being subtracted from said error generated in said first amplifier.

Preferably, said second potential divider comprises two substantially equal resistive components. Said resistive components may be high precision components.

In one embodiment, said amplifier apparatus has an overall gain, and said first and second amplifiers each have an associated gain, said gain associated with each of said first and second amplifiers being approximately twice the overall gain of said amplifier apparatus.

In that embodiment, said first potential divider may comprise a first resistive component and a second resistive component, each of said first and second resistive components having an associated resistance, the ratio of said resistance associated with said first resistive component to said resistance associated with said second resistive component being such that the amplitude of said signal at a junction of said first and second resistive components is

substantially equal to the amplitude of said input signal to said second amplifier divided by the gain of said second amplifier.

In that case, said first amplifier may have an output, and the sum of the associated resistances of said first and second resistive components of said first potential divider may be substantially equal to a resistive load applied to said output of said first amplifier.

Advantageously, said proportion of said input signal received by said second amplifier is approximately 50%.

According to a second aspect there is provided an audio amplifier system comprising the amplifier apparatus defined above.

According to a third aspect of the invention there is provided a method of amplifying a signal comprising:

- applying an input signal to a first amplifier;
- applying a proportion of said input signal to a second amplifier, said second amplifier having an output signal;
- applying to a first potential divider said output signal of said second amplifier;
- applying a proportion of said output signal to said first amplifier;
- and
- subtracting in said first amplifier said proportion of said output signal of said second amplifier from said input signal to produce a difference signal amplifiable by said first amplifier.

The method may further comprise applying said input signal to a second potential divider, said proportion of said input signal applied to said second amplifier being applied by said second potential divider.

The method may further comprise applying said input signal to a third potential divider, and applying a proportion of said input signal to said first amplifier through said third potential divider.

Preferably, said proportion of said input signal received by said second amplifier is approximately 50% of said signal applied to said first amplifier through said third potential divider.

The method may further comprise reducing variation in the loading of said first amplifier using a resistive element connected between the output of said first amplifier and ground.

Preferably, said first and second amplifiers each have a negative input and an output and said method further comprises setting the gain of the second amplifier by feedback applied by connecting a first resistive element between the negative input of the second amplifier and ground, and a second resistive element between the output of the second amplifier and the negative input of the second amplifier.

The method may further comprise setting the gain of the first amplifier by feedback applied by connecting a third resistive element between the negative input of the first amplifier and the junction of the resistors forming the first potential divider, and a fourth resistive element between the output of the first amplifier and the negative input of the first amplifier.

Preferably, said first and second amplifiers are substantially identical, and said second potential divider comprises two substantially equal resistive components, said step of applying a proportion of said input signal to said second amplifier comprises applying approximately 50% of said input signal to said second amplifier.

Preferably, said amplifier apparatus has an overall gain, and said first and second amplifiers each have an associated gain, the method further comprising arranging said first and second amplifiers such that the gain associated with each of said first and second amplifiers is approximately twice the overall gain of said amplifier apparatus.

Preferably, said first potential divider comprises a first resistive component and a second resistive component, each of said first and second resistive components having an associated resistance, the method further comprising selecting said resistive components such that the ratio of said resistance associated with said first resistive component to said resistance associated with said second resistive component is such that the amplitude of said signal at a junction of said first and second resistive components is substantially equal to the amplitude of said input signal to said second amplifier divided by the gain of said second amplifier.

Preferably, said first amplifier has an output, said method further comprising the step of applying a resistive load to said output of said first amplifier such that the sum of the associated resistances of said first and second resistive components of said first potential divider is substantially equal to said applied load.

Preferably, said first and said second amplifiers have substantially identical errors generated therein, the method further comprising substantially cancelling said errors by subtracting said error generated in said second amplifier from said error generated in said first amplifier.

Features described in relation to one aspect of the invention may also be applicable to another aspect of the invention.

Brief Description of the Drawings

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the accompanying drawings, of which:

Figure 1 is a schematic circuit diagram of an amplifier circuit according to one embodiment of the invention;

Figure 2a is a graph showing the frequency response of an amplifier circuit taken at the output of amplifier 20 in the circuit of Figure 1;

Figure 2b is a graph showing the frequency response of an amplifier taken at the output of amplifier 10 in the circuit of Figure 1;

Figure 3a is a further graph showing the phase shift of an amplifier circuit taken at the output of amplifier 20 in the circuit of Figure 1;

Figure 3b is a further graph showing the phase shift of an amplifier taken at the output of amplifier 10 in the circuit of Figure 1;

Figure 4a is a spectrum plot of the output signal the amplifier 20 in the circuit of Figure 1 with an input of 1kHz;

Figure 4b is a spectrum plot of the output signal the amplifier 10 in the circuit of Figure 1 with an input of 1kHz;

Figure 5 is a schematic circuit diagram of an amplifier circuit according to a second embodiment of the invention;

Figure 6 is a schematic circuit diagram of an amplifier circuit according to a third embodiment of the invention;

Figure 7 is a schematic circuit diagram of an amplifier circuit according to a fourth embodiment of the invention; and

Figure 8 is a schematic circuit diagram of an amplifier circuit according to a fifth embodiment of the invention.

Description of Preferred Embodiments

Figure 1 shows an amplifier circuit according to one embodiment of the invention. The circuit comprises two identical amplifiers, a main amplifier (X1) 10 and a second amplifier (X2) 20. Both amplifiers have twice the gain G_v required of the overall system. As the amplifiers are identical, they will have similar errors E generated during the amplification process. Ideally, the same operating conditions, such as the same supply voltage, same input voltage and same load impedance are applied to both amplifiers 10 and 20.

In the system of Figure 1, the incoming signal V_{in} is applied to a first point (point 1) and is then applied to the positive input of the main amplifier 10. The incoming signal is also applied to a first end of a first resistor R1, the other end of the first resistor R1 being connected to a first end of a second resistor R2. The other end of the second resistor R2 is connected to the system ground. The junction of the first and second resistors R1 and R2 which form a potential divider is connected to the positive input of the second amplifier 20. The negative input of the second amplifier 20 is connected, at a point 2, to the system ground.

The output of the second amplifier 20 is connected, at a point 3, to the first end of a third resistor R3, the other end of the third resistor R3 being connected to a first end of a fourth resistor R4. The second end of the fourth resistor R4 is connected to system ground.

The junction of the third and fourth resistors R3 and R4, which is termed point 4, is connected to the negative input 9 of the main amplifier 10. The output of the main amplifier 10 is connected to one end of a load, which may be, for example, another amplifier such as a power amplifier in which case the load is a resistive element to ground, or another element such as a loud speaker. The other end of the load is connected to the system ground. The voltage across the load constitutes the output of the amplifier circuit.

The first and second resistors R1 and R2 are preferably identical and the signal at a point 5, which is the positive input of the second amplifier 20, will be half the input signal at point 1. Thus, if

$$\begin{aligned} R1 &= R2 \quad \text{then} \\ V5 &= \frac{1}{2} V1 = \frac{1}{2} V_{in} \end{aligned} \quad \text{----- (1)}$$

The voltage at point 3, which is the output of the second amplifier 20, is given by:

$$V3 = 2 \times G_V (V5 - V2) + E \quad \text{where E is the error generated by X2}$$

$$\begin{aligned}
 &= 2 \times G_V \left(\frac{1}{2} V_{in} - 0 \right) + E && \text{Substitute eq (1)} \\
 &= 2 \times G_V \left(\frac{1}{2} V_{in} \right) + E \\
 &= G_V \times V_{in} + E \\
 V_3 &= G_V V_{in} + E && \text{----- (2)}
 \end{aligned}$$

The third and fourth resistors R3 and R4 are preferably high precision resistors and the values are related as follows:

$$\frac{R_4}{R_3 + R_4} = \frac{1}{2 \times G_V} \text{----- (3)}$$

Further, if $R_3 + R_4 = R_{load}$, so that both amplifiers 10 and 20 are equally loaded, this is the optimal condition but is not essential for the invention to work. Ideally, this load condition should be implemented for optimal results. However, the present invention will still work even if there is deviation from this load condition.

The voltage at the output of the potential divider formed by the third and fourth resistors R3 and R4, is given by:

$$\begin{aligned}
 V_4 &= \frac{R_4}{R_3 + R_4} \times V_3 \\
 &= \frac{1}{2 \times G_V} \times (G_V V_{in} + E) \text{ Substitute eq (2) and eq (3)} \\
 V_4 &= \frac{V_{in}}{2} + \frac{E}{2G_V} \text{----- (4)}
 \end{aligned}$$

This voltage V_4 is applied to the negative input of the main amplifier 10 at a point 9 and the voltage at point 9 may be denoted as follows:

$$V_9 = \frac{V_{in}}{2} + \frac{E}{2G_V} \quad (5)$$

The positive input of the main amplifier 10 at point 8 is connected to the input of the system at point 1. Therefore the voltage at point 8 may be denoted by:

$$V_8 = V_{in} \quad (6)$$

The voltage at the output of the main amplifier 10 at point 6 may given by:

$$V_6 = 2 \times G_V (V_8 - V_9) + E$$

If Equations (6) and (5) are substituted in the above equation for V_8 and V_9 respectively, then:

$$\begin{aligned} V_6 &= 2 \times G_V \left[V_{in} - \left(\frac{V_{in}}{2} + \frac{E}{2G_V} \right) \right] + E \\ &= 2 \times G_V \left[V_{in} - \frac{V_{in}}{2} - \frac{E}{2G_V} \right] + E \\ &= 2 \times G_V \left[\frac{V_{in}}{2} - \frac{E}{2G_V} \right] + E \\ &= G_V V_{in} - E + E \\ V_6 &= G_V V_{in} \quad (7) \end{aligned}$$

It will be seen that the error E generated during amplification is cancelled out leaving the output of the amplifier circuit V_{out} at point 7 as:

$$V_{out} = G_V V_{in}$$

An alternative presentation of the above equations is set out below. In this alternative presentation, the errors generated in the amplifier 10 and in the amplifier 20 are made distinct by naming them E1 and E2 respectively. It is also shown that, in this embodiment, $R_1=R_2$ is a condition for the output level of both amplifiers 10 and 20 to be the same and consequently for the errors from both amplifiers 10 and 20 to be the same. In general, the input to amplifier 20 should be half the magnitude of the input to amplifier 10.

The signal at a point 5, which is the positive input of the second amplifier 20

$$V_5 = \frac{R_2}{R_1 + R_2} V_{in}$$

Let A1 be the attenuation of the potential divider formed by the resistors R1 and

$$R_2, \text{ ie } A_1 = \frac{R_2}{R_1 + R_2}.$$

$$\text{Then } V_5 = A_1 V_{in} \quad \text{-----}(1)$$

Let G be the gain of the individual amplifiers (not the whole system), then

$$V_3 = G(V_5 - V_2) + E_2 \quad \text{Substitute eq(1)}$$

$$V_3 = A_1 G V_{in} + E_2 \quad \text{-----}(2)$$

where E_2 is error generated in second amplifier 20 and $V_2=0$.

The voltage at the output of the potential divider formed by the third and fourth resistors R3 and R4, may be given by:

$$V_4 = \frac{R_4}{R_3 + R_4} V_3$$

Let A2 be the attenuation of the potential divider formed by the resistors R3 and

$$R_4, \text{ ie } A_2 = \frac{R_4}{R_3 + R_4}.$$

$$\text{Then } V_4 = A_2 V_3$$

This voltage V_4 is applied to the negative input of the main amplifier 10 at a point 9 and the voltage at point 9 may be denoted as follows:

$$V_9 = V_4 = A_2 A_1 G V_{in} + A_2 E_2 \quad \text{-----}(3)$$

The voltage at the output of the main amplifier 10 at point 6 may be given by:

$V_6 = G(V_8 - V_9) + E_1$, where E_1 is the error generated in the first amplifier 10, so

$$\begin{aligned} V_6 &= G(V_{in} - A_2 A_1 G V_{in} - A_2 E_2) + E_1 \\ &= G(1 - A_2 A_1 G) V_{in} - A_2 G E_2 + E_1 \quad \text{-----}(4) \end{aligned}$$

For the error terms to cancel out,

$$-A_2 G E_2 + E_1 = 0$$

If the errors generated in both amplifiers 10 and 20 are the same, that is, $E_1 = E_2$, then

$$E_1(1 - A_2 G) = 0$$

$$A_2 = \frac{1}{G}$$

In order to have the same errors from both amplifiers 10 and 20, that is, $E_1 = E_2$, the operating conditions of both amplifiers 10 and 20 should be the same. One consideration is that the output level from both amplifiers 10 and 20 should be the same for the operating conditions to be the same, since they have the same gain and are identical.

Thus, one way to check is to set the output of the first amplifier 10 equal to the output of the second amplifier 20. Thus,

$$V_3 = V_6$$

$$A_1 G V_{in} + E_2 = G(1 - A_2 A_1 G) V_{in} - A_2 G E_2 + E_1, \text{ from Eq(2) and Eq(4)}$$

As the magnitude of the errors are very much smaller than the amplified output signal, ignoring the error terms,

$$A_1 G V_{in} = G(1 - A_2 A_1 G) V_{in}$$

$$\text{As } A_2 = \frac{1}{G},$$

Then $A_1 = 1 - A_1$

$$A_1 = \frac{1}{2}$$

This implies that for this embodiment, $R_1 = R_2$ is a necessary condition for both amplifiers to have effectively the same output level and therefore same errors. However, it should be noted that the system embodying the present invention should still work even if there is slight deviation from this condition, that is, R_1 is not equal to R_2 . In such a condition, the error will be higher at the output. This has been verified by simulation.

Using $A_1 = \frac{1}{2}$ and $A_2 = \frac{1}{G}$, from Eq(4),

$$\begin{aligned} V_6 &= G(1 - A_2 A_1 G)V_{in} - A_2 G E_2 + E_1 \\ &= G\left(1 - \frac{1}{G} \frac{1}{2} G\right)V_{in} - \frac{1}{G} G E_2 + E_1 \\ &= \frac{G}{2} V_{in} - E_2 + E_1 \end{aligned}$$

If the errors are equal and cancel each other,

$$V_6 = \frac{G}{2} V_{in}$$

If we let the gain of the overall system be G_v (as was previously), then $G_v = \frac{G}{2}$.

And $V_6 = G_v V_{in}$

Thus, the output is an amplified version of the input signal with a gain of G_v , without error.

Figure 2a is a graph showing the frequency response of an amplifier circuit taken at the output of amplifier 20 in the circuit of Figure 1, which gives a bandwidth at the -3db point of 1.373 MHz. As the amplifiers 10 and 20 are identical and operating under similar conditions, the amplifier 20 alone may be considered to be a standard amplifier not embodying the invention.

Figure 2b is a graph showing the frequency response of an amplifier taken at the output of amplifier 10 in the circuit of Figure 1 according to one embodiment of the present invention and giving a bandwidth of 3.234 MHz at the -3db point.

Figure 3a is a graph showing the phase shift of an amplifier circuit taken at the output of amplifier 20 in the circuit of Figure 1. A phase deviation of -5.252 degrees at 100kHz is shown.

Figure 3b is a graph showing the phase shift of an amplifier taken at the output of amplifier 10 in the circuit of Figure 1. A phase deviation of -2.082 degrees at 100kHz is shown.

It may be noted that 20kHz is the typical upper limit for audio frequency.

Figure 4a is a spectrum plot of the output signal the amplifier 20 in the circuit of Figure 1 with an input of 1kHz and Figure 4b is a spectrum plot of the output signal the amplifier 10 in the circuit of Figure 1 with an input of 1kHz.

Figures 4a and 4b show more clearly the improvement in total harmonic distortion (THD). As shown in these figures, the THD+Noise from amplifier 20 is 0.9415% and that of amplifier 10 is 0.0367%. The numerical values will vary according to the input level set for the simulation.

Figure 5 shows an amplifier circuit according to a second embodiment of the invention. The circuit comprises two identical amplifiers, a main amplifier (X1) 10 and a second amplifier (X2) 20. Both amplifiers have twice the gain G_v required of the overall system. As the amplifiers are identical, they will have similar errors E generated during the amplification process. Ideally, the same operating conditions, such as the same supply voltage, same input voltage and same load impedance are applied to both amplifiers 10 and 20.

In the system of Figure 5, the incoming signal V_{in} is applied to a first point (point 1) and is then applied to the positive input of the main amplifier 10. The incoming signal is also applied, at half level, to the positive input of the second amplifier 20. The negative input of the second amplifier 20 is connected, at a point 2, to the system ground.

The output of the second amplifier 20 is connected, at a point 3, to the first end of a first resistor R3, the other end of the first resistor R3 being connected to a first end of a second resistor R4. The second end of the second resistor R4 is connected to system ground.

The junction of the first and second resistors R3 and R4, which is termed point 4, is connected to the negative input 9 of the main amplifier 10. The output of the main amplifier 10 is connected to one end of a load, which may be, for example, another amplifier such as a power amplifier in which case the load is a resistive element to ground, or another element such as a loud speaker. The other end of the load is connected to the system ground. The voltage across the load constitutes the output of the amplifier circuit.

The operation of the circuit of Figure 5 is the same as that described above in connection with Figure 1, the only difference being the removal from the circuit of Figure 5 of the potential divider formed by R1 and R2 which is present in the circuit of Figure 1. However, for the embodiment of Figure 5 to work optimally, the input to amplifier 20 should be half the magnitude of the input to amplifier 10. In this embodiment, an input V_{in} is applied to amplifier 10 and the same input but at half the magnitude, $V_{in}/2$, is applied to amplifier 20. These inputs may be from a source, such as a digital source with a Digital-to-Analogue converter being used to obtain the above configuration.

Figure 6 shows an amplifier circuit according to a third embodiment of the invention. The circuit comprises two identical amplifiers, a main amplifier (X1) 10 and a second amplifier (X2) 20. Both amplifiers have twice the gain G_v

required of the overall system. As the amplifiers are identical, they will have similar errors E generated during the amplification process. Ideally, the same operating conditions, such as the same supply voltage, same input voltage and same load impedance are applied to both amplifiers 10 and 20.

In the system of Figure 6, the incoming signal is applied to a first point (point 1) and is then applied to a potential divider formed of two resistors $R5$ and $R6$. The junction (point 8) of the potential divider is connected to the positive input of the main amplifier 10. The end of resistor $R6$ which is not connected to resistor $R5$ is connected to the system ground. The input signal is applied to that end of resistor $R5$ which is not connected to resistor $R6$. The incoming signal is also applied to a first end of a further resistor $R1$, the other end of the resistor $R1$ being connected to a first end of another resistor $R2$. The other end of the resistor $R2$ is connected to the system ground. The junction (point 5) of the resistors $R1$ and $R2$ which form a potential divider is connected to the positive input of the second amplifier 20. The negative input of the second amplifier 20 is connected, at a point 2, to the system ground.

The values of $R1$, $R2$, $R5$ and $R6$ are selected such that the voltage applied to the positive input (point 5) of the amplifier 20 is half that applied to the positive input of the amplifier 10.

The output of the second amplifier 20 is connected, at a point 3, to the first end of a further resistor $R3$, the other end of the further resistor $R3$ being connected to a first end of another resistor $R4$. The second end of the resistor $R4$ is connected to system ground.

The junction of the resistors $R3$ and $R4$, which is termed point 4, is connected to the negative input 9 of the main amplifier 10. The output of the main amplifier 10 is connected to one end of a load, which may be, for example, another amplifier such as a power amplifier in which case the load is a resistive element to ground, or another element such as a loud speaker. The other end of the

load is connected to the system ground. The voltage across the load constitutes the output of the amplifier circuit.

The operation of the circuit of Figure 6 is essentially the same as that described above in connection with Figure 1, the only difference being the addition in the circuit of Figure 6 of a further potential divider formed by resistors R5 and R6 which is not present in the circuit of Figure 1. In this embodiment, an input V_{in} is applied to amplifier 10 and the same input but at half the magnitude, $V_{in}/2$, is applied to amplifier 20. As with the circuit of Figure 5, these inputs may be from a source, such as a digital source with a Digital-to-Analogue converter being used to obtain the above configuration.

Figure 7 shows an amplifier circuit according to a fourth embodiment of the invention. The circuit comprises two identical amplifiers, a main amplifier (X1) 10 and a second amplifier (X2) 20. Both amplifiers have twice the gain G_v required of the overall system. As the amplifiers are identical, they will have similar errors E generated during the amplification process. Ideally, the same operating conditions, such as the same supply voltage, same input voltage and same load impedance are applied to both amplifiers 10 and 20.

In the system of Figure 7, the incoming signal V_{in} is applied to a first point (point 1) and is then applied to the positive input of the main amplifier 10. The incoming signal is also applied to a first end of a first resistor R1, the other end of the first resistor R1 being connected to a first end of a second resistor R2. The other end of the second resistor R2 is connected to the system ground. The junction (point 5) of the first and second resistors R1 and R2 which form a potential divider is connected to the positive input of the second amplifier 20. The negative input of the second amplifier 20 is connected, at a point 2, to the system ground.

The output of the second amplifier 20 is connected, at a point 3, to the first end of a third resistor R3, the other end of the third resistor R3 being connected to a

first end of a fourth resistor R4. The second end of the fourth resistor R4 is connected to system ground.

The junction of the third and fourth resistors R3 and R4, which is termed point 4, is connected to the negative input 9 of the main amplifier 10. The output of the main amplifier 10 is connected to one end of a load R_{load} , which may be, for example, another amplifier such as a power amplifier in which case the load R_{load} is a resistive element to ground, or another element such as a loud speaker. The other end of the load R_{load} is connected to the system ground. The voltage across the load R_{load} constitutes the output of the amplifier circuit. A further resistor R7 is connected across the output of the amplifier 10 and the system ground, in parallel with the load R_{load} .

The loading on the amplifier 10 will depend on the load R_{load} the user connects to the amplifier system and therefore the resistor R7 is included to reduce the variation in the overall load applied to the system. If, for example, the implementation is for a pre-amplifier, the load R_{load} may be another amplifier, which may have a typical input impedance of between 10K ohms to 47K ohms. If the resistor R7, having a typical value of 1K ohms, is added in parallel with R_{load} , as shown in Figure 7, the load of amplifier 10 is the effective resistance of resistor R7 in parallel with R_{load} ($R7//R_{load}$). Thus, the range of load conditions will then be narrower, as:

$R7//R_{load}=1k//10k=909$ ohms, if the load has an input impedance of 10k ohms and

$R7//R_{load}=1k//47k=979$ ohms, if the load has an input impedance of 47k ohms.

At the same time, the resistance value of resistors R3 + R4 may be set between around 909 ohms and around 979 ohms so that the load conditions for the amplifier 10 and the amplifier 20 are close to each other.

Thus, the circuit of Figure 7 is identical to that of Figure 1 with the exception of the addition of the further resistor R7 to the circuit of Figure 7. The operation of

the circuit of Figure 7 is essentially the same as that described above in connection with Figure 1.

Figure 8 shows an amplifier circuit according to a fifth embodiment of the invention. The circuit comprises two identical amplifiers, a main amplifier (X1) 10 and a second amplifier (X2) 20. Both amplifiers have twice the gain G_v required of the overall system. As the amplifiers are identical, they will have similar errors E generated during the amplification process. Ideally, the same operating conditions, such as the same supply voltage, same input voltage and same load impedance are applied to both amplifiers 10 and 20.

In the system of Figure 8, the incoming signal V_{in} is applied to a first point (point 1) and is then applied to the positive input of the main amplifier 10. The incoming signal is also applied to a first end of a first resistor R1, the other end of the first resistor R1 being connected to a first end of a second resistor R2. The other end of the second resistor R2 is connected to the system ground. The junction (point 5) of the first and second resistors R1 and R2 which form a potential divider is connected to the positive input of the second amplifier 20. The negative input of the second amplifier 20 is connected, at a point 2, to the junction of two further resistors R8 and R9. The other end of R9 which is not connected to R8 is taken to the system ground. The end of resistor R8 not connected to resistor R9 is connected to the output the amplifier 20, to control the gain of the amplifier 20 by applying feedback.

The output of the second amplifier 20 is connected, at a point 3, to the first end of a third resistor R3, the other end of the third resistor R3 being connected to a first end of a fourth resistor R4. The second end of the fourth resistor R4 is connected to system ground.

The junction of the third and fourth resistors R3 and R4, which is termed point 4, is connected to a further resistor R11, the other end of which is connected to the negative input 9 of the main amplifier 10. A further resistor R10 is

connected between the negative input to the amplifier 10 and the output of the amplifier 10 at a point 6, to control the gain of the amplifier 10 by applying feedback. The values of the resistors R8, R9, R10 and R11 are preferably selected that the gains of the amplifiers 10 and 20 are substantially the same.

The output of the main amplifier 10 is connected to one end of a load, which may be, for example, another amplifier such as a power amplifier in which case the load is a resistive element to ground, or another element such as a loud speaker. The other end of the load is connected to the system ground. The voltage across the load constitutes the output of the amplifier circuit.

Thus, the circuit of Figure 8 is identical to that of Figure 1 with the exception of the addition of the further resistors R8 to R11 to the circuit of Figure 7. The operation of the circuit of Figure 7 is essentially the same as that described above in connection with Figure 1, except that feedback is applied to both amplifiers 10 and 20 to control the gain of the amplifiers.

Thus, one or more embodiments of the invention may provide an amplifier system in which the bandwidth is significantly greater than that of conventional amplifiers with reduced phase shift and minimal distortion as the distorting errors generated by the individual amplifiers in the circuit are cancelled out.

The amplifiers 10 and 20 used in the simulation to obtain the figures quoted above did not have feedback applied internally. However, embodiments of the present invention may be applied to amplifiers with or without feedback.

Various modifications to the embodiments of the present invention described above may be made. For example, other components and method steps can be added or substituted for those above. Thus, although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to the skilled reader, without departing from the spirit and scope of the invention.

Claims:

1. An amplifier apparatus comprising:
 - a first amplifier arranged to receive an input signal;
 - a second amplifier arranged to receive a proportion of said input signal, said second amplifier having an output signal; and
 - a first potential divider arranged to receive said output signal of said second amplifier and to feed a proportion of said output signal to said first amplifier;wherein said first amplifier is arranged to subtract said proportion of said output signal of said second amplifier from said input signal to produce a difference signal amplifiable by said first amplifier.
2. An amplifier apparatus according to claim 1, further comprising a second potential divider arranged to receive said input signal and feed said proportion of said input signal to said second amplifier.
3. An amplifier apparatus according to claim 2, further comprising a third potential divider arranged to receive said input signal and feed a proportion of said input signal to said first amplifier.
4. An amplifier apparatus according to claim 3, wherein said proportion of said input signal received by said second amplifier is approximately 50% of the proportion of said signal received by said first amplifier.
5. An amplifier apparatus according to any one of the preceding claims, wherein said first amplifier has an output, said apparatus further comprising a resistive element connected between the output of said first amplifier and ground, said resistive element being arranged to reduce variation in the loading of said first amplifier.
6. An amplifier apparatus according to any one of the preceding claims, wherein said first and second amplifiers each have a negative input and an

output, said apparatus further comprising a first resistive element connected between the negative input of the second amplifier and ground, and a second resistive element connected between the output of the second amplifier and the negative input of the second amplifier to set the gain of the second amplifier by feedback.

7. An amplifier apparatus according to claim 6, further comprising a third resistive element connected between the negative input of the first amplifier and the junction of the resistors forming the first potential divider, and a fourth resistive element connected between the output of the first amplifier and the negative input of the first amplifier to set the gain of the first amplifier by feedback.

8. An amplifier apparatus according to any one of the preceding claims, wherein said first and second amplifiers are substantially identical.

9. An amplifier apparatus according to claim 8, wherein said first and said second amplifiers have substantially identical errors generated therein, said errors being substantially cancelled by the error generated in said second amplifier being subtracted from said error generated in said first amplifier.

10. An amplifier apparatus according to any one of claims 2 to 9, wherein said second potential divider comprises two substantially equal resistive components.

11. An amplifier apparatus according to claim 10, wherein said resistive components are high precision components.

12. An amplifier apparatus according to any one of the preceding claims, wherein said amplifier apparatus has an overall gain, and said first and second amplifiers each have an associated gain, said gain associated with each of said

first and second amplifiers being approximately twice the overall gain of said amplifier apparatus.

13. An amplifier apparatus according to claim 12, wherein said first potential divider comprises a first resistive component and a second resistive component, each of said first and second resistive components having an associated resistance, the ratio of said resistance associated with said first resistive component to said resistance associated with said second resistive component being such that the amplitude of said signal at a junction of said first and second resistive components is substantially equal to the amplitude of said input signal to said second amplifier divided by the gain of said second amplifier.

14. An amplifier apparatus according to claim 13, wherein said first amplifier has an output, and wherein the sum of the associated resistances of said first and second resistive components of said first potential divider is substantially equal to a resistive load applied to said output of said first amplifier.

15. An amplifier apparatus according to any one of the preceding claims, wherein said proportion of said input signal received by said second amplifier is approximately 50%.

16. A method of amplifying a signal comprising:
applying an input signal to a first amplifier;
applying a proportion of said input signal to a second amplifier,
said second amplifier having an output signal;
applying to a first potential divider said output signal of said
second amplifier;
applying a proportion of said output signal to said first amplifier;
and
subtracting in said first amplifier said proportion of said output
signal of said second amplifier from said input signal to produce a difference
signal amplifiable by said first amplifier.

17. A method according to claim 16, further comprising applying said input signal to a second potential divider, said proportion of said input signal applied to said second amplifier being applied by said second potential divider.

18. A method according to claim 17, further comprising applying said input signal to a third potential divider, and applying a proportion of said input signal to said first amplifier through said third potential divider.

19. A method according to claim 18, wherein said proportion of said input signal received by said second amplifier is approximately 50% of said signal applied to said first amplifier through said third potential divider.

20. A method according to any one of claims 16 to 19, further comprising reducing variation in the loading of said first amplifier using a resistive element connected between the output of said first amplifier and ground.

21. A method according to any one of claims 16 to 20, wherein said first and second amplifiers each have a negative input and an output, said method further comprising setting the gain of the second amplifier by feedback applied by connecting a first resistive element between the negative input of the second amplifier and ground, and a second resistive element between the output of the second amplifier and the negative input of the second amplifier.

22. A method according to claim 21, further comprising setting the gain of the first amplifier by feedback applied by connecting a third resistive element between the negative input of the first amplifier and the junction of the resistors forming the first potential divider, and a fourth resistive element between the output of the first amplifier and the negative input of the first amplifier.

23. A method according to any one of claims 17 to 22, wherein said first and second amplifiers are substantially identical, and said second potential divider

comprises two substantially equal resistive components, said step of applying a proportion of said input signal to said second amplifier comprises applying approximately 50% of said input signal to said second amplifier.

24. A method according to any one of claims 16 to 23, wherein said amplifier apparatus has an overall gain, and said first and second amplifiers each have an associated gain, the method further comprising arranging said first and second amplifiers such that the gain associated with each of said first and second amplifiers is approximately twice the overall gain of said amplifier apparatus.

25. A method according to any one of claims 16 to 24, wherein said first potential divider comprises a first resistive component and a second resistive component, each of said first and second resistive components having an associated resistance, the method further comprising selecting said resistive components such that the ratio of said resistance associated with said first resistive component to said resistance associated with said second resistive component is such that the amplitude of said signal at a junction of said first and second resistive components is substantially equal to the amplitude of said input signal to said second amplifier divided by the gain of said second amplifier.

26. A method according to any one of claims 16 to 25, wherein said first amplifier has an output, said method further comprising the step of applying a resistive load to said output of said first amplifier such that the sum of the associated resistances of said first and second resistive components of said first potential divider is substantially equal to said applied load.

27. A method according to any one of claims 16 to 26, wherein said first and said second amplifiers have substantially identical errors generated therein, the method further comprising substantially cancelling said errors by subtracting

said error generated in said second amplifier from said error generated in said first amplifier.

28. An audio amplifier system comprising the amplifier apparatus of any one of claims 1 to 15.

1/6

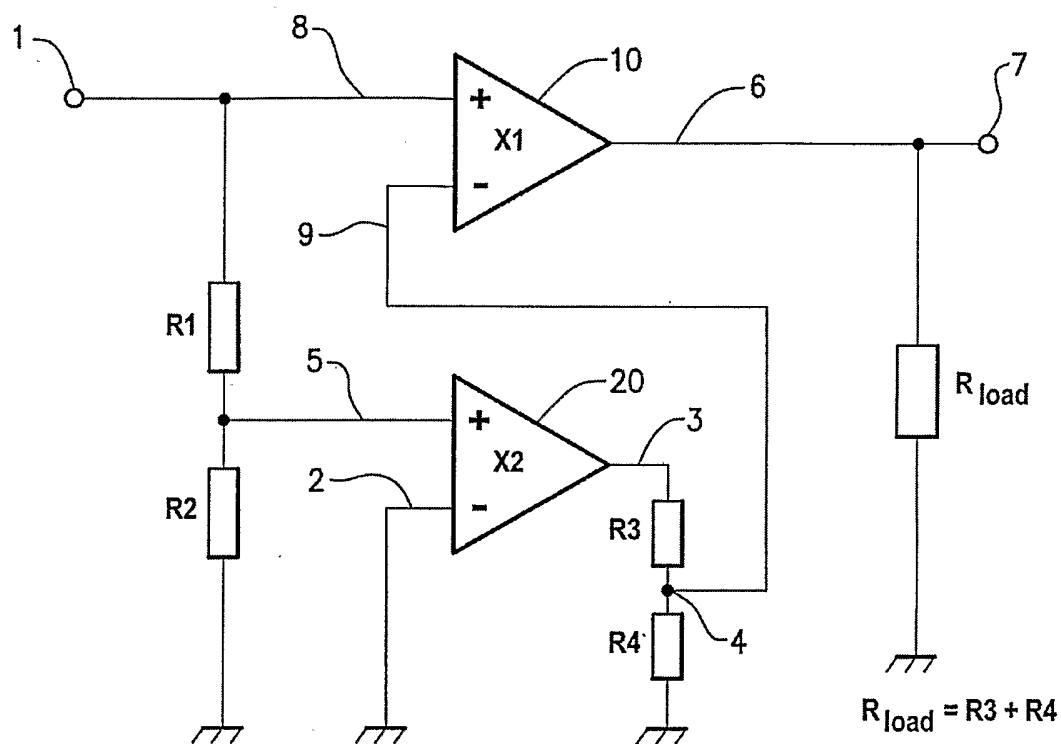


Fig. 1

2/6

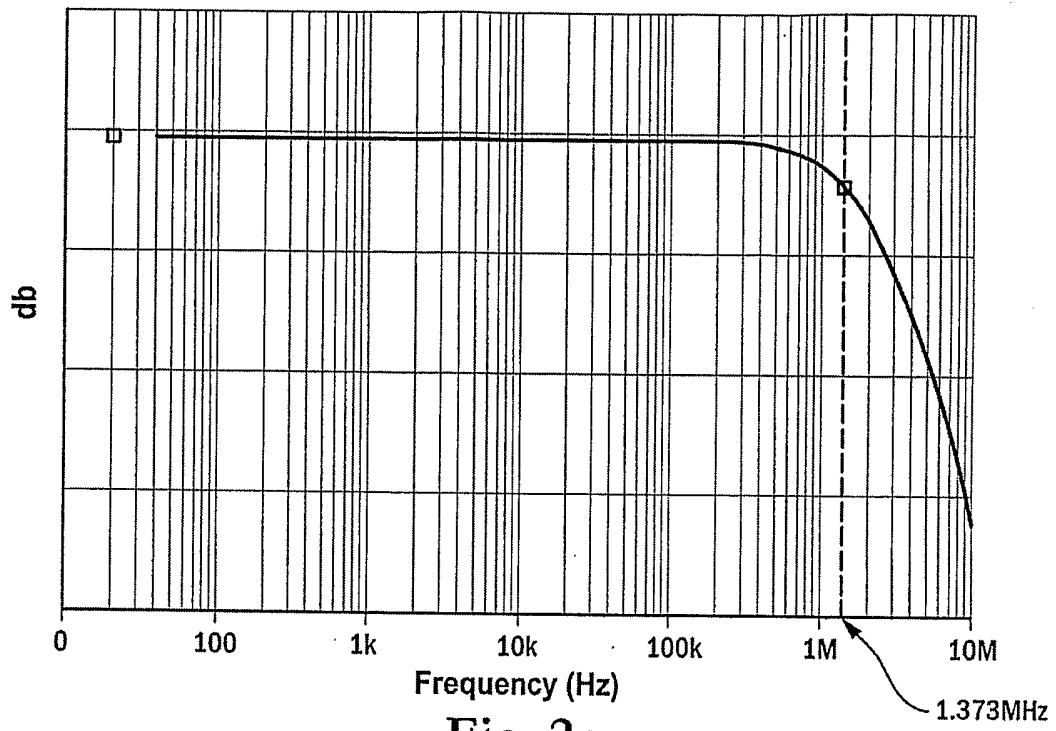


Fig. 2a

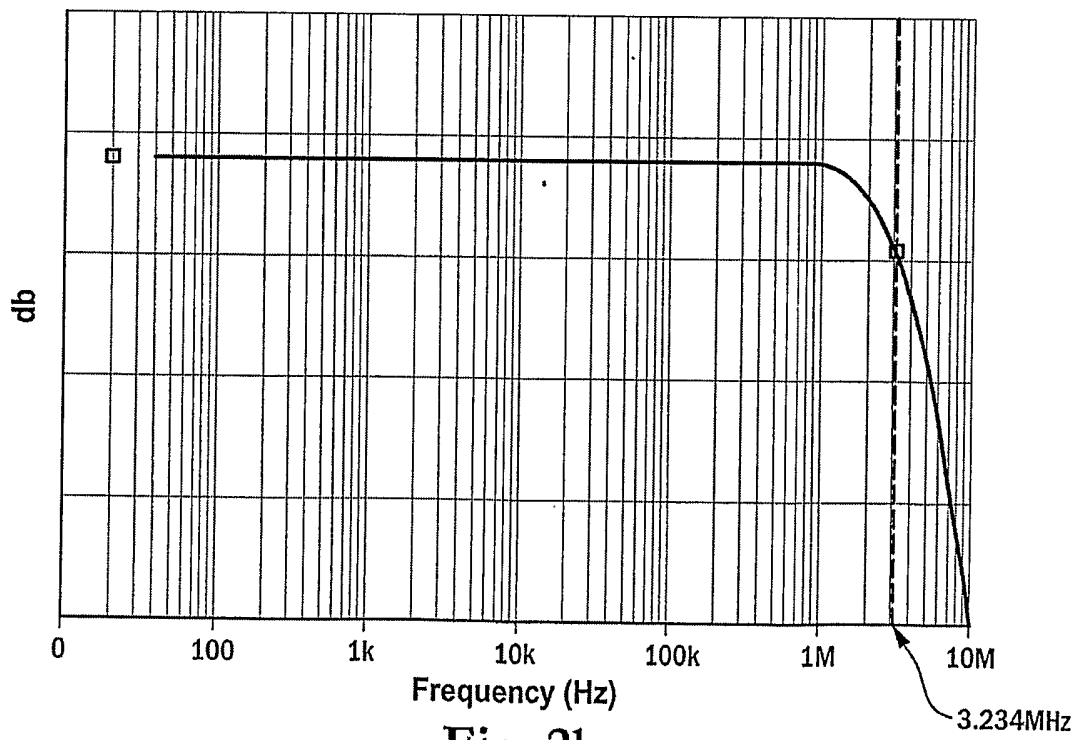


Fig. 2b

3/6

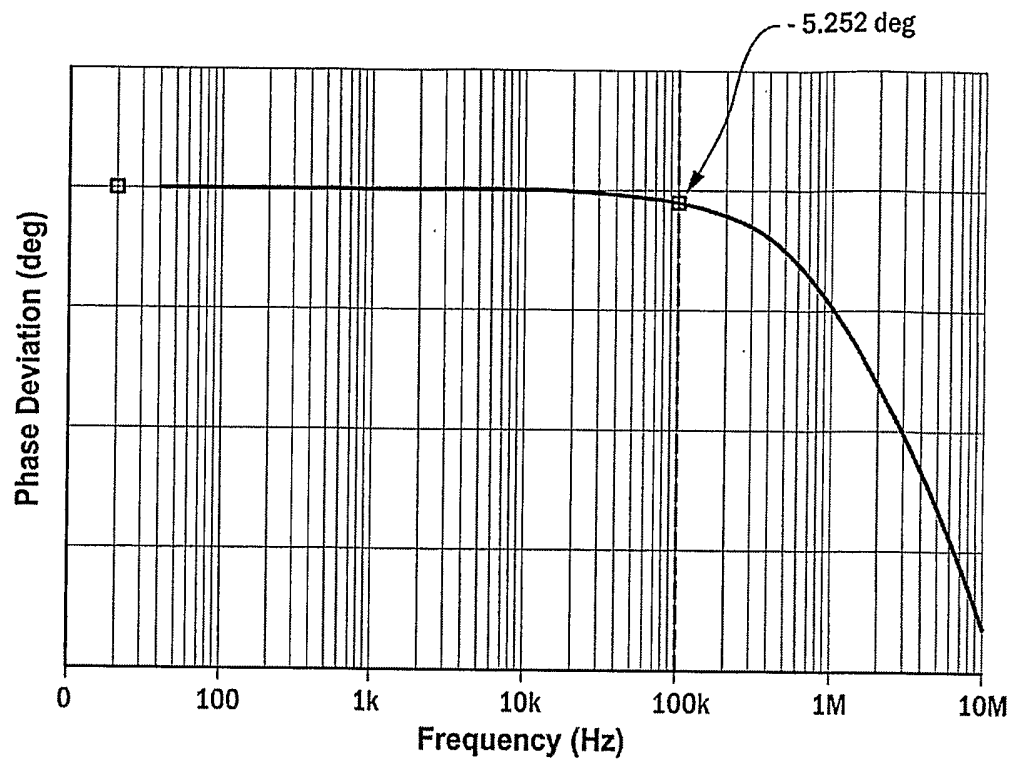


Fig. 3a

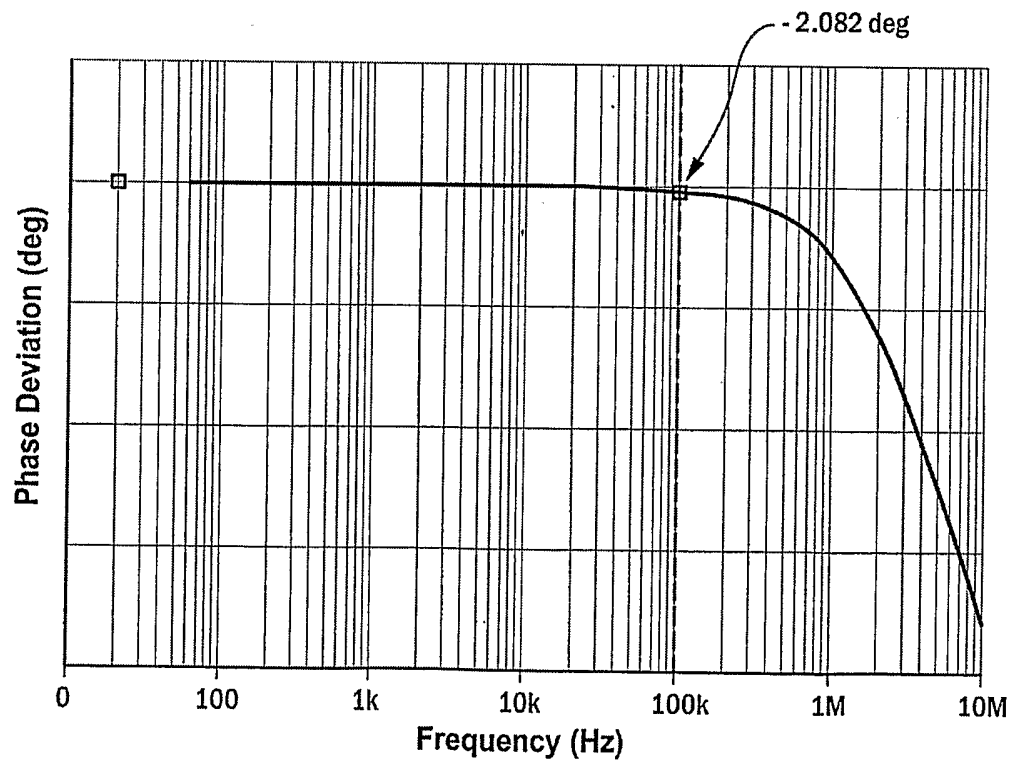


Fig. 3b

4/6

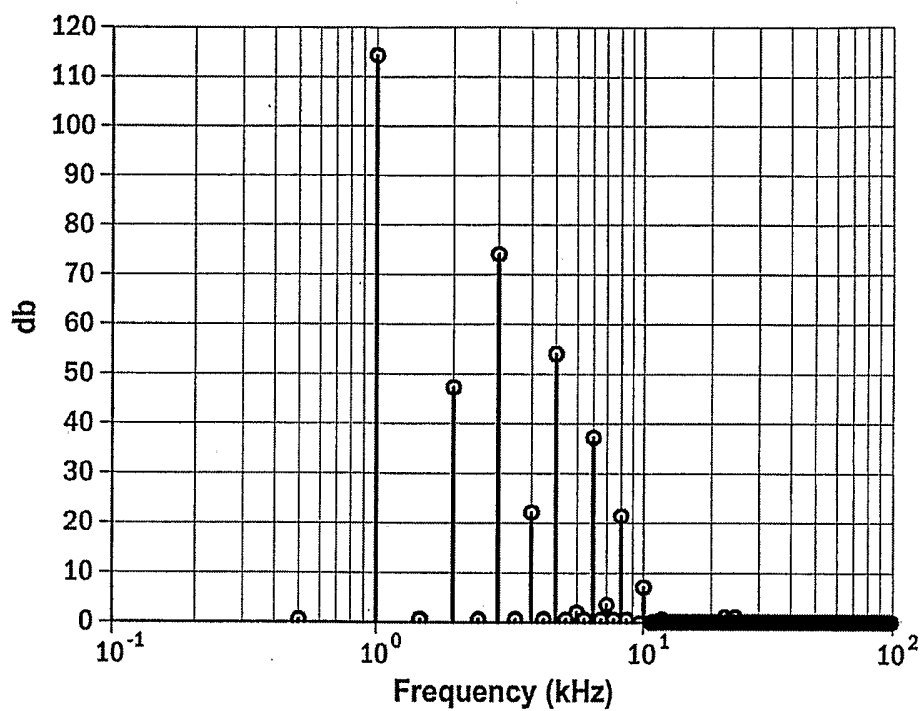


Fig. 4a

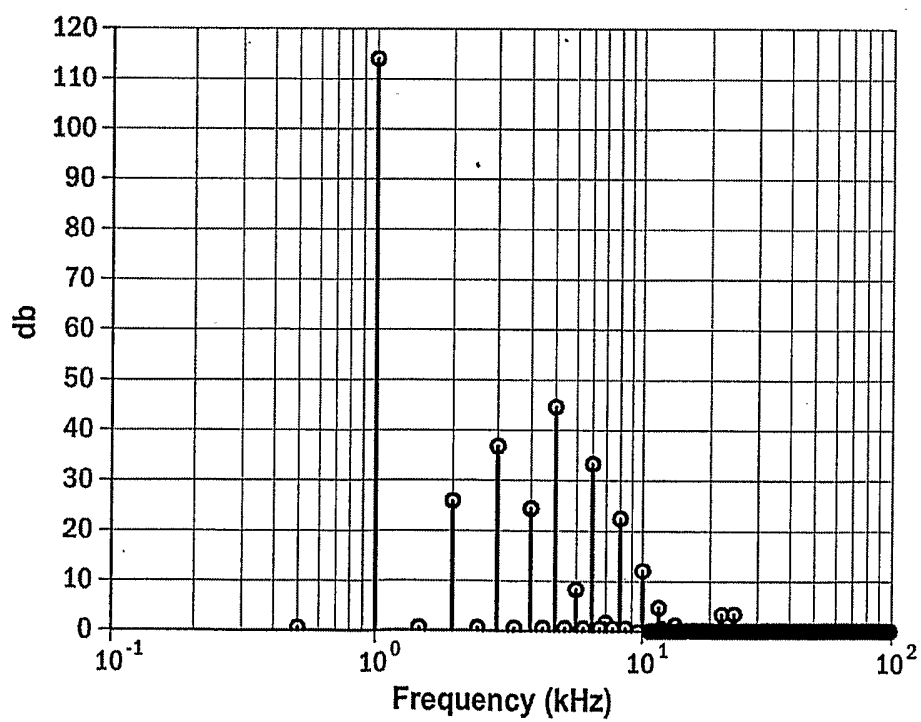


Fig. 4a

5/6

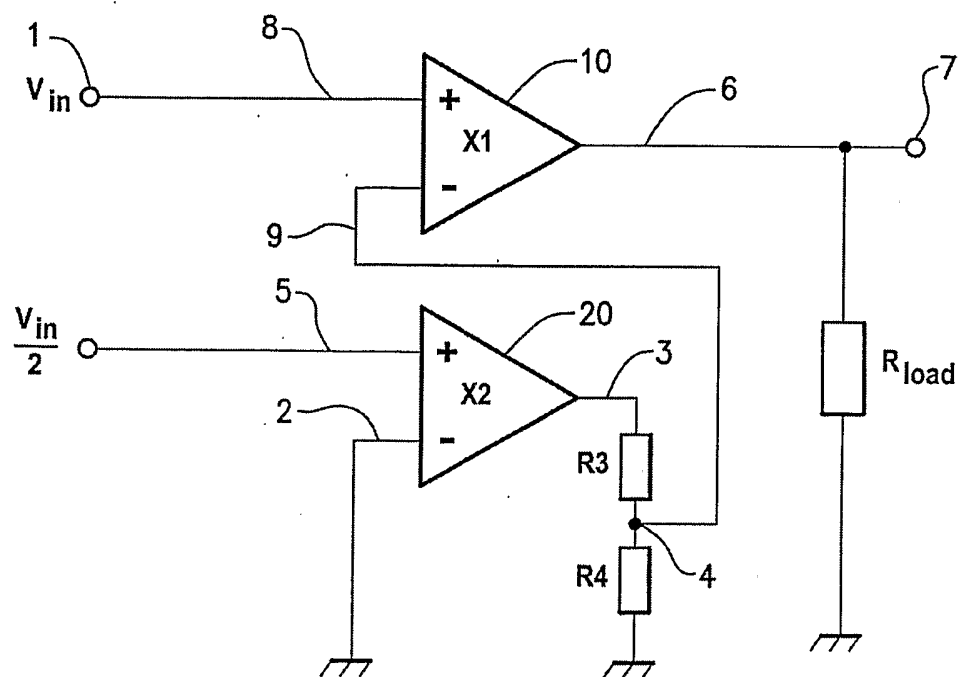


Fig. 5

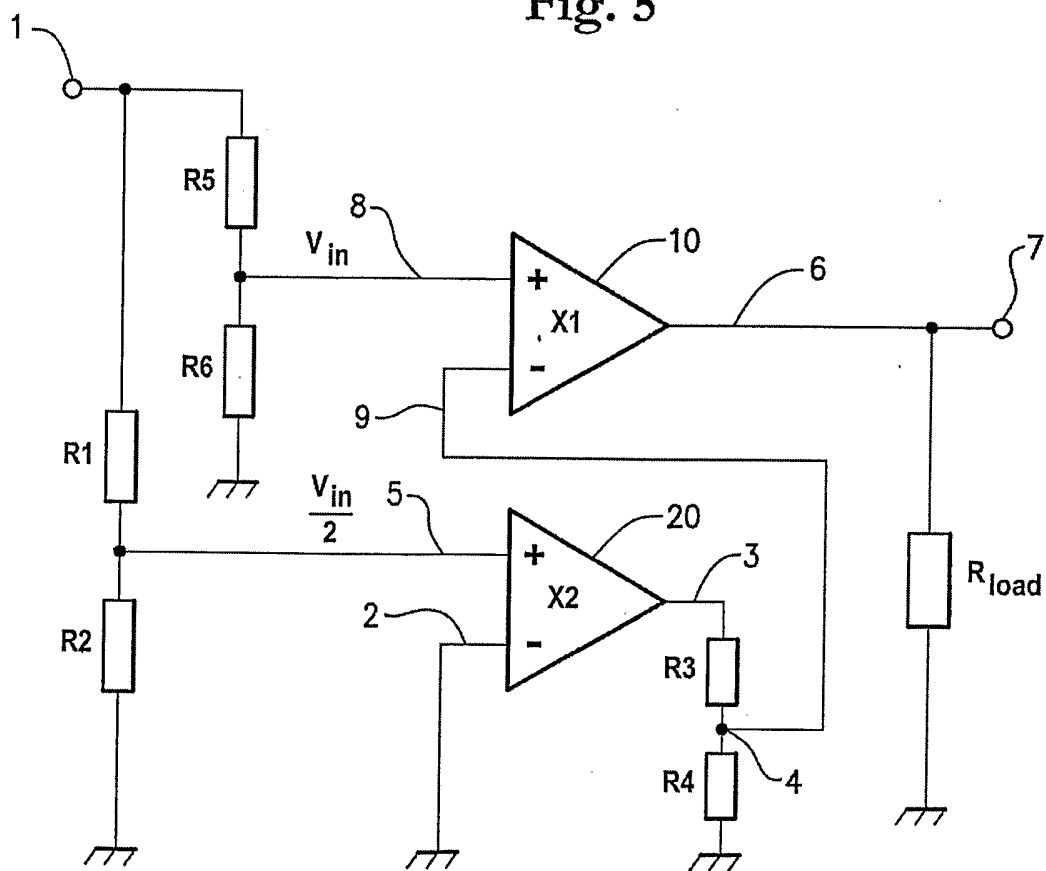


Fig. 6

6/6

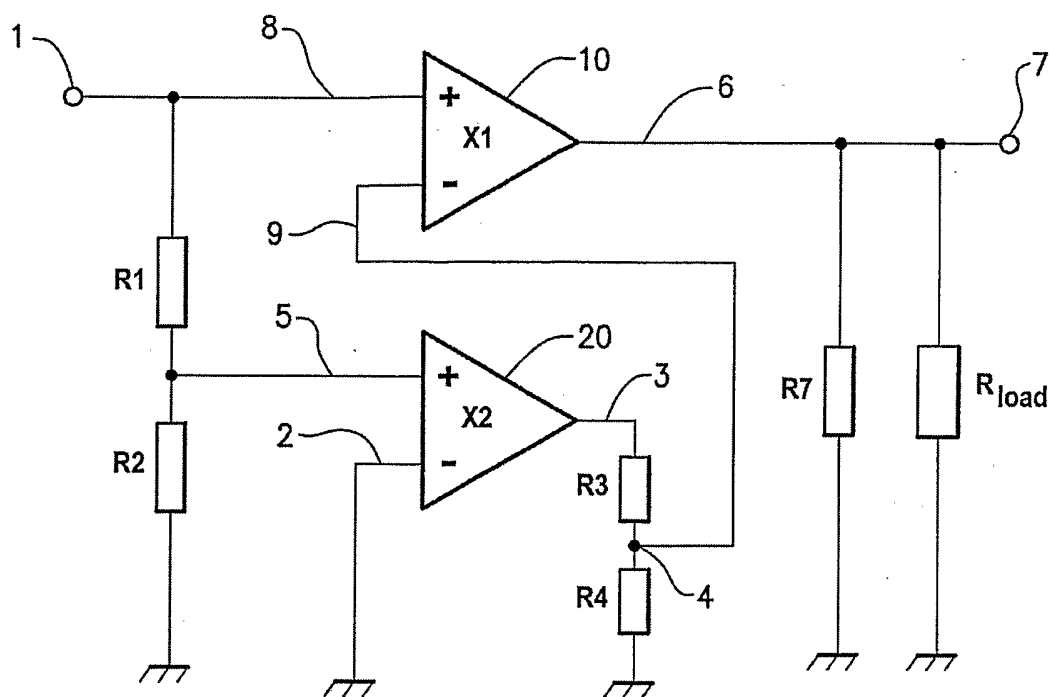


Fig. 7

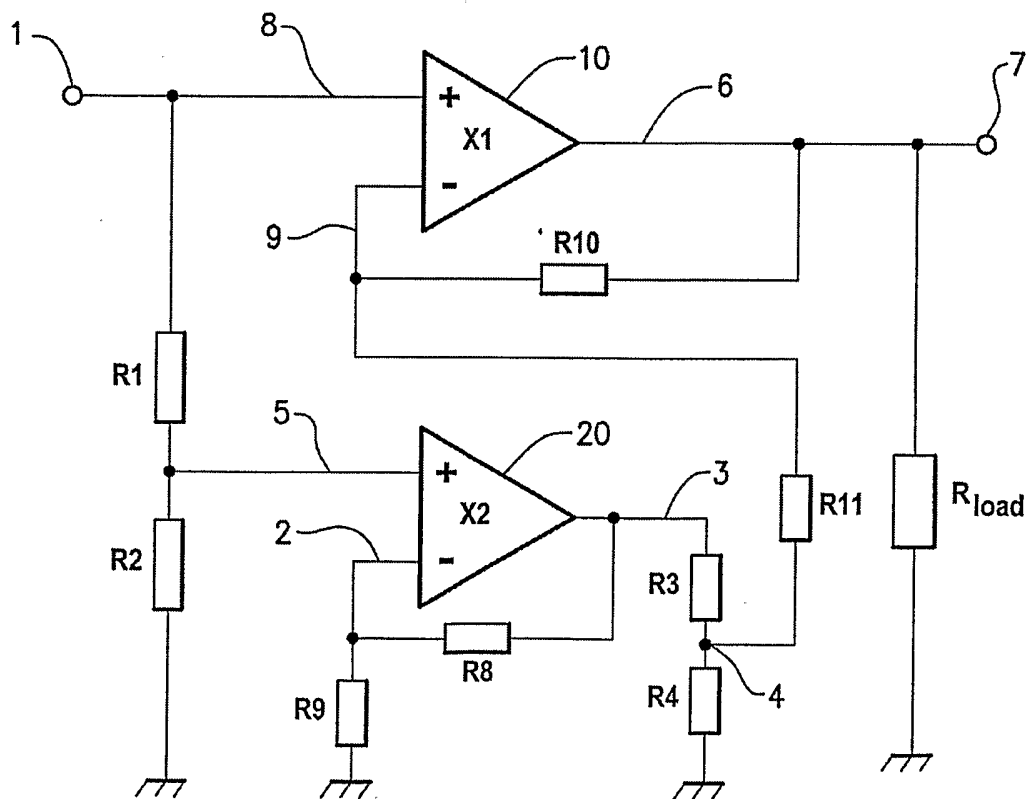


Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2005/000363

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. ⁷: H03F 1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI,USPTO,GOOGLE SCHOLAR,IEEE XPLORE (amplifier, distortion, divider, subtract, cancel and like terms)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/0184373 A1 (CAMERON et al.) 2 October 2003 Abstract, claims 1-4	1
A	US 4628278 A (BOTTMAN) 9 December 1986 Abstract, figures, column 9 lines 36-44	1
A	US 2002/0097090 A1 (SMEDEGAARD-PEDERSEN et al.) 25 July 2002 Abstract, figures 6,7, sections [0072],[0073], claim 20	1
A	US 6057731 A (GORCEA et al.) 2 May 2000 Abstract, Fig. 2A, claims	1



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
8 November 2005

Date of mailing of the international search report
16 NOV 2005

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2005/000363

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US	2003184373	US	6788140
US	4628278	EP	0168123
US	2002097090	US	6476674
US	6057731	US	6137359

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX