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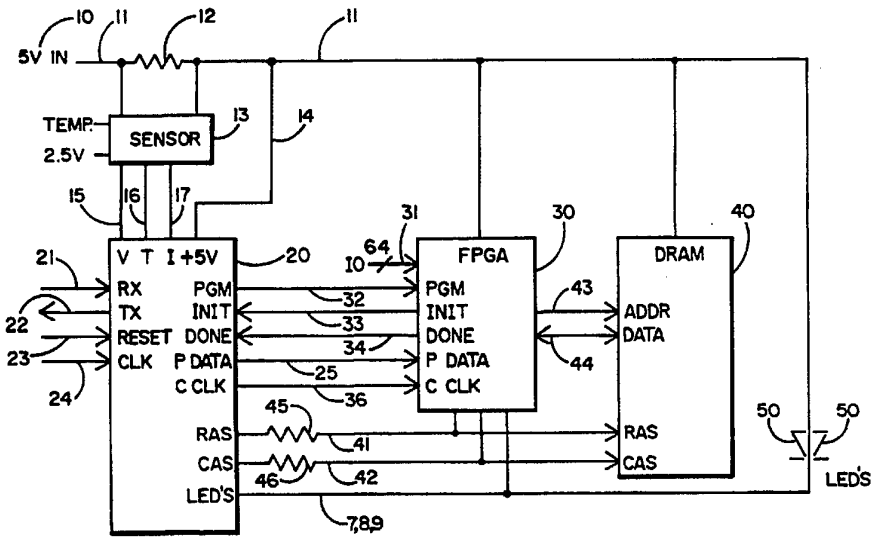

(57) Abstract

A monitor CPU (20) includes inputs for sensors (13) to measure selected environmental conditions and a connection to a semiconductor device that can temporarily disable the device in case an unacceptable environmental condition is detected. This is particularly useful where the semiconductor device is in a field programmable gate array (FPGA). The monitor CPU can be loaded with a unique identification number to allow communication over a bus and in turn use that as a means for a host to selectively access the connected semiconductor device. The monitor CPU (20) can be connected to DRAM (40) which ordinarily also is connected to and controlled by a semiconductor device, such as an FPGA (30). During certain periods when the device (FPGA) (30) is unavailable the monitor CPU (20) can initiate a DRAM (40) refresh circle as needed. The monitor CPU (20) can be connected directly to the program pin(s) of an (FPGA) (30) for controlling the configuration state of the FPGAS (30).

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MONITOR CPU FOR A LOGIC DEVICE

Field of the Invention

This invention relates to a monitor CPU to be used in conjunction with one or more FPGAs. In particular, this invention relates to using a small, general purpose CPU to monitor environmental conditions which may affect an FPGA and to modify the system environment when needed to protect the FPGA.

Background of the Invention

A wide variety of semiconductor logic devices are in use today in an overwhelming variety of applications. Each device, however, is designed to operate under certain environmental conditions and if those conditions are not present, operating the device can lead to inaccurate output or perhaps damage to the device. This is particularly true for programmable logic devices, which can be configured in a wide range of electrical characteristics.

A variety of programmable, configurable semiconductor devices have been designed sold in volume since about 1984. One interesting class of such devices are field programmable gate arrays (FPGAs). Such devices are manufactured by a variety of vendors, notably including Xilinx Corporation, San Jose, California.

FPGAs have been used in a wide variety of applications. See, for example, United States Patent Nos. 5,077,451 (Mohsen, assigned to Aptix Corporation), 5,036,473 (Butts, et al., assigned to Mentor Graphics Corporation) and 5,109,353 (Sample, et al., assigned to Quickturn Systems, Incorporated).

One particularly interesting application for FPGAs is described in detail in co-pending, commonly assigned patent application Serial No. 08/415,750, filed April 3, 1995, which is a continuation of Serial No.

07/972,933, filed November 5, 1992, entitled "SYSTEM FOR COMPILING ALGORITHMIC LANGUAGE SOURCE CODE FOR IMPLEMENTATION IN PROGRAMMABLE HARDWARE." The current application, Serial No. 08/415,750 is incorporated herein in full by reference.

FPGAs provide a designer with a wide variety of interesting functionality and features. However, it is possible to configure an FPGA with certain logic combinations which under certain conditions may drive the FPGA beyond its physical limits and can damage, even destroy, the FPGA. For example, it is possible to program many, if not all, input and output pins in a typical FPGA. If, for example, 64 I/O pins are set low but then shorted to +5V, this can cause a 3-amp current flow into the FPGA. Dissipating 15 watts of power causes the FPGA package temperature to rise and, if left unchecked, can heat the part above 150° C which can destroy the part.

Summary of the Invention

The present invention provides a monitor CPU with inputs for sensors to measure selected environmental conditions and a connection to a semiconductor device that can temporarily disable the device in case an unacceptable environmental condition is detected. This is particularly useful where the semiconductor device is a field programmable gate array (FPGA). The present invention also provides for a monitor CPU which can be loaded with a unique identification number to allow communication over a bus and, in turn, use that as a means for a host to selectively access a connected semiconductor device. The present invention further provides for connection of the monitor CPU to DRAM which ordinarily also is connected to and controlled by a semiconductor device, such as an FPGA. During certain periods when the device (FPGA) is unavailable, the monitor CPU can initiate a DRAM refresh cycle as needed. The present invention further provides for the monitor CPU to be connected directly to the program pin(s) of an FPGA for controlling the configuration state of the FPGA.

One object of the present invention is to provide an interface with a unique ID for a semiconductor device, in particular a programmable device. This interface can isolate the semiconductor device from a host system and provide controlled access to specific functions of the semiconductor device. For example, the interface can isolate a programmabie logic device from the host system and provide controlled access to programming functions of the programmable logic device.

Another object of the present invention is to provide an environmental monitor that can detect potentially dangerous operating environmental conditions and can shut down or isolate a relatively semiconductor part until a safe operating environment can be provided. Still another object of the present invention is to provide a reporting device which reports the environment conditions of the semiconductor part.

Yet another object of the present invention is to provide a backup refresh monitor for DRAM normally controlled by a semiconductor device so as to maintain the DRAM even if the semiconductor device is temporarily unable to refresh the DRAM.

These and other objects of the invention will be described more fully below. One skilled in the art will appreciate that the description of the preferred embodiments is not limiting and many other embodiments of the invention can be implemented by one skilled in the art.

Brief Description of the Drawings

Figure 1 illustrates a monitor CPU in a system including an FPGA, DRAM, and host system I/O.

Figures 2A and 2B illustrate a circuit for current monitoring.

Figure 3 illustrates a circuit for a voltage monitor.

Figure 4 illustrates a circuit for a temperature monitor.

Figures 5A and 5B illustrate connections to a first and to a second monitor CPU.

Figure 6 illustrates a three-color, RGB light-emitting diode.

Detailed Description of the Invention

The monitor CPU of this invention provides several useful benefits for connecting a system to an FPGA. These include providing a ready means to identify a specific FPGA for programming purposes, a means to control and facilitate programming the FPGA, and a means to monitor the environment and protect the FPGA.

Referring to Figure 1, in one preferred embodiment, Vcc source **10** provides +5V input along rail **11**. A representative sensor **13** is connected across resistor **12**. Sensor lines **15**, **16** and **17** connect sensor **13** to monitor CPU **20**. The connection of monitor CPU **20** (and other devices) to Vss is not shown but understood. Power lead **14** connects rail **11** to the power input of monitor CPU **20**. Monitor CPU **20** is also connected to a host system (not shown) through receive line (RX) **21**, transmit line (TX) **22**. Monitor CPU **20** receives a reset signal (e.g., PIC_RESET, see Figure 5A) from the host over line **23** and a host clock (e.g., PIC_Clk, see Figure 5A) over line **24**.

An FPGA **30** is connected through I/O bus **31** to the host (again, not shown). Here, I/O bus **31** is 64 bits wide, but one skilled in the art can select a variety of useful bus sizes. This configuration is particularly useful with a programmable bus, such as one or more of those described in United States Patent Application Serial No. 08/415,750 (noted above, incorporated herein in full by reference). Lines **32**, **33**, **34**, **35** and **36** connect monitor CPU **20** and FPGA **30** as shown to carry program enable (PGM), initialize (INIT), done, program data (PDATA) and Configure Clock (CClk) signals, respectively, as shown. In many instances, it is useful to connect memory; such as DRAM **40** to FPGA **30**. Address lines **43** carry address information from FPGA **30** to DRAM **40** and data lines **44** carry data between these devices. In a preferred embodiment, DRAM **40** is divided into two banks (only one shown). The

size of each bus is device and system-specific, but selection of these parameters is well within the skill of an average artisan. DRAM RAS and CAS can be driven over lines **41** and **42** (through resistors **45** and **46**), respectively, by either FPGA **30** or monitor CPU **20**. Similarly, one or more LEDs **50** can be driven over LED lines **7**, **8** and **9** by either FPGA **30** or monitor CPU **20**. In one preferred embodiment, one LED **50** is an RGB LED capable of providing a wide variety of colors depending on the respective red, green and blue signals on LED lines **7**, **8** and **9**. In one particularly preferred embodiment, most of these elements are replicated with a second FPGA connected to a second monitor CPU, connected in turn to a second sensor unit and to the host system. The first and second FPGA may be connected to each other through one or more programmable connections, but the details of those connections are not the subject of this invention.

A module including many of these components, but not a monitor CPU, is described in considerable detail in commonly assigned, co-pending application 08/415,750. The present invention is particularly useful in the module or modules described in that patent application.

A variety of devices can be used for a monitor CPU. In general, an 8-bit CPU such as an 8051 is particularly useful. One or more analog to digital converters on inputs to the CPU allows for use of a variety of input devices.

One preferred monitor CPU device is the PIC16C71, available from Microchip Technology Incorporated, 235 West Chandler Blvd., Chandler, AZ 85224-6199. This device provides many useful features, including a language of 35 single word instructions, 1024 x 14 on-chip EPROM program memory (allowing about 1,000 lines of code to be stored), 36 x 8 general purpose registers (SRAM), 15 special function hardware registers, an 8 level deep hardware stack, plus more, in addition to peripheral-interaction and special microcontroller features. The PIC16C71 includes four interrupt sources, a four-channel A/D converter and eight TTL I/O pins.

The manufacturer provides a number of programming options, including devices with UV-erasable programming, anti-fuse programming, and a variety of in-factory programming methods if desired. Programming such a CPU is not difficult for one skilled in the art. The manufacturer's data book for the PIC16C71 includes dozens of pages including logical description of the part, the op codes and function of instructions for the part, and details about each pin, how to connect it, and how to use it.

Adding a monitor CPU between a host system and a semiconductor device provides a number of useful advantages. These include (1) providing a connection and protocol for communications with the host; (2) providing a place to store a unique device ID for the monitor CPU and, by extension, a device such as an FPGA connected to the monitor CPU.

In a preferred embodiment, some portion of the 1,000 lines of code in the monitor CPU are dedicated to a primary event loop which tests the status of each selected input and, depending on the result, drives signals on selected outputs. Each analog input can sample at 100KHz. Thus each analog input can be polled at a rate of 100KHz, although with four analog inputs and a variety of other inputs, plus servicing any request when needed, a more typical time for monitoring each particular input is about 10KHz. This provides more than enough time to initiate corrective action when input conditions warrant.

Since the monitor CPU is programmable, it can be programmed to use one or more conventional communication protocols. Using a simple two-line method of communication, lines **21** and **22** for RX and TX will support a number of known communication protocols. These include:

1. RS232, for example from 300-19,200 baud
2. Up to about 500K baud using RS232-type protocols
3. I^2C protocols.

Each of these well-known, standard protocols uses only two lines for communication.

By using a standard programming interface, the monitor CPU and connected hardware become just another layer to the host system. This also favors and facilitates using a standard command set within the system. This sort of programmable communication provides for a flexible yet universal interface, which is important in many stand-alone applications which might take advantage of the hardware device(s) connected to a monitor CPU.

The monitor CPU can be connected to other devices in a variety of ways. One skilled in the art can select how many and which lines might be connected to another part. In the preferred embodiment illustrated in Figure 1, monitor CPU **20** is connected to send program enable (PGM), PData and Configure Clock (CClk) signals to FPGA **30**. FPGA **30** is connected to send INIT and DONE signals to monitor CPU **20**.

One or more of the EPROM locations or hardware registers can be loaded with an identification number unique to that monitor CPU. The number may be simply a unique serial number. The number might include some information about devices connected to the monitor CPU, for example, encoded information that the monitor CPU is connected to a Xilinx XC4010 FPGA and 2 megabytes of DRAM (in a selected configuration) and that a certain type of sensor is connected to the monitor CPU. The information could include some sort of model number (according, for example, to a company manufacturing modules containing a monitor CPU).

The identification number(s) can be used by the host system. For example the host can scan any connected modules and ascertain from the encoded numbers what sort of resources are connected and available. This might be achieved by polling any connected modules, downloading configuration information from each connected module, then, for example, preparing a database with information from the polling arranged in some useful way.

A unique device ID can be used as an identification address to direct host-slave communications to a specific monitor CPU, and then to downstream devices such as an FPGA. This sort of addressing is quite

well known in packetized communication as is commonly used in modern PC buses.

Since the monitor CPU can include some instructions stored internally, these instructions can include boot instructions which might be only for the monitor CPU but also might include boot instructions for any connected devices. Such boot instructions might include memory initialization of the module DRAM's. They might also include some basic configuration information for a connected FPGA. The monitor CPU could be connected to a ROM, e.g., an EEPROM, containing some form of configuration information, and the monitor CPU could be programmed to access that configuration information and use it to program and configure an attached FPGA or other connectable components. These and other schemes can be used to provide basic configuration information that can be used to bring the system up in a known state, even if the system is not connected to an external host of any sort.

The system also can be initialized, then controlled by a host system to provide one or more FPGA configurations. For example, a host system could use conventional bus arbitration and communication methods to deliver a request to the monitor CPU to initialize and program a connected FPGA. The program or configuration commands might be available within the monitor CPU programmed memory, within an ROM accessible to the monitor CPU, or may be transmitted by the host system and forwarded by the monitor CPU to the FPGA.

A variety of useful sensors is provided by using the analog inputs of the monitor CPU. These include an environment temperature probe, a Vcc level probe, and an input current probe for each of two semiconductor devices. Referring to Figure 3, the voltage reference can be an LM431D from National Semiconductor, Santa Clara, California. This device provides a ratiometric output comparing the input voltage to a reference voltage. In one preferred embodiment, the reference voltage is 2.5V. The output VREF of the LM431D is equal to

$$\frac{V_{known\ input}}{Vcc}$$

This is input to VREF, pin 18 of monitor CPU HUP ("H" (m)microProcessor) shown in Figure 5B. There, as an analog input, the analog value of VREF is compared to a range of 0-5 volts and digitized to one value of 255. The monitor CPU can invert the input value, then divide by Vknown of +2.5V to deliver the actual input voltage as the result. The actual input voltage can be compared to a pre-set reference (which might, for example, be stored in one of the hardware registers of the monitor CPU) and the monitor CPU can make that comparison with each cycle of the main event loop and can direct appropriate action if the comparison is outside of pre-set limits.

Referring to Figure 4, a temperature monitor can be made using an LM34D, from National Semiconductor. This device puts out 10mV/°F, so a value of 1.0V corresponds to 100°F. The LM34D output TEMPERATURE is connected to a corresponding input on pin 18 of monitor CPU XUP, shown in Figure 5A. The input is compared to a range of 0-5 volts, then digitized to one value of 255. As described above for the voltage sensor, a threshold value can be stored in a hardware register. As one stage of the main event loop, the program running in the monitor CPU can compare the input value to the stored threshold and can direct appropriate action if the comparison is outside of pre-set limits. The temperature monitor can be positioned in a variety of locations to provide information about temperature where it is most important.

A current sensor can be made in a variety of ways. By way of background, in one preferred implementation, two monitor CPUs are used in conjunction with two FPGAs and two DRAMs, each composed of two banks. Three copies of Vcc are provided, each independently delivered from the power supply. These copies are Vcc (system), Vcc (FPGA.1) (supplying FPGA.1, the "X" FPGA, and DRAM.1) and Vcc (FPGA.2) (supplying FPGA.2, the "H" FPGA, and DRAM.2).

Referring to Figures 2A and 2B, dual diff amps LMC6842D (by National Semiconductor) each monitor one current flow. The Vcc X.FPGA and Vcc (system) are connected across sense resistor R5, and the difference between each leg and ground is compared in diff amp 60

to deliver output XPGA_CURRENT. This in turn is directed to pin 17 of the XUP monitor CPU. The diff amp circuit is selected to deliver a signal of 1V for each ampere of current flowing through Vcc (FPGA.1). The 0-5V input is digitized to one of 255 values to indicate a current of 0-5 amps. In a similar manner, the Vcc H.FPGA and Vcc (system) are connected across load resistor R10, and the difference between each leg and ground is compared in diff amp **61** to deliver output HPGA_CURRENT. This in turn is directed to pin 17 of the HUP monitor CPU.

The actual input voltage can be compared to a pre-set reference (which might, for example, be stored in one of the hardware registers of the monitor CPU) and the monitor CPU can make that comparison with each cycle of the main event loop and can direct appropriate action if the comparison is outside of pre-set limits.

Note that the differential op amps are connected rail to rail. Power to the part is taken across Vcc (system) at pin 8 to ground at pin 4 (See Figure 2B). Since the sense resistor is also connected rail to rail, this allows the differential op amp to compare small differences on each leg of the sense resistor to derive an accurate value for current. This allows for an amplification factor of 100 [50mV across 10 milliOhms].

These current detectors do not provide a detailed value for current (255/5 = 51.2 steps per amp) but do provide a useful monitor of gross changes in current flow. An FPGA such as a Xilinx XC 4010 should draw approximately 0.5 amp when active (typical values). For certain circuits, this might rise to about 1 amp under some conditions. The condition of concern here is an unanticipated condition, such as two separate programmable parts trying to drive a signal in opposite directions at the same time (one driving high, one driving low) -- in effect a shorted wire. This condition can easily draw about 100 milliamps per pin, and when taken together as, say, a **32** line bus, this can cause a current draw of 3.2 amps. In addition, if during operation a significant number of lines are transitioning at high rates, this can lead to large current flows. Such a high current, however, will cause a rapid buildup of heat in the FPGA and can lead to permanent damage to or destruction

of the part. By monitoring the current flowing through an FPGA, the monitor CPU can initiate an appropriate action to isolate or turn off the FPGA until the current flows return to acceptable limits.

The monitor CPU can be connected to an FPGA to provide several useful functions. The PGM signal (line **32** in Figure 1) allows the monitor CPU to pull a program enable line low to initialize the FPGA. When the line is released, the FPGA is ready to be programmed. In one preferred embodiment, when a monitor CPU is reset, the PGM line floats low.

Although this line would normally be driven low only when initializing the FPGA, this provides a convenient escape mechanism to shut down the FPGA to avoid a runaway or other potentially destructive condition. For example, if the monitor CPU detected an excessive increase in current drawn by an FPGA, or perhaps an unacceptable rise in temperature near the FPGA, the monitor CPU could assert PGM to shut down the FPGA to protect it from damage. Of course, this would compromise, and in general destroy, the configuration of the FPGA, but an operator would probably want to modify any preexisting configuration that allowed the runaway condition to arise. Where a DRAM is also connected to the monitor CPU and the FPGA, the monitor CPU can preserve the state of the DRAM under certain conditions so that the state of the FPGA, or at least certain stored memory values, can be accessed for analysis of the FPGA state before the runaway condition.

The INIT signal (line **33**) is driven by the FPGA, usually to request a wait before sending configuration data (usually less than about 2 milliseconds). This line can also be used so the FPGA can indicate an error, for example, detecting that bad data has been shifted into the FPGA (detected by CRC). The DONE signal (line **35**) is also driven by the FPGA and is set TRUE when the FPGA has been loaded with all configuration data. The PDATA line (line **35**) carries FPGA configuration program data. This configuration data might be communicated by a host to a monitor CPU, then shifted serially into the FPGA. In one preferred embodiment, both monitor CPUs (X and H) and FPGAs (X and H) are connected to a single PDATA line and the monitor CPUs control the chip select (PGM) to program each FPGA individually. The PDATA line can

also be driven by an FPGA under certain conditions, e.g., to provide status information. The CClk configuration clock signal (line **36**) is used to strobe program data into an FPGA. CClk does not necessarily have to come from the same monitor CPU that is providing PDATA, and in general it may be preferable to drive CClk at a different rate than the normal clock for a monitor CPU. In some circuits, an FPGA can provide its own configuration clock signal.

In one preferred embodiment, an FPGA is connected to an associated DRAM or bank of DRAM devices. This is helpful to provide memory resources directly to an FPGA. In such a circuit, RAS and CAS for DRAM are normally sourced by the connected FPGA. However, at certain times, the FPGA may not be available to drive RAS and CAS. Referring to Figure 1, monitor CPU **20** line RB4 is connected to series resistor **45** and line RB5 is connected to series resistor **46** so that monitor CPU **20** is weakly coupled to DRAM **40**. Resistors **45**, **46** are preferably about 1 KOhm. Thus, if corresponding FPGA lines are tristated, monitor CPU **20** can drive RAS and CAS as needed, generally less than or equal to about every 16 microseconds. This can be included in the main event loop (or a secondary event loop) in the program for monitor CPU **20**. This refresh is particularly useful before FPGA **30** has been configured to include a circuit to provide RAS and CAS. This monitor CPU-driven refresh is also useful when, for example, FPGA **30** must be temporarily disabled due to some environmental condition that would damage the FPGA if it continued to operate. Once the FPGA is configured and operating conditions are appropriate, it can take over sourcing RAS and CAS refresh signals. By driving lines **41**, **42** directly, FPGA **30** can swamp the effect of any drive from monitor CPU **20** so FPGA **30** can guarantee RAS and CAS signals whenever FPGA **30** is running normally but can allow monitor CPU **20** to guarantee that RAS and CAS will always be available.

Referring to Figures 1 and 6, LED **50** may be any of a variety of LED output devices, including, in one preferred embodiment, an RGB LED. The lines PIC_RED_, PIC_BLU_, and PIC_GRN_ can be buffered (not shown) or driven directly. However, the blue-colored LED particularly prefers to be buffered, drawing up to about 50 mA. By contrast, red

and green LEDs need only 2 mA and 10 microAmp, respectively. If each color is driven at a selected rate, the overall color of the output can be modified to select one of about 4,000 colors. The human eye detects color at about 20Hz. By feeding the LED at selected rates up to about 1 KHz a wide range of display colors is available. For example, if red and green are driven at comparable rates, the output color is yellow. If a green LED is driven at about 100 Hz while a corresponding red LED is driven at about 10Hz, the resulting color is a reddish green. The LED can be connected simultaneously to the monitor CPU and FPGA so the LED can be driven by either source.

The present invention has been described in terms of certain preferred embodiments but one skilled in the art will recognize a variety of alternative embodiments which come within the teachings of this invention.

WHAT IS CLAIMED

1. A real time monitor for a semiconductor device comprising
a semiconductor device, capable of operating in a first, normal state, and capable of operating in a second, modified state,
a monitor CPU connected to the semiconductor device,
a sensor connected to said monitor CPU to provide information about an
environmental condition that may impact said semiconductor device, and
a connection between said monitor CPU and said semiconductor device which can be used to put the semiconductor device into said modified state when said sensor detects a selected environmental condition.

2. The real time monitor of claim 1 wherein said sensor is a temperature detector.

3. The real time monitor of claim 1 wherein said sensor detects the supply voltage to said semiconductor device.

4. The real time monitor of claim 1 wherein said sensor detects the supply current to said semiconductor device.

5. The real time monitor of claim 1 wherein said semiconductor device is a field programmable gate array (FPGA).

6. The real time monitor of claim 5 wherein said first, normal state is a typical operating state for said FPGA and said second, modified state shuts down said FPGA by controlling the program input of the FPGA.

7. The real time monitor of claim 5 further comprising a host system connected to said monitor CPU, said host system including a system reset line which, when asserted, causes the monitor CPU to reset the FPGA to be returned or initialized to a known, safe state.

8. The real time monitor of claim 7 further comprising a communications channel between said host system and said monitor CPU and means for said monitor CPU to report monitor conditions to said host system.

9. The real time monitor of claim 5, further comprising an optical indicator connected to said monitor CPU capable of indicating the status of any environmental condition as measured by said sensor.

10. The real time monitor of claim 1 further comprising a first sensor to monitor temperature, a second sensor to detect the supply voltage to said semiconductor device and third sensor to detect the supply current to said semiconductor device, each of said first, second and third sensors connected to said monitor CPU.

11. The real time monitor of claim 1 further comprising a DRAM device with RAS and CAS inputs connected to each of said semiconductor device and to said monitor CPU wherein said monitor CPU can detect whether or not said semiconductor device is providing sufficiently frequent RAS and CAS signals to the DRAM and, if not, said monitor CPU can provide RAS and CAS signals to the DRAM so as to maintain the DRAM's memory state.

12. A programming interface comprising

a monitor CPU,

a programmable semiconductor device connected to said monitor CPU such that said monitor CPU can program the configuration state of said programmable semiconductor, and

a source of configuration information and control signals to direct the monitor CPU to program said programmable semiconductor device with said configuration information.

13. The programming interface of claim 12 wherein said source of configuration information and control signals is a host system connectable to said monitor CPU.

14. The programming interface of claim 12 wherein said source of configuration information is memory accessible to said monitor CPU and said source of control signals is program information accessible to said monitor CPU so that said interface monitor can boot up after a restart command and the control signals in the program information will instruct the monitor CPU to access the configuration information and program said programmable semiconductor device with said configuration information so that said programmable semiconductor device will be initialized to a known state.

15. The programming interface of claim 12 further comprising a programmable communication channel in said monitor CPU to provide communication with an external device.

16. The programming interface of claim 15 further comprising information stored in said monitor CPU, said information comprising information about said monitor CPU.

17. The programming interface of claim 16 wherein said information comprises a serial number identifying said monitor CPU.

18. The programming interface of claim 16 wherein said information comprises information about said programmable semiconductor device connected to said monitor CPU.

19. The programming interface of claim 16 further comprising an additional device connected to said monitor CPU and wherein said information comprises information about said additional device.

AMENDED CLAIMS

[received by the International Bureau on 14 October 1996 (14.10.96);
original claims 1-5, 10 and 11 amended; new claims 20-21 added;
remaining claims unchanged (4 pages)]

1. A real time monitor for a semiconductor device comprising

a reprogrammable semiconductor device, capable of accepting user-generated configuration data which may induce device-damaging current flow, capable of operating in a first, normal state, and capable of operating in a second, modified, low power state, and a third, out-of-bounds state,

a monitor CPU connected to the reprogrammable semiconductor device,

one or more sensors connected to said monitor CPU to provide information about a plurality of conditions, any one or more of which may indicate that said reprogrammable semiconductor device is operating in said third, out-of bounds state, potentially damaging said reprogrammable semiconductor device, and

a connection between said monitor CPU and said reprogrammable semiconductor device which can be used to put the reprogrammable semiconductor device into said modified, low power state when one or more of said sensors detects a selected condition.

2. The real time monitor of claim 1 wherein a first of said sensors comprises a temperature detector.

3. The real time monitor of claim 1 wherein a first of said sensors detects the supply voltage to said reprogrammable semiconductor device.

4. The real time monitor of claim 1 wherein a first of said sensors detects the supply current to said reprogrammable semiconductor device.

5. The real time monitor of claim 1 wherein said reprogrammable semiconductor device is a field programmable gate array (FPGA).

6. The real time monitor of claim 5 wherein said first, normal state is a typical operating state for said FPGA and said second, modified state shuts down said FPGA by controlling the program input of the FPGA.

7. The real time monitor of claim 5 further comprising a host system connected to said monitor CPU, said host system including a system reset line which, when asserted, causes the monitor CPU to reset the FPGA to be returned or initialized to a known, safe state.

8. The real time monitor of claim 7 further comprising a communications channel between said host system and said monitor CPU and means for said monitor CPU to report monitor conditions to said host system.

9. The real time monitor of claim 5, further comprising an optical indicator connected to said monitor CPU capable of indicating the status of any environmental condition as measured by said sensor.

10. The real time monitor of claim 1 wherein a first sensor monitors temperature, a second sensor detects the supply voltage to said reprogrammable semiconductor device and a third sensor detects the supply current to said reprogrammable semiconductor device, each of said first, second and third sensors connected to said monitor CPU.

11. The real time monitor of claim 1 further comprising a DRAM device with RAS and CAS inputs connected to said reprogrammable semiconductor device and to said monitor CPU wherein said monitor CPU can detect whether or not said reprogrammable semiconductor device is providing sufficiently frequent RAS and CAS signals to the DRAM and, if not, said monitor CPU can provide RAS and CAS signals to the DRAM so as to maintain the DRAM's memory state.

12. A programming interface comprising
a monitor CPU,
a programmable semiconductor device connected to said monitor CPU such that said monitor CPU can program the configuration state of said programmable semiconductor, and

a source of configuration information and control signals to direct the monitor CPU to program said programmable semiconductor device with said configuration information.

13. The programming interface of claim 12 wherein said source of configuration information and control signals is a host system connectable to said monitor CPU.

14. The programming interface of claim 12 wherein said source of configuration information is memory accessible to said monitor CPU and said source of control signals is program information accessible to said monitor CPU so that said interface monitor can boot up after a restart command and the control signals in the program information will instruct the monitor CPU to access the configuration information and program said programmable semiconductor device with said configuration information so that said programmable semiconductor device will be initialized to a known state.

15. The programming interface of claim 12 further comprising a programmable communication channel in said monitor CPU to provide communication with an external device.

16. The programming interface of claim 15 further comprising information stored in said monitor CPU, said information comprising information about said monitor CPU.

17. The programming interface of claim 16 wherein said information comprises a serial number identifying said monitor CPU.

18. The programming interface of claim 16 wherein said information comprises information about said programmable semiconductor device connected to said monitor CPU.

19. The programming interface of claim 16 further comprising an additional device connected to said monitor CPU and wherein said information comprises information about said additional device.

20. The real time monitor of claim 1 wherein said out-of-bounds state is a current flow reading at or greater than about 2 amperes.

21. The real time monitor of claim 1 wherein said out-of-bounds state is a temperature reading at or greater than about 150 degrees centigrade.

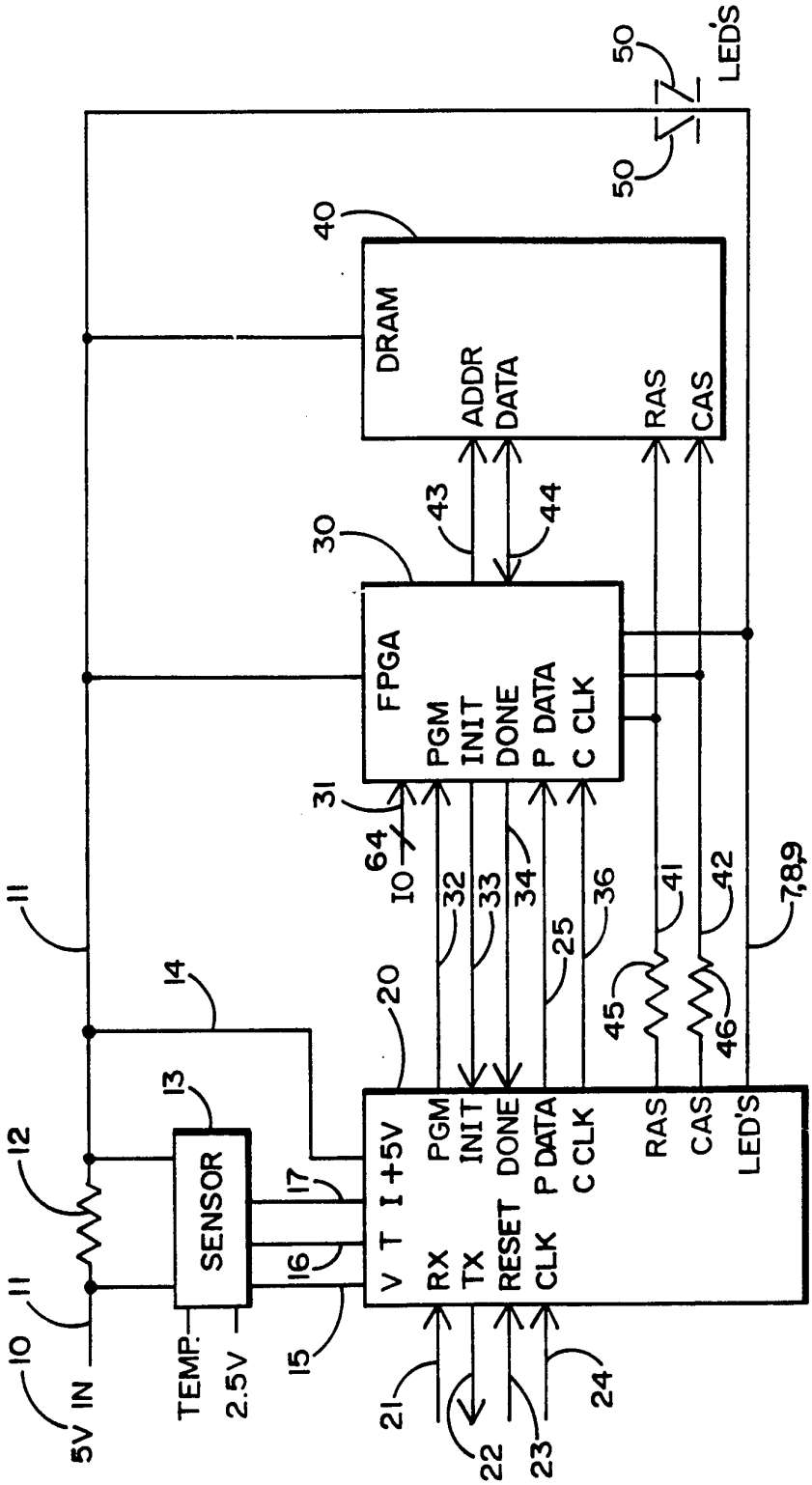
50
LED'S
50
40
DRAM
ADDR
DATA
RAS
CAS
43
44
30
FPGA
PGM
INIT
DONE
P DATA
C CLK
31
64
IO
32
33
34
25
36
41
42
7,8,9
11
14
20
45
46
13
12
SENSOR
17
16
15
V T I +5V
RX
TX
RESET
CLK
PGM
INIT
DONE
P DATA
C CLK
RAS
CAS
LED'S
11
10
5V IN
TEMP.
2.5V
21
22
23
24

FIG. 1

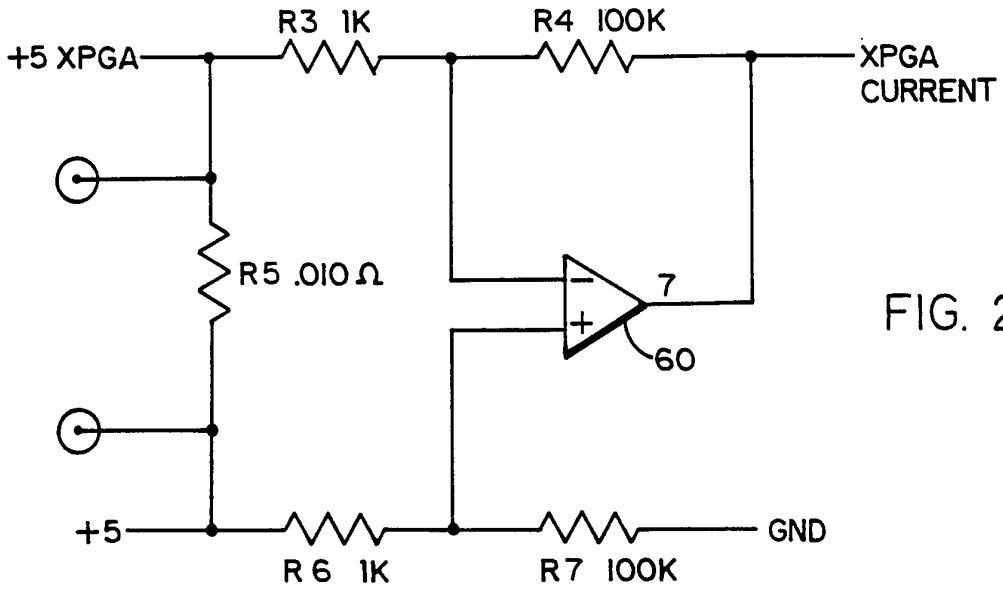

FIG. 2a

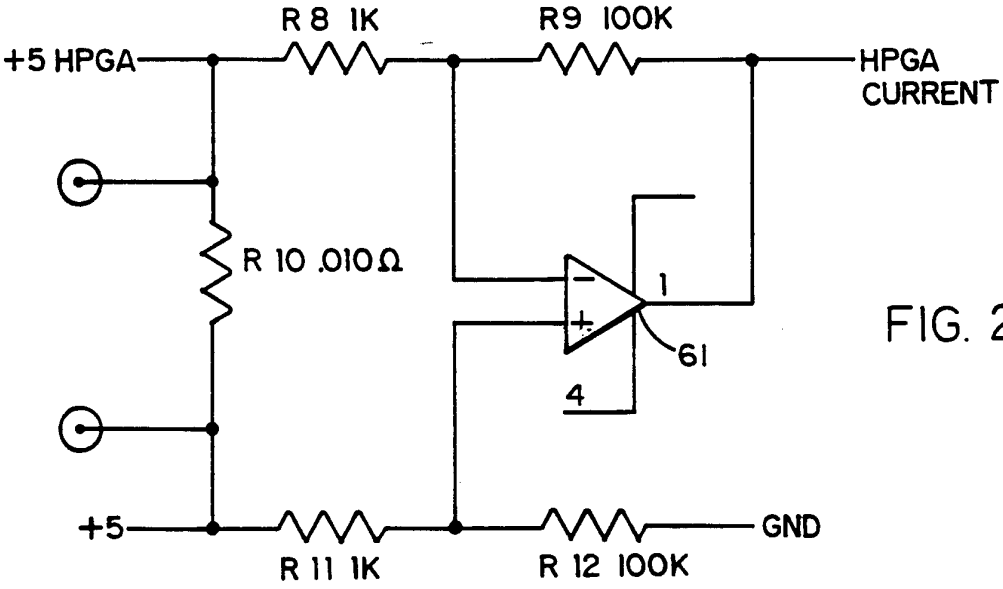

FIG. 2b

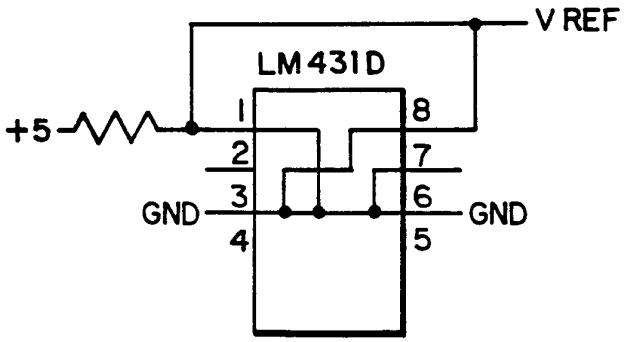

FIG. 3

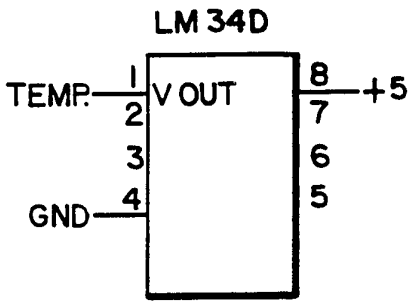

FIG. 4

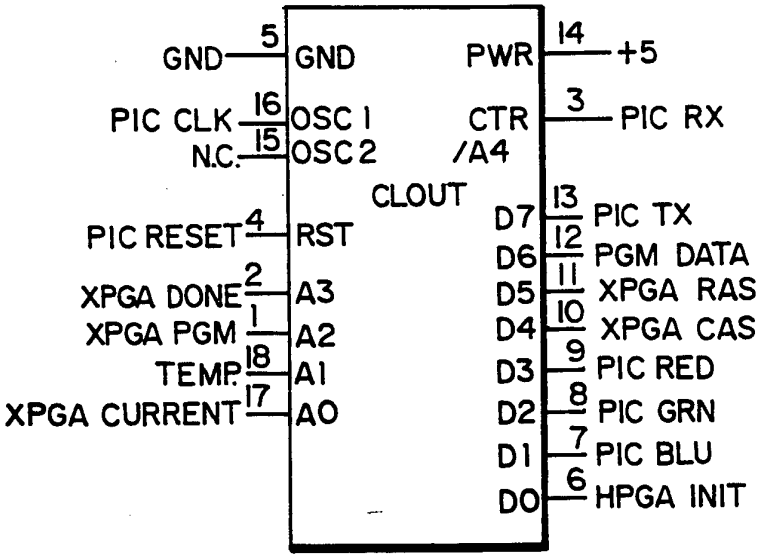

FIG. 5a

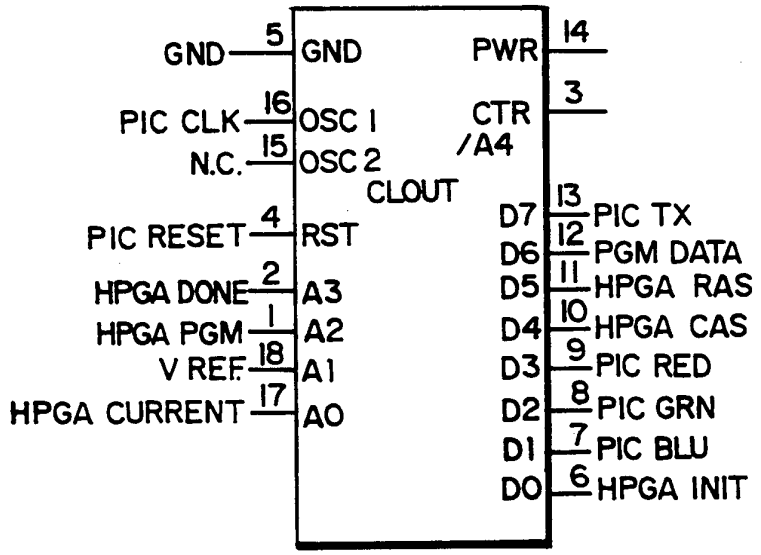

FIG. 5b

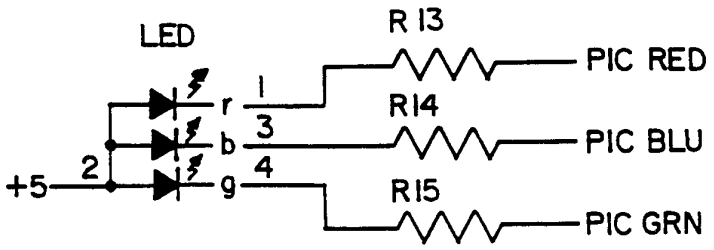

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07017

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :GO6F 17/50; HO1S 3/00
US CL : 395/185.02, 421.05, 800; 364/571.03, 221.9, 249, 267.6, Dig.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/185.02, 421.05, 800; 364/571.03, 221.9, 249, 267.6, Dig.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

1. APS US PATENT FILE DATABASE SEARCHED.
2. IEEE DATABASE CD-ROM SEARCHED

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US, A, 5,073,838 (AMES) 17 December 1991 Fig.1.	1-4 ---- 5-11
Y	US, A, 5,086,238, (WATANABE ET AL) 04 February 1992, col. 37 lines 30-36.	1-11
Y	US, A, 5,233,446, (INOUE ET AL) 03 August 1993 Fig. 1.	1-11
A	US, A, 5,244,146 (JEFFERSON ET AL) 14 September 1993.	1-11
A	US, A, 5,329,470 (SAMPLE ET AL) 12 July 1994.	1-11
A	US, A, 4,001,649 (YOUNG) 04 January 1977.	1-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
17 JULY 1996	06 AUG 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DZUNG C. NGUYEN Telephone No. (703) 305-9695

Form PCT/ISA/210 (second sheet)(July 1992)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07017

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-11

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/07017

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

Group I, Claims 1-11, drawn to real time monitor.
Group II, Claims 12-19, drawn to programming a gate array.

This invention contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all the inventions to be examined, the appropriate additional examination fees must be paid.

The inventions listed as Group I and Group II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the inventive concept of group I and Group II are only related as subcombinations which are disclosed as usable together in a single combination. The subcombinations; however; can be shown to be separately usable. In the instant case, inventive concept of Group II has separate utility from Group I such as real time temperature monitor does not require to monitor conditions of the programmable semiconductor.