

[54] **EIGHT BIT DIGITAL PHASE SHIFTER
UTILIZING PLURALITY OF SWITCHABLE
LOW PASS FILTERS**

[75] Inventor: **Gerald E. Johnson**, Littleton, Colo.

[73] Assignee: **Martin Marietta Corporation**,
Washington, D.C.

[22] Filed: **May 17, 1972**

[21] Appl. No.: **254,262**

[52] U.S. Cl. **333/31 R, 333/73 R, 333/73 S**

[51] Int. Cl. **H01p 1/18**

[58] Field of Search **333/29 R, 31 R, 70 R, 73 R,
333/73 C, 73 S**

[56] **References Cited**

UNITED STATES PATENTS

2,743,367 4/1956 Felch et al. 333/31 X

3,546,636 12/1970 Di Piazza 333/31 R
3,471,711 10/1969 Poschenrieder et al. 333/29 X

Primary Examiner—Paul L. Gensler

Attorney, Agent, or Firm—Sughrue, Rothwell, Mion,
Zinn & Macpeak

[57] **ABSTRACT**

An eight bit digital phase shifter includes a plurality of low pass filter networks to provide the lowest five bits. The first three bits are provided by low pass pi networks, phase shift being controlled by controlling the network series inductance. The next two bits are provided by low pass tee networks, phase shift being controlled by selectively shorting the network series inductance to effectively remove the filter from the phase shifter. The three highest bits are provided by 3dB hybrids.

9 Claims, 4 Drawing Figures

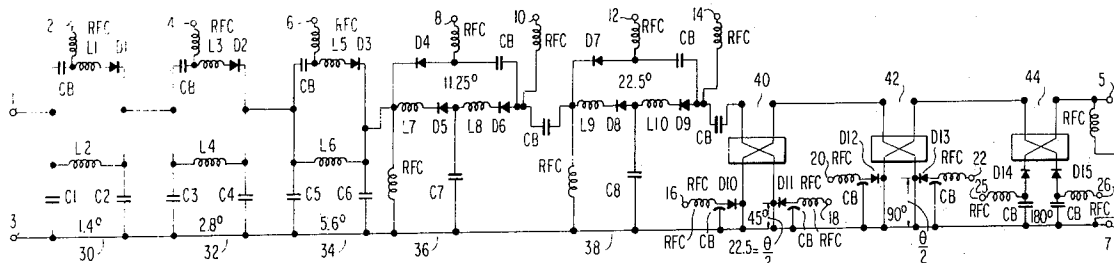


FIG. 1

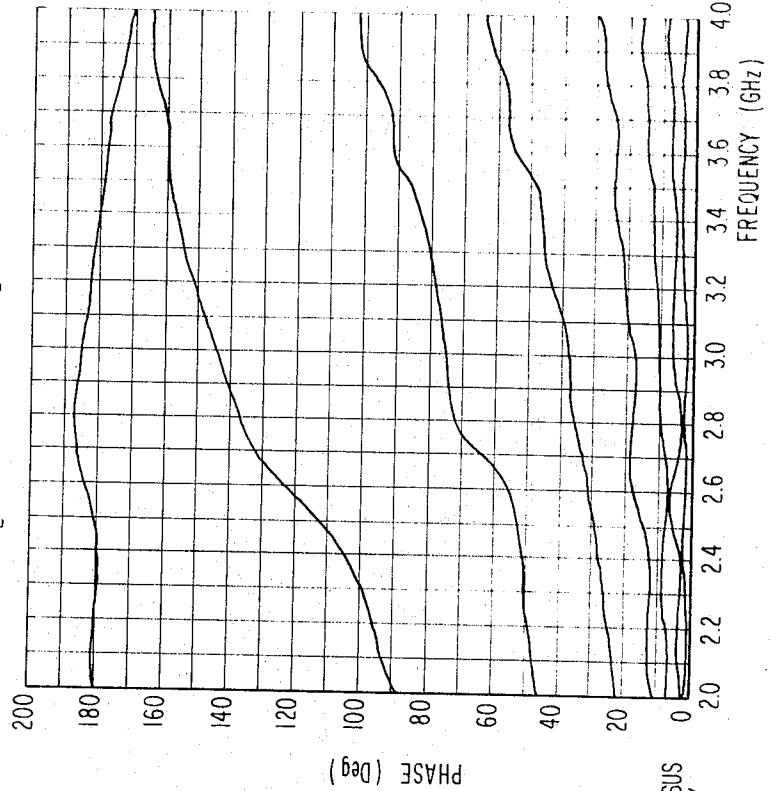
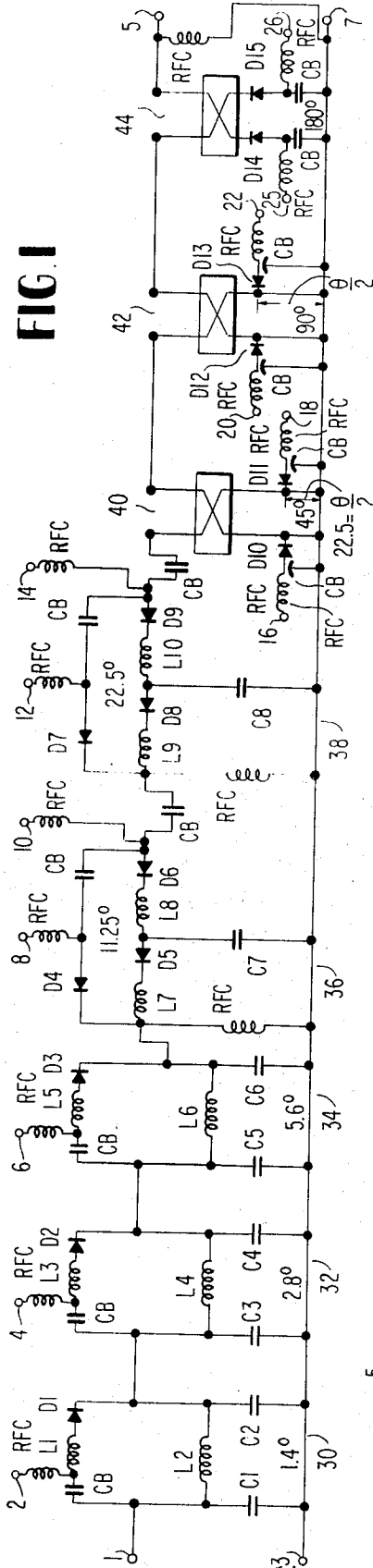


FIG. 4

PHASE VERSUS
FREQUENCY

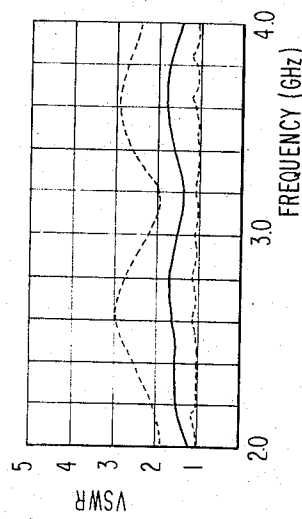


FIG. 2

VSWR VERSUS
FREQUENCY

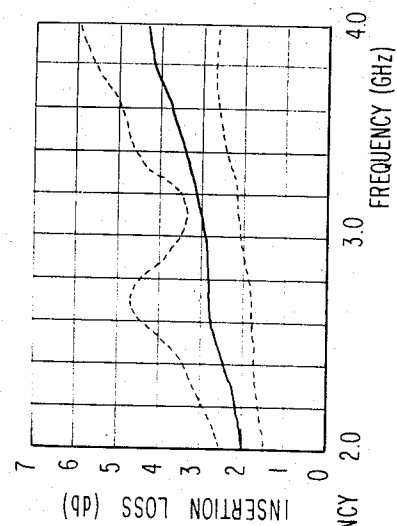


FIG. 3

INSERTION LOSS
VERSUS FREQUENCY

EIGHT BIT DIGITAL PHASE SHIFTER UTILIZING PLURALITY OF SWITCHABLE LOW PASS FILTERS

GOVERNMENT CONTRACTS

Development of the invention herein described and claimed was carried out in part under contract with the United States Air Force.

BACKGROUND OF THE INVENTION

In recent years, workers in the wave transmission arts have found it desirable to digitally control the phase shifting of microwaves passing along a transmission line. One technique for digital phase shifting is based upon the selective alteration of the reactive impedance of the transmission line. Using such a technique, a phase shift is realized in response to a change in the electrical length of the line. A phase shifter using this technique is not to be confused with a delay line which introduces phase shift as a result of a change in the physical length of the path traveled by a wave. In the interest of clarity the term phase shifter used herein will refer to those microwave networks which introduce phase shift in response to a change in the electrical length of the transmission line.

Examples of such phase shifters are described in U.S. Pat. No. 3,491,314 to Joseph F. White and U.S. Pat. No. 3,436,691 to W.F. Hoffman. In the White phase shifter, varactors or PIN diodes are used to digitally control the reactive impedance of the transmission line. In the Hoffman phase shifter a similar digital control system is used. The Hoffman phase shifter provides phase shift increments or bits of 5.6° with a maximum phase shift of 90° using a four bit network.

An improvement over phase shifters of the type previously described, is found in a digital phase shifter which uses a pi filter network switchable, in response to digital signals, from a low pass pi to a high pass pi filter. Such a phase shifter is disclosed in U.S. Pat. No. 3,546,636 to G.C. Di Piazza. As indicated in the Di Piazza patent, a phase shifter which uses filter networks to accomplish the phase shifting has an advantage over the White and Hoffman type of phase shifter in that the size of the complete phase shifter can be reduced. However, the Di Piazza phase shifter suffers the disadvantage that it is narrow band and presents a constant phase versus frequency response over this narrow band. More specifically, this phase shifter provides only an 18 percent bandwidth for a 12dB return loss.

The present invention is directed to an improved digital phase shifter of the type using filter networks to produce desired phase shifts, the improved phase shifter having a wider bandwidth than the Di Piazza phase shifter as well as greater efficiency, fewer circuit elements and a linear, rather than constant, phase versus frequency response.

SUMMARY OF THE INVENTION

The phase shifter of the present invention comprises low pass filter networks including elements which can selectively change the network impedance. A change in the network impedance causes a change in the phase shift experienced by a wave passing therethrough.

More specifically, the phase shifter includes low pass pi networks and low pass tee networks with means for selectively varying the networks' series inductance.

The use of low pass filter networks rather than filter networks which are switchable from a low pass network to a high pass network, provides a broader band response and a linear phase versus frequency response.

In the preferred embodiment, the phase shifter is formed to provide an octave bandwidth, eight bit phase shifter providing a total phase shift capacity of 360° at the low side of its operating bandwidth in 1.4° phase shift increments or bits. Since the phase shifter possesses a linear phase versus frequency response it has a phase shift capacity of 720° at the high side of its bandwidth with phase shifts in increments of 2.8° .

To control the VSWR within acceptable limits low pass pi filters are used for the three smallest bits while low pass tee filters are used for the next two larger bits. The three largest bits are provided using a conventional 3dB hybrid configuration.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic representation of a phase shifter constructed in accordance with the teachings of the invention;

FIG. 2 is a graph of VSWR versus frequency for the phase shifter of FIG. 1;

FIG. 3 is a graph of insertion loss versus frequency for the phase shifter of FIG. 1; and

FIG. 4 is a graph of phase versus frequency for the phase shifter of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the phase shifter comprises an eight bit PIN diode phase shifter operating over a bandwidth from 2 to 4 GHz. It makes use of low pass filter networks which have a nominally linear phase versus frequency response from D.C. to a region near the cutoff frequency of the filter.

The phase shifter is designed to provide bits, that is phase shift increments, of 1.4° , 2.8° , 5.6° , 11.25° , 45° , 90° and 180° at 2 GHz. Due to the linear phase versus frequency response over the operating range of the phase shifter, eight bits from 2.8° to 720° may be provided at 4GHz. Where a total phase shift of only 540° at 4GHz is acceptable, the 180° bit at 2 GHz is designed to provide a constant phase shift over the frequency bandwidth. Thus the phase shifter would provide eight bits, from 2.8° to 540° at 4 GHz.

FIG. 1 illustrates the eight bit phase shifter embodiment of the invention having input terminals 1, 3 and output terminals 5, 7. Between the input and output terminals are eight phase shifting networks each providing the indicated phase shift at 2 GHz. The low pass pi networks 30, 32 and 34 are used to provide the three smallest bits. Since each pi network is of the same configuration and operates in the same manner only pi network 30 will be discussed in further detail. Network 30 includes a shunt capacitance comprised of capacitors C1 and C2 and a series inductance comprised of inductors L1 and L2. The phase of a wave entering terminals 1, 3 and passing through network 30 is varied by controlling the impedance of the network which in turn is controlled by varying the network series inductance.

The network series inductance is varied between two values by selectively switching inductor L1 into the network. When switched into the network, inductors L1 and L2 are in parallel thus providing a lower series inductance than is present when only inductor L2 is in

the network. The switching of inductor L1 into or out of the network is controlled by PIN diode D1 connected in series with inductor L1. When diode D1 is forward biased the network series inductance comprises inductors L1 and L2 in parallel while when diode D1 is back biased the series inductance is provided by inductor L2 alone. Biasing of diode D1 is controlled by a bias source (not shown) connected to terminal 2. RF signals are isolated from the bias source in a conventional manner through the use of RF choke, RFC, and bypass capacitor CB.

The phase shift experienced by a wave passing through a low pass filter network is directly proportional to the value of the network series inductance. Thus, when diode D1 is forward biased, placing inductor L1 in parallel with inductor L2, a minimum phase shift is experienced by the wave. When inductor L1 is switched out of the network, the phase shift increases. The values of inductors L1 and L2 are selected such that the phase shift increases by 1.4° when inductor L1 is switched out of the network.

Low pass pi networks 32 and 34 operate in an identical manner. Diodes D2 and D3 in networks 32 and 34 correspond to diode D1 in network 30 while inductors L3, L4 and L5, L6 correspond to inductors L1 and L2. Biasing of diodes D2 and D3 is controlled by bias sources coupled to terminals 4 and 6. The shunt capacitance of networks 32 and 34 are provided by capacitors C3, C4 and C5, C6 respectively.

Network 32 provides a phase shift of 2.8° while network 34 a phase shift of 5.6° . The size of the phase shift is controlled by the value of the network inductors and capacitors. The value of the shunt capacitors and the average value of the series inductance are selected from a scaled Chebyshev prototype filter. Further, the ratio of the values of the parallel inductors of a network is selected so that the VSWR is equal in both bias states of the network PIN diode.

As the phase shift provided by the low pass pi filter increases so does the mismatch. Thus, for a given VSWR there is a maximum phase shift which can be provided by the low pass pi network. It has been determined that for a phase shift of 5.6° at 2 GHz (11.25° at 4 GHz) the VSWR assumes a value of about 1.2 : 1. In order to lower the VSWR for larger phase shifts I have determined that low pass tee networks may be used.

Thus, to contain the VSWR while increasing the size of the phase shift bits, low pass tee filters, as illustrated at 36 and 38 of FIG. 1 are used. The values of inductors L7 and L8 and capacitor C7 are selected to provide a phase shift of 11.25° while the values of inductors L9 and L10 and capacitor C8 are selected to provide a phase shift of 22.5° at 2 GHz.

For a minimum phase shift in networks 36 and 38, diodes D4 and D7 are forward biased while diodes D5, D6, D8 and D9 are back biased to effectively remove the low pass tee filters from the transmission line. Selective biasing of these diodes is provided by bias sources (not shown) coupled to terminals 8, 10, 12 and 14. As with the low pass pi networks, RF chokes, RFC, and bypass capacitors, CB, are provided to isolate the bias sources from the RF signals. When the bias conditions are reversed, diodes D4 and D7 are back biased while diodes D5, D6, D8 and D9 are forward biased, thus effectively placing the low pass tee filters 36 and 38 back into the phase shifter. The phase shift is then nominally that of the low pass tee filter. The particular

phase shift provided by each of the tee network filters is controlled by the value of the inductors and capacitors which comprise the filter. As with the low pass pi networks, the filter elements are chosen to give a Chebyshev response.

The circuit of FIG. 1 can be implemented on microstrip. In the microstrip implementation, high impedance and low impedance sections of line are used to approximate the inductors and capacitors. Using a Chebyshev prototype, the designer can vary the cutoff frequency of the filter until the desired change in phase shift (that is the difference between the bias conditions) is obtained. Physical lengths and impedances may be varied from the calculated values by small amounts to optimize the VSWR while maintaining the desired phase shift.

The three large bits (45° , 90° , and 180° at 2 GHz) preferably use a conventional large bit phase shifter network utilizing a three dB hybrid such as that described by Julius Lange in the publication Interdigitated Strip-Line Quadrature Hybrid, G-MTT 1969 International Microwave Symposium, Dallas, Texas, May 1969. This phase shift network uses a 3 dB hybrid with PIN diodes to shift the shorted output arms an electrical length $\theta/2$ closer to the hybrid for a phase change of θ . Phase shifting networks 40 and 42 illustrate the configuration required for developing a 45° and 90° phase shift respectively. With respect to network 40, when diodes D10 and D11 are forward biased in response to bias signals applied at the terminals 16 and 18, the shorted output arms of the hybrid are shifted an electrical length 22.5° closer to the hybrid. This has the effect of producing a 45° phase shift. It should be noted that the phase change of θ is frequency dependent and in fact the phase shift provided by the hybrid varies substantially linearly over the frequency bandwidth. Thus, for the 45° phase shift provided by hybrid 40 at 2 GHz, the same network will provide a 90° phase shift at 4 GHz.

Hybrid 42 is used to provide a 90° phase shift at 2 GHz. To accomplish this, diodes D12 and D13 are utilized to selectively bring the shorted output arms of the hybrid 45° closer to the hybrid at 2 GHz.

It has been found that a constant 180° phase shift over the bandwidth provides suitable phase shift flexibility for many design applications. In such a case, network 44 may take the configuration shown. In this case, diodes D14 and D15 are used to switch from an open circuit to a closed circuit thus providing a constant 180° phase shift over the bandwidth. Biasing of diodes D14 and D15 is provided by a bias source coupled to terminals 25 and 26. As with the low pass pi and tee filters, the hybrid phase shifter sections include conventional RF chokes, RFC and RF bypass capacitors, CB, to isolate the RF signals from the bias source.

Greater appreciation of the unique digital phase shifter described hereinabove, may be had by reference to FIGS. 2, 3 and 4. FIGS. 2 and 3 represent respectively by VSWR and insertion loss experimentally determined for the phase shifter of FIG. 1 over the specified bandwidth. The solid lines represent the average values while the dash lines show the maximum and minimum values for all 256 phase states. The phase shifter used to develop these graphs was constructed on two 2×2 inch alumina substrates, 0.060 inches thick. The substrates used have a surface finish of about 20 micro-inches. It was found that some energy was lost above

3.5 GHz due to radiation. This loss could be reduced by using thinner substrates and a better surface finish.

The measured phase characteristics are illustrated in FIG. 4. Each individual bit is shown with all of the bits in the minimum phase state. In the phase shifter utilized to develop the graph of FIG. 4, phase shifter network 44 was of the type providing a constant 180° phase shift over the bandwidth. With respect to the other individual bits, it is seen that the phase shift between 2 GHz and 4 GHz is nominally linear. Deviations from linearity occur primarily in two ways. First, there are variations about the nominal and second there is a gradual increasing phase or dispersion with frequency which is particularly notable on the smaller bits. The variations or wiggles about the nominal are due primarily to the effects of VSWR interactions and will virtually disappear when the individual bits are terminated in 50 ohms.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A digital phase shifter comprising a plurality of phase shift networks connected in series so that the total phase shift is the sum of the phase shift provided by each network, said plurality of networks including at least a first phase shifter network in the form of a low pass pi filter having shunt capacitive reactance and series inductive reactance, and digital means for selectively switching the value of the series inductive reactance between two fixed values to digitally vary the phase shift provided by said low pass pi filter.

2. A digital phase shifter comprising a plurality of phase shift networks connected in series so that the total phase shift is the sum of the phase shift provided by each network, said plurality of networks including at least a first phase shifter network in a form of a low pass pi filter having shunt capacitive reactance and series inductive reactance, means for changing the value of the series inductive reactance to vary the phase shift provided by said low pass pi filter,

at least a second phase shifter network in the form of a low pass tee filter having shunt capacitive reactance and series inductive reactance, and means for selectively causing a signal traveling through said digital phase including to bypass said low pass tee filter by selectively shorting said series inductive reactance.

3. A digital phase shifter comprising a plurality of phase shift networks connected in series so that the total phase shift is the sum of the phase shift provided by each network, said plurality of networks including at least a first phase shifter network in the form of a low pass pi filter having shunt capacitive reactance and series inductive reactance, means for changing the value of the series inductive reactance to vary the phase shift provided by said low pass pi filter,

wherein said means for changing the value of the series inductive reactance of the low pass pi filter comprises a first inductive reactance, a series connected second inductive reactance and a diode, said diode being capable of being placed in either of two conductive states, and means for causing said diode to assume a first state to cause said first

and second inductive reactances to be connected in parallel and for causing said diode to assume a second state to cause said second inductive reactance to be effectively removed from said low pass pi filter.

4. A digital phase shifter comprising a plurality of phase shift networks connected in series so that the total phase shift is the sum of the phase shift provided by each network, said plurality of networks including at least a first phase shifter network in the form of a low pass pi filter having shunt capacitive reactance and series inductive reactance, means for varying the series inductive reactance to vary the phase shift provided by said first network, and

at least a second phase shifter network in the form of a low pass tee filter having shunt capacitive reactance and series inductive reactance and means for selectively shorting said series inductive reactance of said low pass tee filter,

wherein said means for shorting said low pass tee filter series inductive reactance comprises first diode means in series with said tee filter series inductive reactance and second diode means shunting said tee filter series inductive reactance, said first and second diode means being capable of assuming first and second conductive states whereby when said first diode means is in a first conductive state and said second diode means is in a second conductive state, said series inductive reactance is short circuited to effectively remove the low pass tee filter from the phase shifter.

5. The digital phase shifter of claim 4 wherein said means for varying the series inductive reactance of each of the low pass pi filters comprises a first inductive reactance and a series connected second inductive reactance and a diode, said diode being capable of being placed in either of two conductive states whereby in a first state said first and second inductive reactances are in parallel while in the second conductive state said second inductive reactance is effectively removed from said low pass pi network.

6. The digital phase shift network of claim 5 wherein said diodes in said low pass pi filters and said first and second diode means in said low pass tee filters comprise PIN diodes, each of said low pass tee filters comprising first and second series connected inductive reactances, said shunt capacitive reactance being coupled between said tee filter first and second series connected inductive reactances to ground, said first diode means comprising first and second PIN diodes, said second diode means comprising a third PIN diode in parallel with the series circuit comprising the first and second tee filter inductive reactances and said first and second PIN diodes.

7. A digital phase shifter comprising a plurality of phase shift networks connected in series so that the total phase shift is the sum of the phase shift provided by each network, said plurality of networks including at least a first phase shifter network in the form of a low pass pi filter having shunt capacitive reactance and series inductive reactance, means for varying the series inductive reactance to vary the phase shift provided by said first network, and

at least a second phase shifter network in the form of a low pass tee filter having shunt capacitive reactance and series inductive reactance and means for

7

selectively shorting said series inductive reactance of said low pass tee filter, wherein said phase shifter is an eight bit phase shifter each of the three smallest phase shift bits being comprised of said low pass pi filters, each of the next two smallest bits being comprised of said low pass tee filters, the three largest bits being formed from hybrid networks.

8. The digital phase shifter of claim 7 wherein said means for shorting each of said low pass tee filter series inductive reactance comprises, first diode means in series with the tee filter series inductive reactance and second diode means shunting the tee filter series inductive reactance, said first and second diode means being capable of assuming first and second conductive states whereby when said first diode means is in a first con-

8

ductive state and said second diode means is in a second conductive state, said series inductive reactance is short circuited to effectively remove the low pass tee filter from the phase shifter.

9. The digital phase shifter network as claimed in claim 8 further including bias means coupled to each low pass filter, said bias means coupled to said low pass pi filters being adapted to selectively forward or reverse bias said low pass pi filter PIN diodes to thereby selectively vary their series inductive reactance, said bias means coupled to said low pass tee filters being adapted to selectively forward bias said third PIN diodes while back biasing said first and second PIN diodes to thereby effectively remove the low pass tee filters from the phase shifter.

* * * * *

20

25

30

35

40

45

50

55

60

65