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(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 South Federal Way, (a Corporation Of The State Of Delaware), Boise, ID 83716 (US).

(72) Inventors: **MIYASHITA, Toshihiko**; 2180 S. Hudson Avenue, Apt. A204, Boise, ID 83705 (US). **MOCUTA, Dan**; 5778 S. Horseshoe Pi., Boise, ID 83716 (US).

(74) Agent: **MATKIN, Mark, S.** et al.; Wells St. John P.S., 601 West Main Avenue, Suite 600, Spokane, WA 99201 (US).

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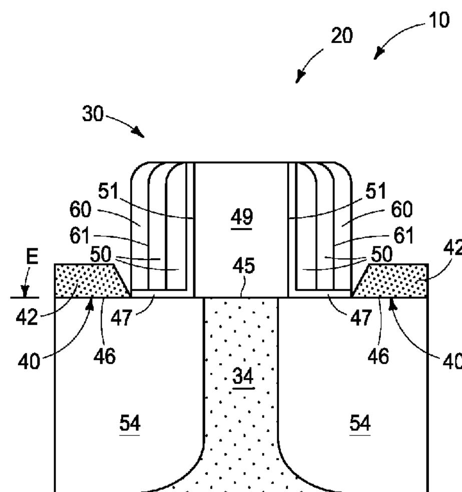

FIG. 49

(57) Abstract: DRAM circuitry comprises a memory array comprising memory cells individually comprising a transistor and a charge-storage device, The transistors individually comprise two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array. One of the source/drain regions is electrically coupled to one of the charge¬ storage devices. The other of the source/drain regions is electrically coupled to one of multiple sense lines of the memory array. Peripheral circuitry comprises wordline-driver transistors having gates which individually comprise one ooff the wordlines aanndd comprises sense-line-amplifier transistors having gates which individually comprise one of the sense lines. The sense-line-amplifier transistors and the wordline-driver transistors individually are a finFET having at least one fin comprising a channel region of the respective finFET. The sense-line- amplifier transistors and the wordline-driver transistors individually comprise two source/drain regions that individually comprise conductively- doped epitaxial semiconductor material that is adjacent one of two laterally- opposing sides of the at least one fin in a vertical cross-section. Methods are also disclosed.

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DESCRIPTION

DRAM CIRCUITRY AND METHOD OF FORMING DRAM CIRCUITRY

5 **TECHNICAL FIELD**

Embodiments disclosed herein pertain to DRAM circuitry and to methods of forming DRAM circuitry.

BACKGROUND

10 Memory is one type of integrated circuitry and is used in computer systems for storing data. Memory may be fabricated in one or more arrays of individual memory cells. Memory cells may be written to, or read from, using digitlines (which may also be referred to as bitlines, data lines, or sense lines) and access lines (which may also be referred to as wordlines).
15 The digitlines may conductively interconnect memory cells along columns of the array, and the access lines may conductively interconnect memory cells along rows of the array. Each memory cell may be uniquely addressed through the combination of a digitline and an access line.

Memory cells may be volatile, semi-volatile, or non-volatile.
20 Non-volatile memory cells can store data for extended periods of time in the absence of power. Non-volatile memory is conventionally specified to be memory having a retention time of at least about 10 years. Volatile memory dissipates and is therefore refreshed/rewritten to maintain data storage. Volatile memory may have a retention time of milliseconds or less.
25 Regardless, memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1”. In other systems, at least some individual memory cells may be configured to store more than two levels or states of information.

30 A capacitor is one type of electronic component that may be used in a memory cell. A capacitor has two electrical conductors separated by electrically insulating material. Energy as an electric field may be electrostatically stored within such material. Depending on composition of the insulator material, that stored field will be volatile or non-volatile. For
35 example, a capacitor insulator material including only SiO_2 will be volatile.

One type of non-volatile capacitor is a ferroelectric capacitor which has ferroelectric material as at least part of the insulating material. Ferroelectric materials are characterized by having two stable polarized states and thereby can comprise programmable material of a capacitor and/or memory cell. The polarization state of the ferroelectric material can be changed by application of suitable programming voltages and remains after removal of the programming voltage (at least for a time). Each polarization state has a different charge-stored capacitance from the other, and which ideally can be used to write (i.e., store) and read a memory state without reversing the polarization state until such is desired to be reversed. Less desirable, in some memory having ferroelectric capacitors the act of reading the memory state can reverse the polarization. Accordingly, upon determining the polarization state, a re-write of the memory cell is conducted to put the memory cell into the pre-read state immediately after its determination. Regardless, a memory cell incorporating a ferroelectric capacitor ideally is non-volatile due to the bi-stable characteristics of the ferroelectric material that forms a part of the capacitor. Other programmable materials may be used as a capacitor insulator to render capacitors non-volatile.

A field effect transistor is another type of electronic component that may be used in a memory cell. These transistors comprise a pair of conductive source/drain regions having a semiconductive channel region there-between. A conductive gate is adjacent the channel region and separated there-from by a thin gate insulator. Application of a suitable voltage to the gate allows current to flow from one of the source/drain regions to the other through the channel region. When the voltage is removed from the gate, current is largely prevented from flowing through the channel region. Field effect transistors may also include additional structure, for example a reversibly programmable charge-storage region as part of the gate construction between the gate insulator and the conductive gate. Regardless, the gate insulator may be programmable, for example being ferroelectric.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic schematic and structural view of DRAM circuitry in accordance with an embodiment of the invention.

Figs. 2-13 are diagrammatic sectional views of portions of DRAM circuitry in accordance with an embodiment of the invention.

Figs. 14-73 are diagrammatic section view of constructions in accordance with some method aspects of the invention in the forming of DRAM circuitry in accordance with some embodiments of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

An embodiment of DRAM Circuitry in accordance with the invention is described initially with respect to Figs. 1-13.

Fig. 1 diagrammatically and schematically illustrates a portion of dynamic random access memory (DRAM) circuitry 10 comprising a memory array 12 comprising memory cells 114 individually comprising a transistor 116 and a charge-storage device 118 (e.g., a capacitor). Transistors 116 individually comprise two source/drain regions 120, 121 having a gate 122 there-between that is part of one of multiple wordlines 14 of memory array 12. One of the source/drain regions (e.g., 120) is electrically coupled (e.g., directly electrically coupled) to one of charge-storage devices 118. The other of the source/drain regions (e.g., 121) is electrically coupled to one of multiple sense lines 16 of memory array 12. Example charge-storage devices 118 as a capacitor has one of its nodes directly electrically coupled to source/drain region 120 of a transistor 116 and another node directly electrically coupled to a cell plate 166. Example cell plate 166 may be at any suitable reference voltage, including by way of example, 0V, a power supply voltage V_{CC}, one half of V_{CC}, or the like, depending upon application. DRAM circuitry 10 comprises peripheral circuitry comprising, for example, wordline-driver circuitry 18 and sense-line-amplifier circuitry 20. Wordlines 14 extend from memory array 12 to wordline-driver circuitry 18 and sense lines 16 extend from memory array 12 to sense-line-amplifier circuitry 20. By way of example, the peripheral circuitry may be wholly laterally aside memory array 12. Such may be partially laterally aside memory array 12 and/or wholly or partially above or below memory array 12. Regardless, additional peripheral circuitry may be provided (not

shown). Wordlines 14 and sense lines 16 individually comprise one or more conductive materials (e.g., metal material) and that may not be the same relative one another.

Referring to Figs. 2-13, wordline-driver circuitry 18 (Figs. 10-13) comprises wordline-driver transistors 30 having gates 31 which individually comprise one of wordlines 14. Sense-line-amplifier circuitry 20 (Figs. 2-9) comprises sense-line-amplifier transistors 32* (an * being used as a suffix to be inclusive of all such same-numerically-designated components that may or may not have other suffixes) having gates 33 which individually comprise one of sense lines 16. Sense-line-amplifier transistors 32* and wordline-driver transistors 30 individually are a finFET (e.g., 30 or 32*) having at least one fin 34 (multiple fins 34 [e.g., two] per individual transistor 30, 32* being shown) comprising a channel region 35 of the respective finFET (e.g., channel region 35 being appropriately doped semiconductive material [e.g., silicon, germanium, etc.] and comprising part of active area 21 having insulator material 22 there-between [e.g., silicon dioxide and/or silicon nitride]). Sense-line-amplifier transistors 32* and wordline-driver transistors 30 individually comprise two source/drain regions 38*/38* and 40/40, respectively, that individually comprise conductively-doped epitaxial semiconductor material 41* and 42, respectively, that is adjacent one of two laterally-opposing sides 43 (Figs. 3, 7, 13) of at least one fin 34 in a vertical cross-section (e.g., that of each of Figs. 3 and 7 for source/drain regions 38*/38* and that of Fig. 13 for source/drain regions 40/40).

In one embodiment, sense-line-amplifier transistors 32* collectively comprise NMOS transistors 32N (Figs. 2-5) and PMOS transistors 32P (Figs. 6-9) (only one of each being shown for brevity). In one embodiment, source/drain regions 38N of sense-line-amplifier transistors 32N that comprise conductively-doped epitaxial semiconductor material 41N of NMOS transistors 32N individually comprise silicon that is conductively-doped with phosphorus. In one embodiment, source/drain regions 38P of sense-line-amplifier transistors 32P that comprise conductively-doped epitaxial semiconductor material 41P of PMOS transistors 32P individually comprise a mixture of silicon and germanium that is conductively-doped with boron. Wordline-driver transistors 30 also collectively may be n-type and p-type, for example, individually being one of PMOS or NMOS.

Ideally, conductivity-imparting dopant concentration in conductively-doped epitaxial semiconductor material 41* and 42 is at least 1 x 10^{20} atoms/cm^3 (e.g., and no greater than 1 x 10^{22} atoms/cm^3). Additional conductivity-modifying impurity material may be in and/or adjacent conductively-doped epitaxial semiconductor material 41* and/or 42 (e.g., LDD and/or halo regions and not shown).

In one embodiment, conductively-doped epitaxial semiconductor material 41* of source/drain regions 38* of sense-line-amplifier transistors 32* has a bottom-most surface 44 that is lower than an uppermost surface 45 of the at least one fin 34. In one embodiment, conductively-doped epitaxial semiconductor material 42 of source/drain regions 40 of wordline-driver transistors 30 has a lower surface 46 that is at the same elevation (e.g., E) as uppermost surface 45 of the at least one fin 34.

In one embodiment, gate insulator 25 that is between the at least one fin 34 and gates 33 of sense-line-amplifier transistors 32* is thinner (i.e., physically or as equivalent oxide thickness [EOT]) than gate insulator 27 that is between the at least one fin 34 and gates 31 of wordline-driver transistors 30. In one embodiment, gate insulator 25 and gate insulator 27 are of the same composition relative one another, and in one such embodiment such same composition is silicon dioxide. In one embodiment, gate insulator 25 has thickness of 5 Angstroms to 30 Angstroms (i.e., physically or EOT) and gate insulator 27 has a thickness of 30 Angstroms to 60 Angstroms (i.e., physically or EOT).

Example conductive vias 75 are shown individually directly electrically coupling to source/drain regions 38*, 40.

Embodiments of the invention encompass methods used in forming DRAM circuitry. Embodiments of the invention encompass DRAM circuitry independent of method of manufacture. Nevertheless, such DRAM circuitry may have any of the attributes as described herein in method embodiments. Likewise, the described method embodiments may incorporate, form, and/or have any of the attributes described with respect to device embodiments.

A method of forming DRAM circuitry in accordance with one embodiment comprises forming a memory array (e.g., 12) comprising memory cells (e.g., 114) individually comprising a transistor (e.g., 116) and a charge-storage device (e.g., 118). The transistors individually comprise

two source/drain regions (e.g., 120, 121) having a gate (e.g., 122) there-between that is part of one of multiple wordlines (e.g., 14) of the memory array. One of the source/drain regions (e.g., 120) is electrically coupled to one of the charge-storage devices. The other of the source/drain regions (e.g., 121) is electrically coupled to one of multiple sense lines (e.g., 16) of the memory array. Peripheral circuitry (e.g., 18) is formed that comprises wordline-driver transistors (e.g., 30) having gates (e.g., 31) which individually comprise one of the wordlines and comprising sense-line-amplifier transistors (e.g., 32*) having gates (e.g., 31) which individually comprise one of the sense lines. The sense-line-amplifier transistors and the wordline-driver transistors are formed individually to be a finFET having at least one fin (e.g., 34) comprising a channel region (e.g., 35) of the respective finFET. In one embodiment, the forming of the at least one fin 34 of the sense-line-amplifier transistors and the wordline-driver transistors occurs at the same time. The sense-line-amplifier transistors and the wordline-driver transistors are formed to individually comprise two source/drain regions (e.g., 38*/38*, 40/40) that individually comprise conductively-doped epitaxial semiconductor material (e.g., 41*, 42) that is adjacent one of two laterally-opposing sides (e.g., 43) of the at least one fin in a vertical cross-section (e.g., that of each of Figs. 3 and 7 for source/drain regions 38*/38* and that of Fig. 13 for source/drain regions 40/40).

In one embodiment, the forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors occurs before the forming of the conductively-doped epitaxial semiconductor material of the wordline-driver transistors (e.g., as shown in Figs. 15-49). In another embodiment, the forming of the wordline-driver transistors occurs before the forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors (e.g., as shown in Figs. 50-73).

Example embodiments of method aspects in accordance with the invention are described with reference to Figs. 14-73, and in groups of three figures that show cross-sectional views corresponding in positions to those of Figs. 3, 7, and 11, respectively, in a single group of three figures. Like numerals from the above-described embodiments have been used for predecessor constructions, with differences/additions using different numerals.

Referring to Figs. 14-16, first masking blocks 48 have been formed that individually are directly above the at least one fin 34 of sense-line-amplifier transistors 32* being formed (e.g., NMOS transistors 32N and PMOS transistors 32P being formed). Second masking blocks 49 have been formed that individually are directly above the at least one fin 34 of wordline-driver transistors 30 being formed. Example materials for masking blocks 48, 49 include silicon nitride atop polysilicon. An example protective layer 47 (e.g., silicon nitride or material other than silicon nitride, or polysilicon) has been formed over masking blocks 48, 49. Example LDD and/or halo implants 52, 53, and 54 have been formed as shown. Such may be separately formed by masking others of the construction as shown in two of Figs. 14-16 while implanting into one.

Referring to Figs. 17-19, first sidewall spacers 50 (e.g., silicon nitride) have been formed over two laterally-opposing sides 51 of first masking blocks 48 and second masking blocks 49.

The example described processing proceeds with some separate processing associated with the NMOS and PMOS transistors being formed, with such example processing occurring with respect to the PMOS transistors first in one ideal embodiment, although the processing order with respect to PMOS and NMOS may be reversed. Further, the described processing with respect to Figs. 14-49 in one ideal embodiment forms the respective conductively-doped epitaxial semiconductor materials of the NMOS and PMOS transistors to be essentially vertically recessed (relative to an uppermost surface of the at least one fin of the finFET being formed) whereas the conductively-doped epitaxial semiconductor material for the wordline-driver transistors is essentially or largely not so vertically recessed. However, any of the described conductively-doped epitaxial semiconductor materials may be formed in manners which are vertically recessed or not vertically recessed relative to an uppermost surface of the at least one fin of the finFET being formed.

Referring to Figs. 20-22, the construction of Figs. 17 and 19 has been masked with masking material 55 (e.g., photoresist) while the construction of Fig. 18 remains unmasked and material of first sidewalls spacers 50 and protective material 47 have been anisotropically etched as shown.

Conductively-doped epitaxial semiconductor material of the source/drain regions of at least some of the sense-line-amplifier transistors being formed are formed laterally outward of the first masking blocks and the first sidewall spacers there-aside. For example, and in one embodiment referring to Figs. 23-25, masking material 55 (not shown) has been removed and first masking blocks 48 and first sidewall spacers 50 there-aside (and material 47 when present) have been used as a mask while etching two recesses 56 into substrate material 53 (e.g., halo-implanted material 53) that is laterally adjacent the at least one fin 34 of sense-line-amplifier transistors 32P (in this example).

Referring to Figs. 26-28, conductively-doped epitaxial semiconductor material 41P of source/drain regions 38P of sense-line-amplifier transistors 32P has been epitaxially grown from recesses 56 (e.g., from monocrystalline material that defines sides and bottoms of recesses 56) to have a lowest/bottom-most surface 44 that is lower than uppermost surface 45 of the least one fin 34.

Figs. 29-40, by way of example, show analogous processing per the above-described processing in forming additive first sidewall spacers 50 in forming n-type conductively-doped epitaxial semiconductor material 41N for NMOS sense-line-amplifier transistors 32N to have a lowest surface 44 that is lower than uppermost surface 45 of the at least one fin 34.

Referring to Figs. 41-43, second sidewall spacers 60 (e.g., silicon nitride) have been formed over two laterally-opposing sides 61 of first sidewall spacers 50 that are laterally over each of first masking blocks 48 and second masking blocks 49.

Conductively-doped epitaxial semiconductor material of the source/drain regions of at least some of the wordline-driver transistors is formed laterally outward of the second masking blocks and the second sidewall spacers there-aside. For example, and referring initially to Figs. 44-46 and in one embodiment, the constructions of Figs. 41/44 and 42/45 have been masked (e.g., with photoresist 55) while second sidewall spacers 60 (and remnant additive first masking block material vertically there-under, etc.) have been anisotropically etched.

Referring to Fig. 47-49, second masking blocks 49 with first and second sidewall spacers 50, 60 there-aside have been used as a mask while

epitaxially growing conductively-doped epitaxial semiconductor material 42 of source/drain regions 40 of wordline-driver transistors 30 from uppermost surface 45 of at least one fin 34 to have a lower surface 46 that is at the same elevation as uppermost surface 45 of the at least one fin 34.

5 Conductive doping of the above-described conductively-doped epitaxial semiconductor materials 41*, 42 may occur *in situ* while being epitaxially grown and/or subsequently, and otherwise optimized as will be appreciated by the artisan. Masking blocks 48, 49 (and some, all, or none of materials there-aside) may be subsequently removed and conductive gate 10 material substituted therefor (plus gate insulator 25, 27), for example in a damascene-like manner or by a manner involving deposition of conductive gate material followed by subtractive etching/patterning thereof.

Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used.

15 Figs. 50-73 show essentially self-explanatory processing analogous/corresponding to that described above wherein, in one example, the forming of the wordline-driver transistors occurs before the forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors. Such includes sequentially steps such as forming first 20 masking blocks that individually are directly above the at least one fin of the sense-line-amplifier transistors and second masking blocks that individually are directly above the at least one fin of the wordline-driver transistors being formed. Sidewall spacers are formed over two laterally-opposing sides of the first and second masking blocks. At least some material of the 25 sidewall spacers is removed (e.g., by etching) from individual of the second masking blocks. The conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors is formed laterally outward of the second masking blocks. More sidewall spacers are formed over the first and second masking blocks. The conductively-doped 30 epitaxial semiconductor material of the source/drain regions of the sense-line-amplifier transistors is formed laterally outward of the first masking blocks and the more sidewall spacers there-aside. In one embodiment, the at least one fin of the sense-line-amplifier transistors and the wordline-driver transistors are formed at the same time. Any other attribute(s) or aspect(s)

as shown and/or described herein with respect to other embodiments may be used.

The above processing(s) or construction(s) may be considered as being relative to an array of components formed as or within a single stack
5 or single deck of such components above or as part of an underlying base substrate (*albeit*, the single stack/deck may have multiple tiers). Control and/or other peripheral circuitry for operating or accessing such components within an array may also be formed anywhere as part of the finished construction, and in some embodiments may be under the array (e.g., CMOS
10 under-array). Regardless, one or more additional such stack(s)/deck(s) may be provided or fabricated above and/or below that shown in the figures or described above. Further, the array(s) of components may be the same or different relative one another in different stacks/decks and different stacks/decks may be of the same thickness or of different thicknesses
15 relative one another. Intervening structure may be provided between immediately-vertically-adjacent stacks/decks (e.g., additional circuitry and/or dielectric layers). Also, different stacks/decks may be electrically coupled relative one another. The multiple stacks/decks may be fabricated separately and sequentially (e.g., one atop another), or two or more
20 stacks/decks may be fabricated at essentially the same time.

The assemblies and structures discussed above may be used in integrated circuits/circuitry and may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules,
25 and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, cameras, wireless devices, displays, chip sets, set top boxes, games, lighting, vehicles, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

30 In this document unless otherwise indicated, “elevational”, “higher”, “upper”, “lower”, “top”, “atop”, “bottom”, “above”, “below”, “under”, “beneath”, “up”, and “down” are generally with reference to the vertical direction. “Horizontal” refers to a general direction (i.e., within 10 degrees) along a primary substrate surface and may be relative to which the substrate
35 is processed during fabrication, and vertical is a direction generally

orthogonal thereto. Reference to "exactly horizontal" is the direction along the primary substrate surface (i.e., no degrees there-from) and may be relative to which the substrate is processed during fabrication. Further, "vertical" and "horizontal" as used herein are generally perpendicular directions relative one another and independent of orientation of the substrate in three-dimensional space. Additionally, "elevationally-extending" and "extend(ing) elevationally" refer to a direction that is angled away by at least 45° from exactly horizontal. Further, "extend(ing) elevationally", "elevationally-extending", "extend(ing) horizontally", "horizontally-extending" and the like with respect to a field effect transistor are with reference to orientation of the transistor's channel length along which current flows in operation between the source/drain regions. For bipolar junction transistors, "extend(ing) elevationally" "elevationally-extending", "extend(ing) horizontally", "horizontally-extending" and the like, are with reference to orientation of the base length along which current flows in operation between the emitter and collector. In some embodiments, any component, feature, and/or region that extends elevationally extends vertically or within 10° of vertical.

Further, "directly above", "directly below", and "directly under" require at least some lateral overlap (i.e., horizontally) of two stated regions/materials/components relative one another. Also, use of "above" not preceded by "directly" only requires that some portion of the stated region/material/component that is above the other be elevationally outward of the other (i.e., independent of whether there is any lateral overlap of the two stated regions/materials/components). Analogously, use of "below" and "under" not preceded by "directly" only requires that some portion of the stated region/material/component that is below/under the other be elevationally inward of the other (i.e., independent of whether there is any lateral overlap of the two stated regions/materials/components).

Any of the materials, regions, and structures described herein may be homogenous or non-homogenous, and regardless may be continuous or discontinuous over any material which such overlie. Where one or more example composition(s) is/are provided for any material, that material may comprise, consist essentially of, or consist of such one or more composition(s). Further, unless otherwise stated, each material may be

formed using any suitable existing or future-developed technique, with atomic layer deposition, chemical vapor deposition, physical vapor deposition, epitaxial growth, diffusion doping, and ion implanting being examples.

Additionally, "thickness" by itself (no preceding directional adjective) is defined as the mean straight-line distance through a given material or region perpendicularly from a closest surface of an immediately-adjacent material of different composition or of an immediately-adjacent region. Additionally, the various materials or regions described herein may be of substantially constant thickness or of variable thicknesses. If of variable thickness, thickness refers to average thickness unless otherwise indicated, and such material or region will have some minimum thickness and some maximum thickness due to the thickness being variable. As used herein, "different composition" only requires those portions of two stated materials or regions that may be directly against one another to be chemically and/or physically different, for example if such materials or regions are not homogenous. If the two stated materials or regions are not directly against one another, "different composition" only requires that those portions of the two stated materials or regions that are closest to one another be chemically and/or physically different if such materials or regions are not homogenous. In this document, a material, region, or structure is "directly against" another when there is at least some physical touching contact of the stated materials, regions, or structures relative one another. In contrast, "over", "on", "adjacent", "along", and "against" not preceded by "directly" encompass "directly against" as well as construction where intervening material(s), region(s), or structure(s) result(s) in no physical touching contact of the stated materials, regions, or structures relative one another.

Herein, regions-materials-components are "electrically coupled" relative one another if in normal operation electric current is capable of continuously flowing from one to the other and does so predominately by movement of subatomic positive and/or negative charges when such are sufficiently generated. Another electronic component may be between and electrically coupled to the regions-materials-components. In contrast, when regions-materials-components are referred to as being "directly electrically coupled", no intervening electronic component (e.g., no diode, transistor,

resistor, transducer, switch, fuse, etc.) is between the directly electrically coupled regions-materials-components.

Any use of "row" and "column" in this document is for convenience in distinguishing one series or orientation of features from another series or orientation of features and along which components have been or may be formed. "Row" and "column" are used synonymously with respect to any series of regions, components, and/or features independent of function. Regardless, the rows may be straight and/or curved and/or parallel and/or not parallel relative one another, as may be the columns. Further, the rows and columns may intersect relative one another at 90° or at one or more other angles (i.e., other than the straight angle).

The composition of any of the conductive/conductor/conducting materials herein may be metal material and/or conductively-doped semiconductive/semiconductor/semiconducting material. "Metal material" is any one or combination of an elemental metal, any mixture or alloy of two or more elemental metals, and any one or more conductive metal compound(s).

Herein, any use of "selective" as to etch, etching, removing, removal, depositing, forming, and/or formation is such an act of one stated material relative to another stated material(s) so acted upon at a rate of at least 2:1 by volume. Further, any use of selectively depositing, selectively growing, or selectively forming is depositing, growing, or forming one material relative to another stated material or materials at a rate of at least 2:1 by volume for at least the first 75 Angstroms of depositing, growing, or forming.

Unless otherwise indicated, use of "or" herein encompasses either and both.

CONCLUSION

In some embodiments, DRAM circuitry comprises a memory array comprising memory cells individually comprising a transistor and a charge-storage device. The transistors individually comprise two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array. One of the source/drain regions is electrically coupled to one of the charge-storage devices. The other of the source/drain regions is electrically coupled to one of multiple sense lines of the memory array.

Peripheral circuitry comprises wordline-driver transistors having gates which individually comprise one of the wordlines and comprises sense-line-amplifier transistors having gates which individually comprise one of the sense lines. The sense-line-amplifier transistors and the 5 wordline-driver transistors individually are a finFET having at least one fin comprising a channel region of the respective finFET. The sense-line-amplifier transistors and the wordline-driver transistors individually comprise two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-10 opposing sides of the at least one fin in a vertical cross-section.

In some embodiments, DRAM circuitry comprises a memory array comprising memory cells individually comprising a transistor and a charge-storage device. The transistors individually comprise two source/drain regions having a gate there-between that is part of one of multiple wordlines 15 of the memory array. One of the source/drain regions is electrically coupled to one of the charge-storage devices. The other of the source/drain regions is electrically coupled to one of multiple sense lines of the memory array. Peripheral circuitry comprises wordline-driver transistors having gates which individually comprise one of the wordlines and comprise 20 sense-line-amplifier transistors having gates which individually comprise one of the sense lines. The sense-line-amplifier transistors and the wordline-driver transistors individually are a finFET having at least one fin comprising a channel region of the respective finFET. The sense-line-amplifier transistors and the wordline-driver transistors individually 25 comprise two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section. The conductively-doped epitaxial semiconductor material of the source/drain regions of the sense-line-amplifier transistors has a bottom-most surface that 30 is lower than an uppermost surface of the at least one fin. The conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors has a lower surface that is at the same elevation as the uppermost surface of the at least one fin. Gate insulator is between the at least one fin and the gates of the sense-line-35 amplifier transistors and the wordline-driver transistors. The gate insulator

that is between the at least one fin and the gates of the sense-line-amplifier transistors and the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors are of the same composition relative one another. The gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors is thinner than the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors.

In some embodiments, a method of forming DRAM circuitry comprises forming a memory array comprising memory cells individually comprising a transistor and a charge-storage device. The transistors individually comprise two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array. One of the source/drain regions is electrically coupled to one of the charge-storage devices. The other of the source/drain regions is electrically coupled to one of multiple sense lines of the memory array. Peripheral circuitry is formed that comprises wordline-driver transistors having gates which individually comprise one of the wordlines and comprises sense-line-amplifier transistors having gates which individually comprise one of the sense lines. The sense-line-amplifier transistors and the wordline-driver transistors are formed individually to be a finFET having at least one fin comprising a channel region of the respective finFET. The sense-line-amplifier transistors and the wordline-driver transistors are formed individually to comprise two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section. The forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors occurs before the forming of the conductively-doped epitaxial semiconductor material of the wordline-driver transistors.

In some embodiments, a method of forming DRAM circuitry comprises forming a memory array comprising memory cells individually comprising a transistor and a charge-storage device. The transistors individually comprise two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array. One of the source/drain regions is electrically coupled to one of the charge-storage devices. The other of the source/drain regions is electrically coupled to one

of multiple sense lines of the memory array. Peripheral circuitry is formed that comprises wordline-driver transistors having gates which individually comprise one of the wordlines and comprises sense-line-amplifier transistors having gates which individually comprise one of the sense lines. The sense-
5 line-amplifier transistors and the wordline-driver transistors are formed individually to be a finFET having at least one fin comprising a channel region of the respective finFET. The sense-line-amplifier transistors and the wordline-driver transistors are formed individually to comprise two source/drain regions that individually comprise conductively-doped epitaxial
10 semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section. The forming of the wordline-driver transistors occurs before the forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors.

CLAIMS:

1. DRAM circuitry comprising:

a memory array comprising memory cells individually comprising a transistor and a charge-storage device, the transistors individually comprising two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array, one of the source/drain regions being electrically coupled to one of the charge-storage devices, the other of the source/drain regions being electrically coupled to one of multiple sense lines of the memory array;

peripheral circuitry comprising wordline-driver transistors having gates which individually comprise one of the wordlines and comprising sense-line-amplifier transistors having gates which individually comprise one of the sense lines; and

the sense-line-amplifier transistors and the wordline-driver transistors individually being a finFET having at least one fin comprising a channel region of the respective finFET, the sense-line-amplifier transistors and the wordline-driver transistors individually comprising two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section.

2. The DRAM circuitry of claim 1 wherein the finFETs individually have more than one fin comprising the channel region.

3. The DRAM circuitry of claim 1 wherein the sense-line-amplifier transistors collectively comprise NMOS transistors and PMOS transistors.

4. The DRAM circuitry of claim 3 wherein the source/drain regions of the sense-line-amplifier transistors that comprise conductively-doped epitaxial semiconductor material of the NMOS transistors individually comprise silicon that is conductively-doped with phosphorus.

5. The DRAM circuitry of claim 3 wherein the source/drain regions of the sense-line-amplifier transistors that comprise conductively-doped epitaxial semiconductor material of the PMOS transistors individually comprise a mixture of silicon and germanium that is
5 conductively-doped with boron.

6. The DRAM circuitry of claim 1 wherein the conductively-doped epitaxial semiconductor material of the source/drain regions of the sense-line-amplifier transistors have a bottom-most surface that is lower than an uppermost surface of the at least one fin.

10 7. The DRAM circuitry of claim 1 wherein the conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors have a lower surface that is at the same elevation as an uppermost surface of the at least one fin.

8. The DRAM circuitry of claim 7 wherein the
15 conductively-doped epitaxial semiconductor material of the source/drain regions of the sense-line-amplifier transistors have a bottom-most surface that is lower than the uppermost surface of the at least one fin.

9. The DRAM circuitry of claim 1 comprising gate insulator between the at least one fin and the gates of the sense-line-amplifier
20 transistors and the wordline-driver transistors, the gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors being thinner than the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors.

10. The DRAM circuitry of claim 9 wherein the sense-line-
25 amplifier transistors collectively comprise NMOS transistors and PMOS transistors.

11. The DRAM circuitry of claim 9 wherein the gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors and the gate insulator that is between the at least one fin and the
30 gates of the wordline-driver transistors are of the same composition relative one another.

12. The DRAM circuitry of claim 11 wherein the same composition is silicon dioxide.

13. The DRAM circuitry of claim 11 wherein the gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors has thickness of 5 Angstroms to 30 Angstroms and the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors has thickness of 30 Angstroms to 60 Angstroms.

14. DRAM circuitry comprising:

a memory array comprising memory cells individually comprising a transistor and a charge-storage device, the transistors individually comprising two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array, one of the source/drain regions being electrically coupled to one of the charge-storage devices, the other of the source/drain regions being electrically coupled to one of multiple sense lines of the memory array;

peripheral circuitry comprising wordline-driver transistors having gates which individually comprise one of the wordlines and comprising sense-line-amplifier transistors having gates which individually comprise one of the sense lines;

the sense-line-amplifier transistors and the wordline-driver transistors individually being a finFET having at least one fin comprising a channel region of the respective finFET, the sense-line-amplifier transistors and the wordline-driver transistors individually comprising two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section;

the conductively-doped epitaxial semiconductor material of the source/drain regions of the sense-line-amplifier transistors having a bottom-most surface that is lower than an uppermost surface of the at least one fin;

the conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors having a lower surface that is at the same elevation as the uppermost surface of the at least one fin;

gate insulator between the at least one fin and the gates of the sense-line-amplifier transistors and the wordline-driver transistors, the gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors and the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors being of the same composition relative one another, the gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors being thinner than the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors.

15. The DRAM circuitry of claim 14 wherein the same composition is silicon dioxide.

16. The DRAM circuitry of claim 14 wherein the gate insulator that is between the at least one fin and the gates of the sense-line-amplifier transistors has thickness of 5 Angstroms to 30 Angstroms and the gate insulator that is between the at least one fin and the gates of the wordline-driver transistors has thickness of 30 Angstroms to 60 Angstroms.

17. The DRAM circuitry of claim 14 wherein the sense-line-amplifier transistors collectively comprise NMOS transistors and PMOS transistors.

18. The DRAM circuitry of claim 17 wherein,

the source/drain regions of the sense-line-amplifier transistors that comprise conductively-doped epitaxial semiconductor material of the NMOS transistors individually comprise silicon that is conductively-doped with phosphorus; and

the source/drain regions of the sense-line-amplifier transistors that comprise conductively-doped epitaxial semiconductor material of the PMOS transistors individually comprise a mixture of silicon and germanium that is conductively-doped with boron.

19. A method of forming DRAM circuitry, comprising:

forming a memory array comprising memory cells individually comprising a transistor and a charge-storage device, the transistors individually comprising two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array, one of the source/drain regions being electrically coupled to one of the charge-storage devices, the other of the source/drain regions being electrically coupled to one of multiple sense lines of the memory array;

forming peripheral circuitry comprising wordline-driver transistors having gates which individually comprise one of the wordlines and comprising sense-line-amplifier transistors having gates which individually comprise one of the sense lines; and

forming the sense-line-amplifier transistors and the wordline-driver transistors individually to be a finFET having at least one fin comprising a channel region of the respective finFET;

forming the sense-line-amplifier transistors and the wordline-driver transistors individually to comprise two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section; and

the forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors occurring before the forming of the conductively-doped epitaxial semiconductor material of the wordline-driver transistors.

20. The method of claim 19 sequentially comprising:

forming first masking blocks that individually are directly above the at least one fin of the sense-line-amplifier transistors and second masking blocks that individually are directly above the at least one fin of the wordline-driver transistors;

forming first sidewall spacers over two laterally-opposing sides of the first and second masking blocks;

forming the conductively-doped epitaxial semiconductor material of the source/drain regions of at least some of the sense-line-amplifier transistors laterally outward of the first masking blocks and the first sidewall spacers there-aside;

forming second sidewall spacers over two laterally-opposing sides of the first sidewall spacers that are laterally over each of the first and second masking blocks; and

forming the conductively-doped epitaxial semiconductor material of
5 the source/drain regions of at least some of the wordline-driver transistors laterally outward of the second masking blocks and the second sidewall spacers there-aside.

21. The method of claim 20 comprising using the second masking blocks with the first and second sidewall spacers there-aside as a mask while
10 epitaxially growing the conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors from an uppermost surface of the at least one fin to have a lower surface that is at the same elevation as the uppermost surface of the at least one fin.

22. The method of claim 20 comprising:
15 using the first masking blocks and the first sidewall spacers there-aside as a mask while etching two recesses into substrate material that is laterally adjacent the at least one fin of the sense-line-amplifier transistors; and

epitaxially growing the conductively-doped epitaxial semiconductor
20 material of the source/drain regions of the sense-line-amplifier transistors from the recesses to have a bottom-most surface that is lower than an uppermost surface of the at least one fin.

23. The method of claim 22 comprising using the second masking blocks with the first and second sidewall spacers there-aside as a mask while
25 epitaxially growing the conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors from an uppermost surface of the at least one fin to have a lower surface that is at the same elevation as the uppermost surface of the at least one fin.

24. The method of claim 20 comprising:
30 forming the sense-line-amplifier transistors to collectively comprise NMOS transistors and PMOS transistors;

the forming of the conductively-doped epitaxial semiconductor material of the source/drain regions of the least some of the sense-line-amplifier transistors laterally outward of the first masking blocks and the first sidewall spacers there-aside being p-type of the PMOS transistors being formed;

forming intermediate sidewall spacers laterally aside the first masking blocks and the first sidewall spacers of another some of the sense-line-amplifier transistors which are the NMOS transistors being formed and before forming the second sidewall spacers; and

the forming the conductively-doped epitaxial semiconductor material of the source/drain regions of the NMOS transistors laterally outward of the first masking blocks having the first and intermediate spacers there-aside to be n-type of the NMOS transistors being formed and before forming the second sidewall spacers.

25. The method of claim 19 comprising forming the at least one fin of the sense-line-amplifier transistors and the wordline-driver transistors at the same time.

26. A method of forming DRAM circuitry, comprising:

forming a memory array comprising memory cells individually comprising a transistor and a charge-storage device, the transistors individually comprising two source/drain regions having a gate there-between that is part of one of multiple wordlines of the memory array, one of the source/drain regions being electrically coupled to one of the charge-storage devices, the other of the source/drain regions being electrically coupled to one of multiple sense lines of the memory array;

forming peripheral circuitry comprising wordline-driver transistors having gates which individually comprise one of the wordlines and comprising sense-line-amplifier transistors having gates which individually comprise one of the sense lines;

forming the sense-line-amplifier transistors and the wordline-driver transistors individually to be a finFET having at least one fin comprising a channel region of the respective finFET;

forming the sense-line-amplifier transistors and the wordline-driver transistors individually to comprise two source/drain regions that individually comprise conductively-doped epitaxial semiconductor material that is adjacent one of two laterally-opposing sides of the at least one fin in a vertical cross-section; and

the forming of the wordline-driver transistors occurring before the forming of the conductively-doped epitaxial semiconductor material of the sense-line-amplifier transistors.

27. The method of claim 26 sequentially comprising:

forming first masking blocks that individually are directly above the at least one fin of the sense-line-amplifier transistors and second masking blocks that individually are directly above the at least one fin of the wordline-driver transistors;

forming sidewall spacers over two laterally-opposing sides of the first and second masking blocks;

removing at least some material of the sidewall spacers from individual of the second masking blocks;

forming the conductively-doped epitaxial semiconductor material of the source/drain regions of the wordline-driver transistors laterally outward of the second masking blocks;

forming more sidewall spacers over the first and second masking blocks; and

forming the conductively-doped epitaxial semiconductor material of the source/drain regions of the sense-line-amplifier transistors laterally outward of the first masking blocks and the more sidewall spacers there-aside.

28. The method of claim 26 comprising forming the at least one fin of the sense-line-amplifier transistors and the wordline-driver transistors at the same time.

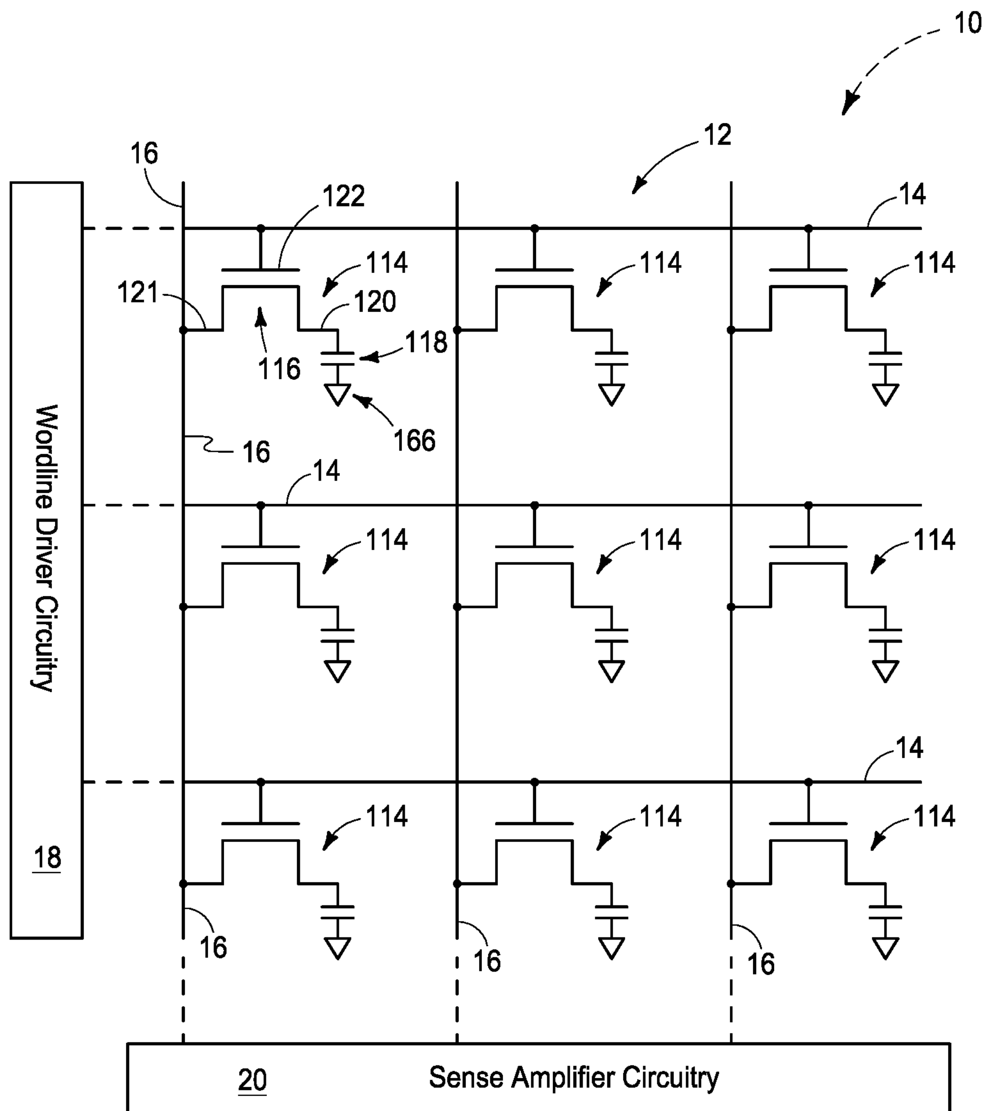


FIG. 1

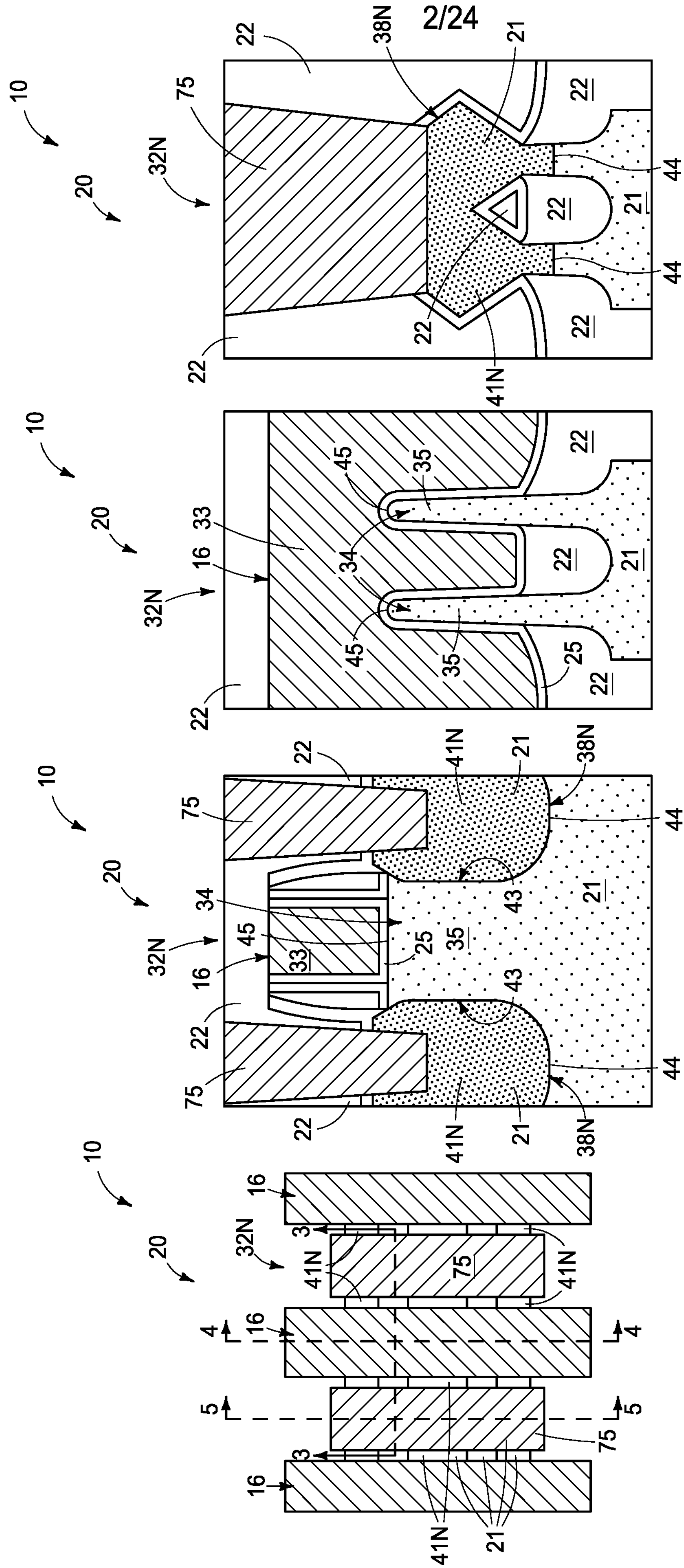


FIG. 2

FIG. 3

FIG. 4

FIG. 5

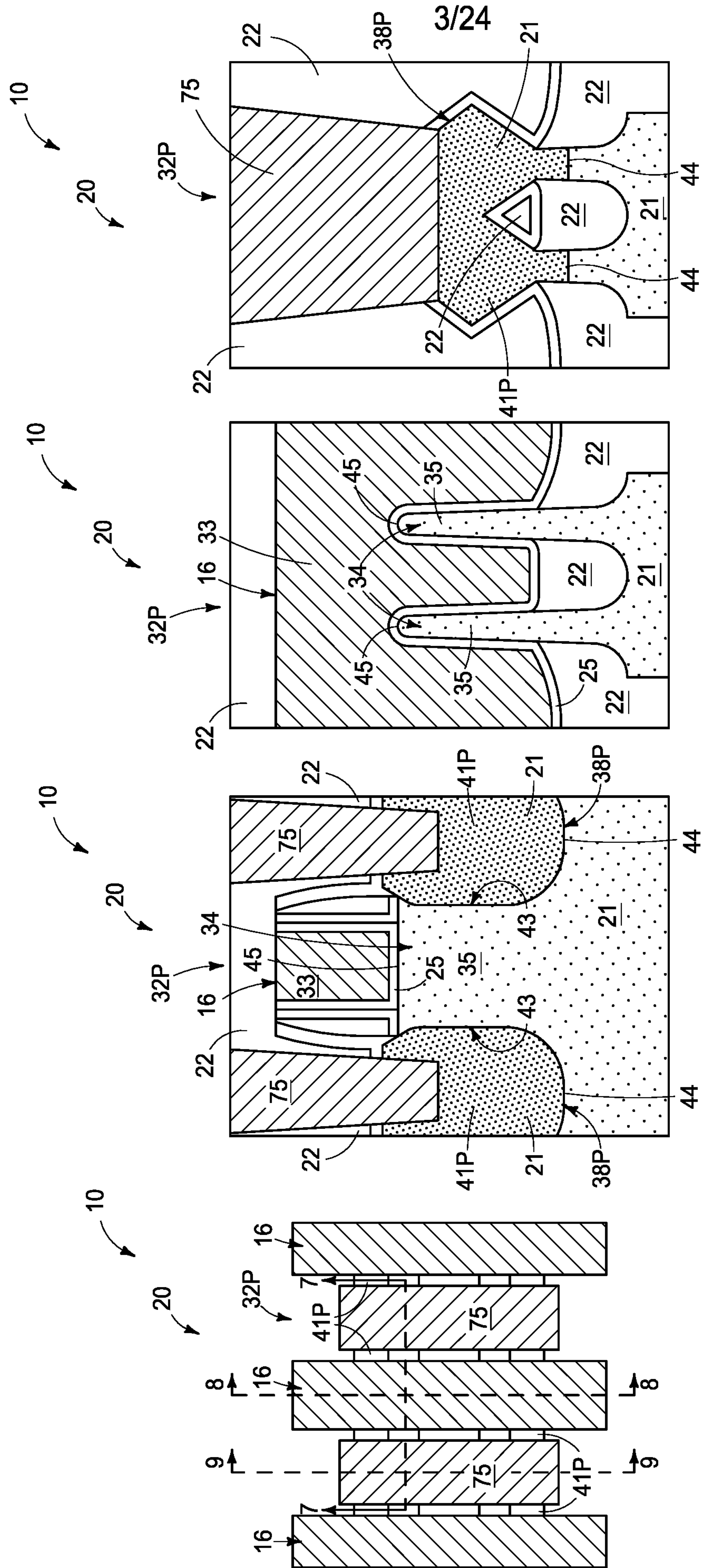


FIG. 6

FIG. 7

FIG. 8

FIG. 9

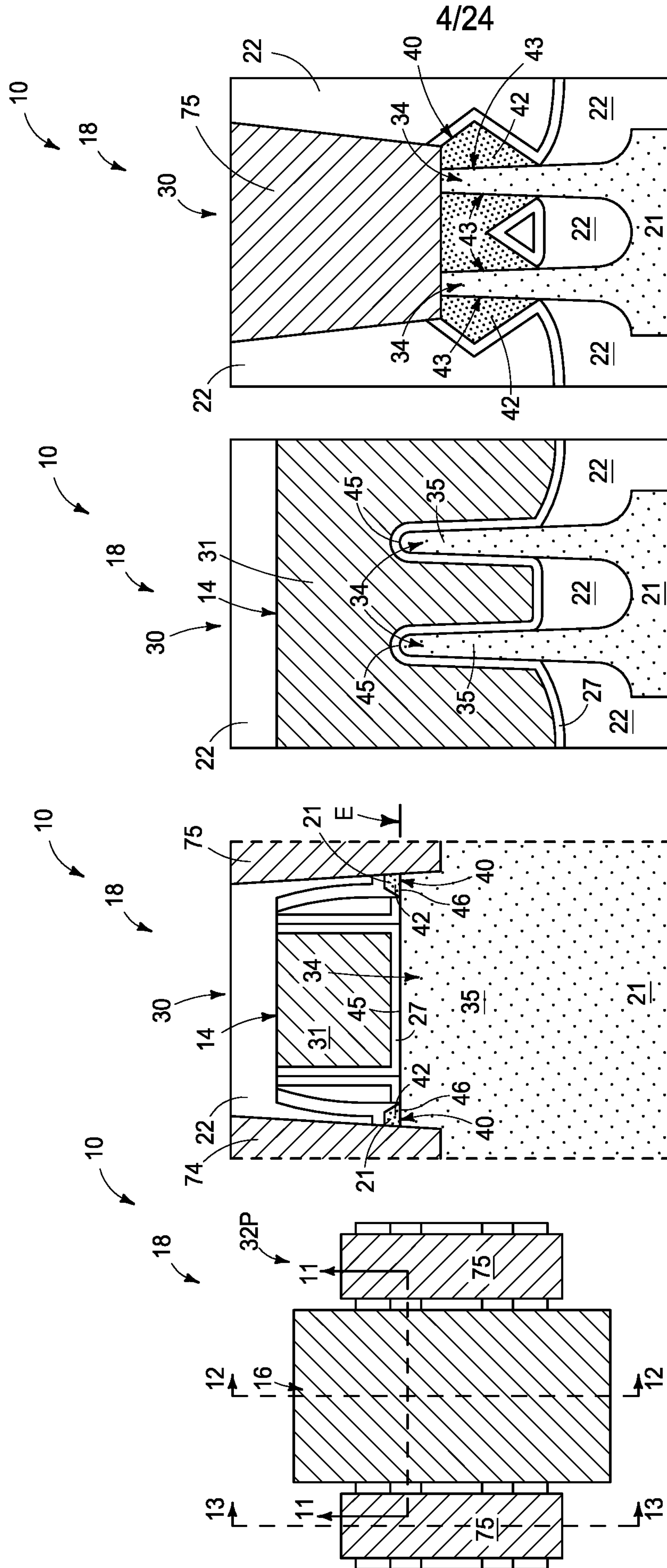


FIG. 10

FIG. 11

FIG. 12

FIG. 13

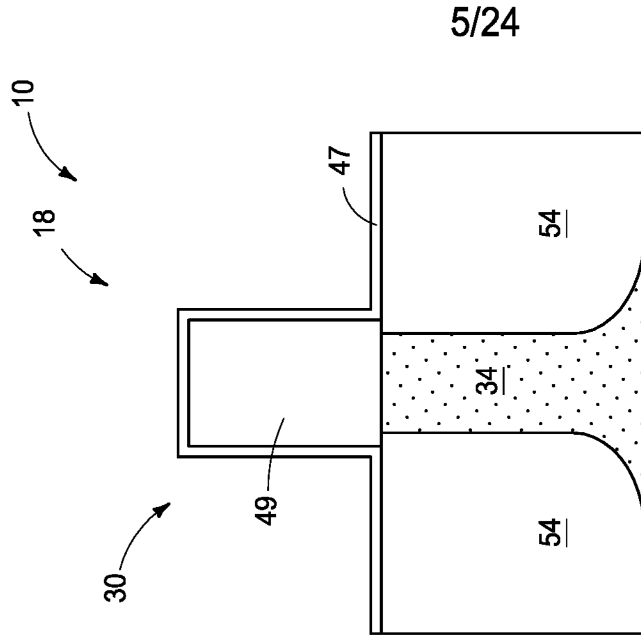
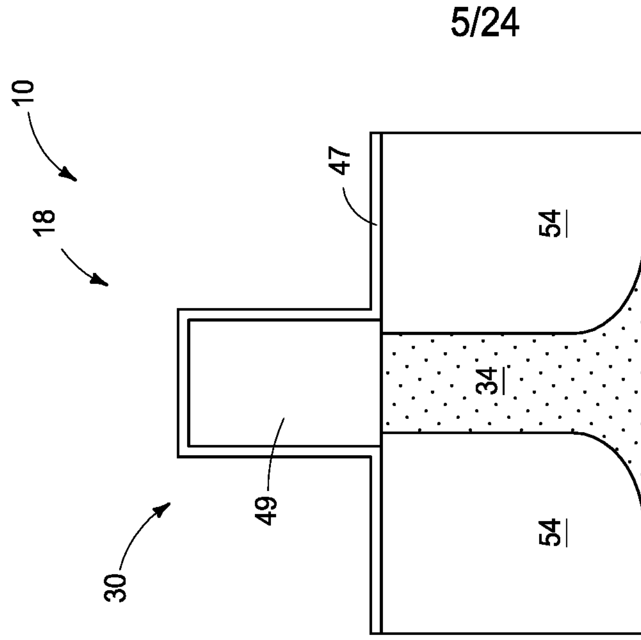


FIG. 16



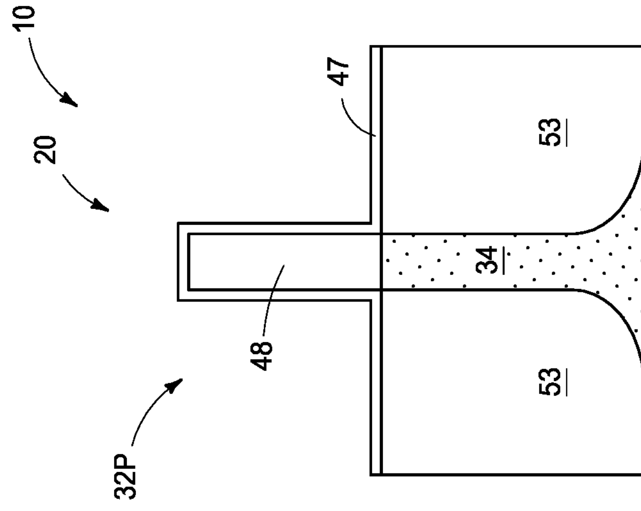


FIG. 15

10
20
47
52
34
48
52
32N

FIG. 14

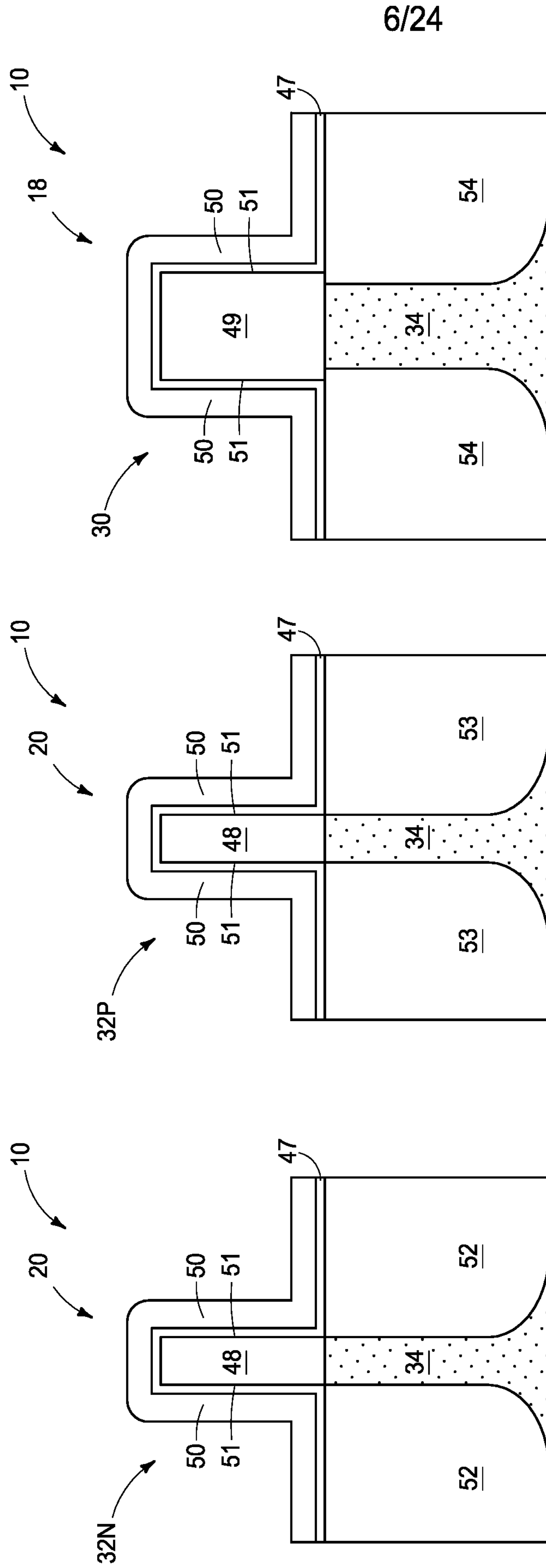


FIG. 19

FIG. 18

FIG. 17

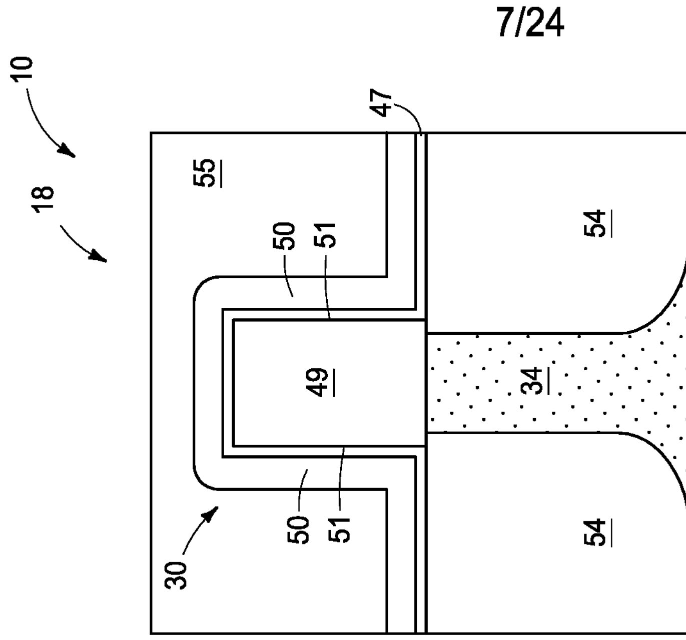


FIG. 22

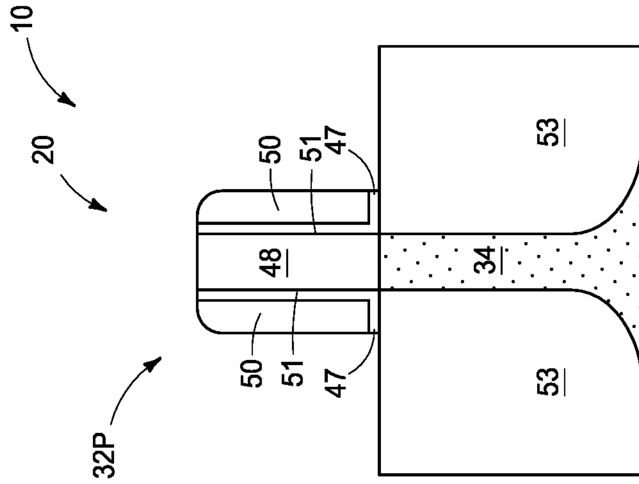


FIG. 21

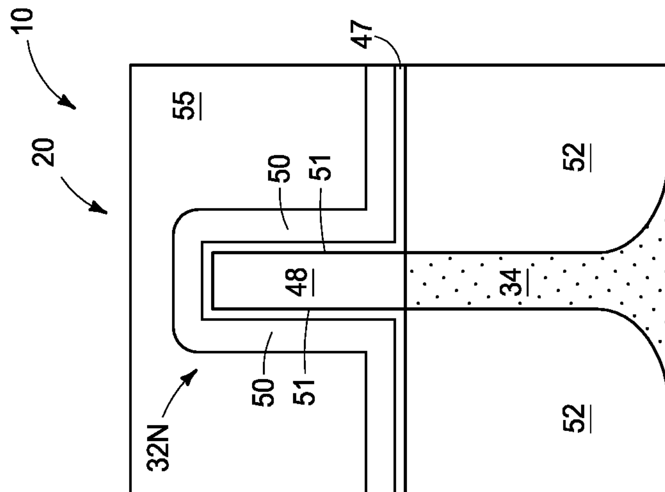
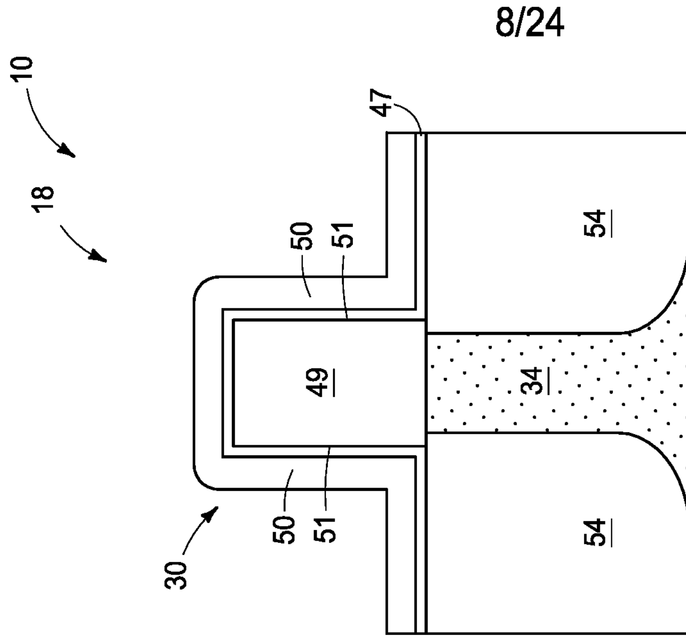


FIG. 20



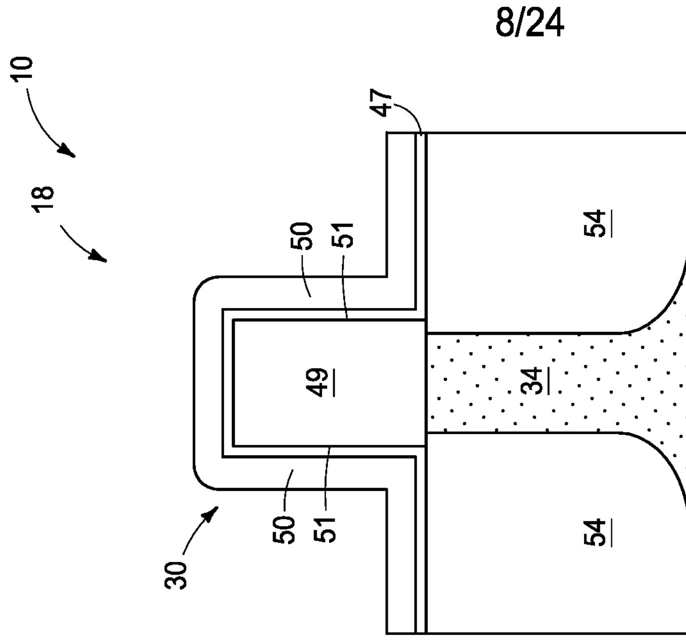


FIG. 25

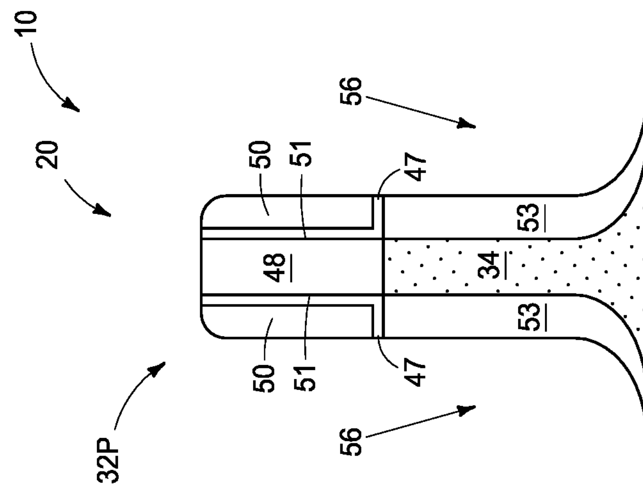


FIG. 24

10
20
47
50
51
48
34
52
52
50
51
32N

FIG. 23

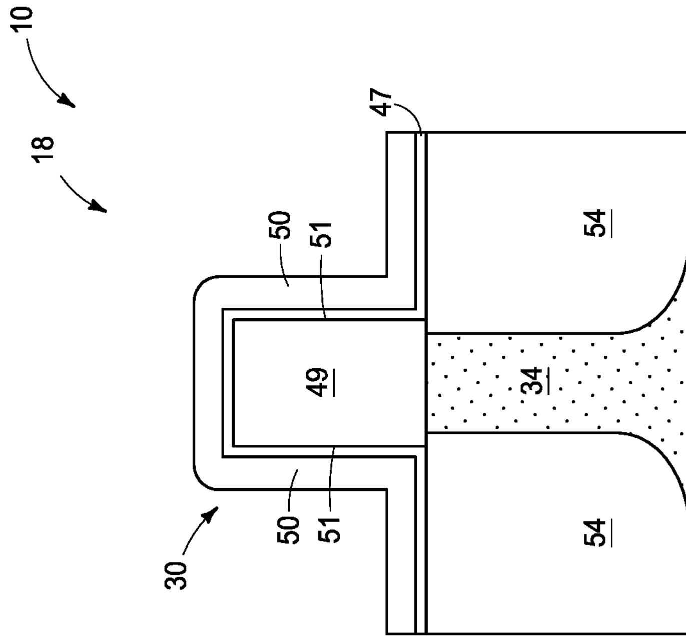


FIG. 28

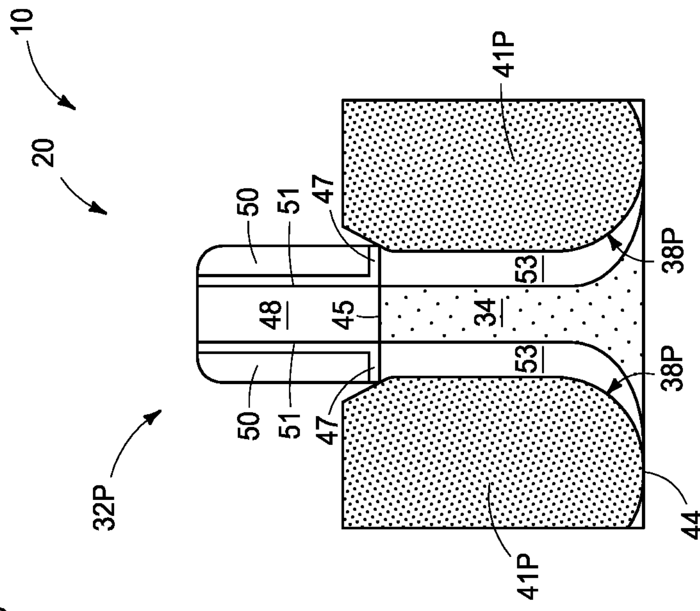


FIG. 27

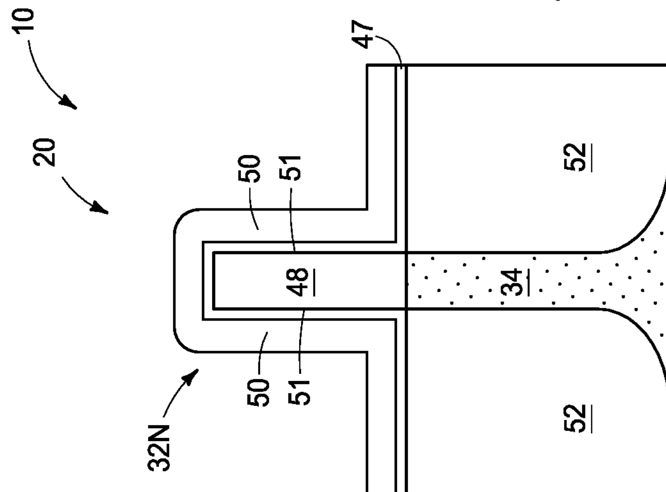


FIG. 26

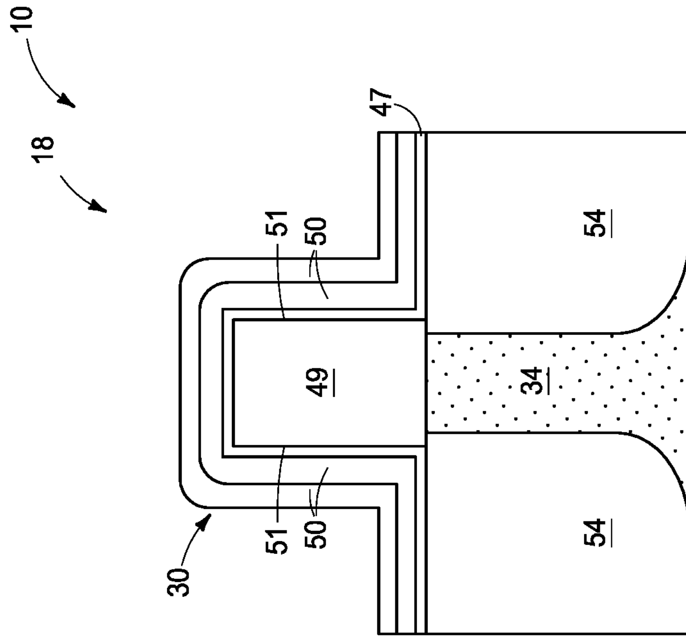
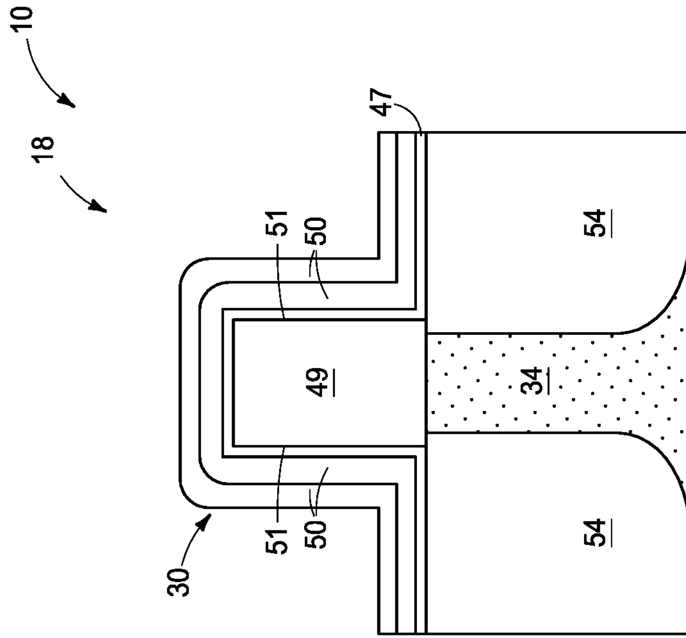


FIG. 31



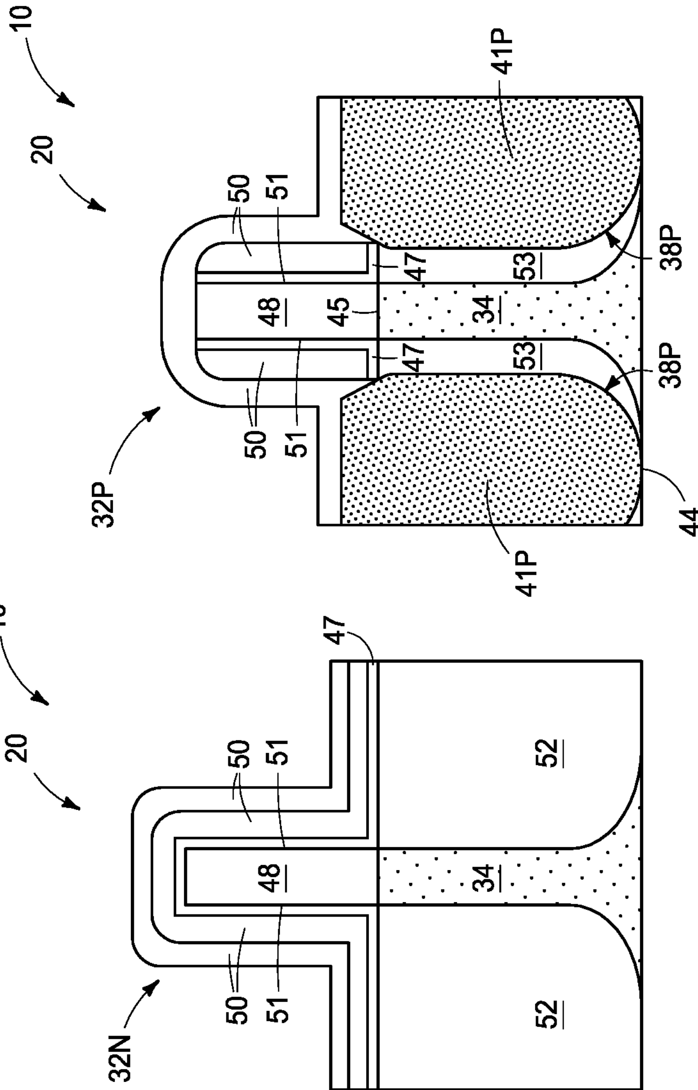


FIG. 30

FIG. 29

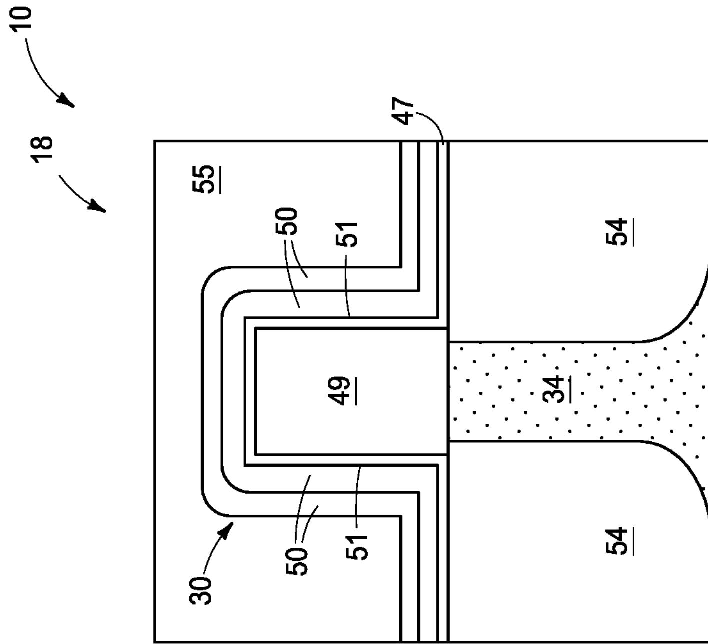


FIG. 34

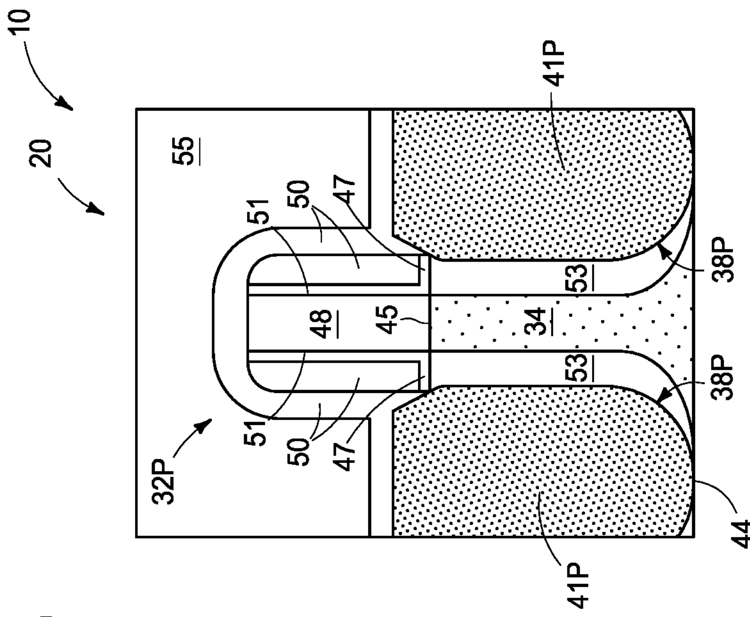


FIG. 33

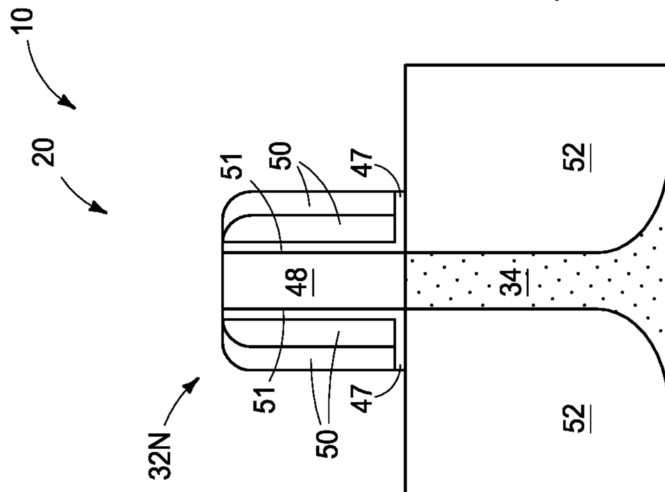


FIG. 32

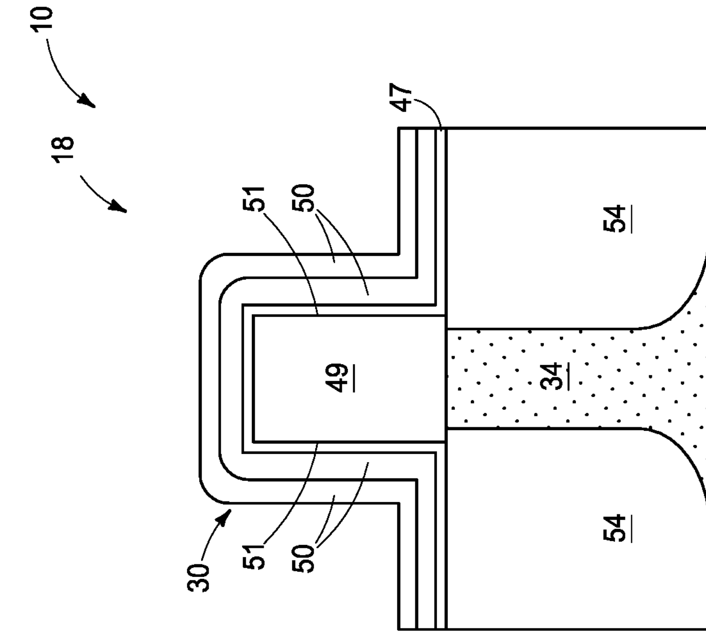


FIG. 37

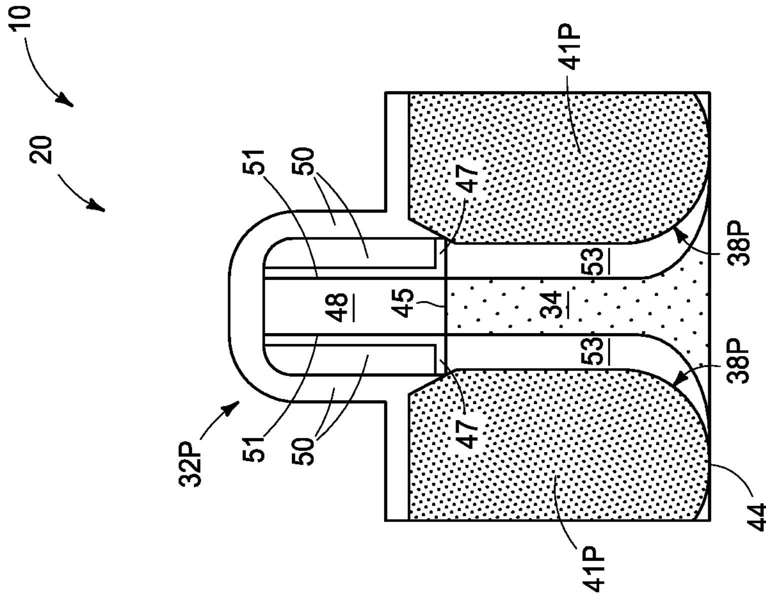


FIG. 36

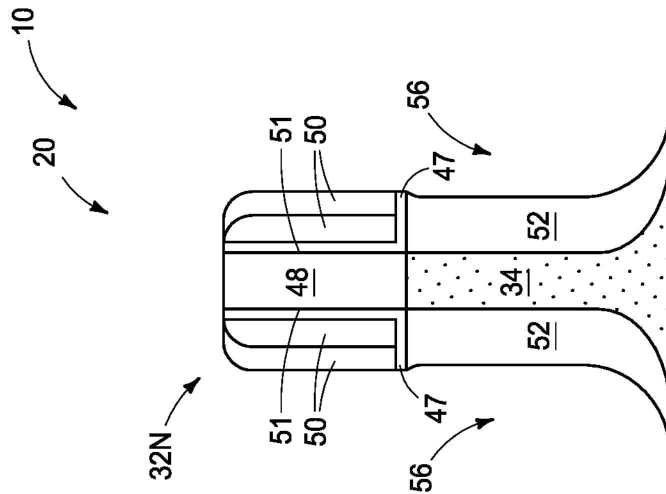


FIG. 35

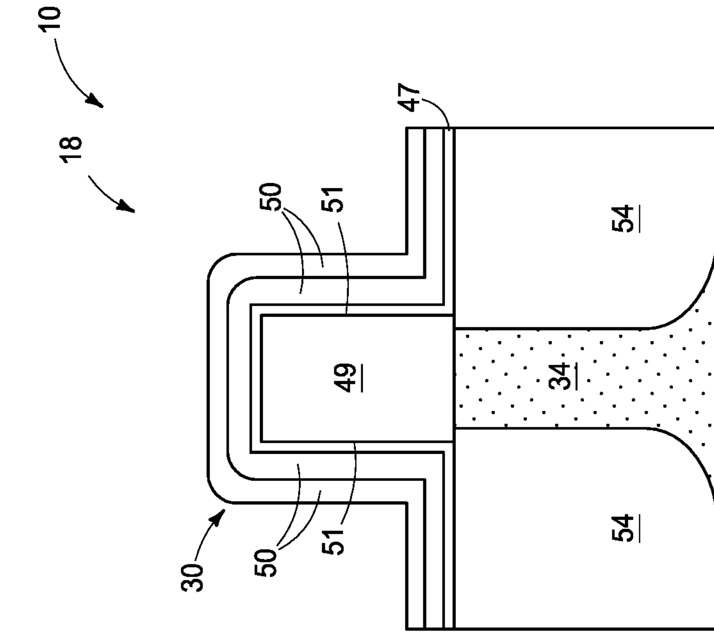


FIG. 40

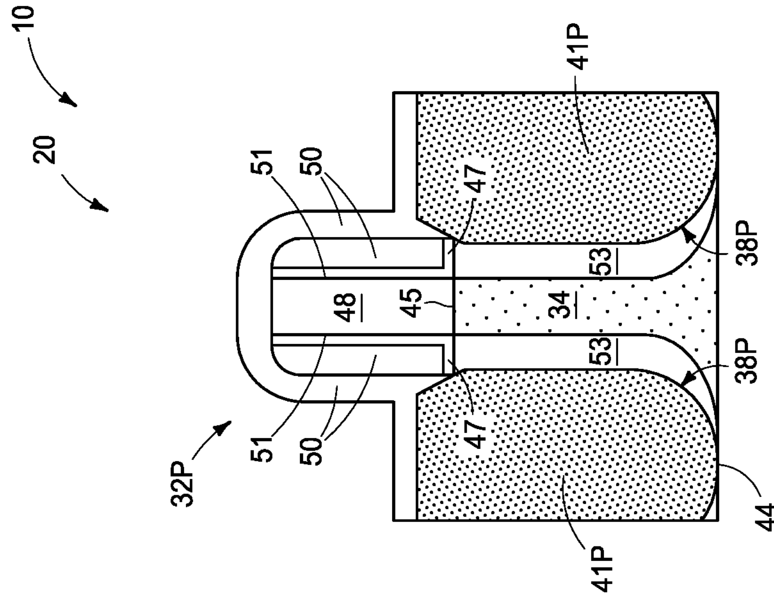


FIG. 39

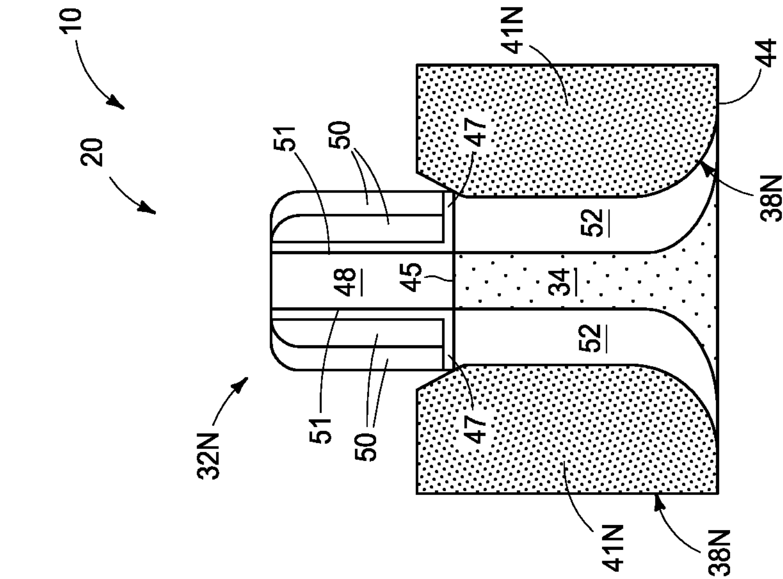


FIG. 38

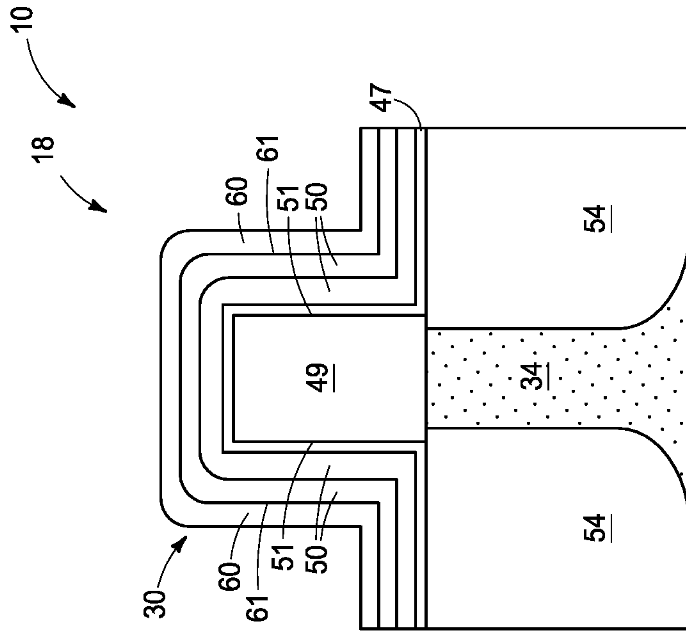


FIG. 43

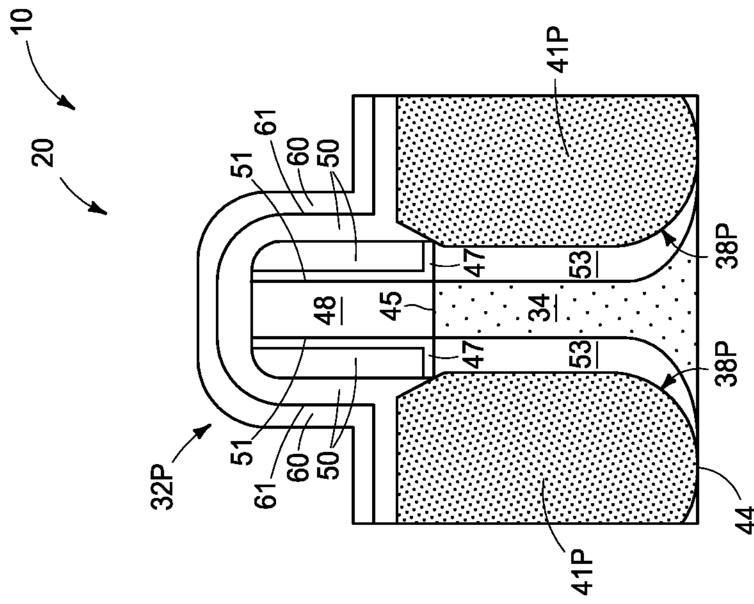


FIG. 42

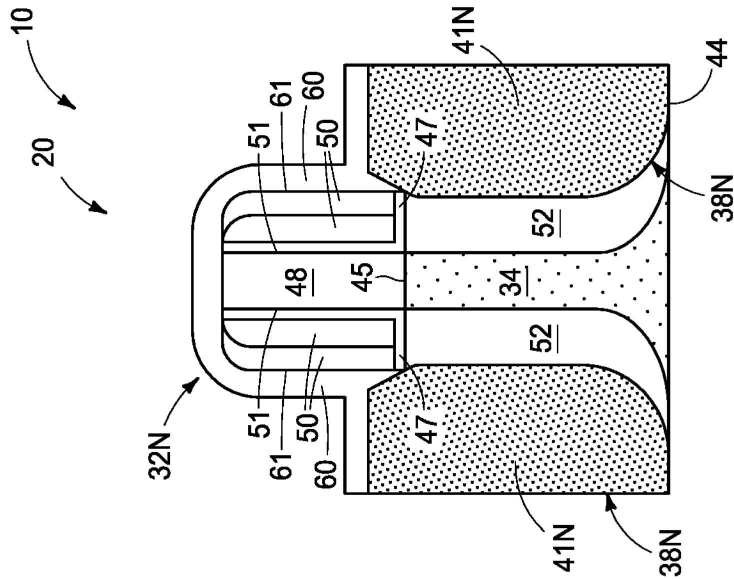


FIG. 41

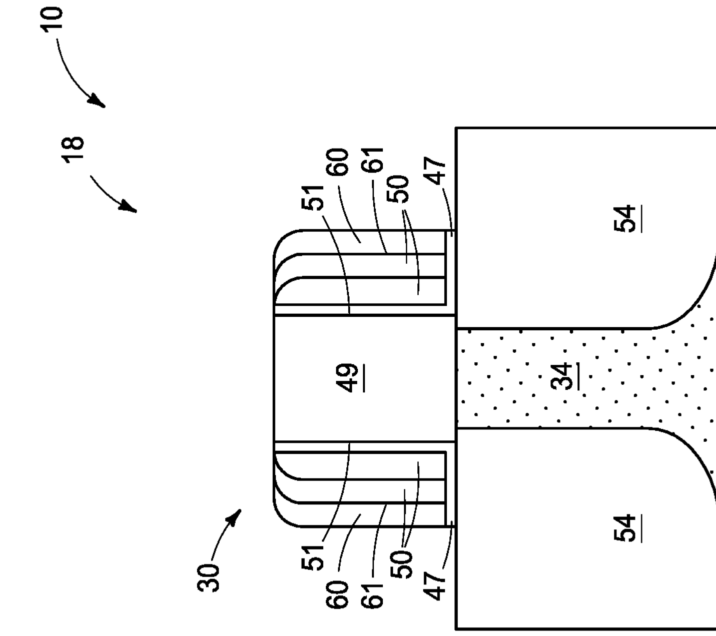
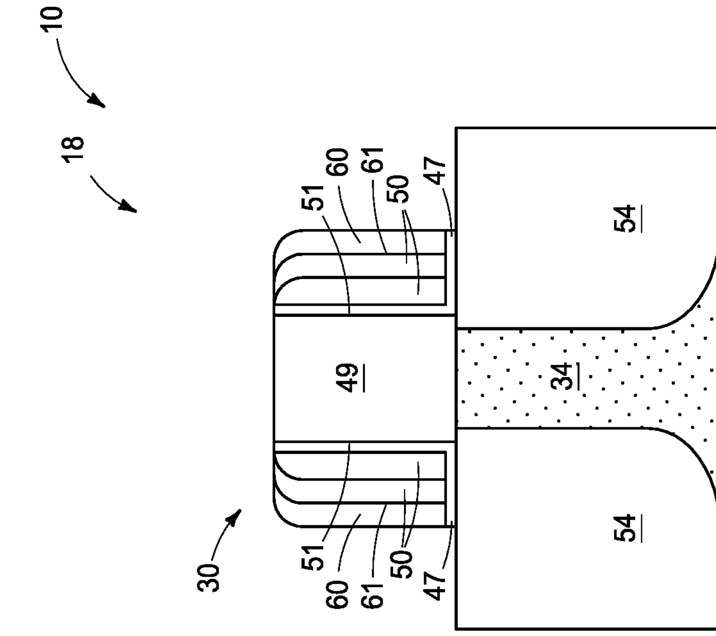


FIG. 46



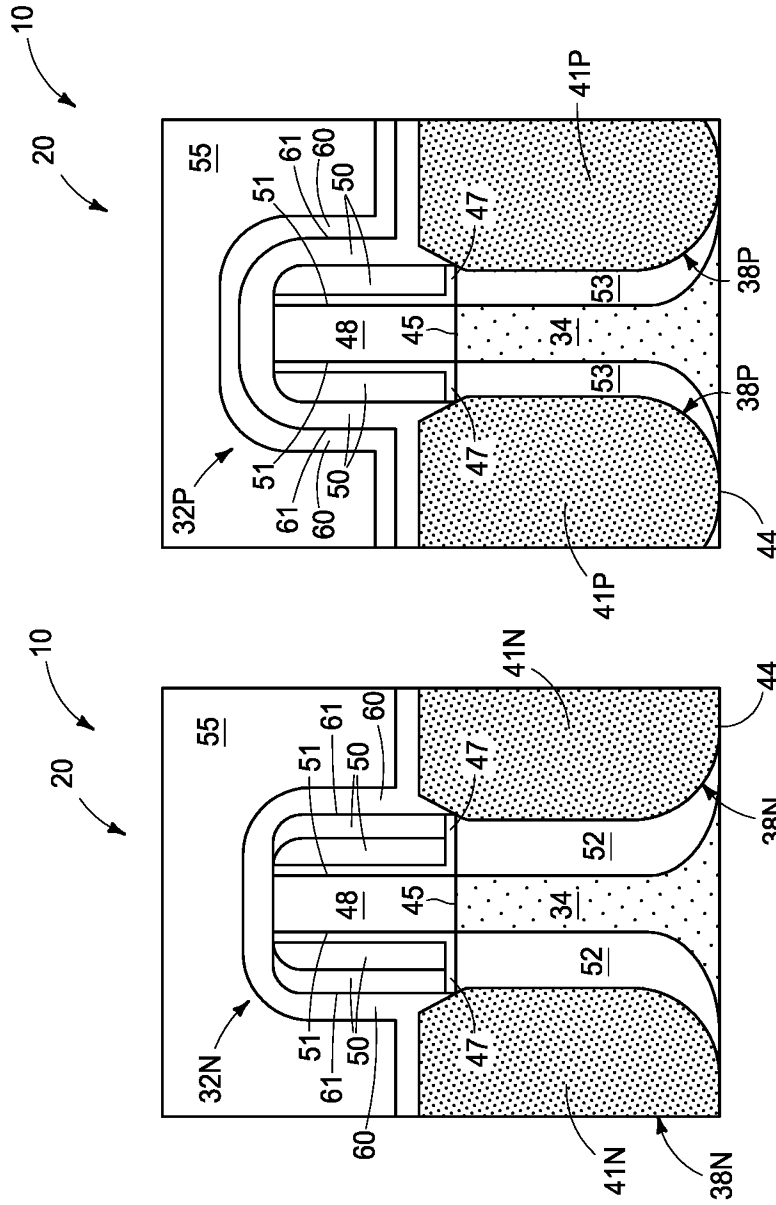


FIG. 45

FIG. 44

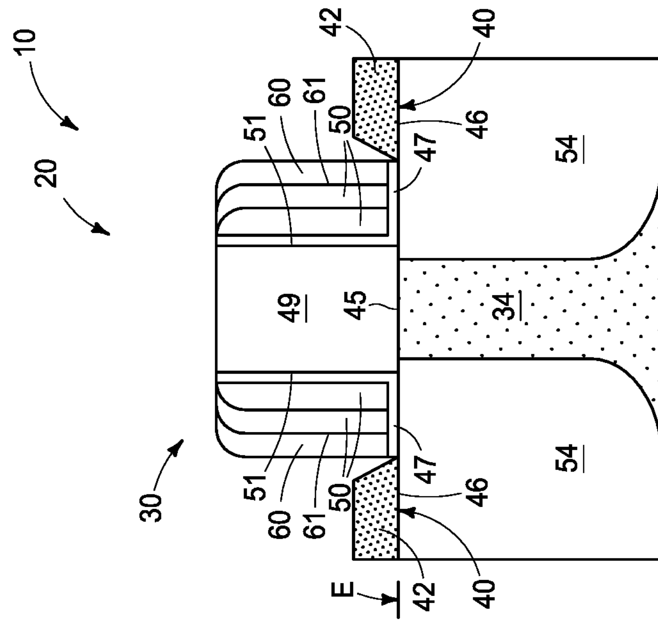


FIG. 49

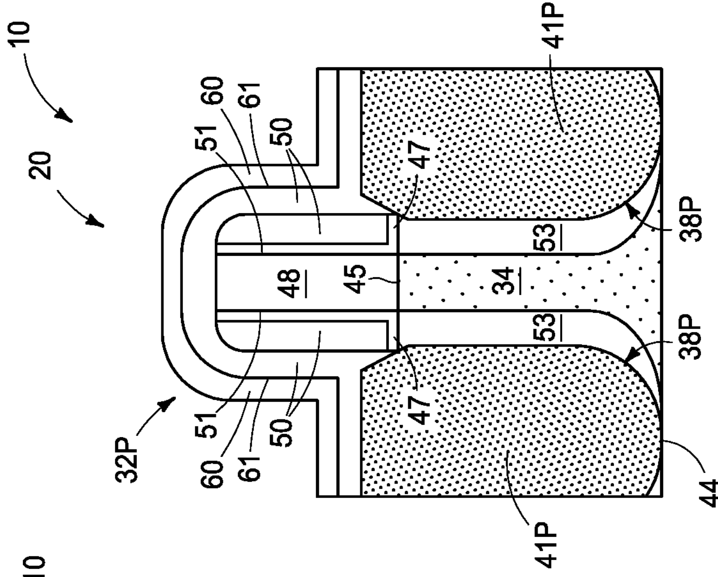


FIG. 48

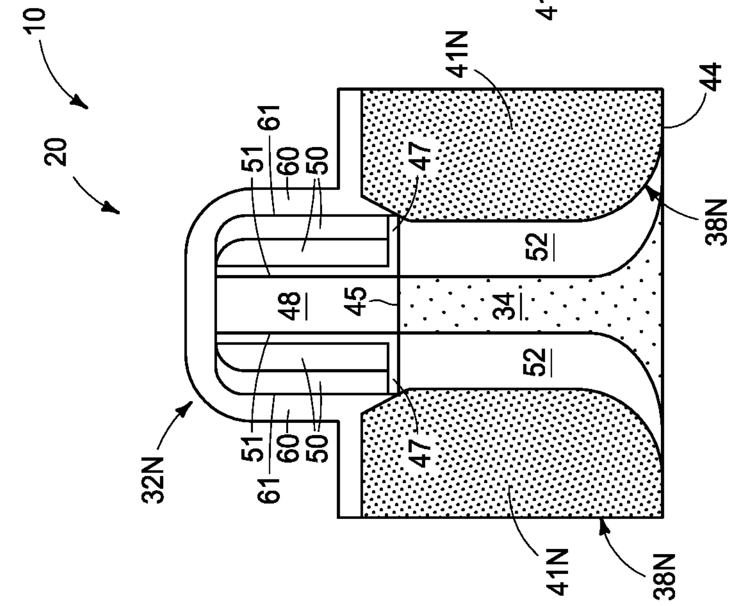
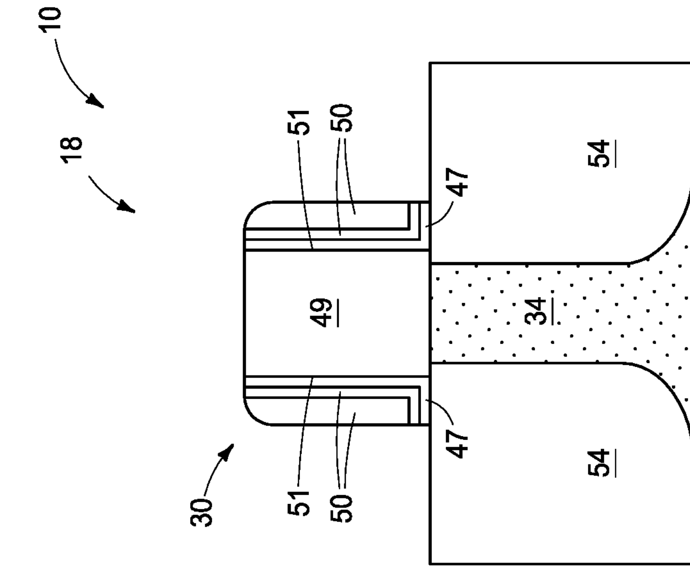


FIG. 47



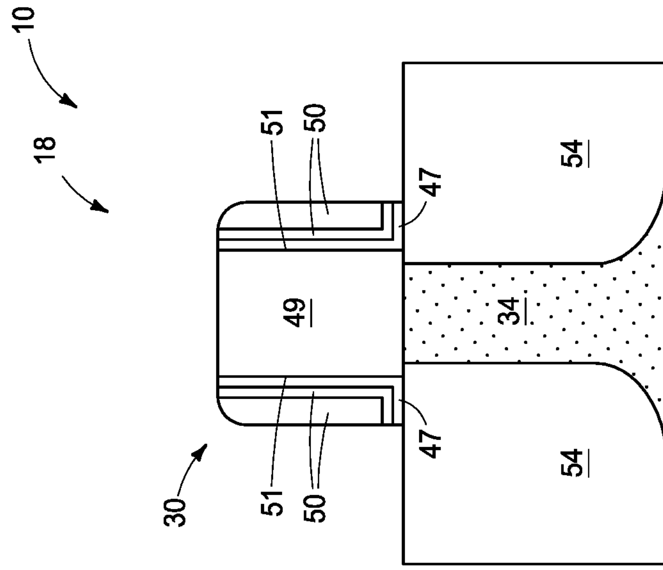


FIG. 52

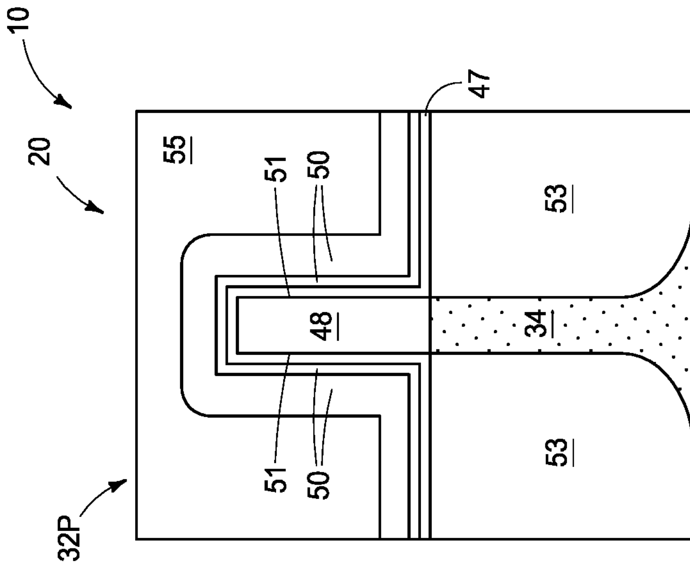


FIG. 51

FIG. 50

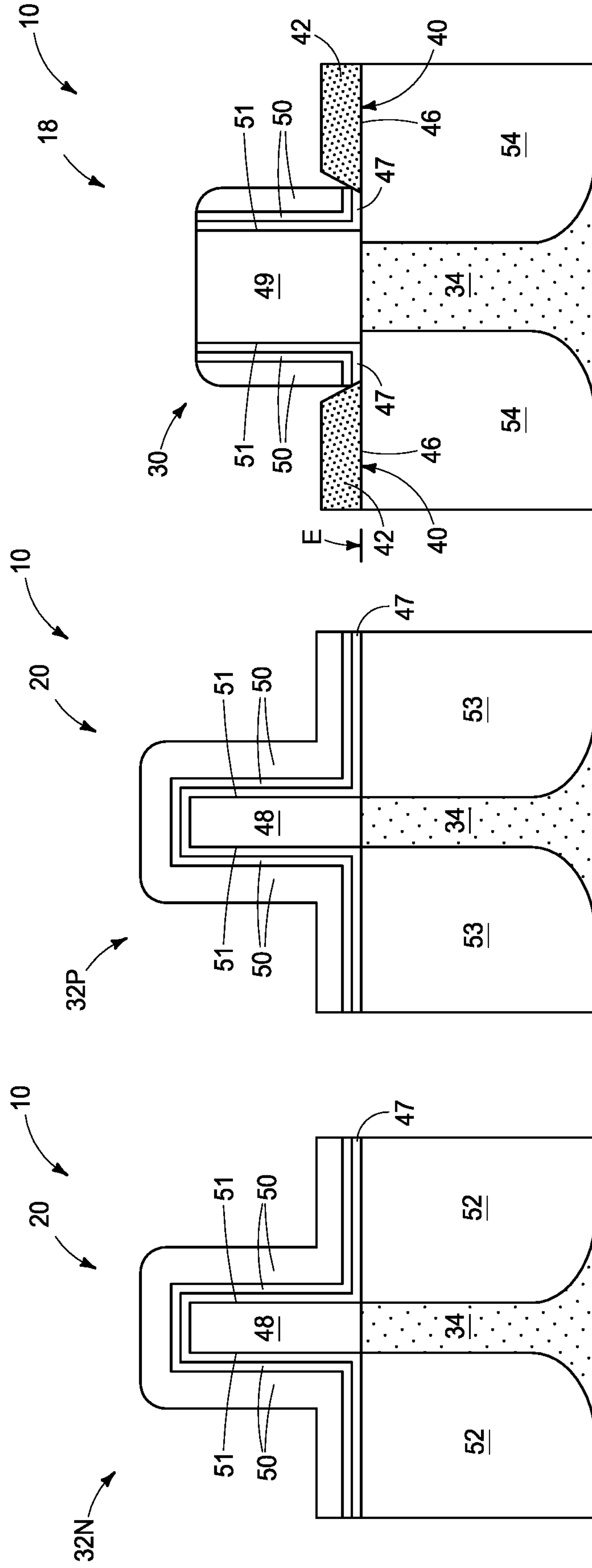


FIG. 55

FIG. 54

FIG. 53

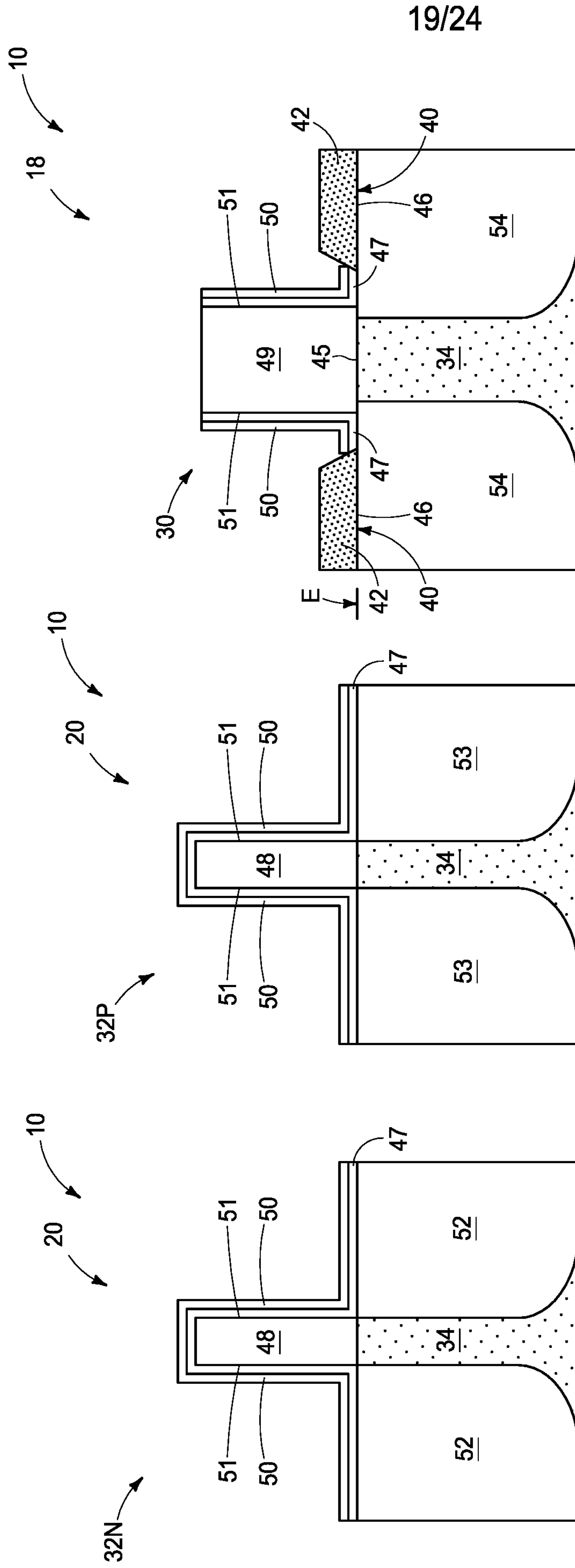


FIG. 58

FIG. 57

FIG. 56

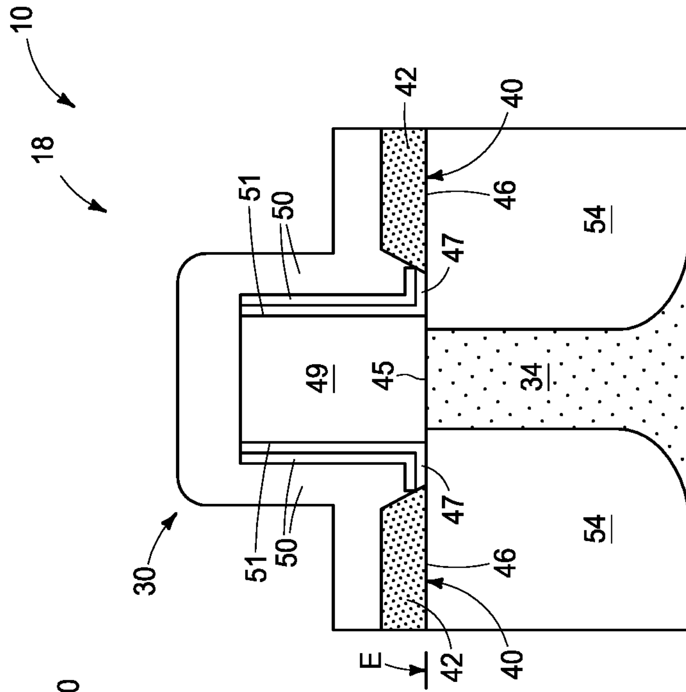
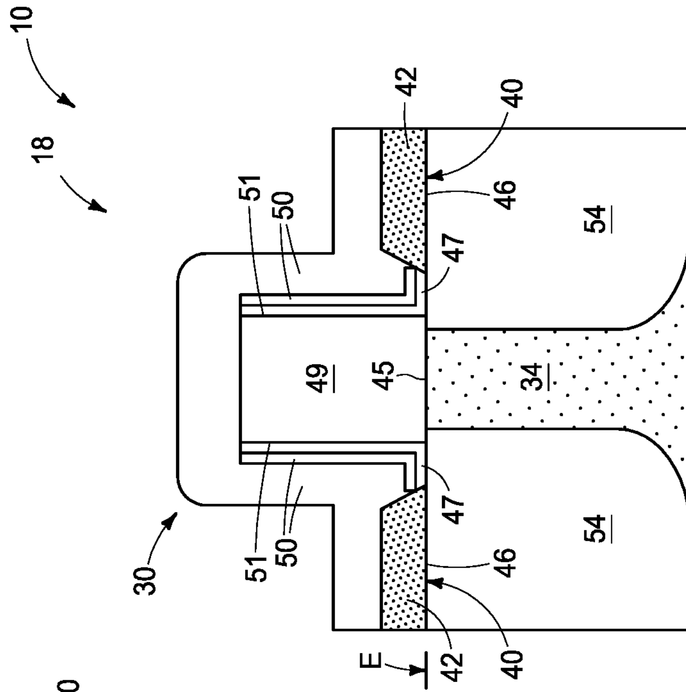


FIG. 61



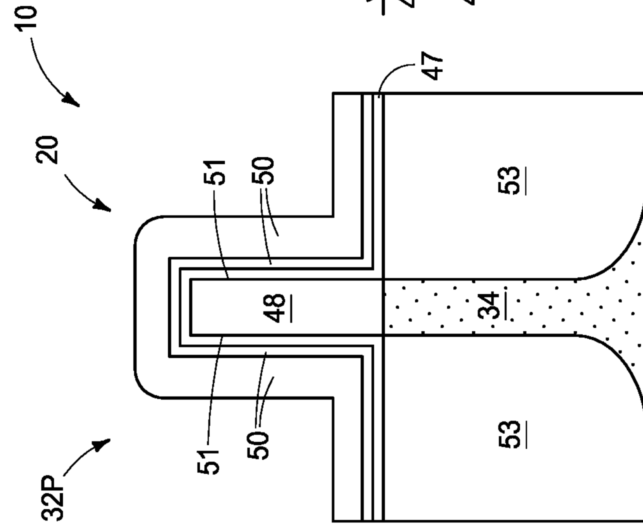


FIG. 60

FIG. 59

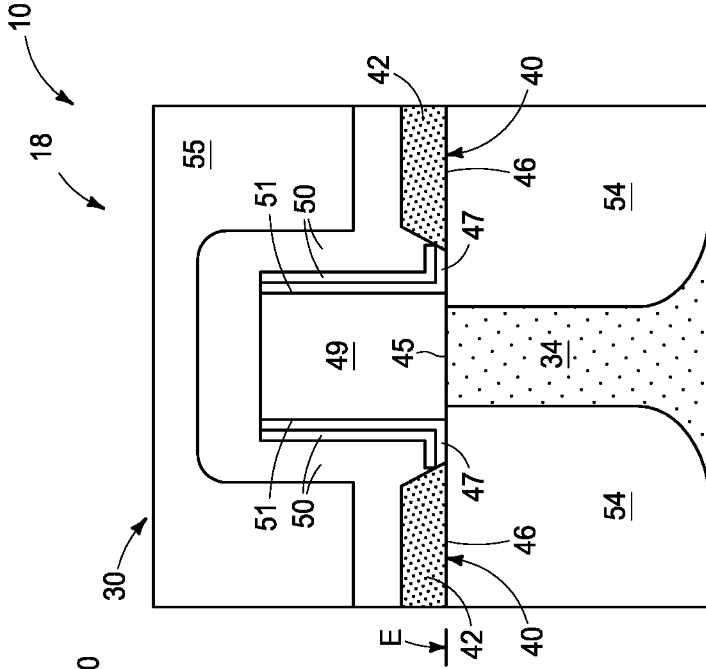


FIG. 64

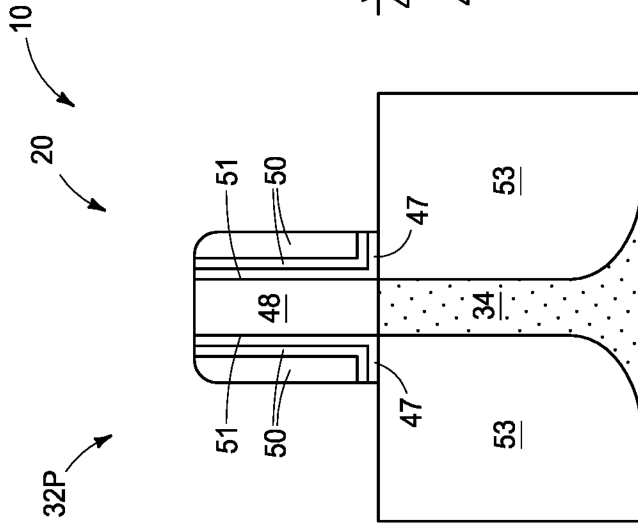


FIG. 63

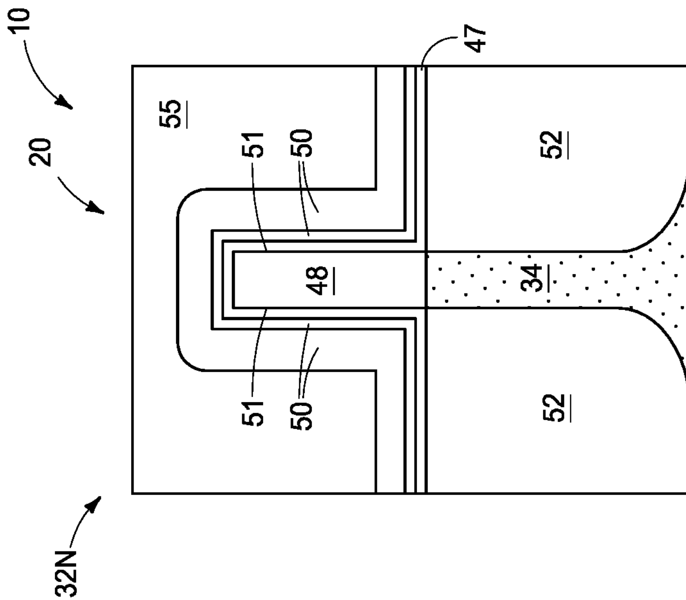


FIG. 62

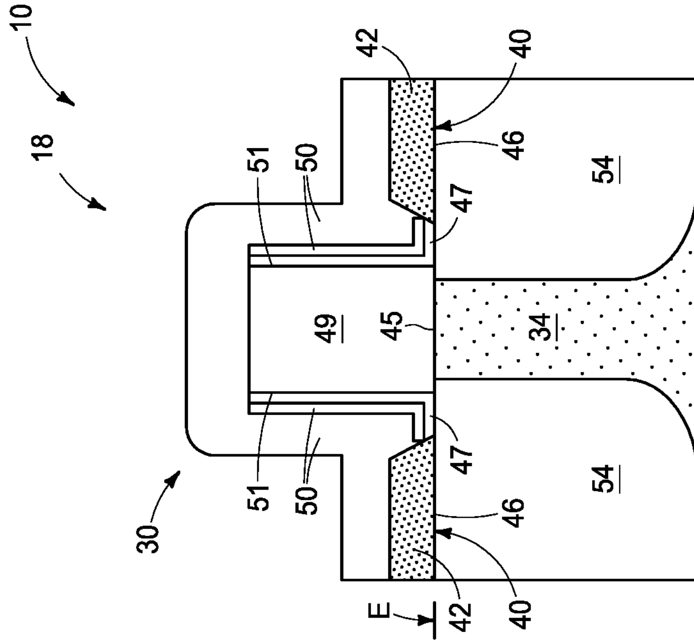


FIG. 67

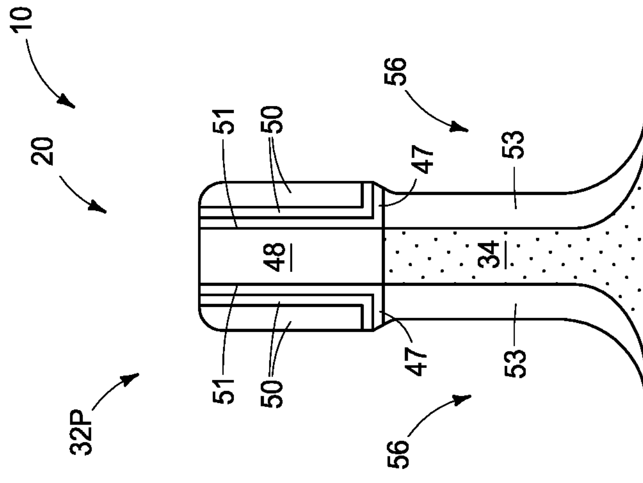


FIG. 66

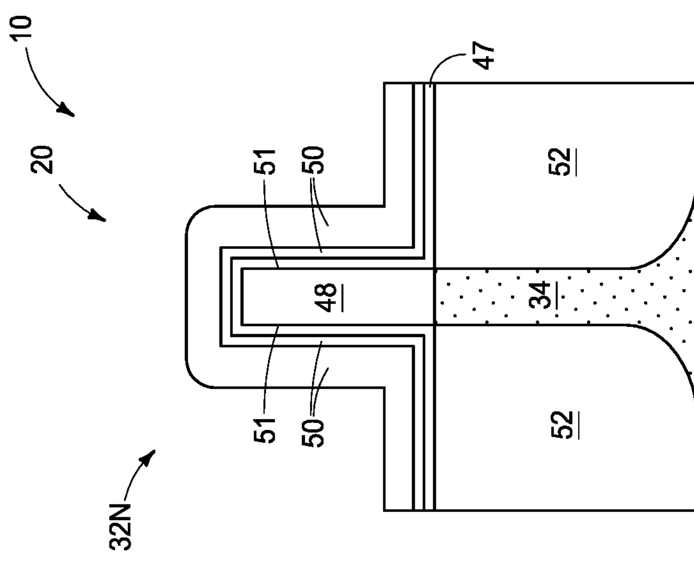


FIG. 65

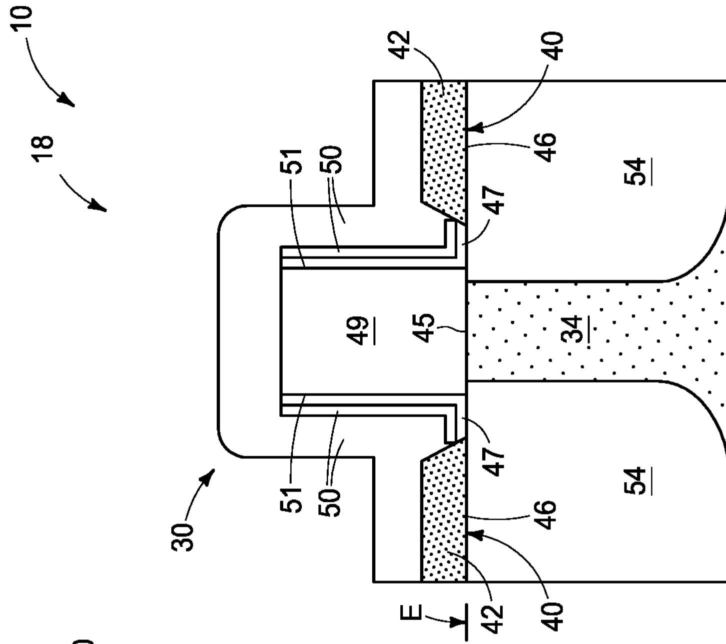
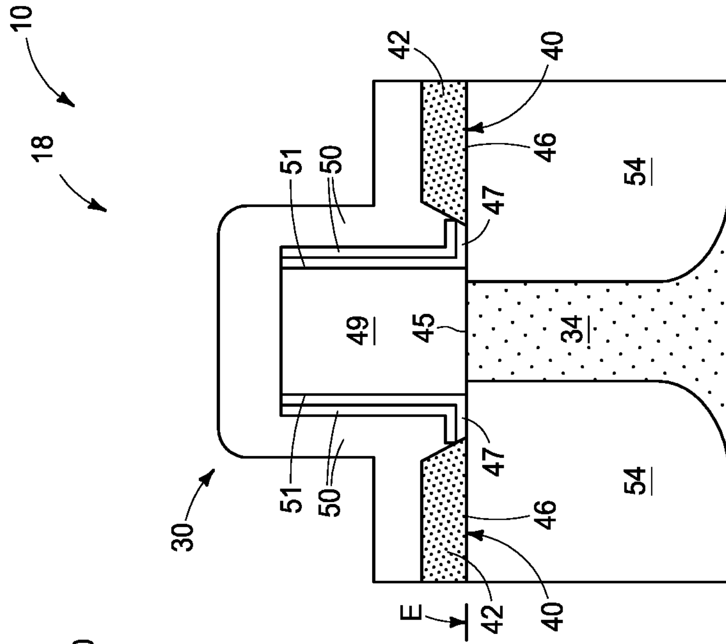


FIG. 70



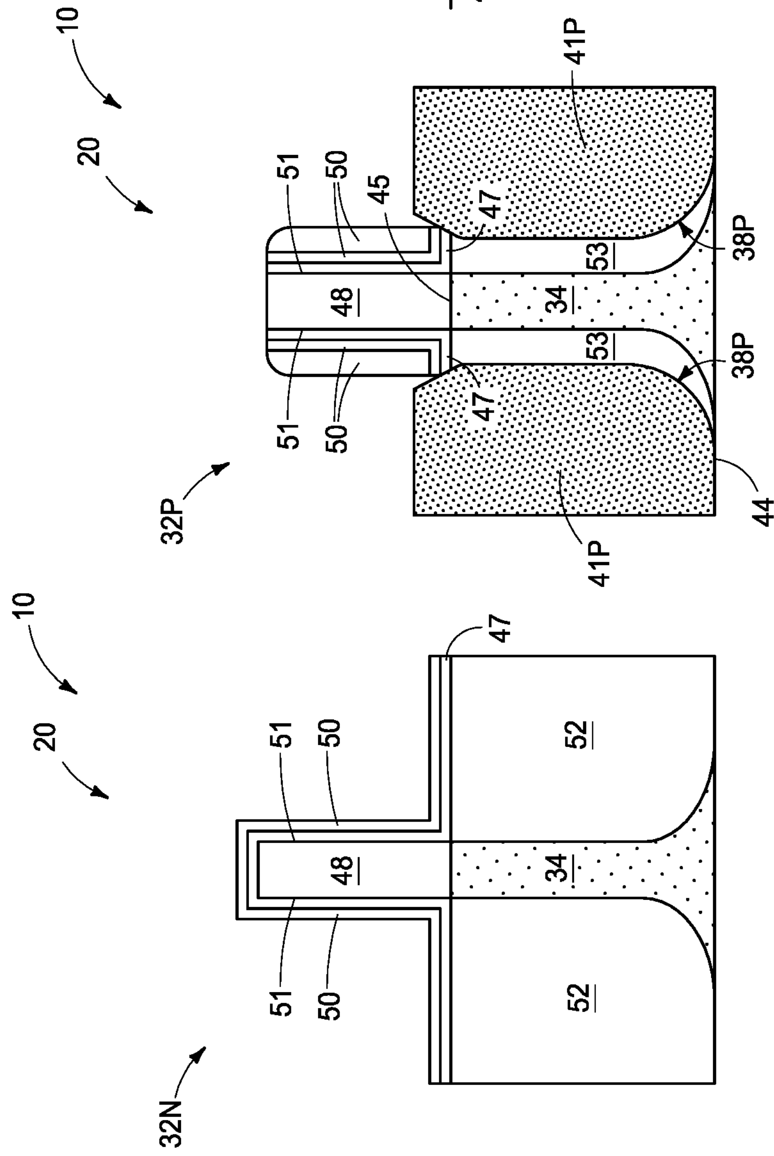


FIG. 69

FIG. 68

FIG. 71

FIG. 72

FIG. 73

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/034440

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/108(2006.01)i; **H01L 27/092**(2006.01)i; **H01L 29/78**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/108(2006.01); H01L 21/308(2006.01); H01L 21/8234(2006.01); H01L 27/11(2006.01); H01L 29/08(2006.01); H01L 29/161(2006.01); H01L 29/167(2006.01); H01L 29/36(2006.01); H01L 29/66(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: DRAM circuitry, wordlines-driver transistors, sense-line-amplifier transistors, finFET, conductively-doped epitaxial semiconductor material

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002-0122344 A1 (RIICHIRO TAKEMURA et al.) 05 September 2002 (2002-09-05) See paragraphs [0050], [0060] and figures 1A, 4.	1-28
Y	US 2015-0333075 A1 (SAMSUNG ELECTRONICS CO., LTD.) 19 November 2015 (2015-11-19) See paragraphs [0103]-[0220] and figures 17-28.	1-28
Y	US 2017-0133275 A1 (SAMSUNG ELECTRONICS CO., LTD.) 11 May 2017 (2017-05-11) See paragraphs [0078]-[0111] and figures 3-11.	4-5,12,15,18-28
A	US 2019-0259840 A1 (SAMSUNG ELECTRONICS CO., LTD.) 22 August 2019 (2019-08-22) See paragraphs [0019]-[0122] and figures 1A-7D.	1-28
A	US 2019-0198640 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 27 June 2019 (2019-06-27) See paragraphs [0024]-[0082] and figures 1-14.	1-28

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
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"D" document cited by the applicant in the international application
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 October 2022	**27 October 2022**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**PARK, Hye Lyun**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-3463**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2022/034440

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