

[72] Inventor **Gilbert R. Grado**  
17611 Orange Tree Lane, Tustin, Calif.  
92680

[21] Appl. No. **819,181**

[22] Filed **Apr. 25, 1969**

[45] Patented **June 22, 1971**

[56] **References Cited**  
**UNITED STATES PATENTS**

|           |         |                    |              |
|-----------|---------|--------------------|--------------|
| 3,264,457 | 8/1966  | Seegmiller et al.  | 235/150.53   |
| 3,320,409 | 5/1967  | Carrowe            | 235/197 X    |
| 3,345,505 | 10/1967 | Schmid             | 235/197      |
| 3,373,273 | 3/1968  | Schubert           | 235/150.53 X |
| 3,480,767 | 11/1969 | Hower              | 235/150.53   |
| 3,484,622 | 12/1969 | Keiper, Jr. et al. | 235/197 X    |

Primary Examiner—Malcolm A. Morrison  
Assistant Examiner—Joseph F. Ruggiero  
Attorney—White and Haefliger

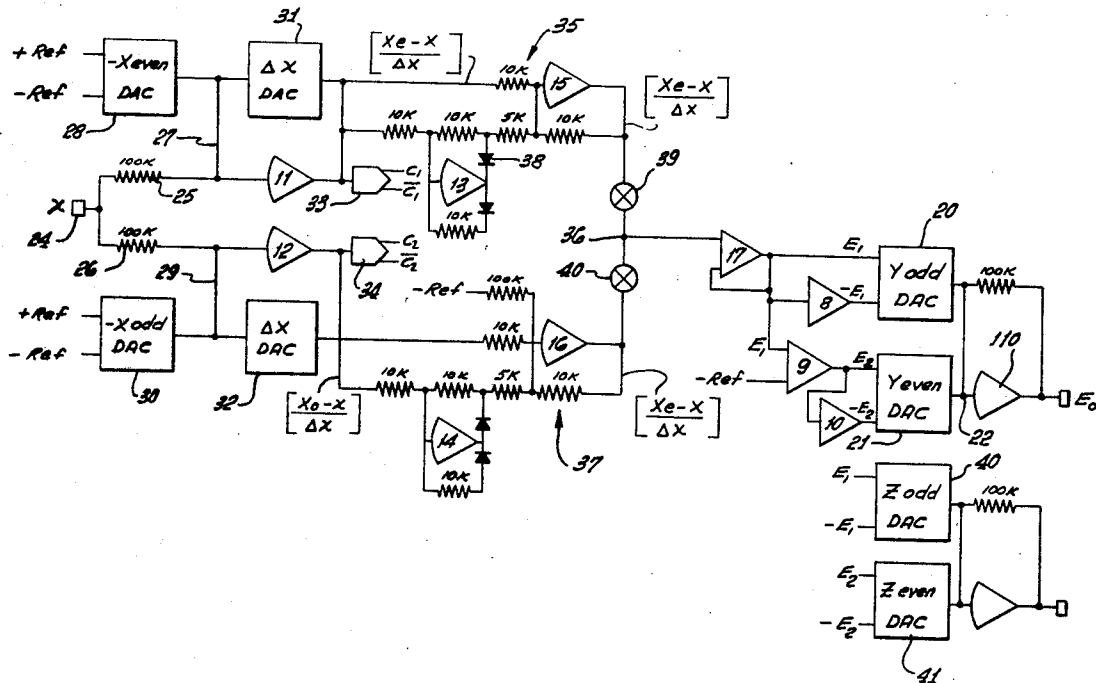
[54] **INTERPOLATIVE FUNCTION GENERATOR  
HAVING A PAIR OF DIGITAL-TO-ANALOG  
CONVERTERS CONNECTED IN SUMMING  
RELATION**  
8 Claims, 10 Drawing Figs.

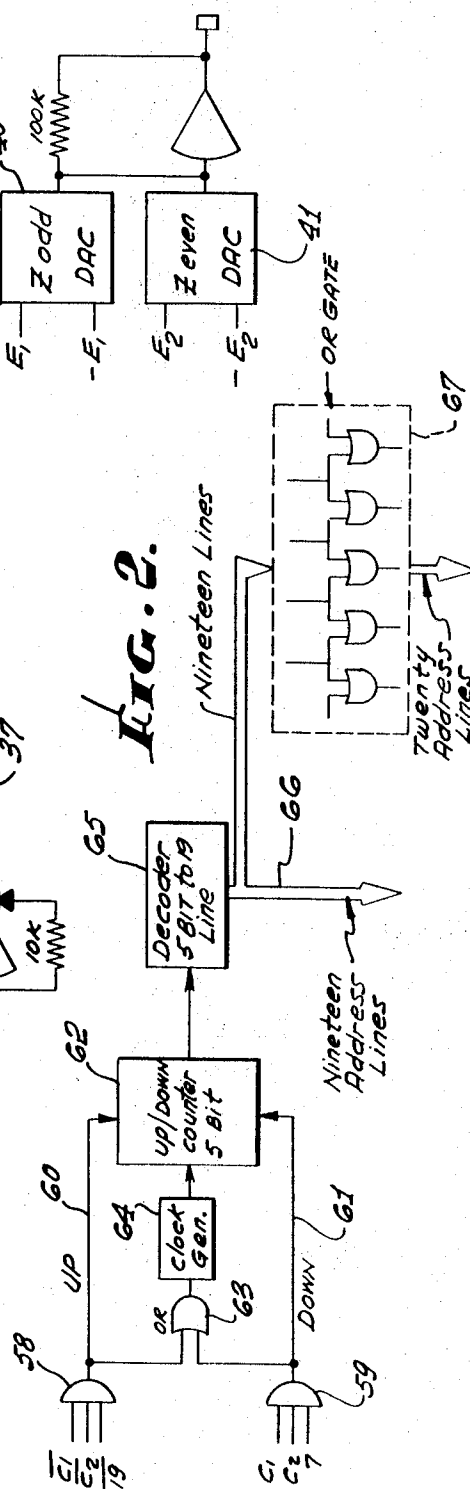
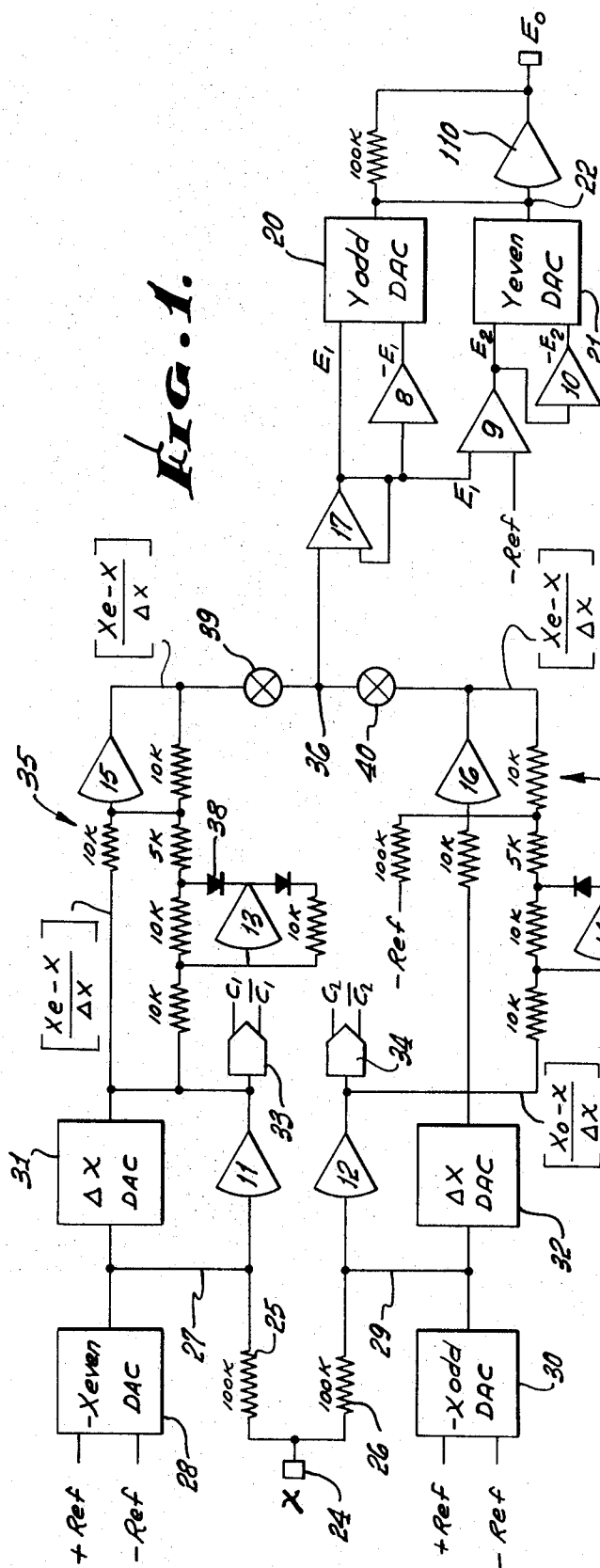
[52] U.S. Cl. .... 235/150.53,  
235/197, 340/347

[51] Int. Cl. .... G06j 7/20,  
G06j 1/00

[50] Field of Search ..... 235/197,  
193, 194, 195, 196, 150.53, 150.52, 150.51,  
150.5; 328/142; 340/347 OA

**ABSTRACT:** The disclosure concerns a function generator as used in an analog computer and employing a pair of digital to analog converters having outputs connected in summing relation; and circuit means connected with the converters to drive the output of one converter back and forth between function and reference values, and further characterized in that the output of one converter increases while the output of the other converter decreases, and vice versa.





INVENTOR.  
**GILBERT R. GRADO**  
 By *White & Hefflinger*  
 ATTORNEYS.

**FIG. 3.**

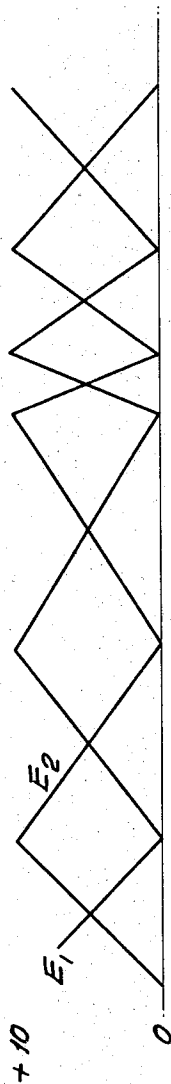
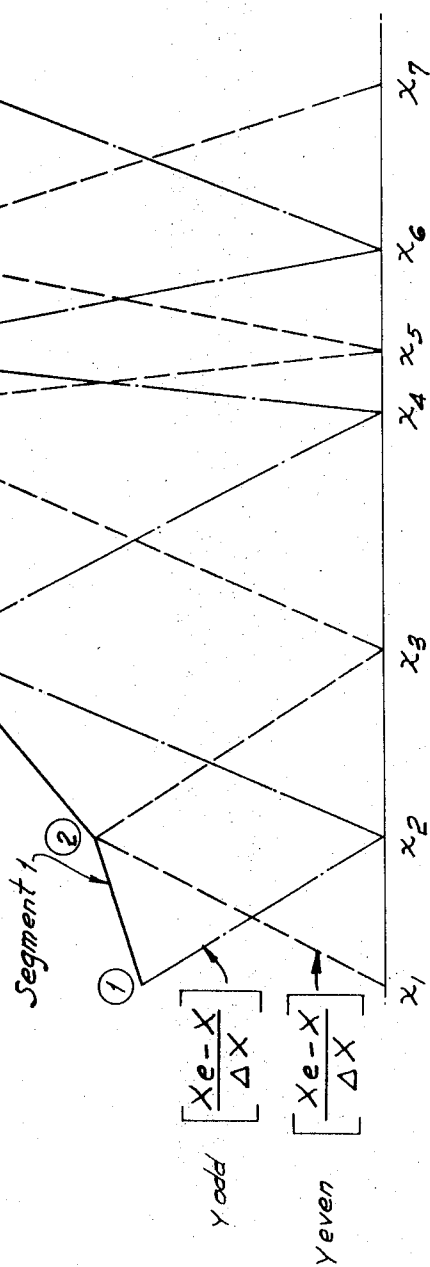


**FIG. 4.**



INVENTOR  
**GILBERT R. GRADO**

By *White & Haefliger*

ATTORNEYS.

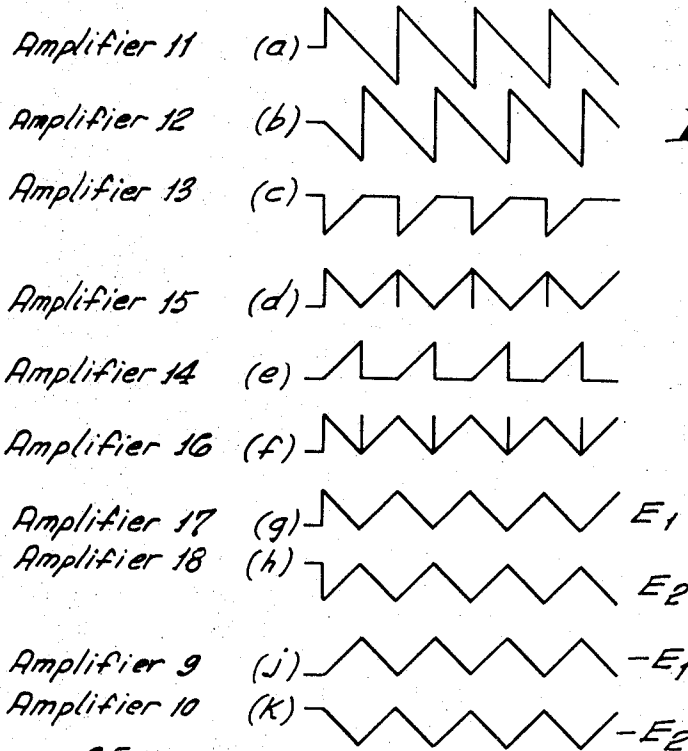


**FIG. 5.**

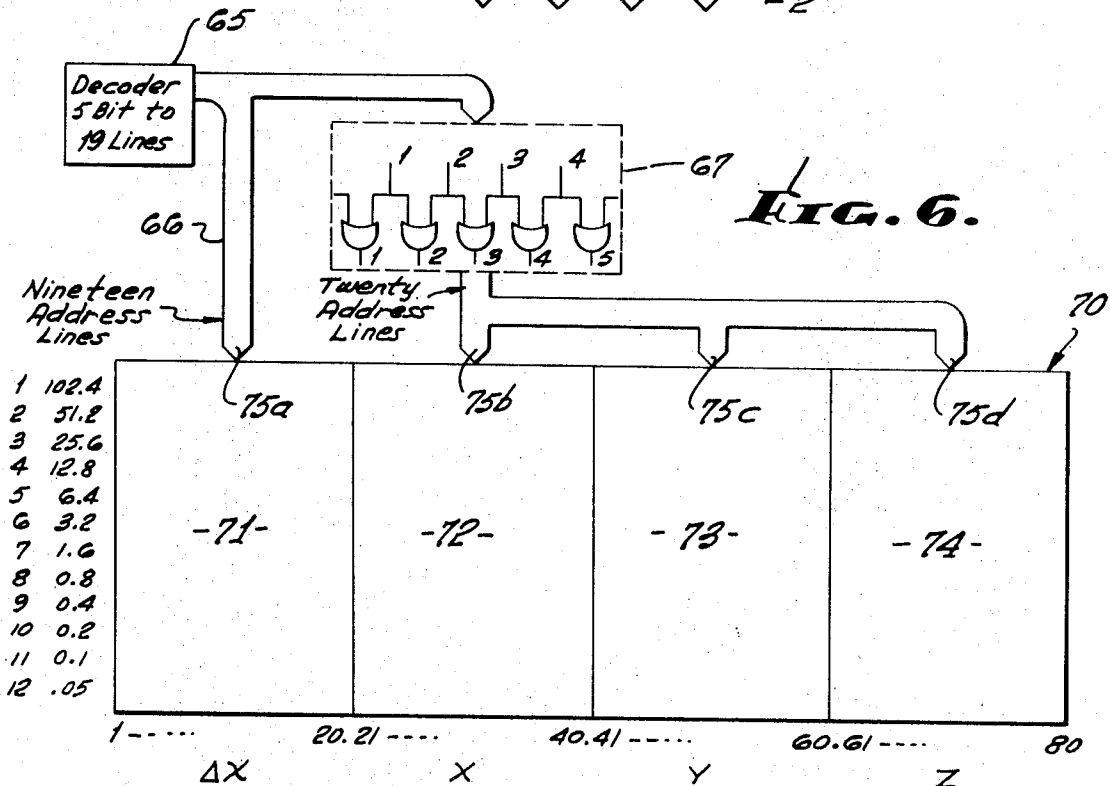


**FIG. 6.**

INVENTOR.  
**GILBERT R. GRADO**  
 By *White & Hefflinger*  
 ATTORNEYS.

**Fig. 8.**

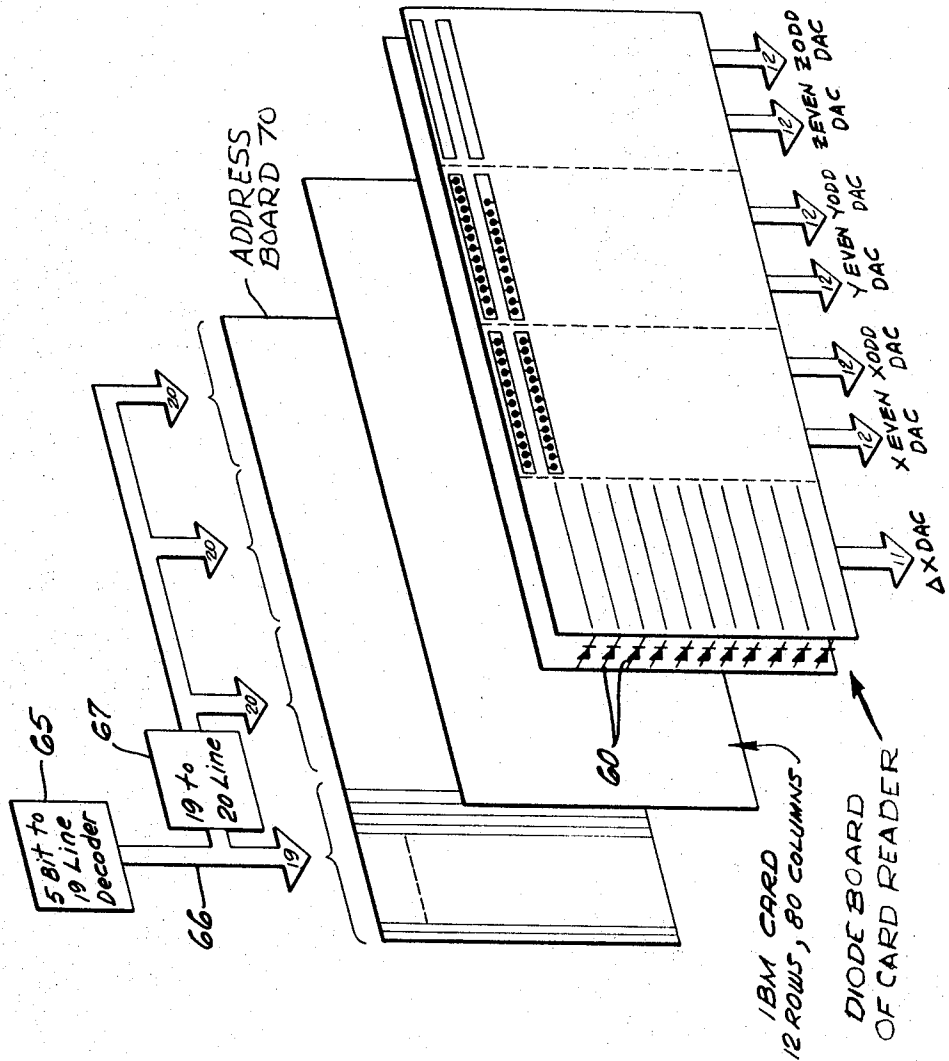


**FIG. 9.**

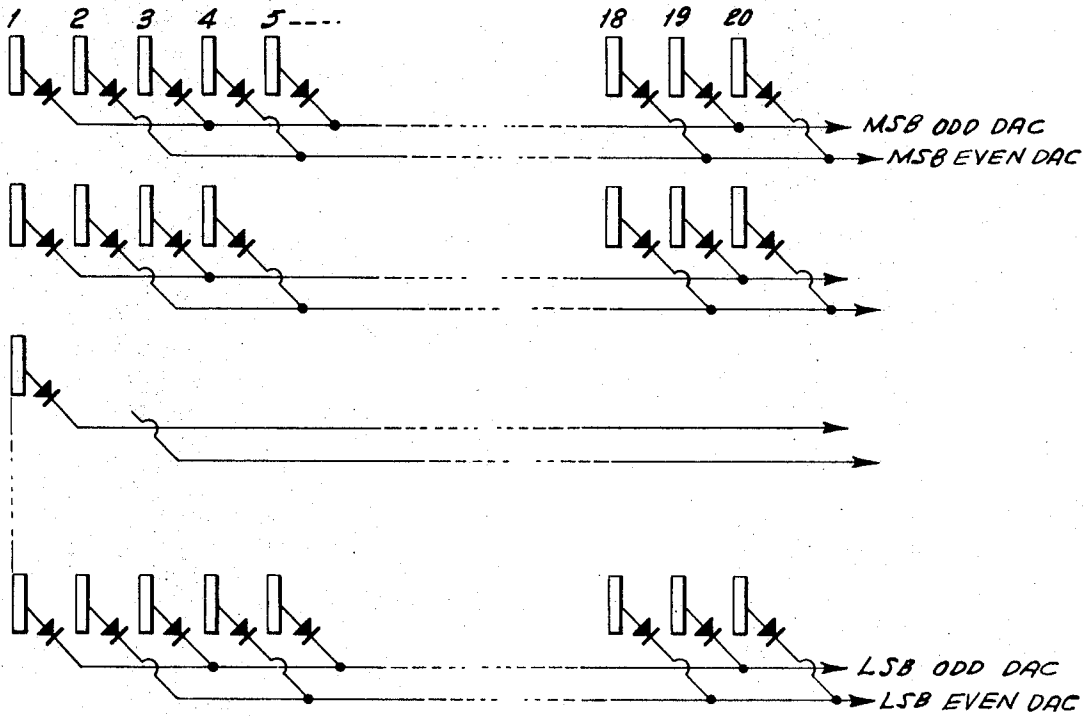
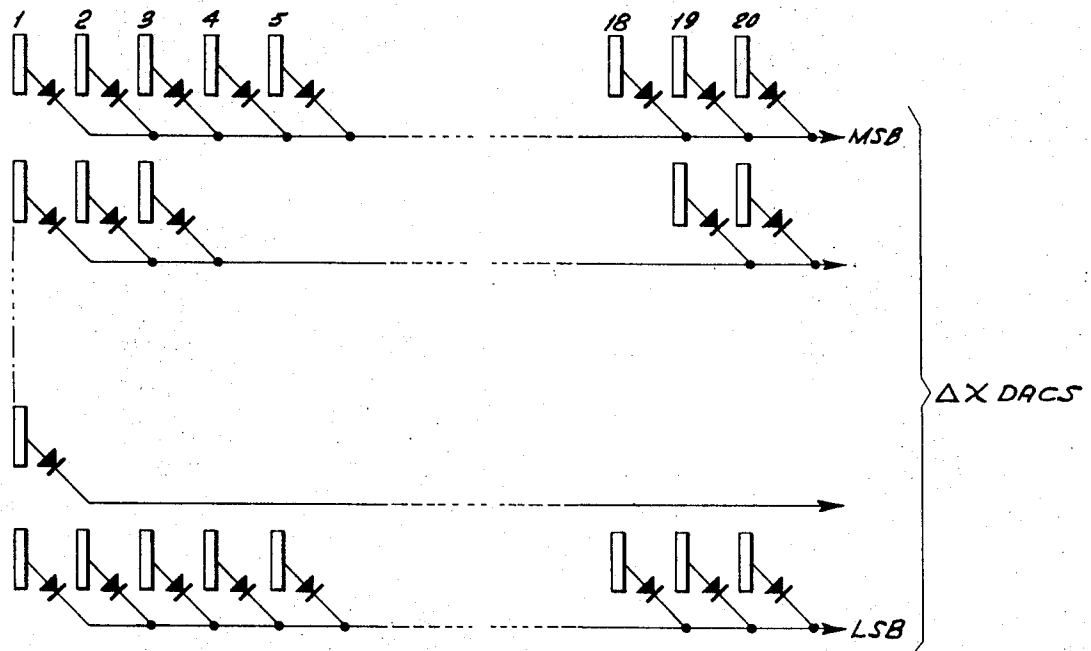


**FIG. 10.**



INVENTOR.  
**GILBERT R. GRADO**  
 By *White & Haefliger*  
 ATTORNEYS.

# INTERPOLATIVE FUNCTION GENERATOR HAVING A PAIR OF DIGITAL-TO-ANALOG CONVERTERS CONNECTED IN SUMMING RELATION

## BACKGROUND OF THE INVENTION

This invention relates generally to analog computers, and more specifically to function generators in such equipment.

Function generators are used in analog computers to generate an output voltage related to an input voltage by some arbitrary set of values not easily defined mathematically. For example, in the simulation of missile and airplane systems, there are aerodynamic functions determined by wind tunnel tests, and it is necessary to simulate these relationships in an analog computer. The data determined by the wind tunnel tests involve relationships such as coefficients of lift and drag as a function of angle of attack, Mach number (velocity), and air density. It is the purpose of the function generator to accept an analog input representative of one of the problem variables, and to generate an output voltage representative of the related problem parameter.

Present day analog computers use diode function generators for arbitrary function generation. In this technique diode resistance networks are used to change slopes at selected breakpoints to duplicate the desired function, potentiometers being employed to store the breakpoint and slope data of each segment. One disadvantage of this technique is that each succeeding segment is cumulative (added on to the previous segments) and set up requires a sequence of adjustments. The use of diodes to effect a breakpoint causes undesirable accuracy limitations due to temperature drift. Recent developments have seen the use of digital-to-analog converters (DAC's) instead of potentiometers, the set up time being greatly reduced since it is possible to store the breakpoint and slope data in either a punched card or in a computer memory; however, the disadvantages of diode function generators remain.

A different approach using fixed locations for the input data points but having a noncumulative technique for the various segments is described in U.S. Pat. No. 3,217,151 entitled "Nonlinear Element for an Analog Computer" by David R. Miller and Roger H. Rathburn. This device uses potentiometers for the storage of the data values. The logic selects two data points depending on the input variable, and then linear interpolation is performed between the two data values by a time division scheme. The disadvantages of this technique are that the breakpoints are fixed, and the frequency response is limited by the interpolation scheme employing the time division principle.

## SUMMARY OF THE INVENTION

It is a major object of the present invention to provide a function generator capable of overcoming the above referred to disadvantages, and further characterized by one or more of the following advantages: function generation is accomplished using only a series of data value pairs describing a particular function; there is no restriction on the spacing of breakpoints; accuracy and frequency response are considerably improved as compared with diode function generators; setup time is greatly simplified because the output is always a function of two stored values and other points have no contribution to the output; and it becomes possible to change the value of one point without affecting the rest of the function.

Basically, the generator broadly comprises a pair of digital to analog converters having outputs connected in the summing relation; and circuit means connected with the converters to drive the output of one converter back and forth between reference and function values and simultaneously to drive the output of the other converter back and forth between function and reference values, and further characterized in that the output of one converter increases while the output of the other converter decreases and vice versa. Typically, each converter includes parallel branches in each of which switchable resistance is connected, the circuit means in-

cluding a source to supply a first sawtooth input to the branches of the converter and a second sawtooth input to the branches of the other converter, the sawtooth inputs being opposite in phase, and digital means to controllably switch resistance in the branches of one converter when the sawtooth input to the branches of the other converter is approximately peaking, and to controllably switch resistance in the branches of the other converter when the sawtooth input to the branches of the one converter is approximately peaking.

These and other objects and advantages of the invention, as well as the details of an illustrative embodiment, will be more fully understood from the following detailed description of the drawings, in which:

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of analog circuitry incorporating the invention;

FIG. 2 is a block diagram showing a method of stored data selection corresponding to a line segment of the function to be generated, the data to be fed to the digital to analog converters;

FIG. 3 is a graph of sawtooth input voltages to the converters;

FIG. 4 is a graph of a typical function to be generated;

FIG. 5 is waveform diagram;

FIG. 6 is a block diagram showing a method of storage in a punched card of data to be used in operating various digital to analog converters usable in the circuitry of the invention;

FIG. 7 is a wiring diagram of a typical digital to analog converter usable in the circuitry of the invention;

FIG. 8 is a perspective exploded schematic view of data storage and reading apparatus;

FIG. 9 is a diagram showing an isolation diode array for  $X_{even}$ ,  $X_{odd}$ , or  $Y_{even}$ ,  $Y_{odd}$ , or  $Z_{even}$ ,  $Z_{odd}$  DAC's; and

FIG. 10 is a diagram showing an isolation diode array for  $\Delta X$  DAC's.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a pair of digital to analog converters are shown at 20 and 21 as having outputs which are connected at summing point 22, in turn connected to the input of amplifier 110 whose output is  $E_o$ . In accordance with the invention, circuit means is connected with inputs to the converters to drive the output of one converter back and forth between reference and function values, and simultaneously to drive the output of the other converter back and forth between function and reference values. Also, the output of one converter increases while the output of the other decreases.

The relationships are made clear by reference to FIGS. 3 and 4. In the latter, data points are seen at (1)–(7) on a function to be generated, and are connected by line segments which approximate the true value of the function between such points. The output of the  $Y_{odd}$  converter 20 drops from function value (1) at  $x_1$  to reference (say, zero) value at  $x_2$ , while the output of the  $Y_{even}$  converter 21 increases from reference value at  $x_1$  to function value (2) at  $x_2$ . Next, the output of converter 20 increases from reference value at  $x_2$  to function value (3) at  $x_3$ , while the output of converter 21 decreases from function value (2) to reference value at  $x_3$ , and so on. The curve thus generated has the value  $E_o$  which varies with time and which closely approximates the true function.

An equation representing  $E_o$  is as follows:

$$E_o = Y_{odd}E_1 + Y_{even}E_2 \quad (1)$$

where,

$E_1$  = an increasing and decreasing voltage, (as for example is seen in FIG. 3) which drives converter 20,

$E_2$  = a decreasing and increasing voltage (as for example is seen in FIG. 3), which drives converter 21,

$Y_{odd}$  = the digital "function weighting" input to converter 20 which is periodically updated (as for example at  $x_2, x_4$ )

$Y_{even}$  = the digital "function weighting" input to converter 21, which is periodically updated (as for example at  $x_1, x_3, x_5$ )

One example of circuitry to generate the  $E_1$  and  $E_2$  driving voltages, in such manner as to contribute unusual advantages, is shown in FIG. 1 at the left of the converters 20 and 21. Two identical input amplifiers 11 and 12 are provided, with inputs connected to a source 24 of input voltage  $X$ , as via identical resistors 25 and 26. Also connected at 27 to input to amplifier 11 is a digital to analog converter 28 having reference inputs as shown and whose output is an  $X_{\text{even}}$  stored value  $X_e$ ; likewise, connected at 29 to input to amplifier 12 is a digital to analog converter 30 having reference inputs as shown, and whose output is an  $X_{\text{odd}}$  stored value  $X_o$ . Connected in feedback relation with the amplifiers 11 and 12 are the respective  $\Delta X$  digital to analog converters 31 and 32 operating to scale the maximum outputs of the amplifiers (say for example 10 volts). Accordingly, the output of amplifier 11 is represented by the expression  $(X_e - x)/\Delta X$ , where  $\Delta X$  is the absolute value of the difference between  $X_e$  and  $X_o$ , and the output of amplifier 12 is represented by the expression  $(X_o - X)/\Delta X$ . In normal operating mode, the input voltage variable  $X$  should be between the two stored values  $X_e$  and  $X_o$ . Comparators 33 and 34 connected with the outputs of the respective amplifiers indicate the polarity of the amplifier outputs. In this regard,

$$C_1 \text{ is true if } X_e > X \quad (2)$$

$$C_2 \text{ is true if } X_o > X \quad (3)$$

A circuit leg 35 connects the output of amplifier 11 with a summing point 36, and a circuit leg 37 connects the output of amplifier 12 with summing point 36. Leg 35 includes two amplifiers 13 and 15 with associated resistors and diodes, connected as shown, and serving to generate the absolute value of the amplifier 11 output, i.e.  $|X_e - X/\Delta X|$ , FIG. 5(d) showing this absolute value. For negative voltages at amplifier 11, the output of amplifier 15 is the inverted input because amplifier 13 does not contribute any input to amplifier 15; for positive voltages at amplifier 11, amplifier 13 has the inverted signal at the anode of diode 38, and this signal is fed to amplifier 15 with a gain of two to give a net input of a negative signal. The output of amplifier 15 is of course positive.

Similarly, FIGS. 5(b), 5(e) and 5(f) illustrate the outputs of amplifiers 12, 14 and 16 in branch 37. The inputs to amplifier 16 are:

$$-R + \left| \frac{X_o - X}{\Delta X} \right| \quad (4)$$

and the output of amplifier 16 is the inverse:

$$R - \left| \frac{X_o - X}{\Delta X} \right| \quad (5)$$

The offsetting of the output of amplifier 16 by the term  $R$  is the same as by the term  $(X_e - X_o)/\Delta X$  for a typically scaled system. Accordingly the output of amplifier 16 is

$$\left| \frac{X_e - X_o}{\Delta X} \right| - \left| \frac{X_o - X}{\Delta X} \right| = \left| \frac{X_e - X}{\Delta X} \right| \quad (6)$$

As illustrated in FIGS. 5(d) and 5(f) the outputs of amplifiers 15 and 16 in the two branches are identical except that waveform 5(d) has switching transients at the point of amplifier 11 switching (see FIG. 5(a)) and waveform 5(f) has switching transients caused by switching of amplifier 12 (see FIG. 5(b)). A smooth (switching transient free) output of amplifier 17 is obtained by providing switching means to maintain the output of amplifier 15 connected to the input to amplifier 17 while amplifier 16 is undergoing a switch transient, and to maintain the output of amplifier 16 connected to the input of amplifier 17 while amplifier 15 is undergoing a switching transient. As an example, switch 39 between amplifier 15 and summing point 36 is closed whenever the output of amplifier 15 is between 0 and  $0.6 |X_e - X/\Delta X|$ , and otherwise is open; and switch 40 between amplifier 16 and point 36 is closed whenever the output of amplifier 16 is between  $0.4 |X_e - X/\Delta X|$  and  $1.0 |X_e - X/\Delta X|$ , and otherwise open. There is some overlap in the input to the switches 39 and 40 to prevent transients arising from their operators.

Amplifier 17 is connected as a unity-gain noninverter, commonly called a potentiometric amplifier having the following characteristics: high input impedance, low output impedance and unity gain. Another amplifier 18 is connected between the output of amplifier 17 and the converter 20, and the outputs of both amplifiers 17 and 18 are used to supply voltages  $E_1$  and  $E_2$  to the converter. Amplifiers 19 and 20 are used to generate voltages  $E_2$  and  $-E_2$  driving the converter 21. Amplifier 19 receives inputs  $E_1$  and  $-Ref$ . From FIG. 3,  $E_1 + E_2 = Ref$ , so that amplifier 19 generates  $E_2 = Ref - E_1$ .

Regarding equation (1) above, it can be rewritten as:

$$E_o = Y_{\text{odd}} \left| \frac{X_o - X}{\Delta X} \right| + Y_{\text{even}} \left| \frac{X_e - X}{\Delta X} \right| \quad (7)$$

It will be observed from this equation that if  $X = E_e$ ,  $E_o = Y_{\text{even}}$  because  $X_o - X_e = \Delta X$ . Also, if  $X = X_o$ ,  $E_o = Y_{\text{odd}}$ . The  $E_1$ ,  $-E_1$ ,  $E_2$ , and  $-E_2$  values referred to above may also be used as driving input voltages to other digital to analog converters 40 and 41, as seen in FIG. 1, having digital "weighting inputs" represented by the values  $Z_{\text{odd}}$  and  $Z_{\text{even}}$  associated with another function to be generated.

FIG. 7 illustrates one typical digital to analog converter usable in FIG. 1, as for example the converter 20 or the converter 21. It has  $E$  and  $-E$  input voltage terminals 50 and 51, an output terminal 52, a branch 53 connecting terminals 50 and 52, and a series of parallel branches 54 connecting terminals 51 and 52. Each such branch includes a switch 55 and bit resistance  $R$  connected in series as shown, the resistors having differential weighting as shown. The  $\Delta X$  converters 31 and 32 use only the input 51, because  $\Delta X$  is the absolute value of  $X_e - X_o$ , and no sign bit is required.

FIG. 2 shows the logic outputs of the comparators 33 and 34 connected via gates 58 and 59, and leads 60 and 61 to drive an up/down counter 62. In normal operating mode, the input signal "X" is always located between two "X" stored data values; however, assuming  $X$  increases positively, it will eventually become more positive than both the stored values. At that point, the outputs of both amplifiers 11 and 12 will become negative, and both  $C_1$  and  $C_2$  will be true. Gate 58 in FIG. 2 will become true if the counter is not at the last count and an "UP" command is generated. OR gate 63 will function to operate clock 64 to generate a clock signal to step the counter up one unit.

The binary contents of the counter are decoded at 65 into, typically, nineteen lines represented at 66. The 19 lines are also connected to a series of OR gates at 67, so that a pair of lines is activated for each line from the decoder. Set 66 of 19 lines is used to select data for the  $\Delta X$  converters 31 and 32 corresponding to a line segment selected. The segment count is then used to select two adjacent data points for both the  $X$  and  $Y$  pairs of converters 28, 30, and 20, 21.

FIG. 6 illustrates how the data may be stored in a punched card 70. 19 columns of the card are used to store the  $\Delta X$  values, in zone 71. 20 columns are used to store the  $X_{\text{even}}$  and  $X_{\text{odd}}$  values in zone 72, and twenty columns are used to store the  $Y_{\text{odd}}$  and  $Y_{\text{even}}$  weighting values in zone 73. In addition, zone 74 may be used to store the weighting values  $Z_{\text{even}}$  and  $Z_{\text{odd}}$  of a second function. Referring to zone 72, the odd numbered columns and the horizontal rows on the card are selected to have typically, a binary scale of 0.050 volts up to a full scale value of  $\pm 102.4$  volts: The card reader 75, as represented by address lines 75a, 75b, 75c, 75d in FIG. 6, is wired so that the 19 address lines at 66 "drive" the columns for the  $\Delta X$  converters 31 and 32, and the bits in those converters are activated every time there is a hole punched in the card for that column. For example, as shown in FIG. 8, the second row for columns 1-19 is through isolation diodes 60 to the 51.2 bit (i.e. via activating switch 55 in a branch connected with resistor 512 R in FIG. 7) in the  $\Delta X$  converter. The bits in the other converters are similarly wired to the card. In this regard, and referring to zone 72, the odd numbered columns between 21 and 40 are wired to the  $X_{\text{odd}}$  converter 30, and the even numbered columns are wired to the  $X_{\text{even}}$  converter 31. Similar wiring is effected between zone 73 and

the  $Y_{odd}$  and  $Y_{even}$  converters, and between zone 74 and the  $Z_{odd}$  and  $Z_{even}$  converters. The diodes 60 are used to isolate the data from other columns that are not selected, i.e. ensure that only data from the selected column is used to activate the converters. FIGS. 9 and 10 show arrays of such diodes and connection to most significant bit (MSB) and least significant bit (LSB) lines. The FIG. 8 array is for  $X_{even}$ ,  $X_{odd}$ , or  $Y_{even}$ ,  $Y_{odd}$ , or  $Z_{even}$ ,  $Z_{odd}$  DMS; while FIG. 9 is for the  $\Delta X$  DACs.

It should be noted that as the line segment count increases by 1, two of the 20 address lines in each set 76-78 is selected. For example, consider an increase from line segment 1 (defined by data points (1) and (2)) to line segment 2 (defined by data points (2) and (3)) in FIG. 4. During this segment increase, data column 2 remains selected, and data column 3 is newly selected. In effect, the odd data converters ( $X_{odd}$ ,  $Y_{odd}$ ,  $Z_{odd}$ ) are thereby updated, and at that time their contribution to the output is zero.

In summary, the advantages of the generator are: dependence upon only two points of the function, thereby simplifying set up; no restriction on slopes, since "X" data points can be programmed as close together as desired; improved dynamic performance and accuracy; and noise free output, because one circuit is in use while the other is being updated. Further, control logic is straight forward. Thus, an "UP" command causes the counter to increment by one count, and new data in the X converter will cause one of the comparators to inhibit any further count. If the input is still more positive than the two stored values, the clock will continue to increment the counter until such time as the input is between two stored X values. The "DOWN" command functions in the same manner, since  $C_1$  and  $C_2$  will both be true if the input is more negative than the stored X values. Gate 59 in FIG. 2, contains the first count inhibit term (1) so that the counter cannot count down once the counter has decremented to a count of one.

#### I claim:

1. In a function generator, the combination comprising
  - a. a pair of digital to analog converters having outputs operatively connected in summed relation, and
  - b. circuit means connected with the converters to drive the output of one converter back and forth between reference and function values and simultaneously to drive the output of the other converter back and forth between function and reference values, and further characterized in that the output of one converter increases while the output of the other converter decreases and vice versa,
  - c. each converter including parallel branches in each of which switchable resistance is connected, the circuit means including a source to supply a first sawtooth input to the branches of said one converter and a second sawtooth input to the branches of the other converter, said sawtooth inputs being opposite in phase, and digital

means to controllably switch resistance in said branches of one converter when the sawtooth input to the branches of the other converter is approximately peaking, and to controllably switch resistance in said branches of the other converter when the sawtooth input to the branches of said one converter is approximately peaking.

2. The combination of claim 1 wherein the summed output of the converters is approximately defined by the equation

$$E_o = Y_{odd} \left| \frac{X_e - X}{\Delta X} \right| + Y_{even} \left| \frac{X_o - X}{\Delta X} \right|$$

where,

$|X_e - X/\Delta X|$  corresponds to the first sawtooth input,

$|X_o - X/\Delta X|$  corresponds to the second sawtooth input,

$Y_{odd}$  corresponds to the equivalent resistance of said one converter to which said first sawtooth is applied

$Y_{even}$  corresponds to the equivalent resistance of the other converter to which said second sawtooth is applied.

3. The combination of claim 1 wherein said source includes first and second circuit legs to supply in-phase sawtooth inputs containing out-of-phase switching transients, and said legs being connected to a junction via switches alternately operable to pass sawtooth input from one leg to said junction when the sawtooth inputs from the other leg is disconnected from the junction and is undergoing a switching transient, and to pass sawtooth input from the other leg to said junction when the sawtooth input from said one leg is disconnected from the junction and is undergoing a switching transient.

4. The combination of claim 3 wherein the source includes amplifier and digital to analog converter elements operatively connected to said legs to produce a signal  $X_e - X/\Delta X$  in the first leg and a signal  $X_o - \Delta X/\Delta X$  in the second leg, where

$X_o$  = a stored signal

$X_e$  = a stored signal different from  $X_o$

$X$  = input signal that varies between  $X_o$  and  $X_e$ , and

$\Delta X = X_e - X_o$

5. The combination of claim 2 including means to adjust the value of  $Y_{odd}$  when X reaches  $X_o$  and to adjust the value of  $Y_{even}$  when X reaches  $X_e$ .

6. The combination of claim 5 wherein said last named means includes comparator apparatus to sense excursions of X to the values  $X_o$  and  $X_e$ , a source of stored data values corresponding to function values and means responsive to the comparator output to effect selective active connection of converter resistances in converter biasing relation in correspondence with selected data values.

7. The combination of claim 6 wherein said source of data values includes a punched card.

8. The combination of claim 4 wherein the summed output of the converters is approximately defined by the equation for  $E_o$  of claim 4.