Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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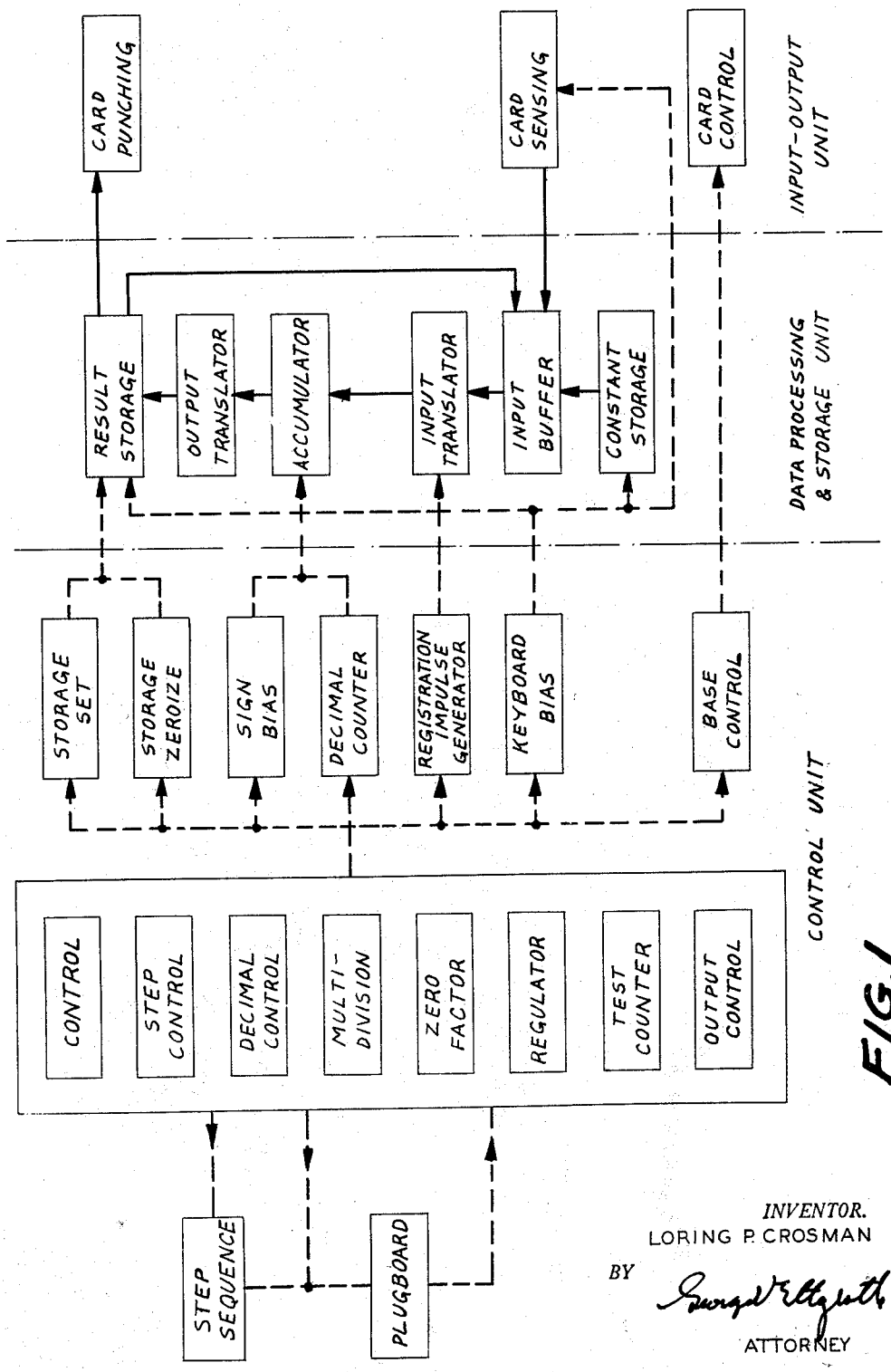


FIG. 1

INVENTOR.
LORING P. CROSMAN
BY George V. Illgath
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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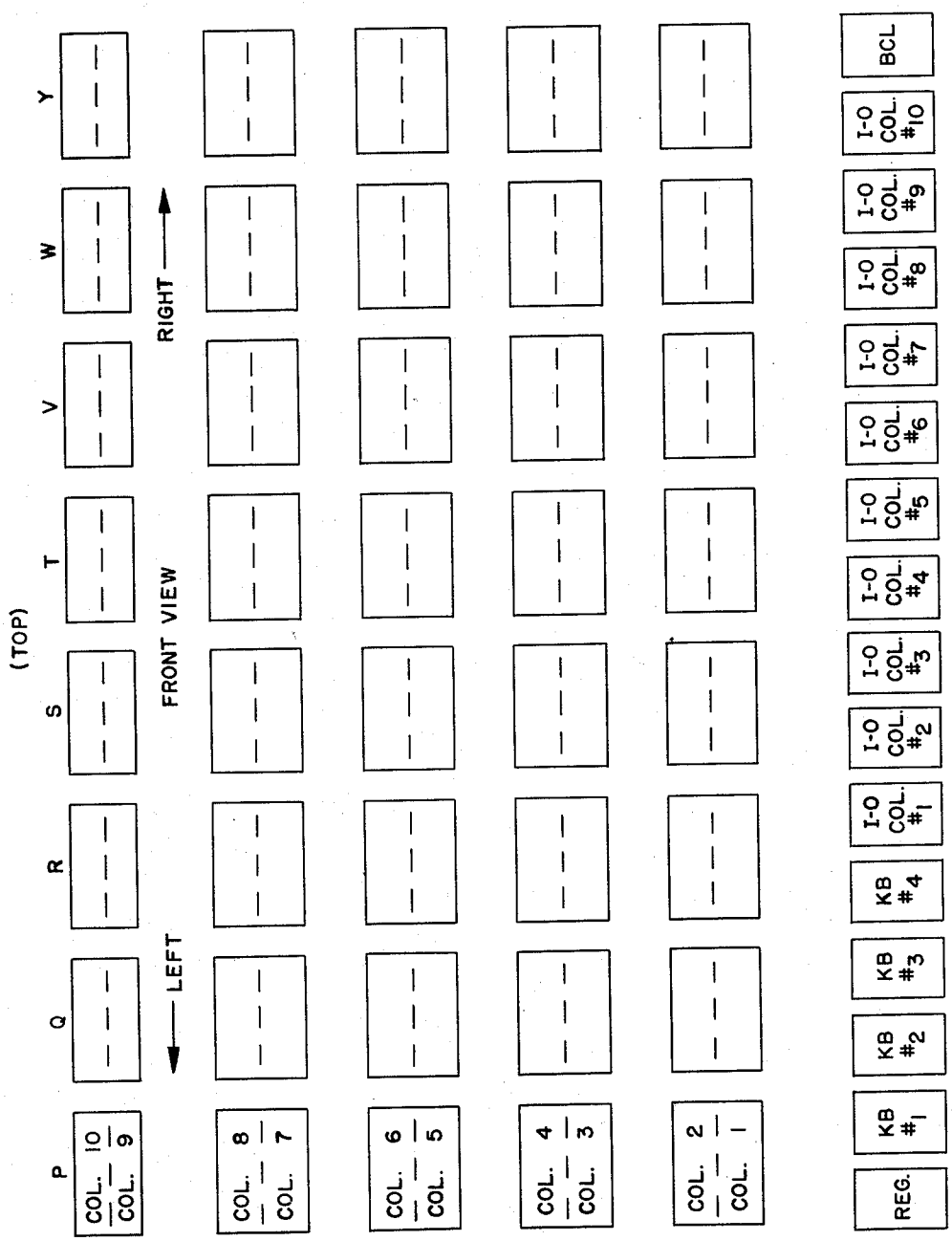


FIG. 2

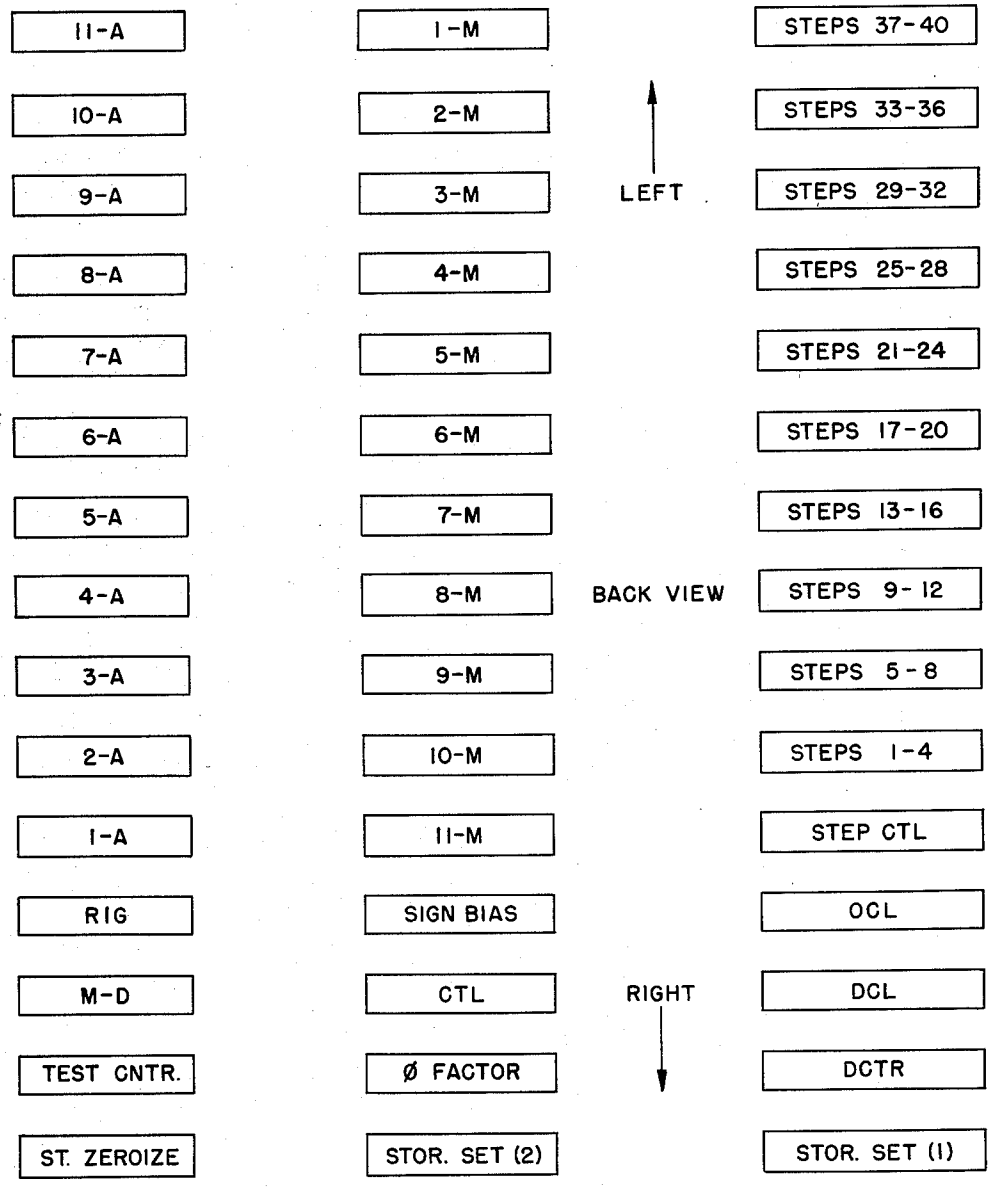
INVENTOR.

LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

FIG. 3



INVENTOR.
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 4

FIG. 4

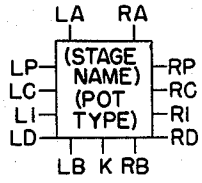


FIG. 5

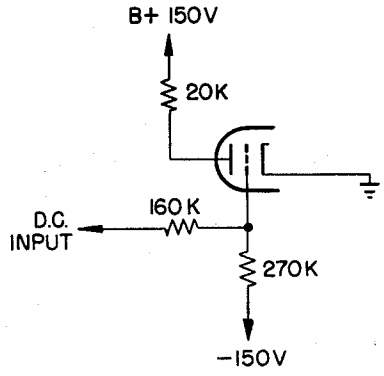


FIG. 6

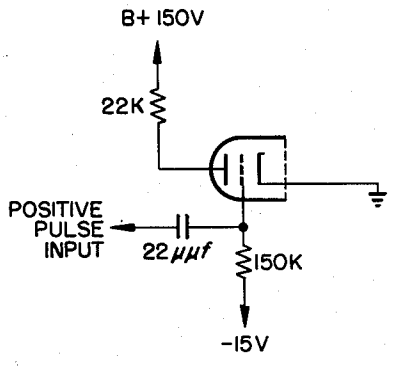


FIG. 7

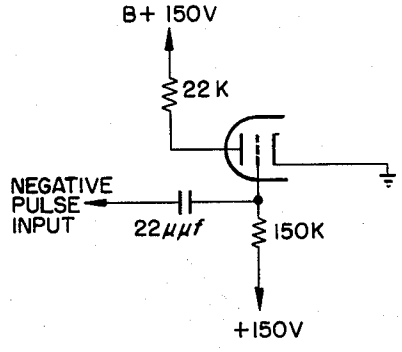


FIG. 8

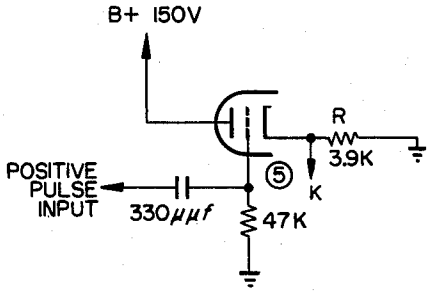
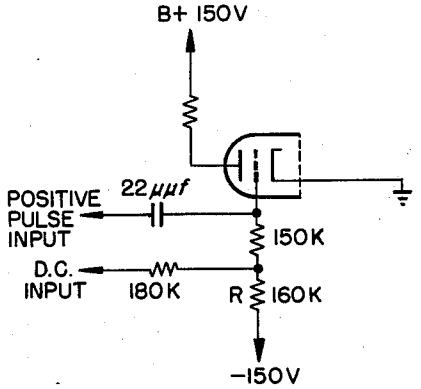


FIG. 9



INVENTOR.

LORING P. CROSMAN

BY George V. Retzroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 5

FIG. 10

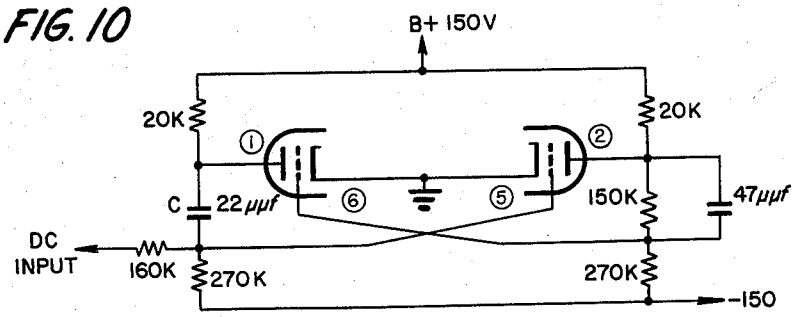


FIG. 11

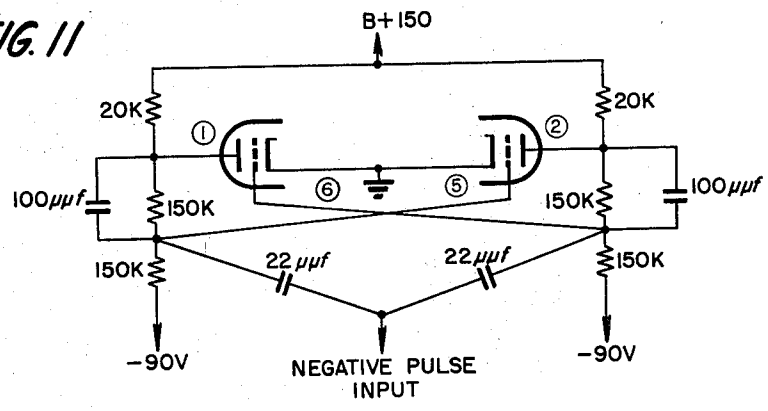
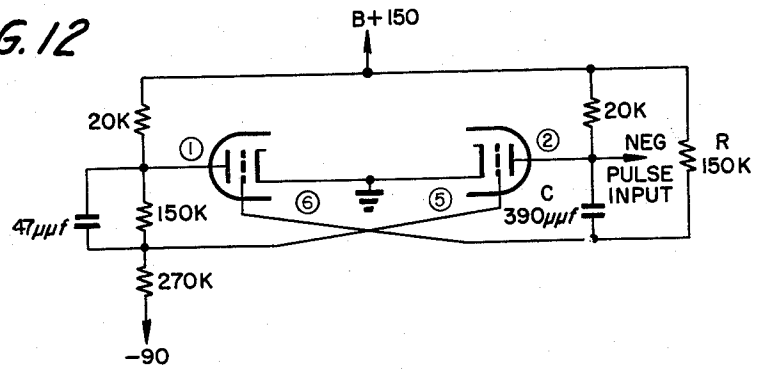


FIG. 12



INVENTOR.

LORING P. CROSMAN

BY George V. Ketzpath

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 6

FIG. 13

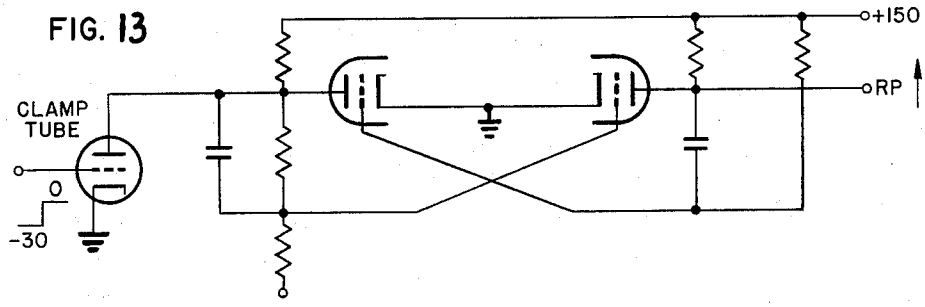


FIG. 14

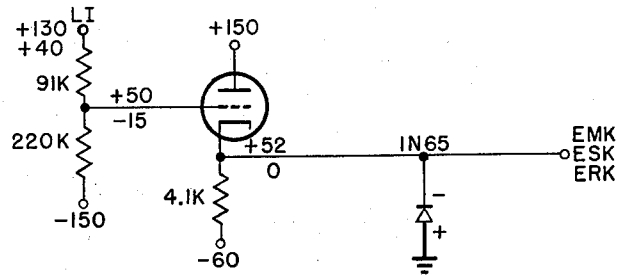
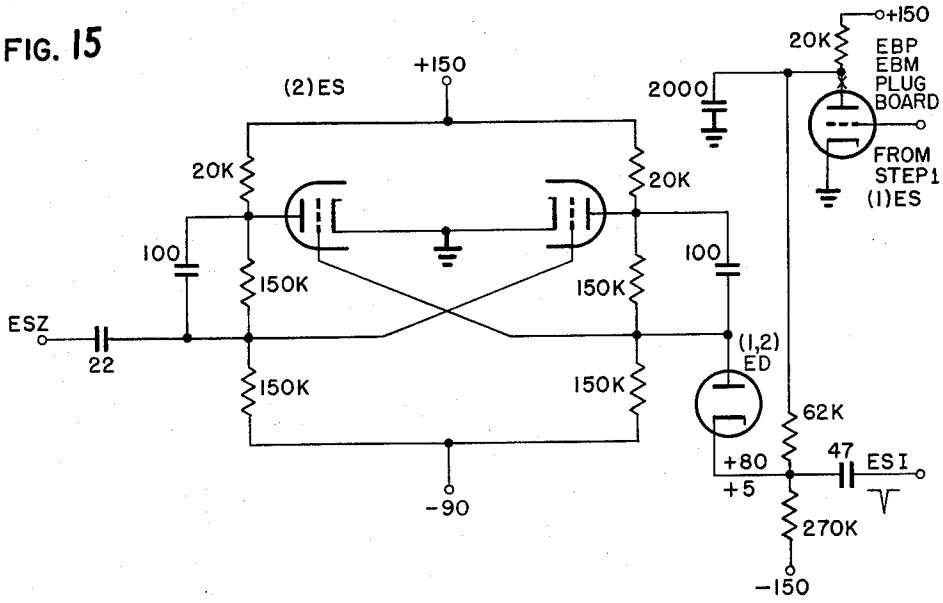


FIG. 15



INVENTOR.
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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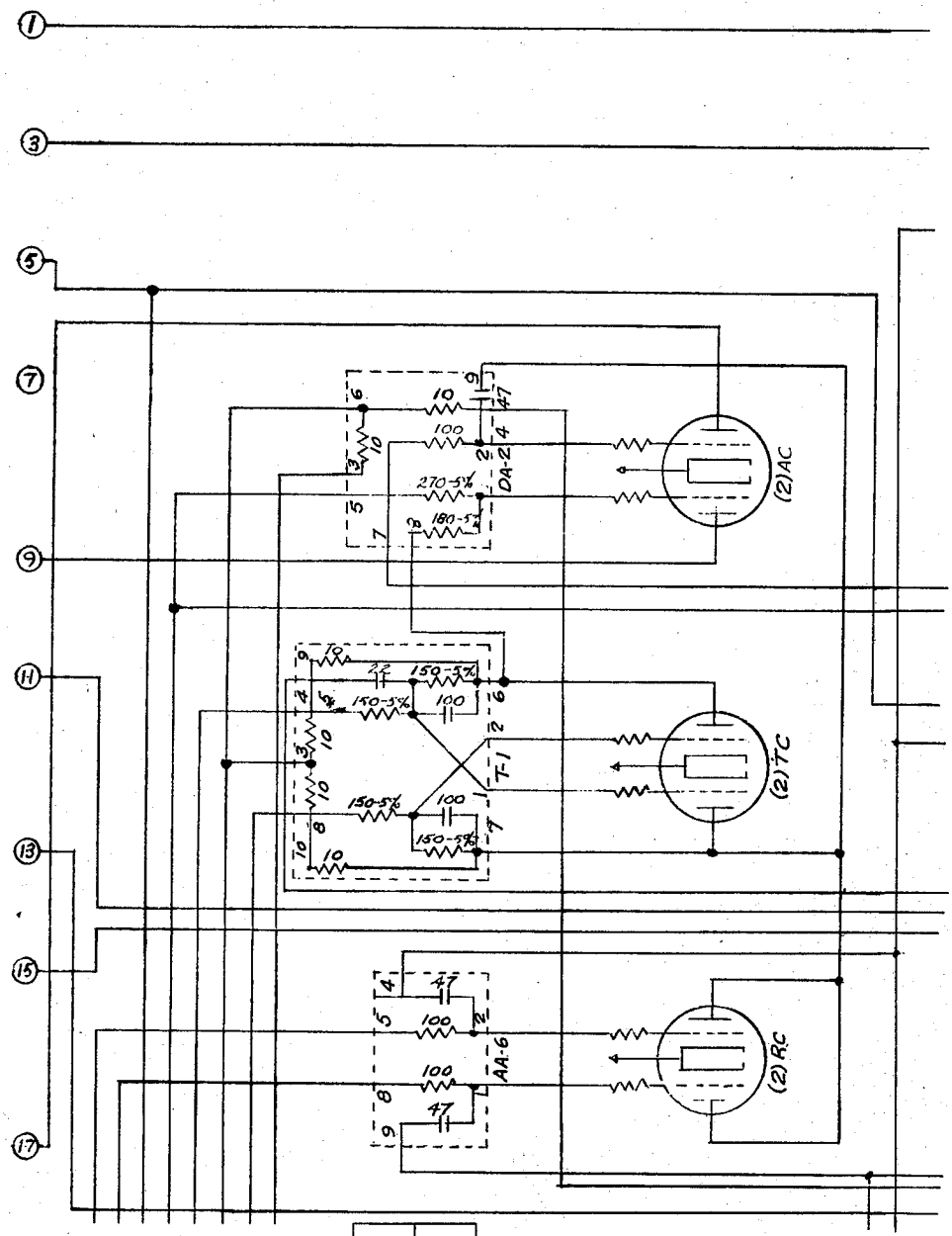


FIG. 16a

FIG. 16a.	FIG 16b.
FIG. 16c	FIG. 16d
FIG. 16e	FIG. 16f

FIG. 16g

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 8

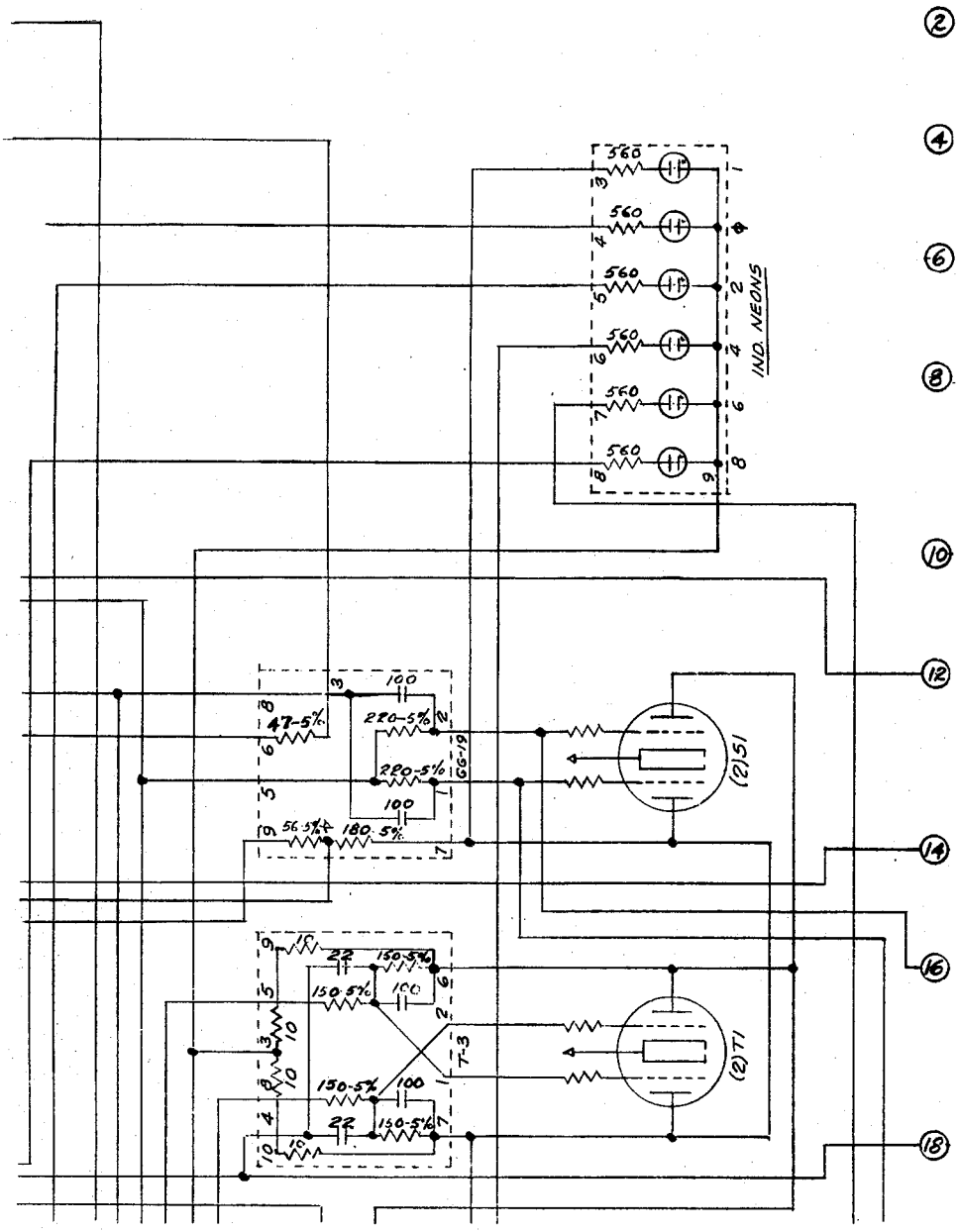


FIG. 16L

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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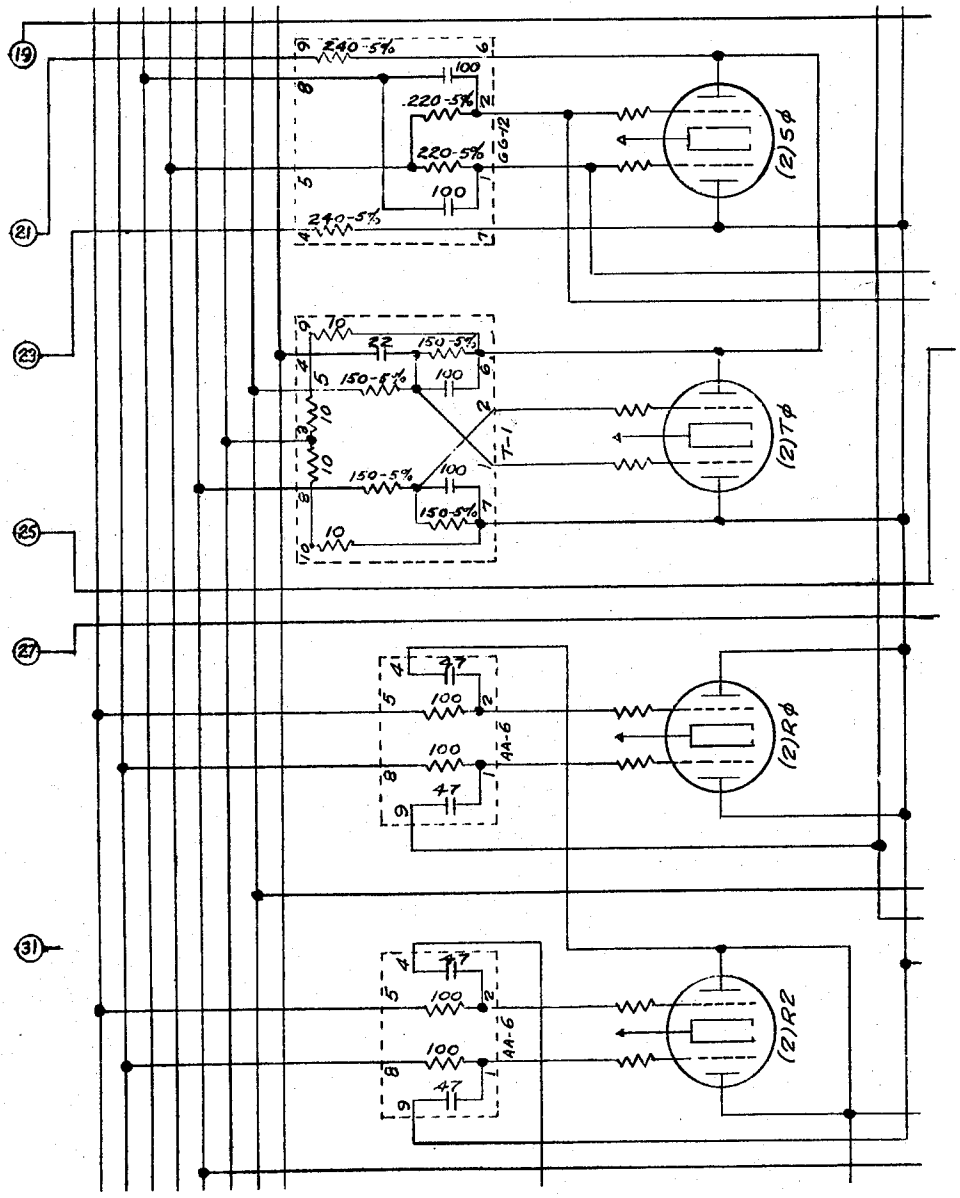


FIG. 16c

INVENTOR
LORING P. CROSMAN
BY George V. Eckroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 10

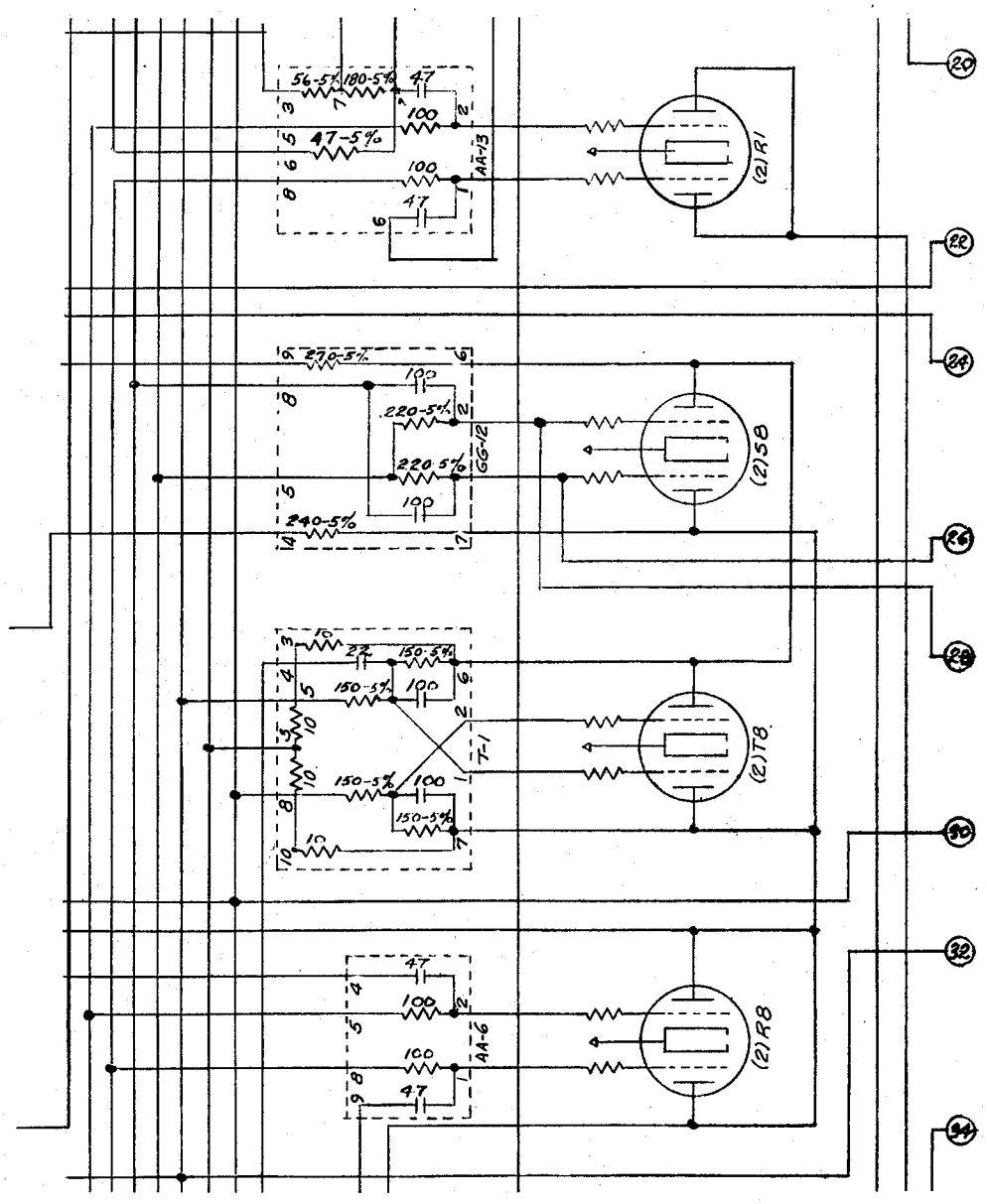


FIG. 16d

INVENTOR
LORING P. CROSMAN
BY George V. Eckroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 11

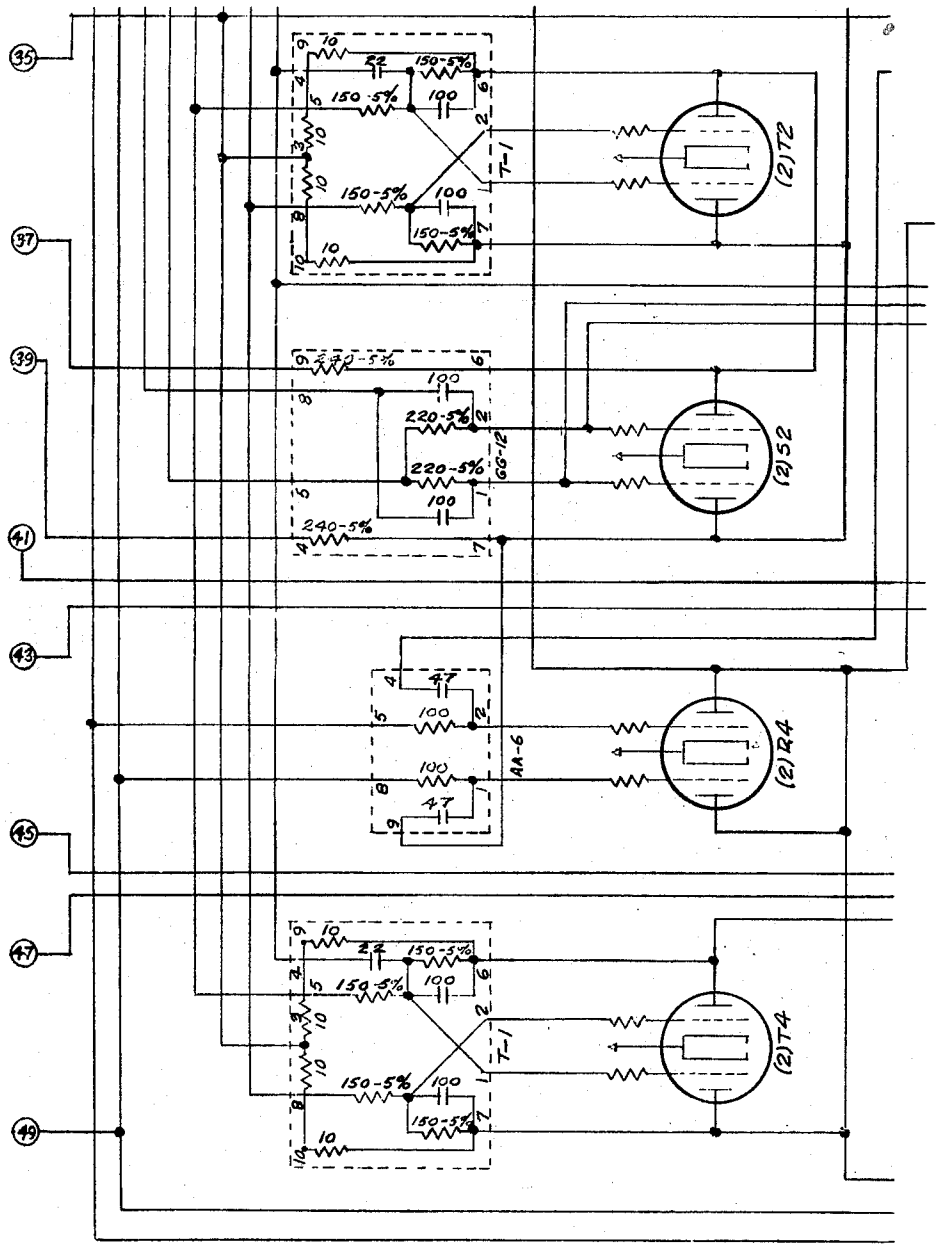


FIG. 16a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 12

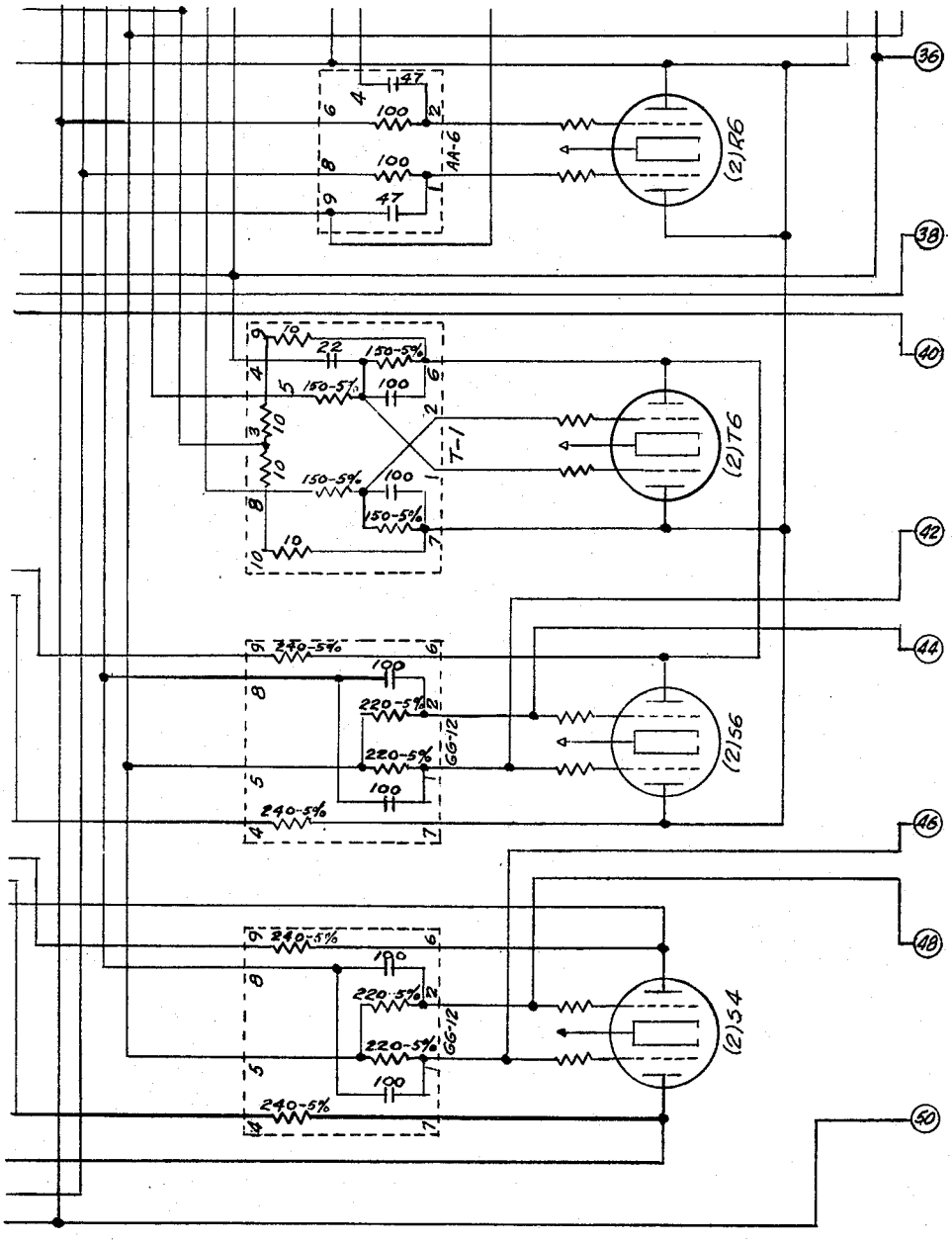


FIG. 16f

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 13

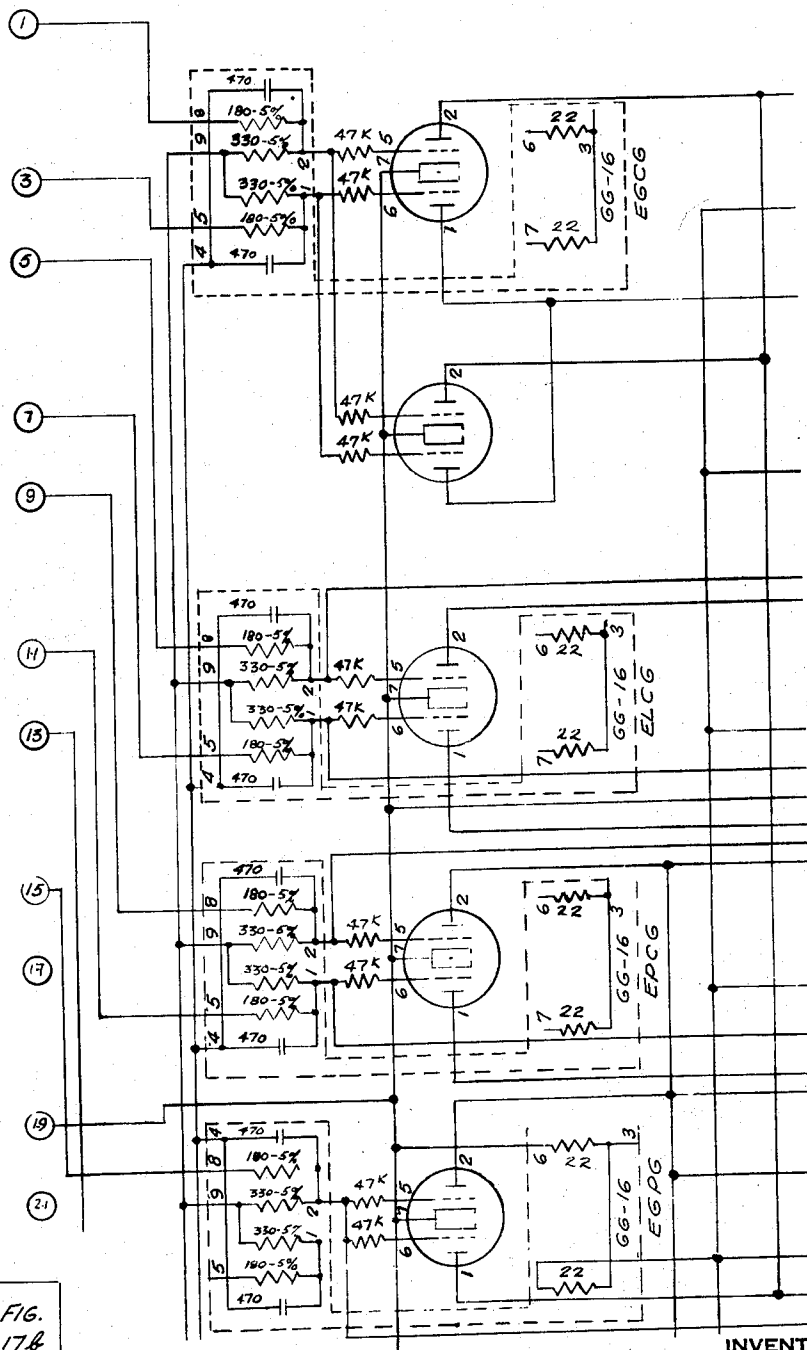


FIG. 17a	FIG. 17b
FIG. 17c	FIG. 17d

FIG. 17a

FIG. 17c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 14

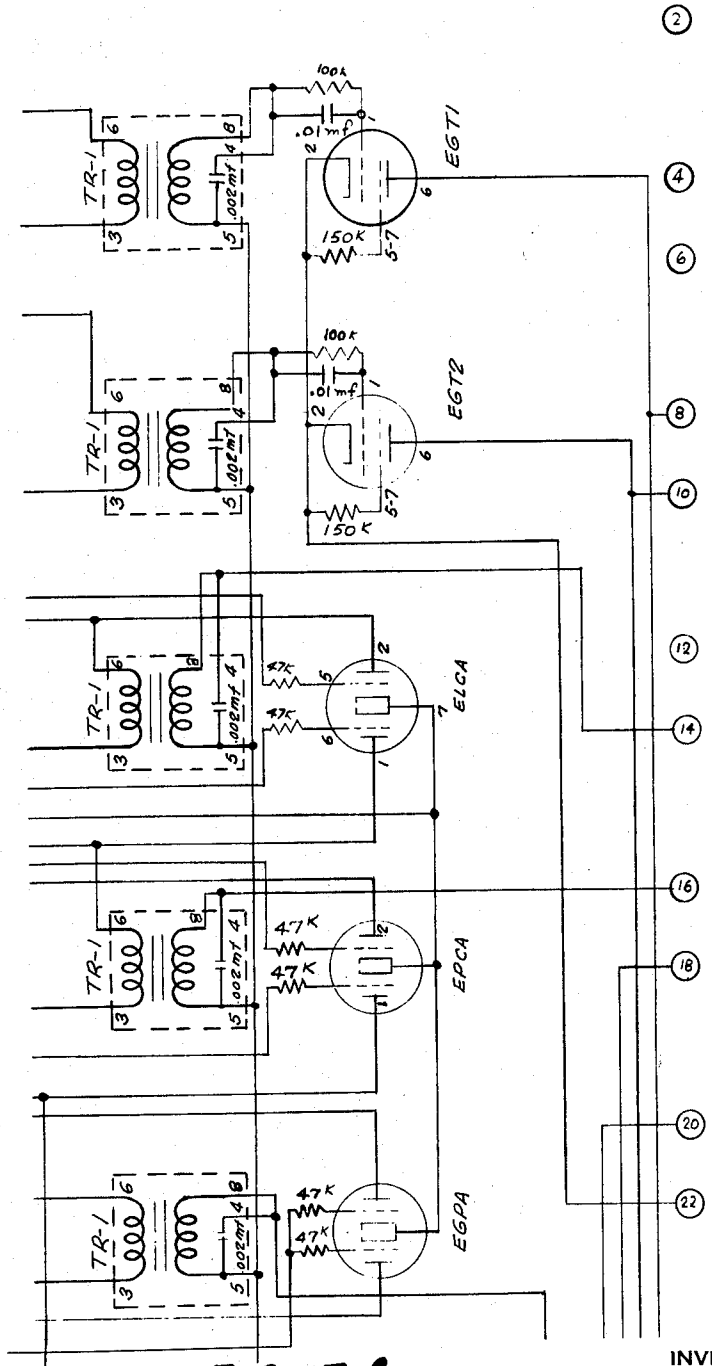


FIG. 17b

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 15

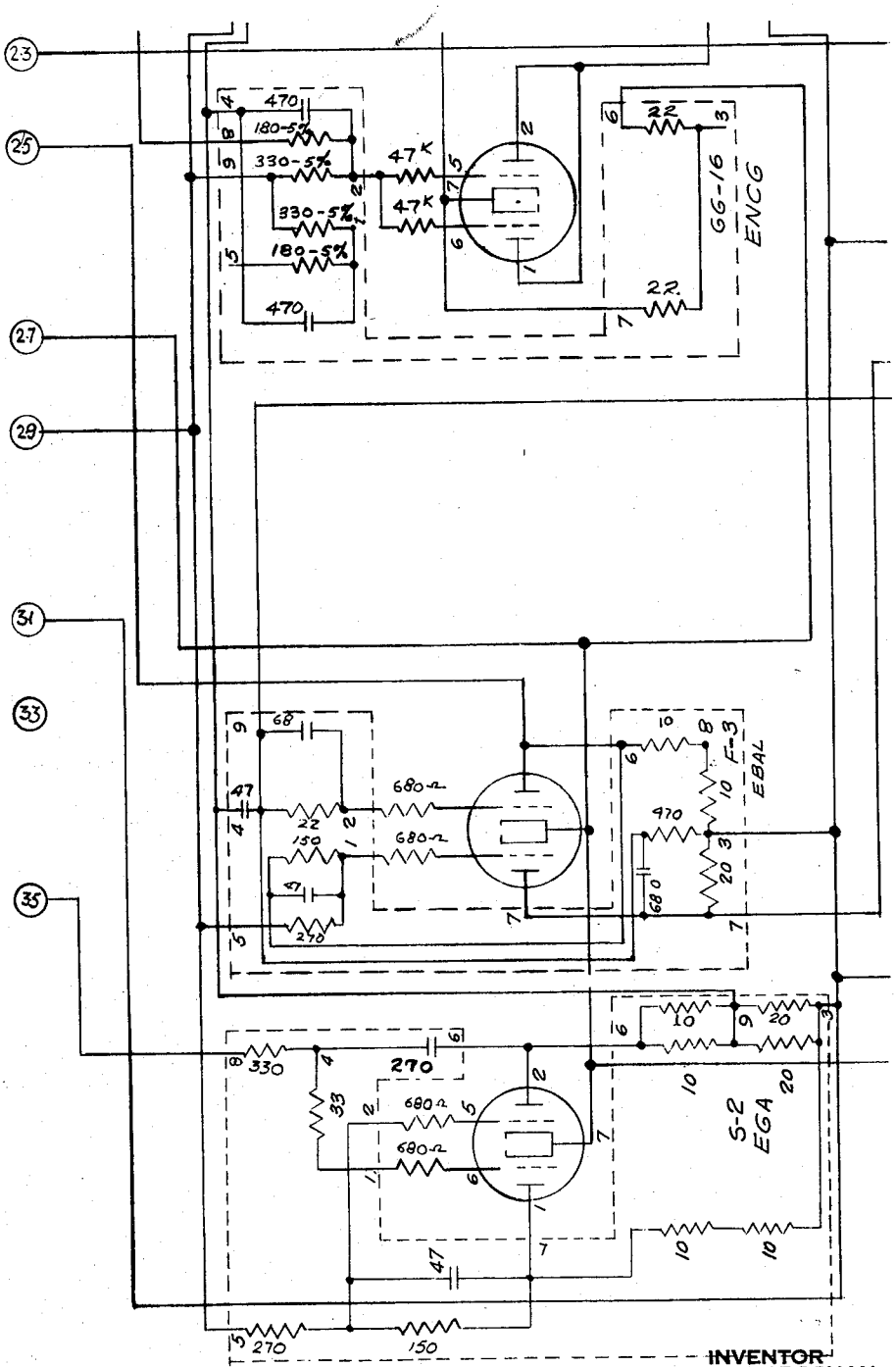


FIG. 17c

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 16

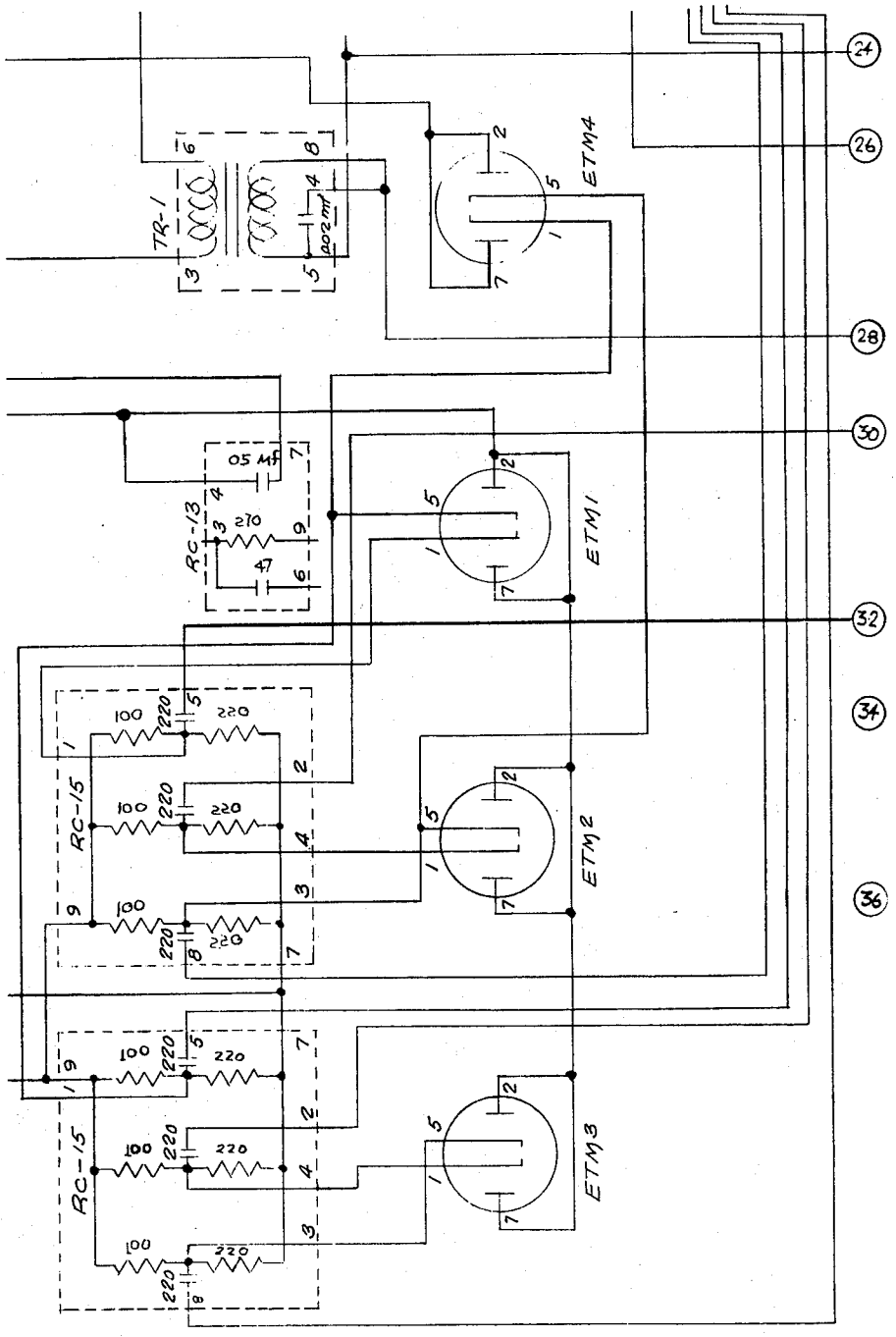


FIG. 17d

INVENTOR
LORING P. CROSMAN
BY George V. Ketzproth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 17

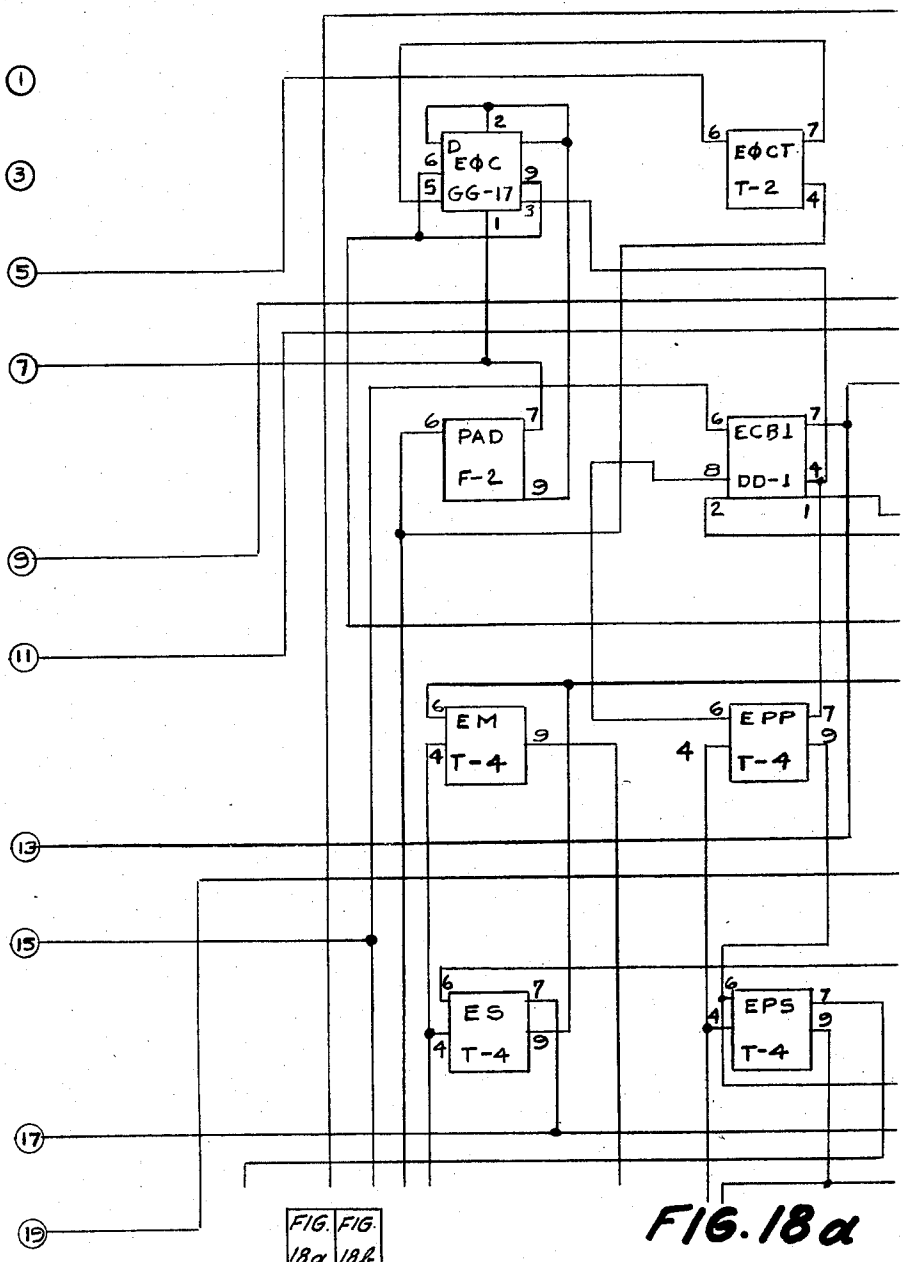


FIG. 18a

FIG. 18a	FIG. 18b
FIG. 18c	FIG. 18d
FIG. 18e	FIG. 18f

FIG. 18g.

INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 18

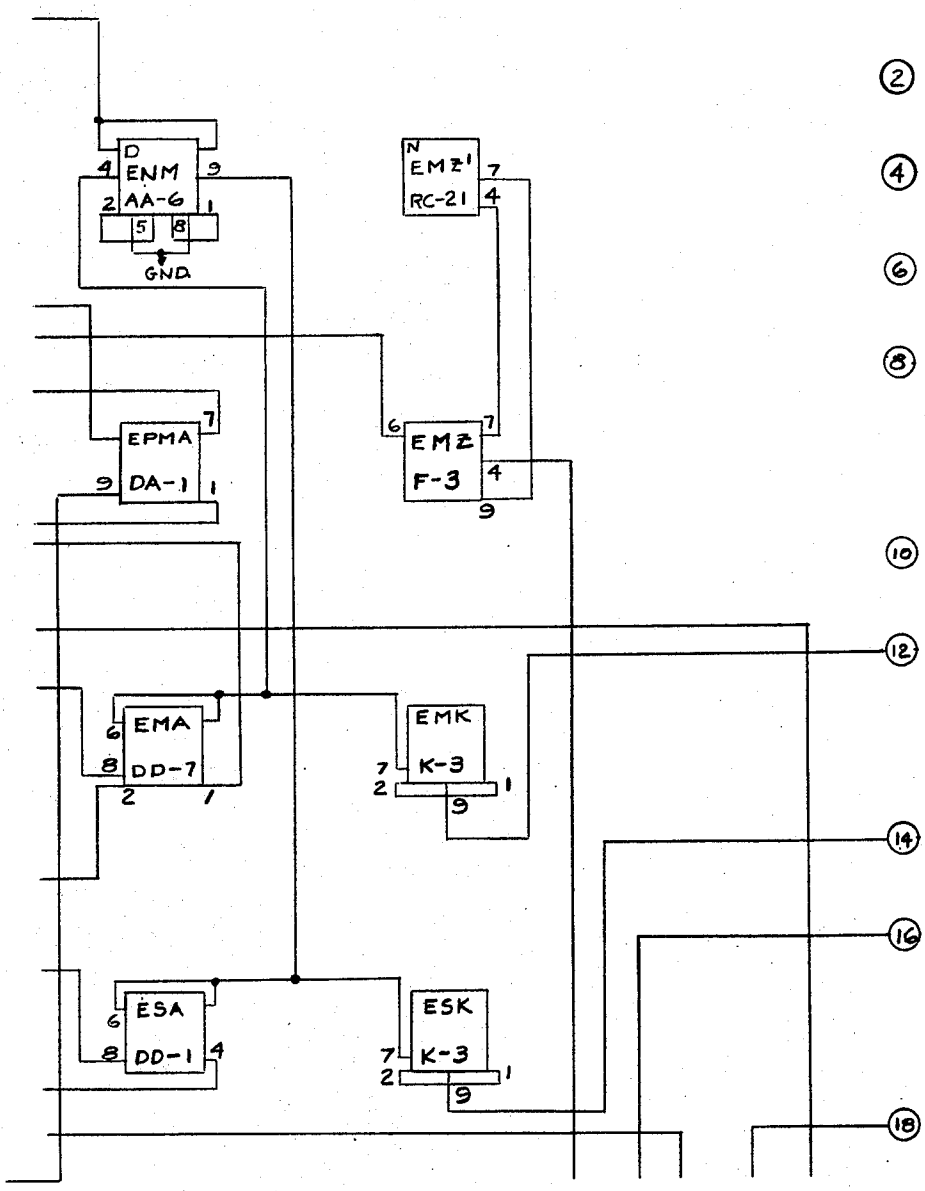


FIG. 18B

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

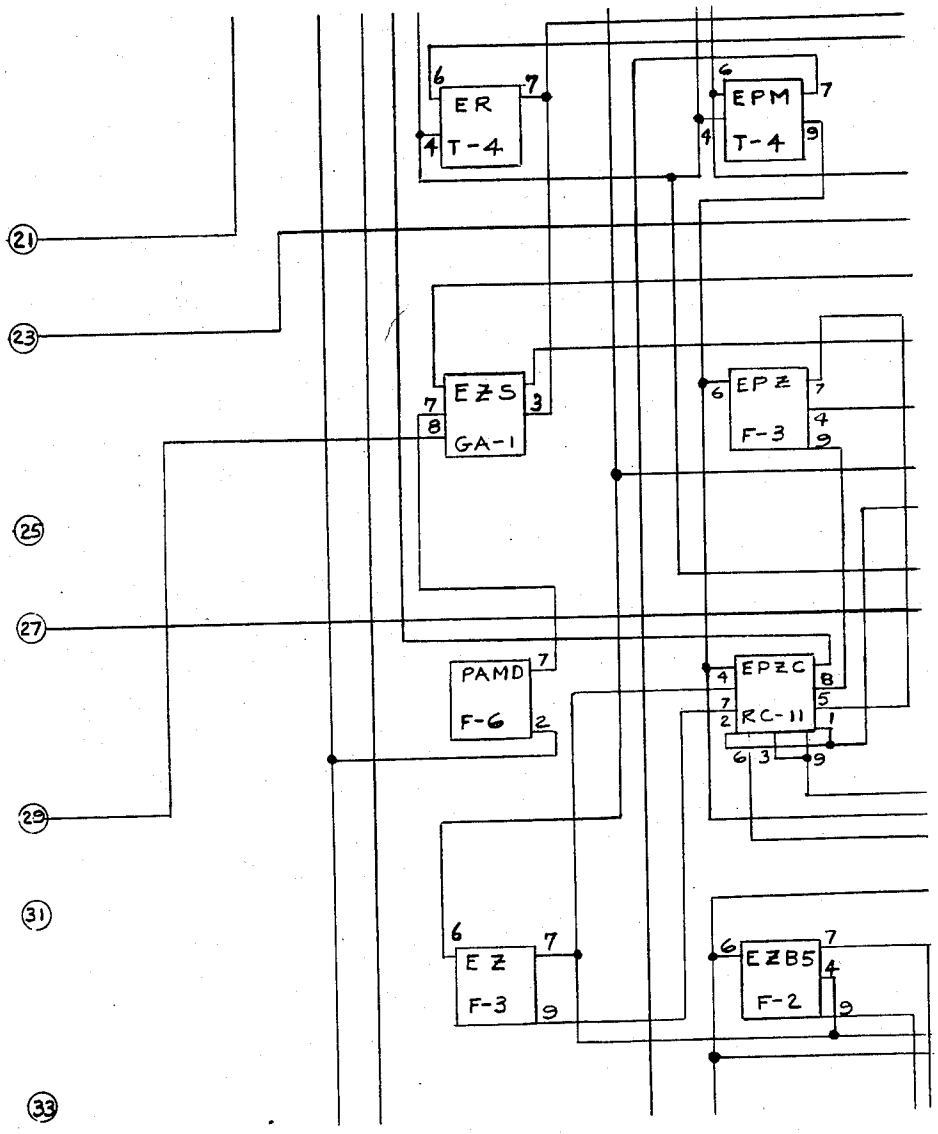


FIG. 18c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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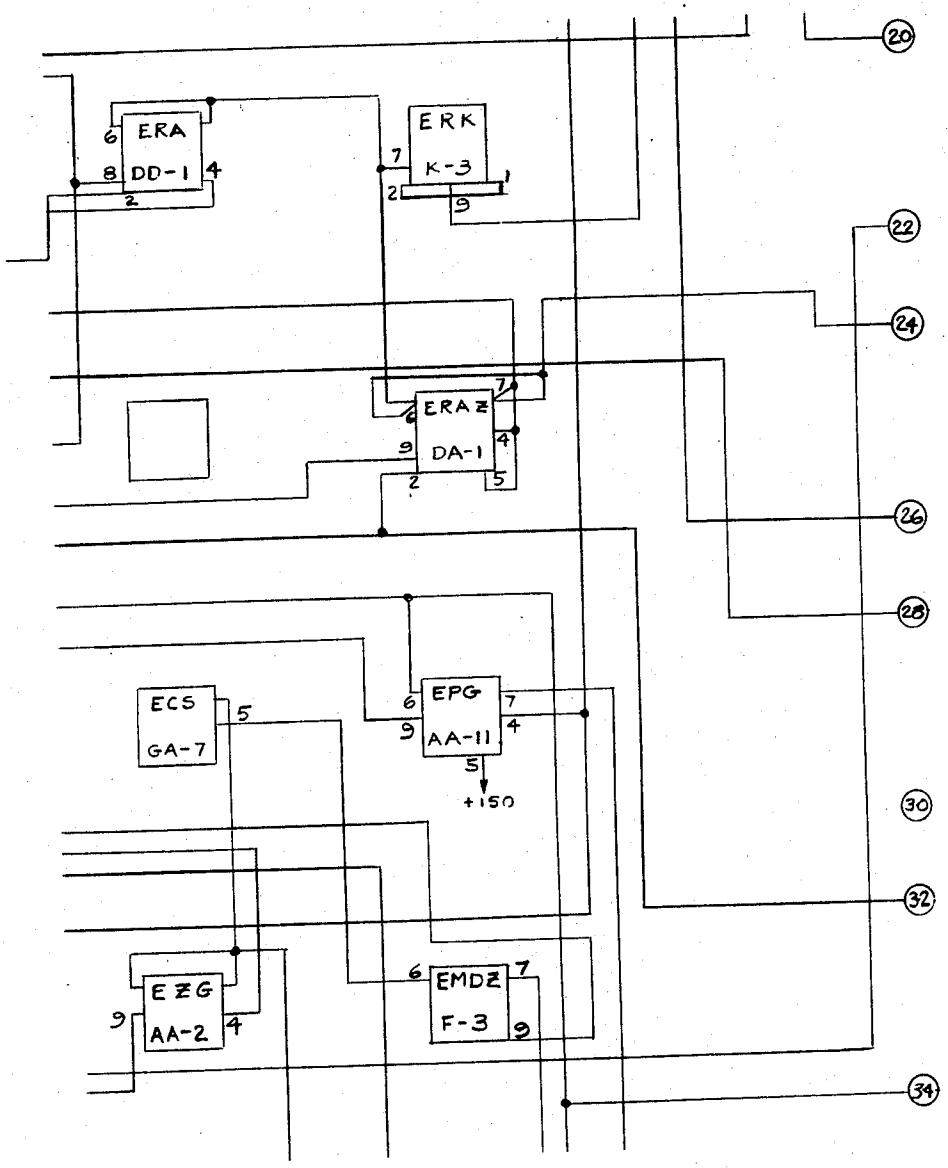


FIG. 18d

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 21

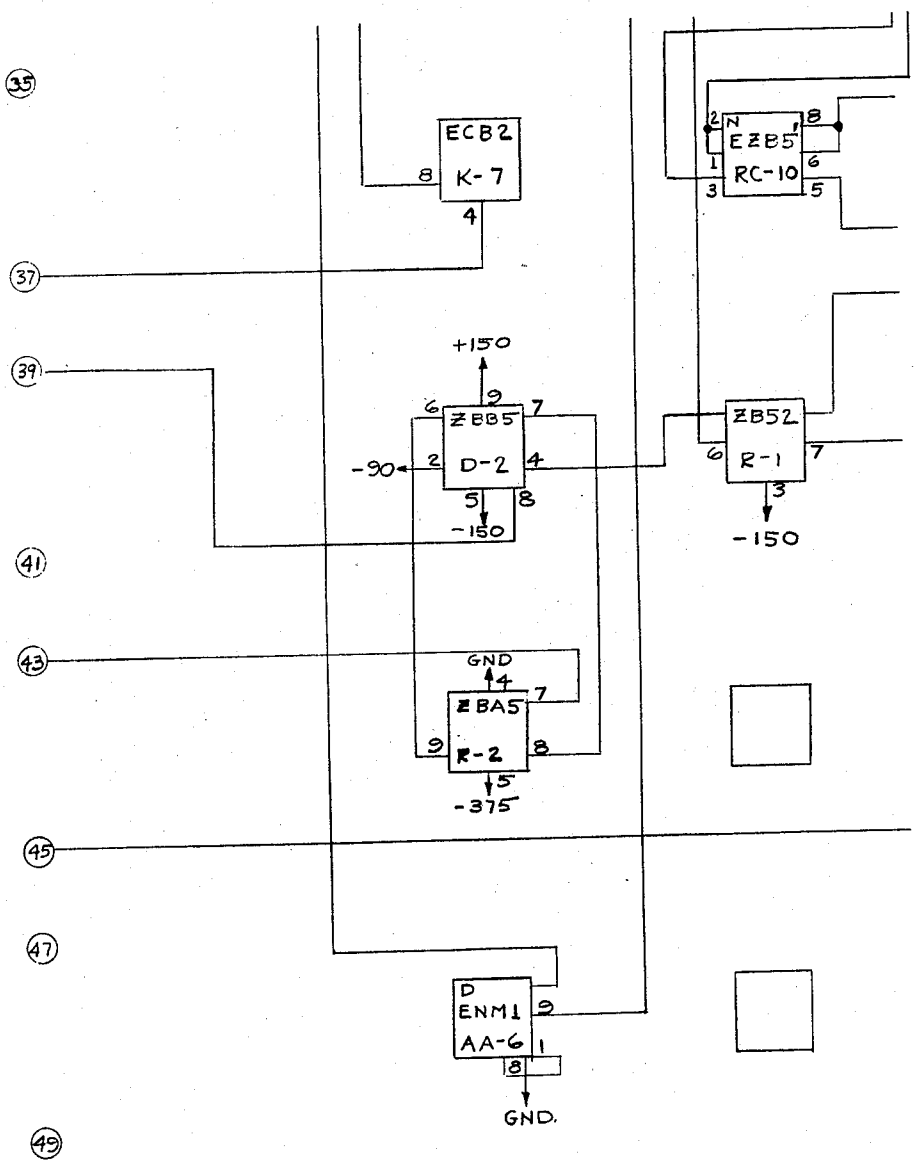


FIG. 18a

INVENTOR
LORING P. CROSMAN
BY Bernard V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 22

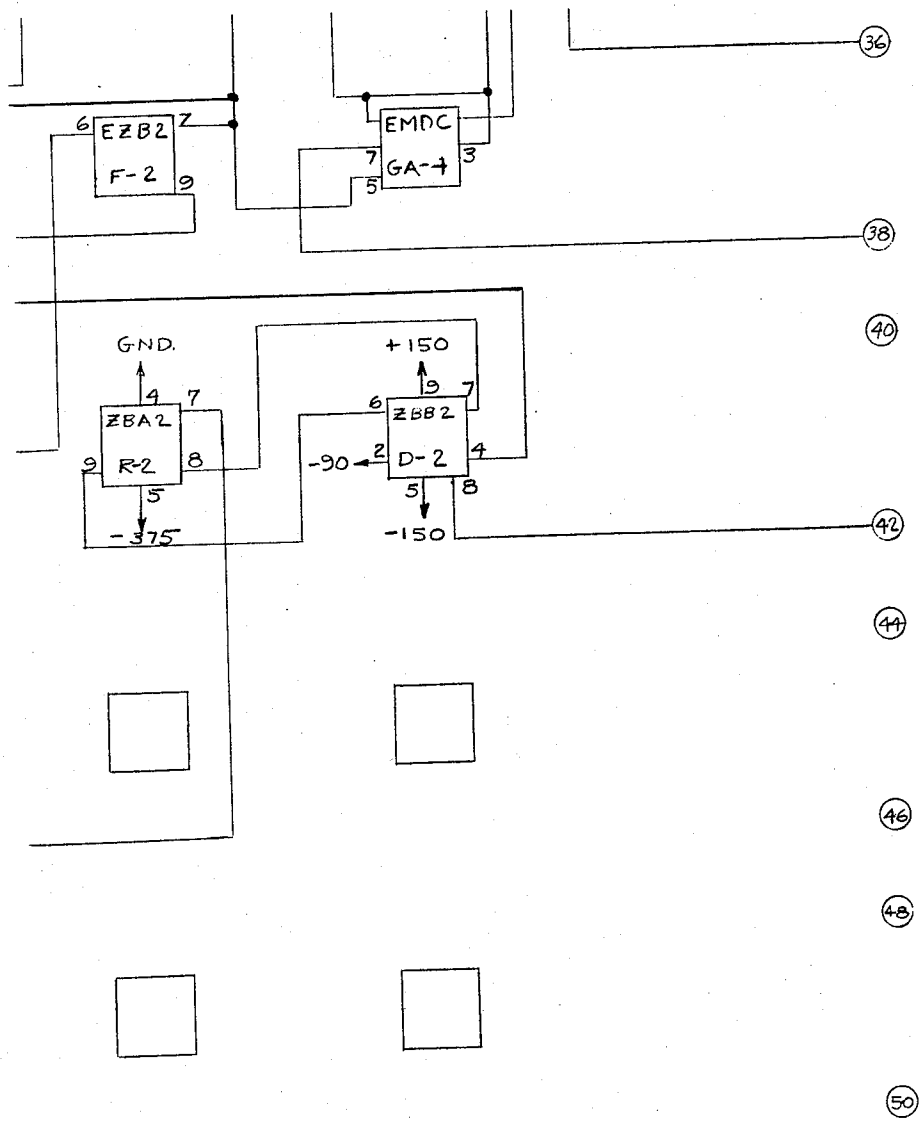


FIG. 18f

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 23

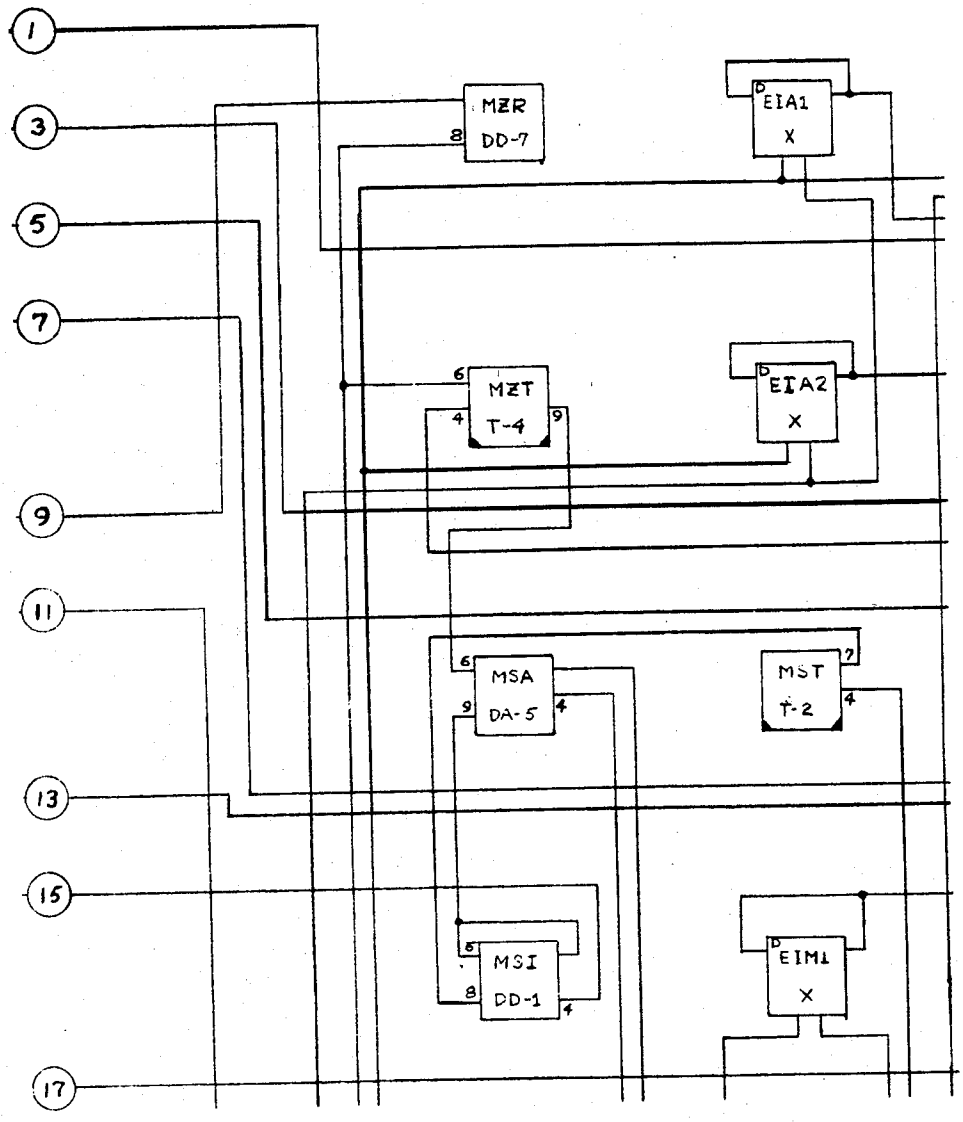


FIG. 19a

FIG. 19a	FIG. 19b
FIG. 19c	FIG. 19d
FIG. 19e	FIG. 19f

FIG. 19g

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 24

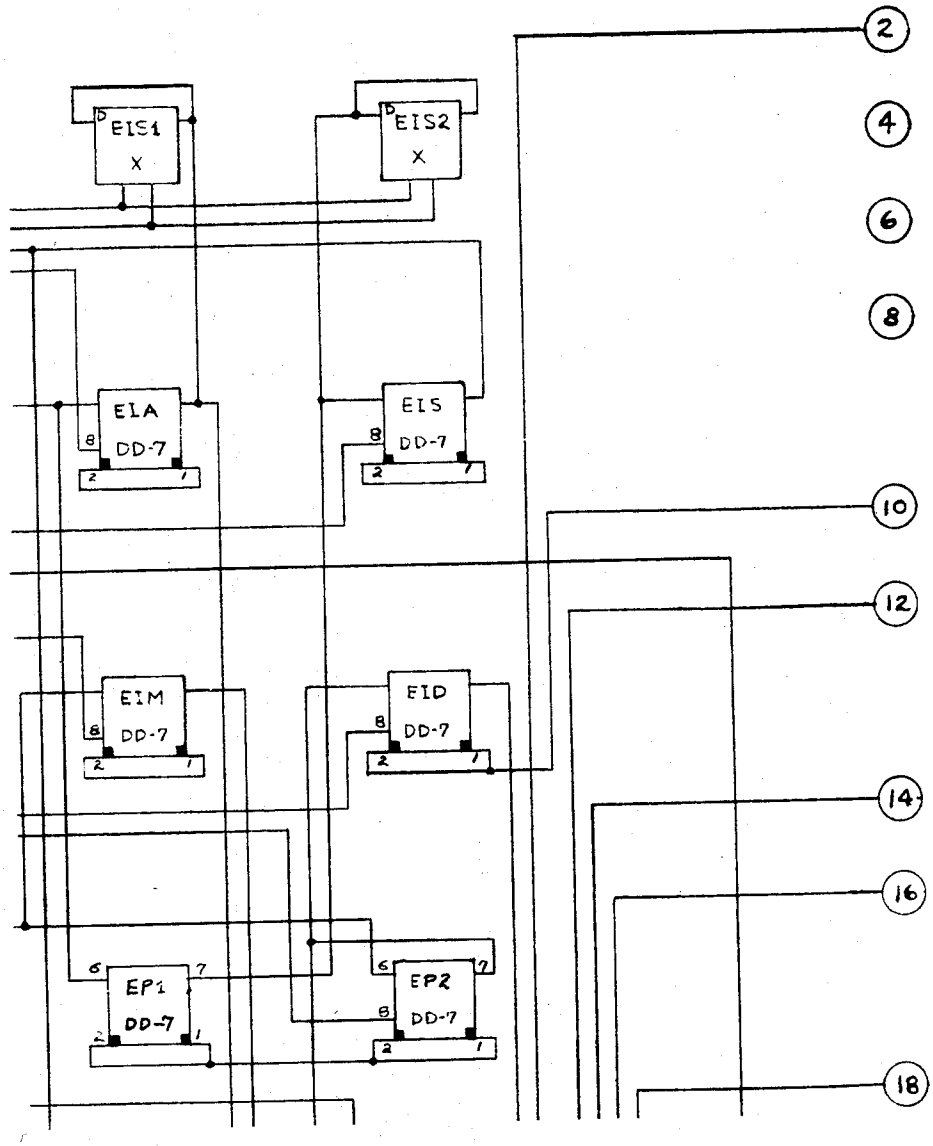


FIG. 19B

INVENTOR
LORING P. CROSMAN
BY George V. Ectgroth
ATTORNEY

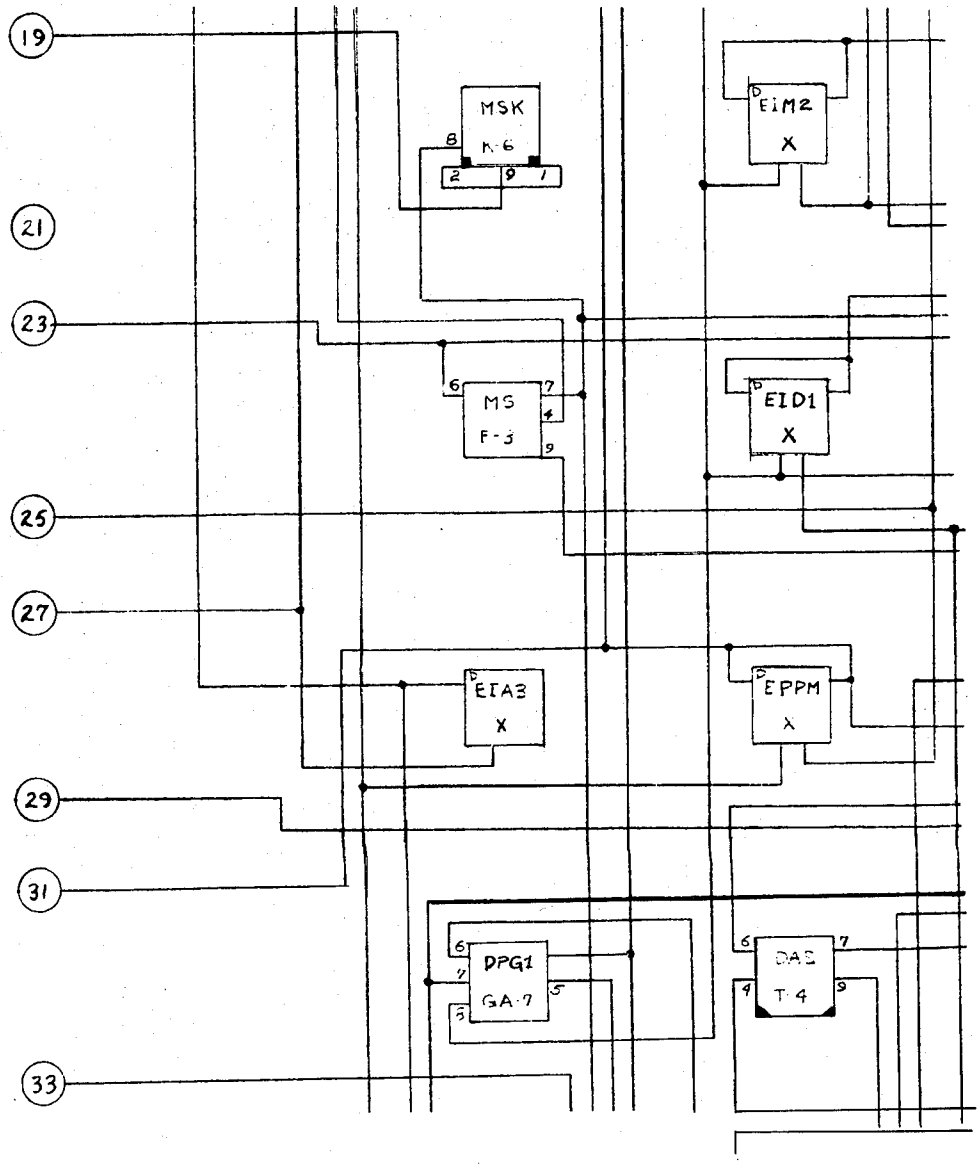


FIG. 19c

INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 26

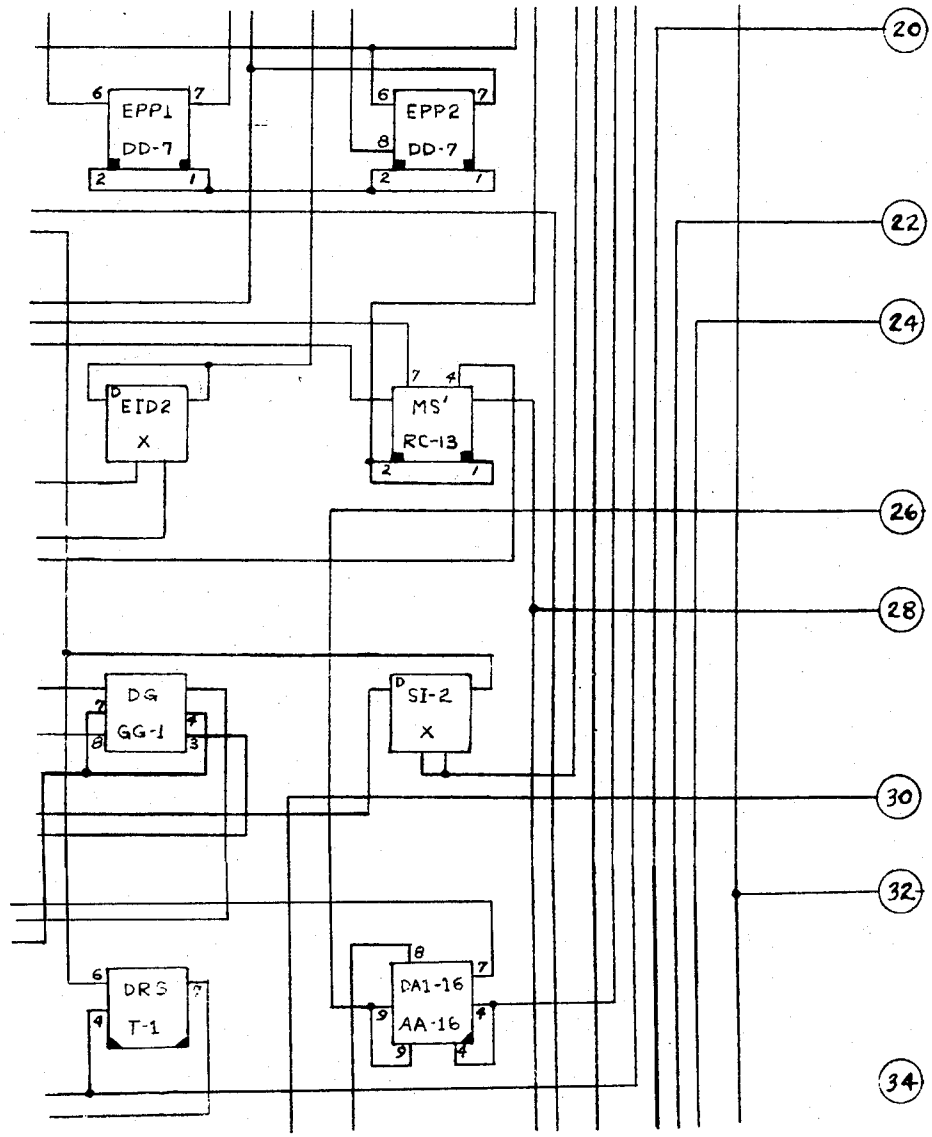


FIG. 19d

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 27

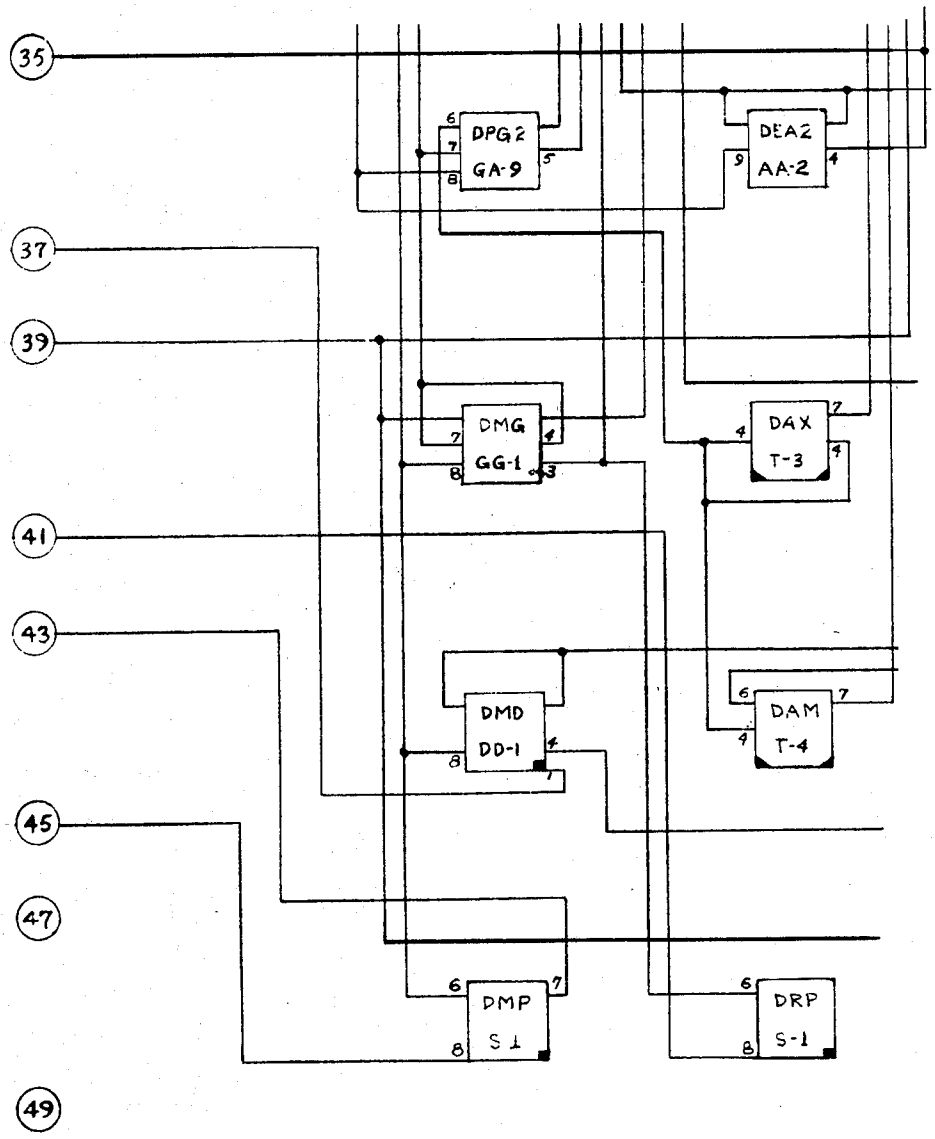


FIG. 19 2

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 28

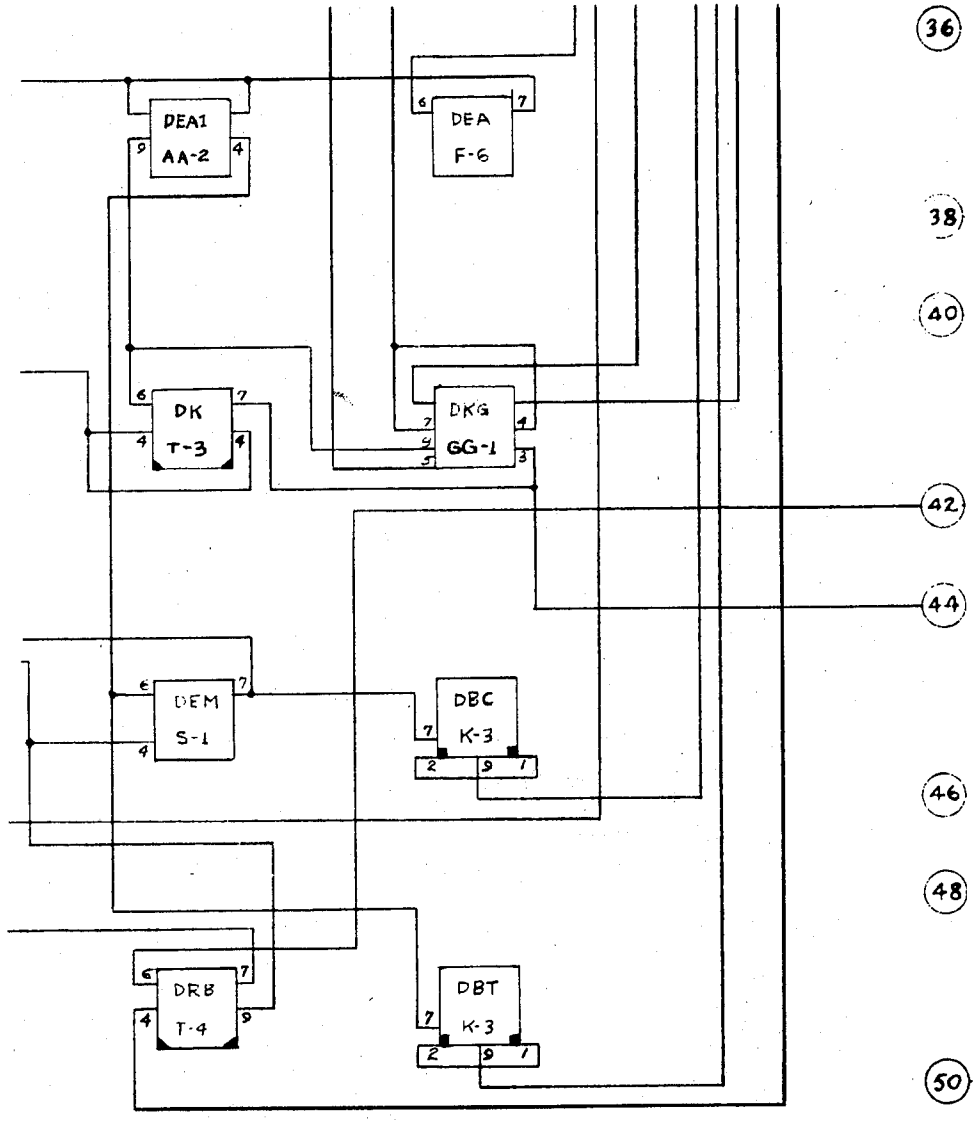


FIG. 19f

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 29

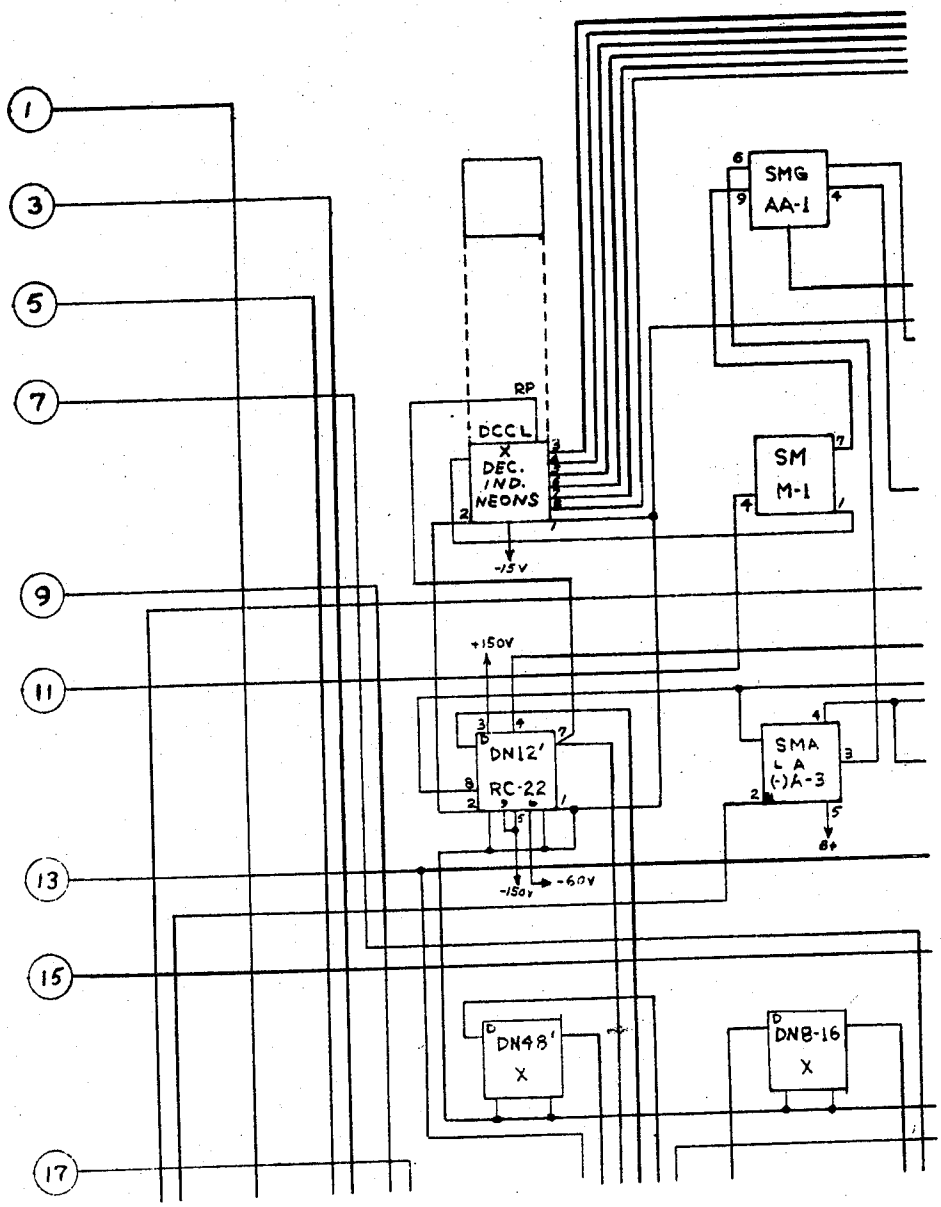


FIG. 20a

FIG. 20a	FIG. 20b
FIG. 20c	FIG. 20d
FIG. 20e	FIG. 20f

FIG. 20g

INVENTOR
LORING P. CROSMAN
BY George V. Ettgrath
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 30

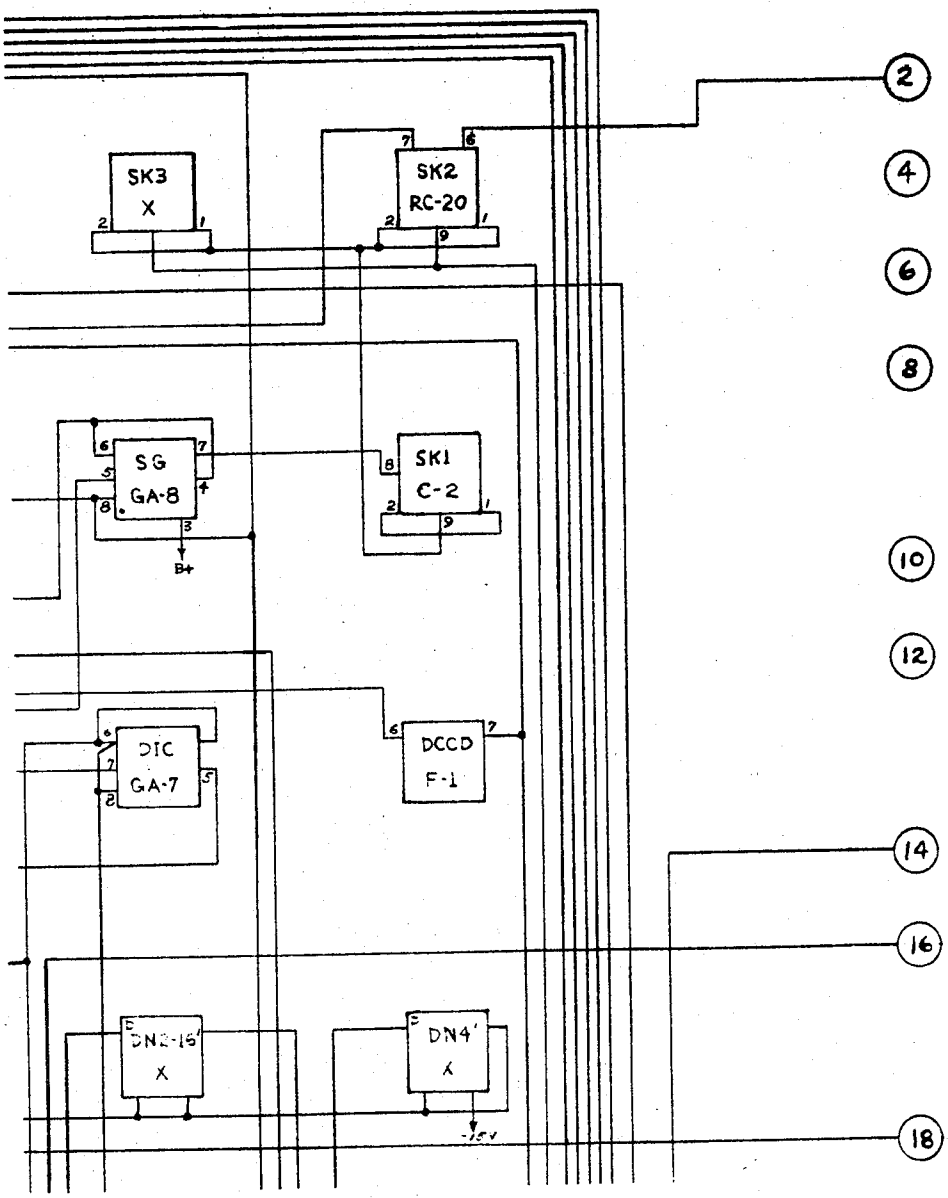


FIG. 20B

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

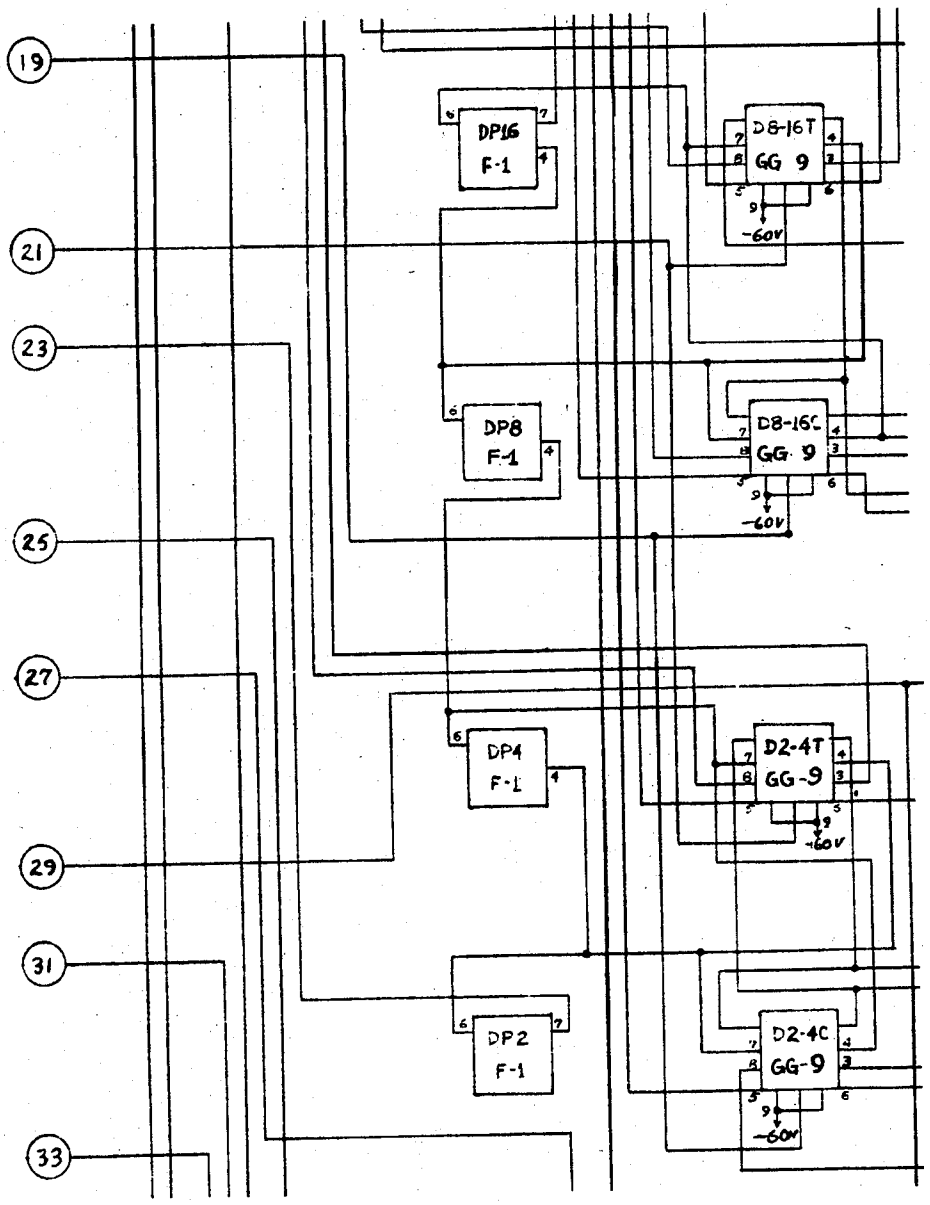


FIG. 20c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 32

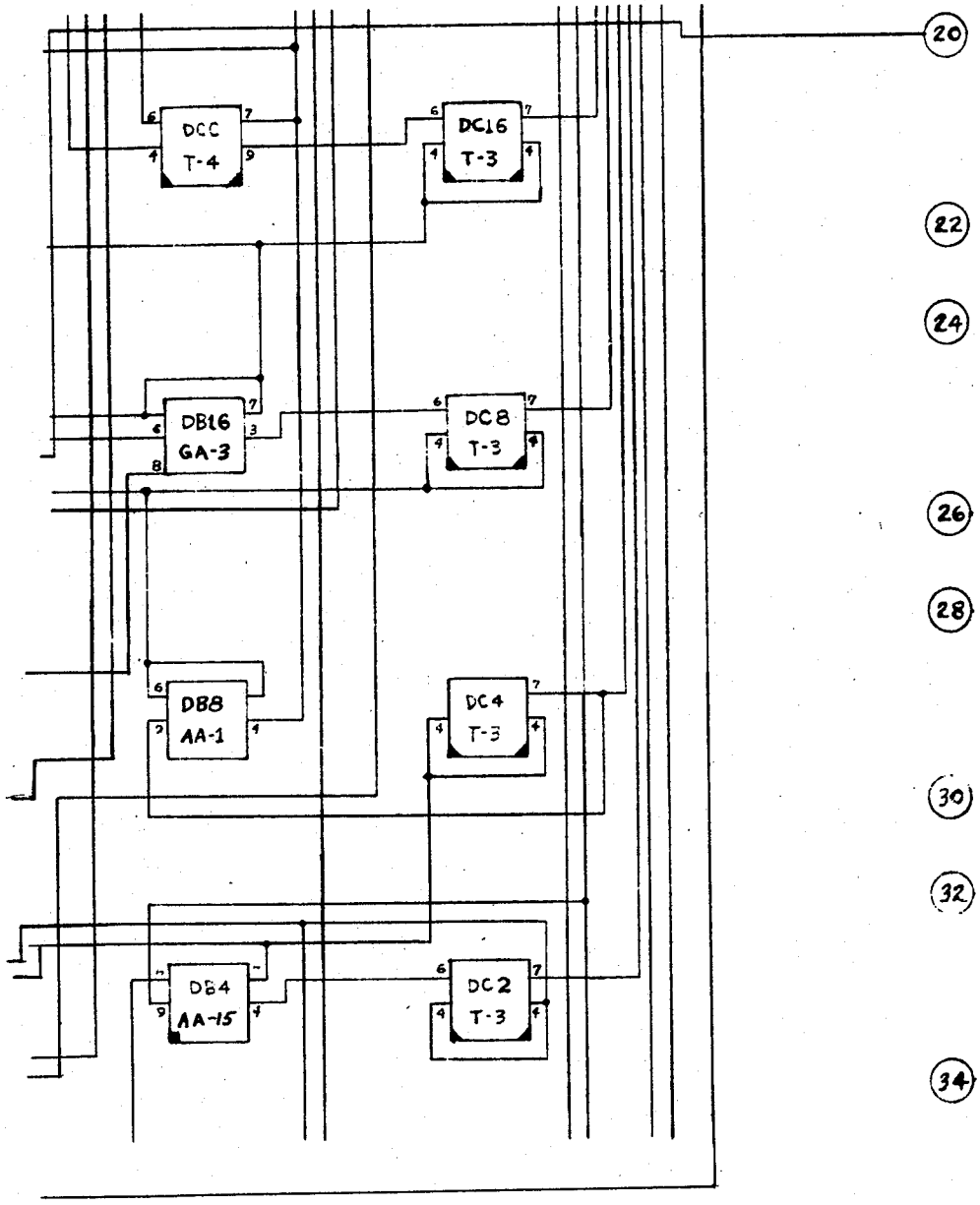


FIG. 20d

INVENTOR
LORING P. CROSMAN

BY George V. Zeigrath

ATTORNEY

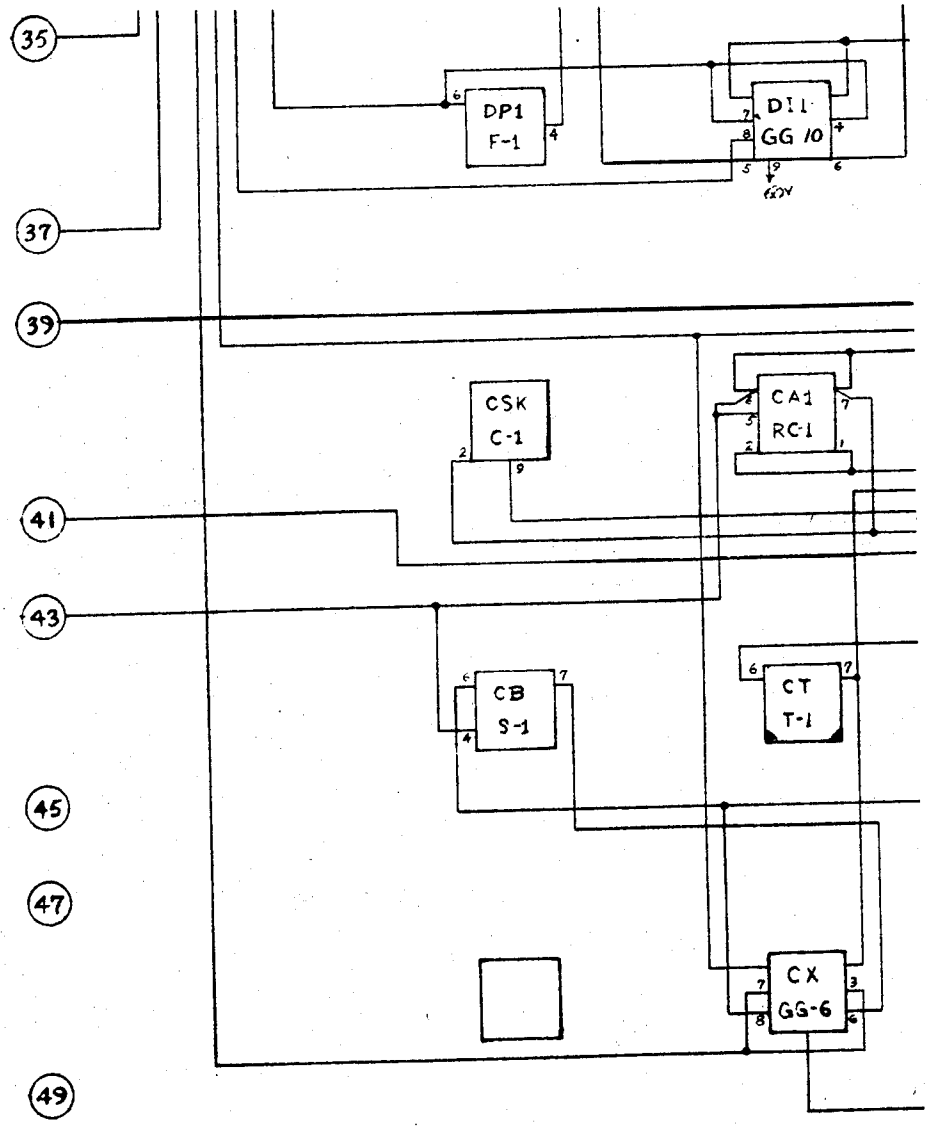


FIG. 20a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

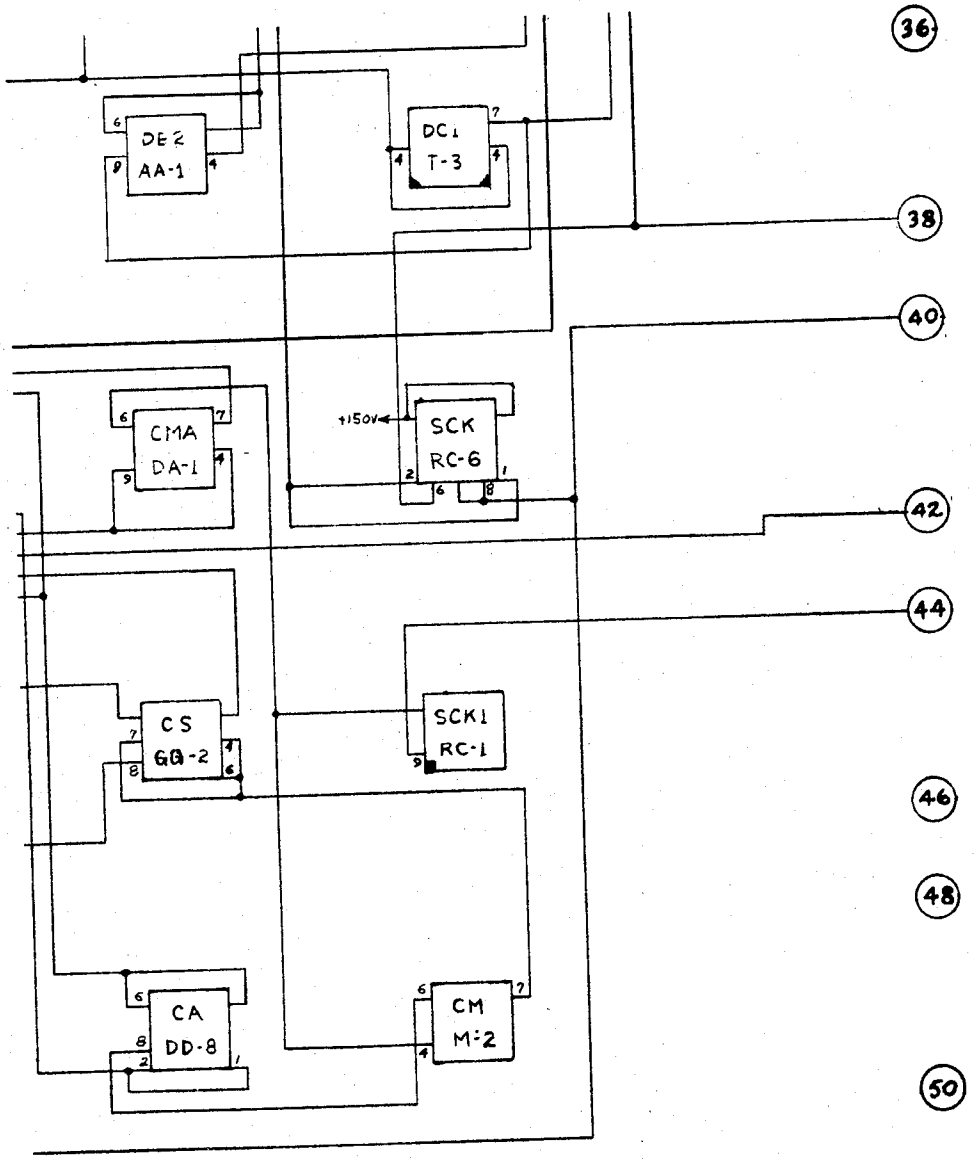


FIG. 20f

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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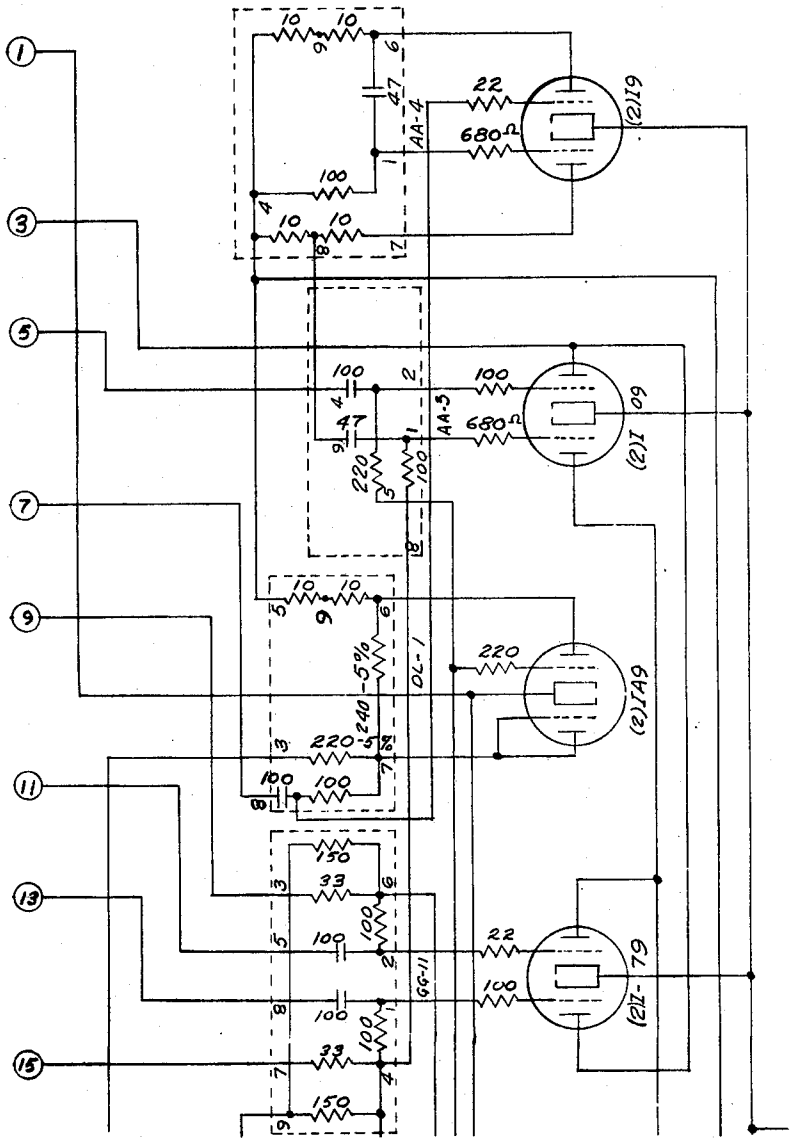


FIG. 21a	FIG. 21b
FIG. 21c	FIG. 21d

FIG. 21a

FIG. 21b

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 36

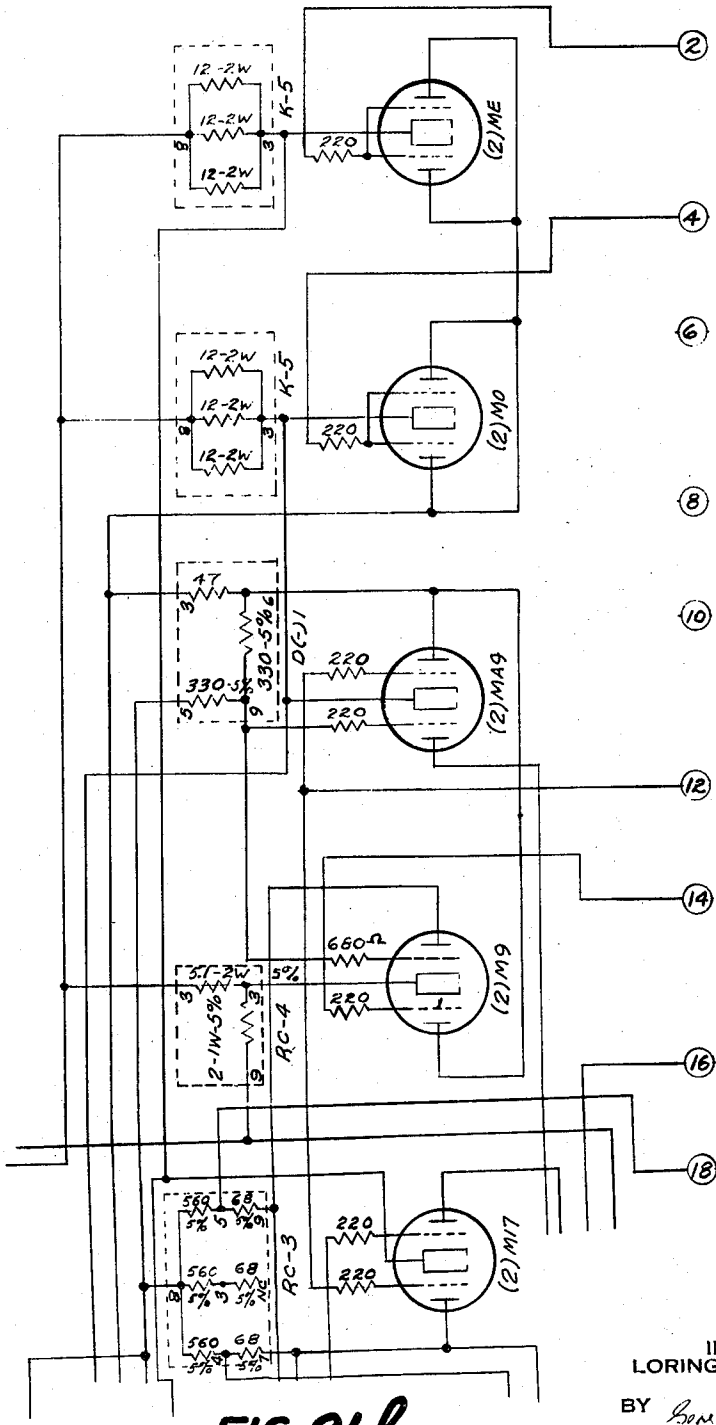


FIG. 21b

INVENTOR
LORING P. CROSMAN

BY George W. Ellyrath

ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 37

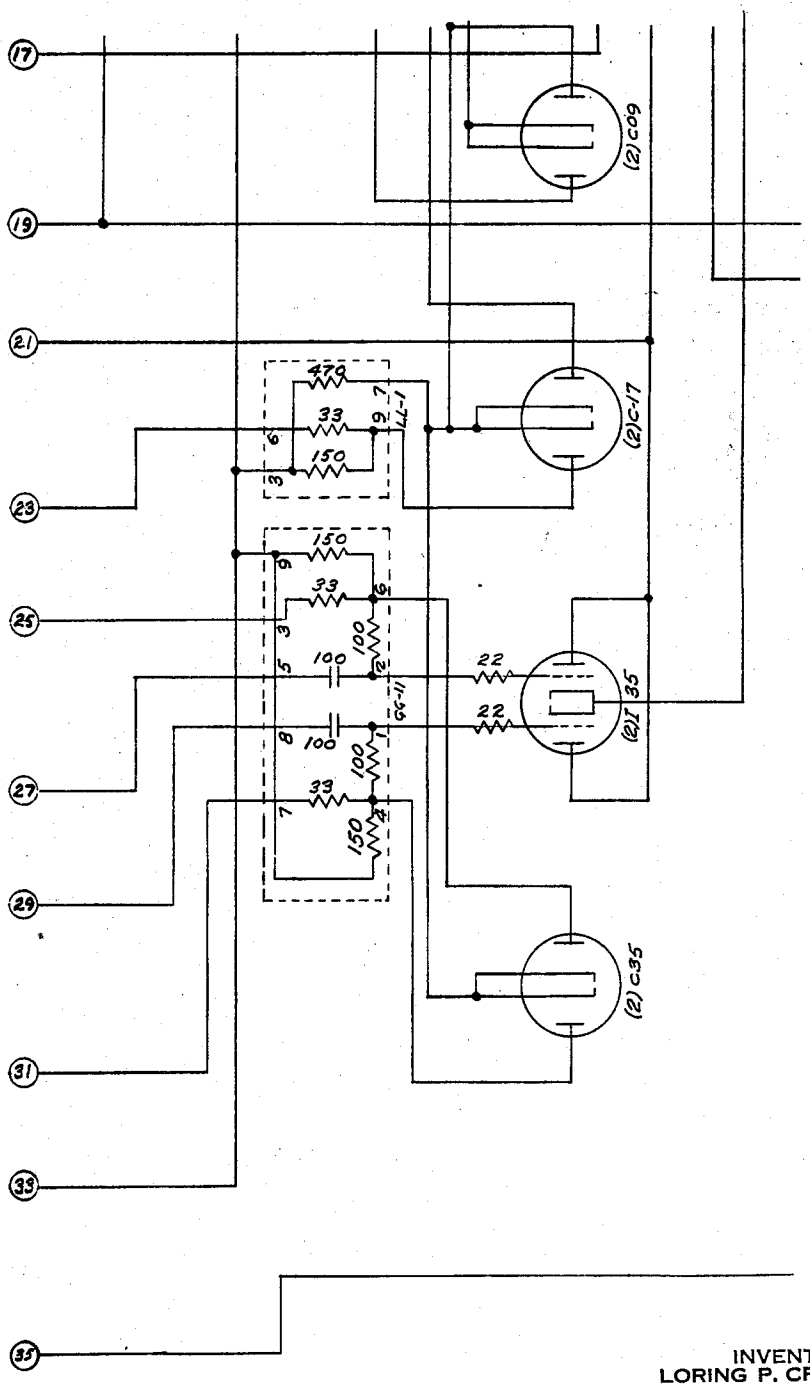


FIG. 21c

INVENTOR
LORING P. CROSMAN

BY George U. Eldredth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 38

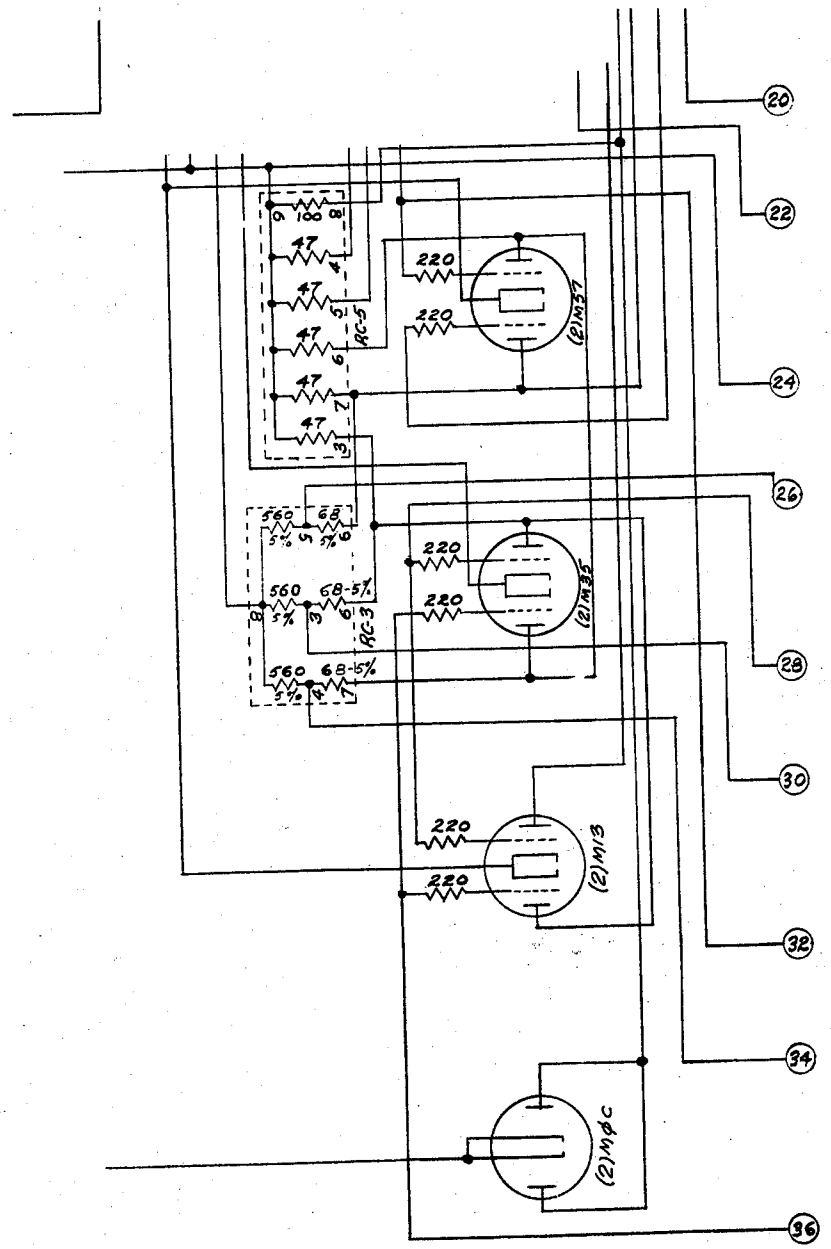


FIG. 21d

INVENTOR
LORING P. CROSMAN
BY George V. Kilgrath
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 39

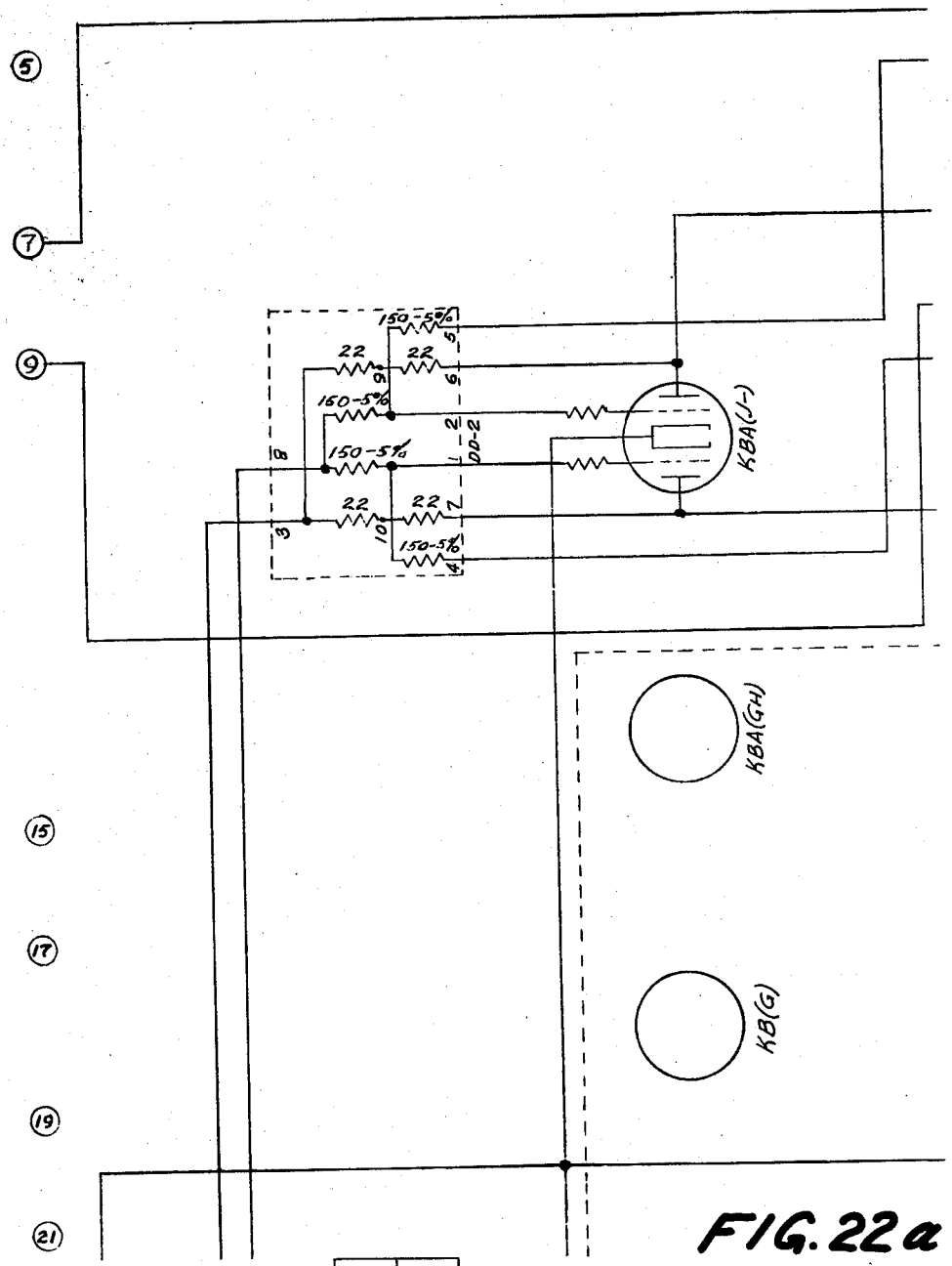


FIG. 22a

FIG. 22a	FIG. 22b
FIG. 22c	FIG. 22d

FIG. 22

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 40

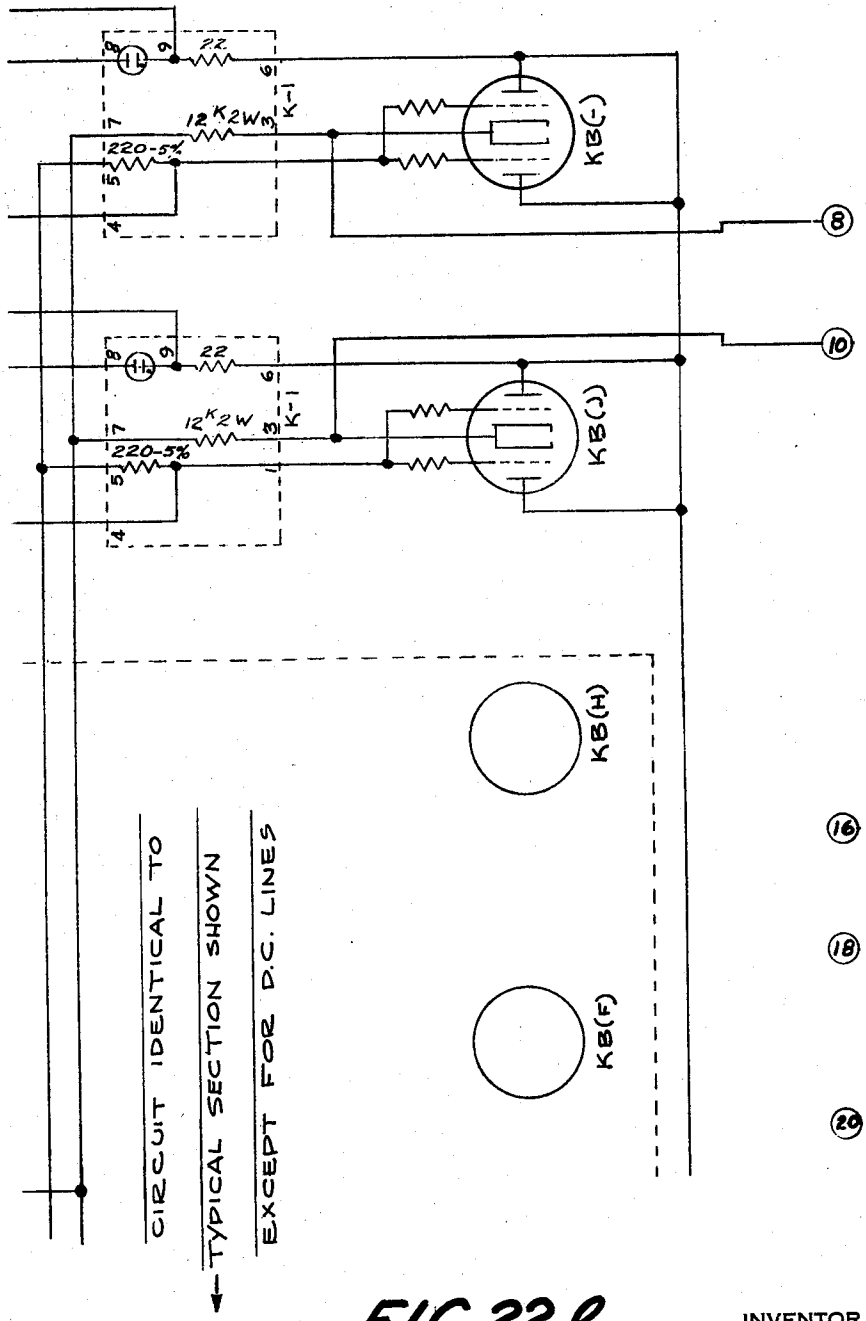


FIG. 22e

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 41

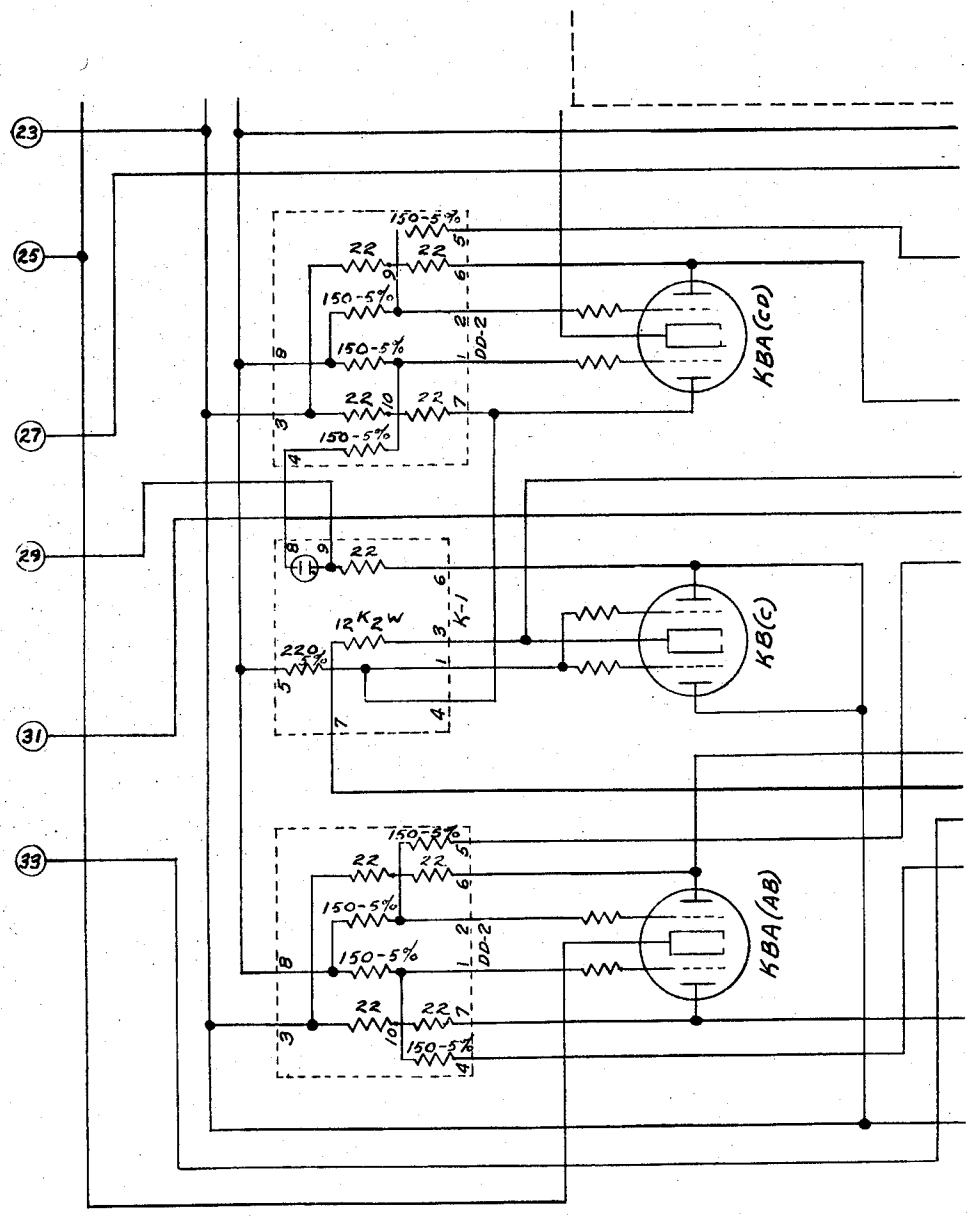


FIG. 22c

INVENTOR
LORING P. CROSMAN
BY George V. Leitzell
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 42

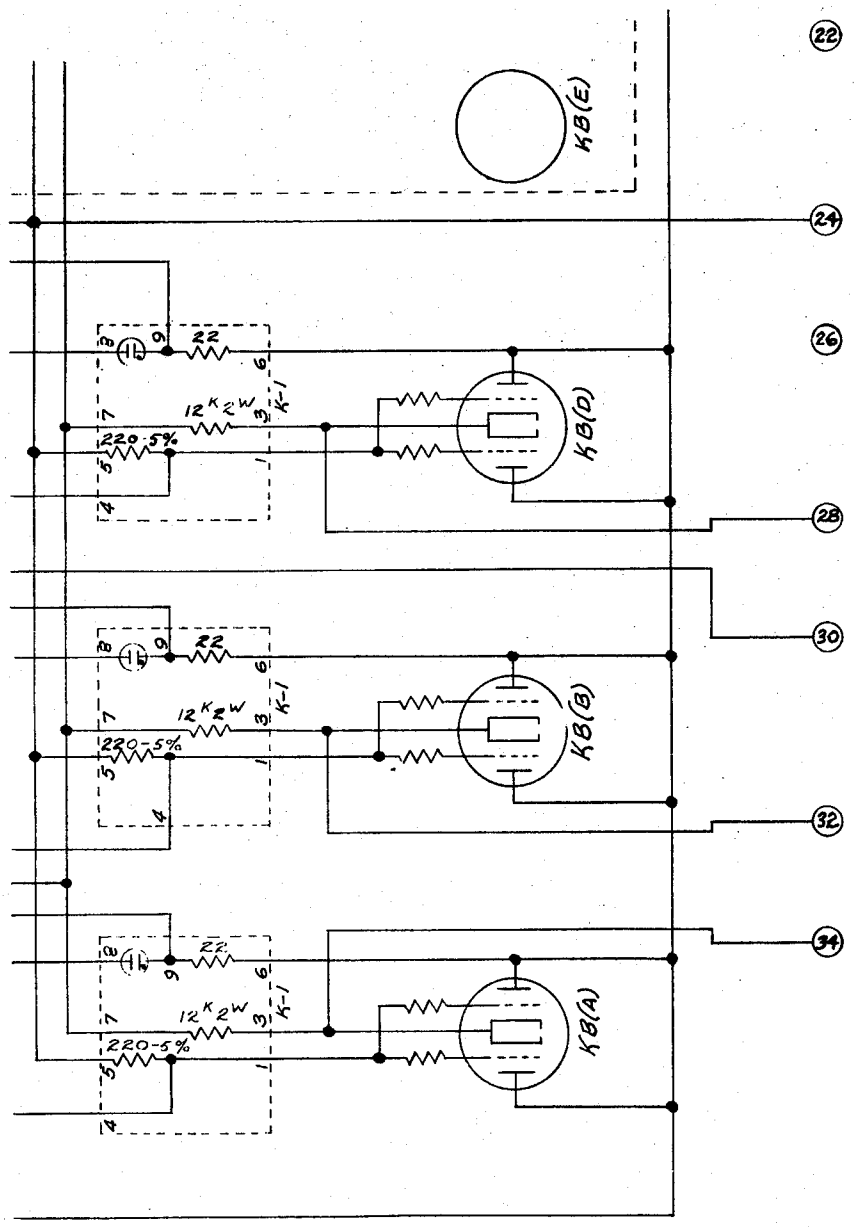


FIG. 22d

INVENTOR
LORING P. CROSMAN

BY George H. Elgin

ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 43

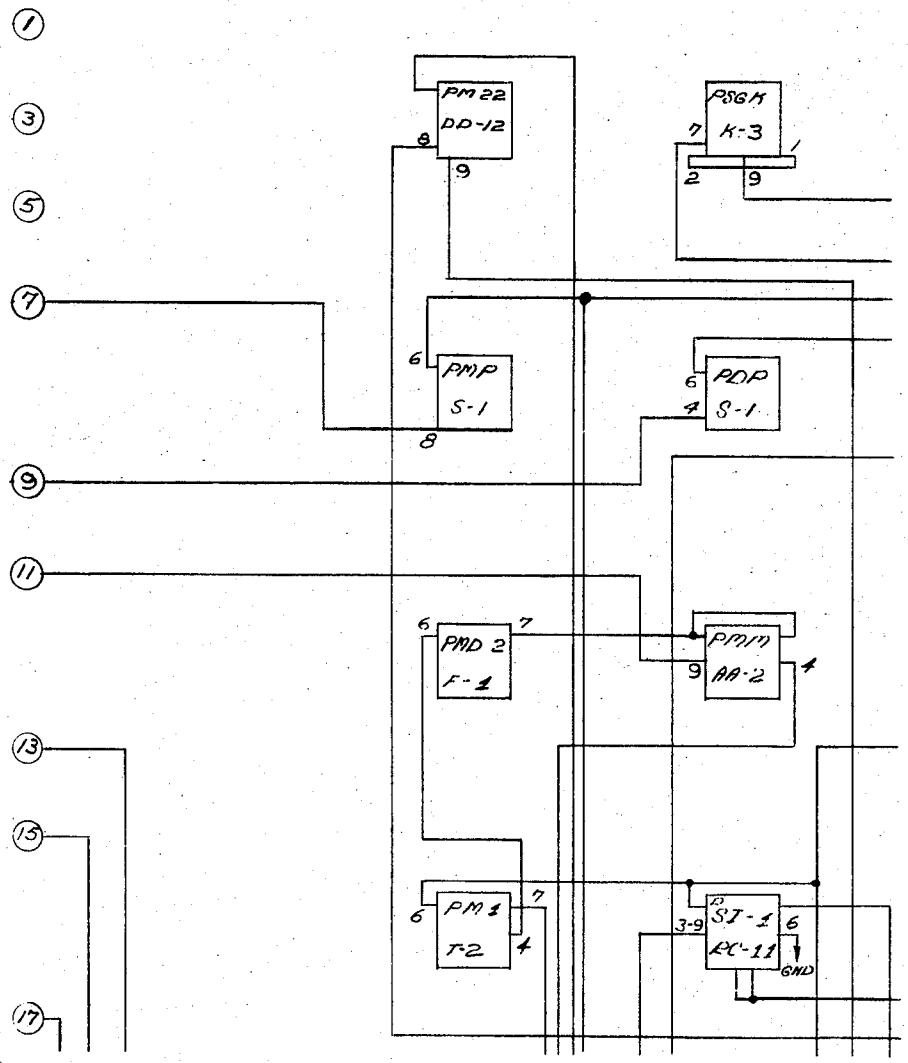


FIG. 23a

FIG. 23a	FIG. 23b
FIG. 23c	FIG. 23d
FIG. 23e	FIG. 23f

FIG. 23g

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 44

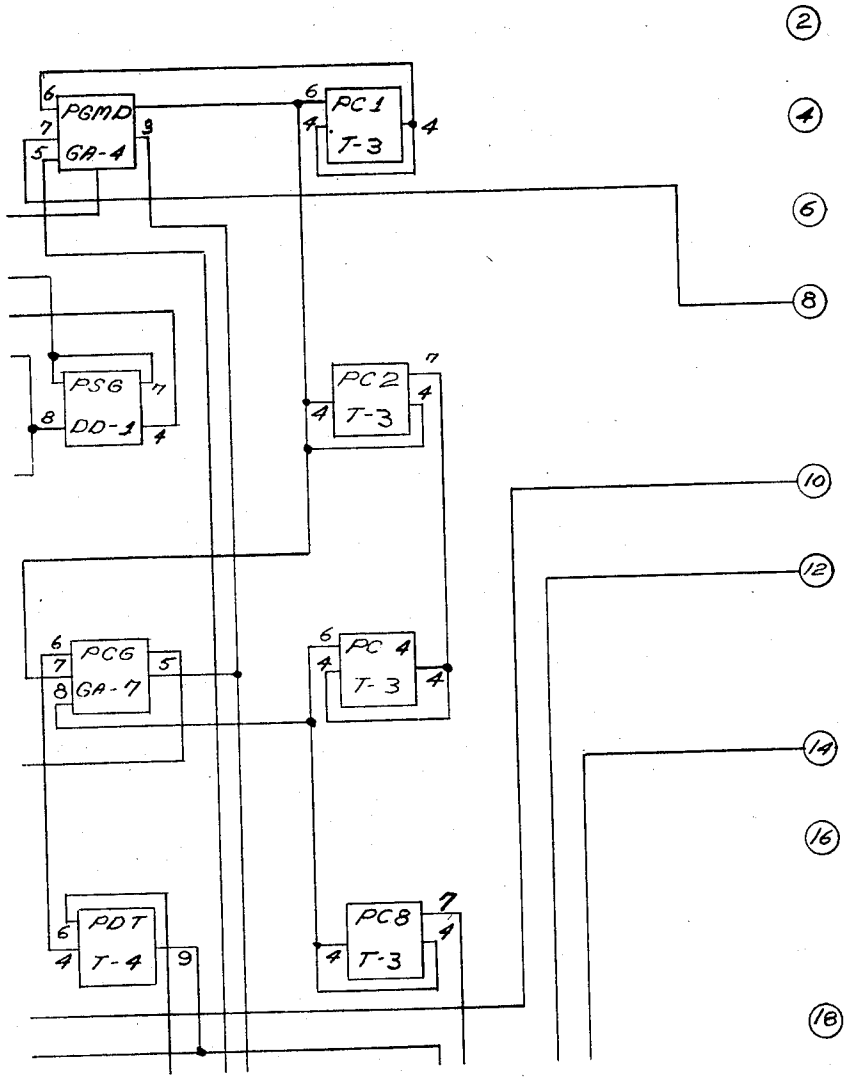


FIG. 23b

INVENTOR
LORING P. CROSMAN

BY George V. Blythe

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 45

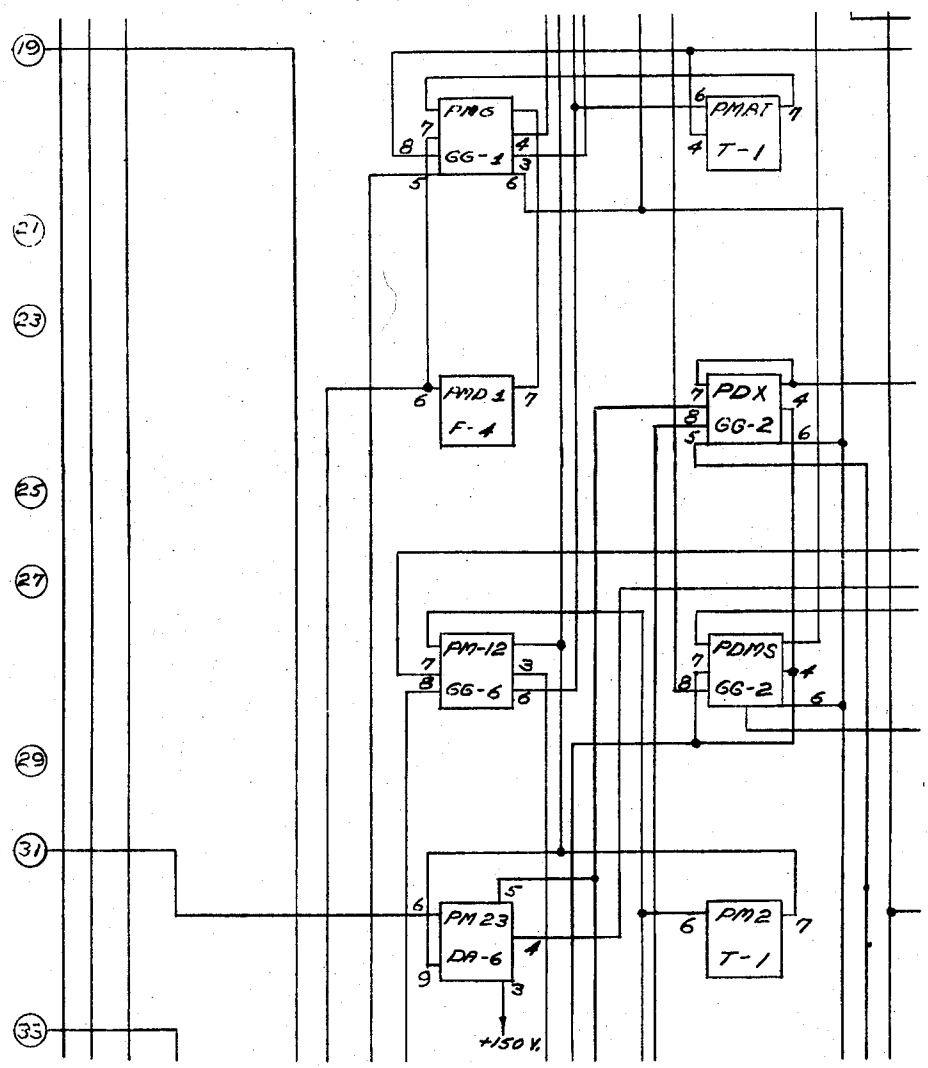


FIG. 23c

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

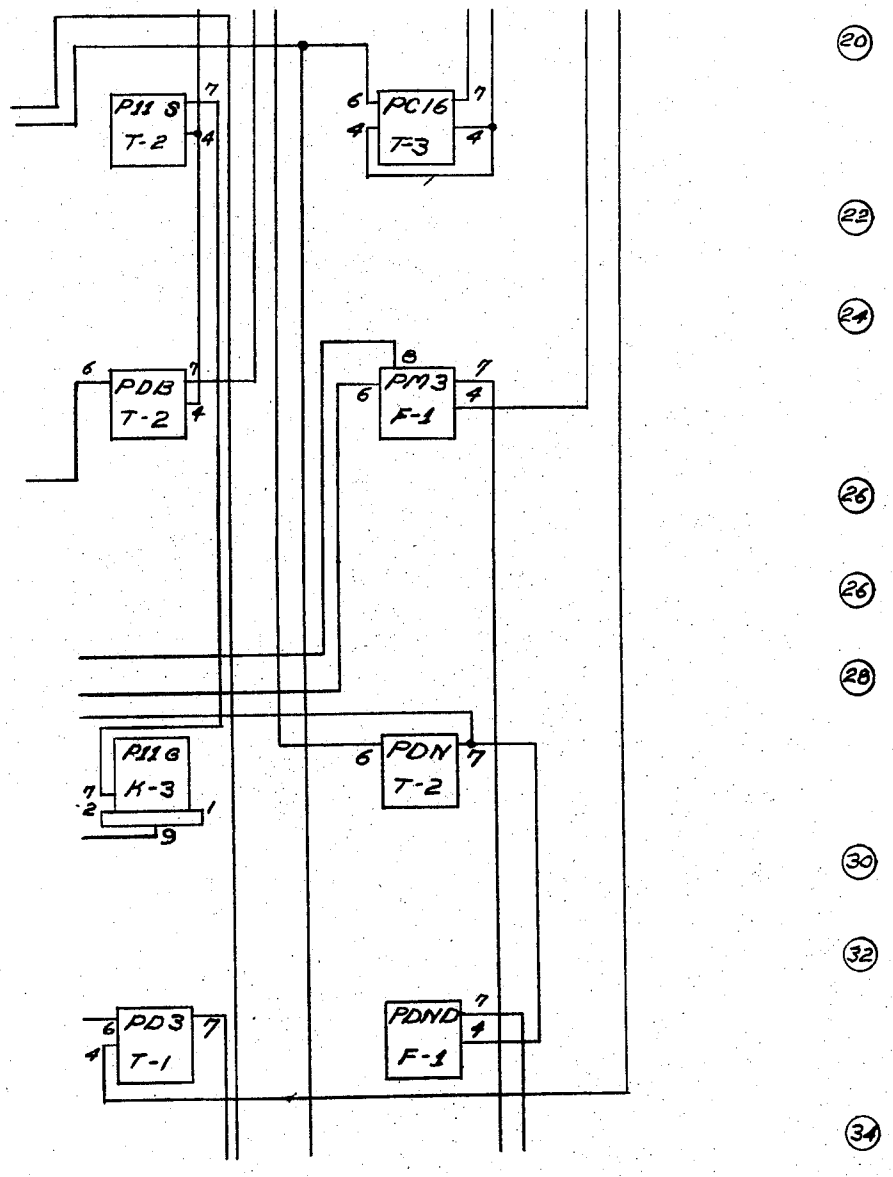


FIG. 23d

INVENTOR
LORING P. CROSMAN
BY George V. Ettgrath
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 47

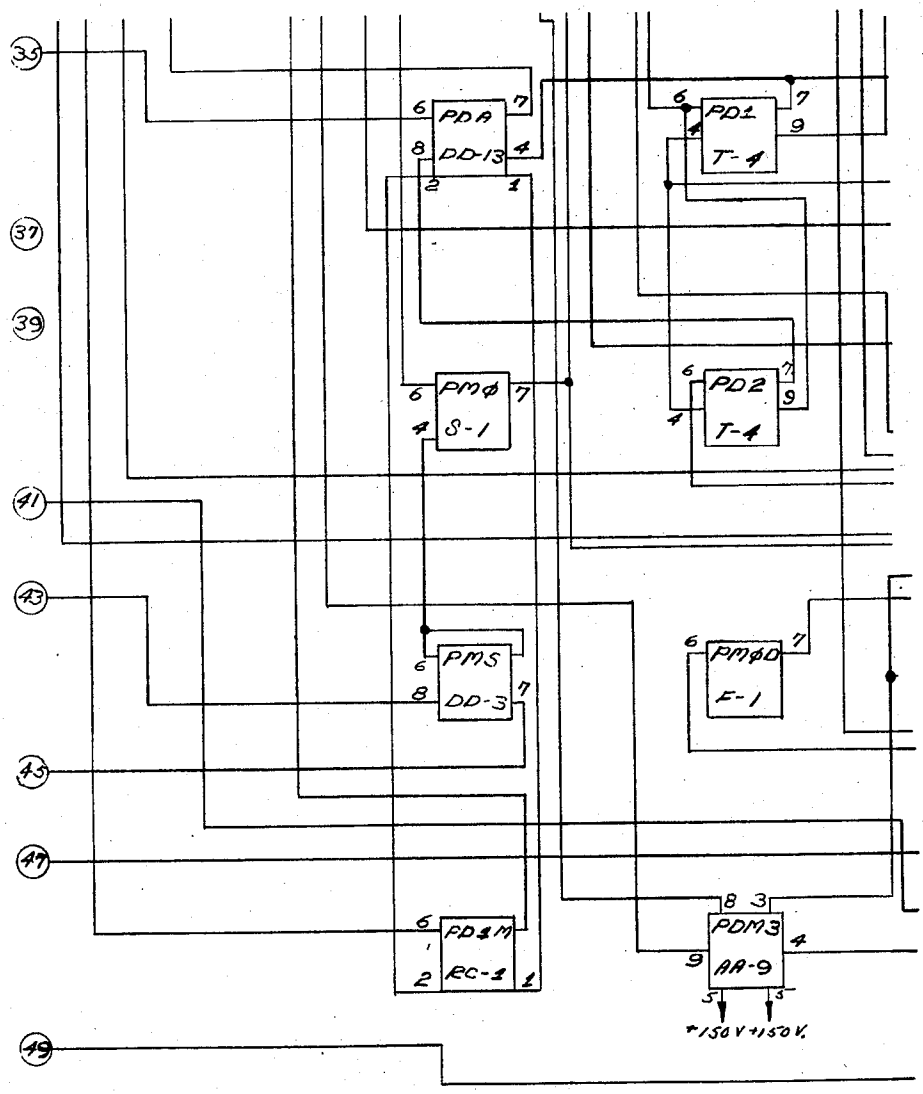


FIG. 23a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

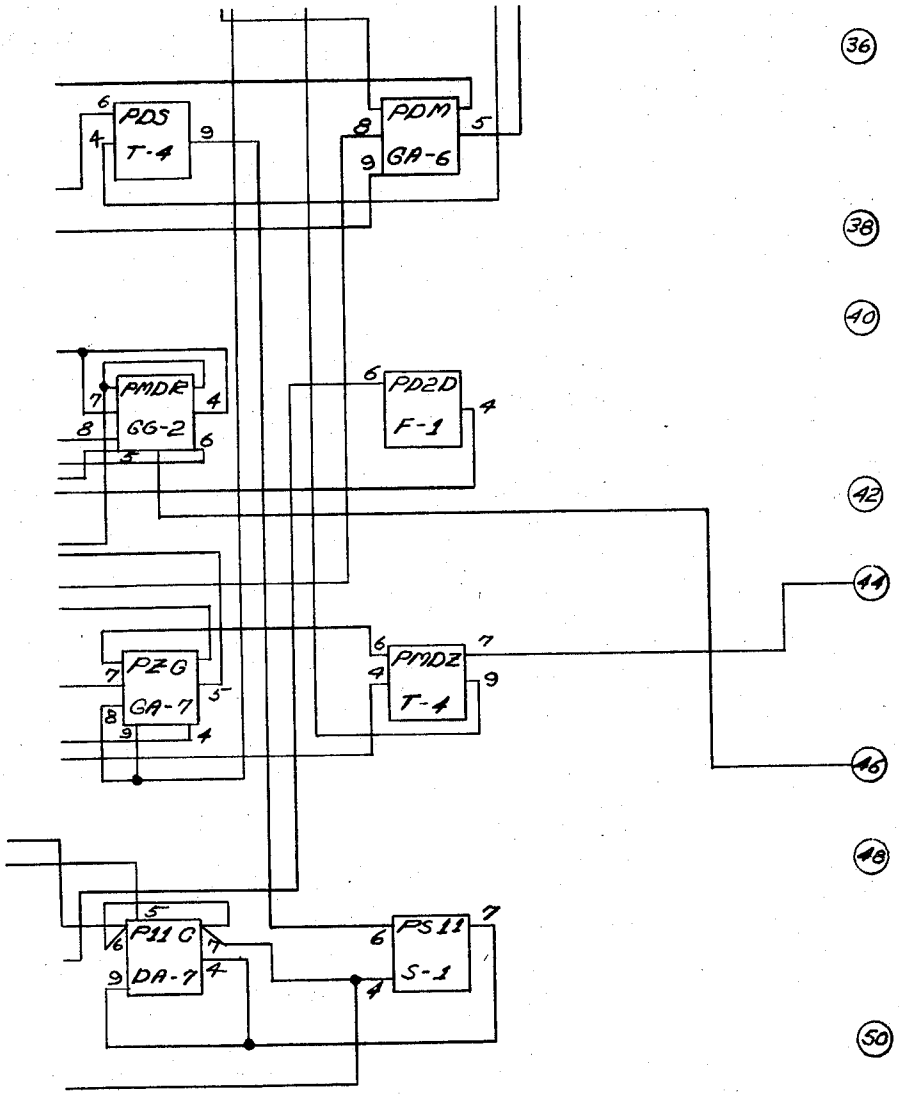


FIG. 23f

INVENTOR
LORING P. CROSMAN
BY George V. Fitzpatrick
ATTORNEY

FIG. 24a

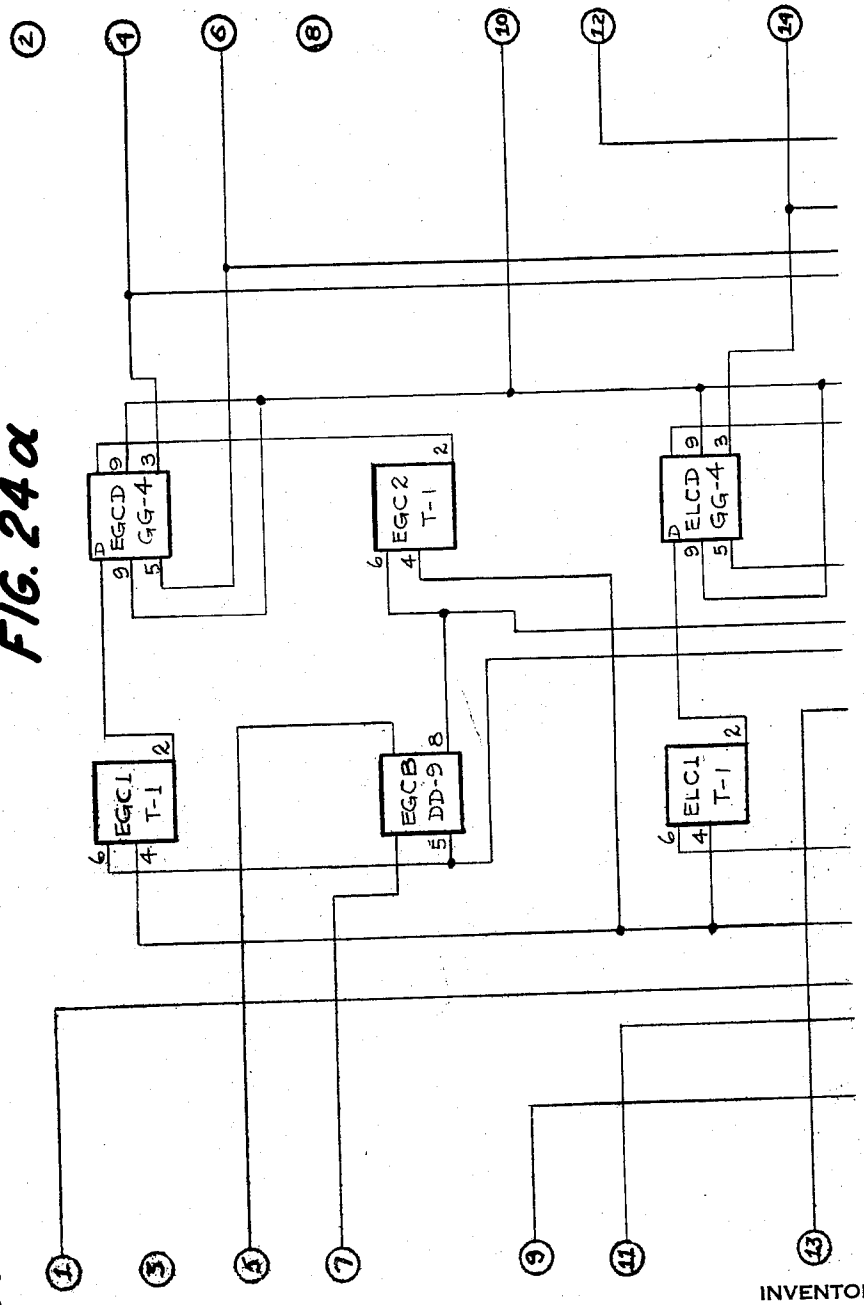


FIG. 24b

FIG. 24a	FIG. 24b	FIG. 24c	FIG. 24d

INVENTOR
LORING P. CROSMAN
BY George V. Telgrath
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 50

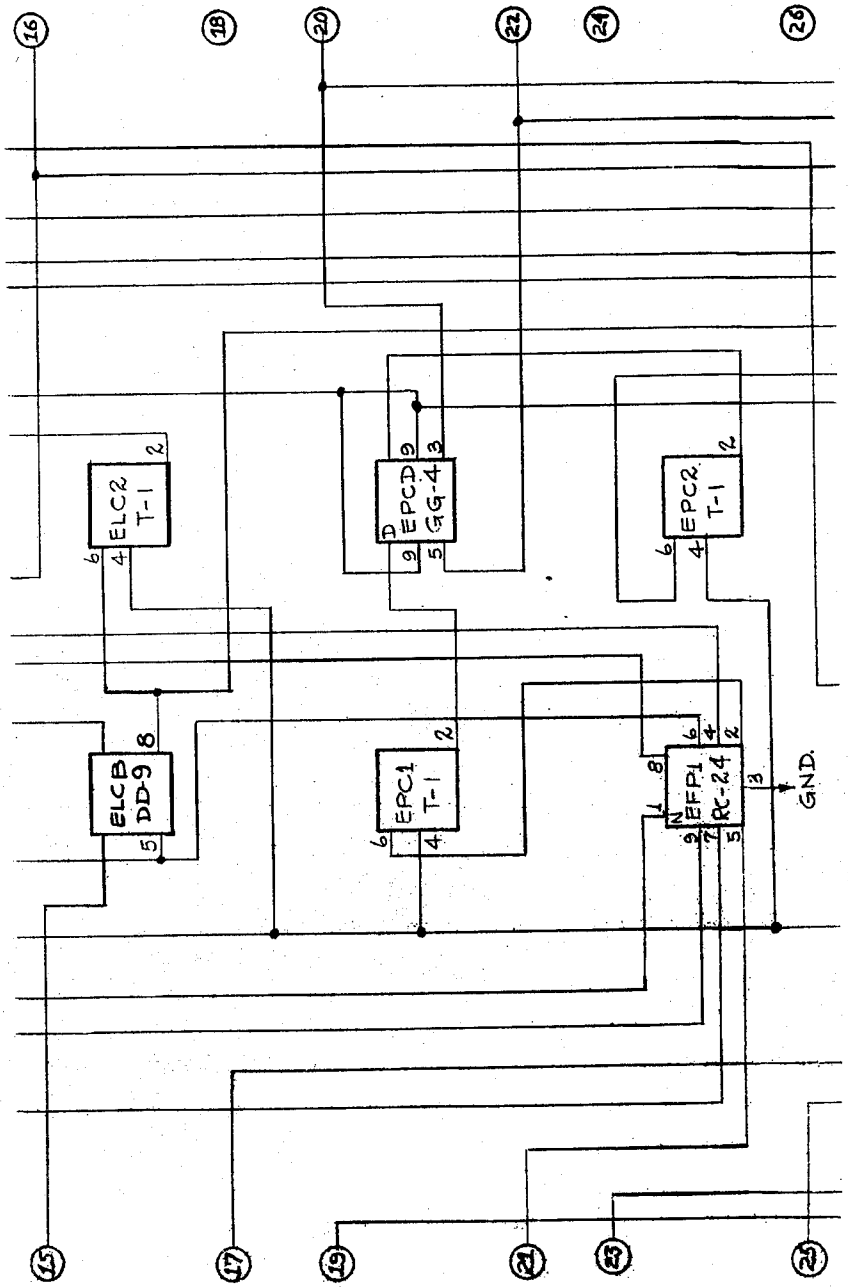
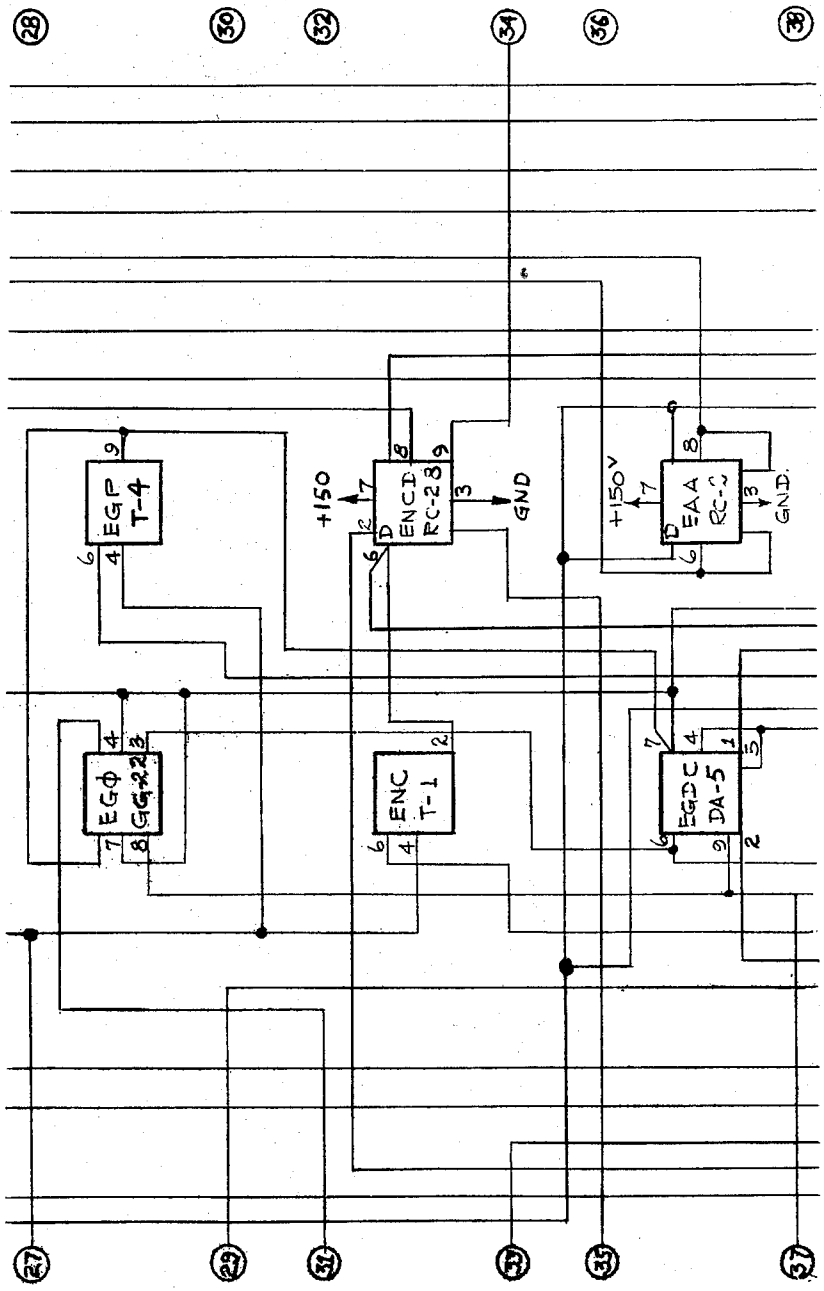


FIG. 24A

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

FIG. 24c

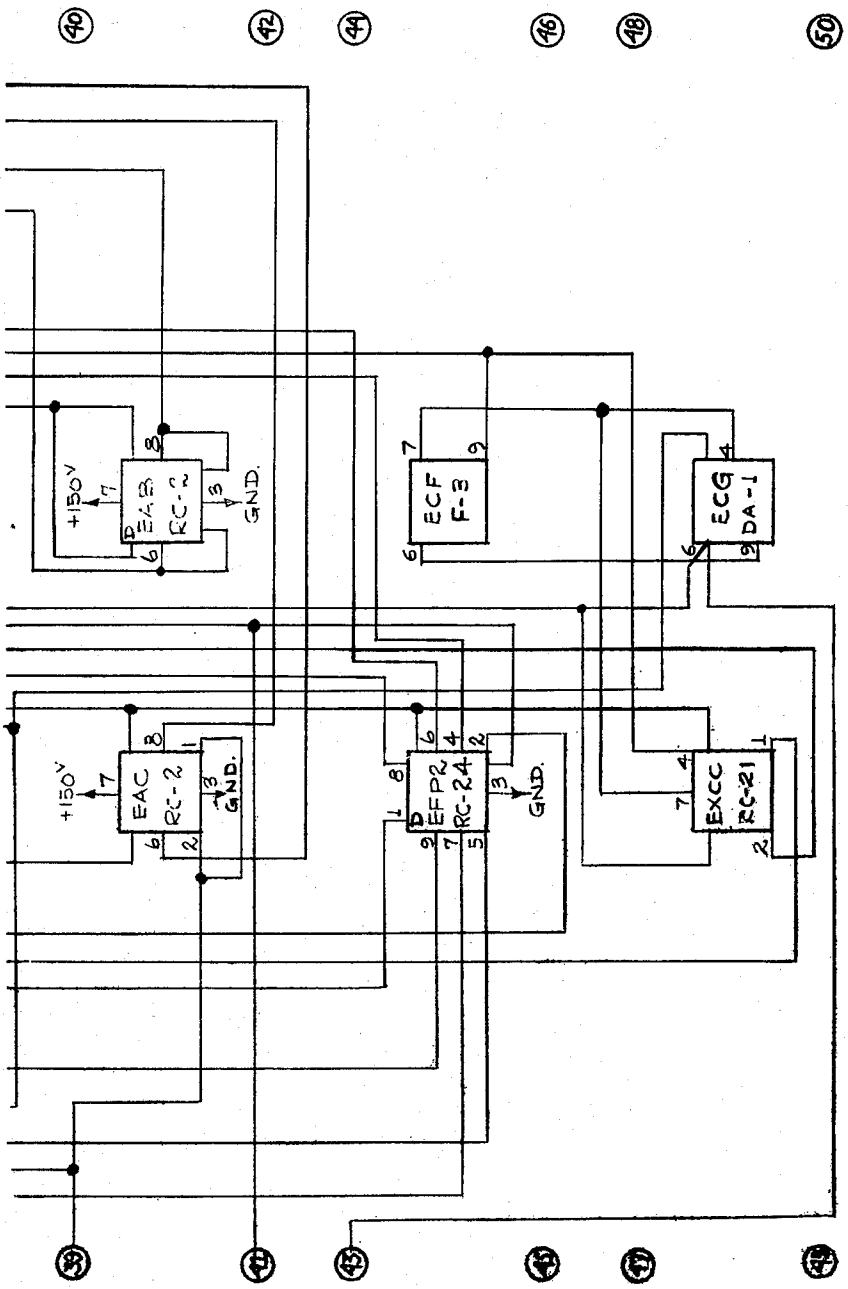


INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 52

FIG. 24d



INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 53

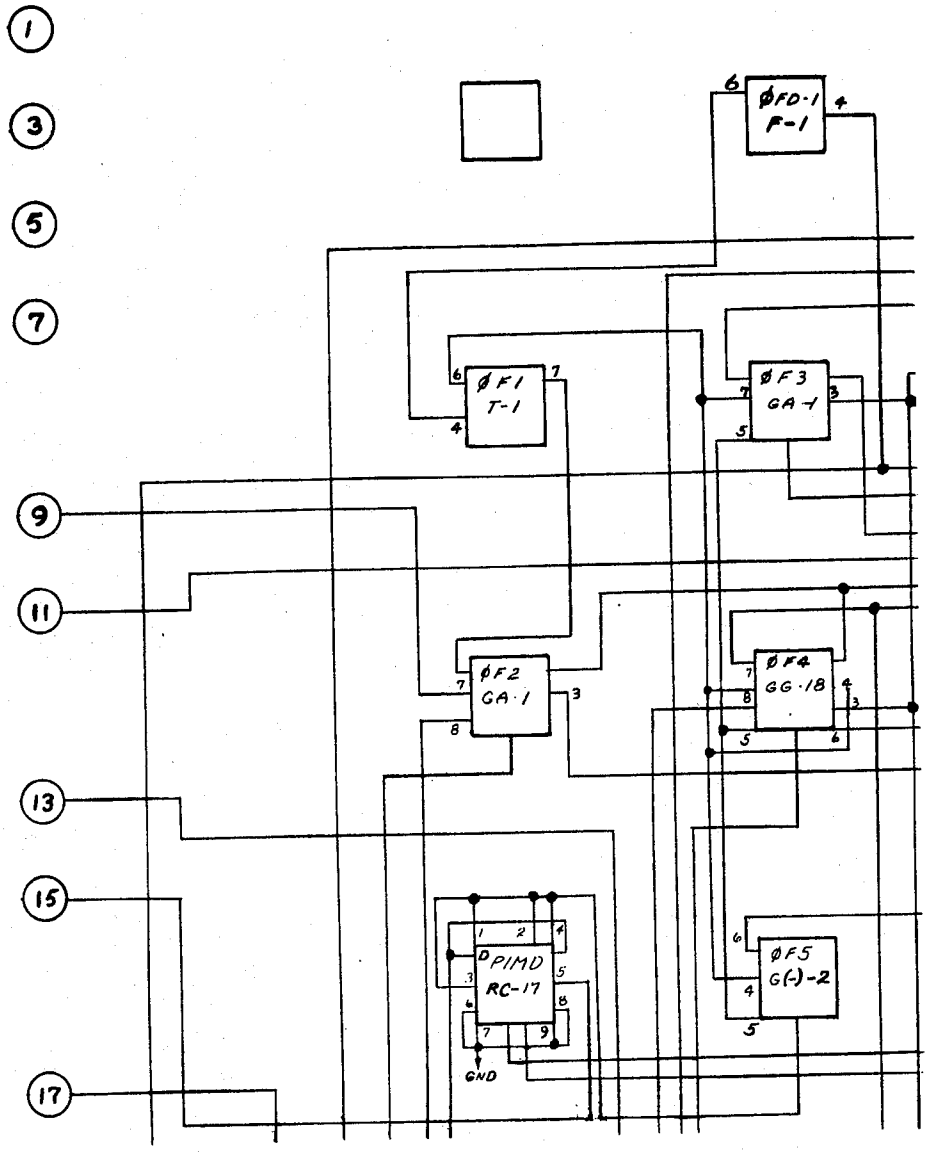


FIG. 25a

FIG. 25a	FIG. 25b
FIG. 25c	FIG. 25d
FIG. 25e	FIG. 25f

FIG. 25g

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 54

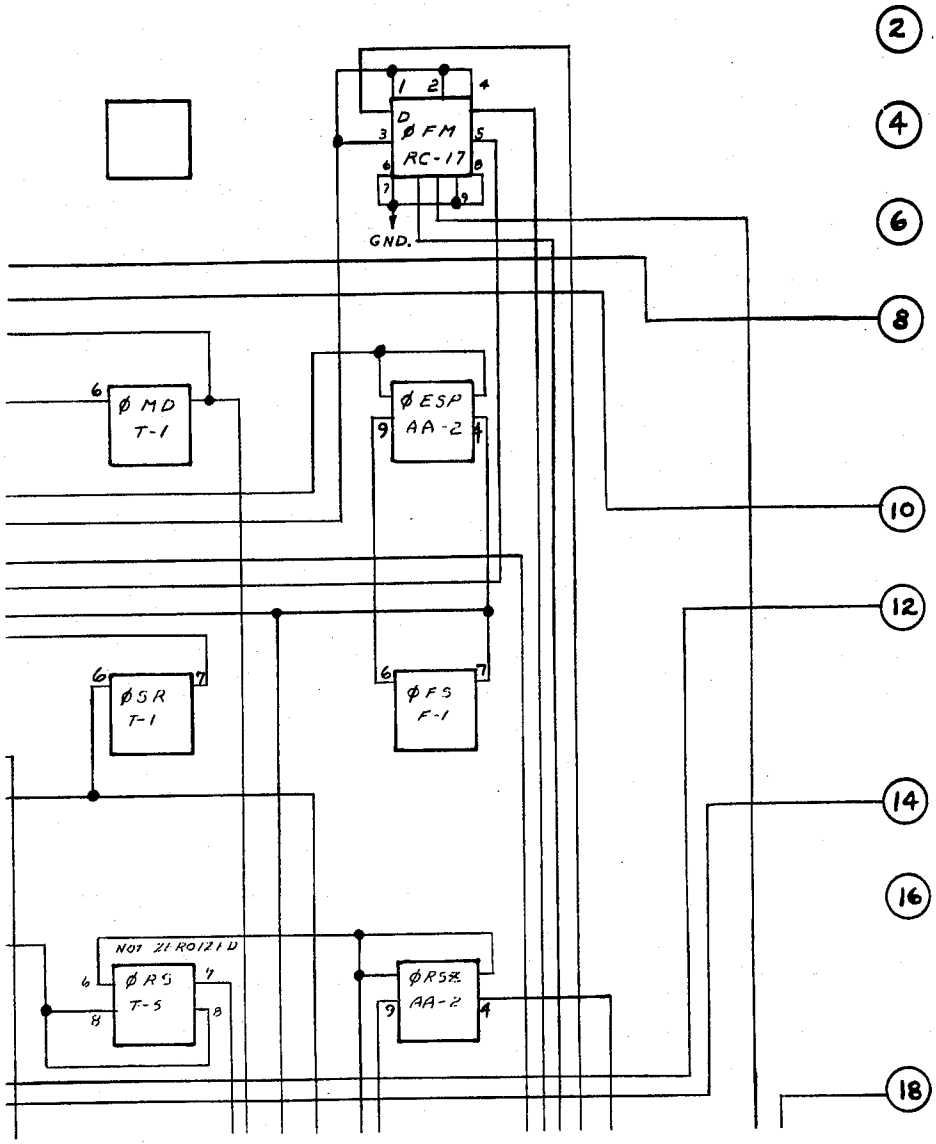


FIG. 25B

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 55

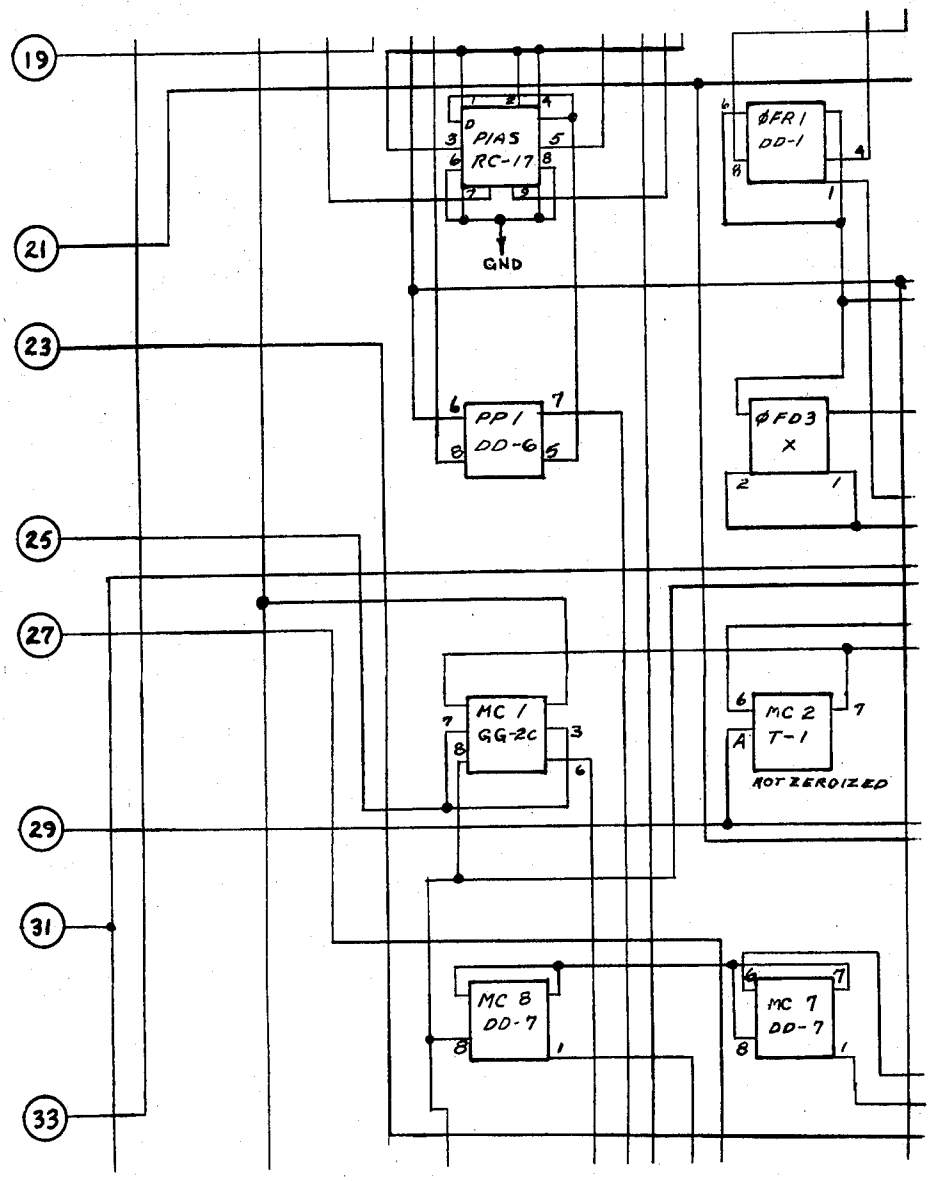


FIG. 25c

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 56

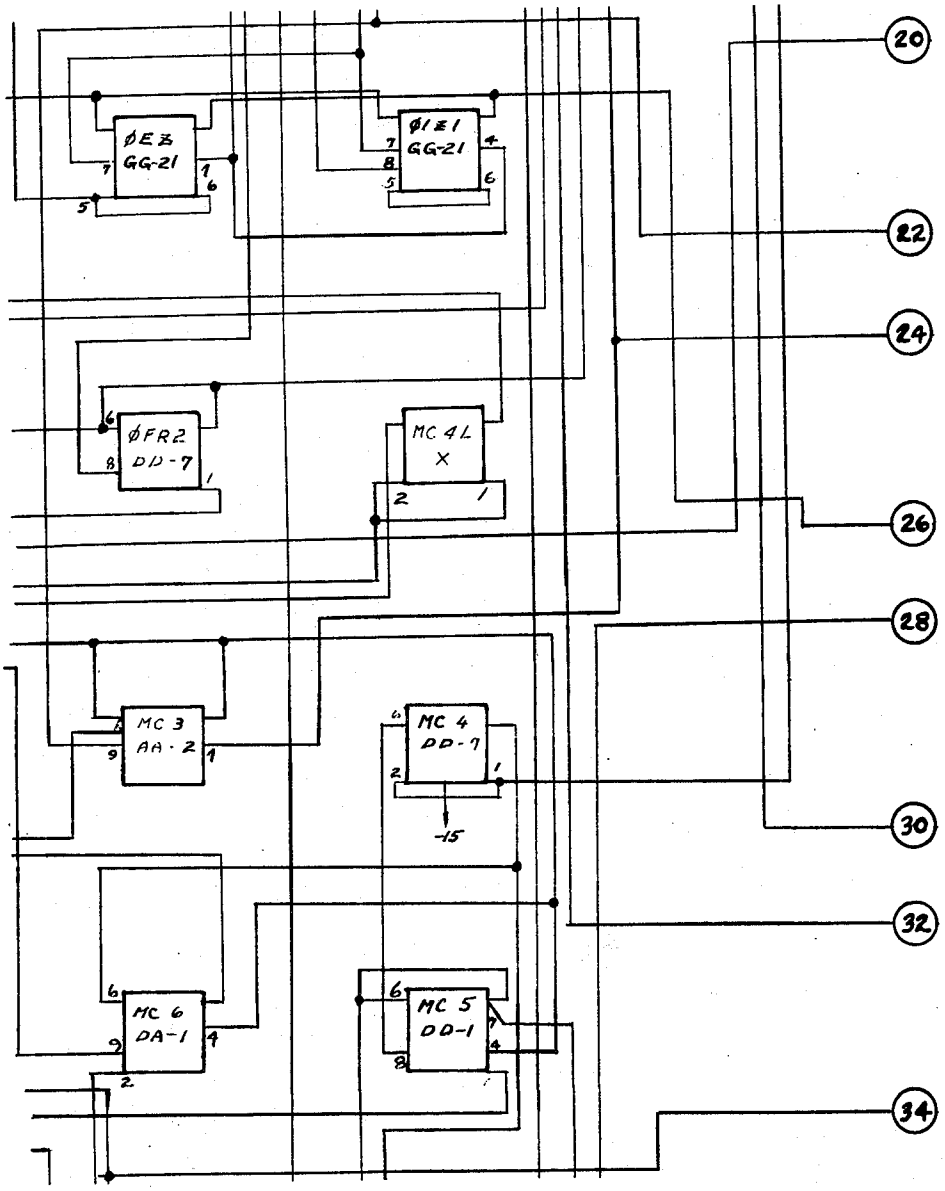


FIG. 25d

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

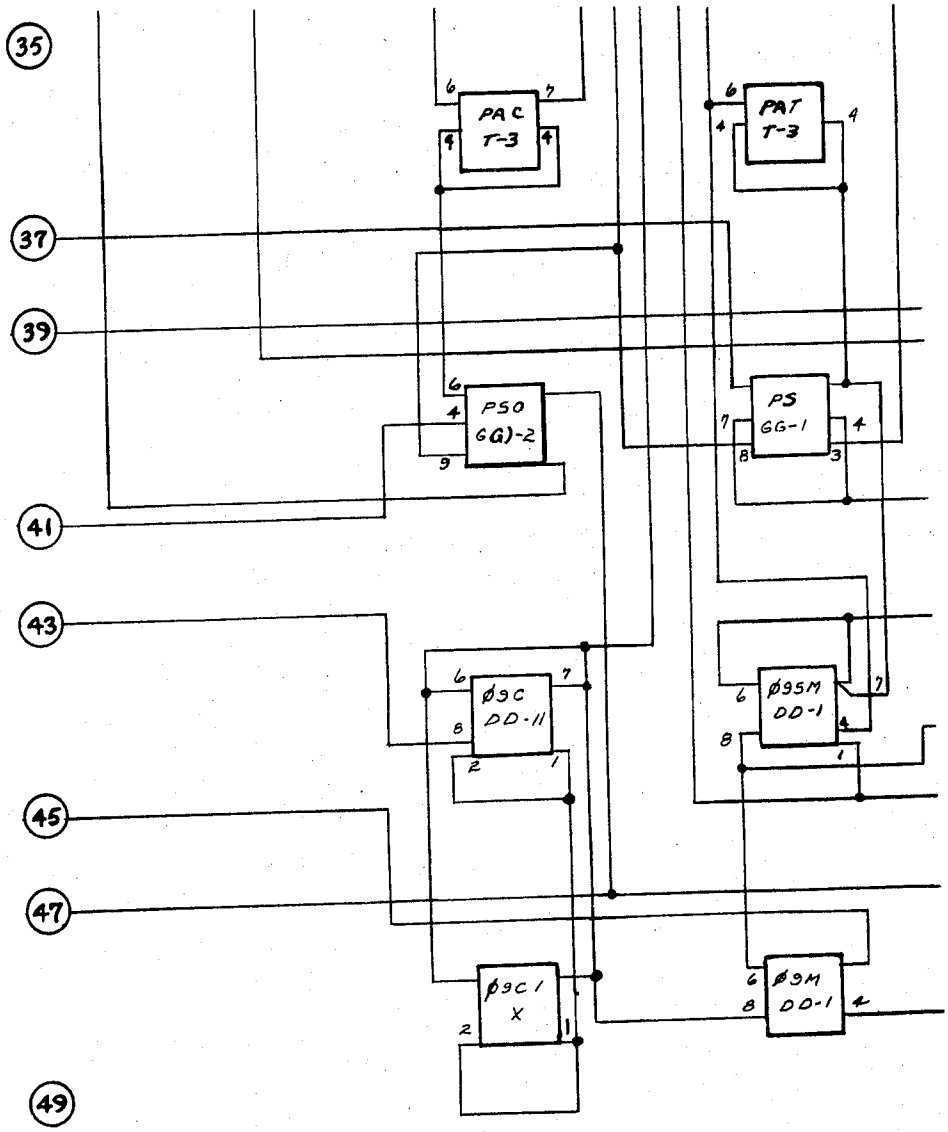


FIG. 25e

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

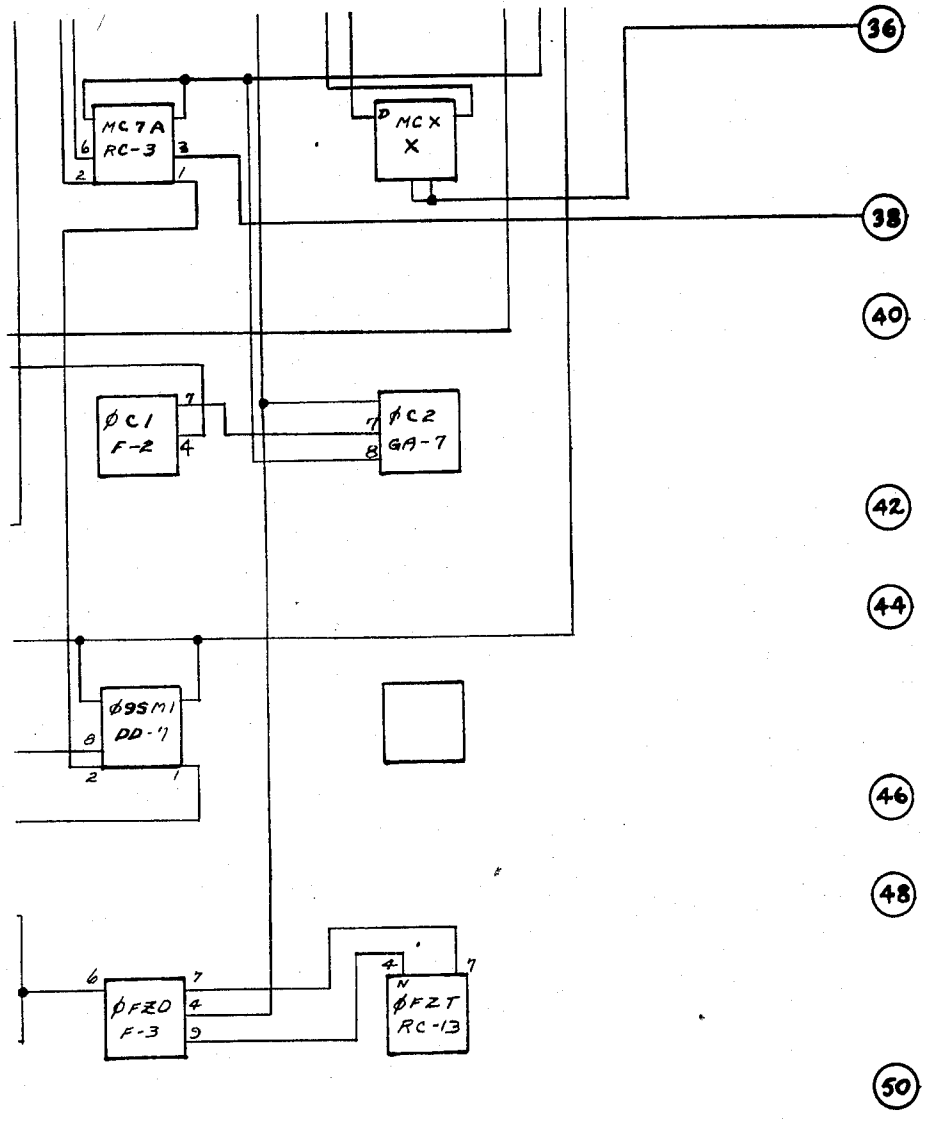


FIG. 25f

INVENTOR
LORING P. CROSMAN
BY George V. Fitzpatrick
ATTORNEY

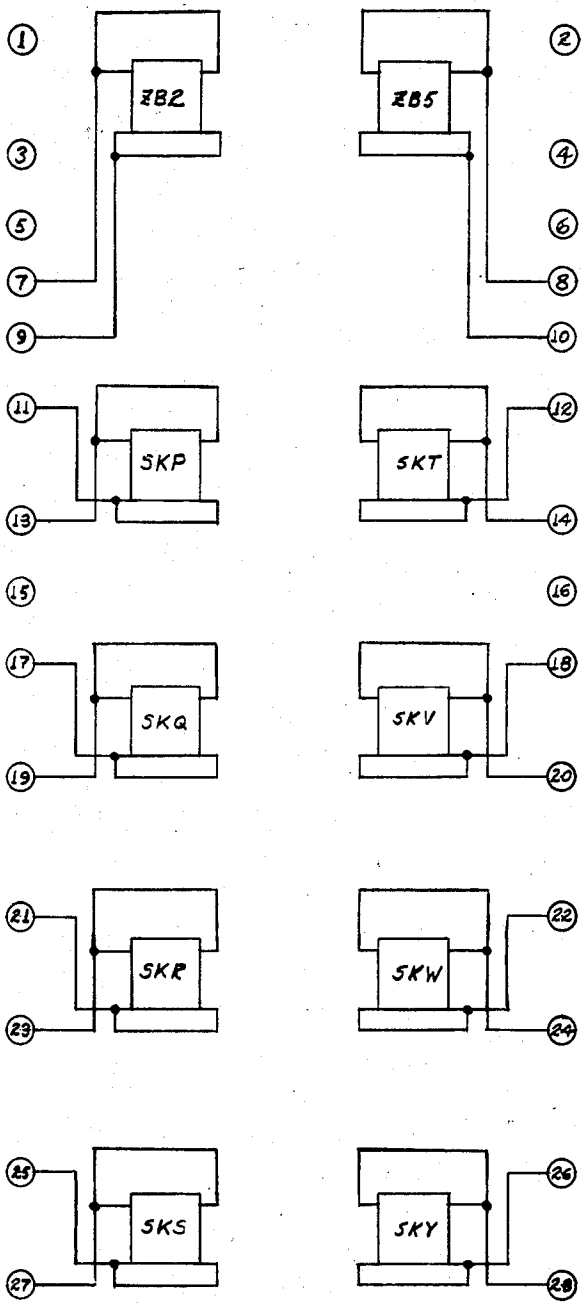


FIG. 26

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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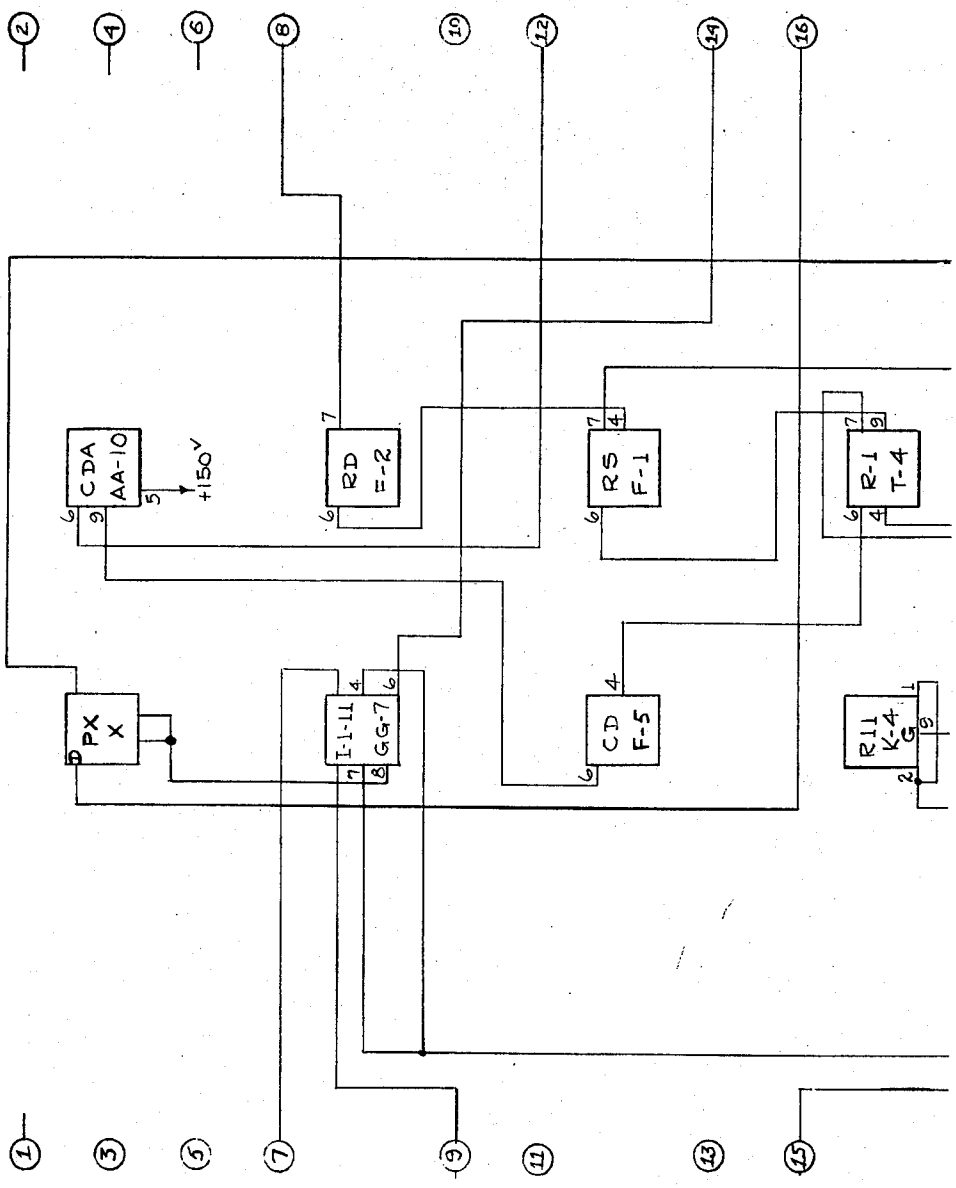


FIG. 27a

FIG. 27a

FIG. 27a	FIG. 27a	FIG. 27c	FIG. 27d

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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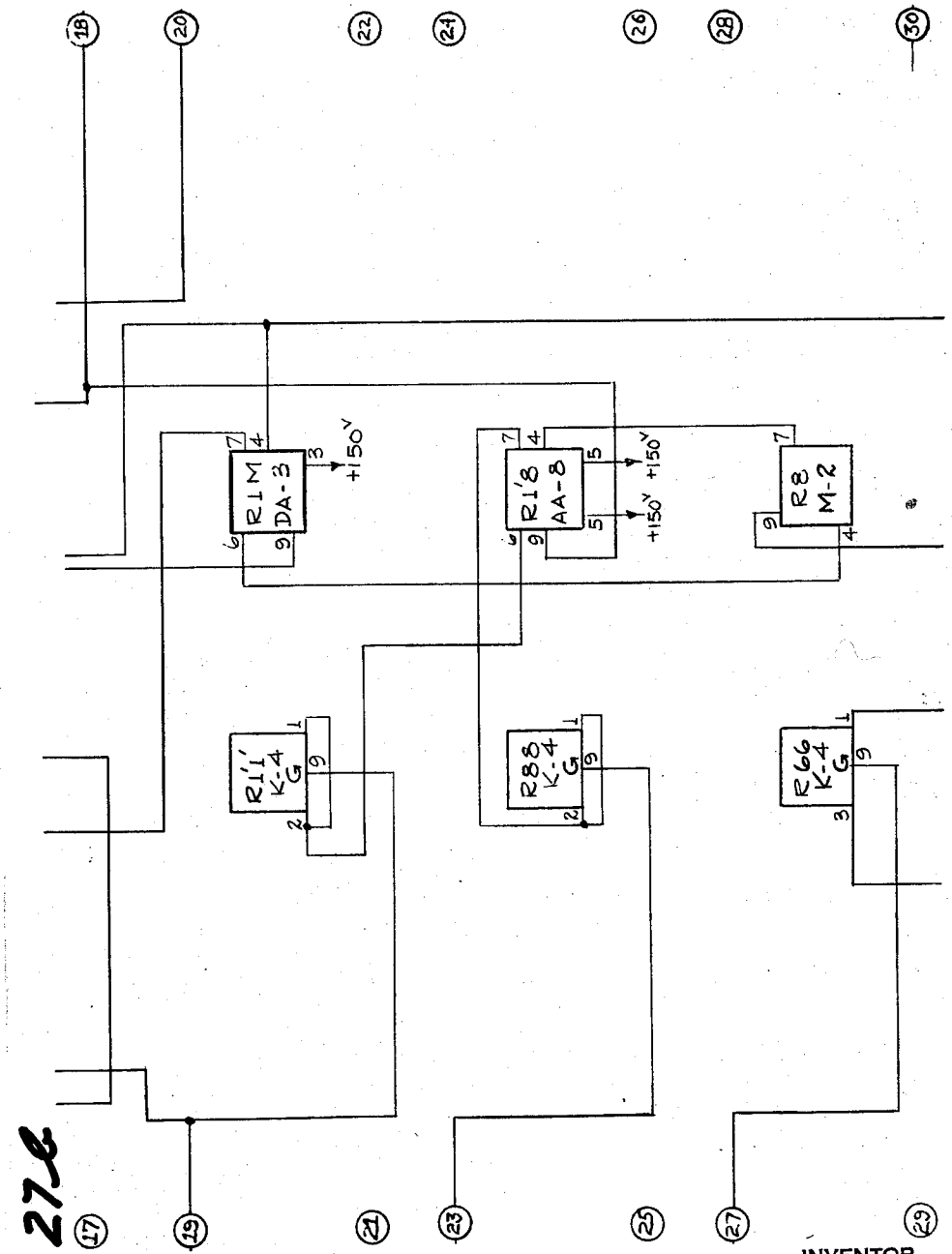


FIG. 27A

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

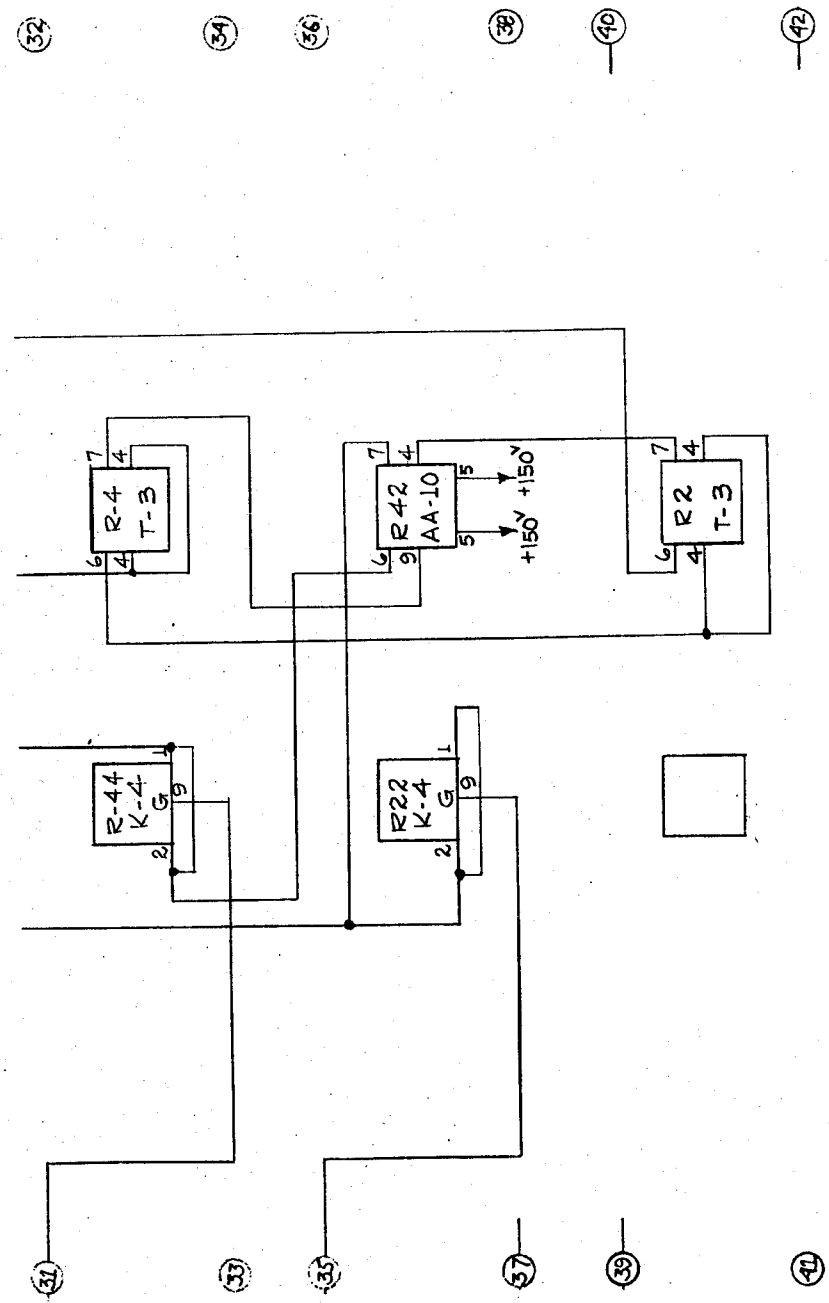


FIG. 27c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

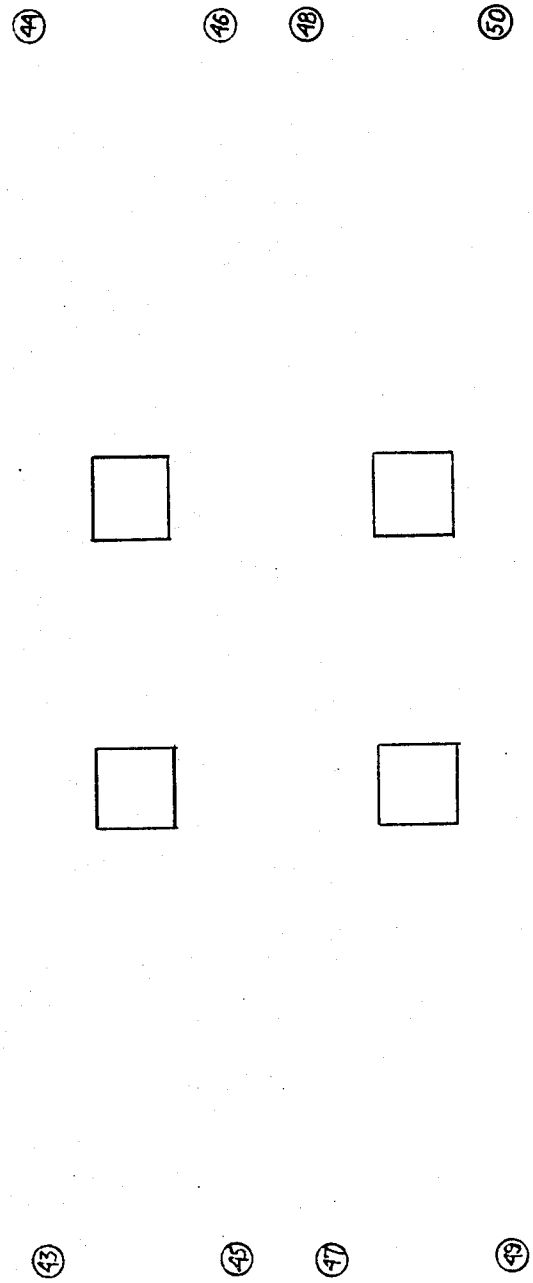


FIG. 27Z

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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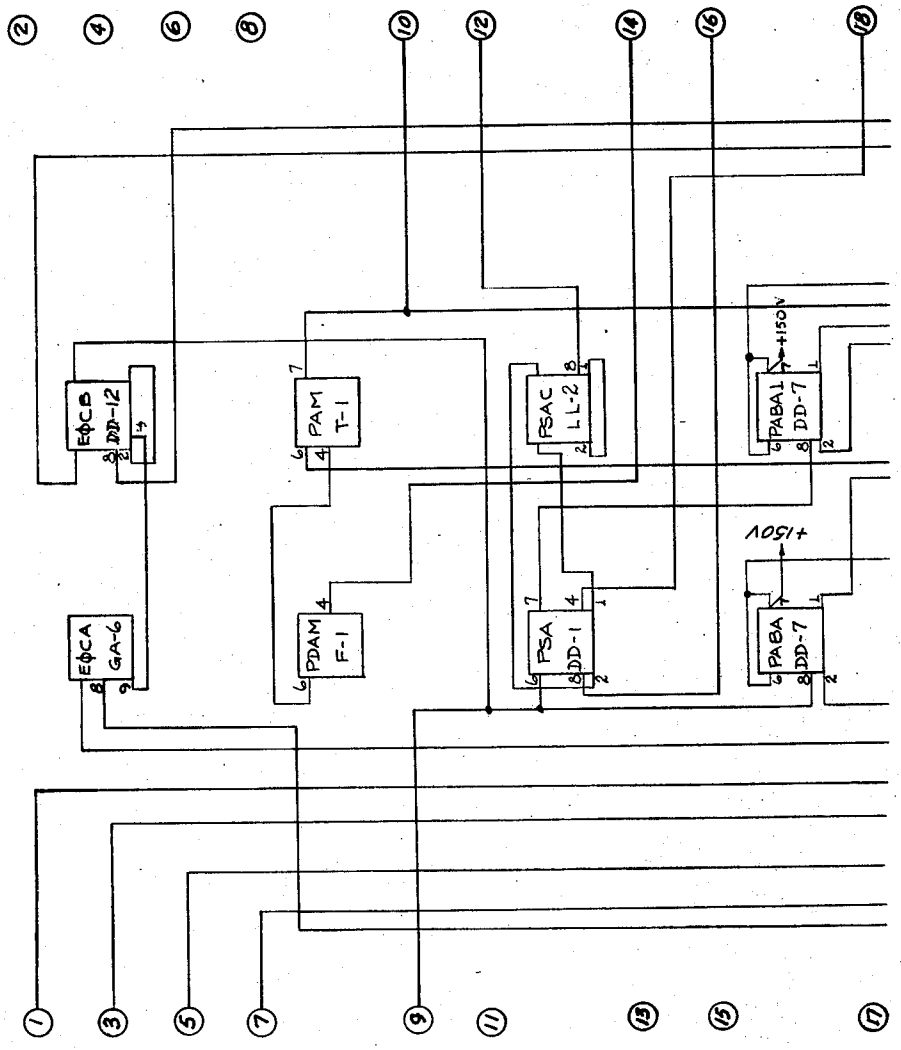


FIG. 28d

FIG. 28a	FIG. 28b	FIG. 28c

FIG. 28a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 65

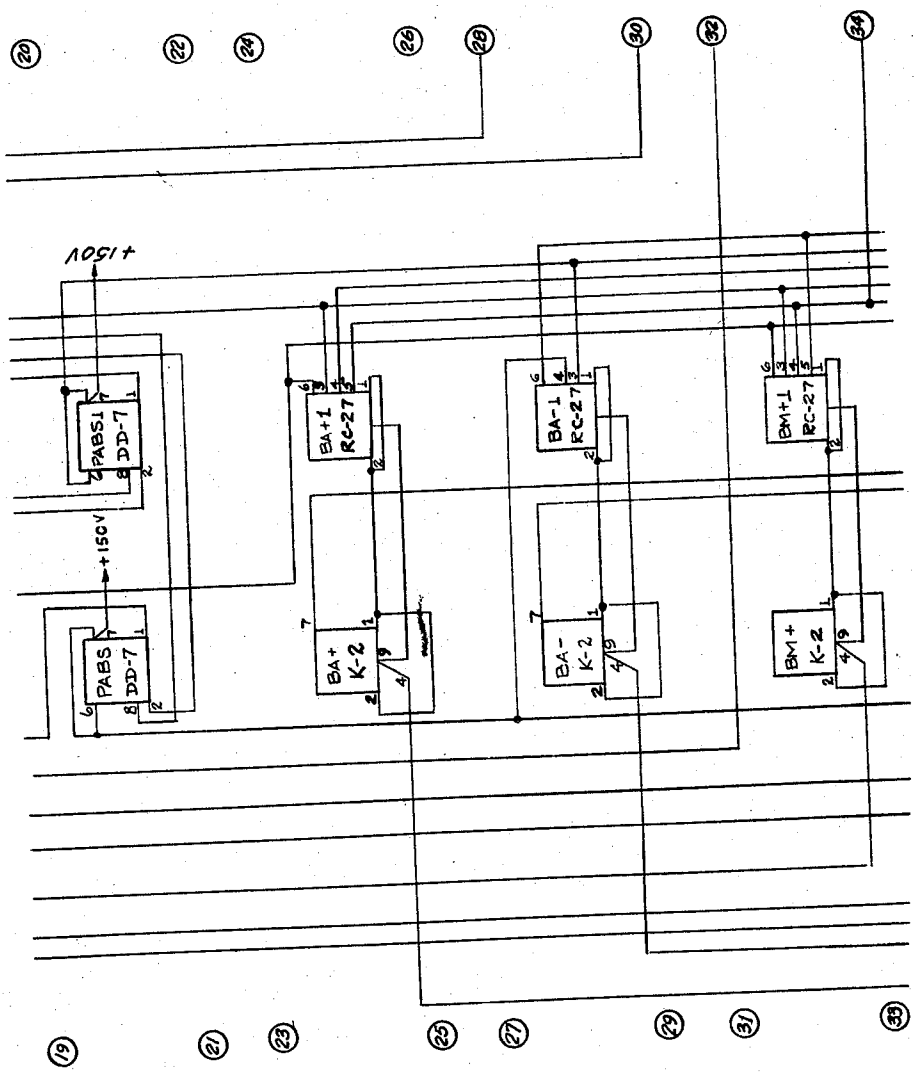


FIG. 28A

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

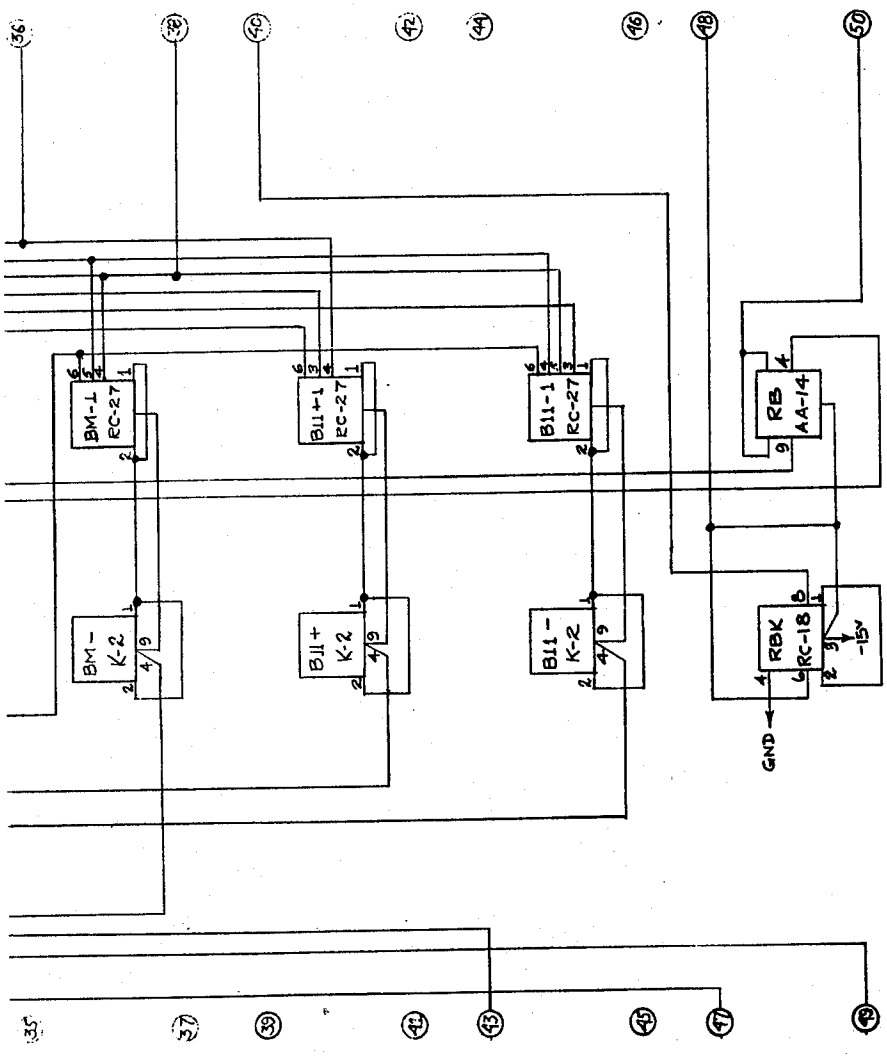


FIG. 28c

INVENTOR
LORING P. CROSMAN
BY George V. Ectgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 67

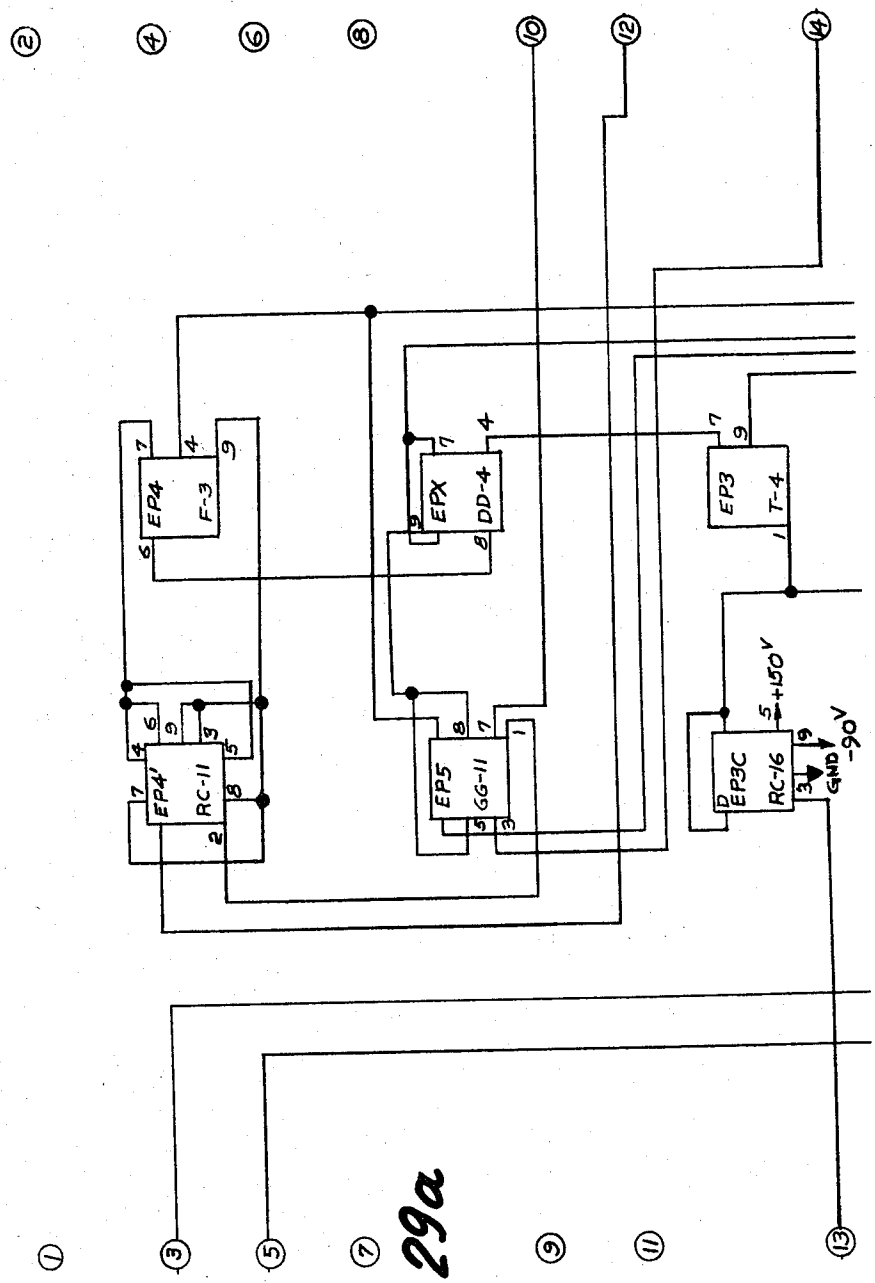


FIG. 29a

FIG. 29a | FIG. 29b | FIG. 29c | FIG. 29d

FIG. 29

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 68

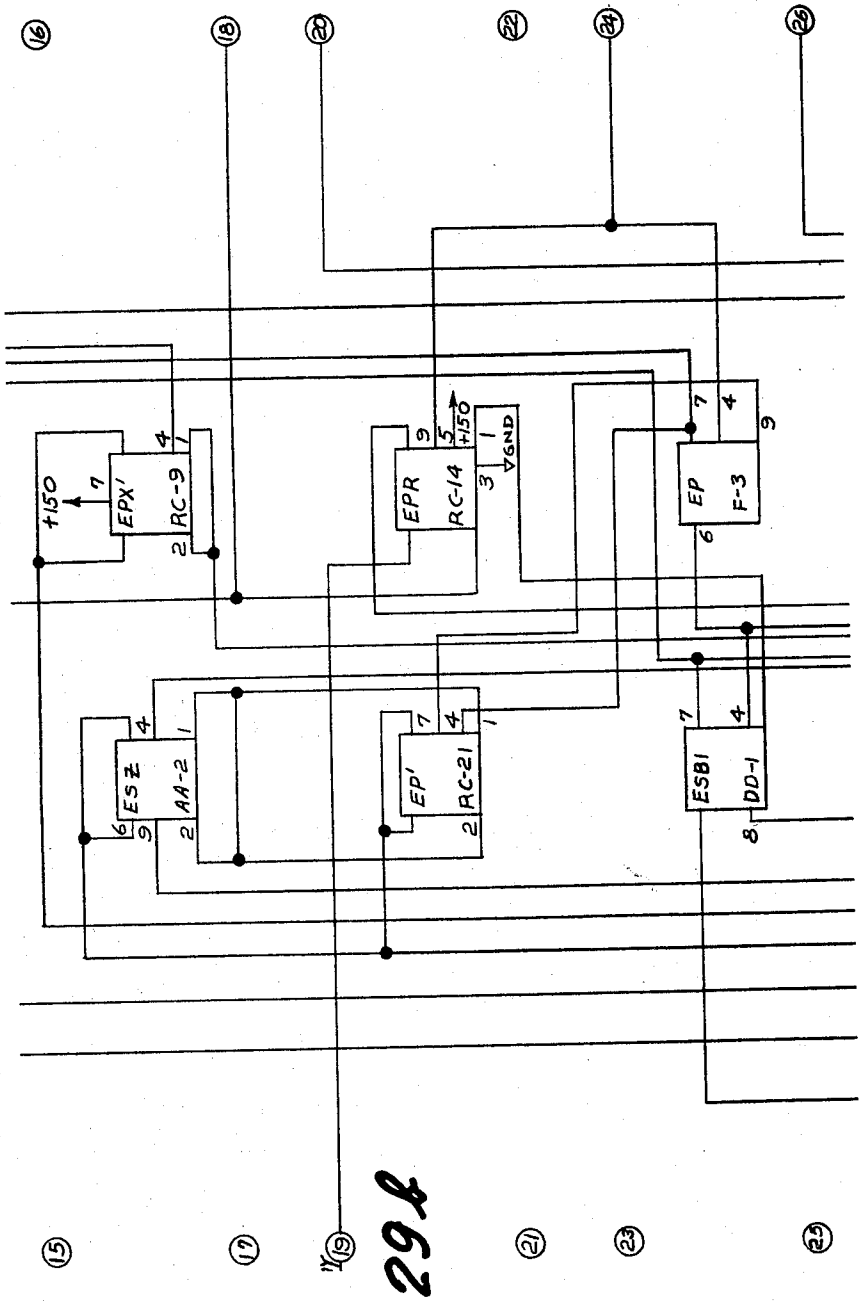


FIG. 29A

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 69

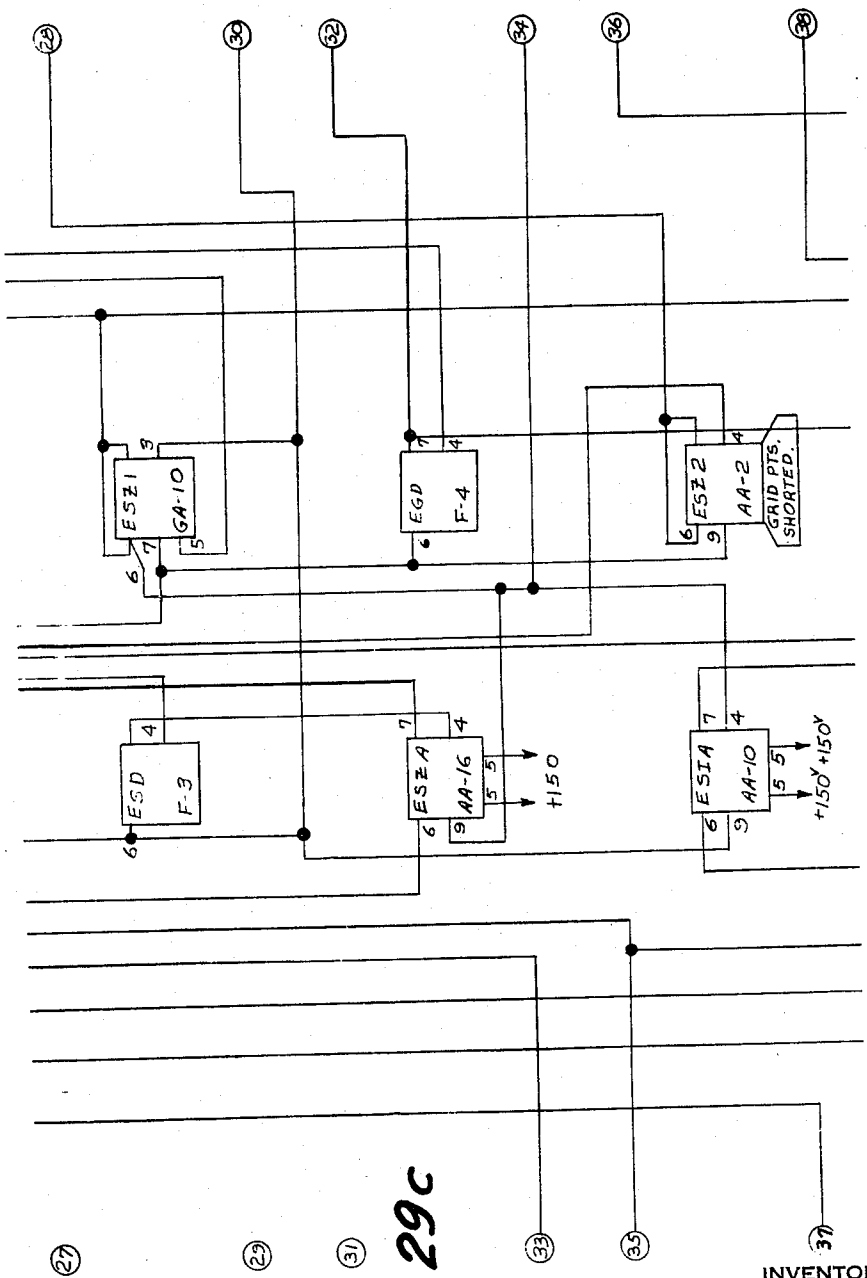


FIG. 29c

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 70

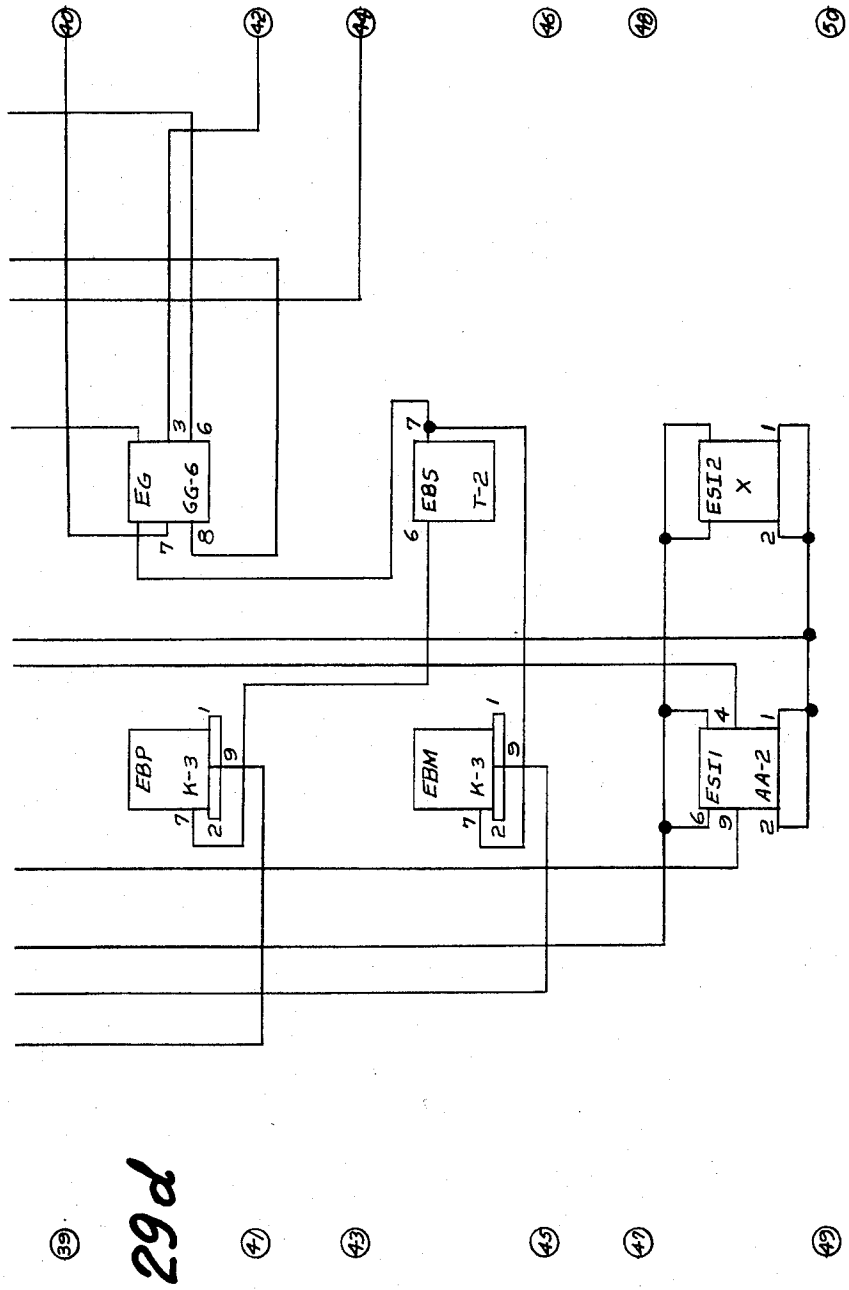


FIG. 29d

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 71

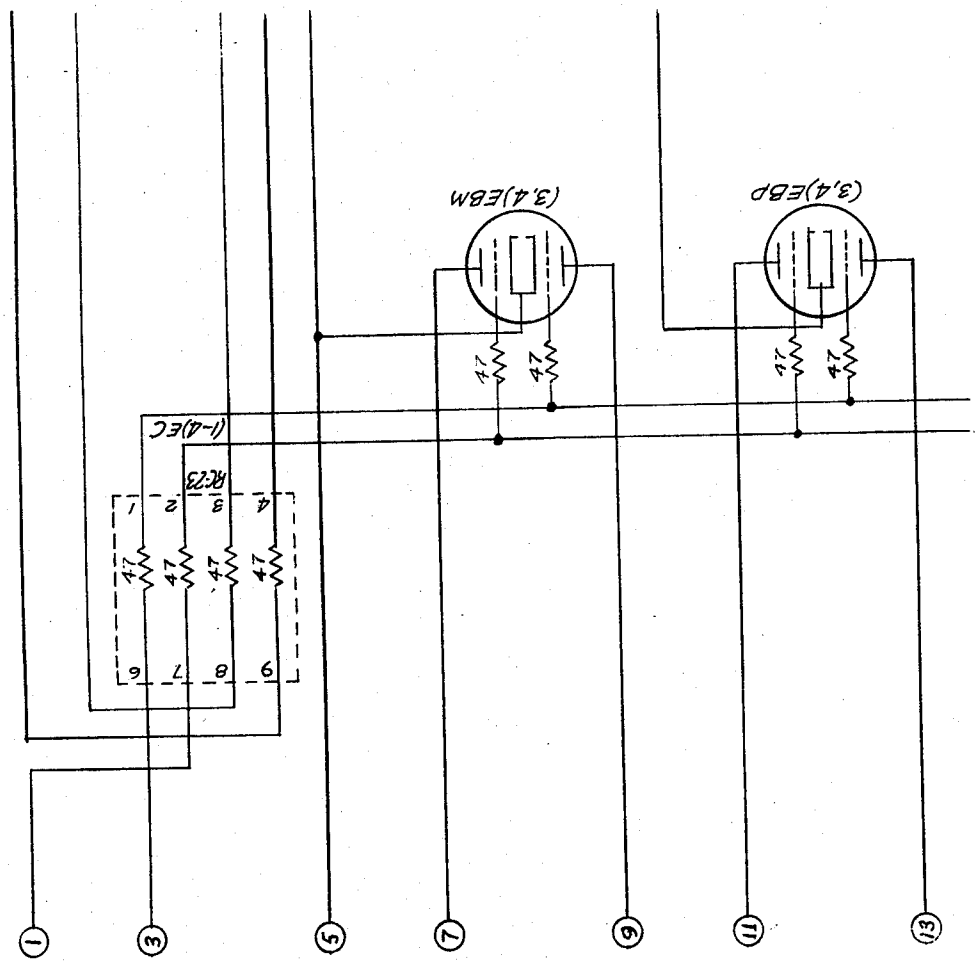


FIG. 30a

FIG. 30g

FIG. 30a	FIG. 30c	FIG. 30e
FIG. 30b	FIG. 30d	FIG. 30f

INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 72

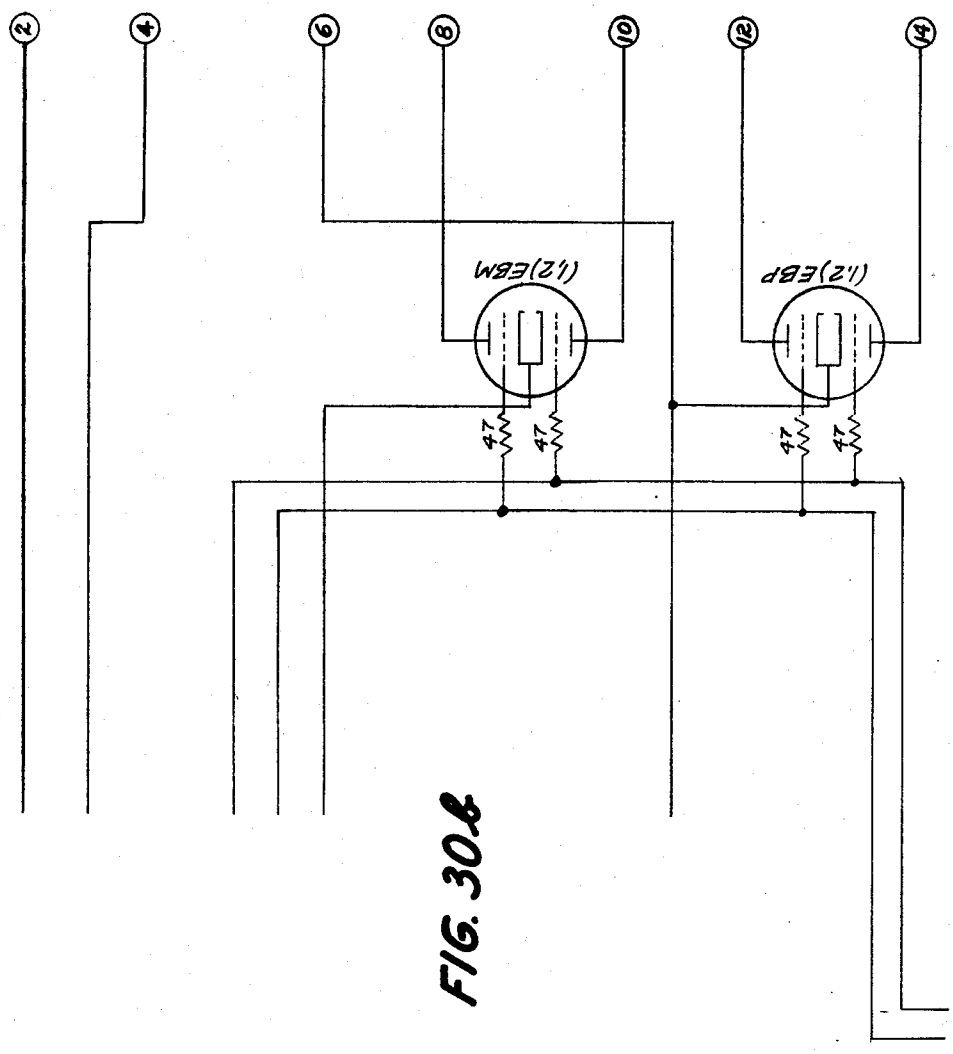


FIG. 30A

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 73

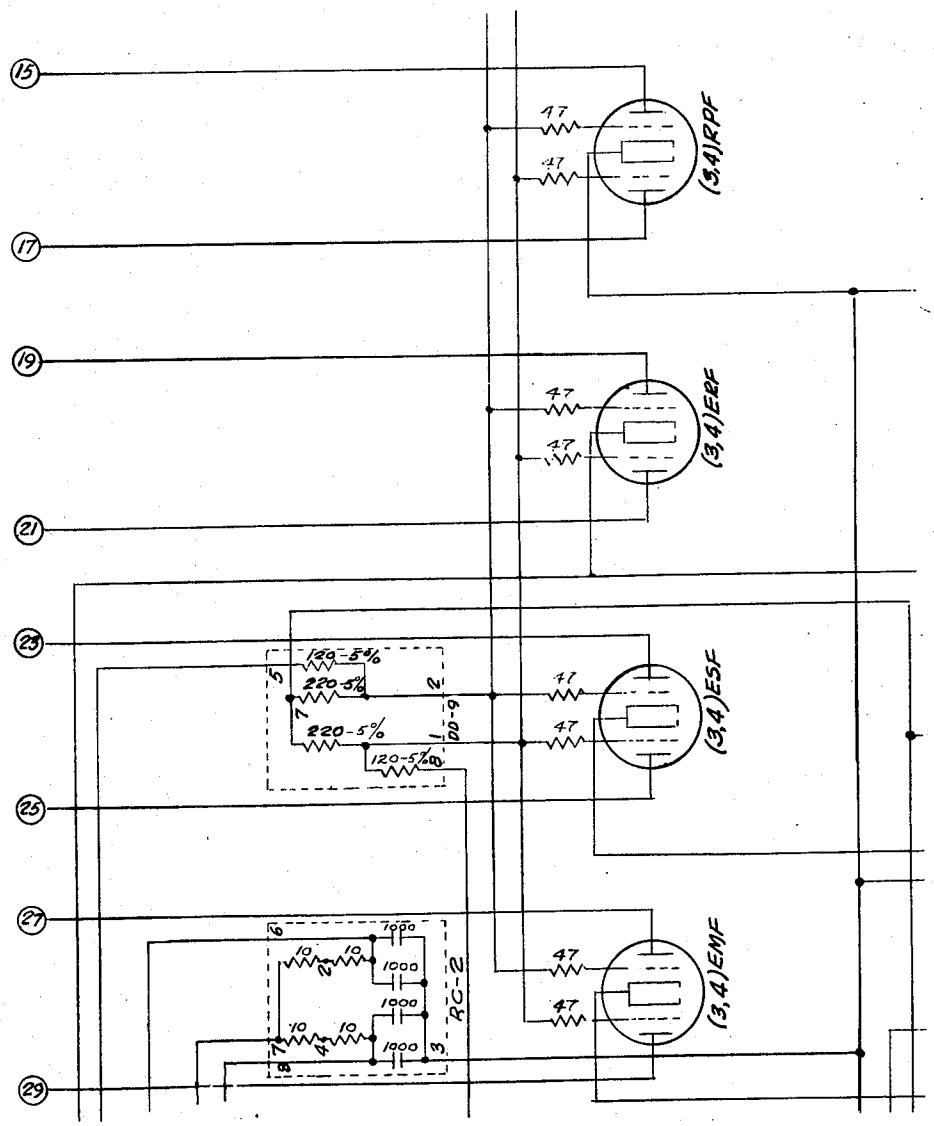


FIG. 30c

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

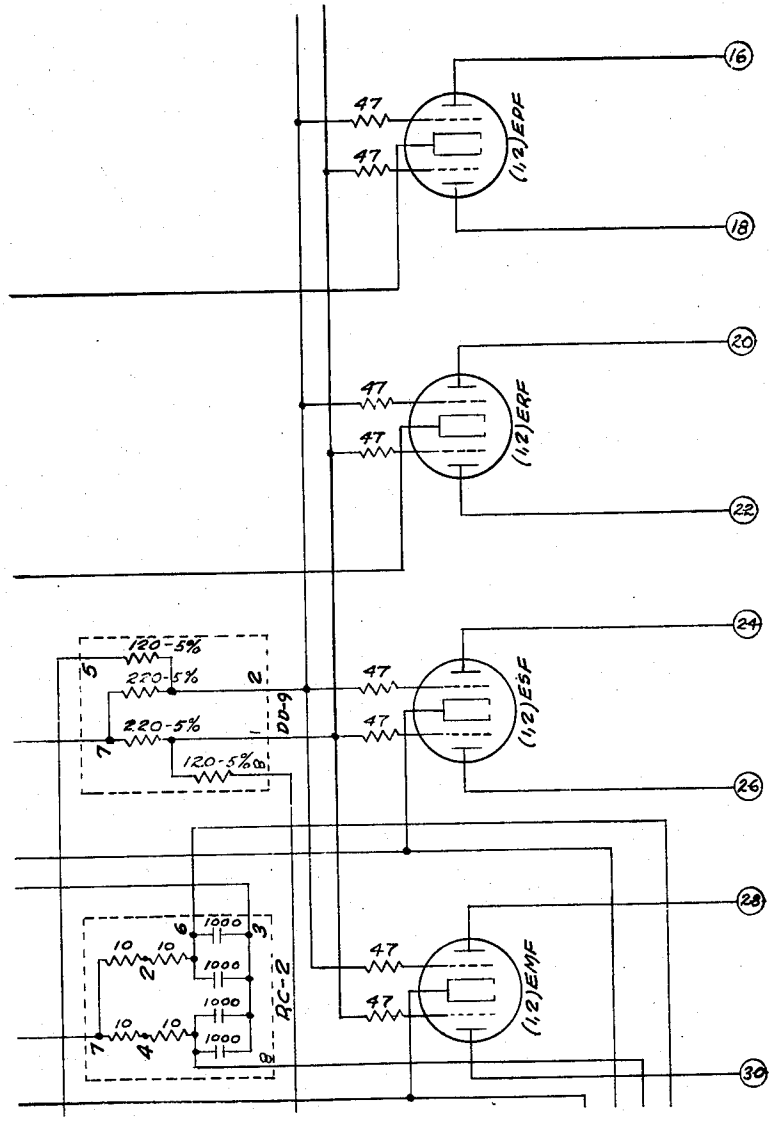


FIG. 30d

INVENTOR
LORING P. CROSMAN
BY George V. Fitzpatrick
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 75

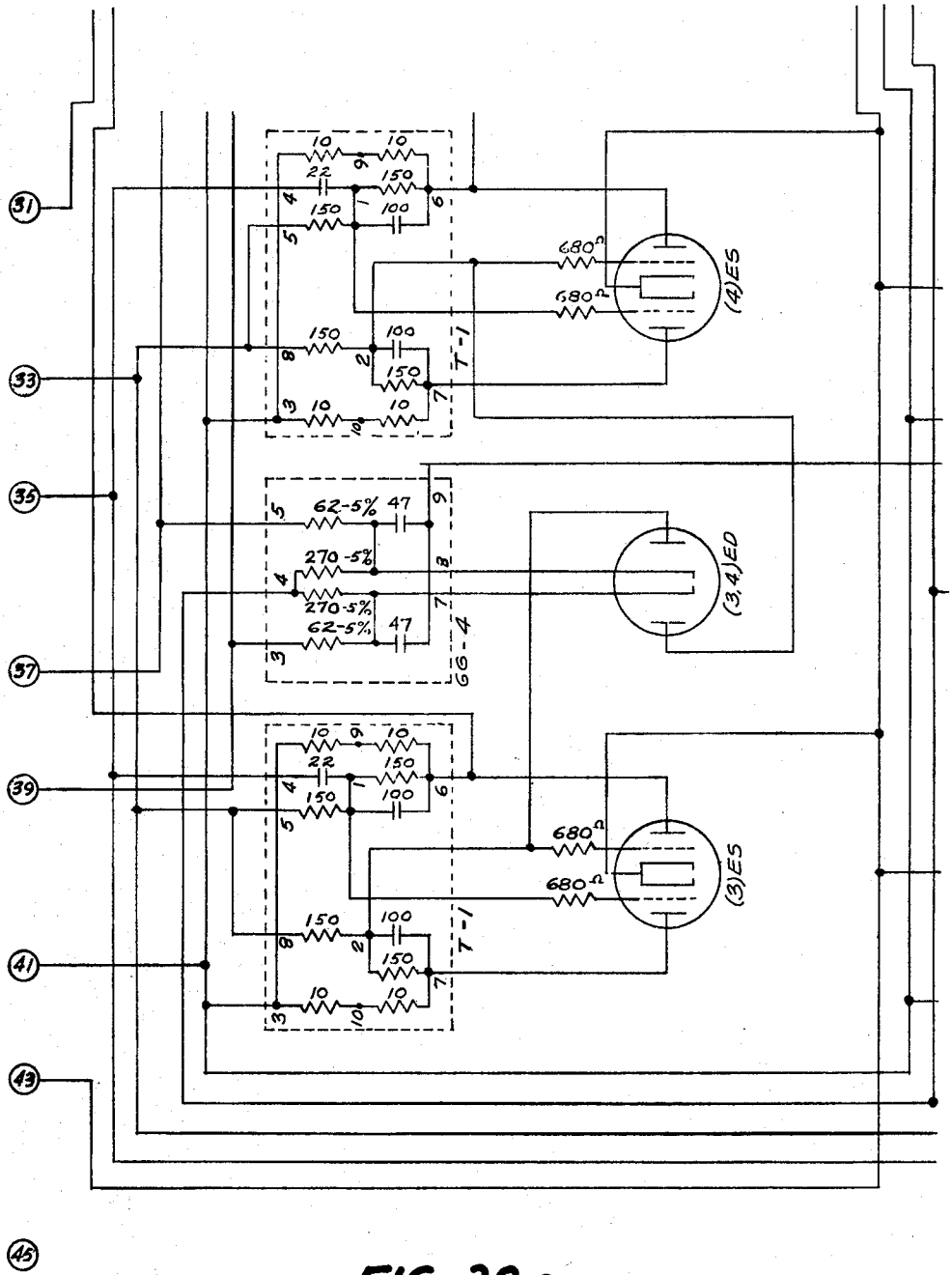


FIG. 30e

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 76

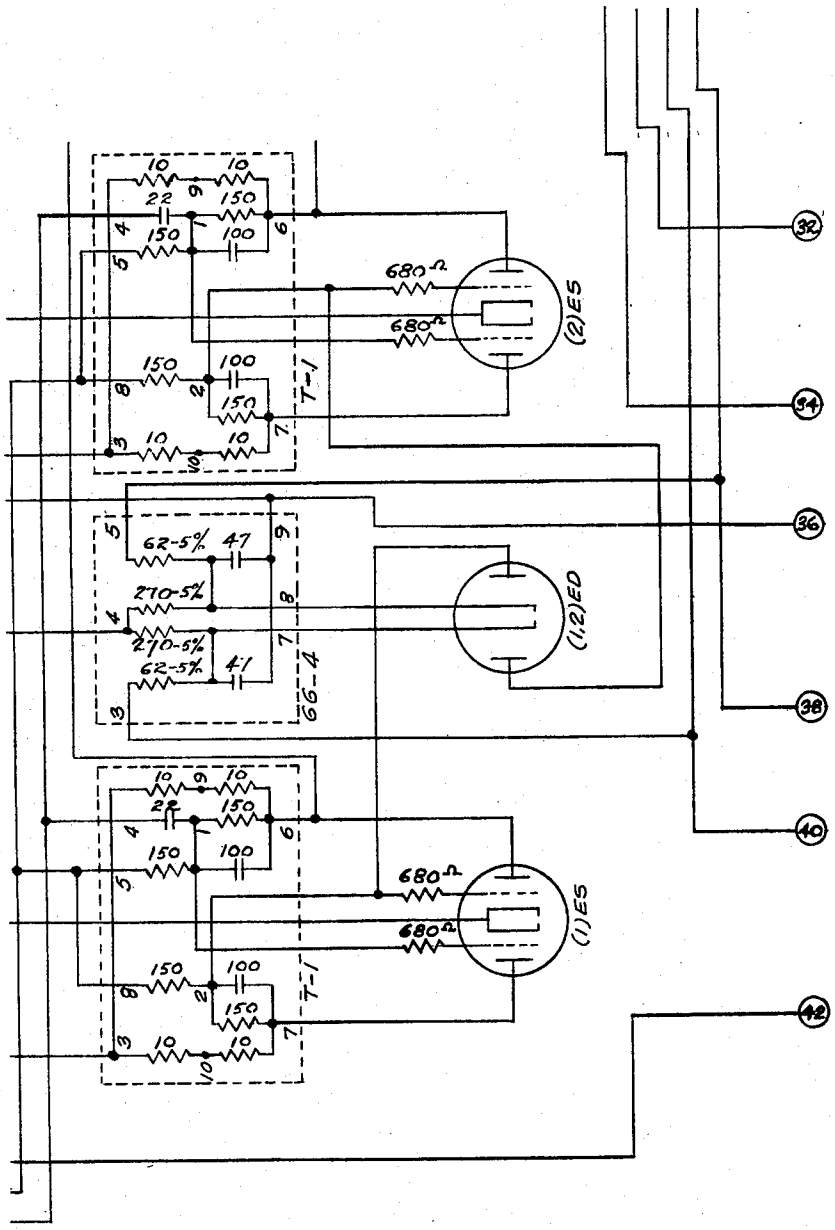


FIG. 30f

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 77

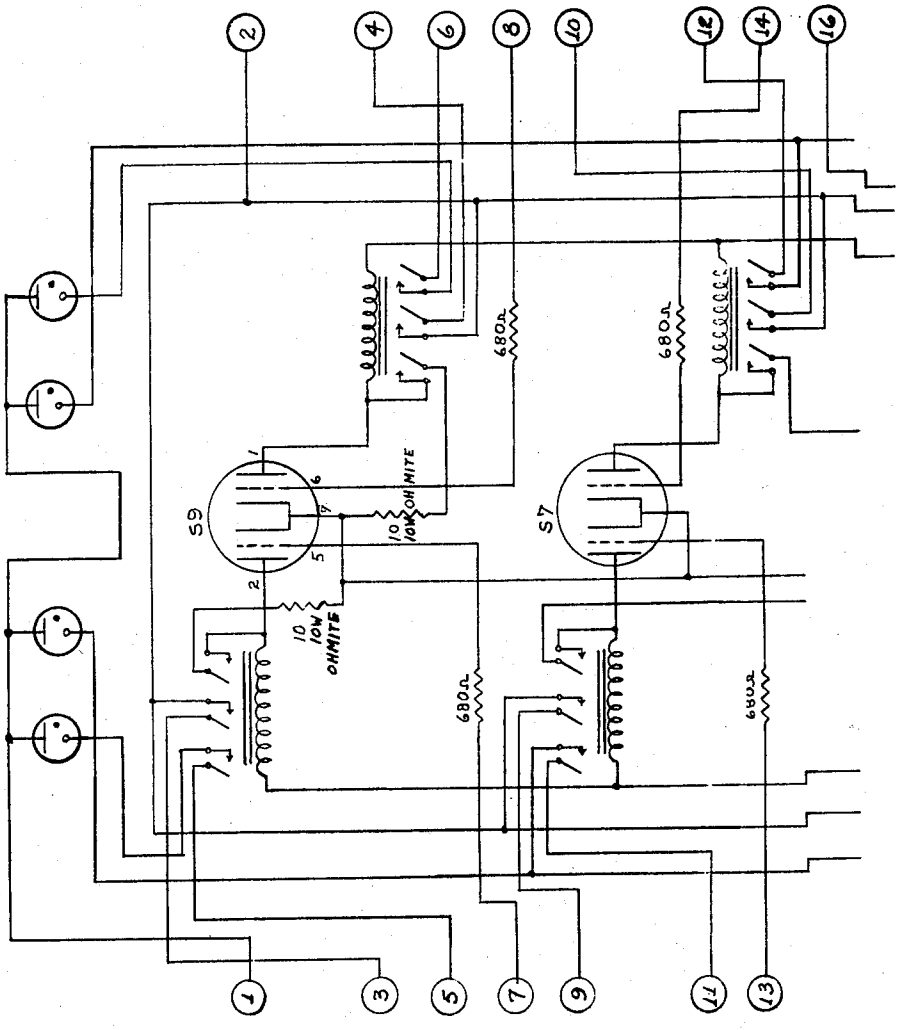


FIG. 31c

FIG. 31a	FIG. 31b

FIG. 31a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 78

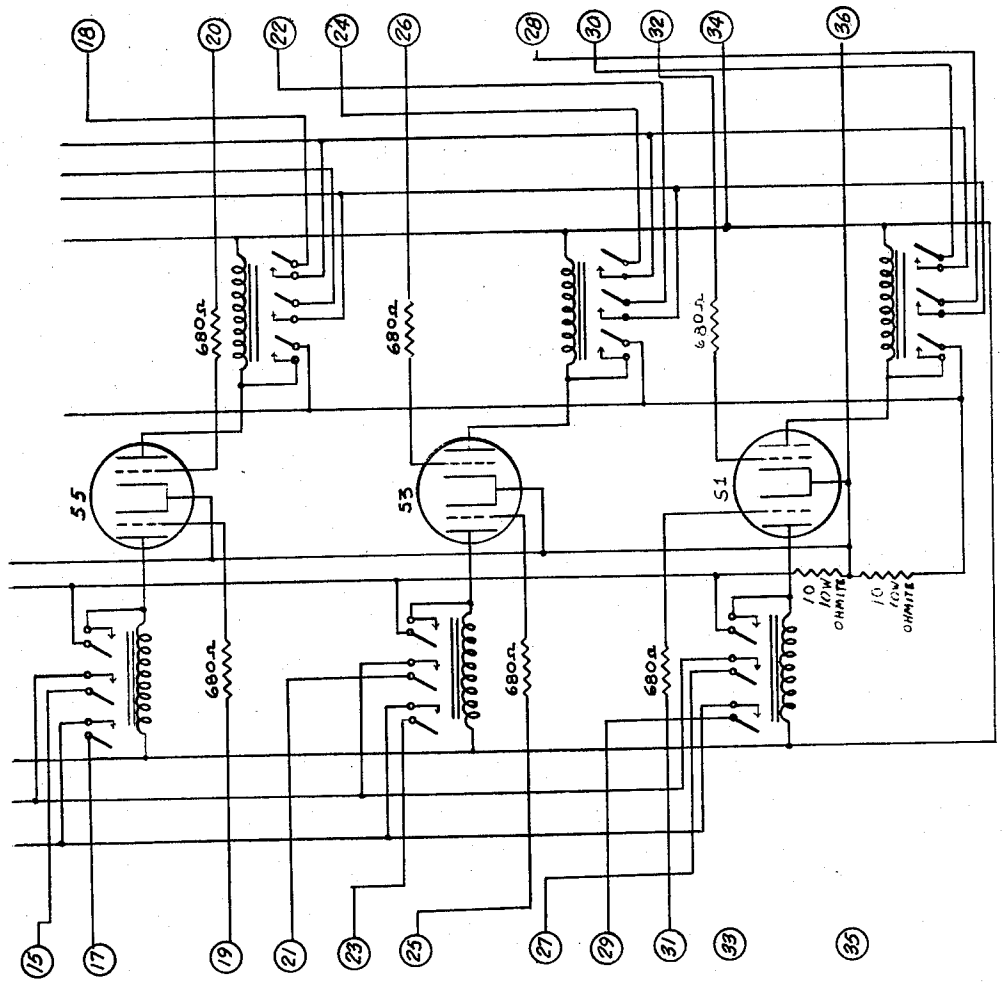


FIG. 314

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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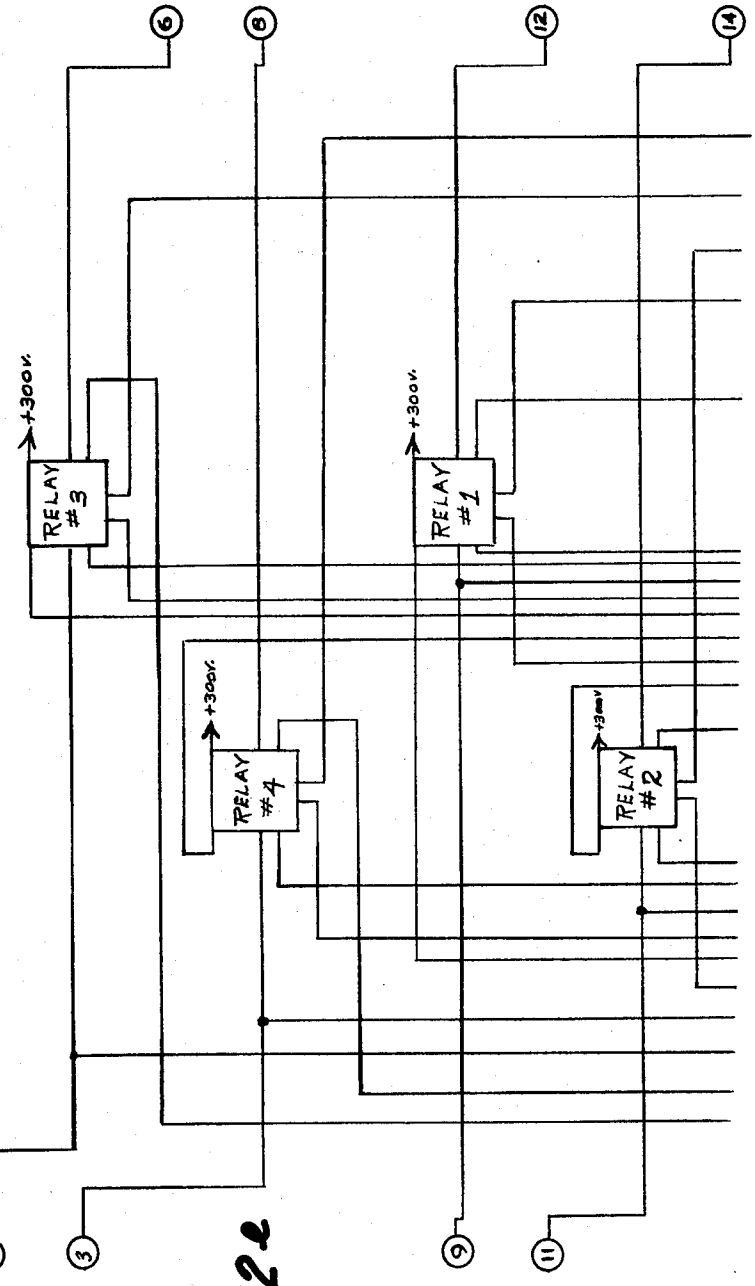


FIG. 32a

FIG. 32b

FIG. 32a	FIG. 32b	FIG. 32c	FIG. 32d

INVENTOR
LORING P. CROSMAN
BY George V. Ketzroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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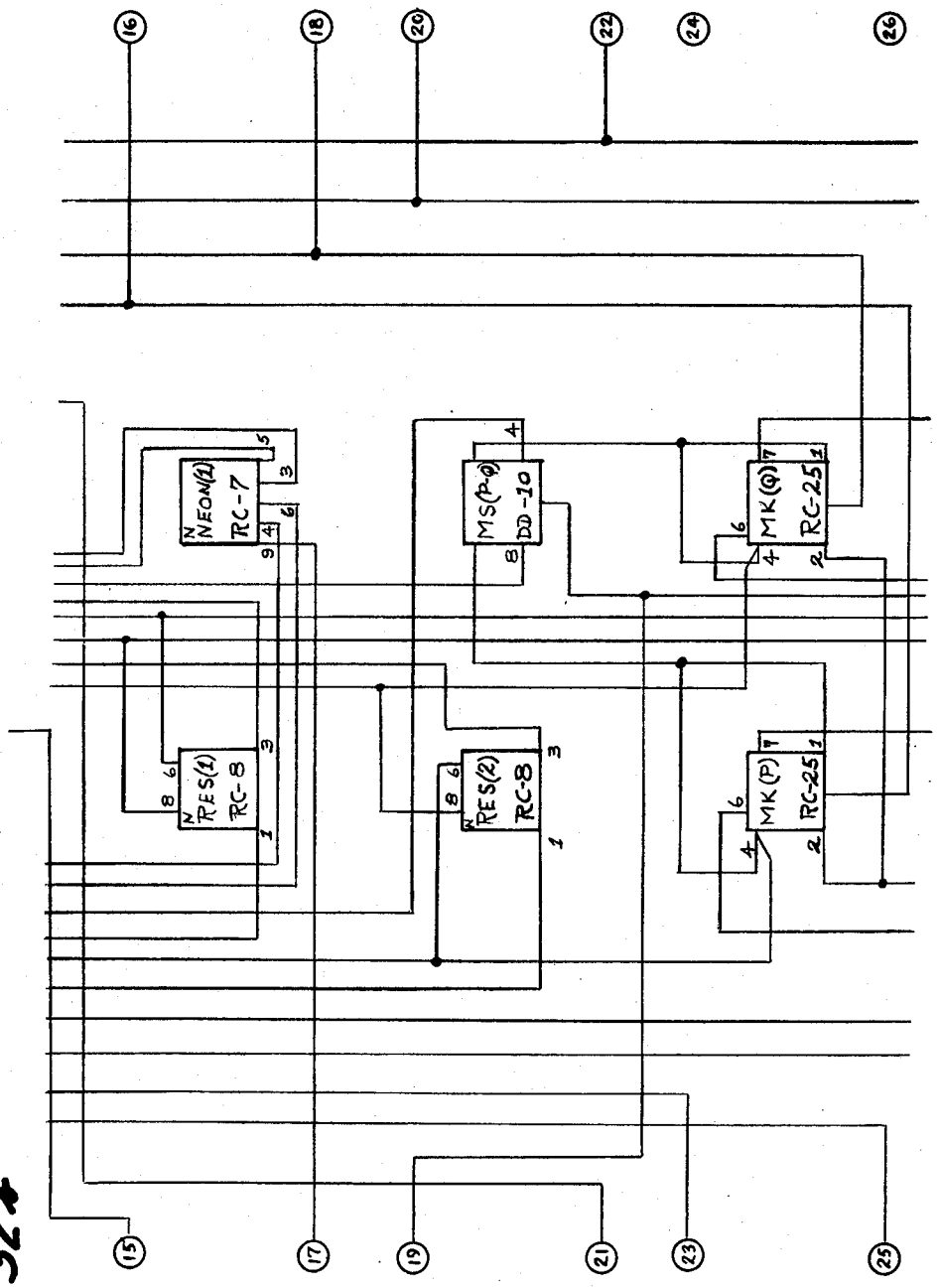


FIG. 32A

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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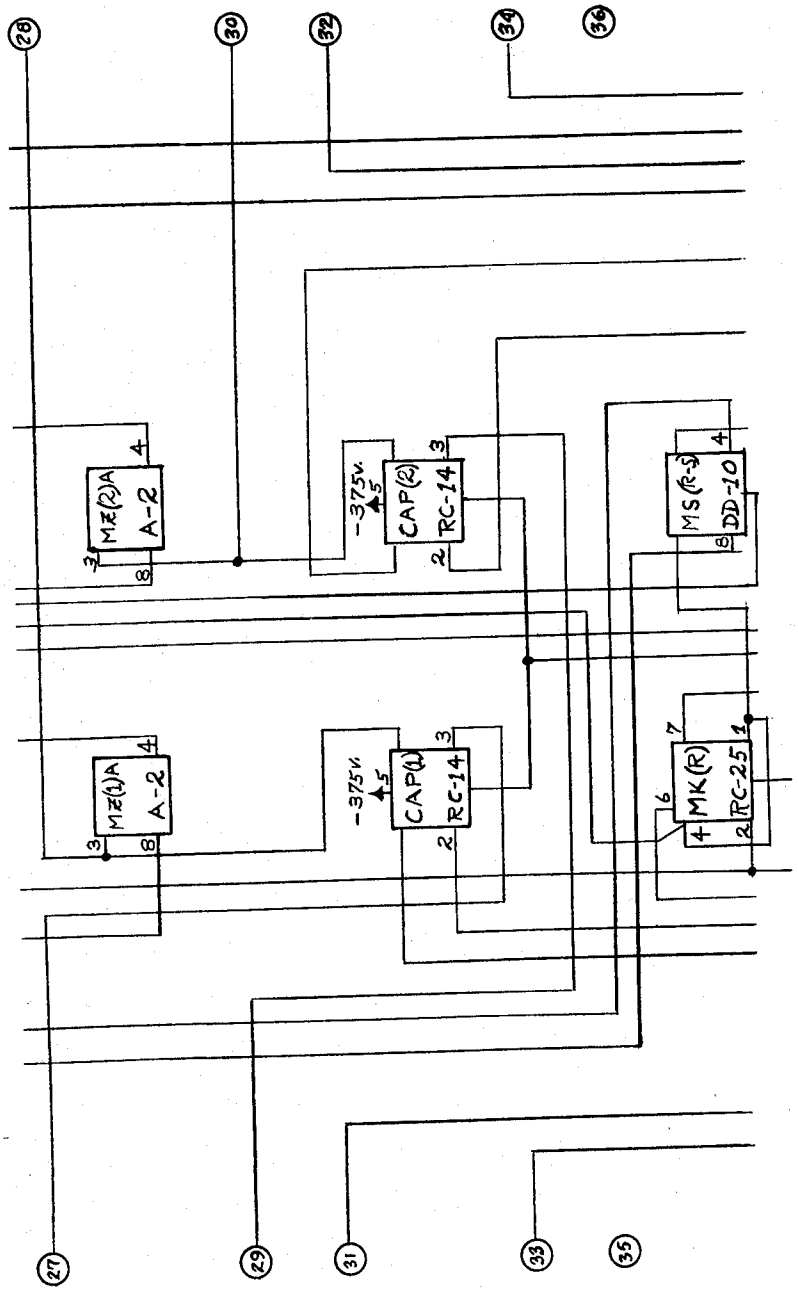


FIG. 32c

INVENTOR
LORING P. CROSMAN
BY George V. Eckroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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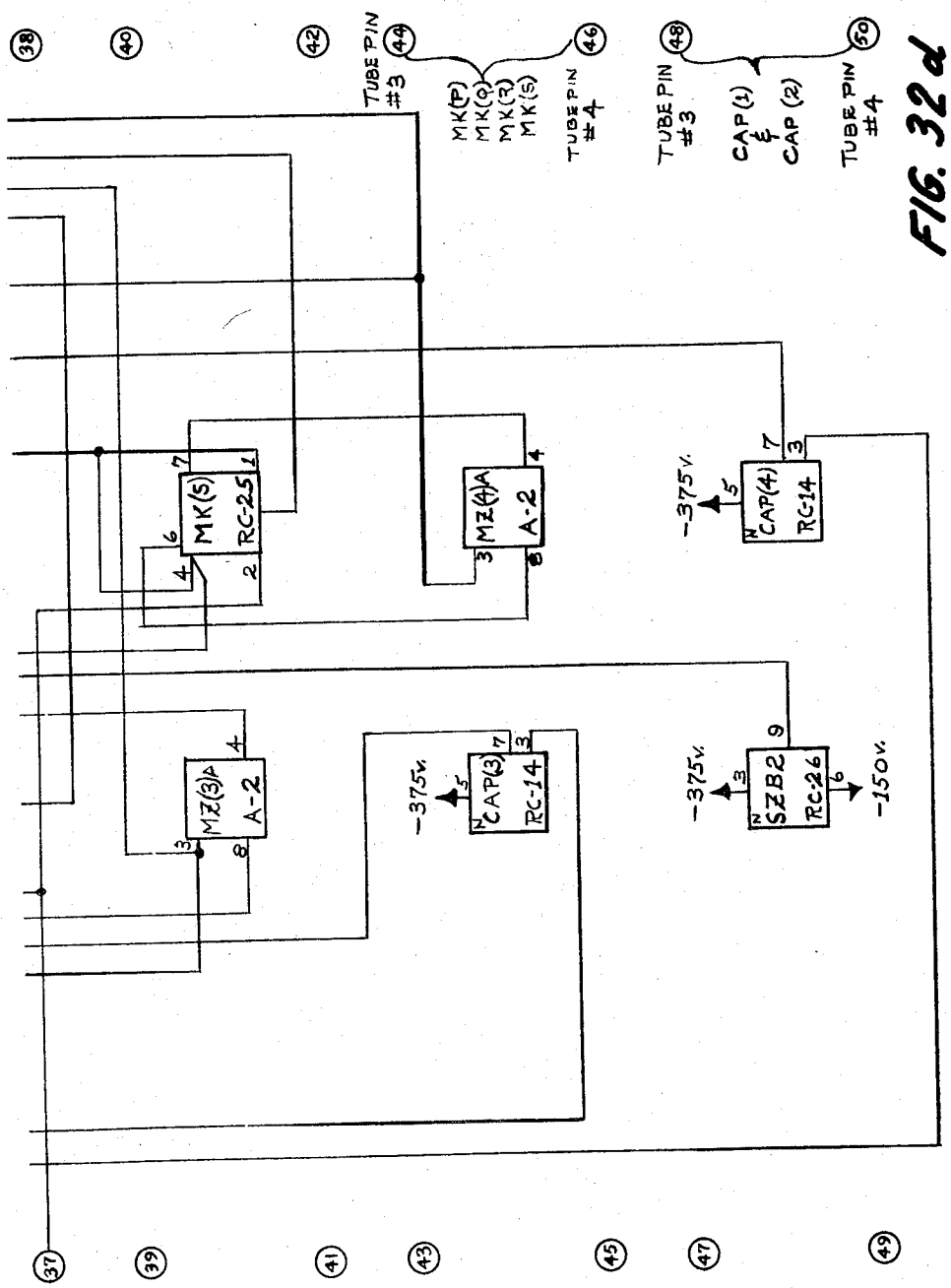


FIG. 32d

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

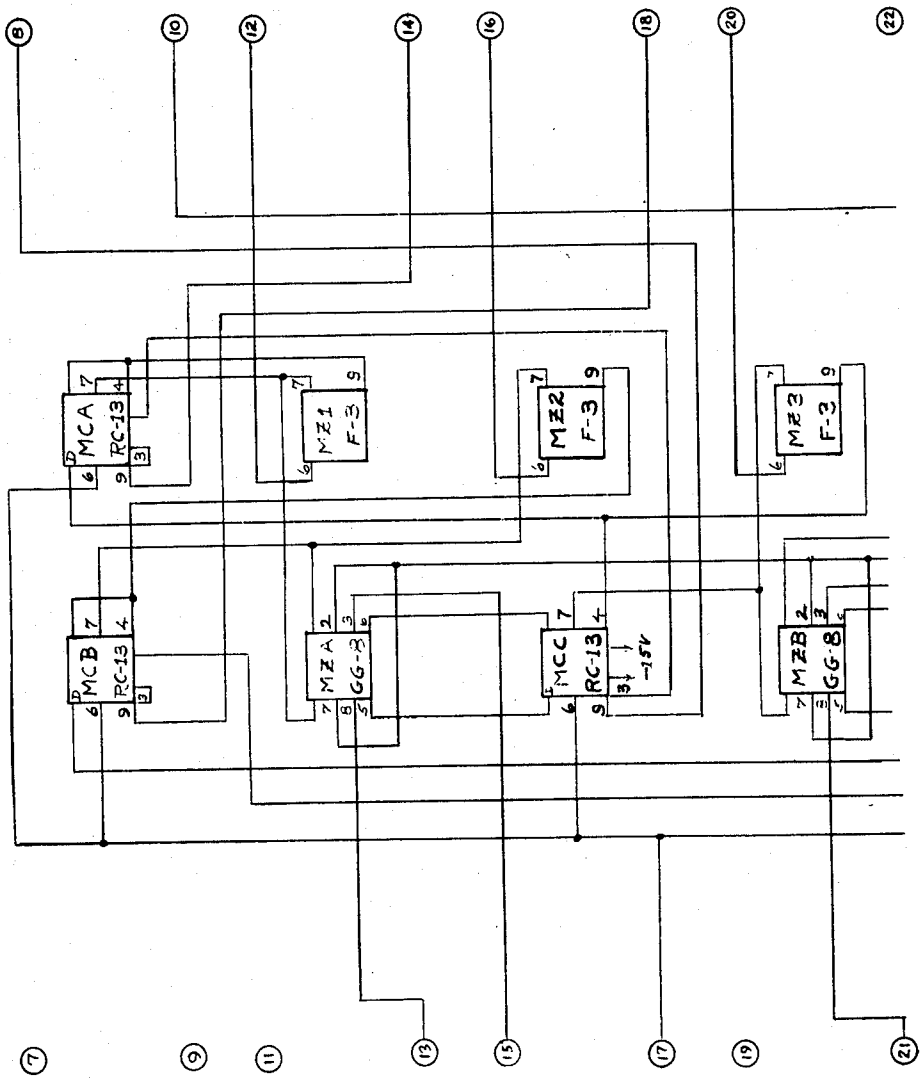


FIG. 33a

FIG. 33a	FIG. 33b	FIG. 33c

FIG. 33a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 84

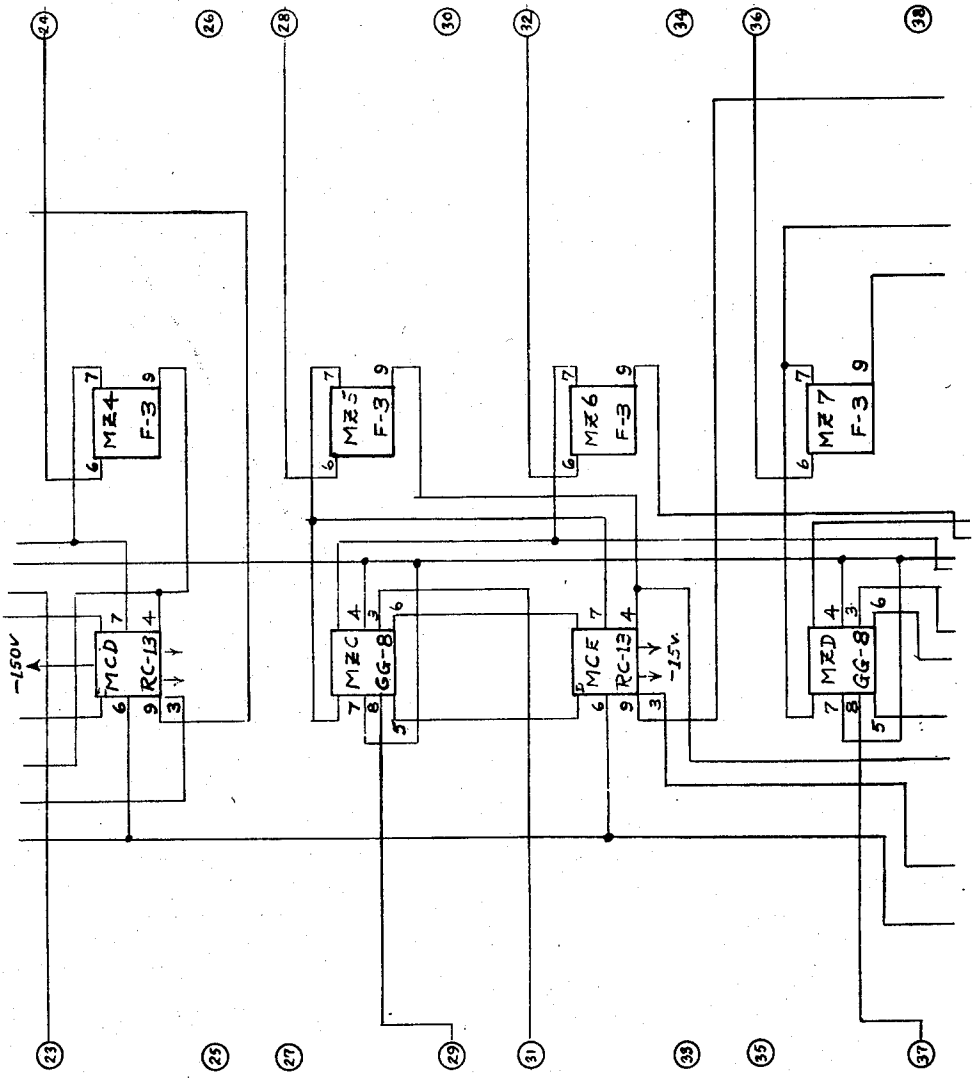


FIG. 33a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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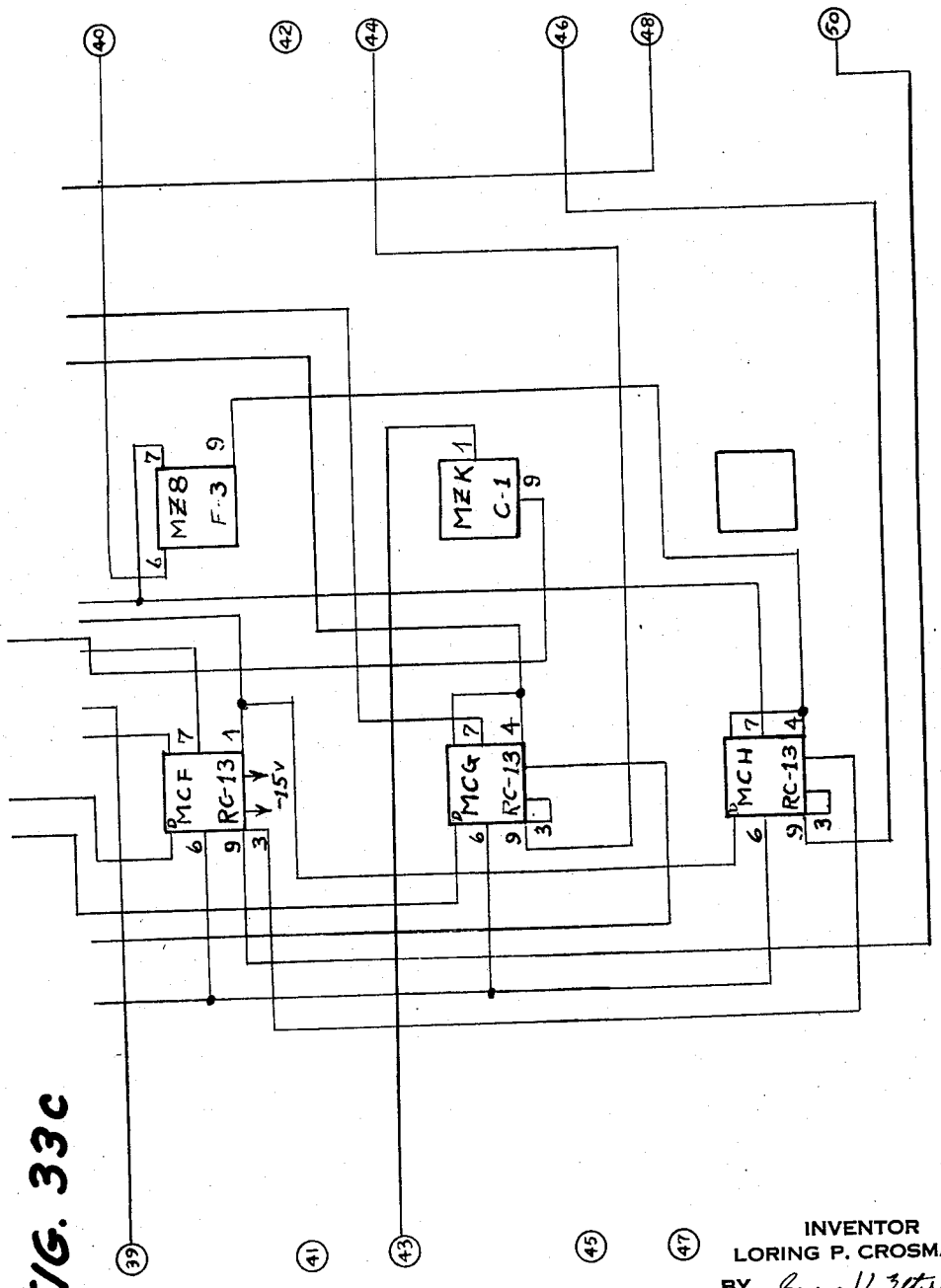


FIG. 33c

INVENTOR
LORING P. CROSMAN
BY George V. Ketzpath
ATTORNEY

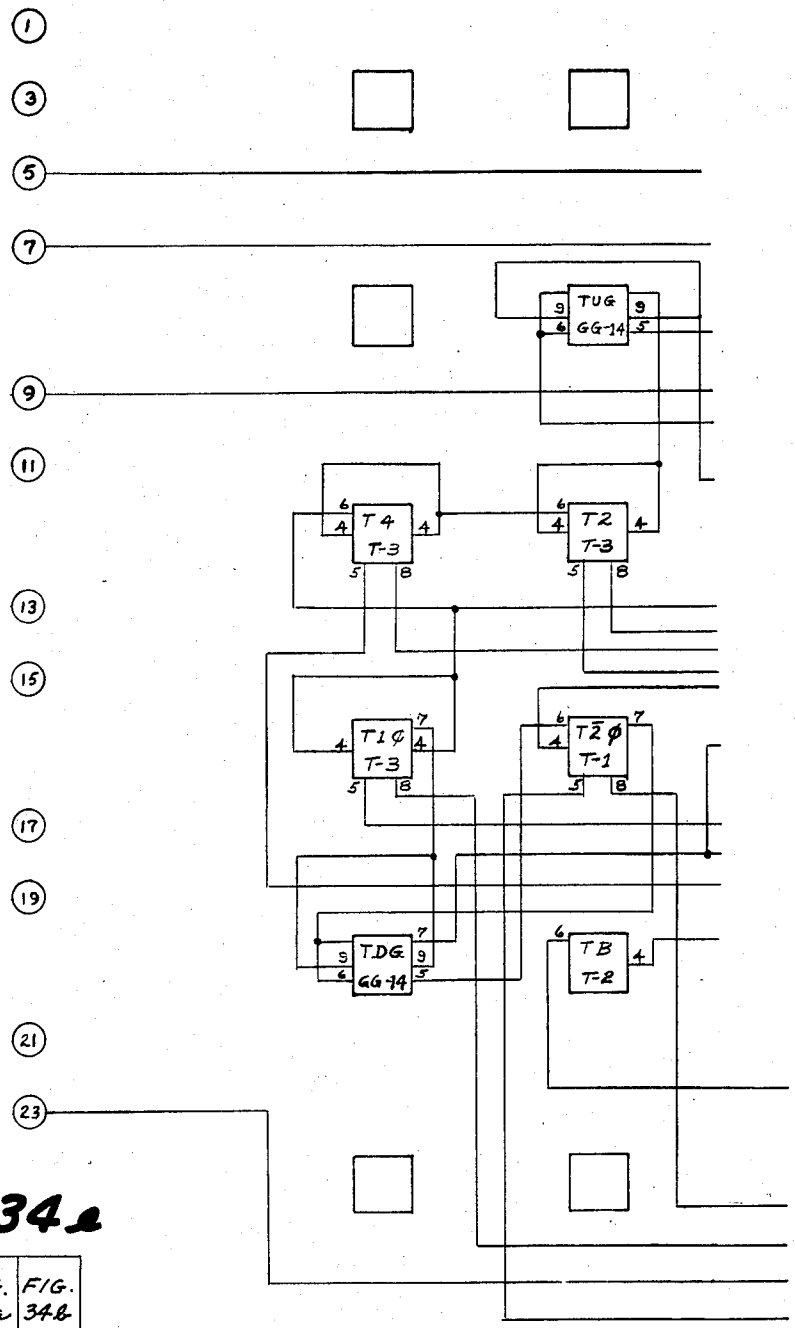


FIG. 34a

FIG. 34a	FIG. 34b
FIG. 34c	FIG. 34d

FIG. 34a

INVENTOR
LORING P. CROSMAN
BY George V. Ketzpath
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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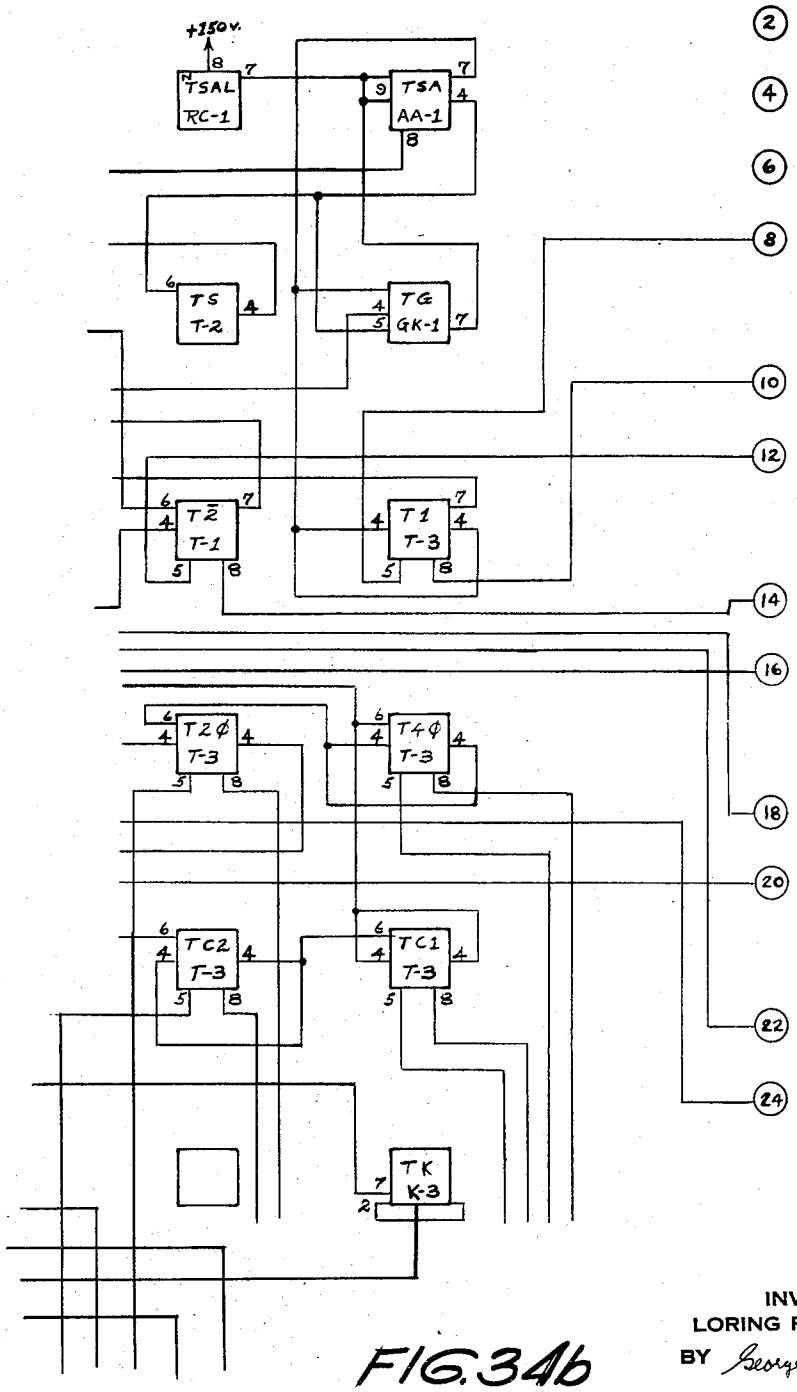


FIG. 34b

INVENTOR
LORING P. CROSMAN
BY George V. Ketzpath
ATTORNEY

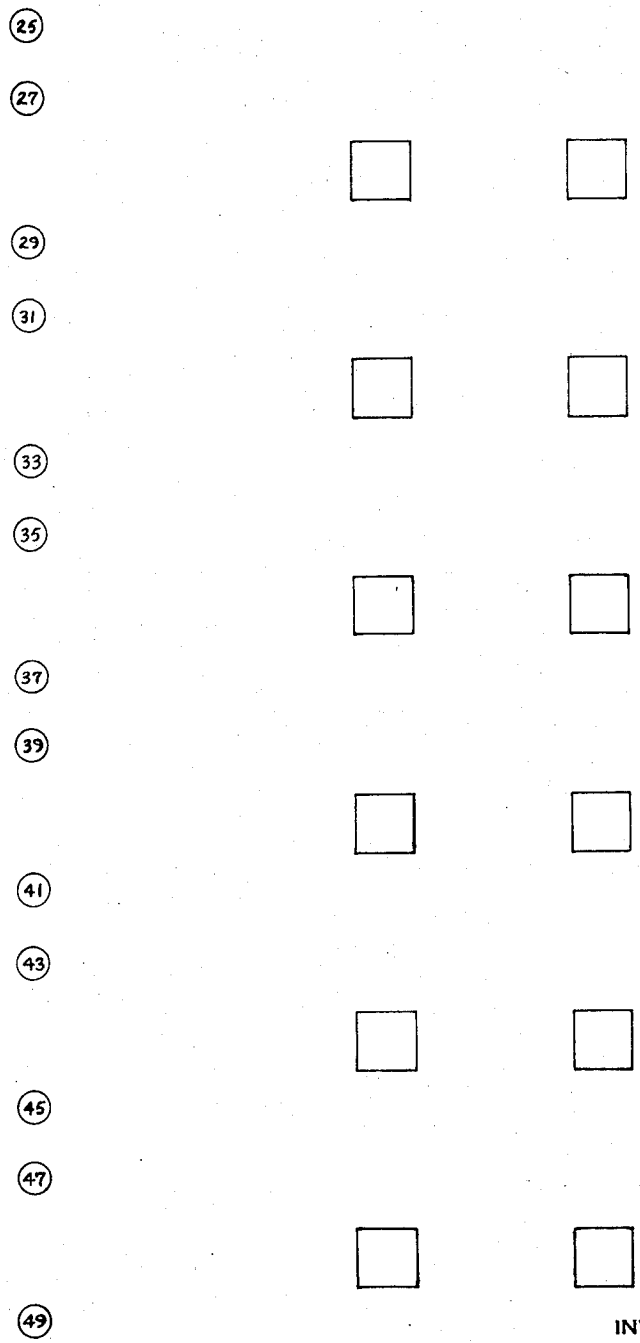


FIG. 34c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

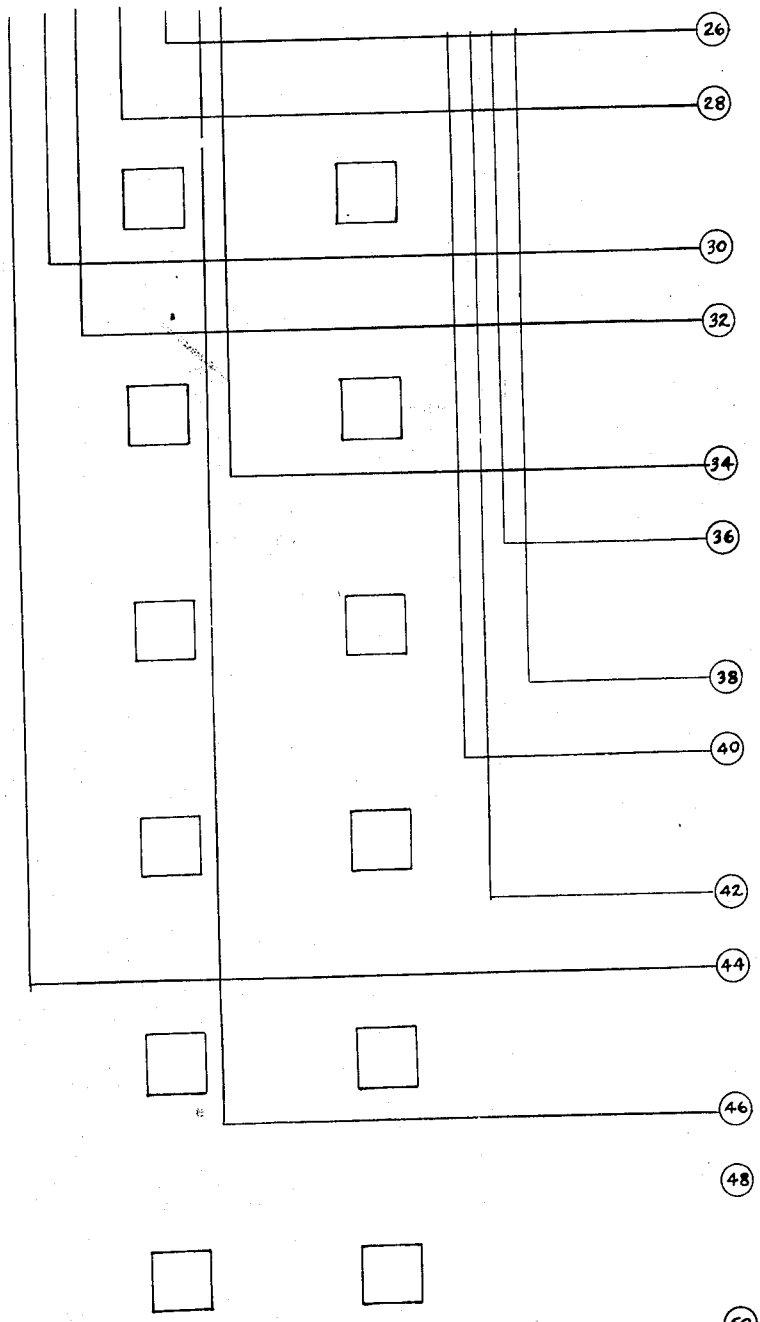
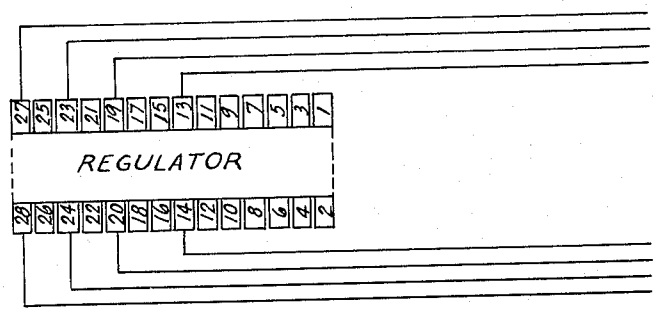


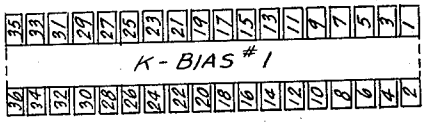
FIG. 34d

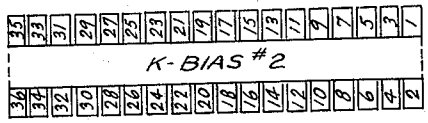
INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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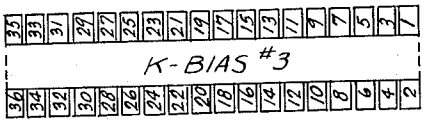


FIG. 35a

FIG. 35a	FIG. 35b	FIG. 35c	FIG. 35d
FIG. 35e	FIG 35f	FIG. 35g	FIG 35h
FIG. 35i	FIG. 35j	FIG. 35k	FIG. 35l
FIG. 35m	FIG. 35n	FIG. 350	FIG. 35p

FIG. 35q

INVENTOR.
LORING P. CROSMAN
BY Richard K. Hamilton
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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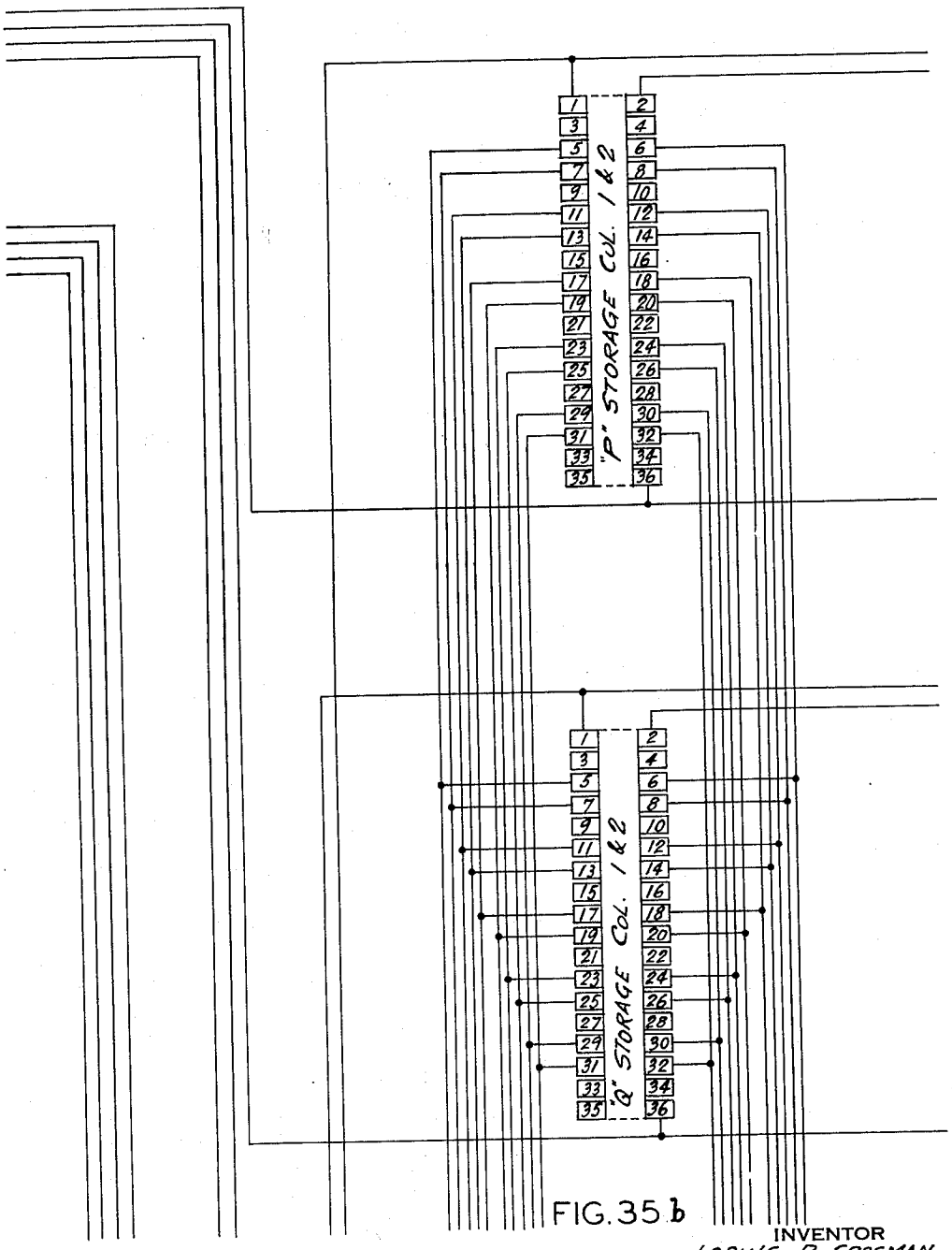


FIG. 35b

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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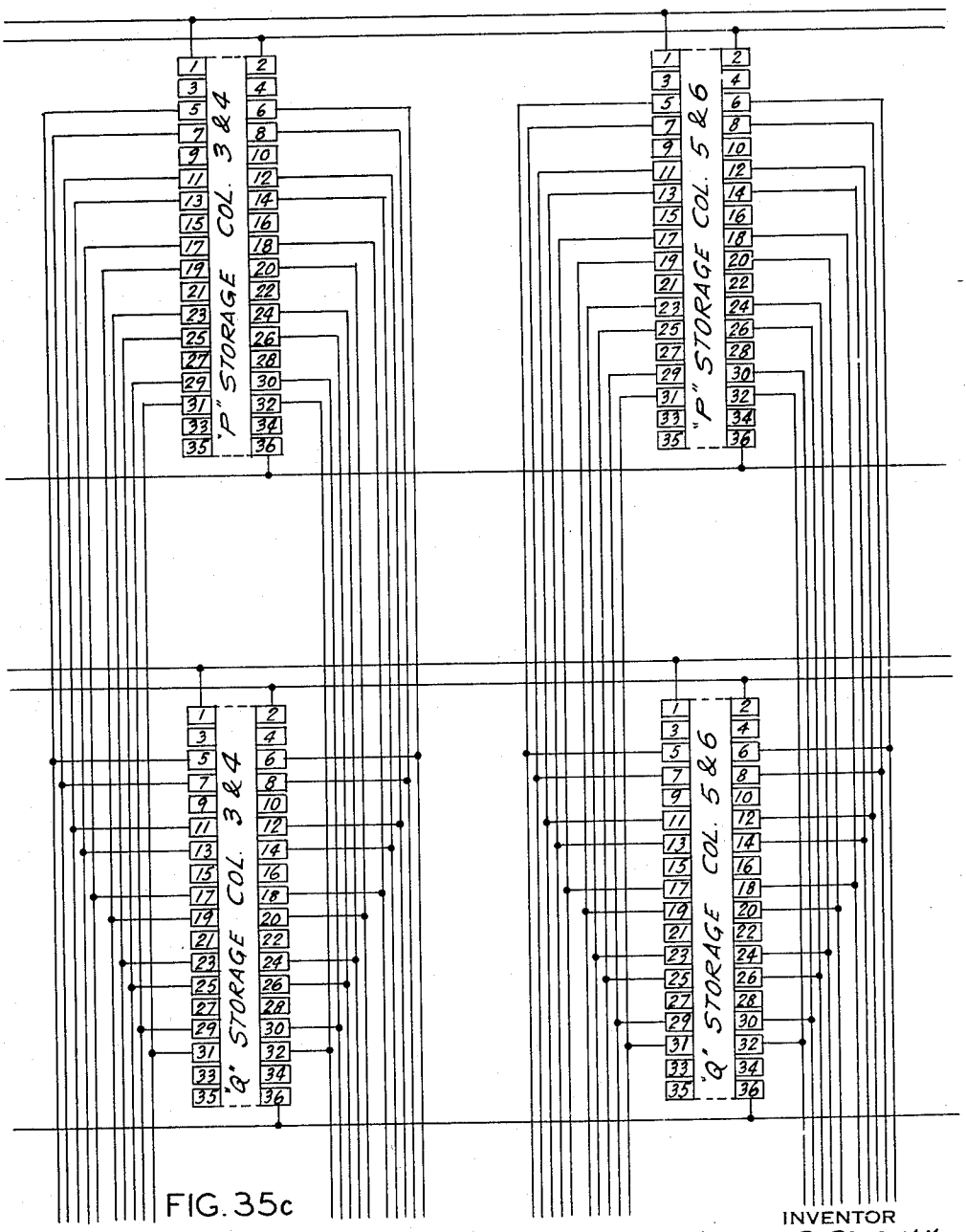


FIG. 35c

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 93

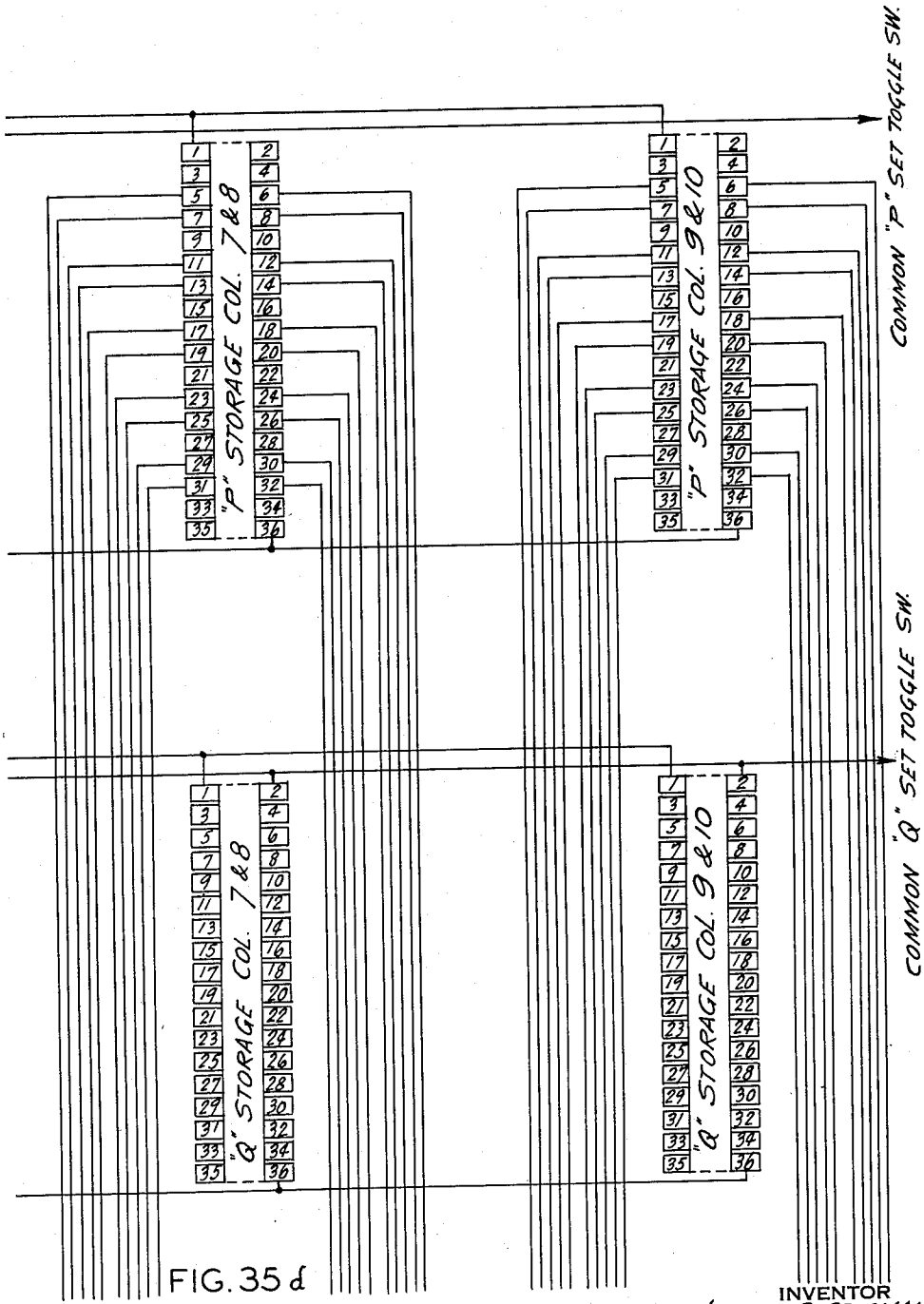


FIG. 35d

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

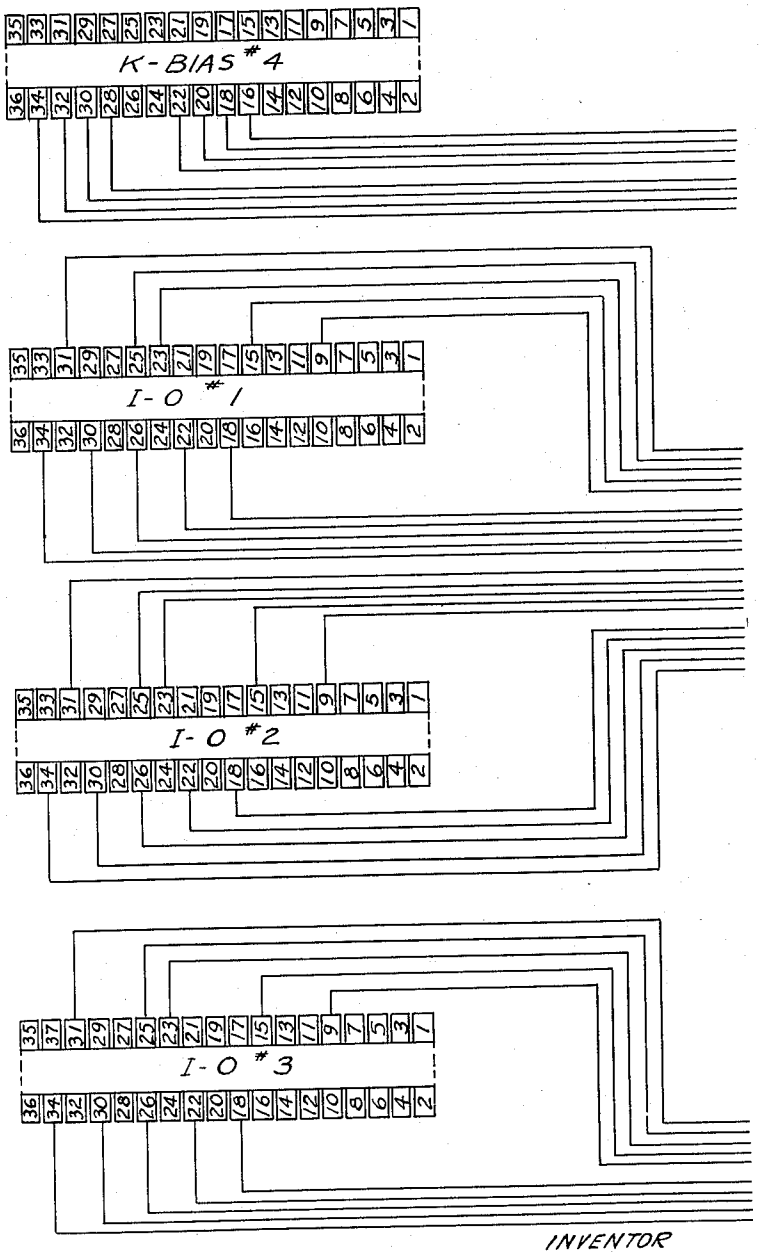


FIG. 35e

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

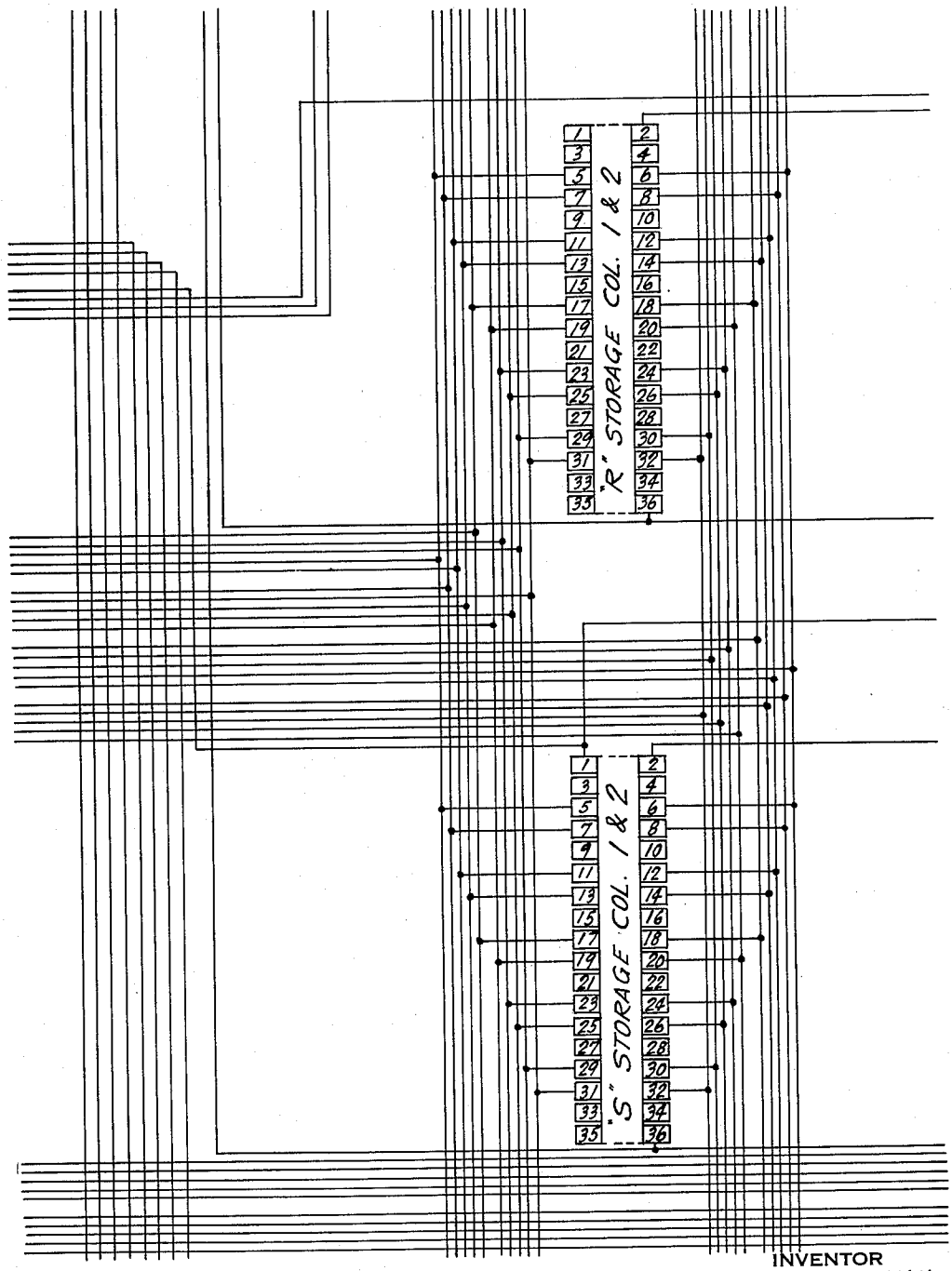


FIG. 35f

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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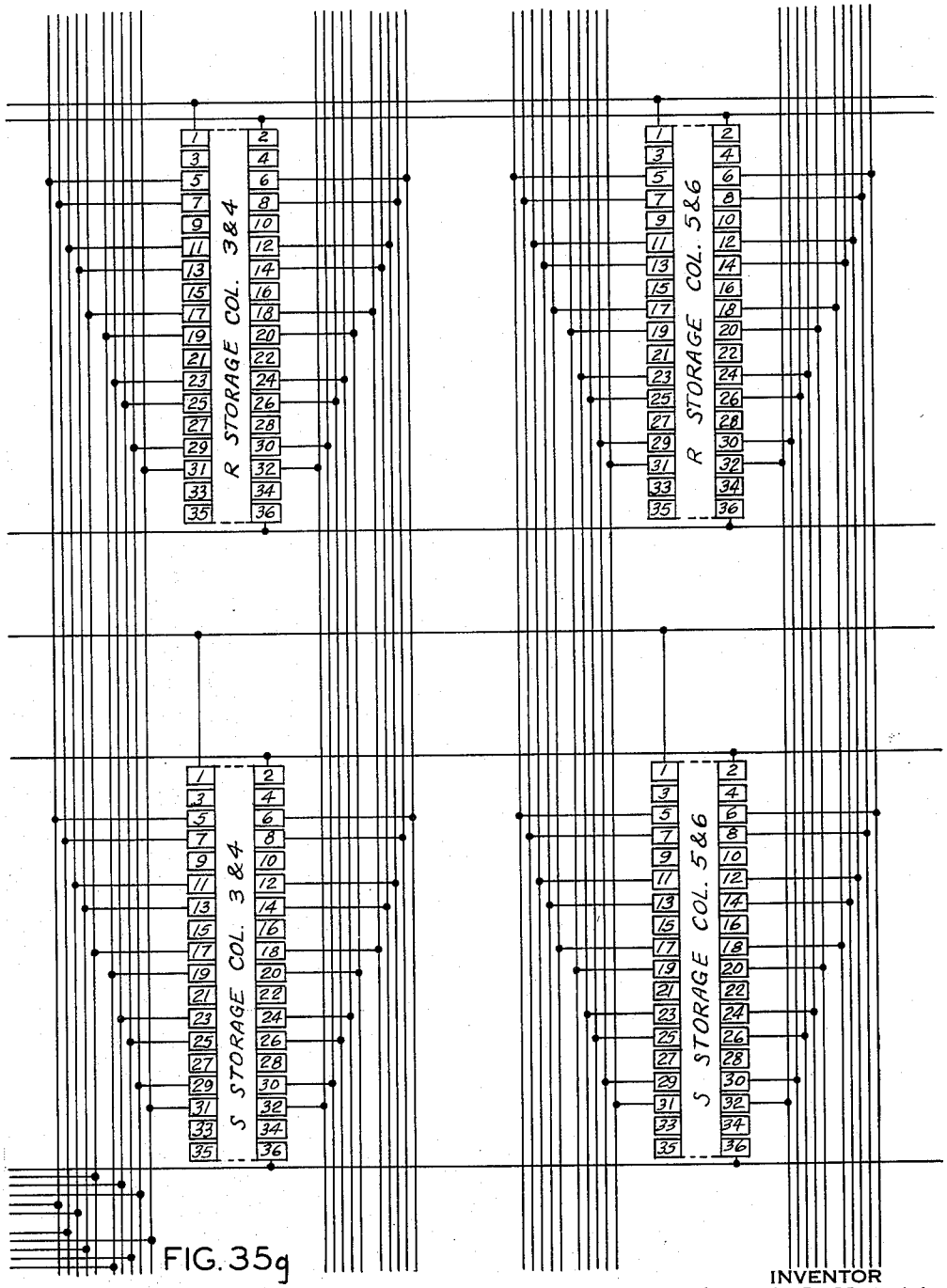


FIG. 35g

INVENTOR
LORING P. CROSMAN
BY Richard W. Crosman
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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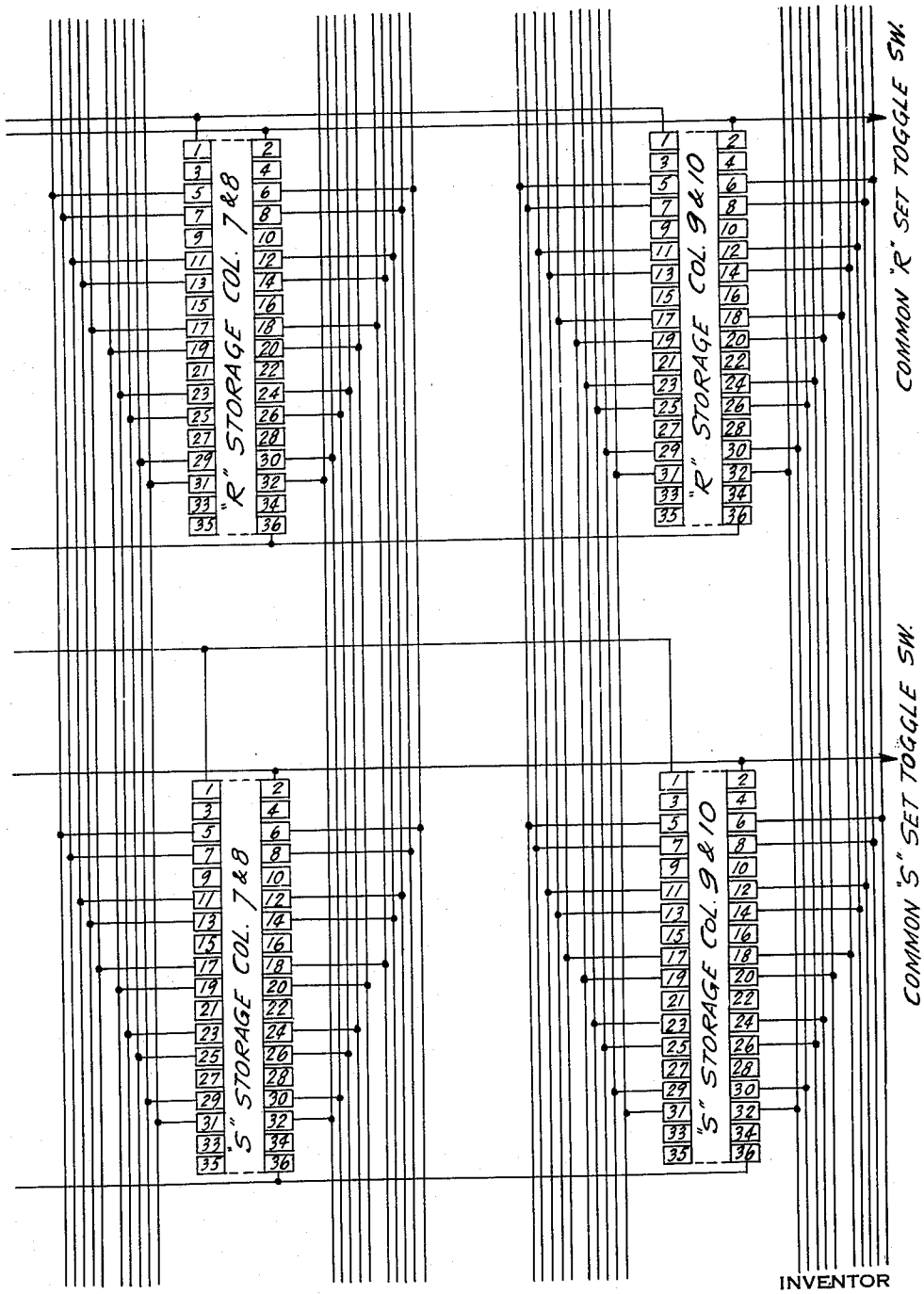


FIG. 35h

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 98

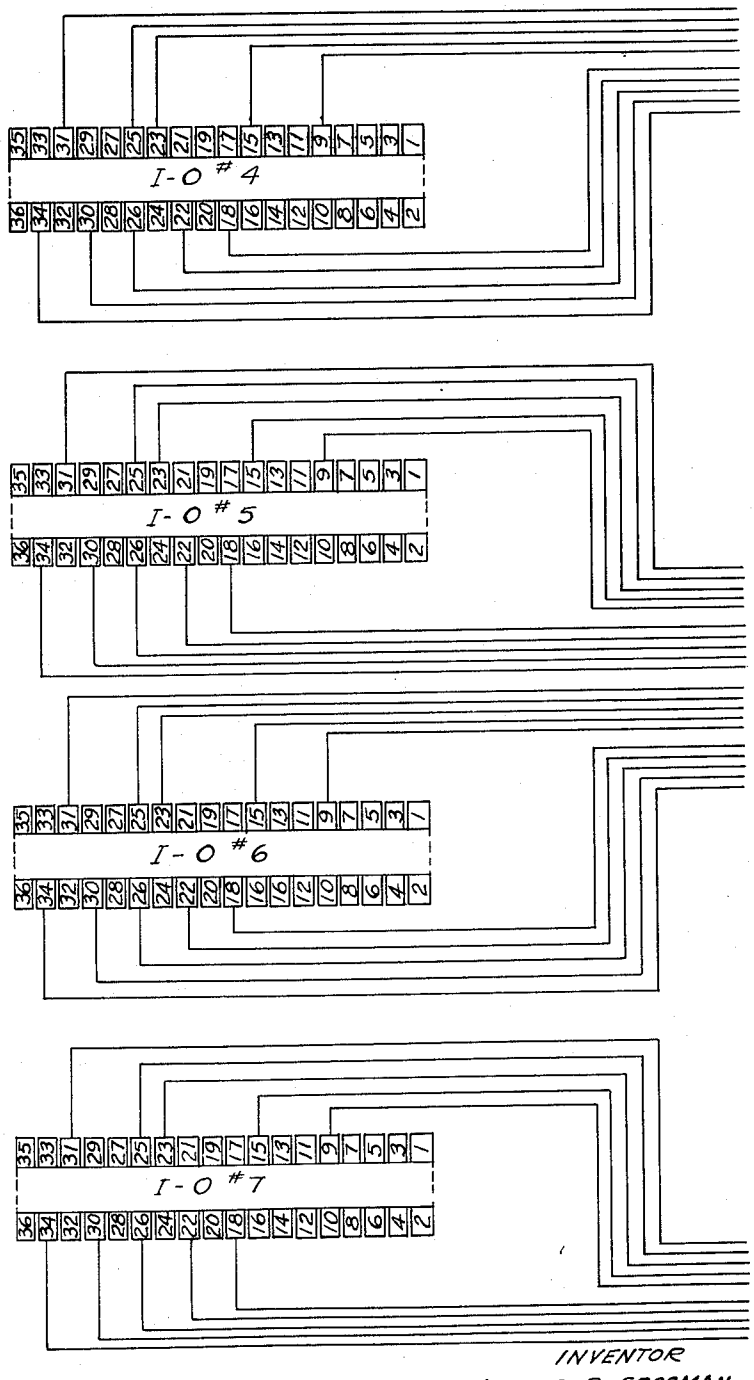


FIG. 35i

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 99

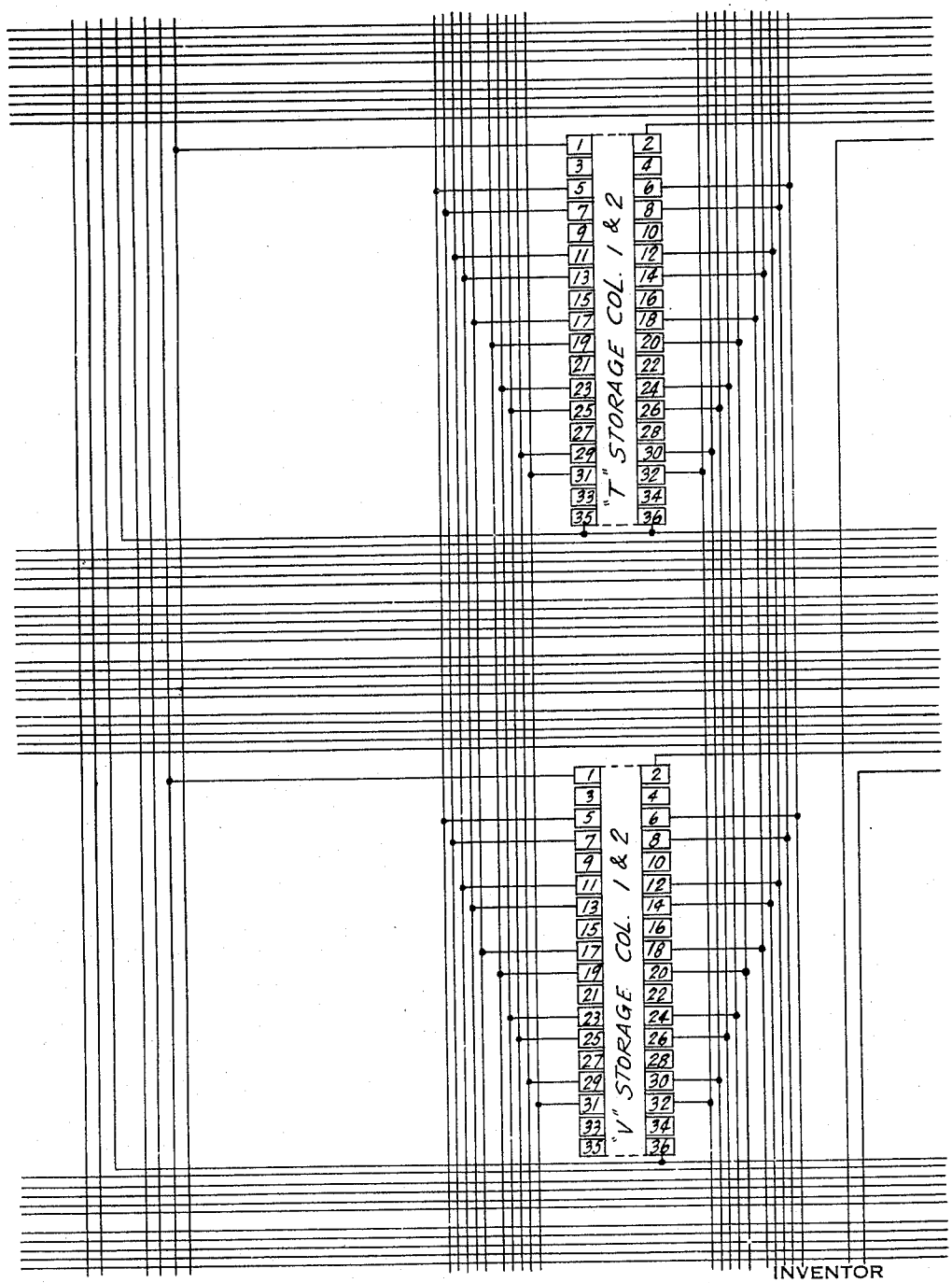


FIG. 35j

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 100

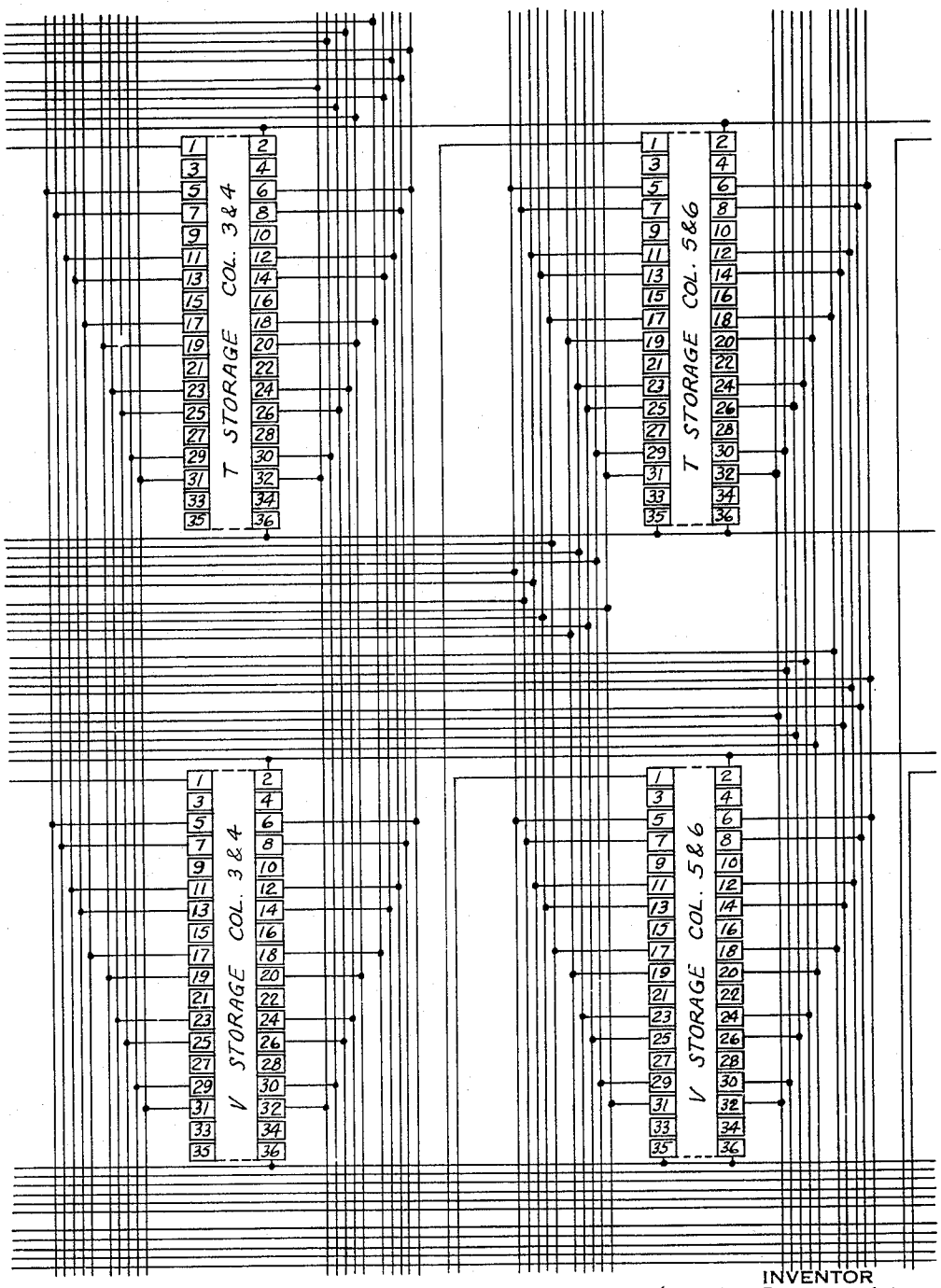


FIG. 35K

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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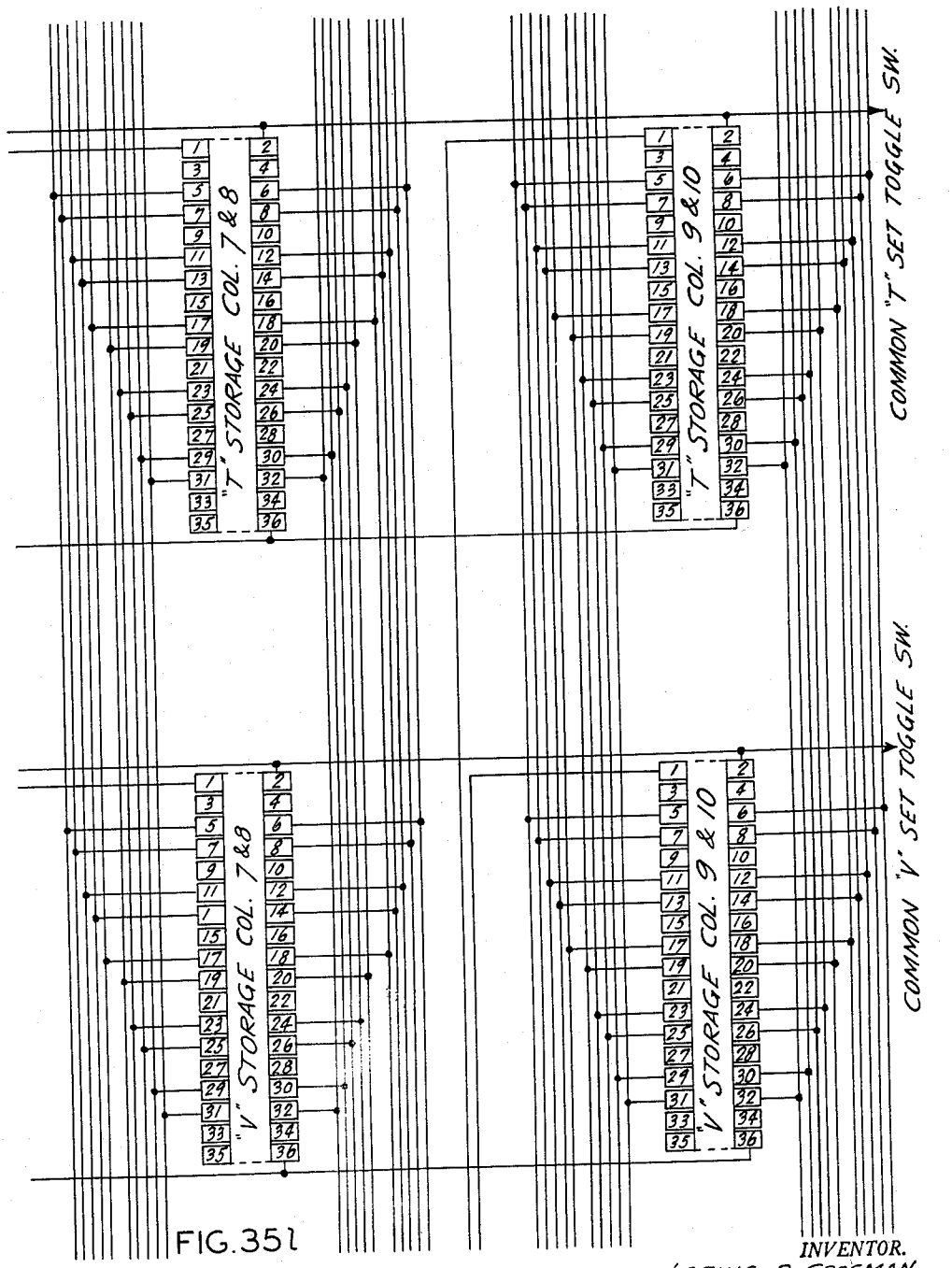


FIG. 351

INVENTOR.
LORING P. CROSMAN
BY Richard K. Franklin

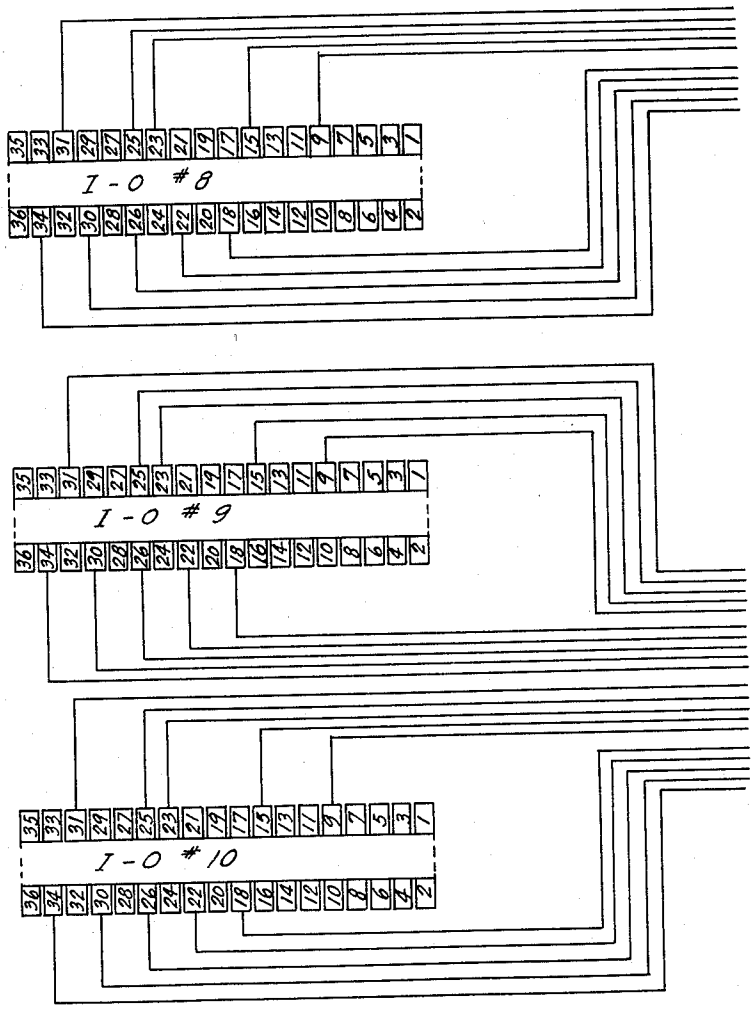


FIG. 35m

INVENTOR.
LORING P. CROSMAN
BY Richard M. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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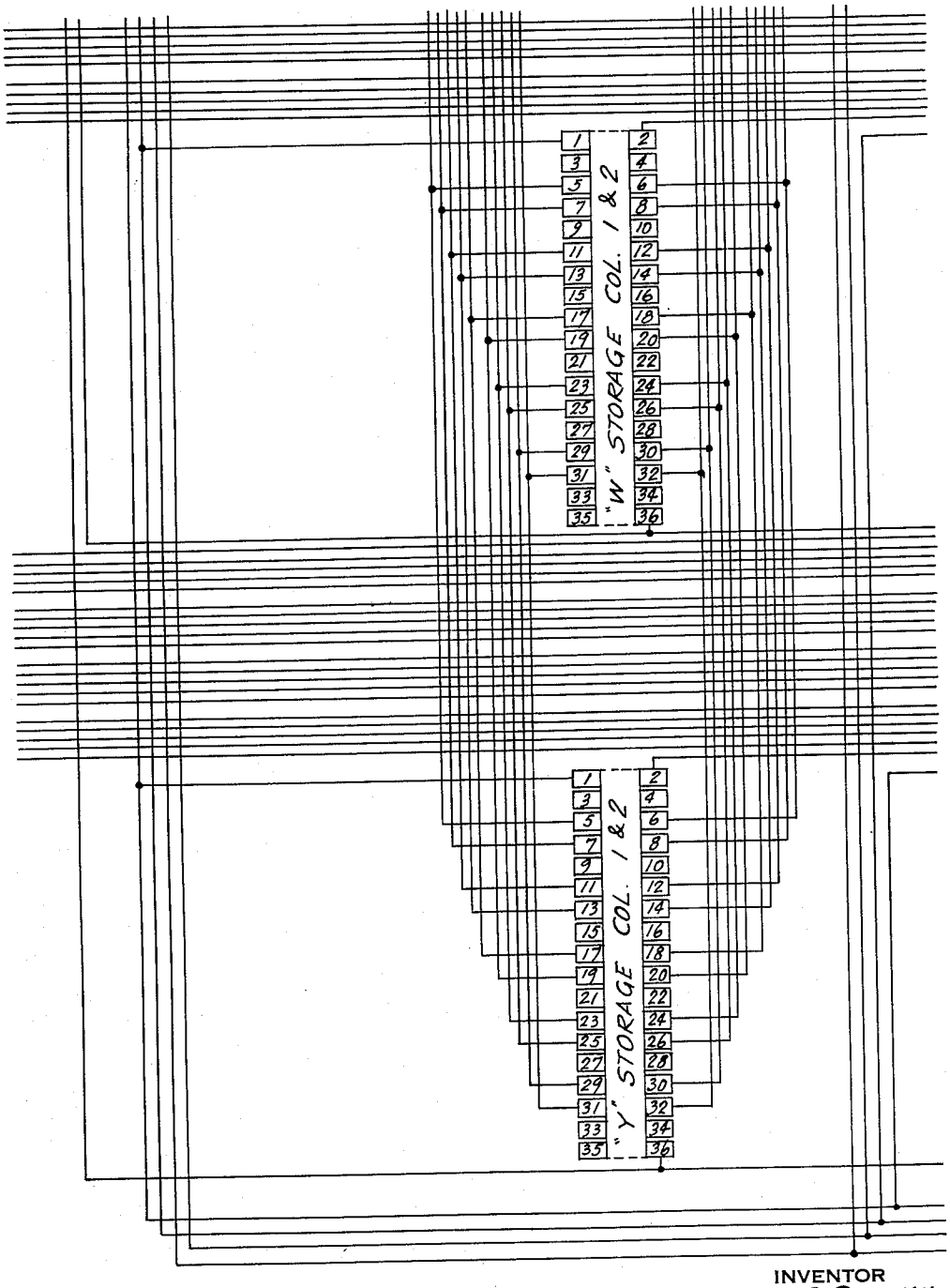


FIG. 35n

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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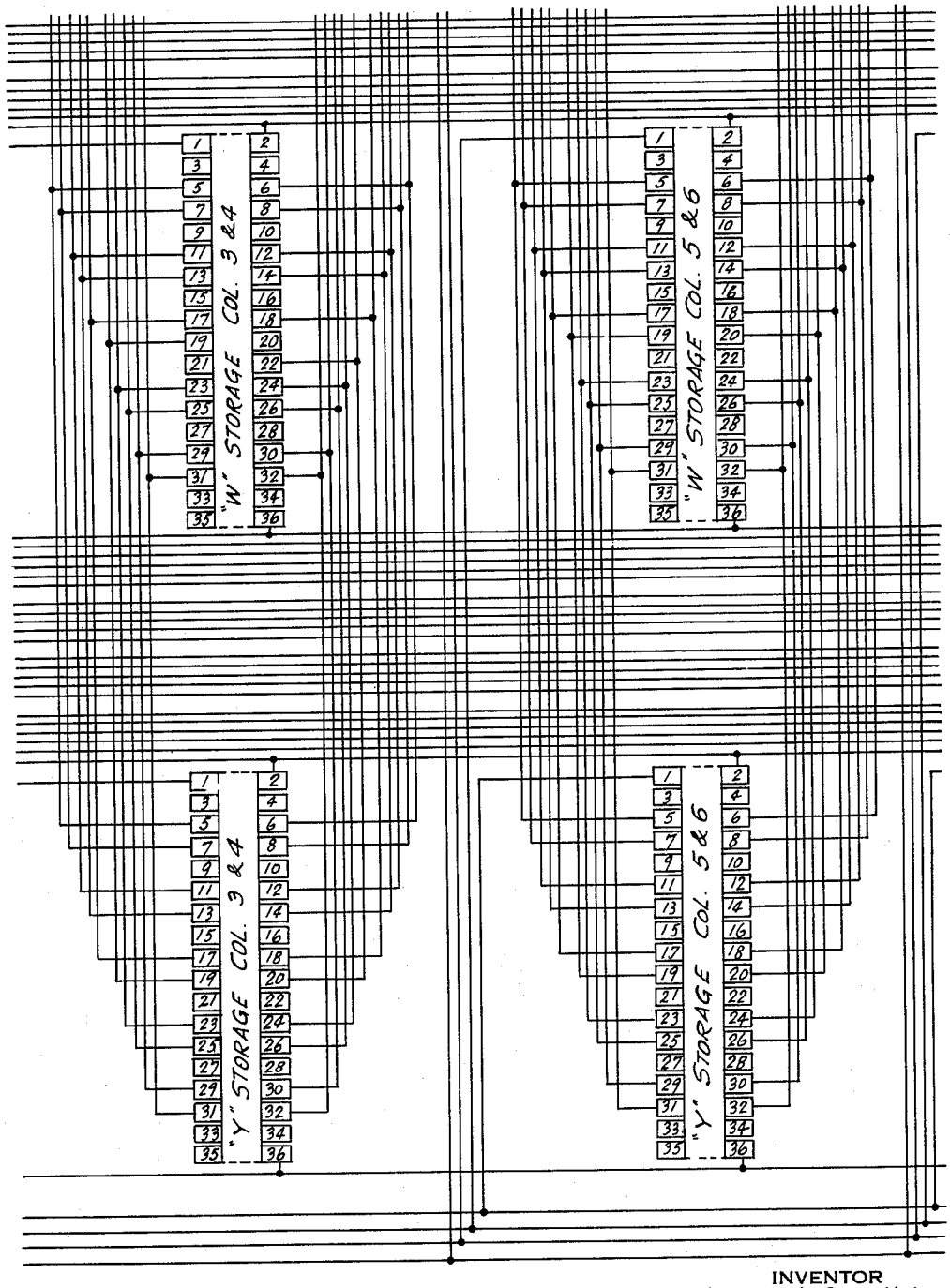


FIG. 35o

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 105

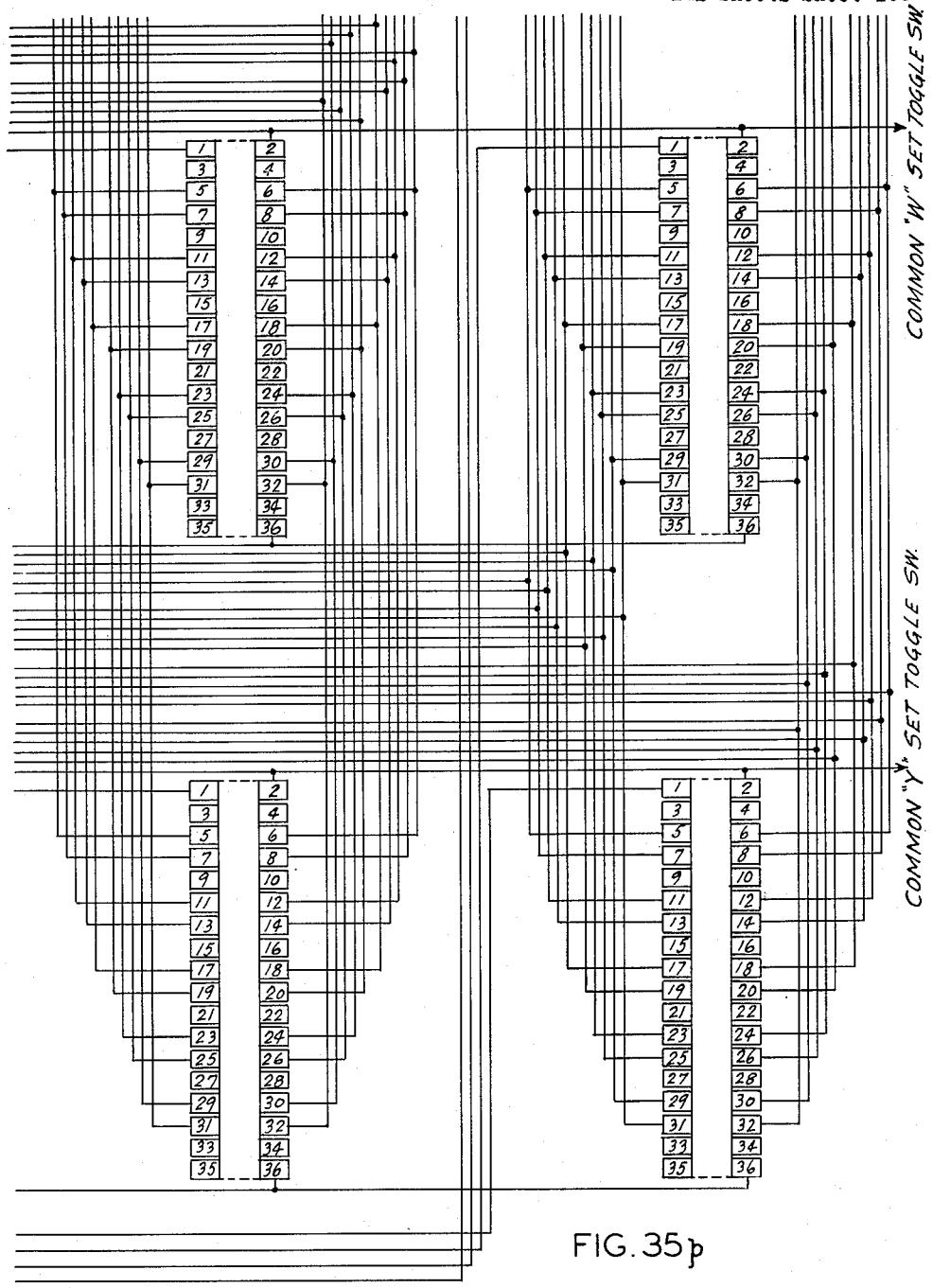


FIG. 35p

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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FIG. 36m

FIG. 36a	FIG. 36b	FIG. 36c
FIG. 36d	FIG. 36e	FIG. 36f
FIG. 36g	FIG. 36h	FIG. 36i
FIG. 36j	FIG. 36k	FIG. 36l

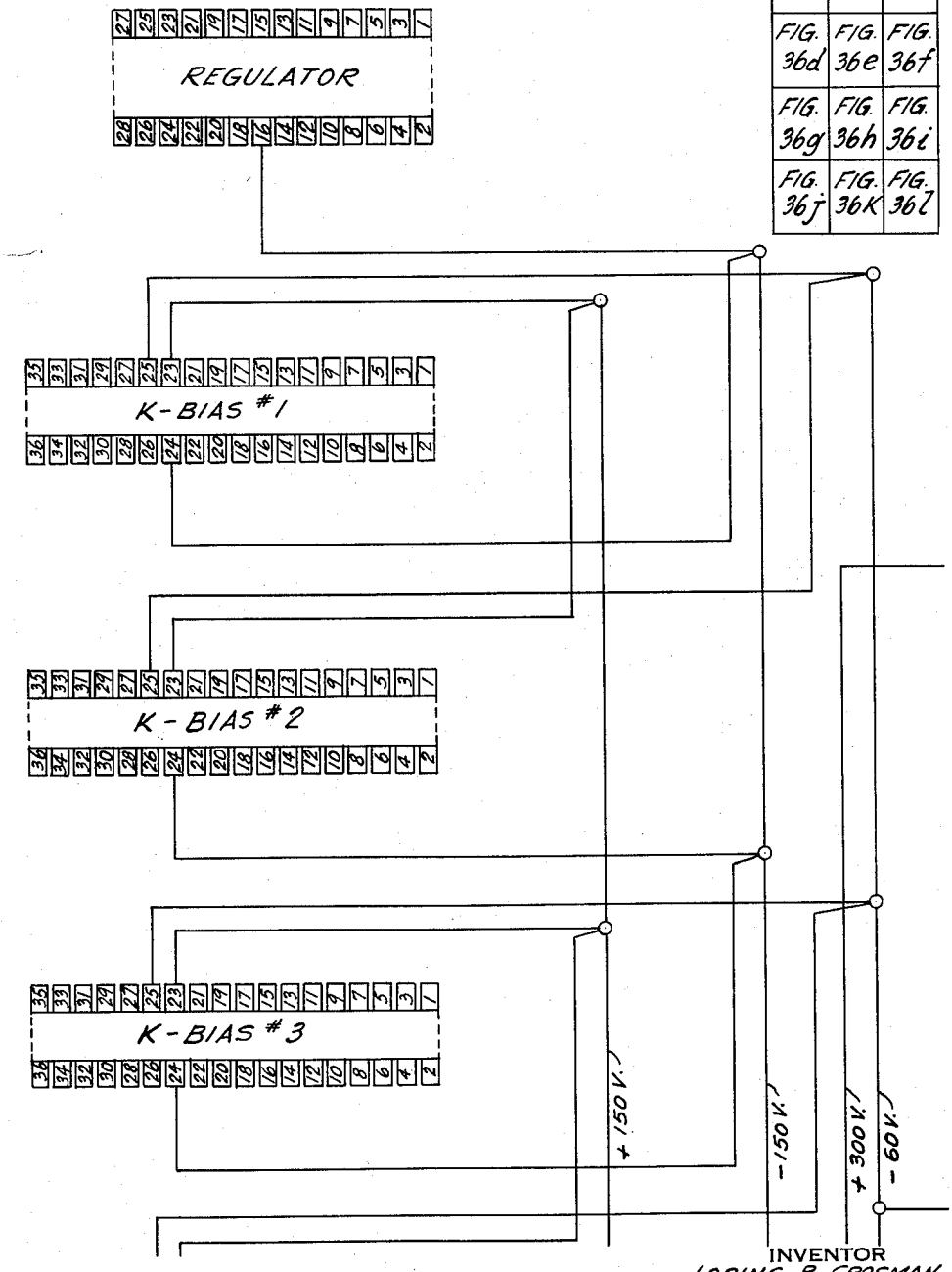
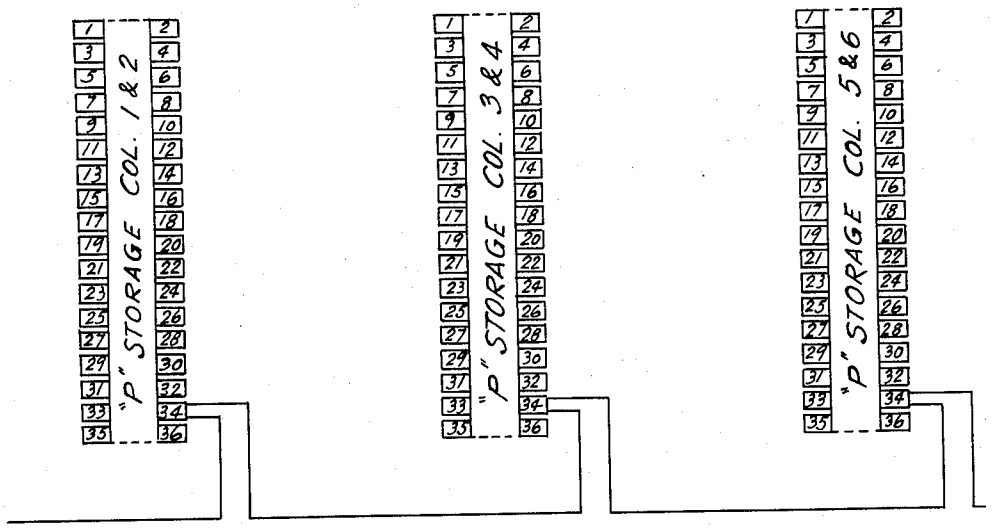


FIG. 36a

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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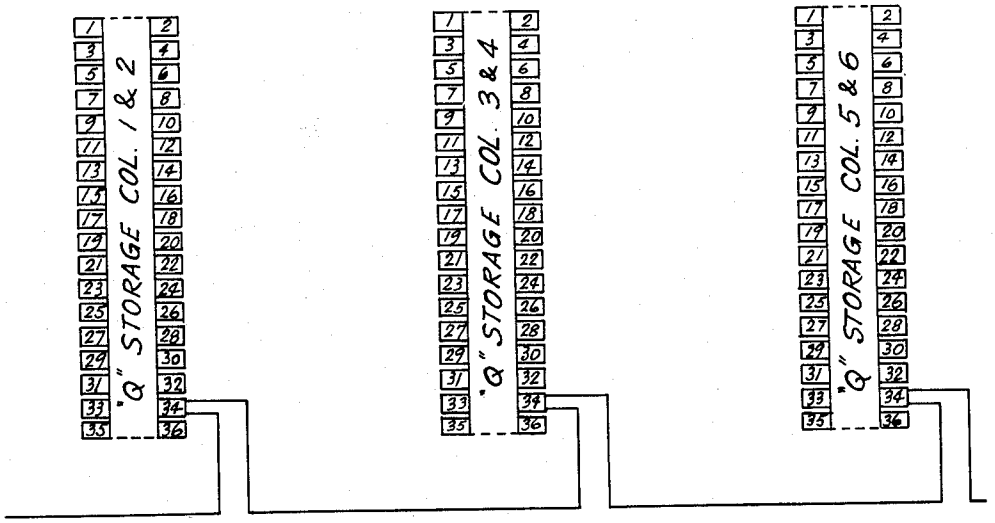


FIG. 36b

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 108

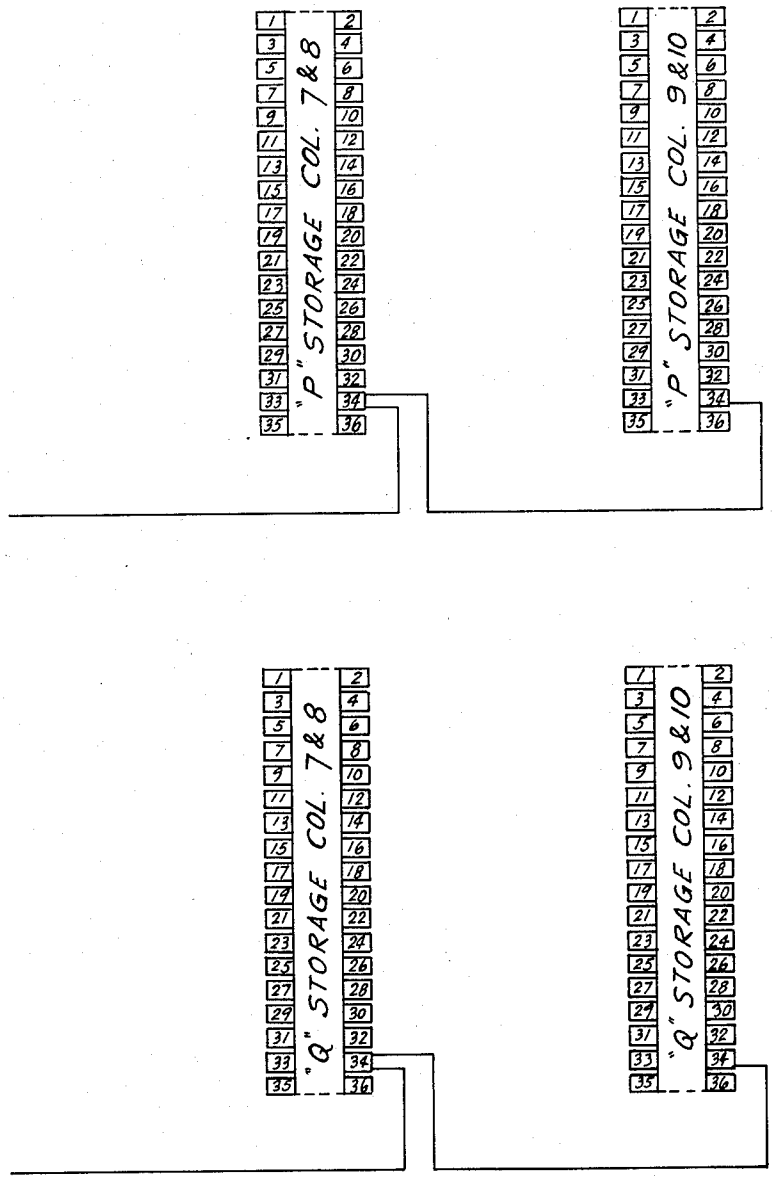


FIG. 36c

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 109

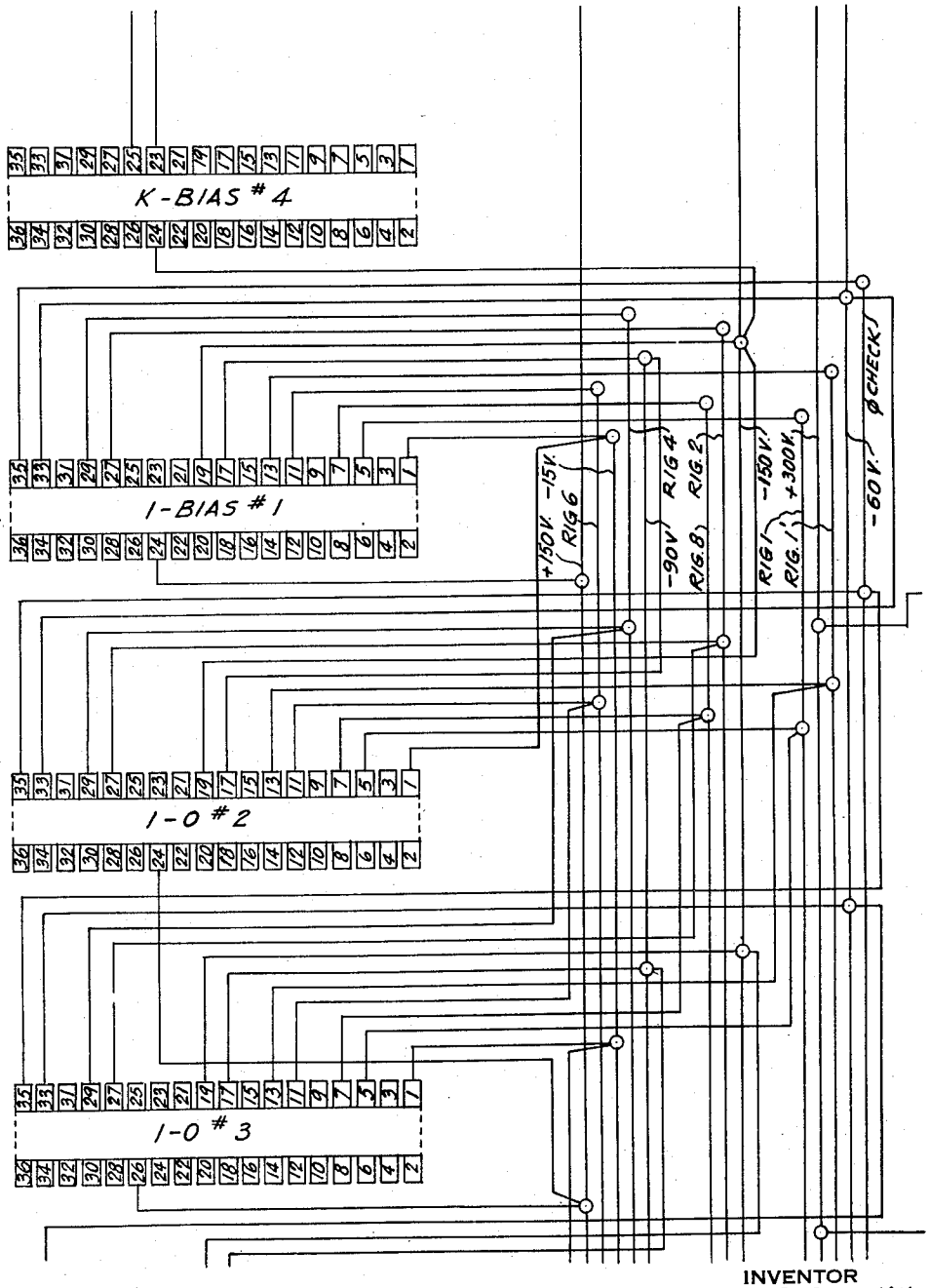


FIG. 36d

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 110

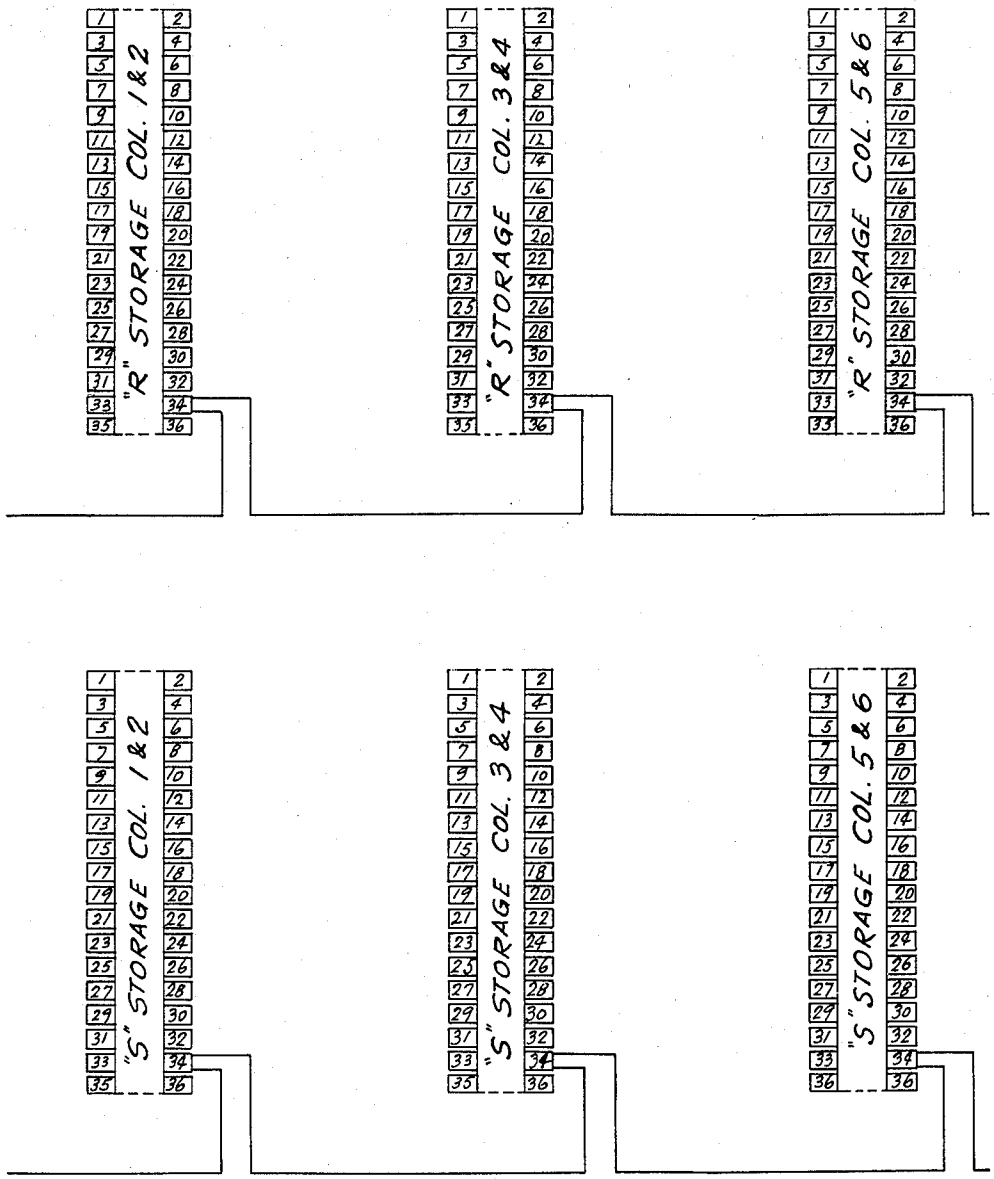


FIG. 36e

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 111

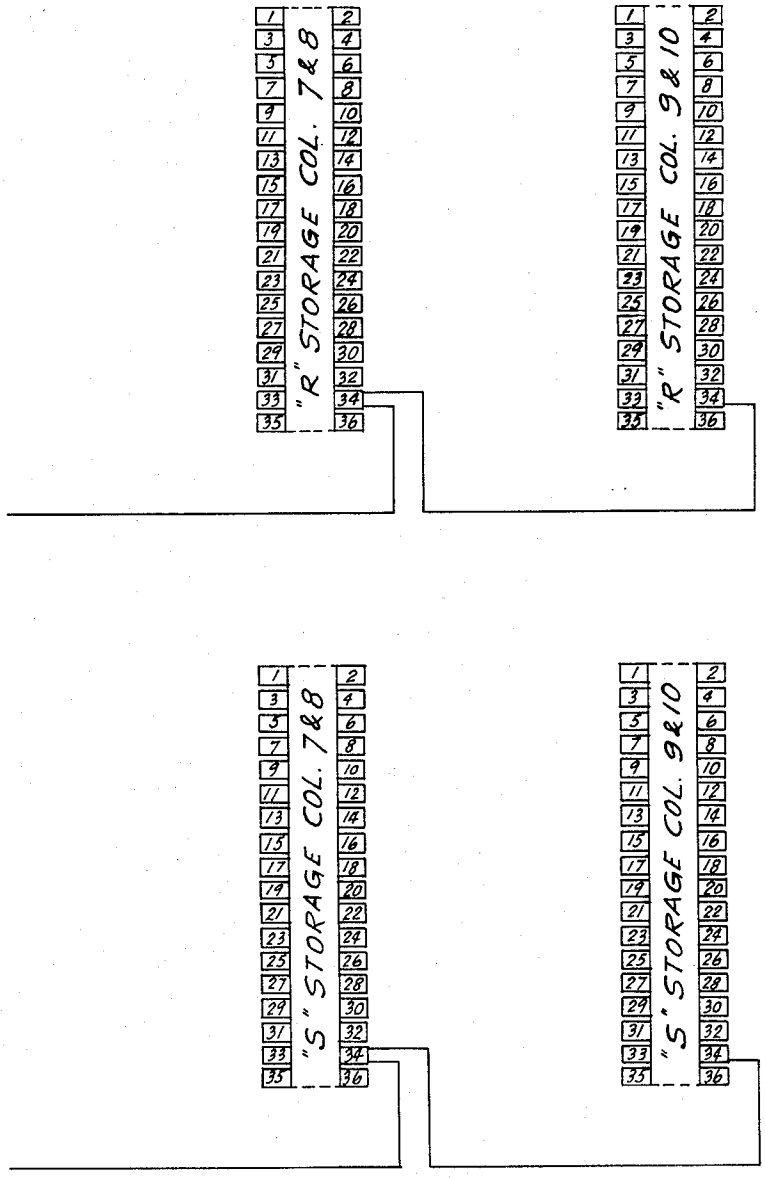


FIG. 36 f

INVENTOR
LORING P CROSMAN
BY Richard K. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 112

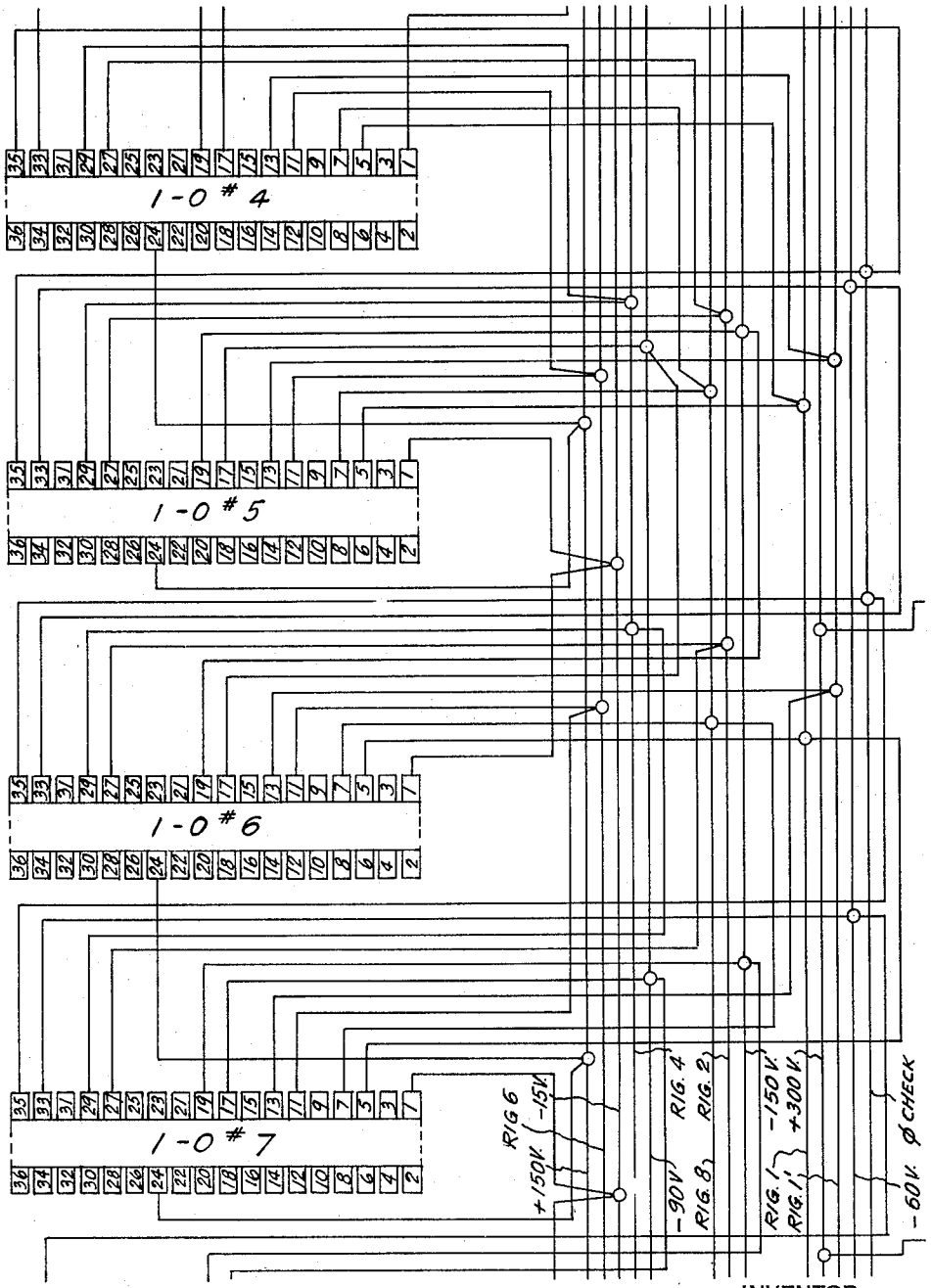
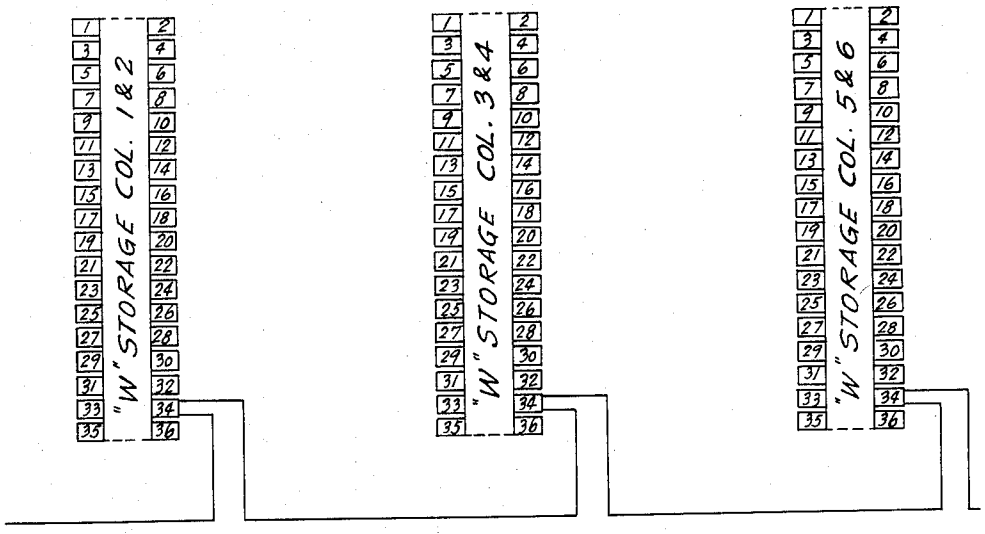


FIG. 36g

INVENTOR
LORING P. CROSMAN
BY Richard M. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 113



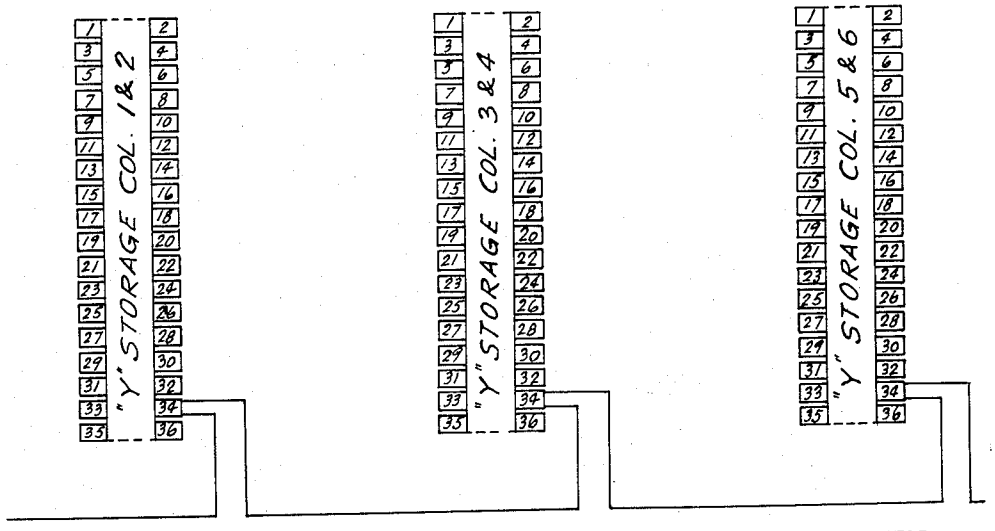


FIG. 36h

INVENTOR.
LORING P. CROSMAN
BY Richard K. Franklin

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 114

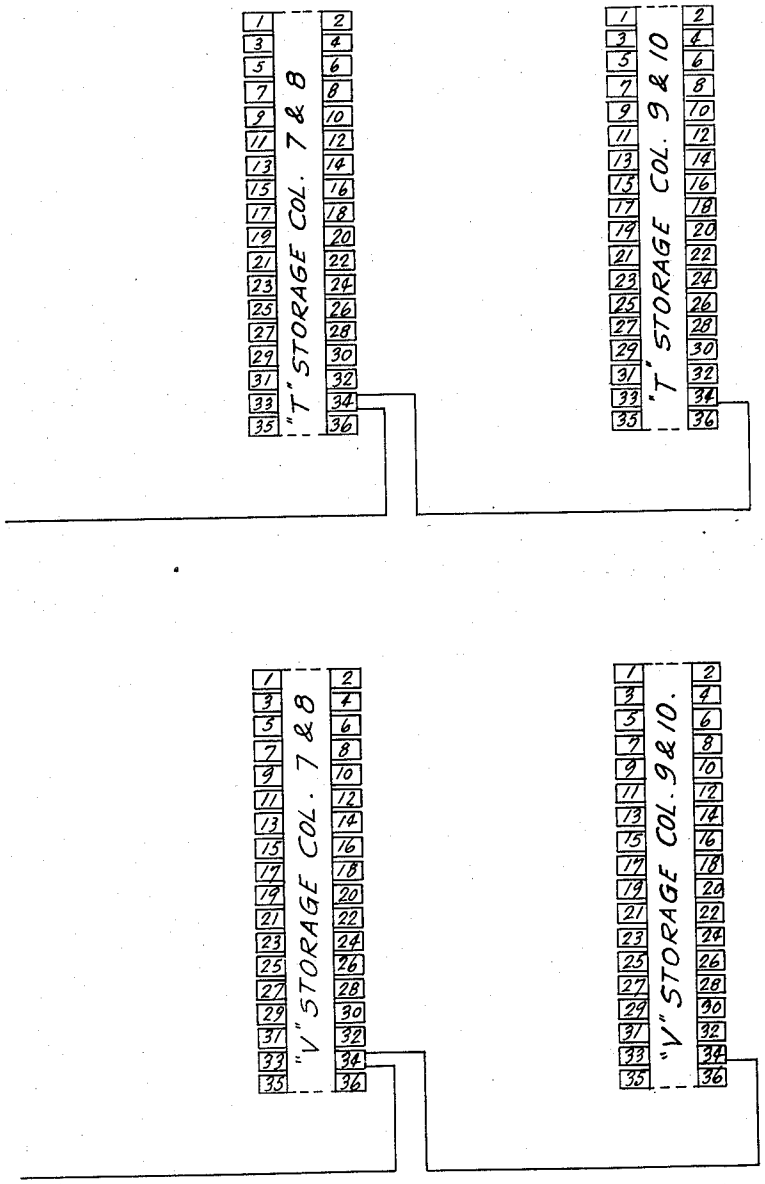


FIG. 36i

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 115

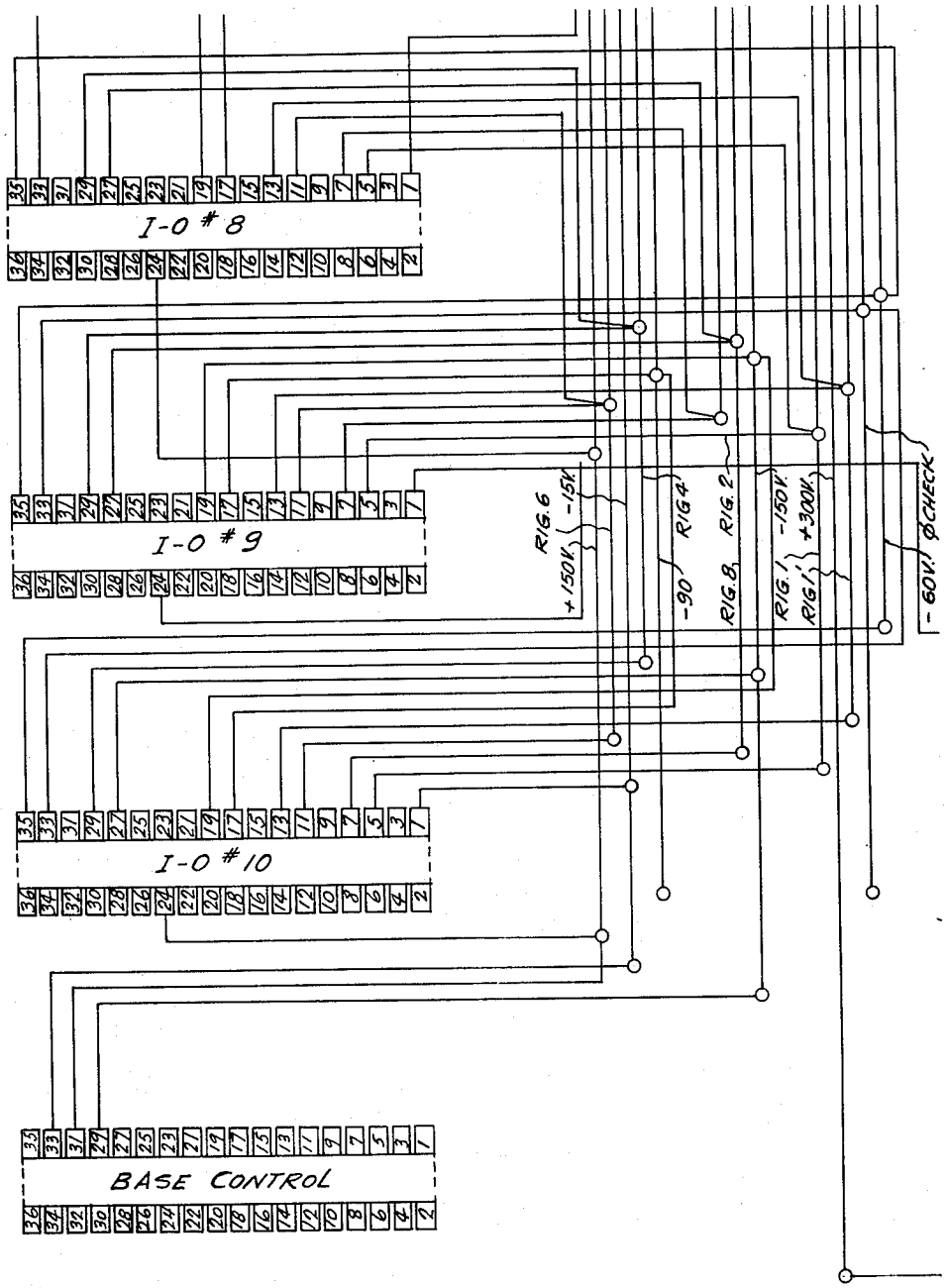


FIG. 36j

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 116

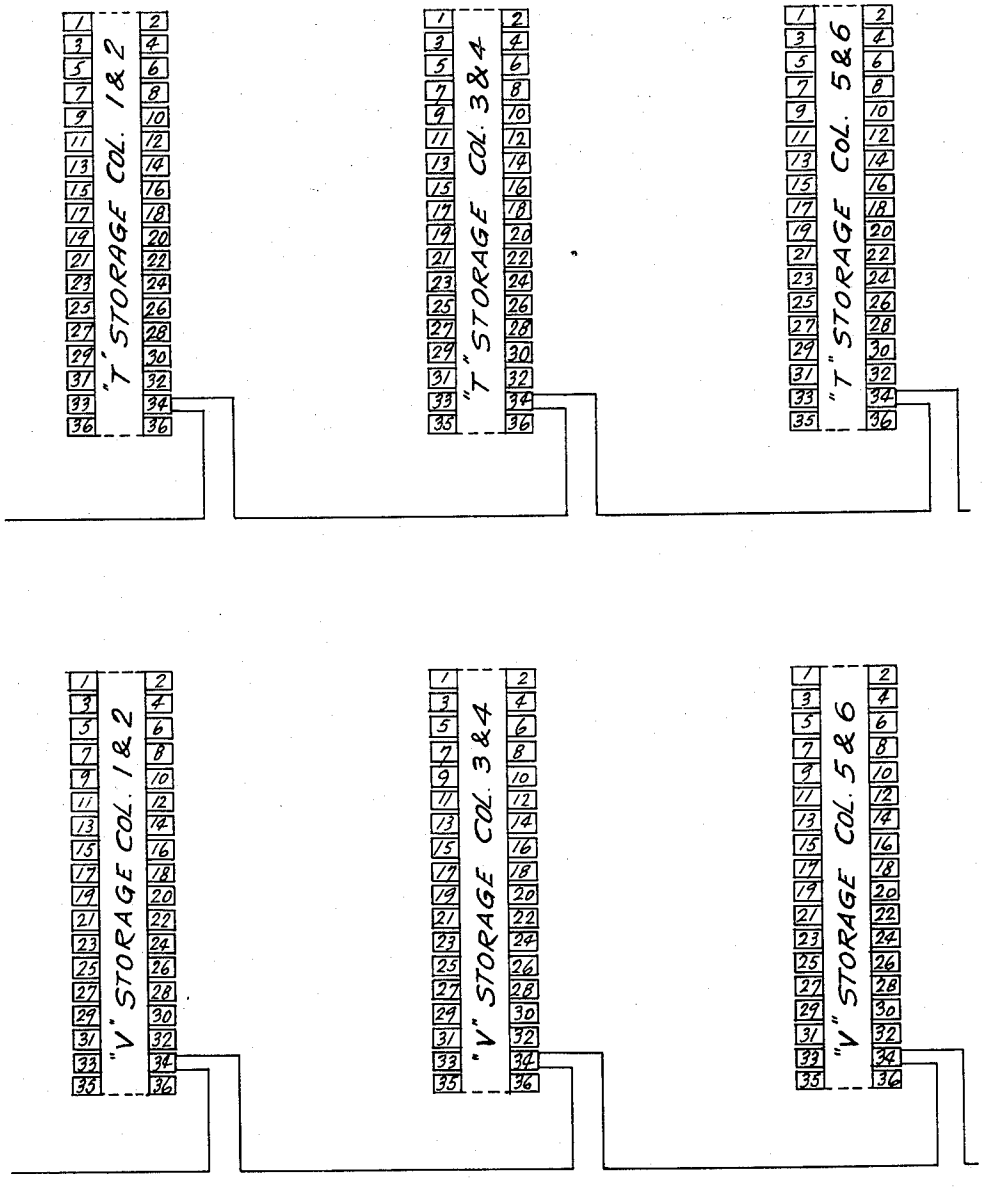


FIG. 36K

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

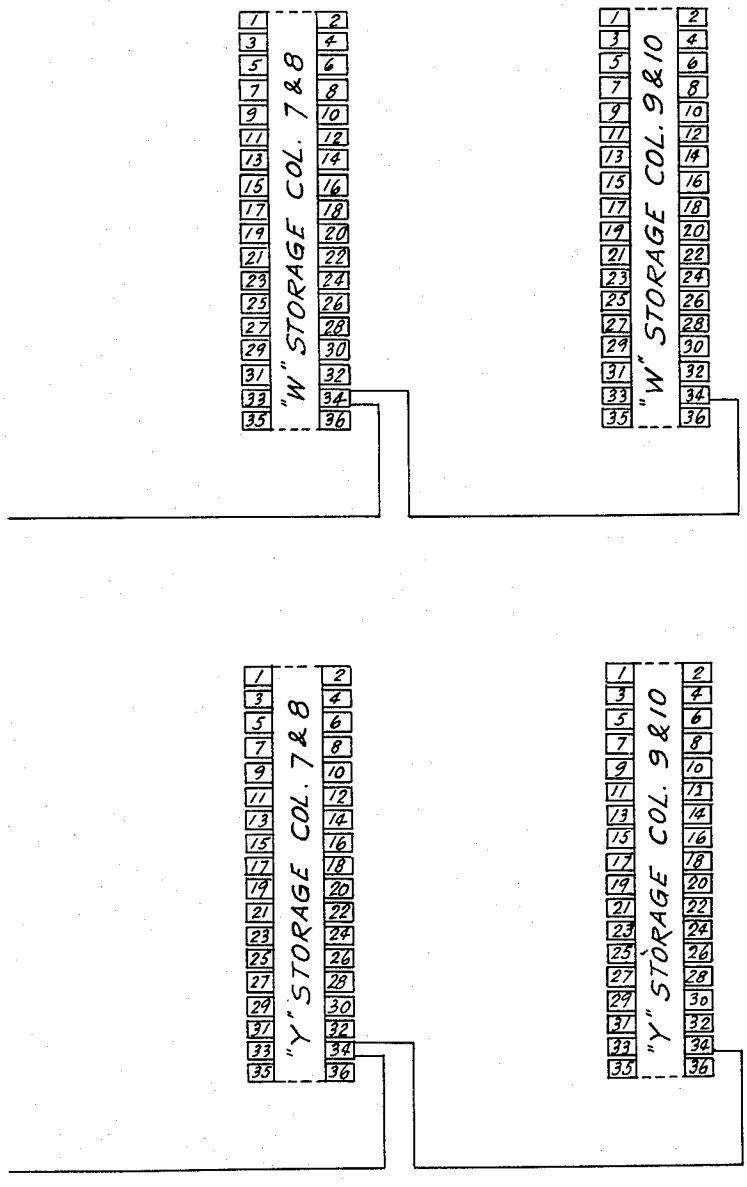


FIG. 36l

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 118

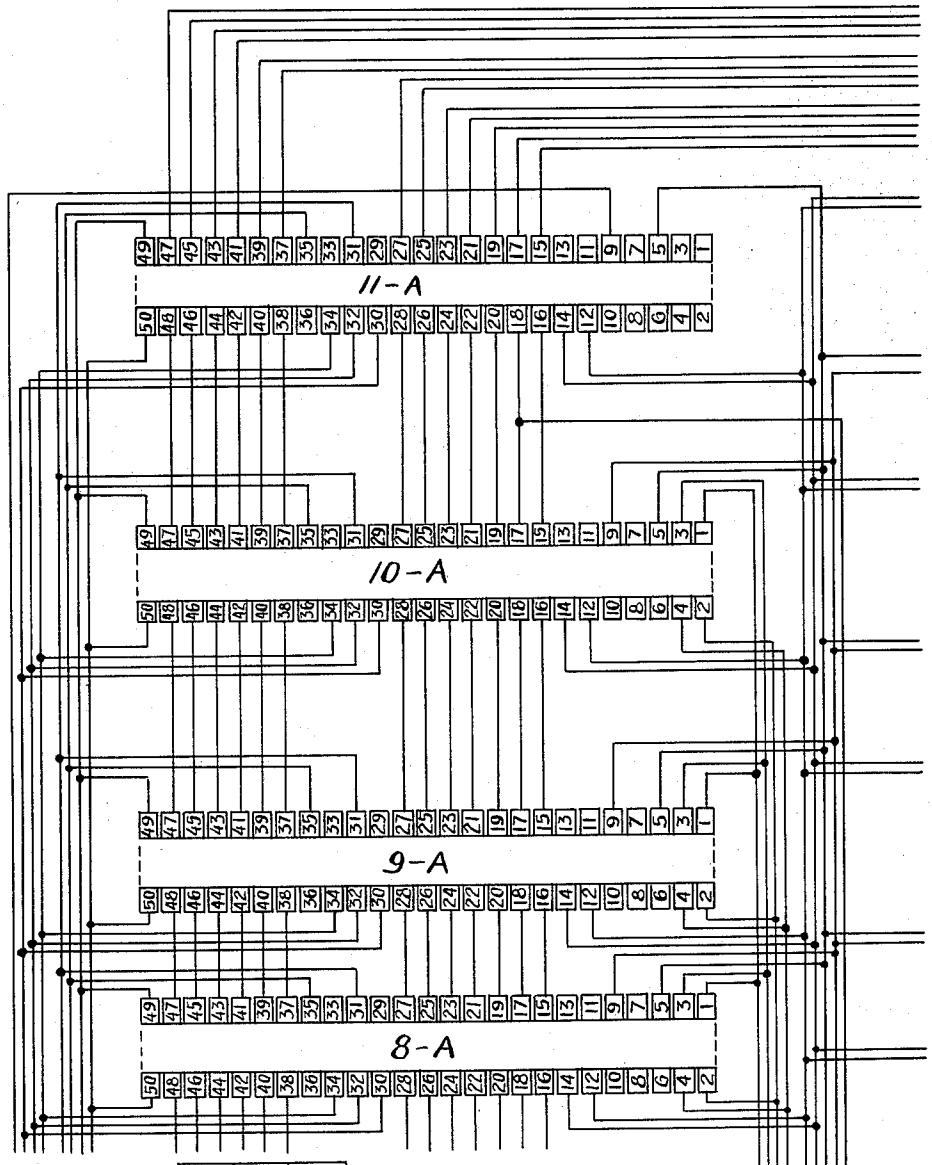


FIG. 37a	FIG. 37b	FIG. 37c
FIG. 37d	FIG. 37e	FIG. 37f
FIG. 37g	FIG. 37h	FIG. 37i
FIG. 37j	FIG. 37k	FIG. 37l

FIG. 37a

FIG. 37m

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

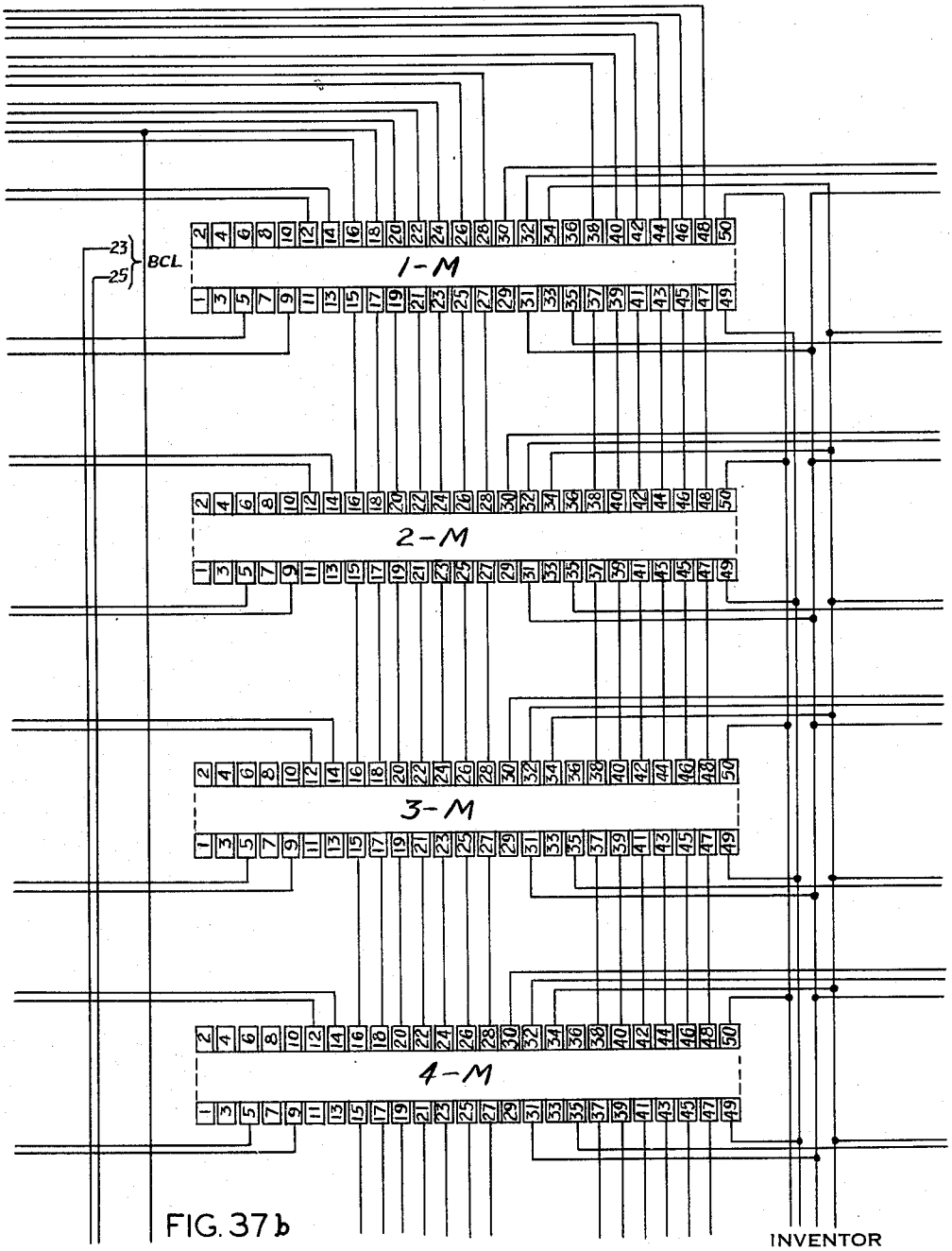


FIG. 37b

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

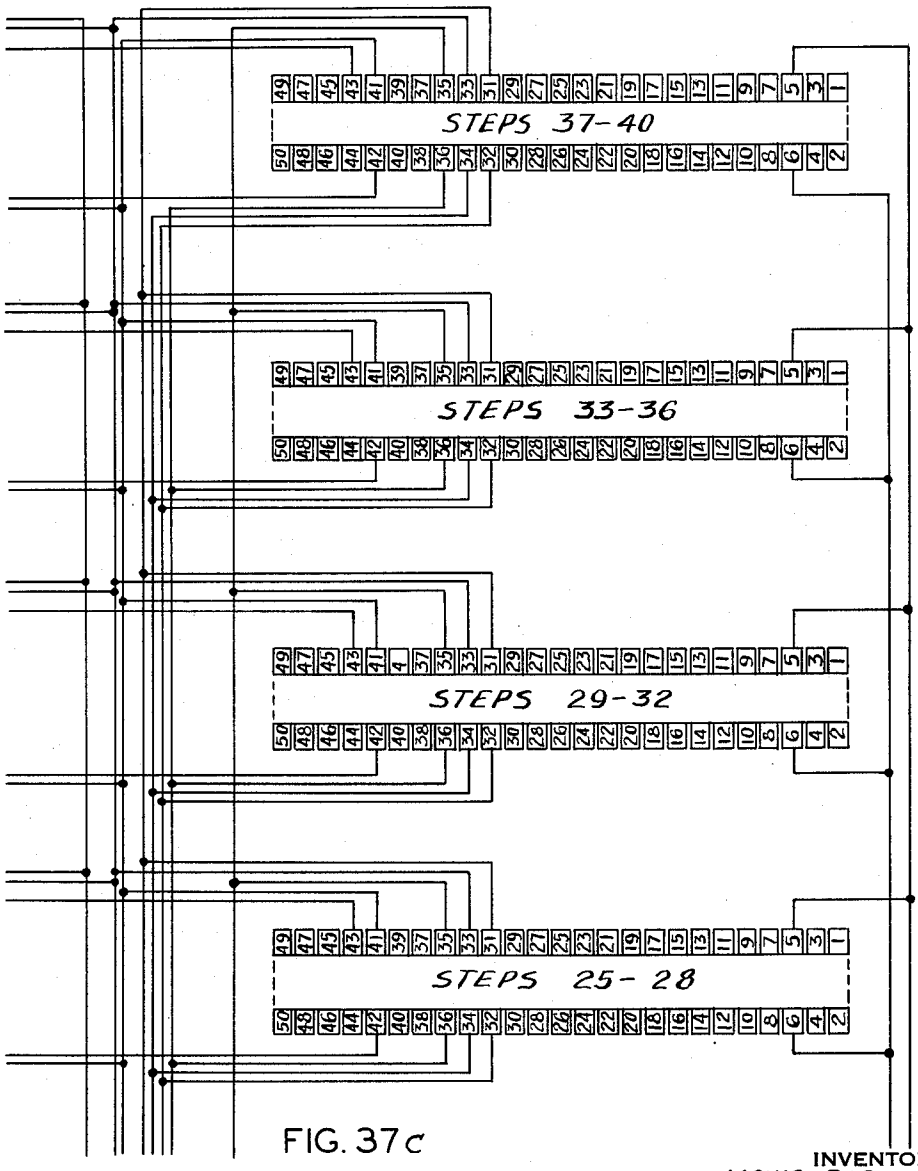


FIG. 37c

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 121

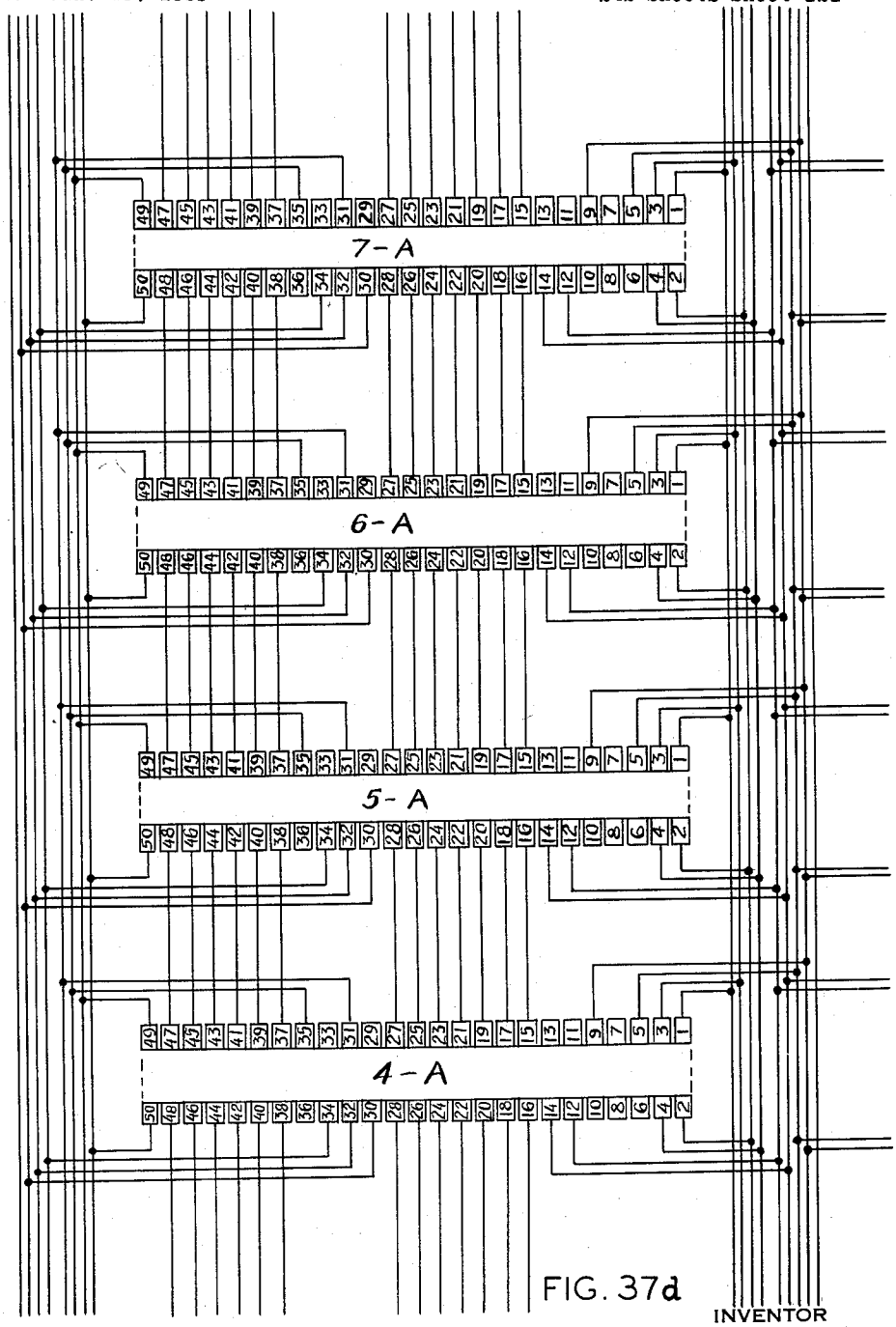


FIG. 37d

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 122

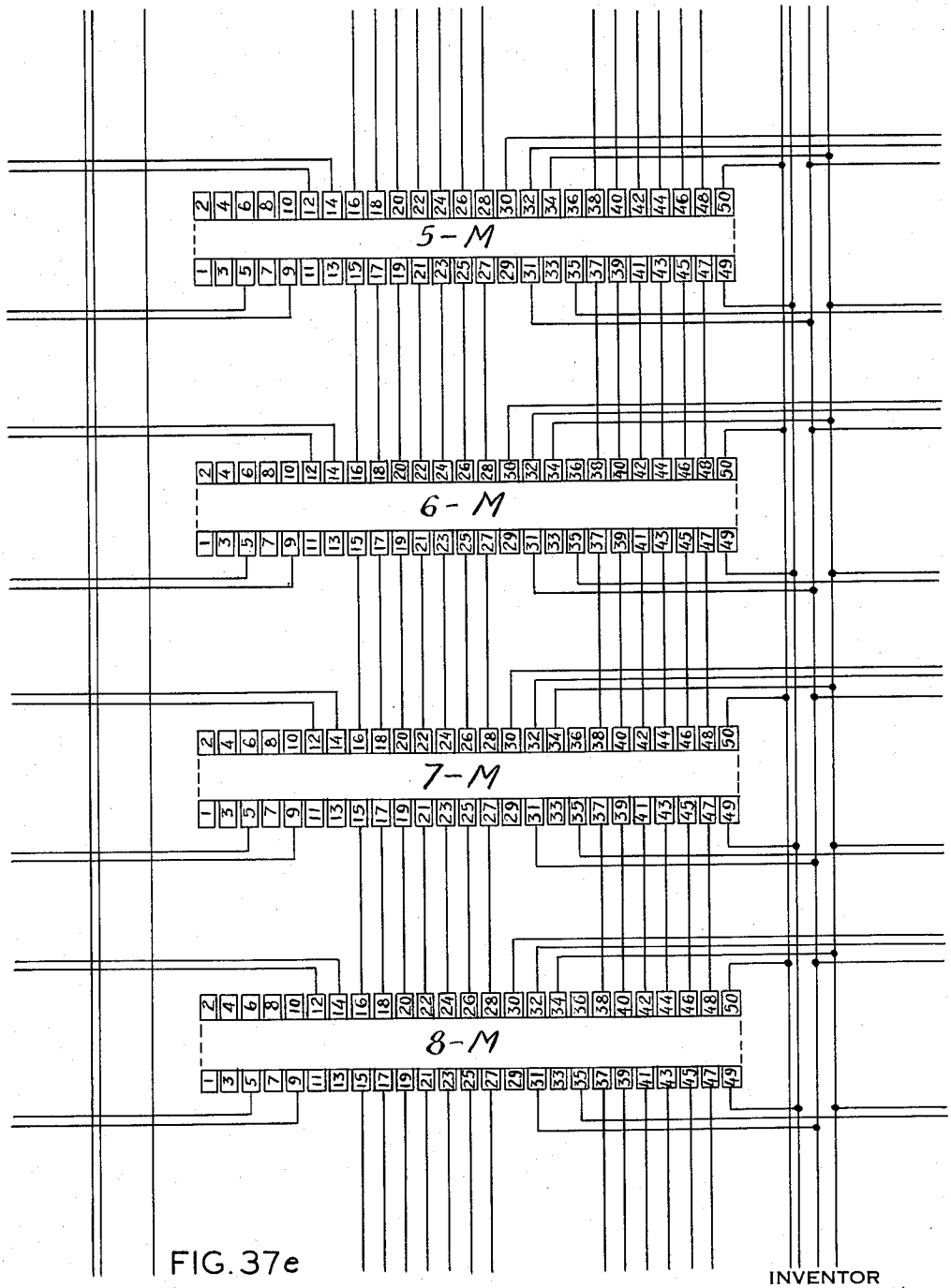


FIG. 37e

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 123

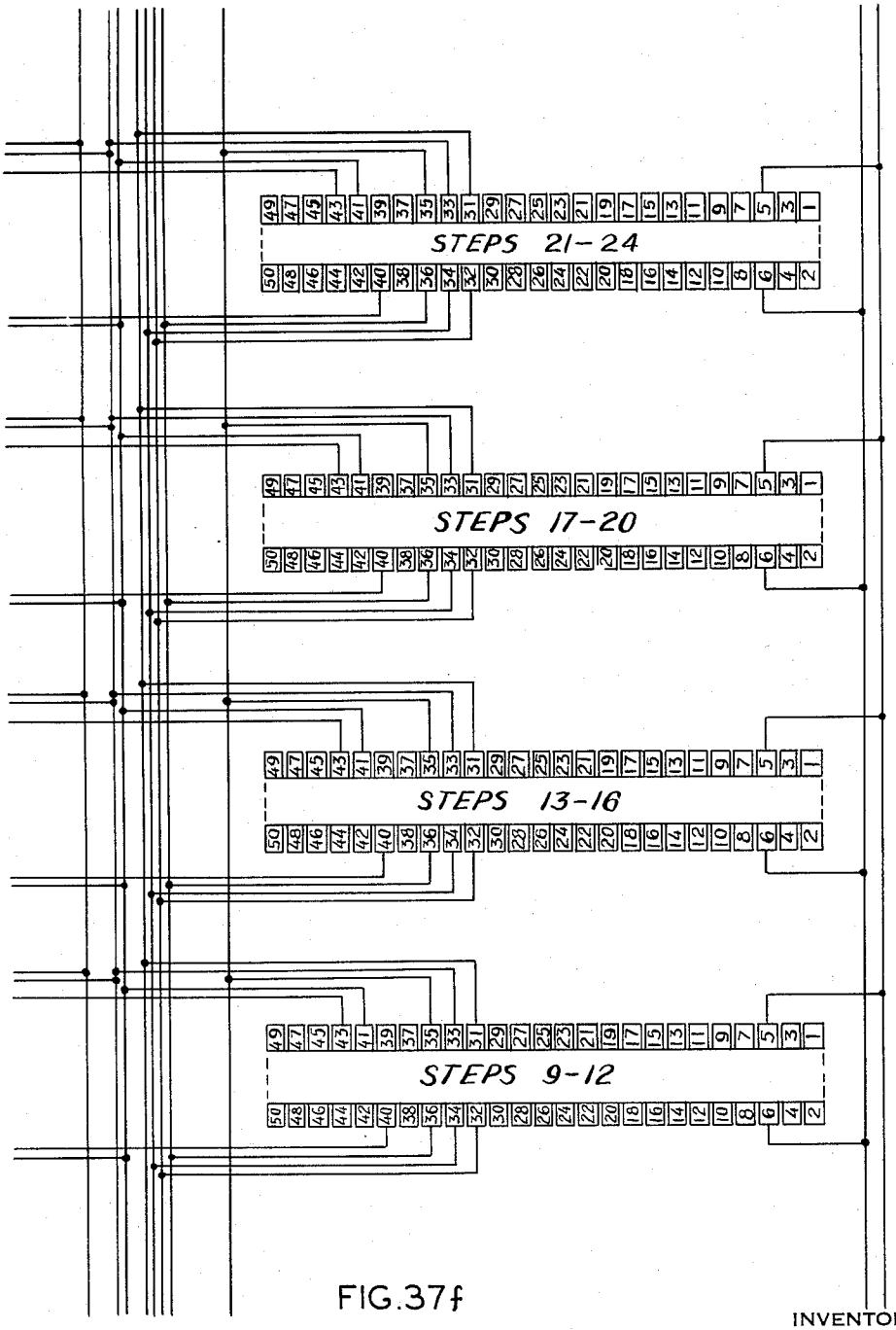


FIG. 37f

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 124

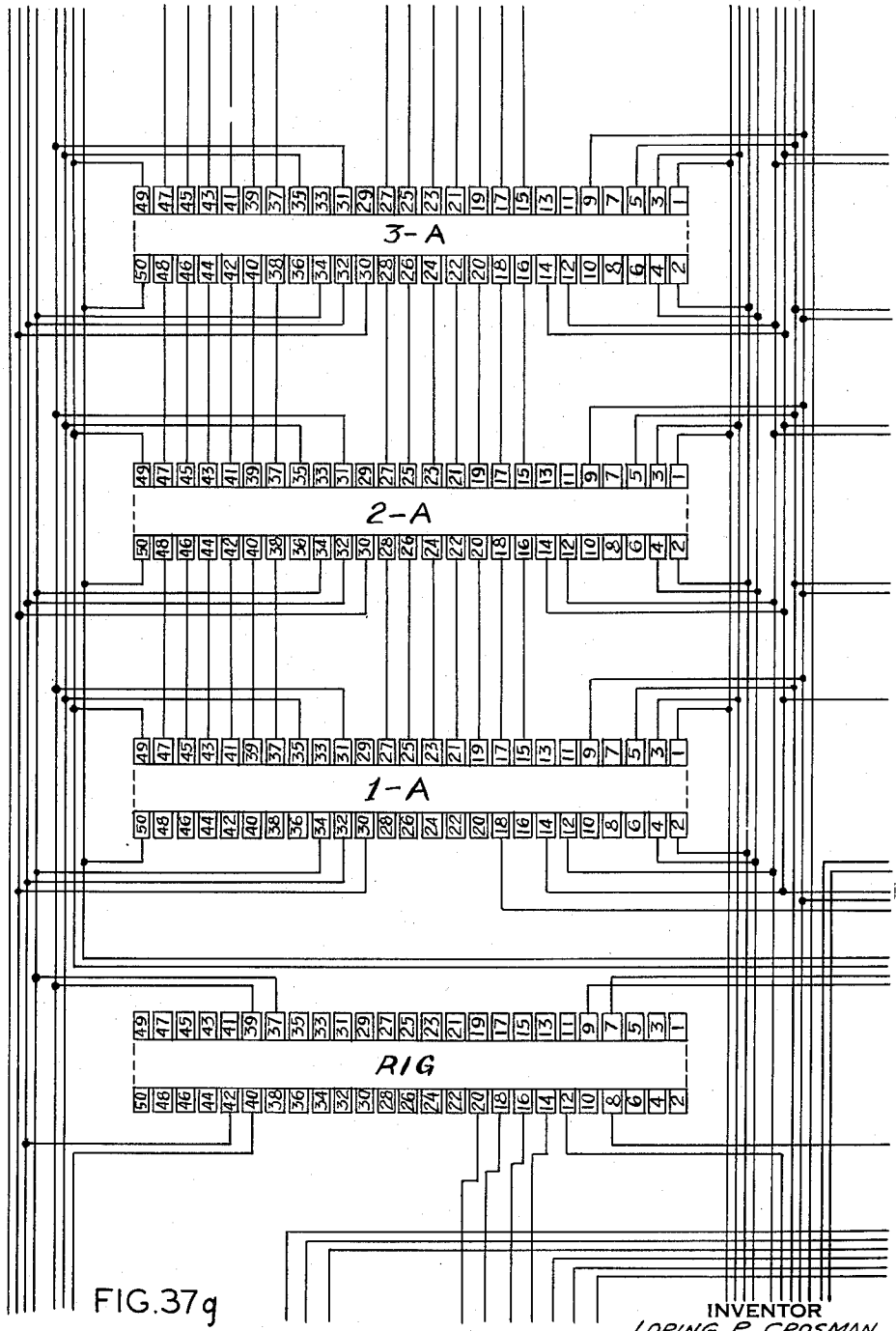


FIG. 37g

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 125

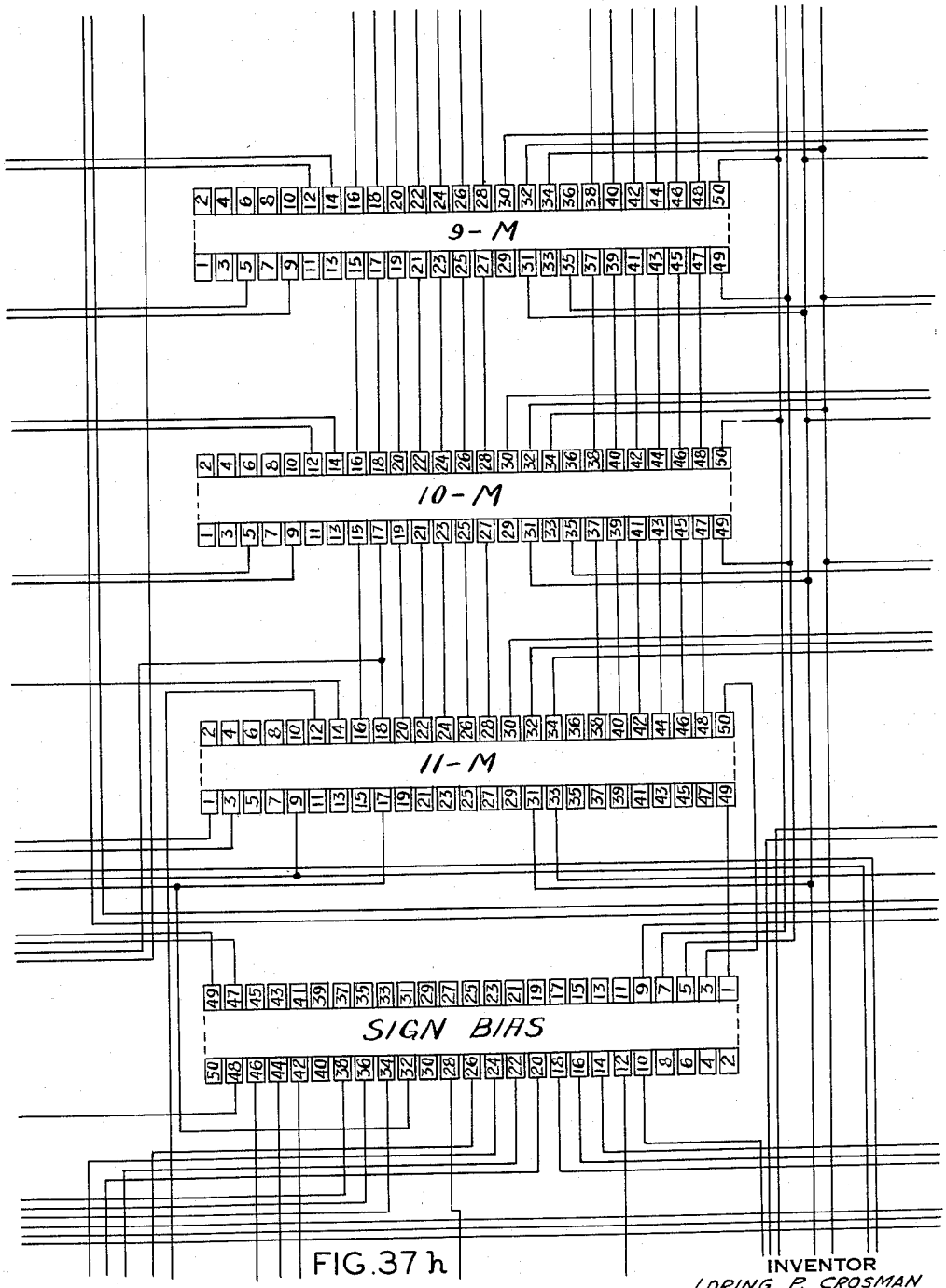


FIG. 37h

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

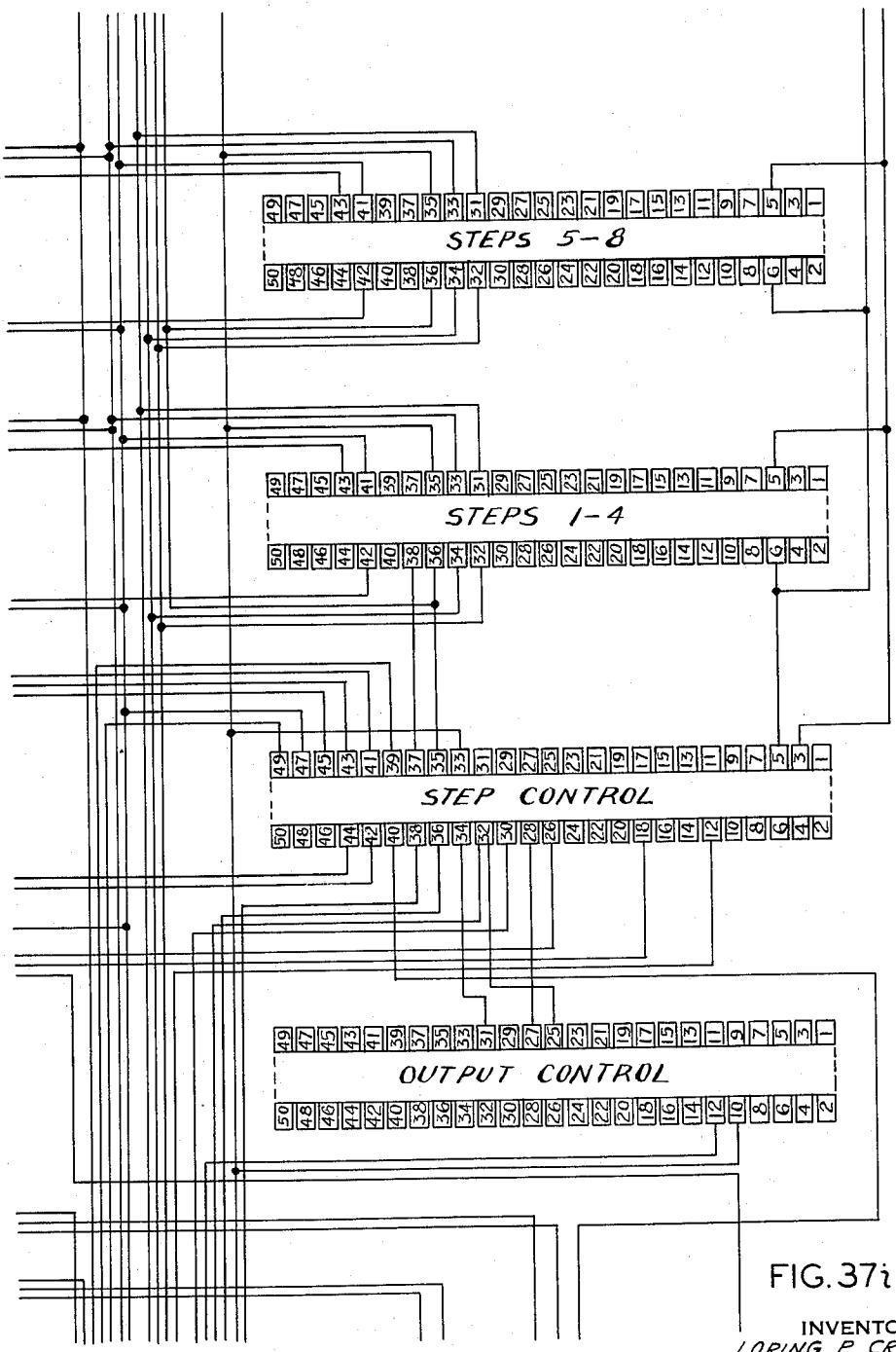


FIG. 37i

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 127

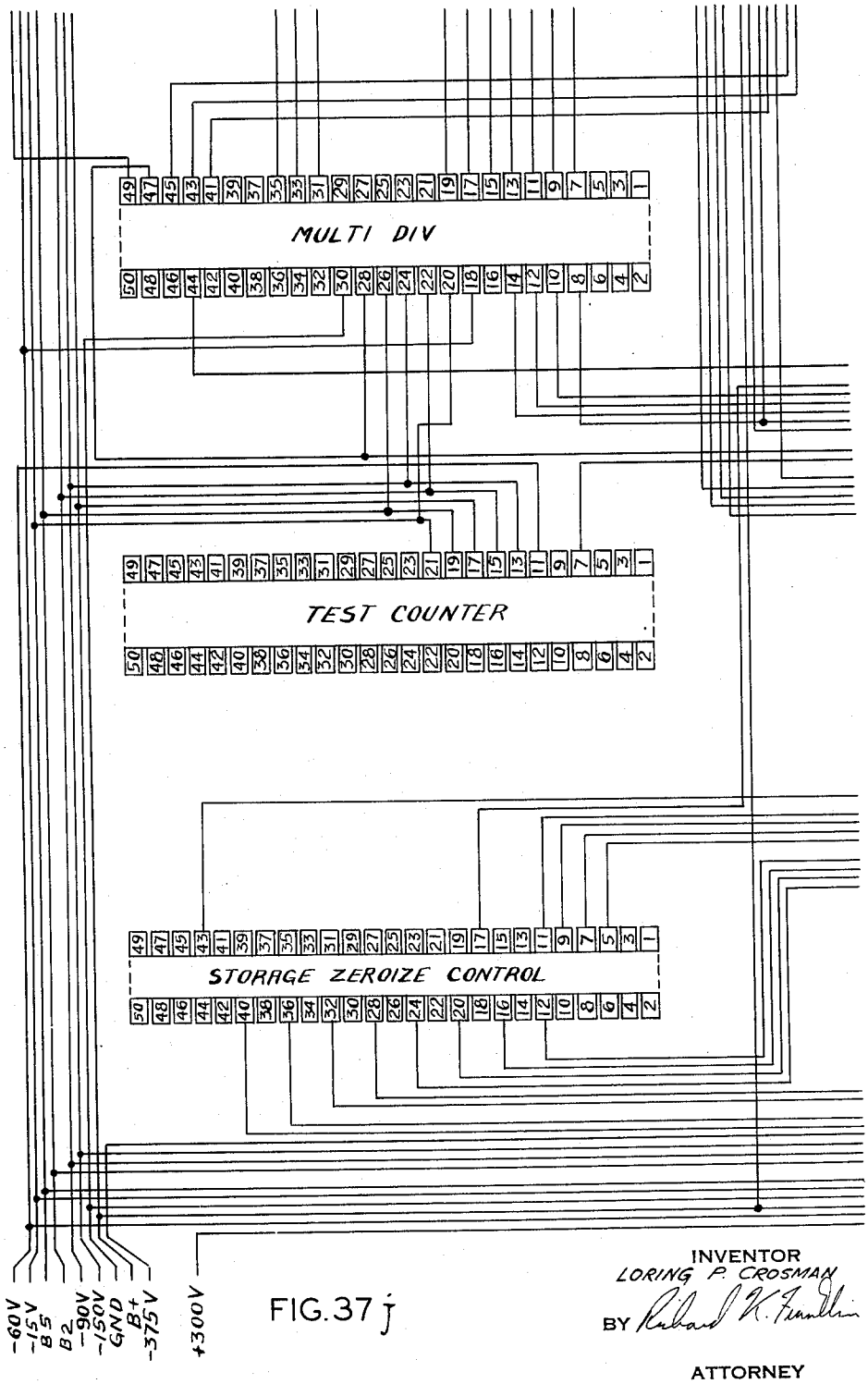


FIG. 37j

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 128

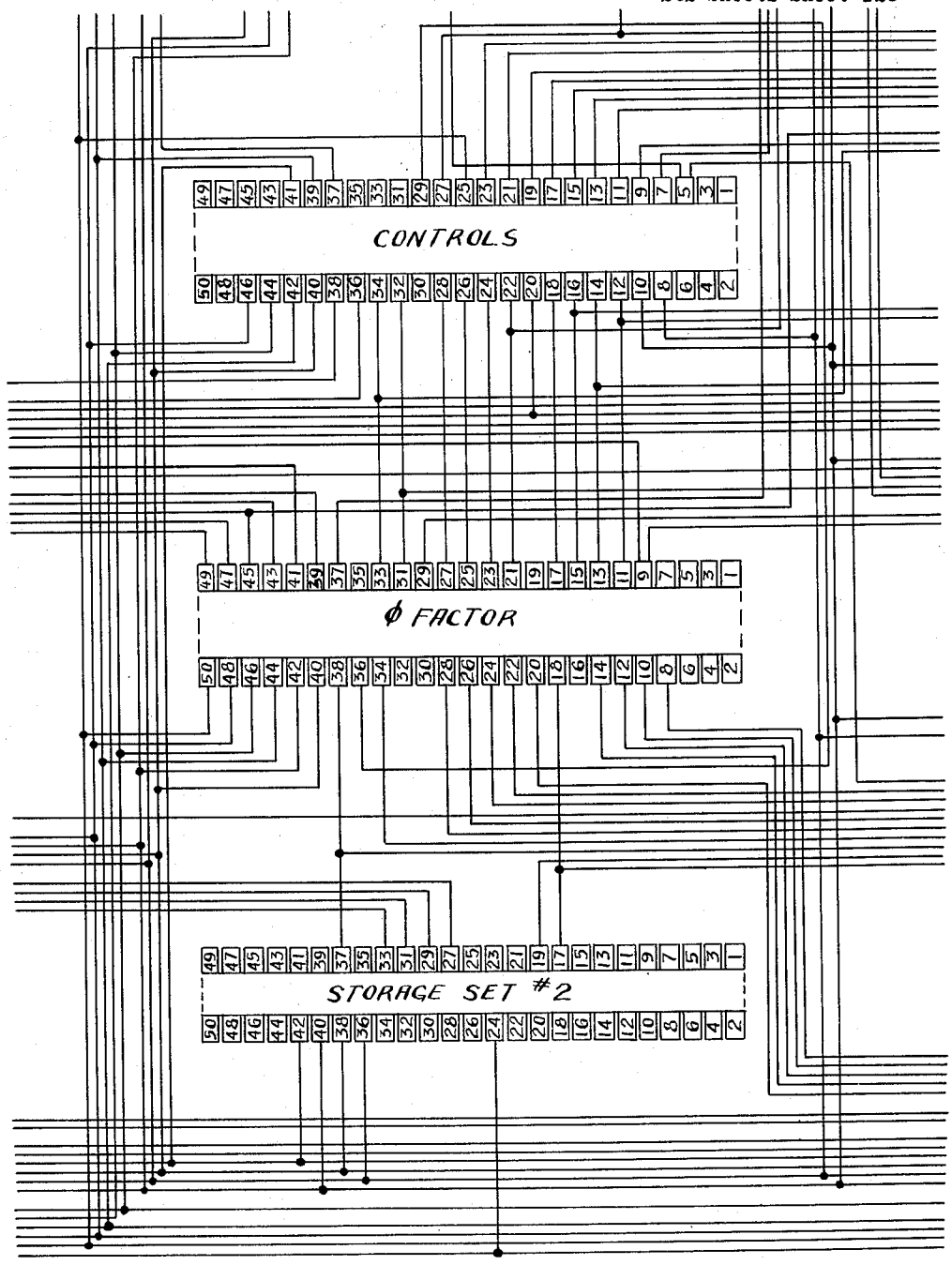


FIG. 37K

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 129

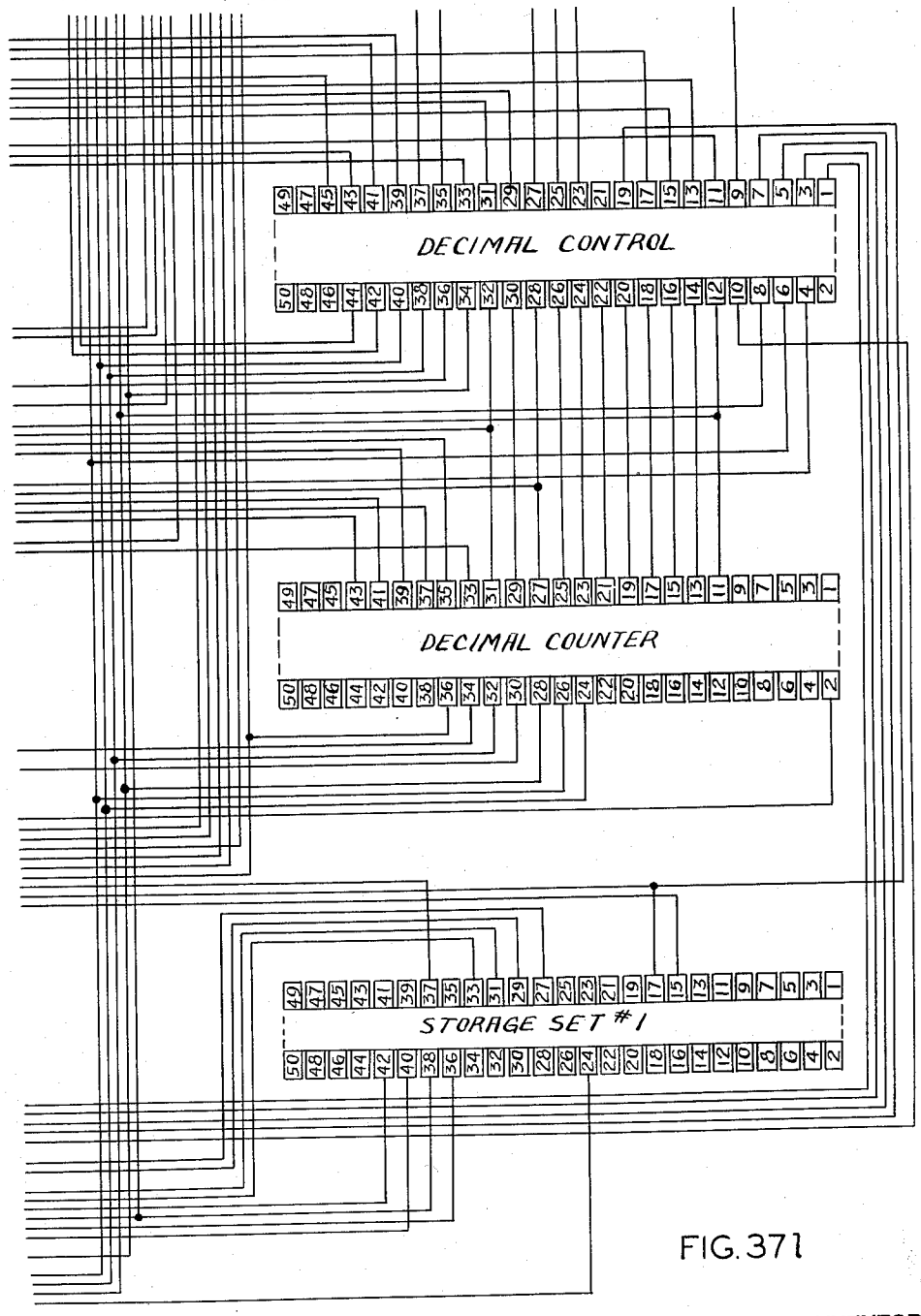


FIG. 371

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 130

FIG. 38a

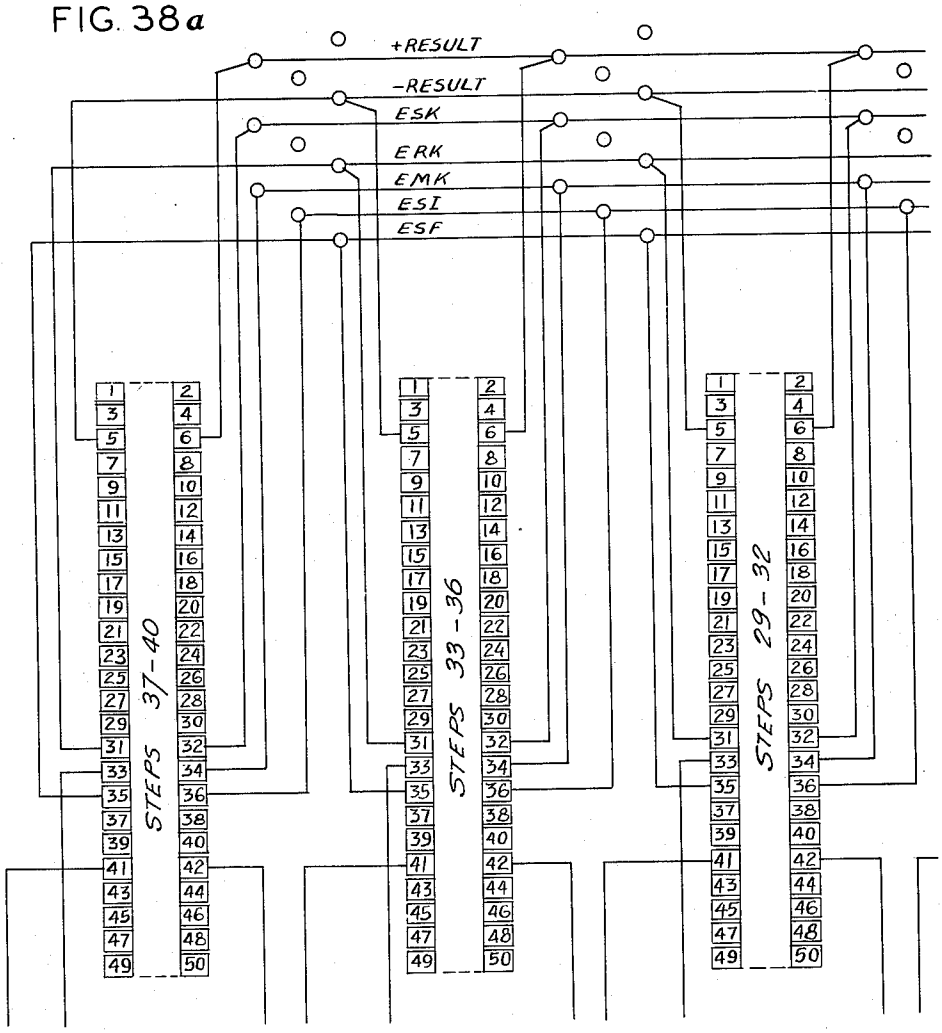


FIG. 38a	FIG. 38b	FIG. 38c	FIG. 38d	FIG. 38e
FIG. 38f	FIG. 38g	FIG. 38h	FIG. 38i	FIG. 38j
FIG. 38k	FIG. 38l	FIG. 38m	FIG. 38n	FIG. 38o

FIG. 38p

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 131

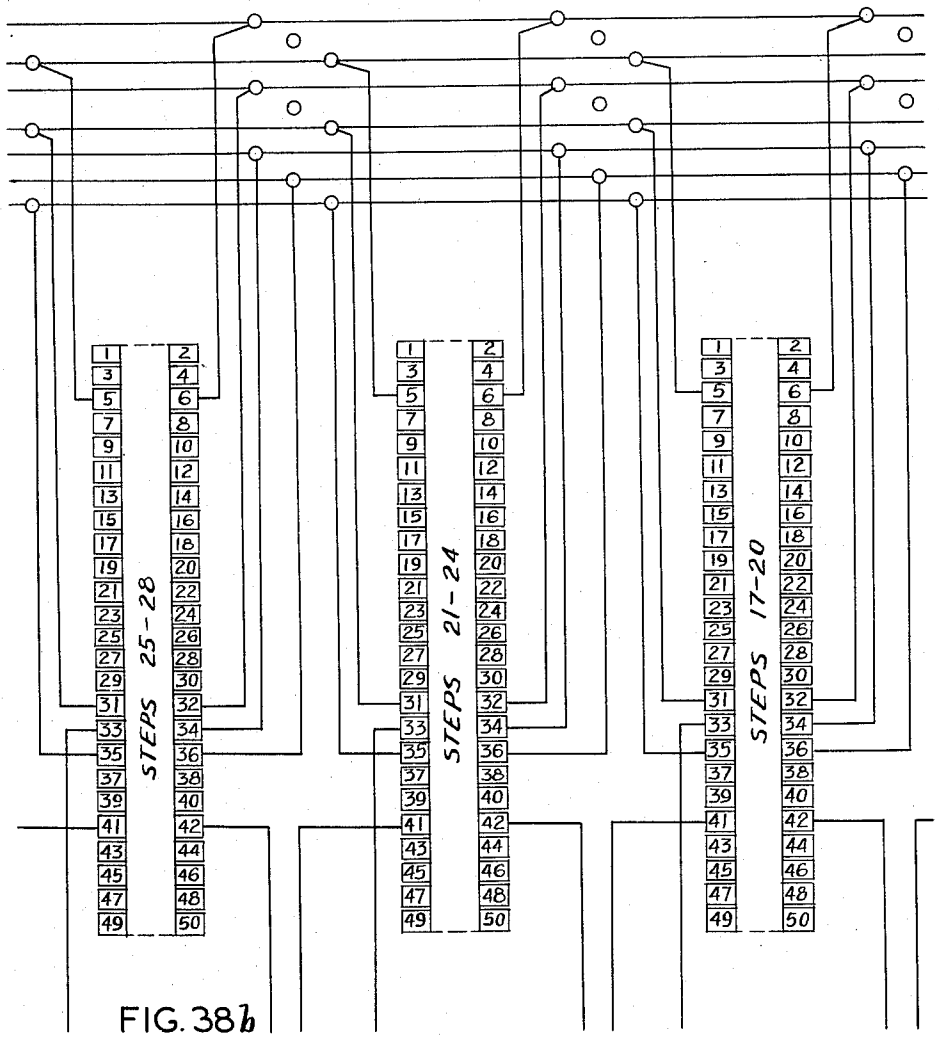


FIG. 38b

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 132

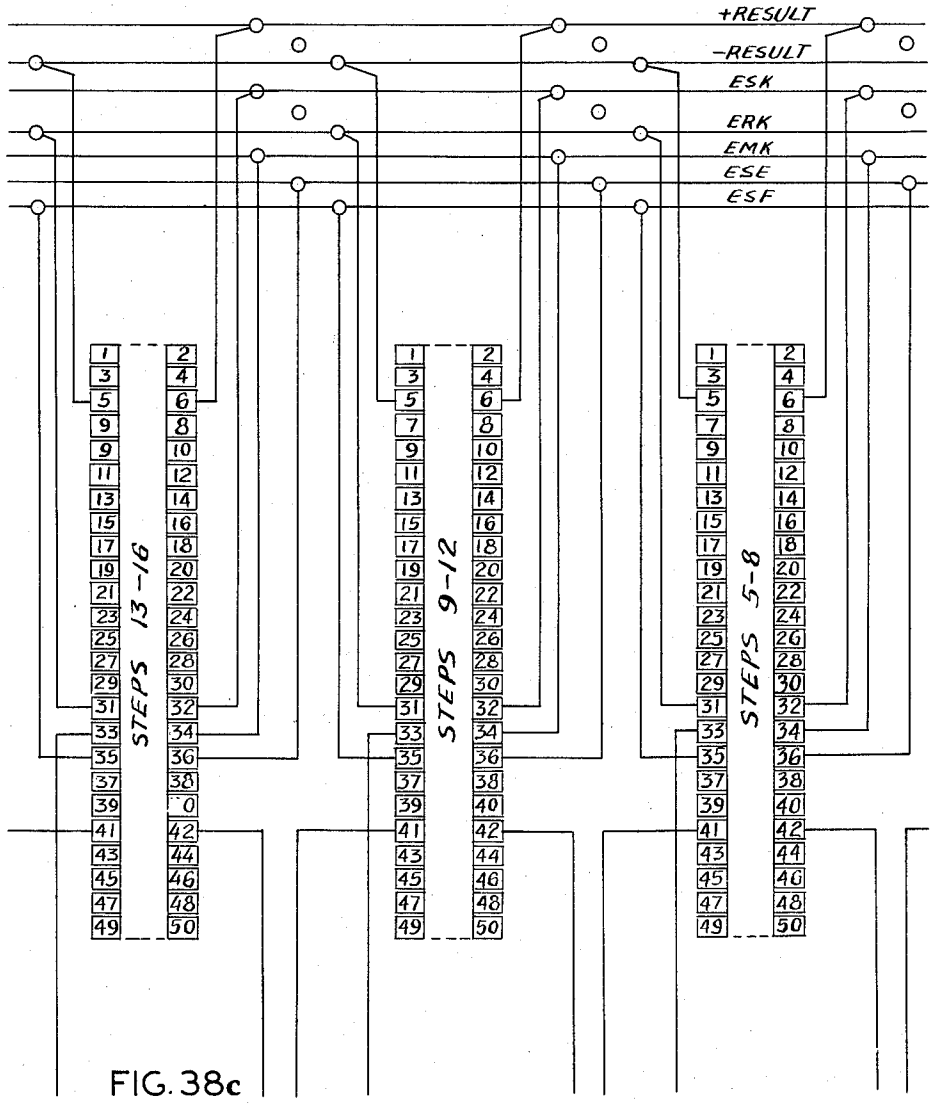


FIG. 38c

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 133

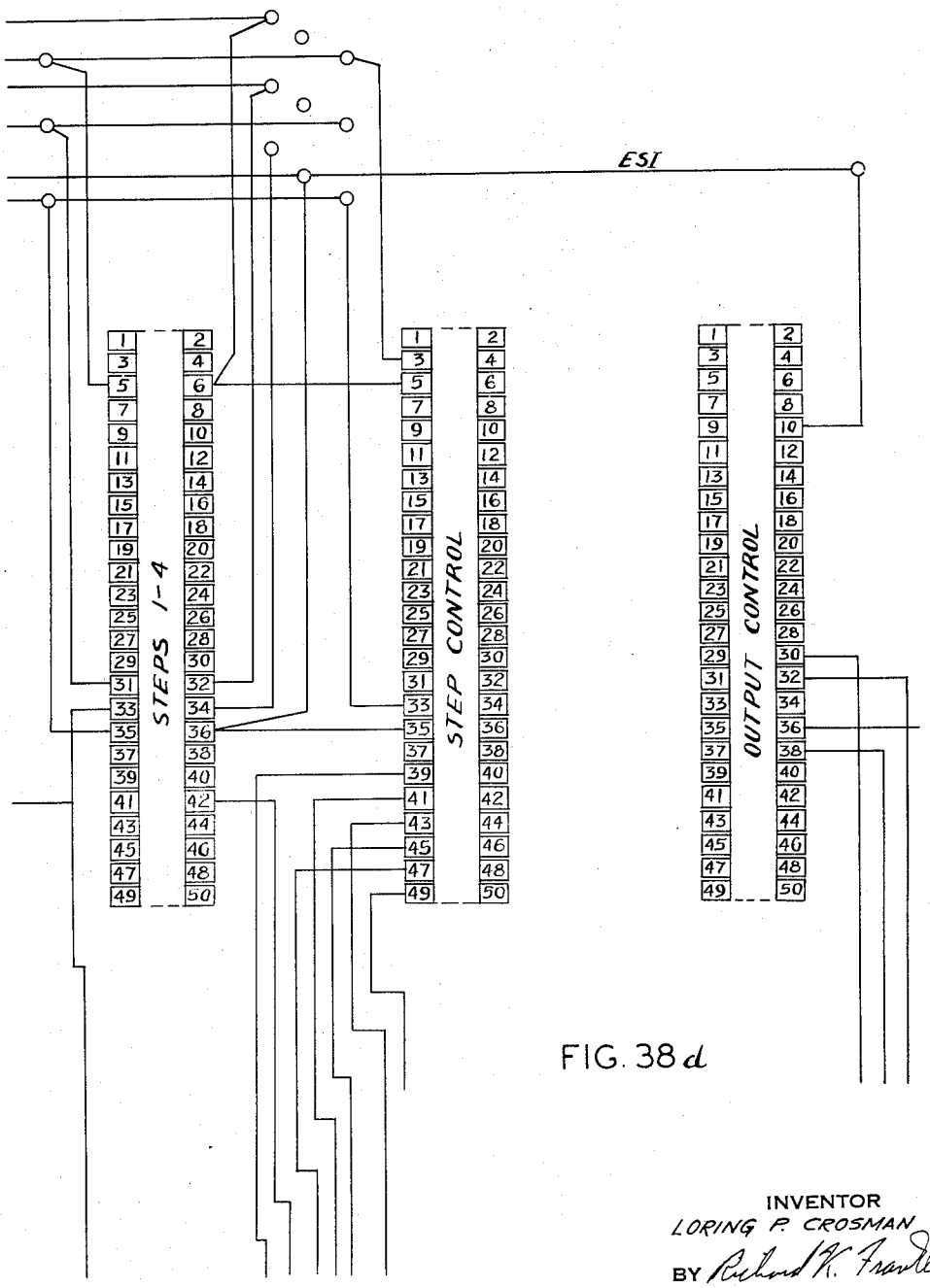


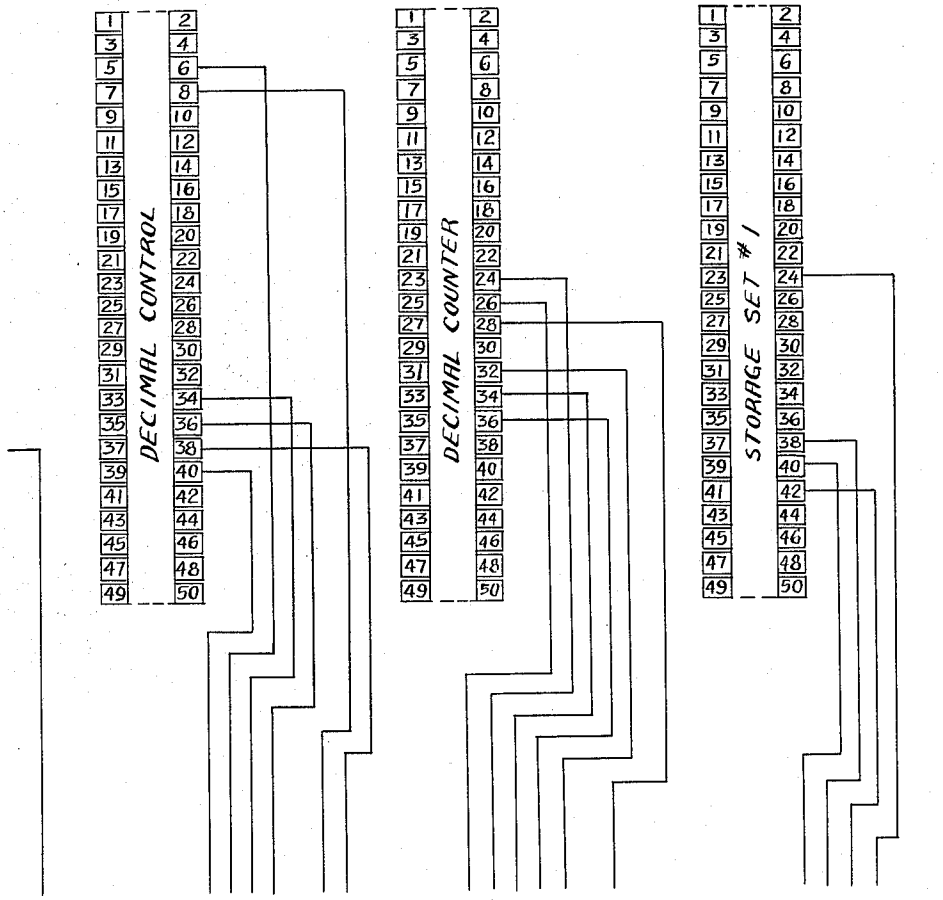
FIG. 38d

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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FIG. 38e



INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 135

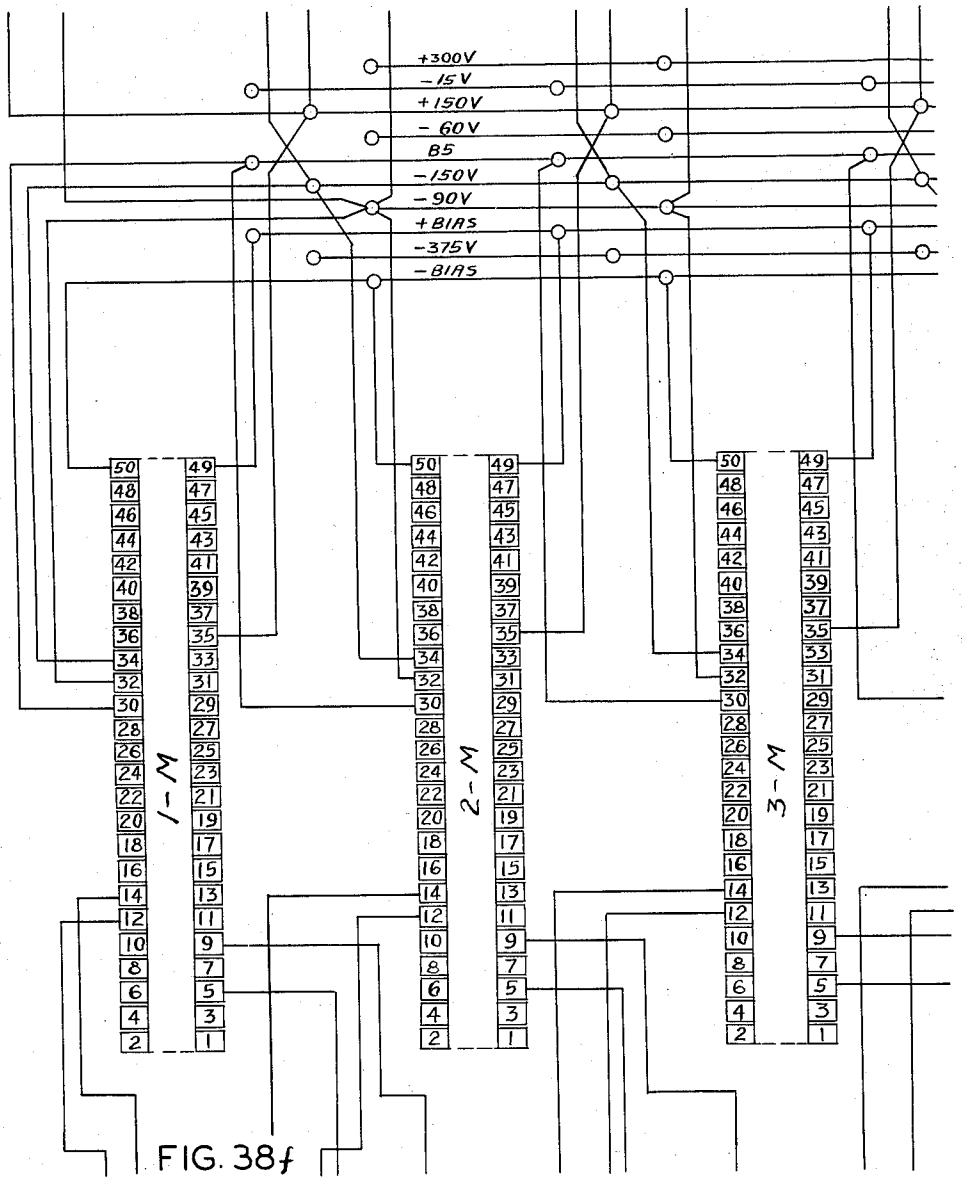


FIG. 38f

INVENTOR
LORING P. CROSMAN
BY Richard M. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 136

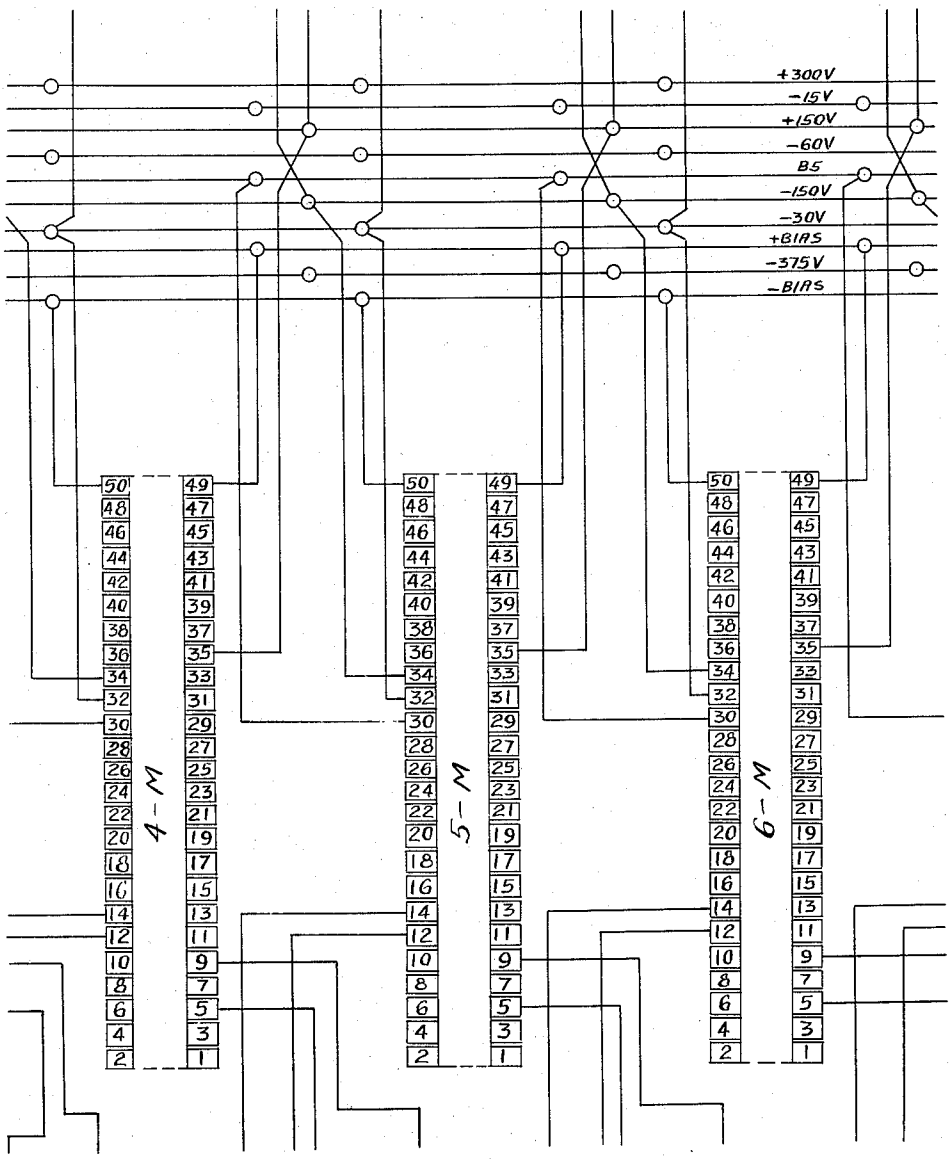


FIG. 38g

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 137

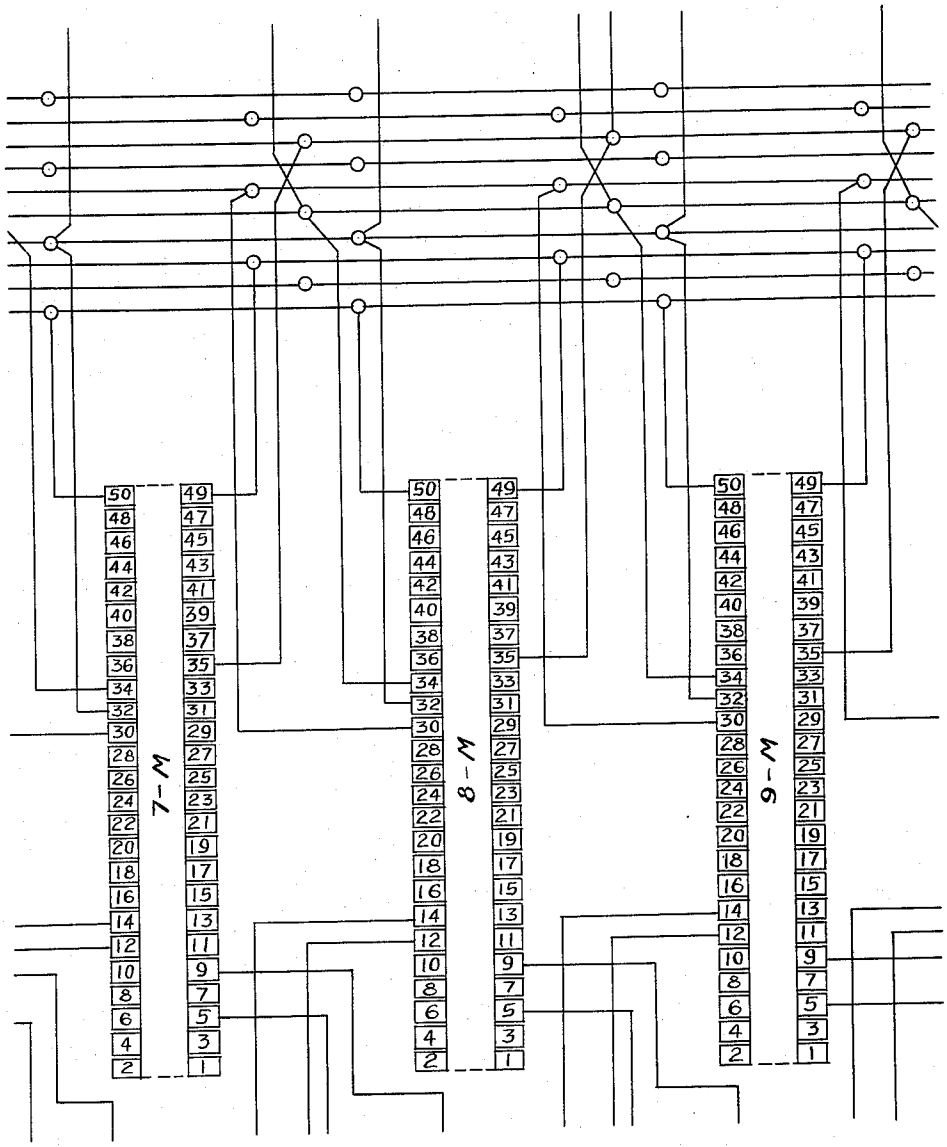


FIG. 38h

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 138

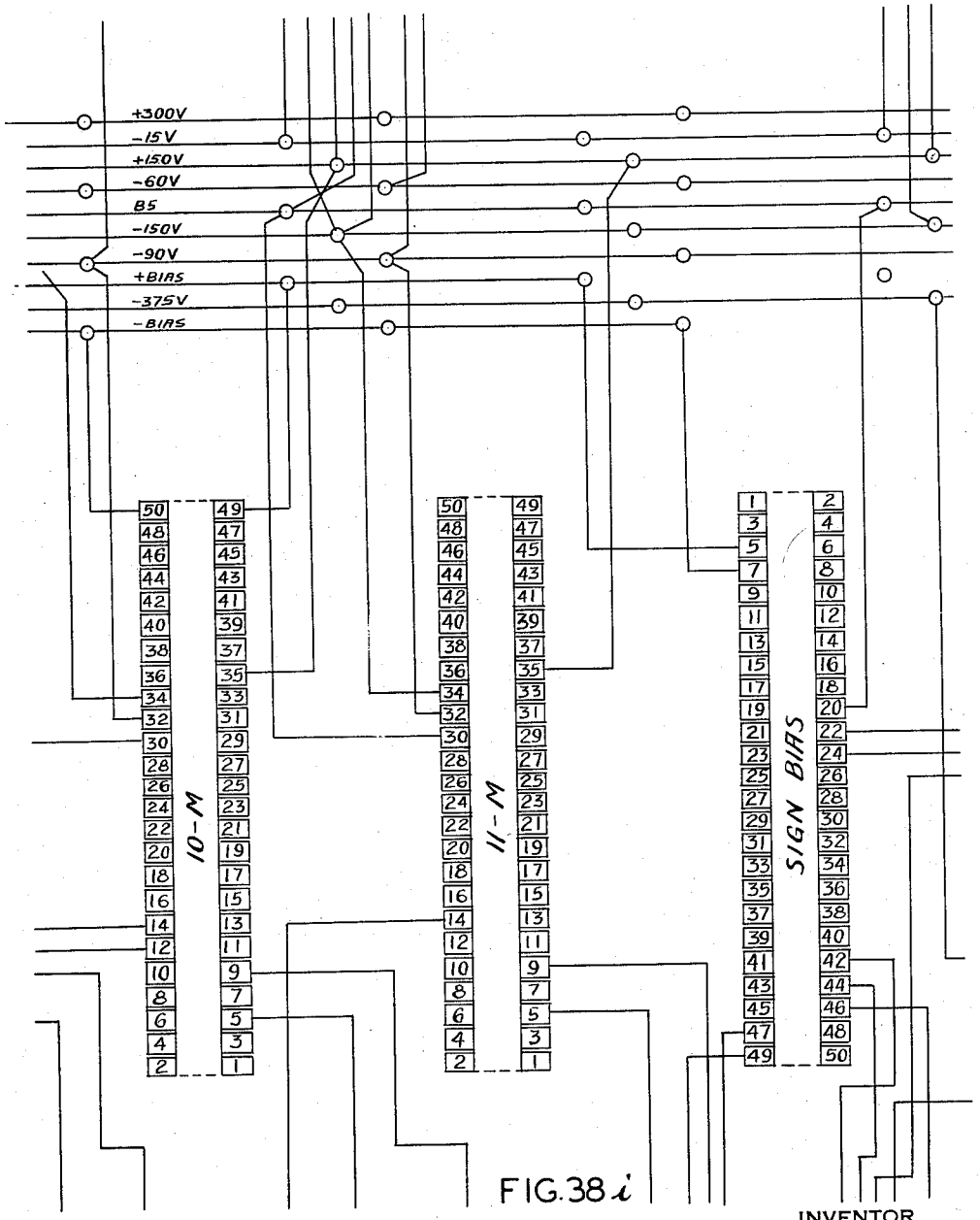


FIG. 38i

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 139

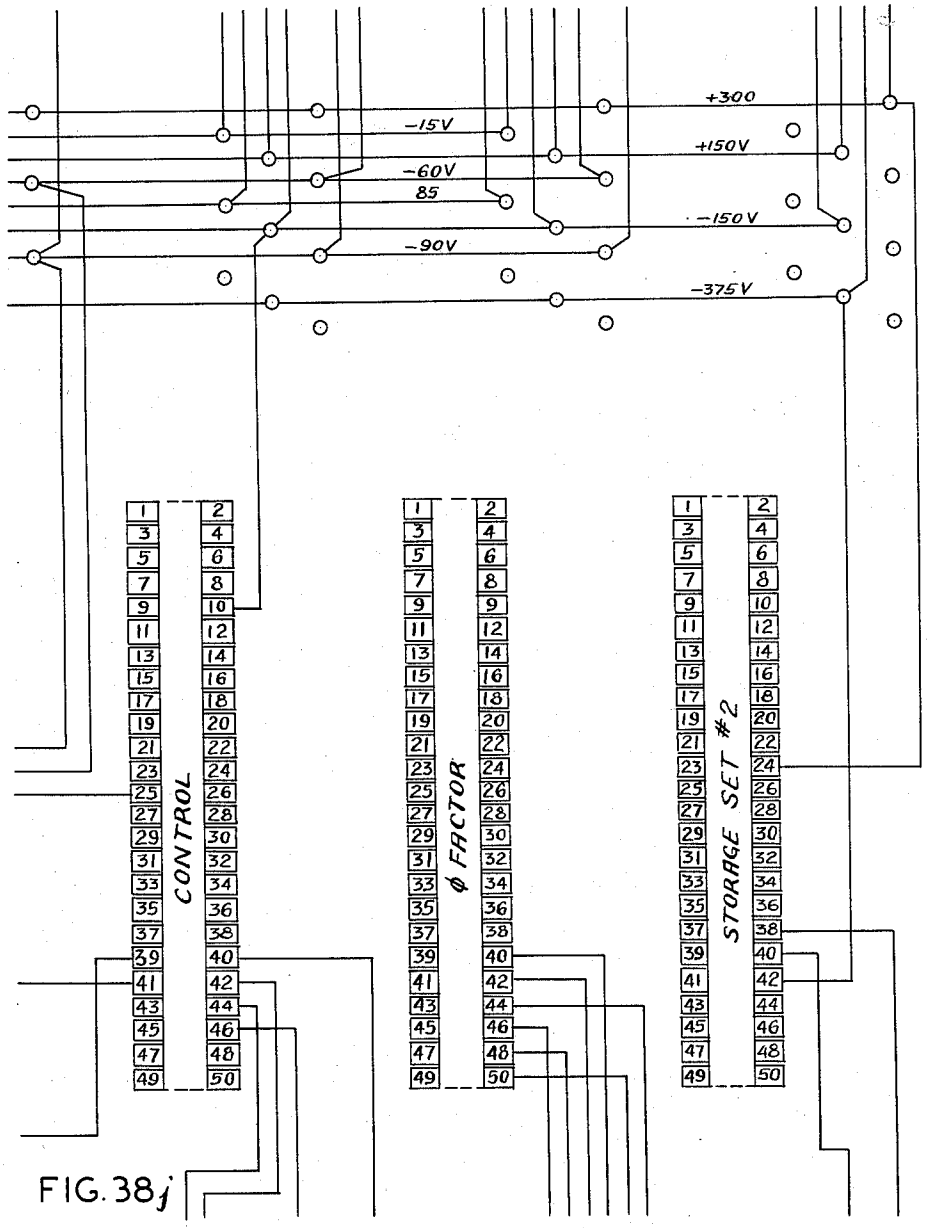


FIG. 38j

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 140

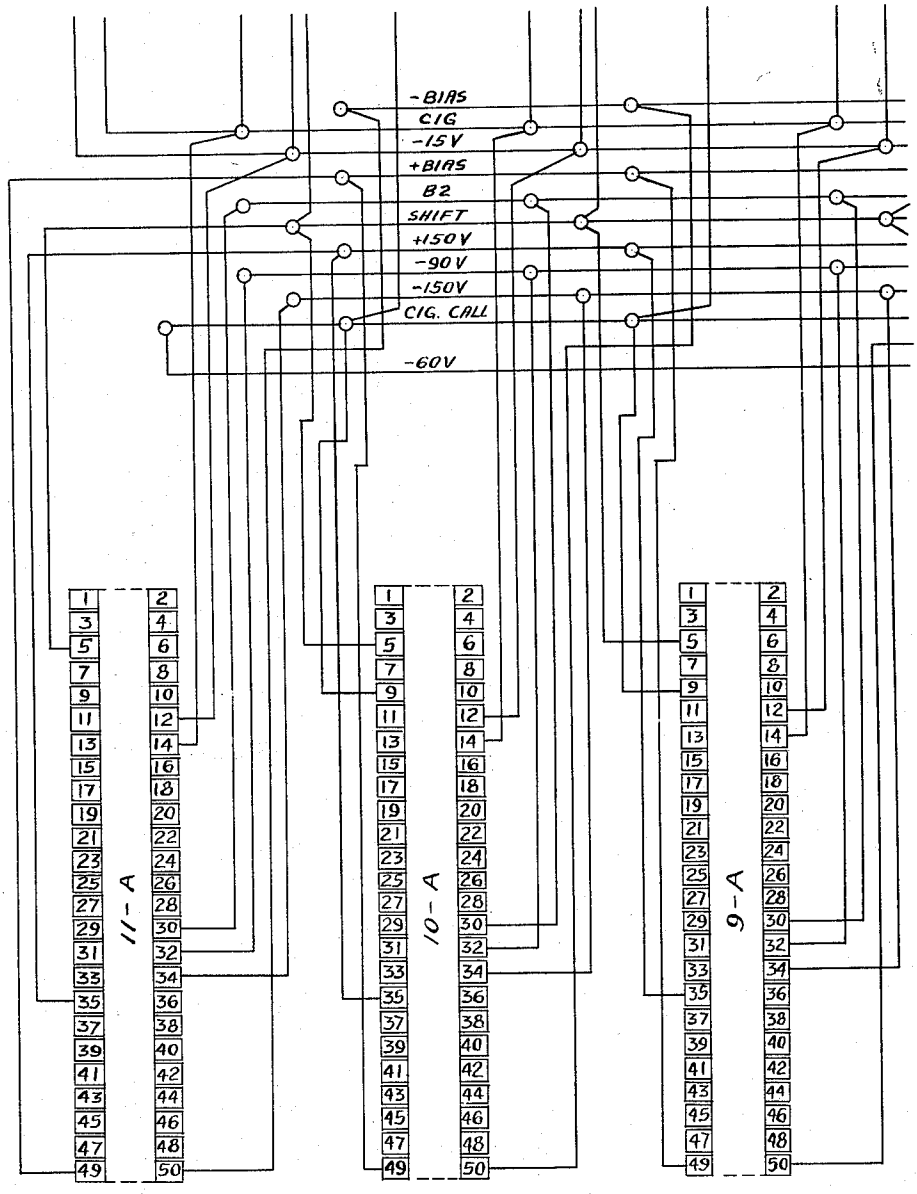


FIG. 38K

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 141

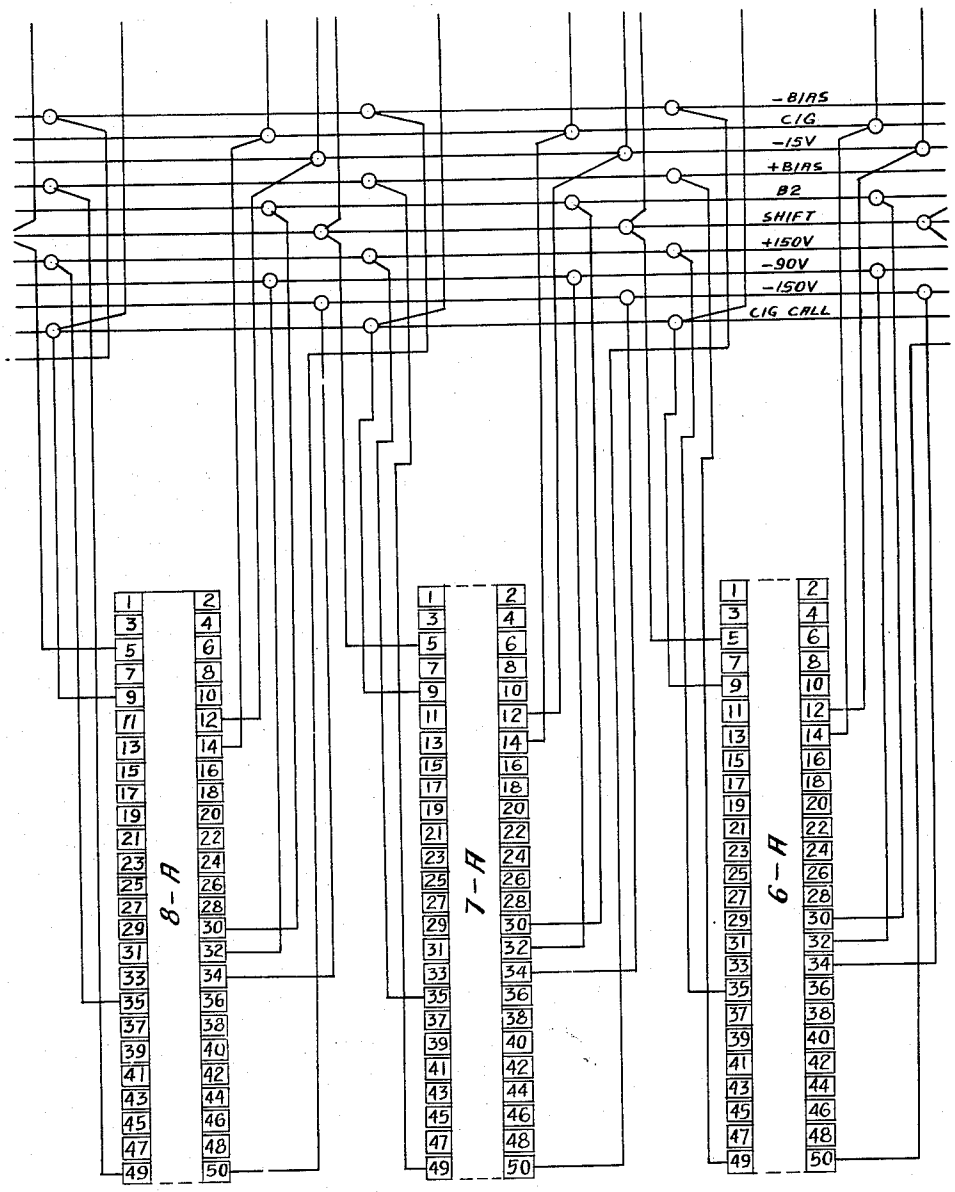


FIG. 38l

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 142

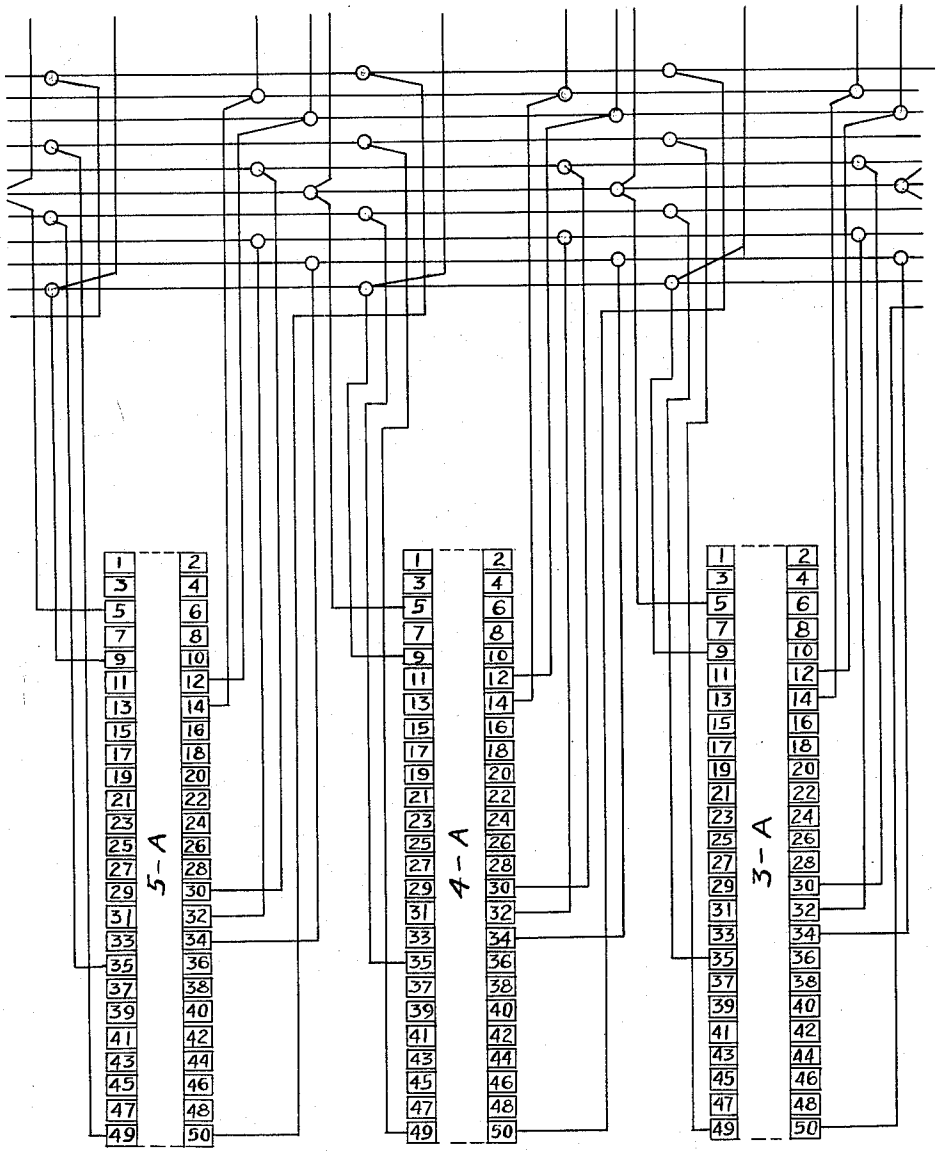


FIG. 38m

INVENTOR
LORING P. CROSMAN
BY Richard M. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 143

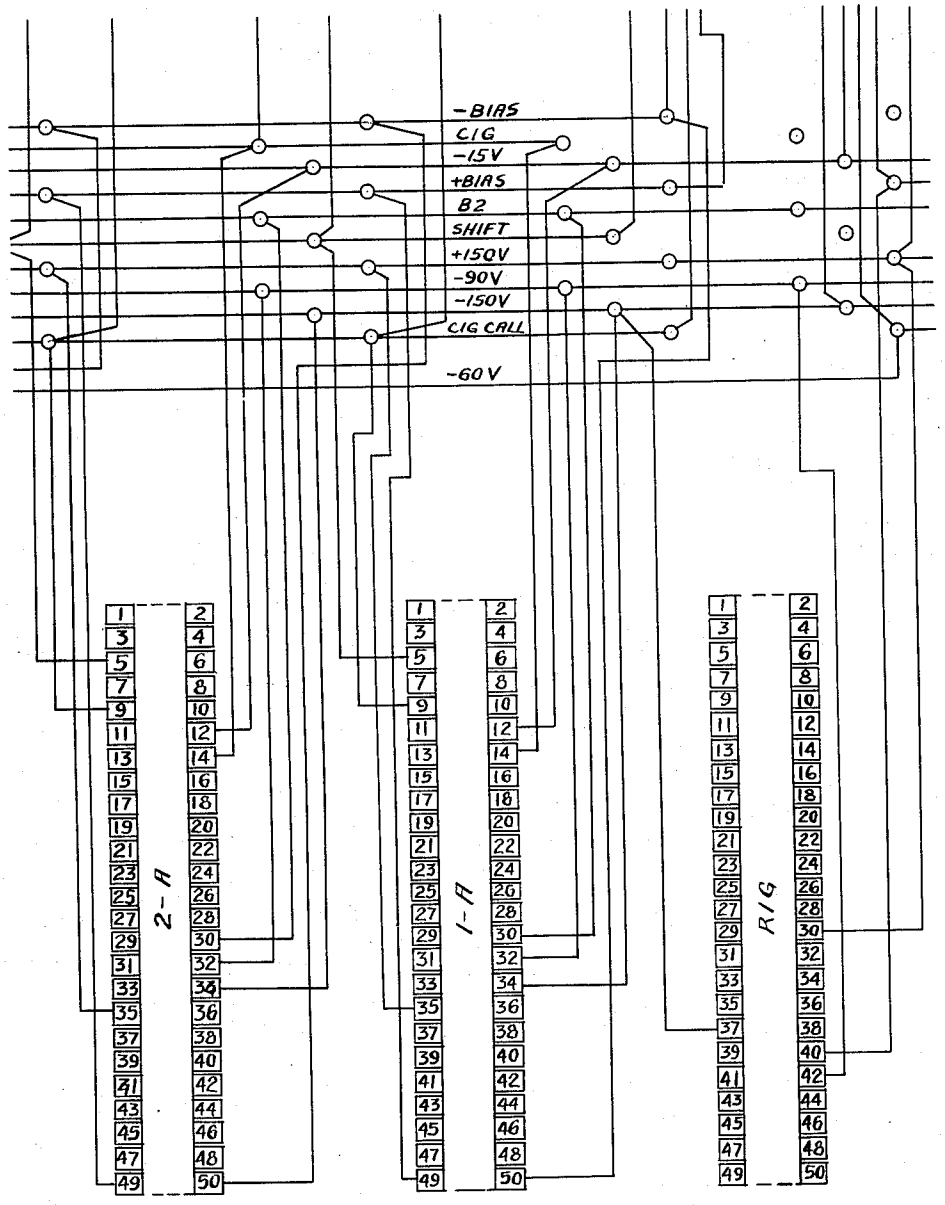


FIG. 38n

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 144

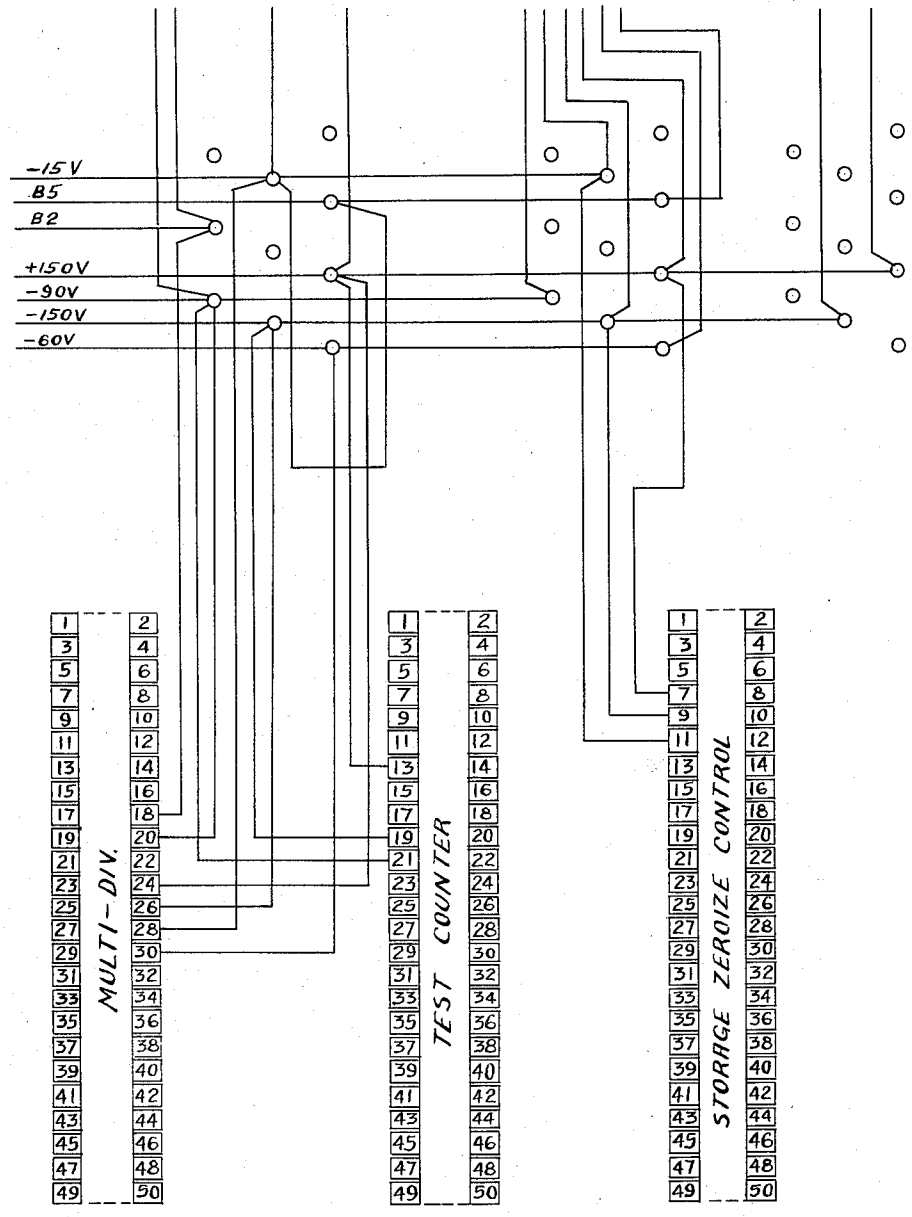


FIG. 38o

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

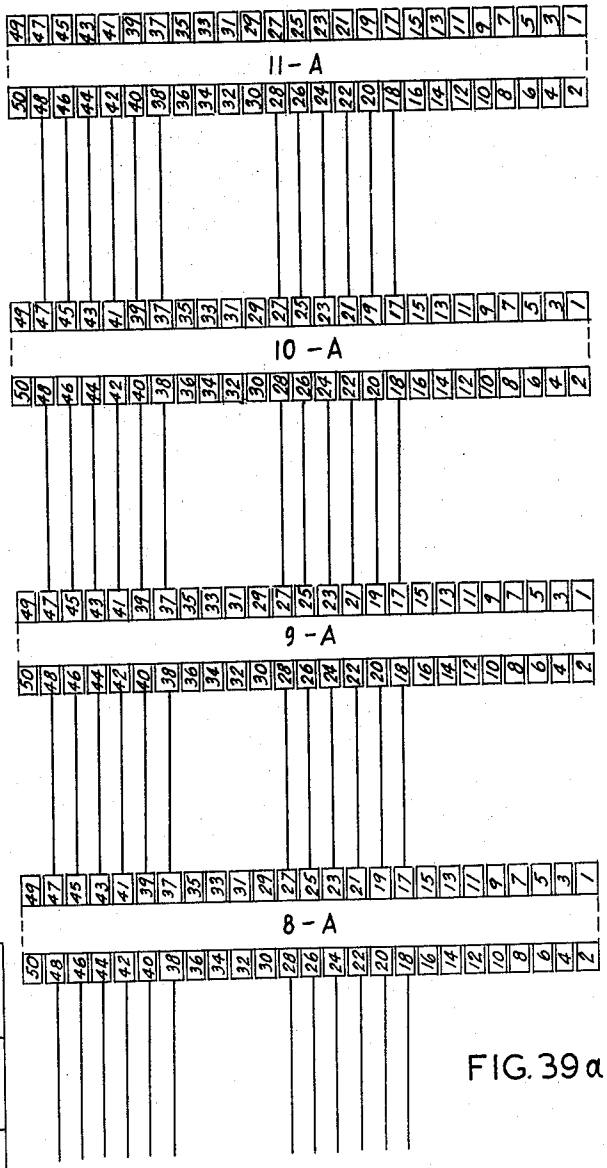


FIG. 39a

FIG. 39a	FIG. 39b	FIG. 39c
FIG. 39d	FIG. 39e	FIG. 39f
FIG. 39g	FIG. 39h	FIG. 39i
FIG. 39j	FIG. 39K	FIG. 39l

FIG. 39m

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 146

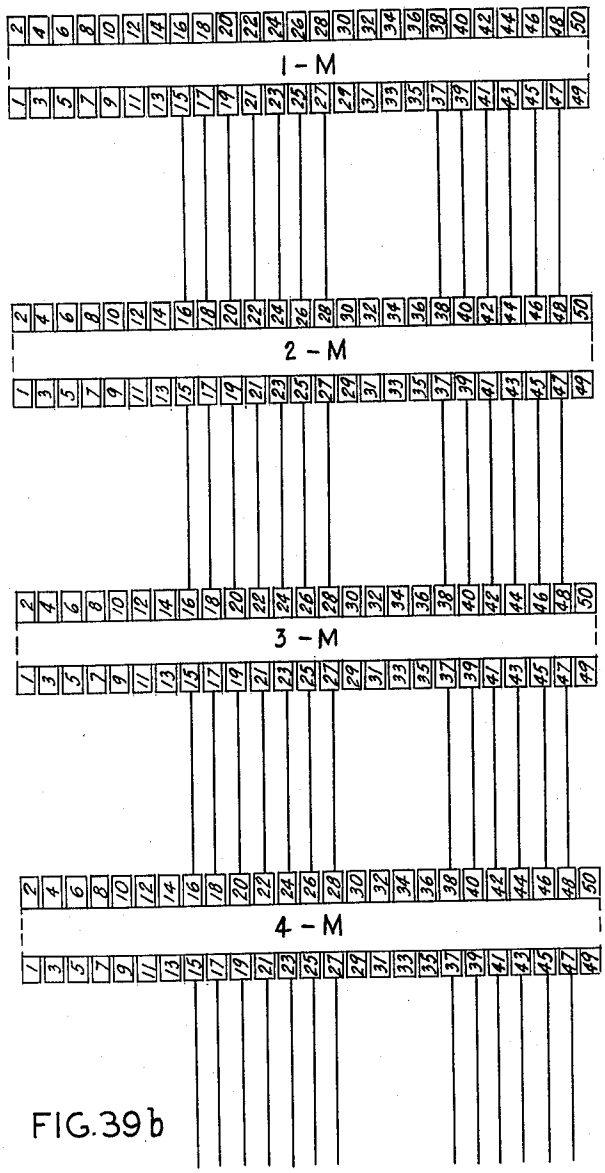
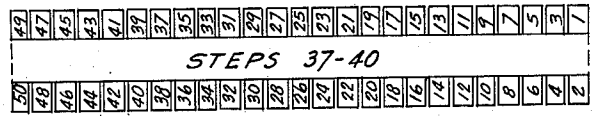


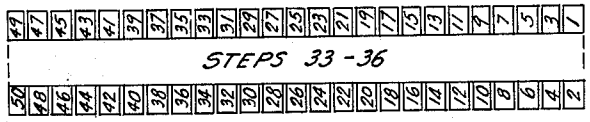
FIG. 39b

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 147







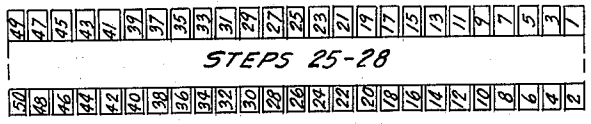


FIG. 39c

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 148

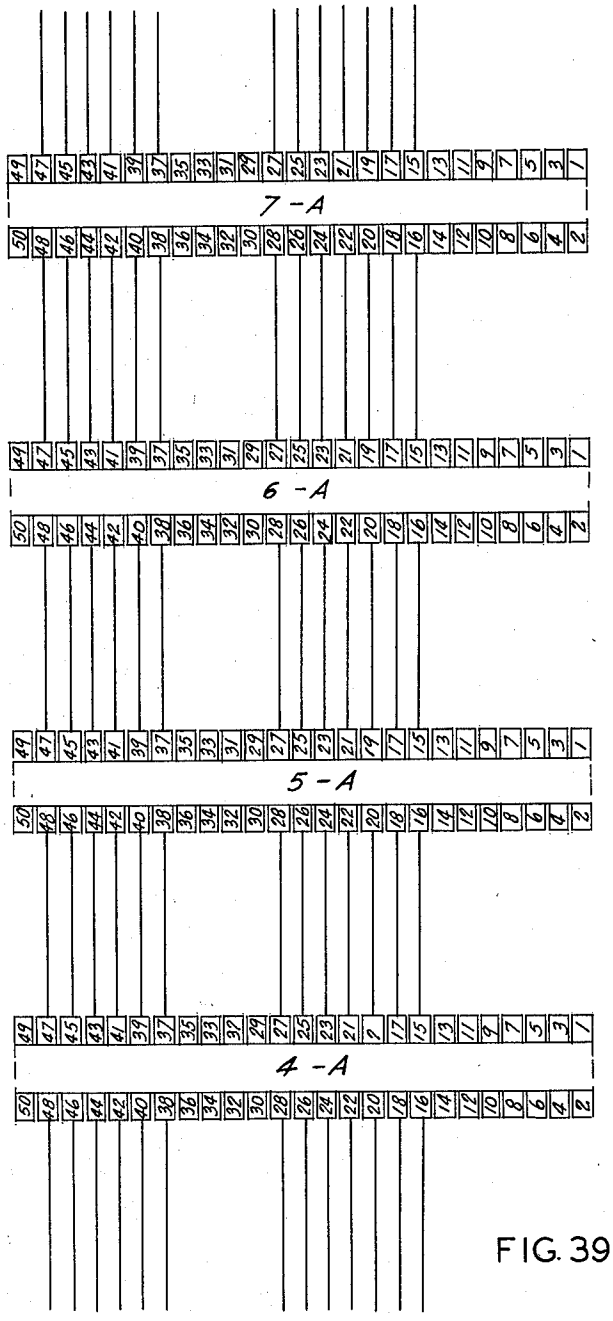


FIG. 39d

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 149

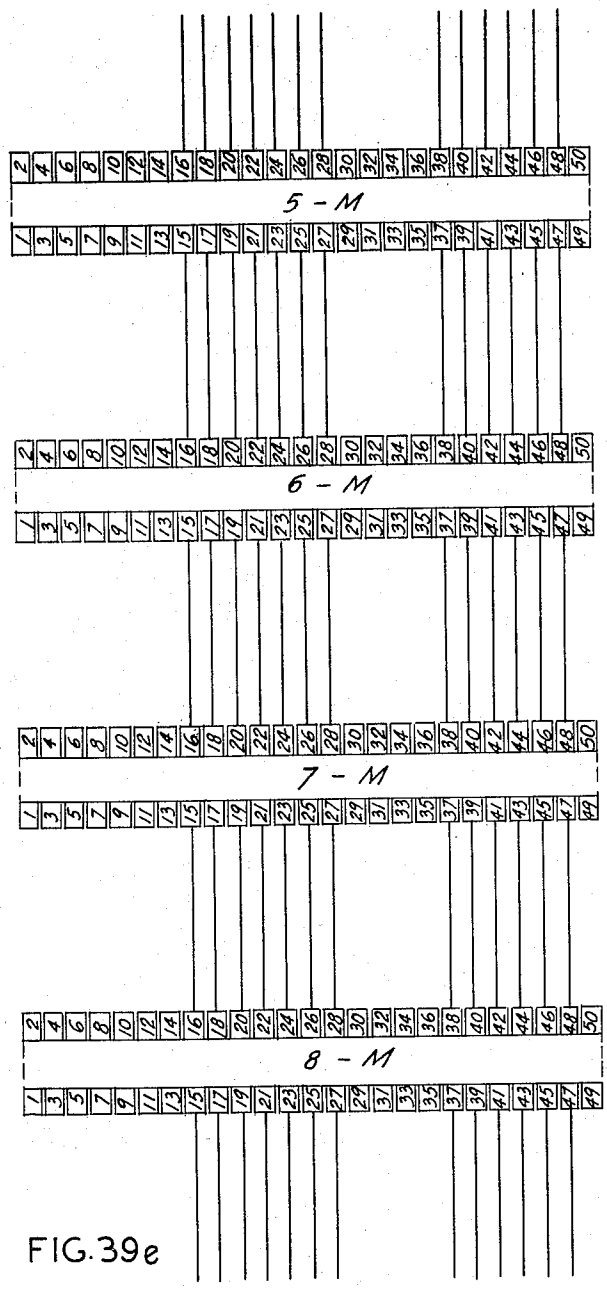


FIG. 39e

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

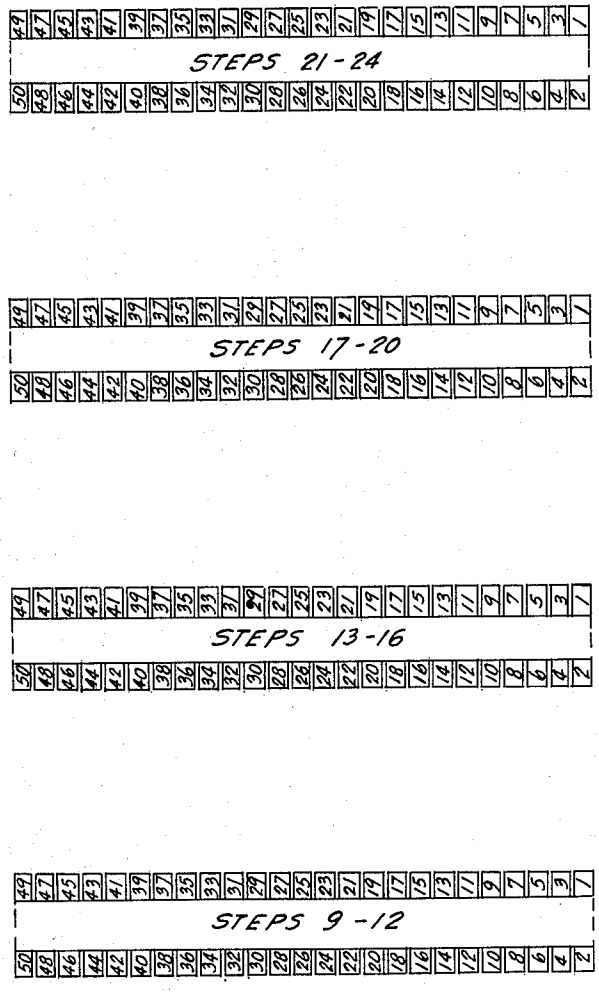


FIG. 39f

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 151

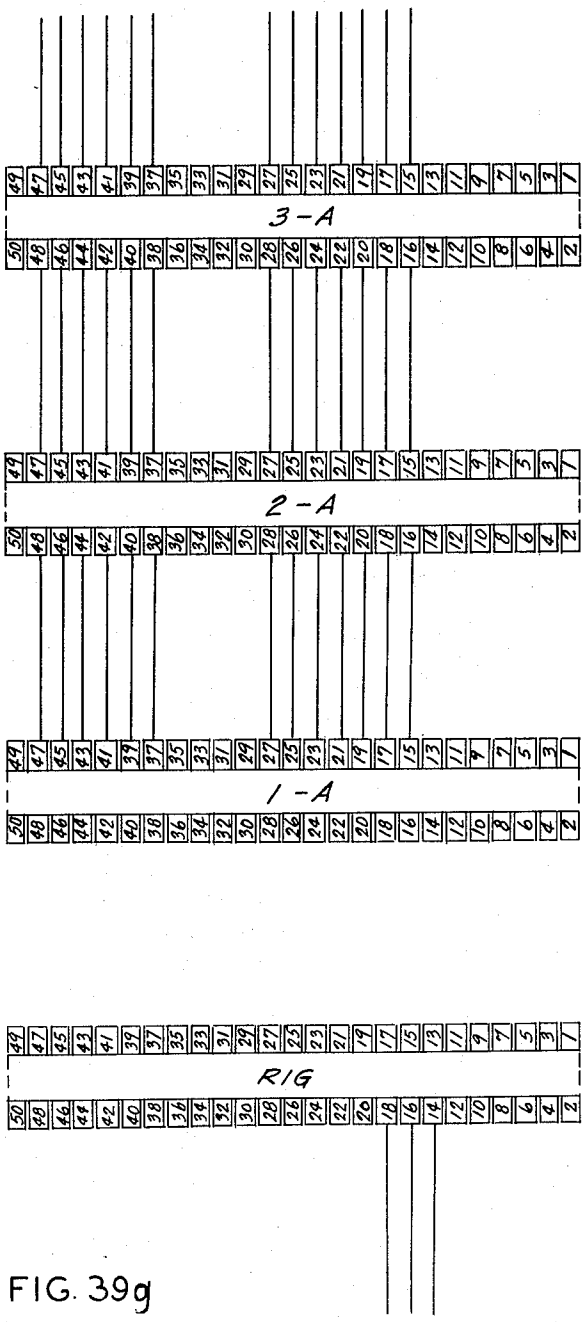


FIG. 39g

INVENTOR
LORING P CROSMAN
BY Richard W. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 152

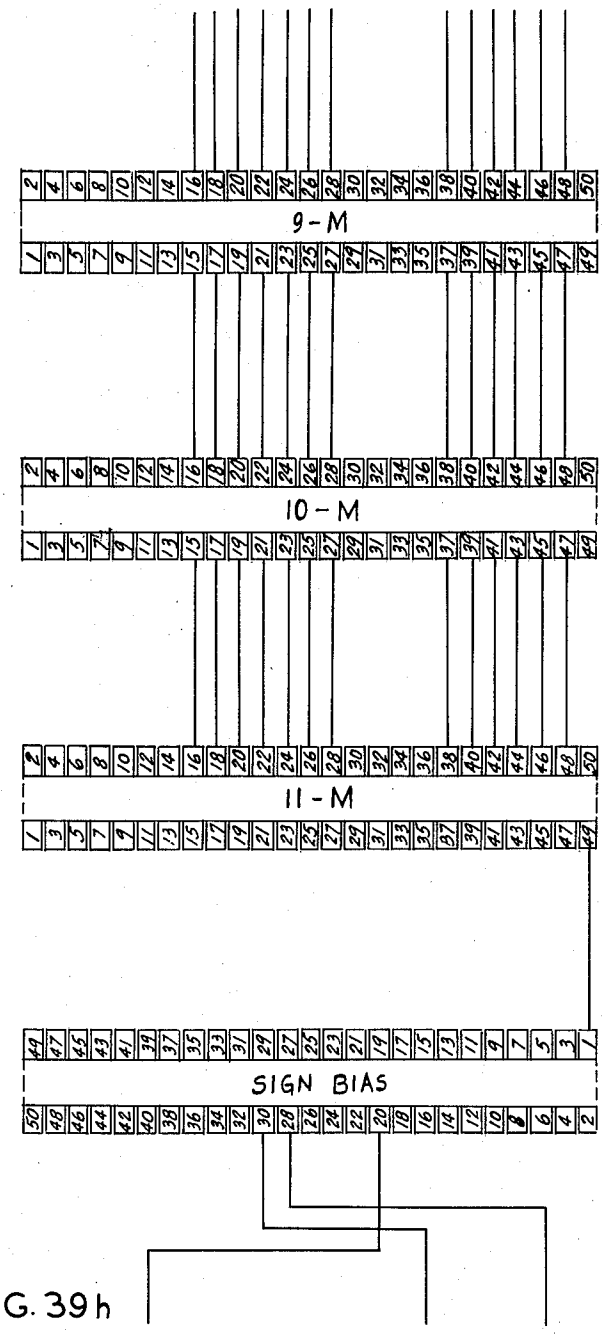


FIG. 39h

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

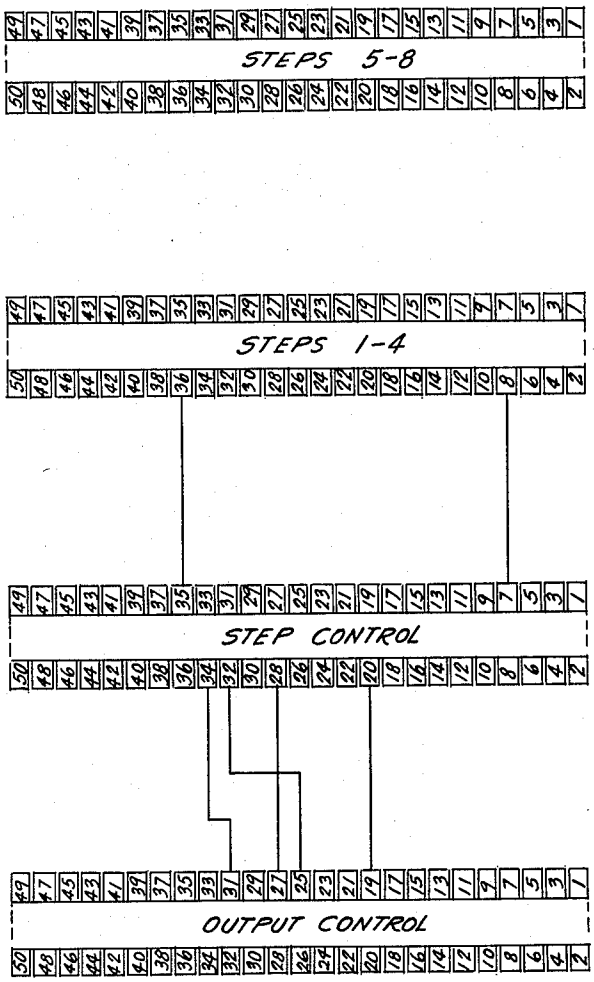
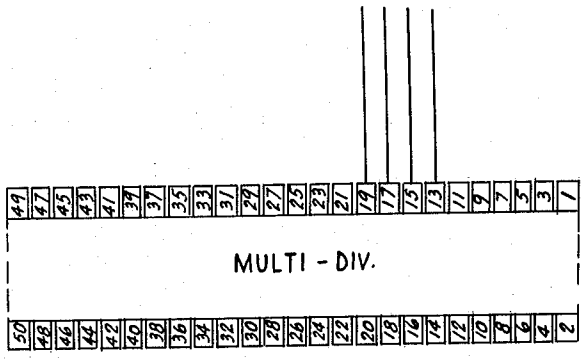


FIG. 39i

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 154



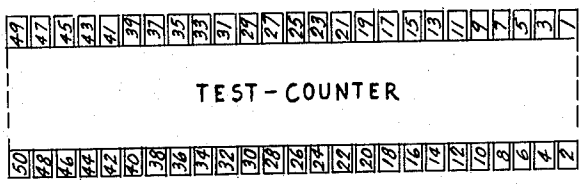




FIG. 39j

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 155

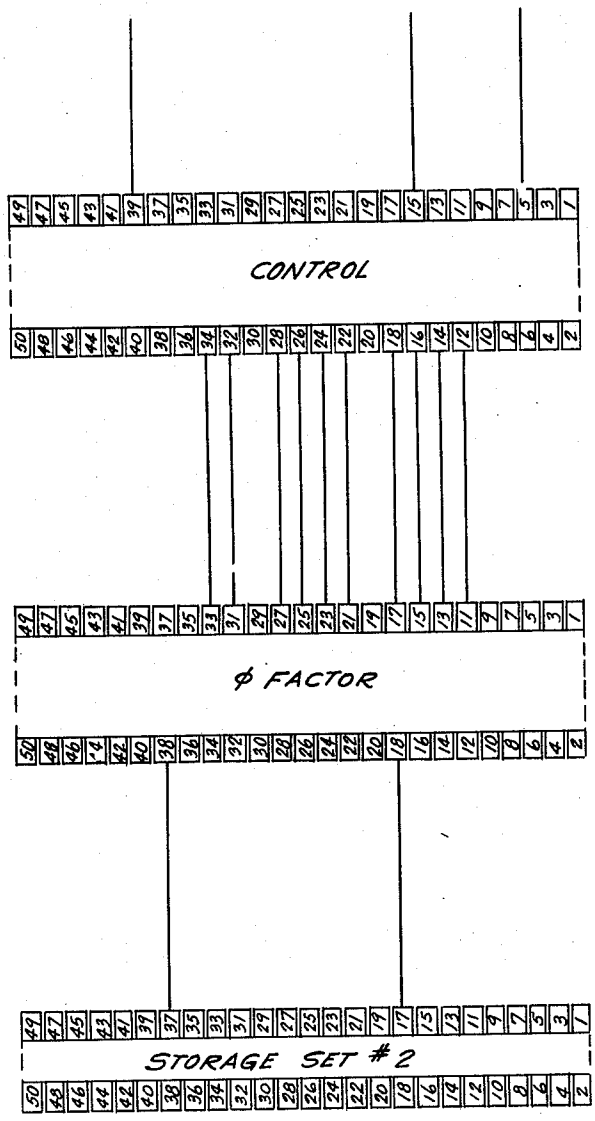


FIG. 39K

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

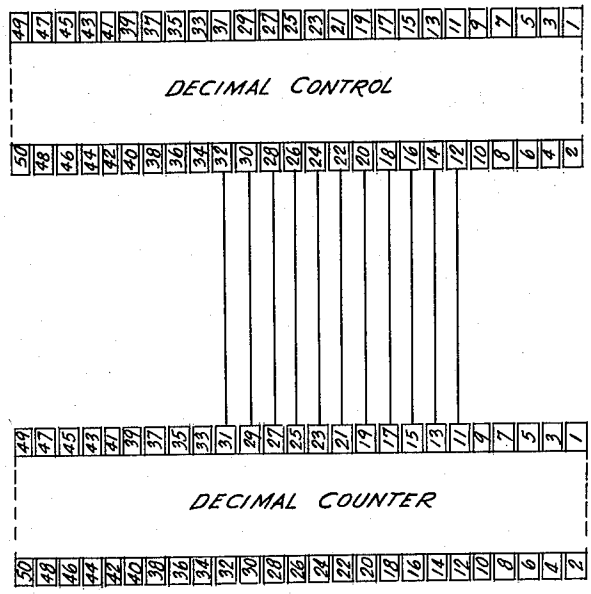




FIG. 39l

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

FIG. 40m

FIG. 40a	FIG. 40b	FIG. 40c
FIG. 40d	FIG. 40e	FIG. 40f
FIG. 40g	FIG. 40h	FIG. 40i
FIG. 40j	FIG. 40k	FIG. 40l

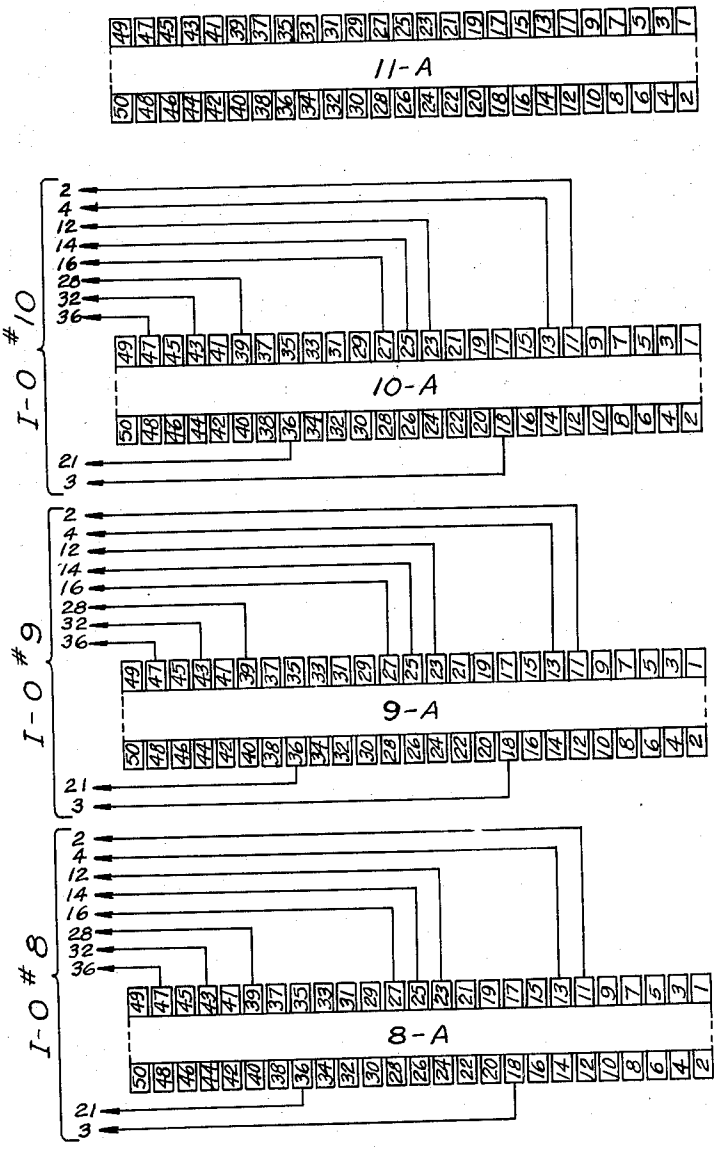


FIG. 40a

INVENTOR.
LORING P. CROSMAN
BY Richard W. Franklin

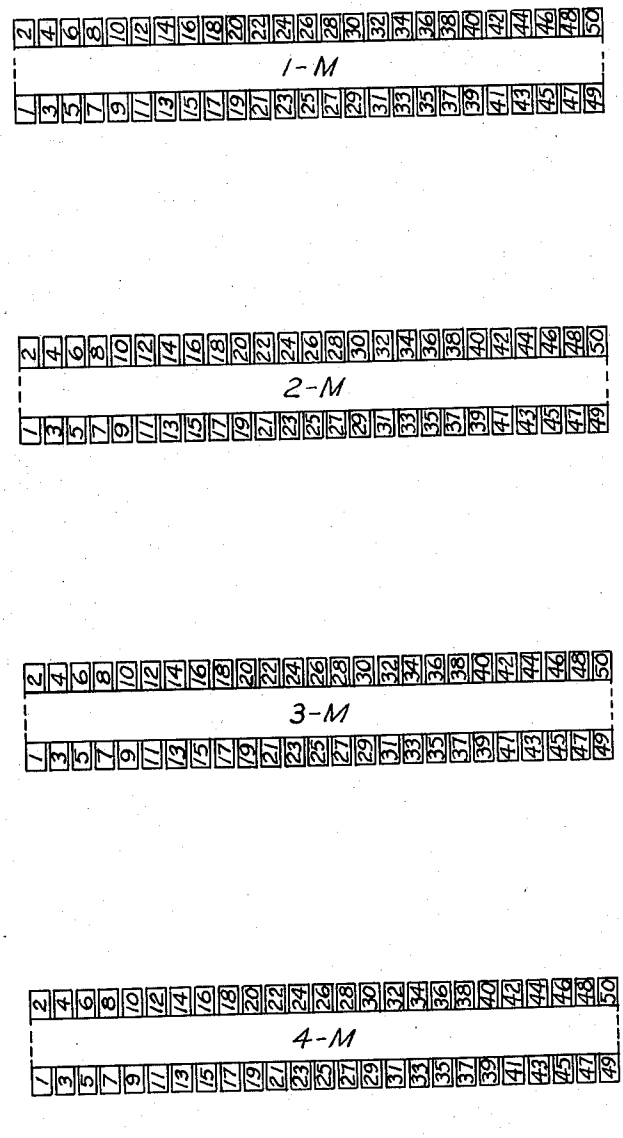
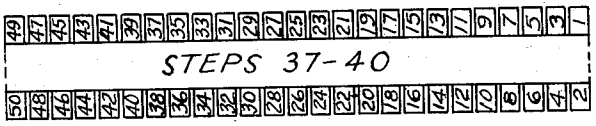
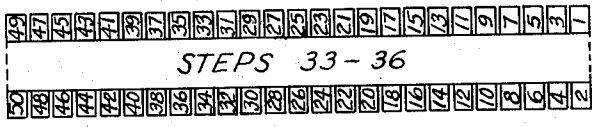


FIG. 40 b

INVENTOR.
LORING P. CROSMAN
BY Richard K. Franklin





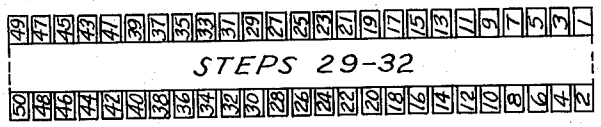




FIG. 40c

INVENTOR.
LORING P. CROSMAN
BY Richard K. Franklin

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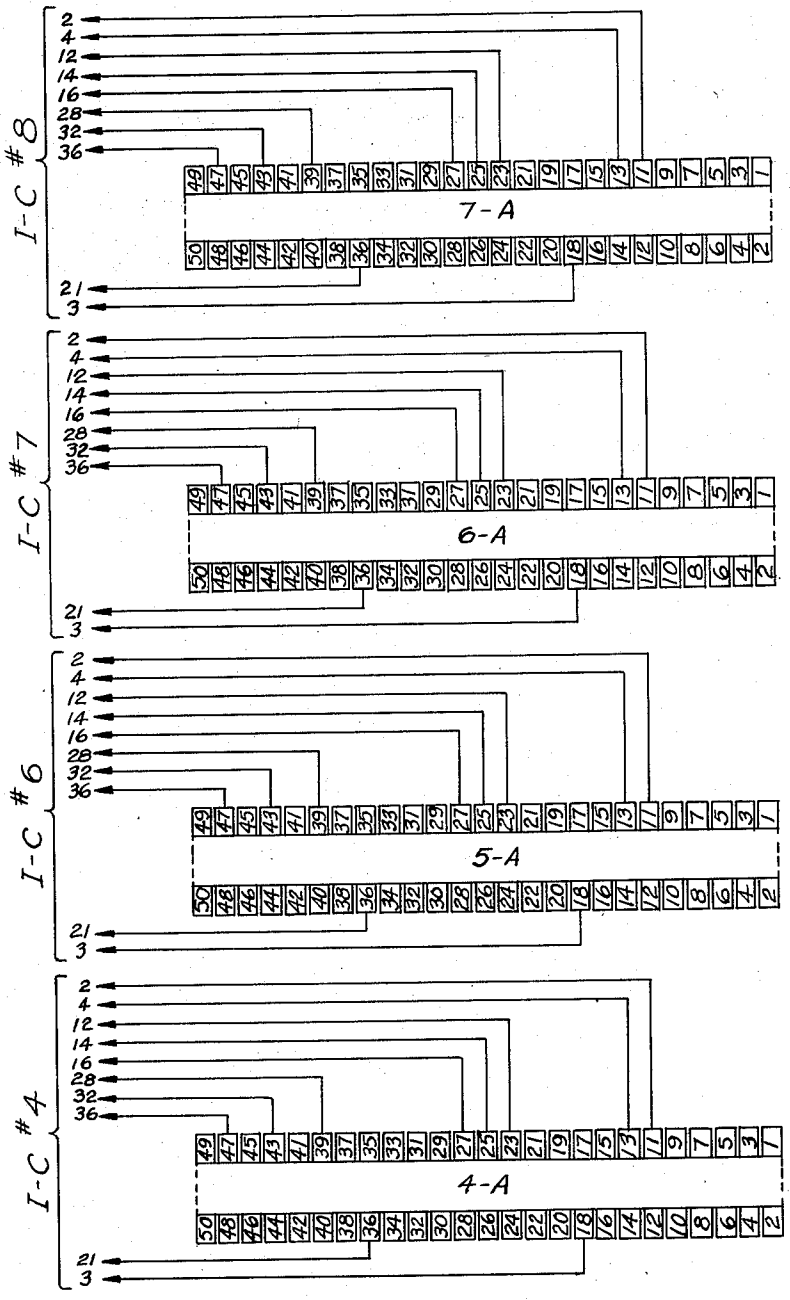


FIG. 40 d

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

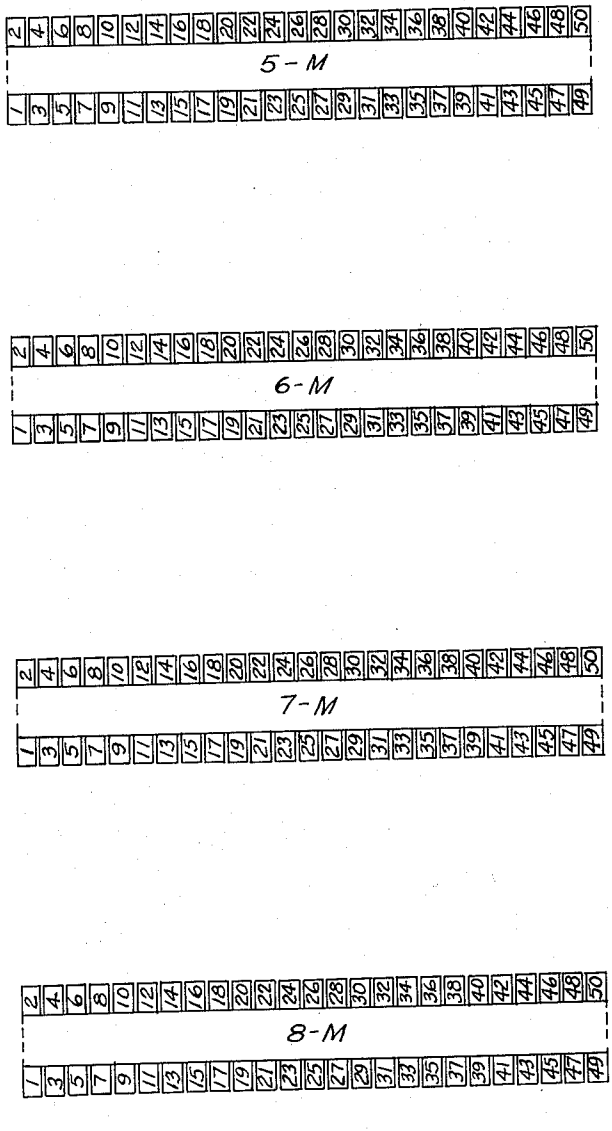


FIG. 40 e

INVENTOR.
LORING P. CROSMAN
BY Richard H. Franklin

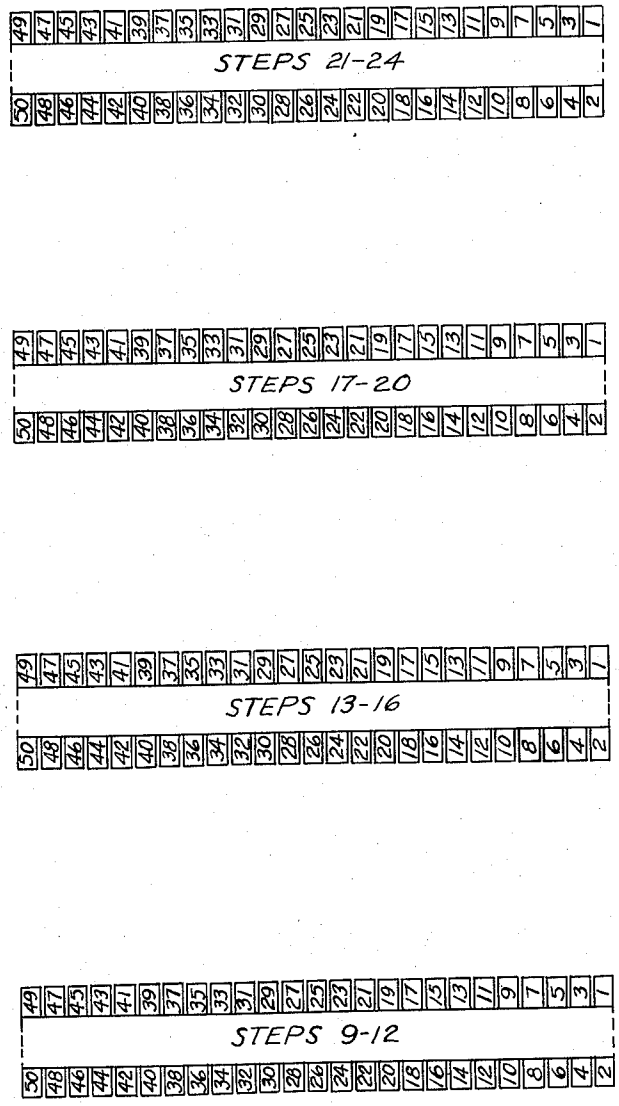


FIG. 40f

INVENTOR.
LORING P. CROSMAN
BY Richard K. Franklin

ELECTRONIC DATA PROCESSING SYSTEM

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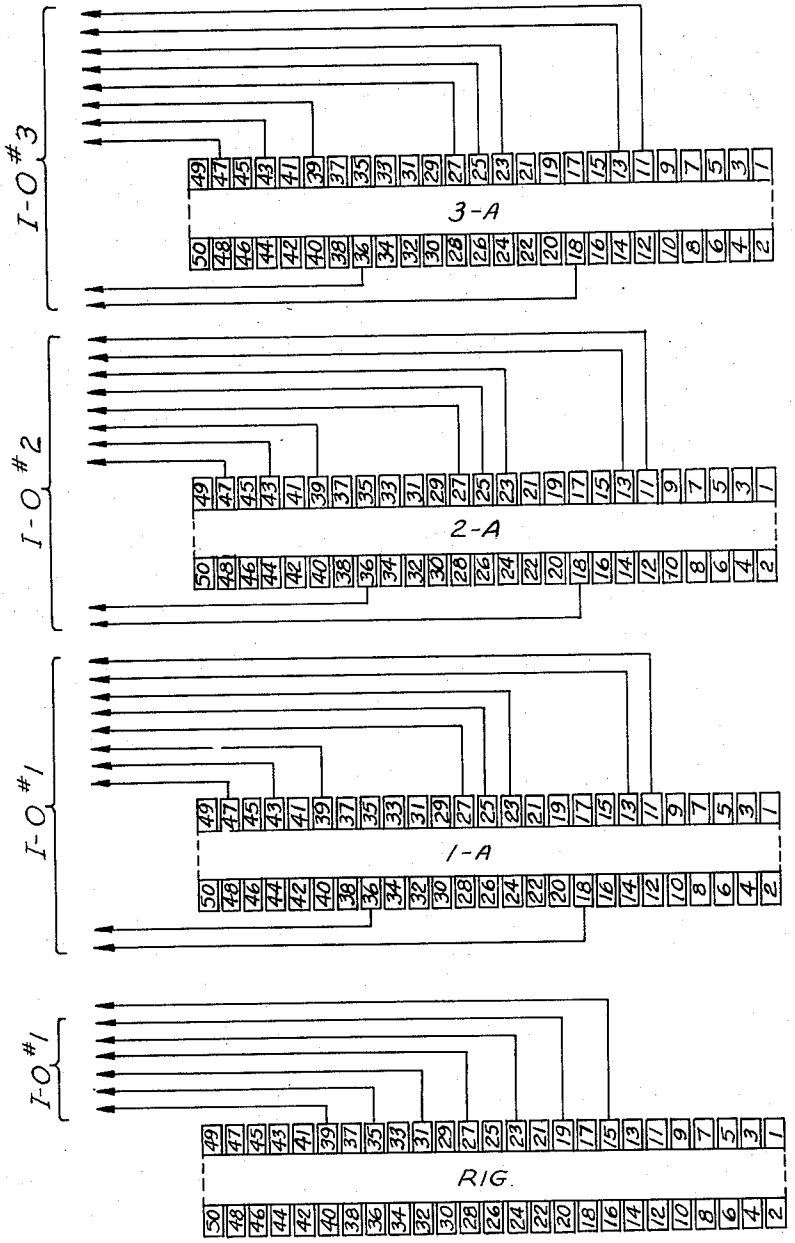
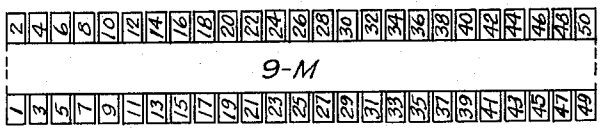
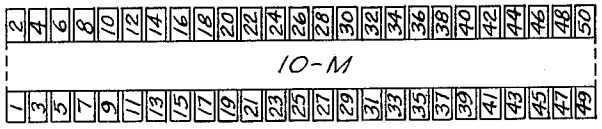
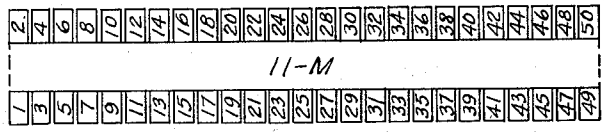


FIG. 40 g

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY







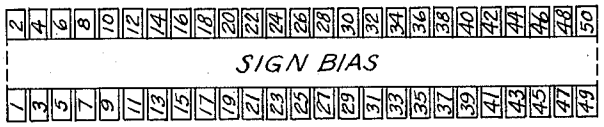
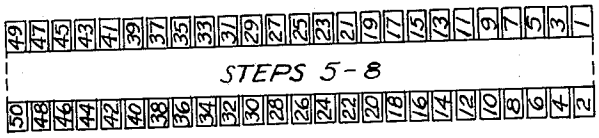


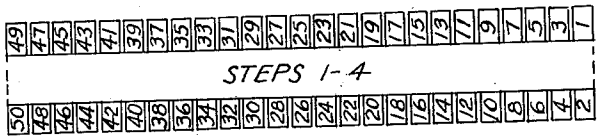
FIG. 40h

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

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Filed Jan. 13, 1953 242 Sheets-Sheet 165





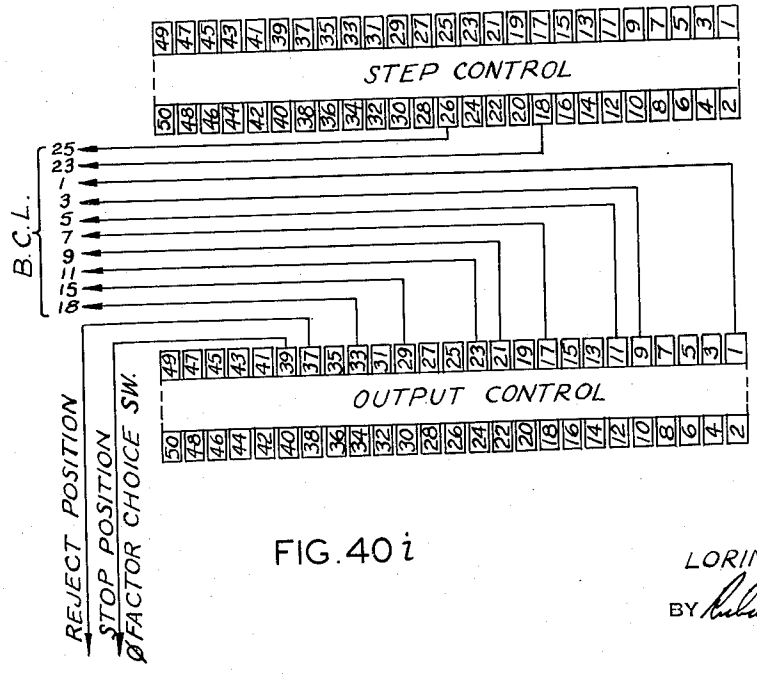


FIG. 40i

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

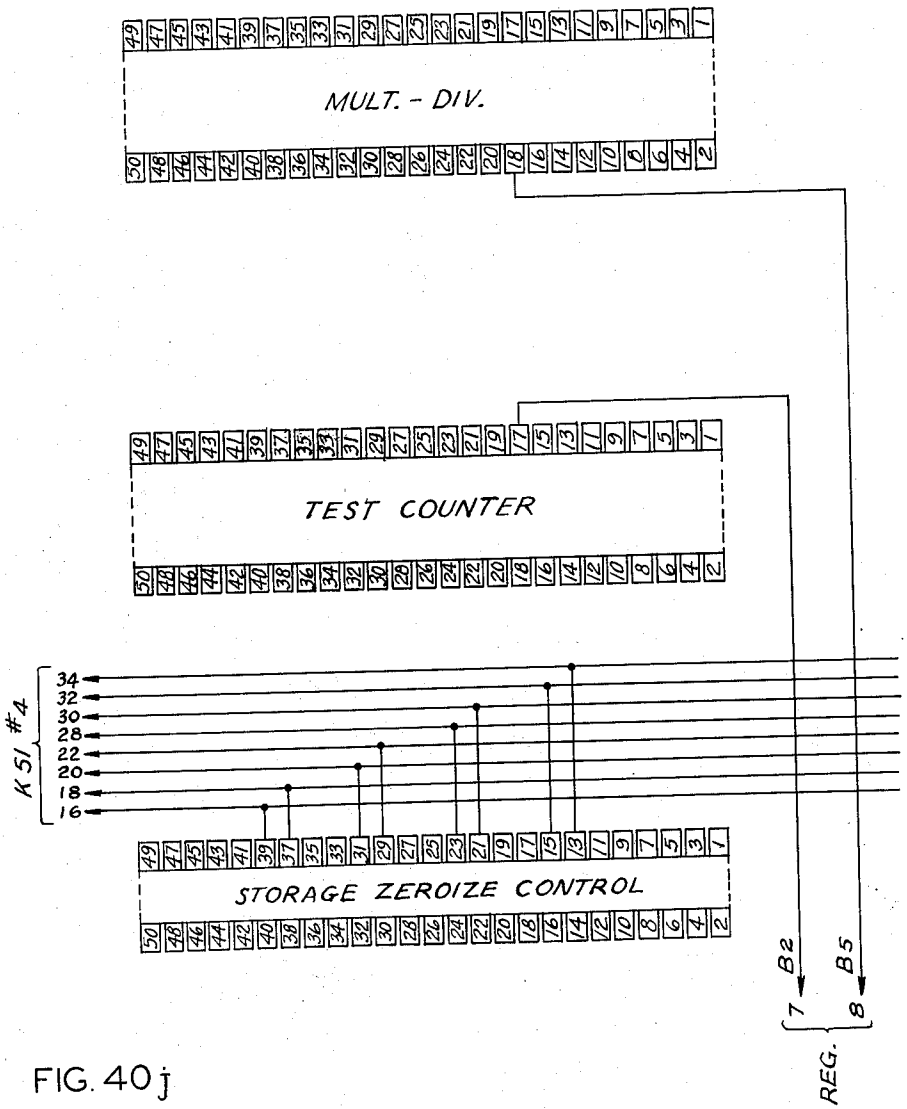


FIG. 40j

INVENTOR
LORING P. CROSMAN
BY Richard W. Franklin
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 167

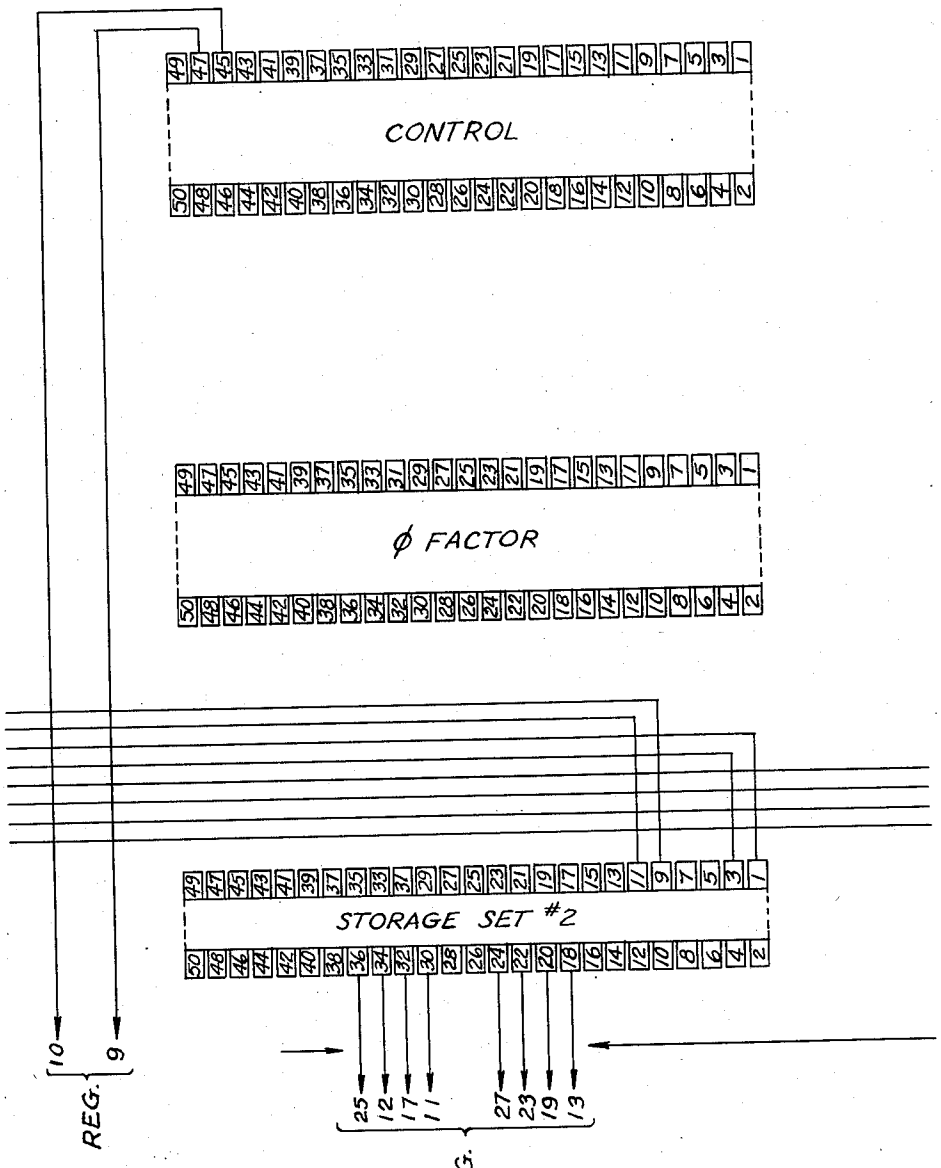
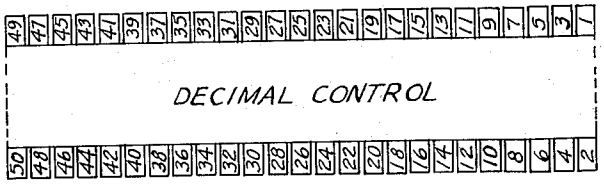


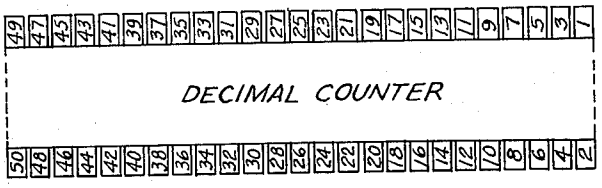
FIG. 40k

INVENTOR
LORING P. CROSMAN
BY Richard K. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 168





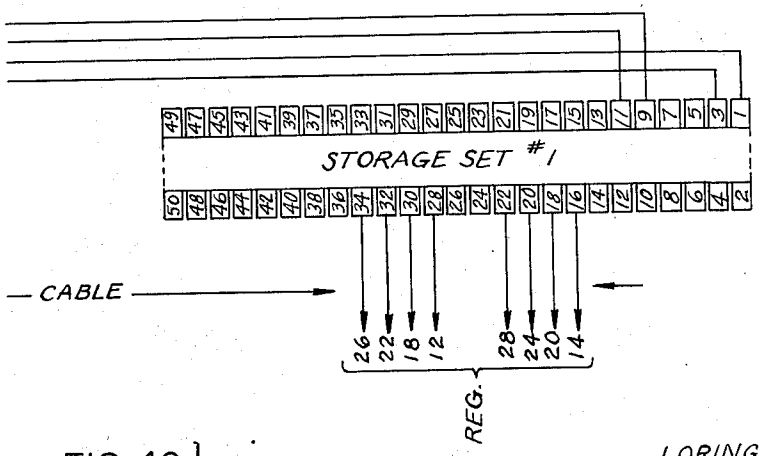


FIG. 40 l

INVENTOR
LORING P. CROSMAN
BY Richard H. Franklin
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 169

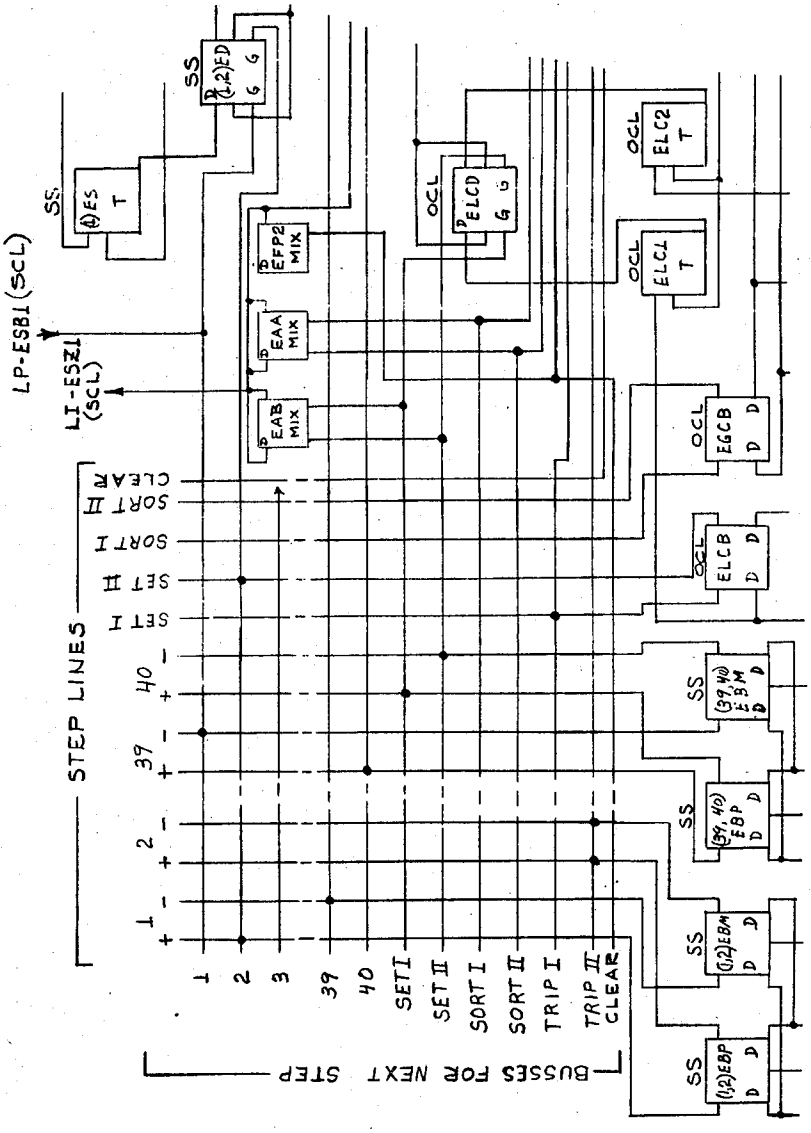


FIG. 41a	FIG. 41b
FIG. 41c	

FIG. 41c

FIG. 41a

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 170

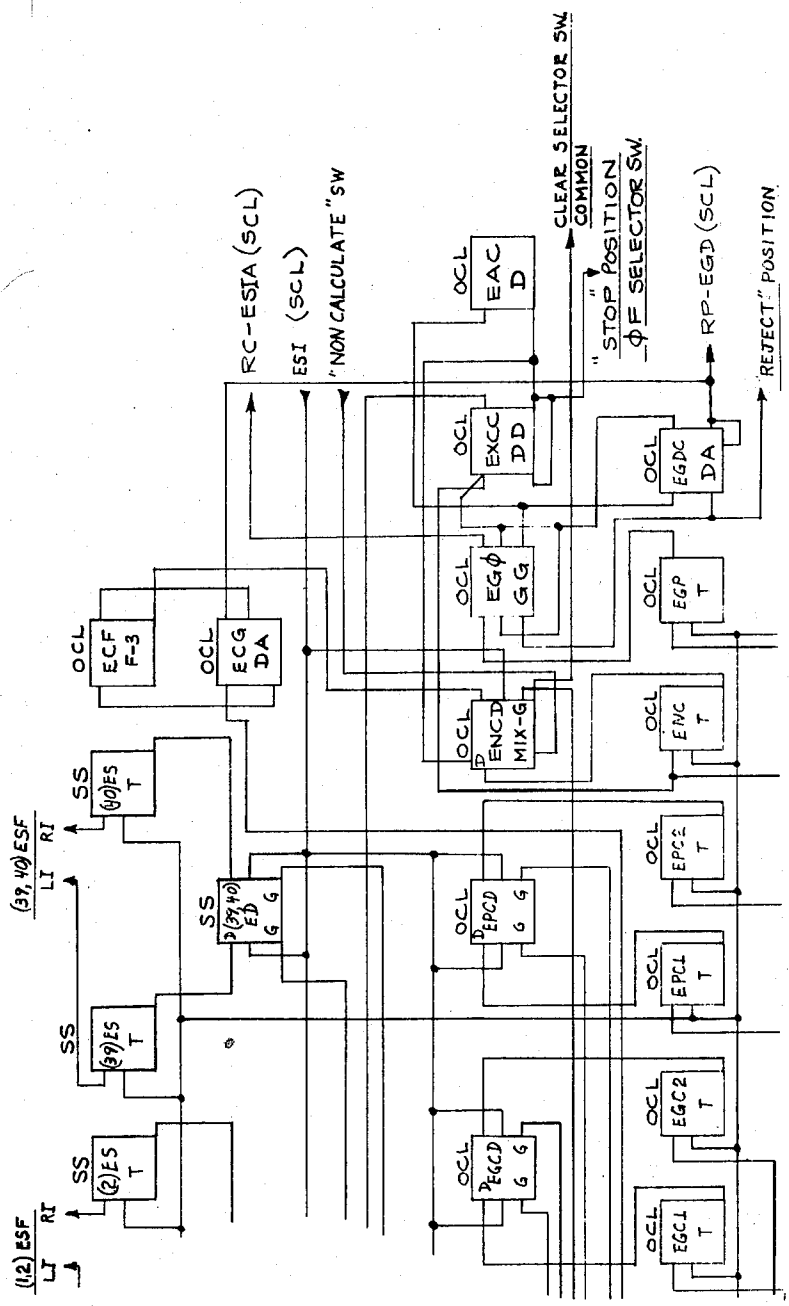


FIG. 41L

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

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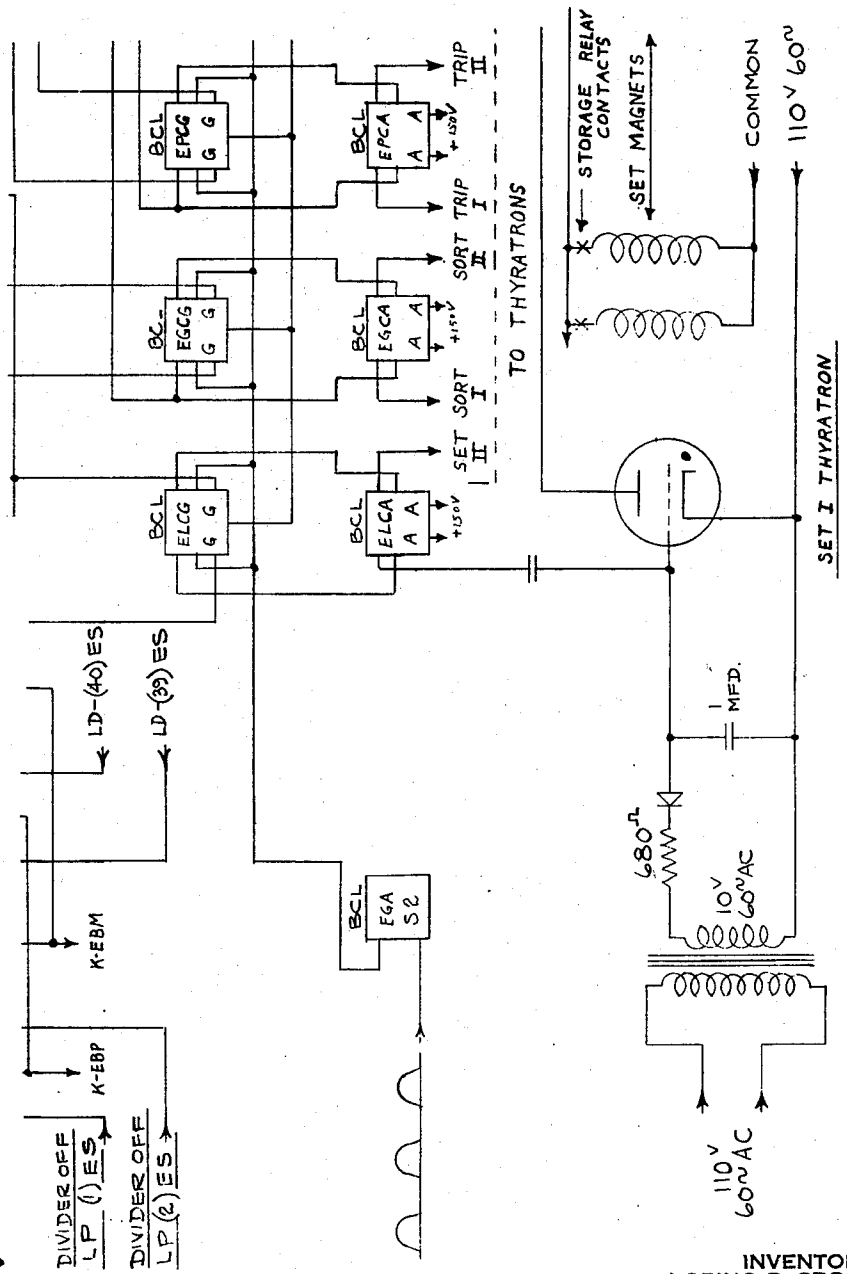


FIG. 41c

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 172

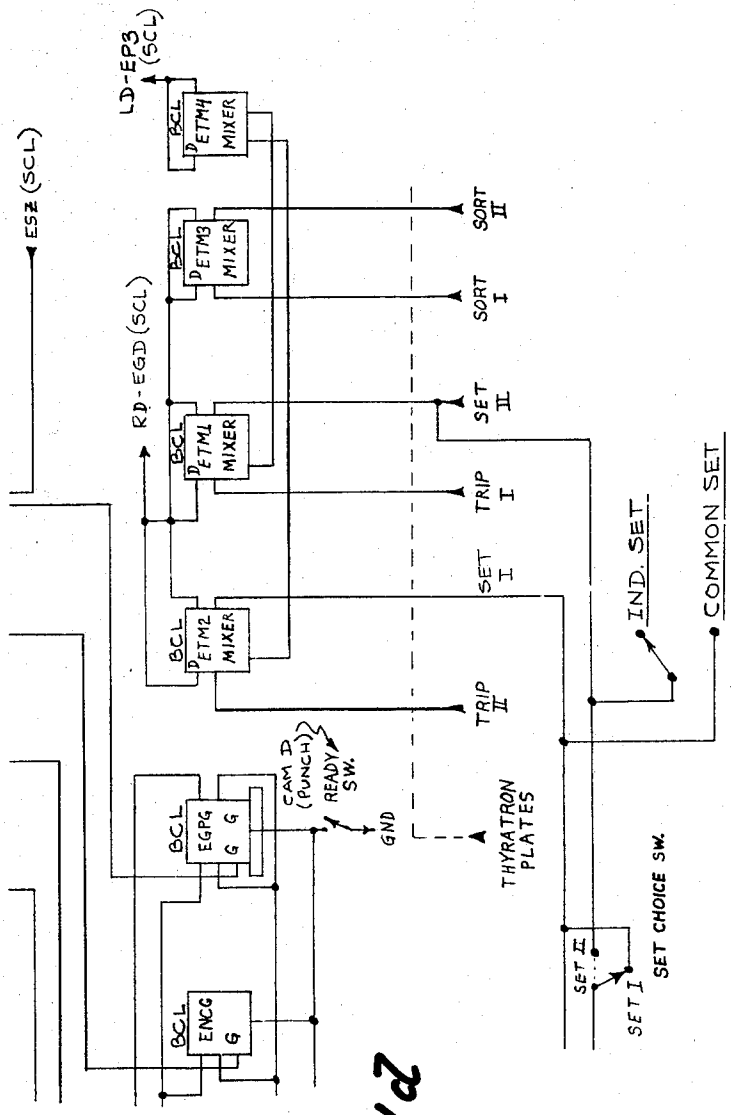


FIG. 41d

INVENTOR
LORING P. CROSMAN
BY George V Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 173

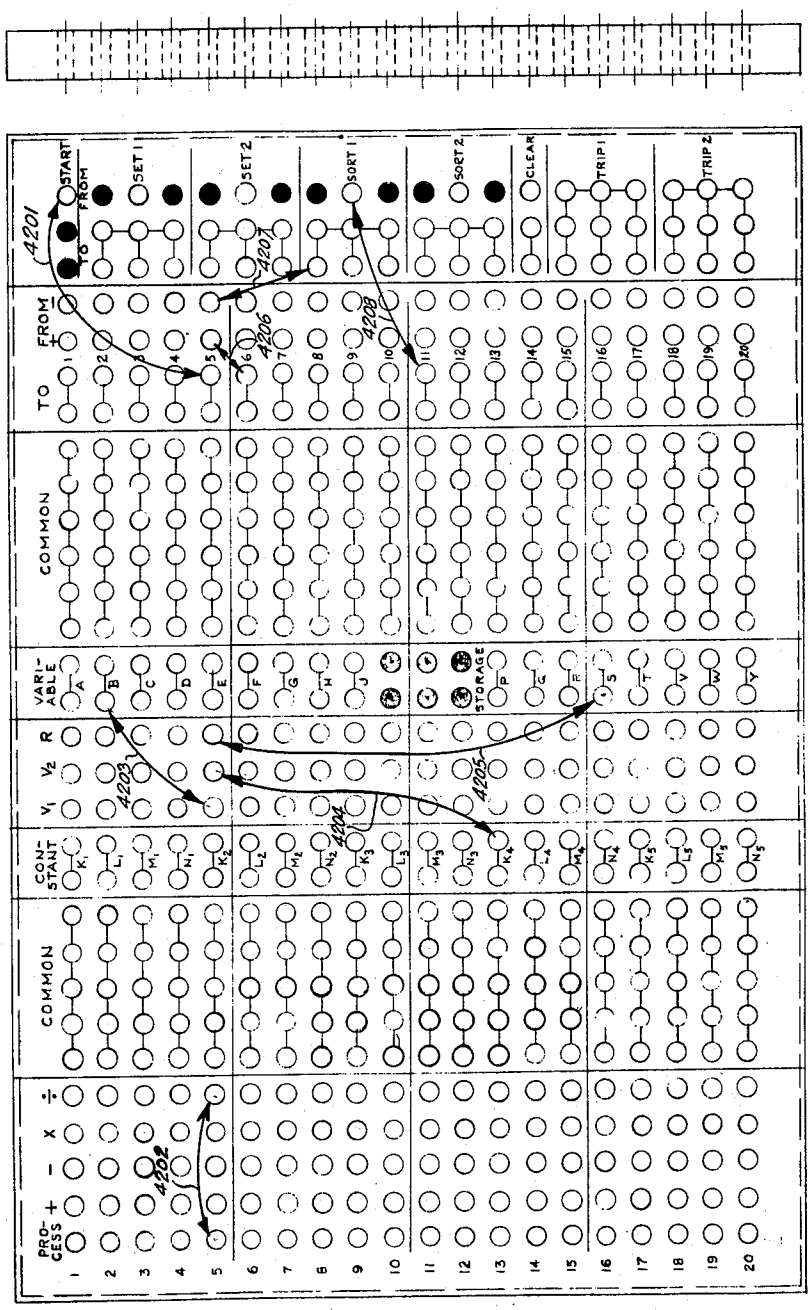


FIG. 42a

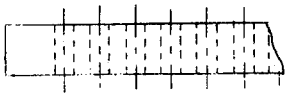
FIG. 42c

FIG. 42a
FIG. 42b

INVENTOR
LORING P. CROSMAN
BY George V. Ketzpath
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 174



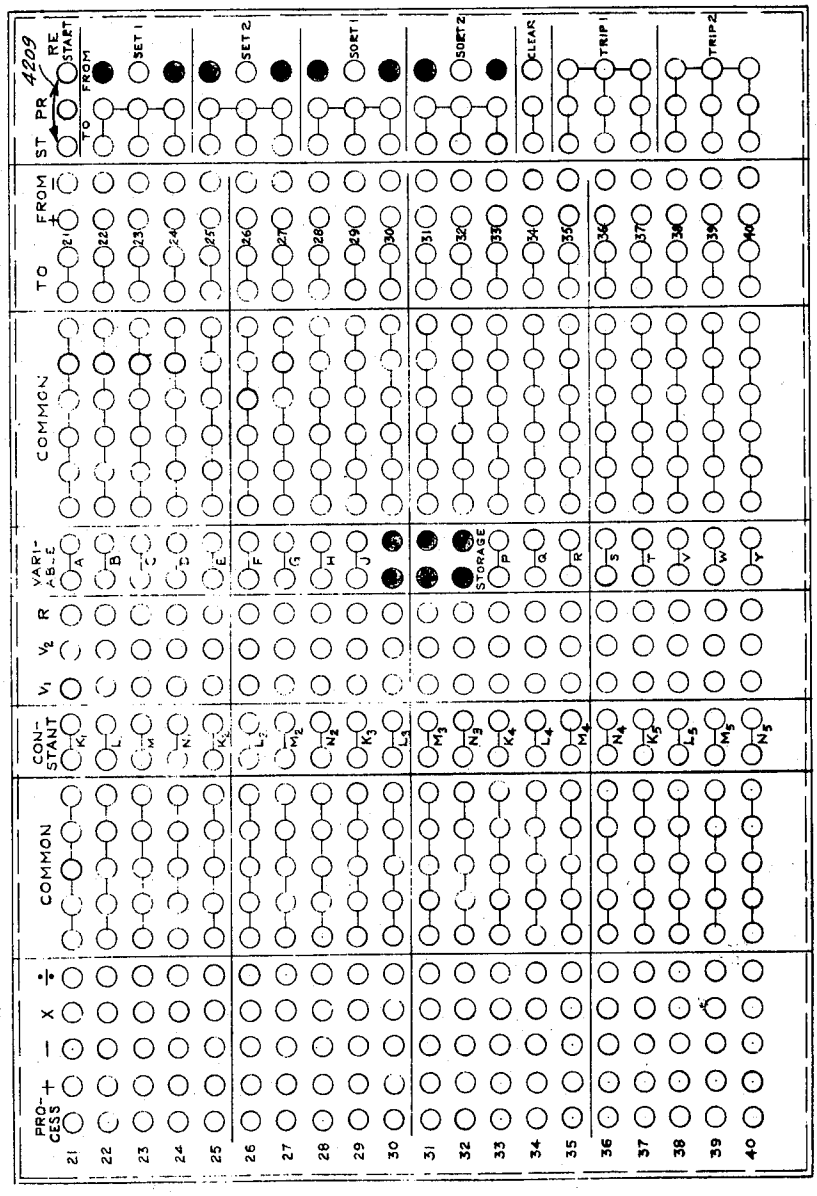


FIG. 42b

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 175

FIG. 43a

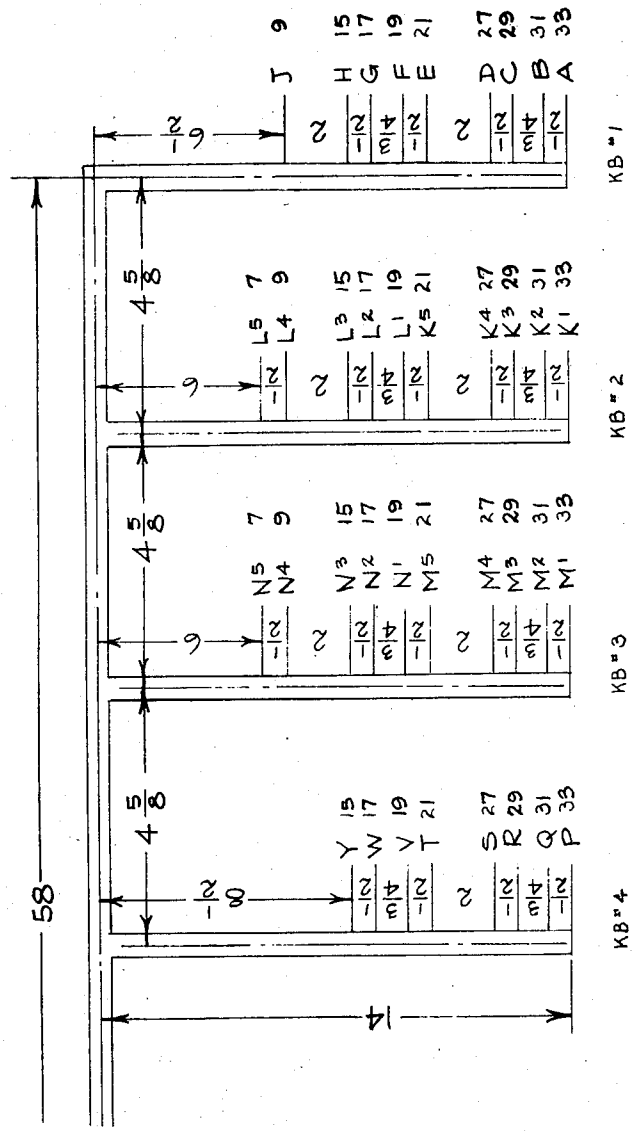
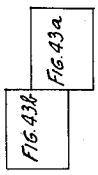
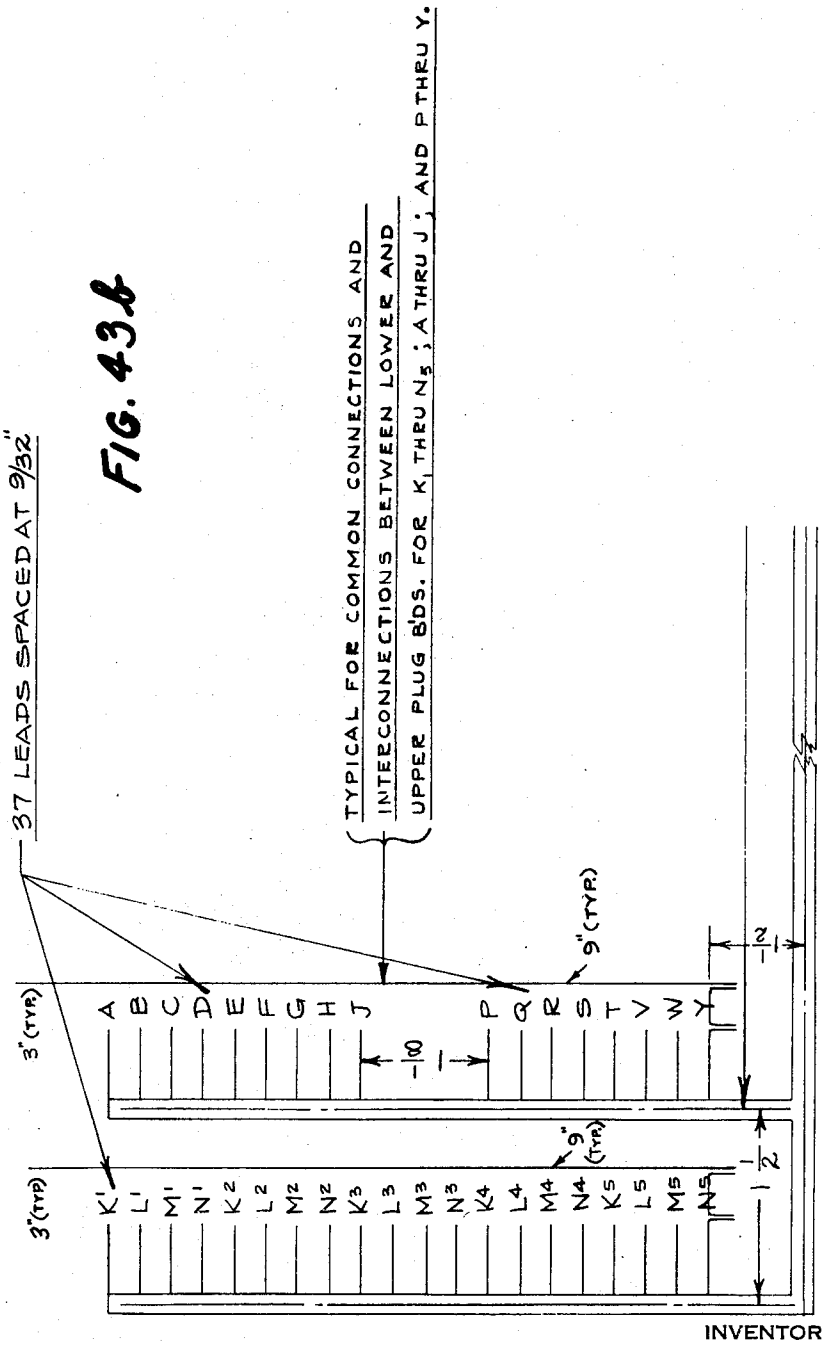


FIG. 43c



INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

FIG. 43B



INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

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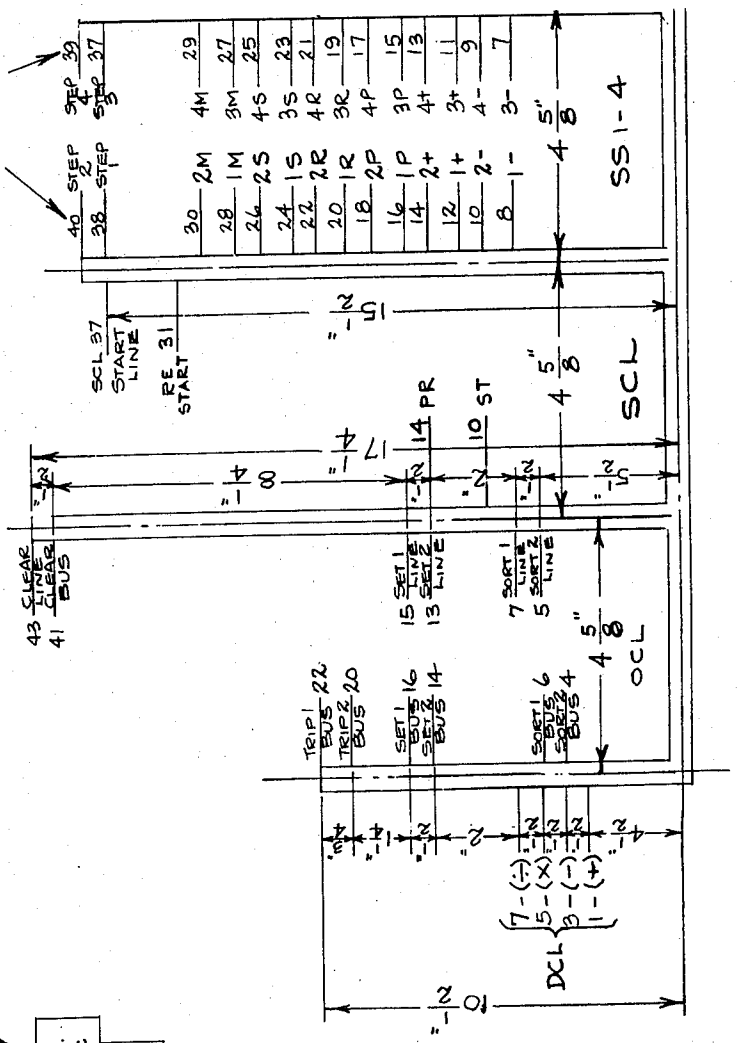


FIG. 44a

FIG. 44b FIG. 44c FIG. 44d FIG. 44e

FIG. 44f

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 178

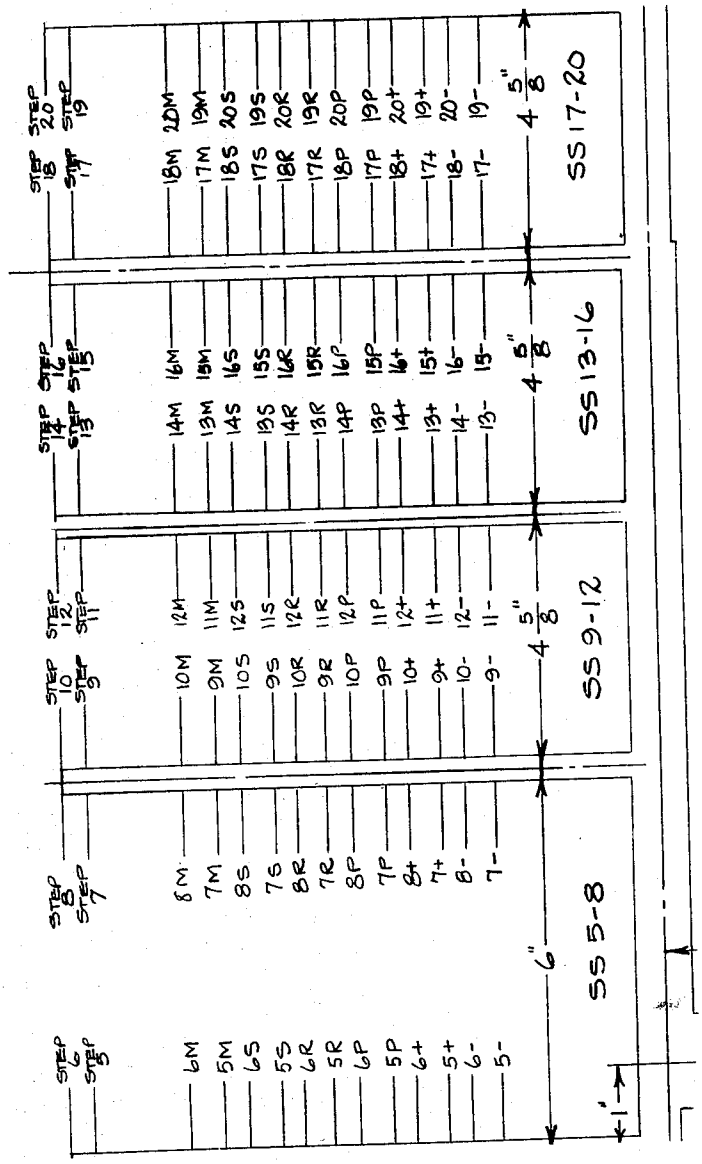


FIG. 44a

INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

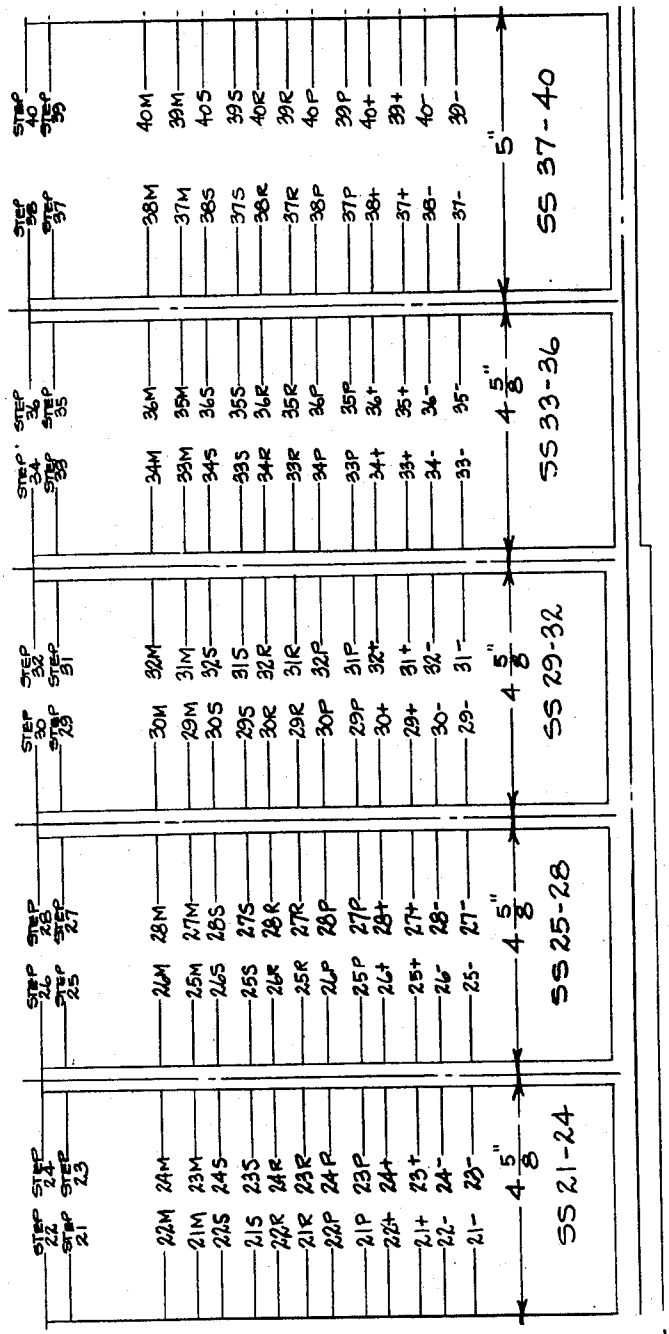


FIG. 44c

INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

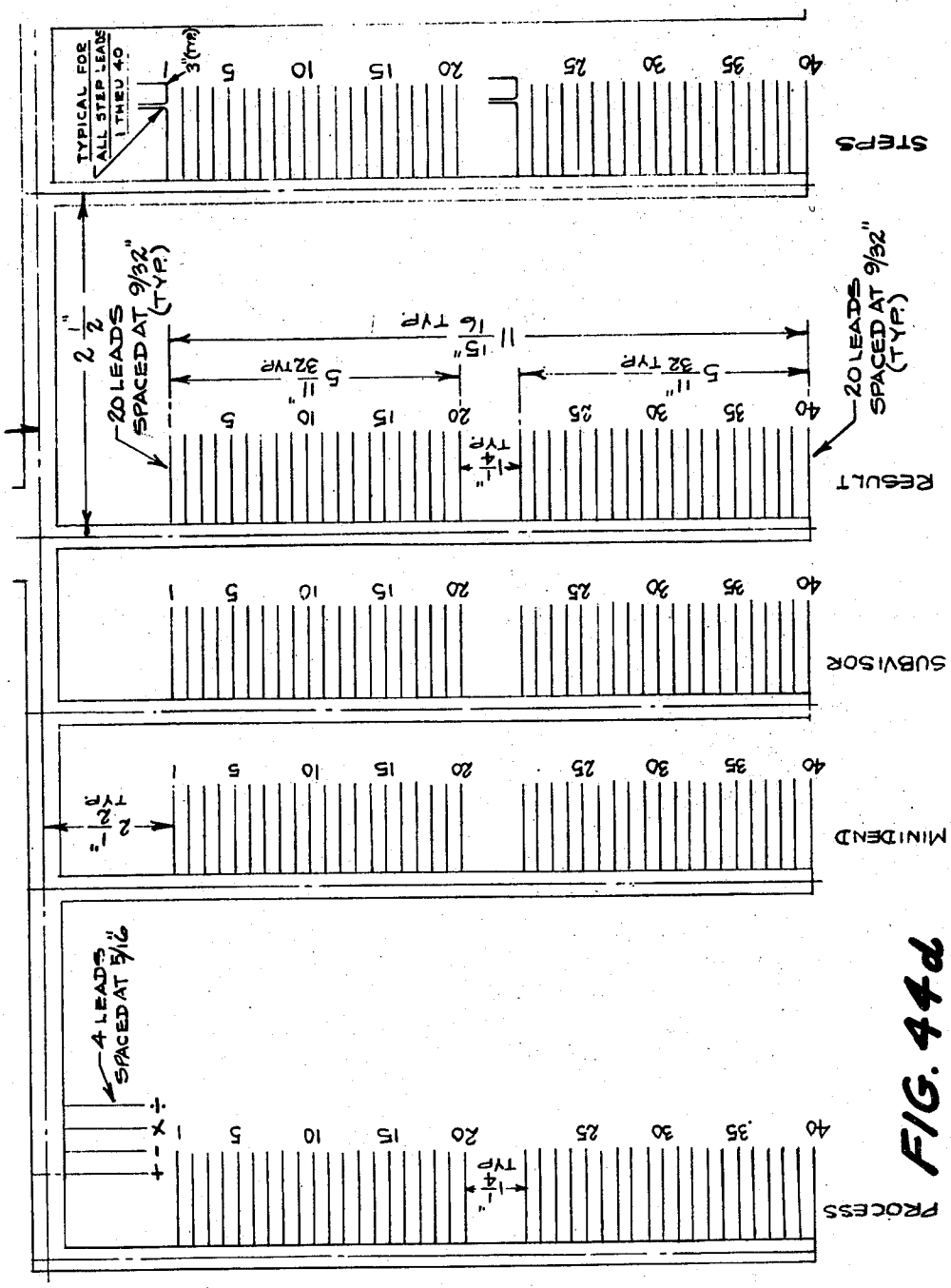
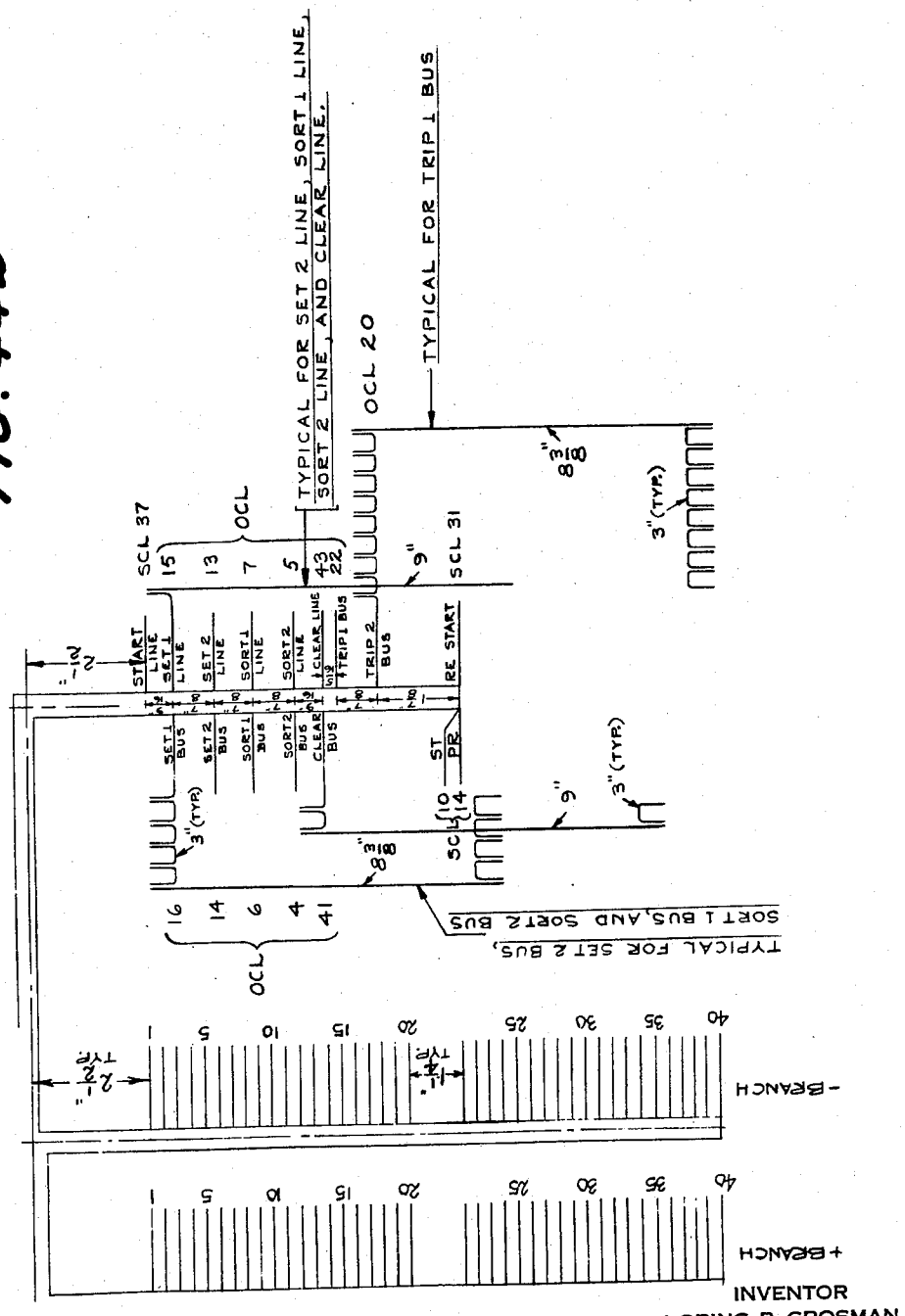

STEPS
TYPICAL FOR ALL STEP LEADS 1 THRU 40
3"(TYP.)
RESULT
20 LEADS SPACED AT 9/32" (TYP.)
SUBVISOR
MINIDEND
PROCESS
4 LEADS SPACED AT 5/16"

FIG. 44d

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 181

FIG. 44L



INVENTOR
LORING P. CROSMAN
BY George V. Ettgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 182

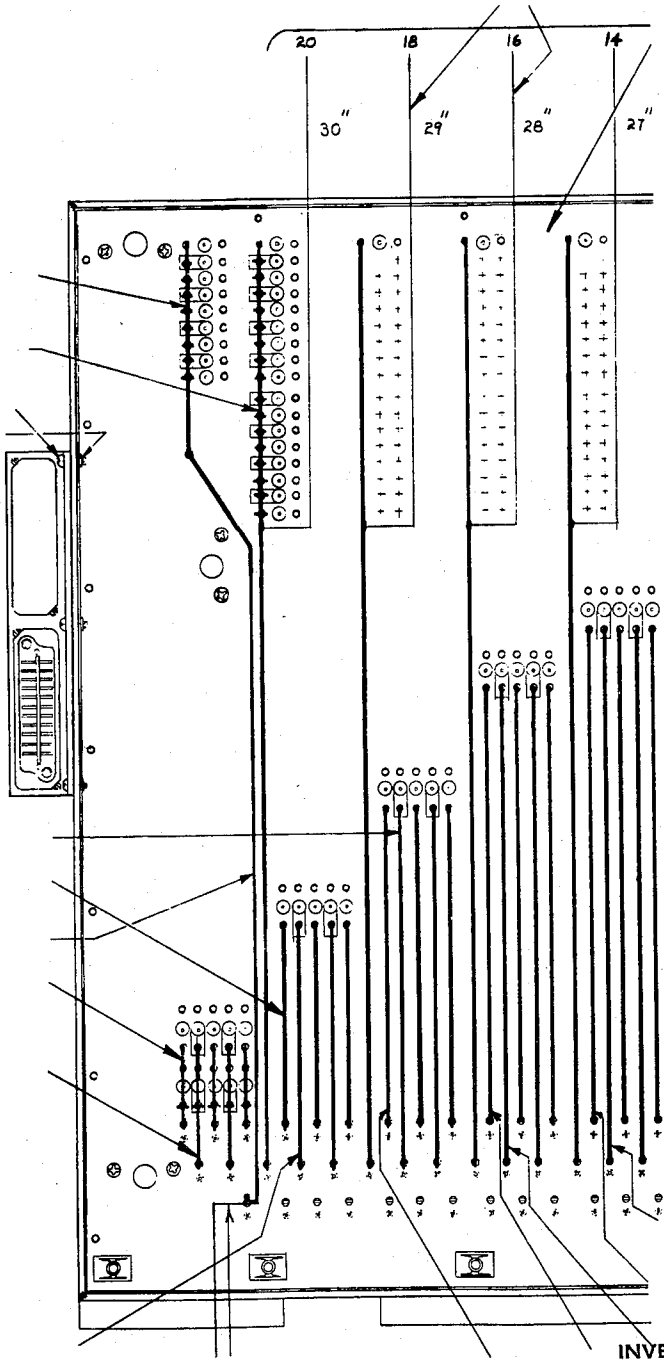


FIG. 45a

FIG. 45a	FIG. 45b

FIG. 45c

INVENTOR
LORING P. CROSMAN
BY George V. Leitzell
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 183

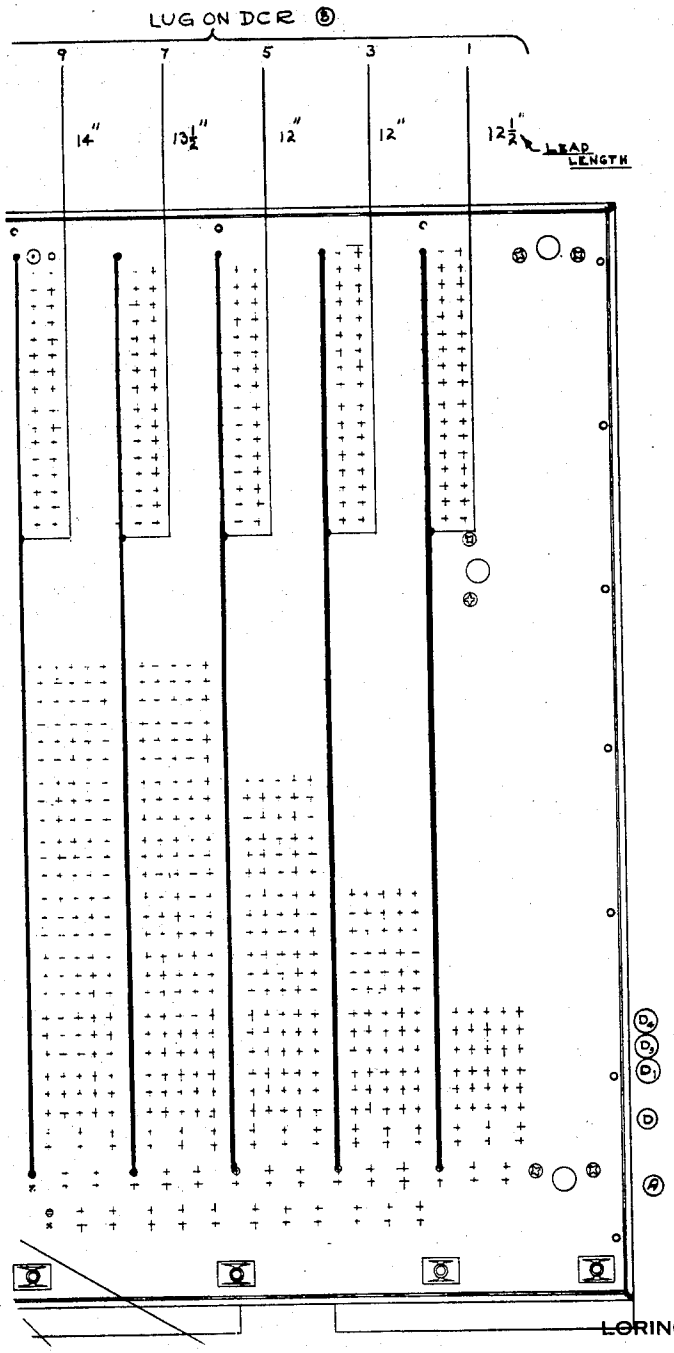


FIG. 45C

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 184

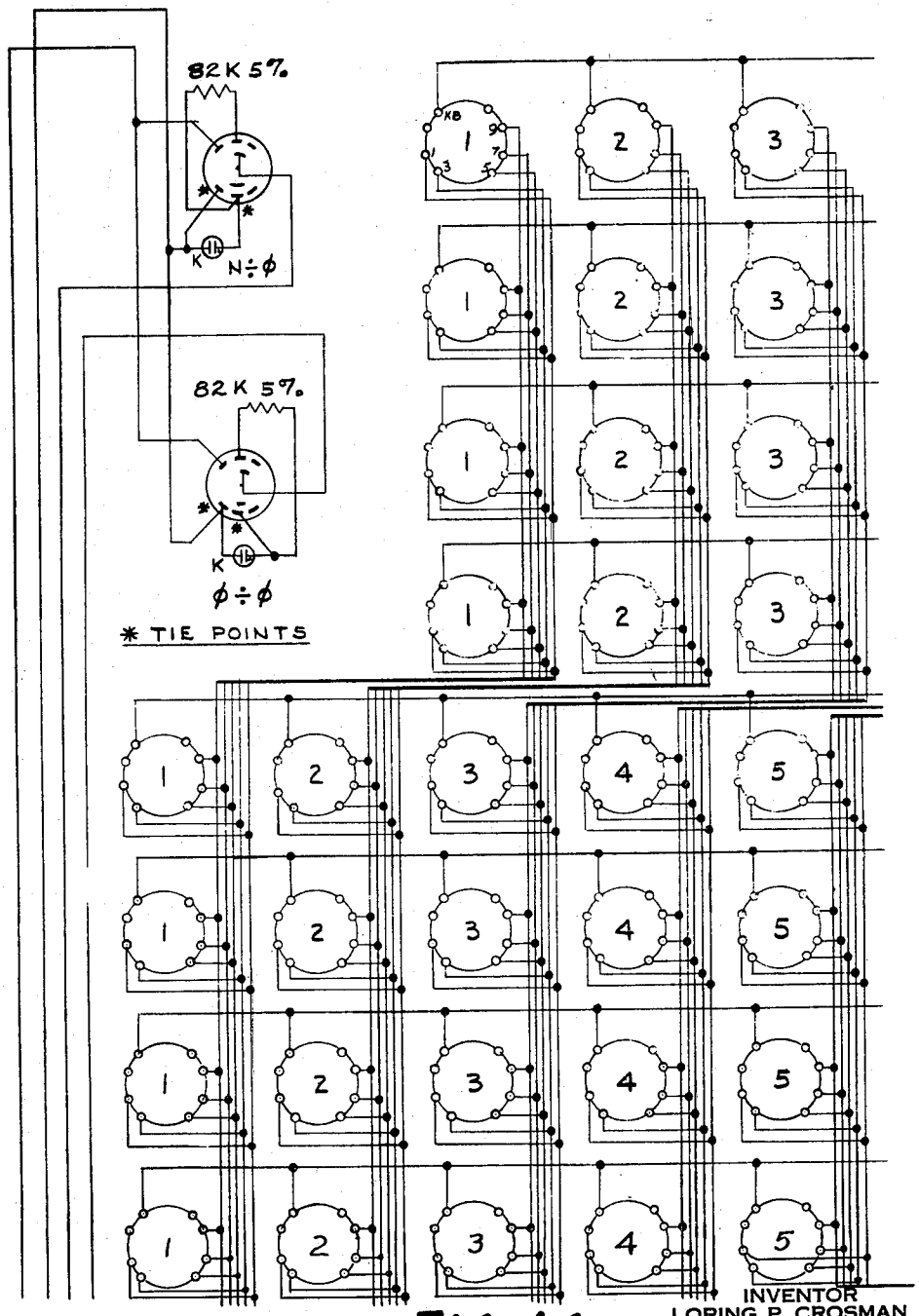


FIG. 46a

FIG. 46a	FIG. 46b	FIG. 46c
FIG. 46d	FIG. 46e	FIG. 46f

FIG. 46g

INVENTOR
LORING P. CROSMAN
BY George V. Illyinth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 185

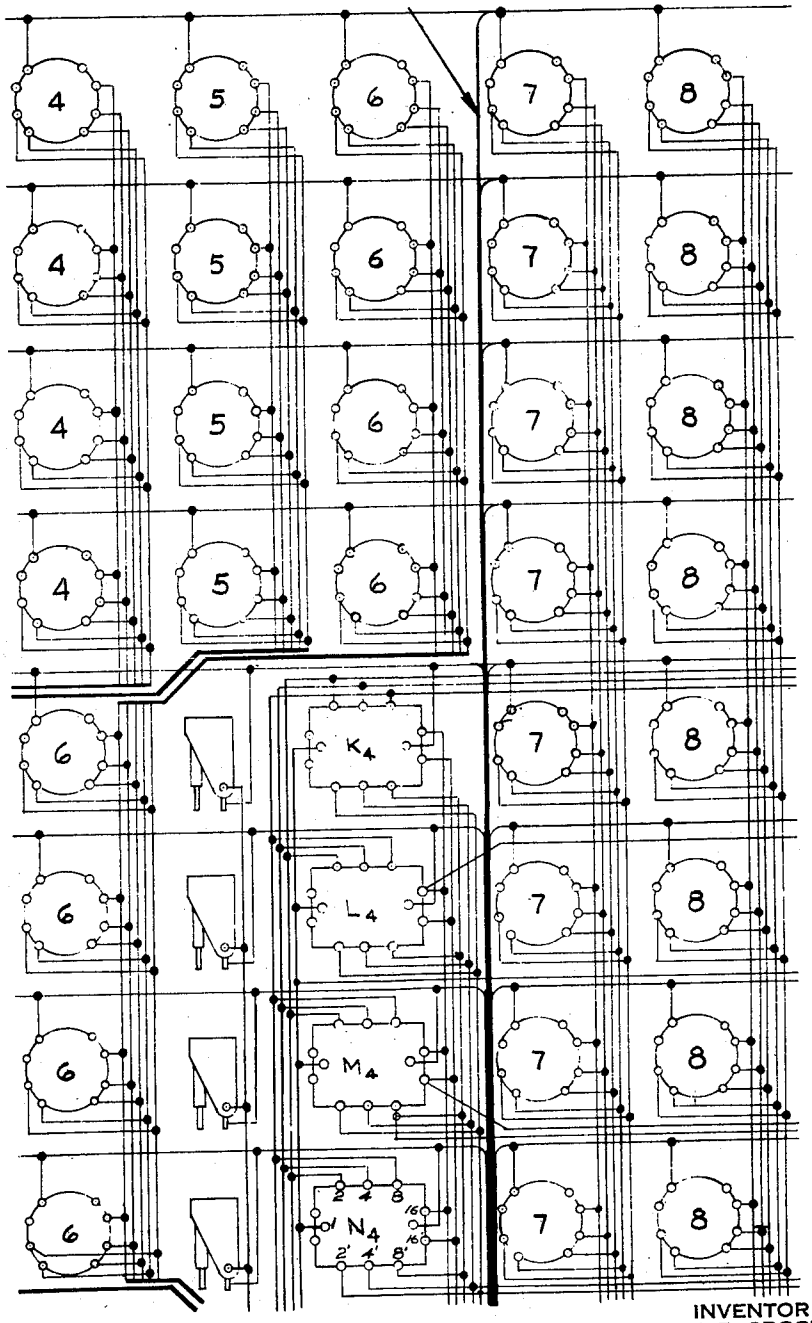


FIG. 46b

INVENTOR
LORING P. CROSMAN

BY George V. Fitzpatrick

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 186

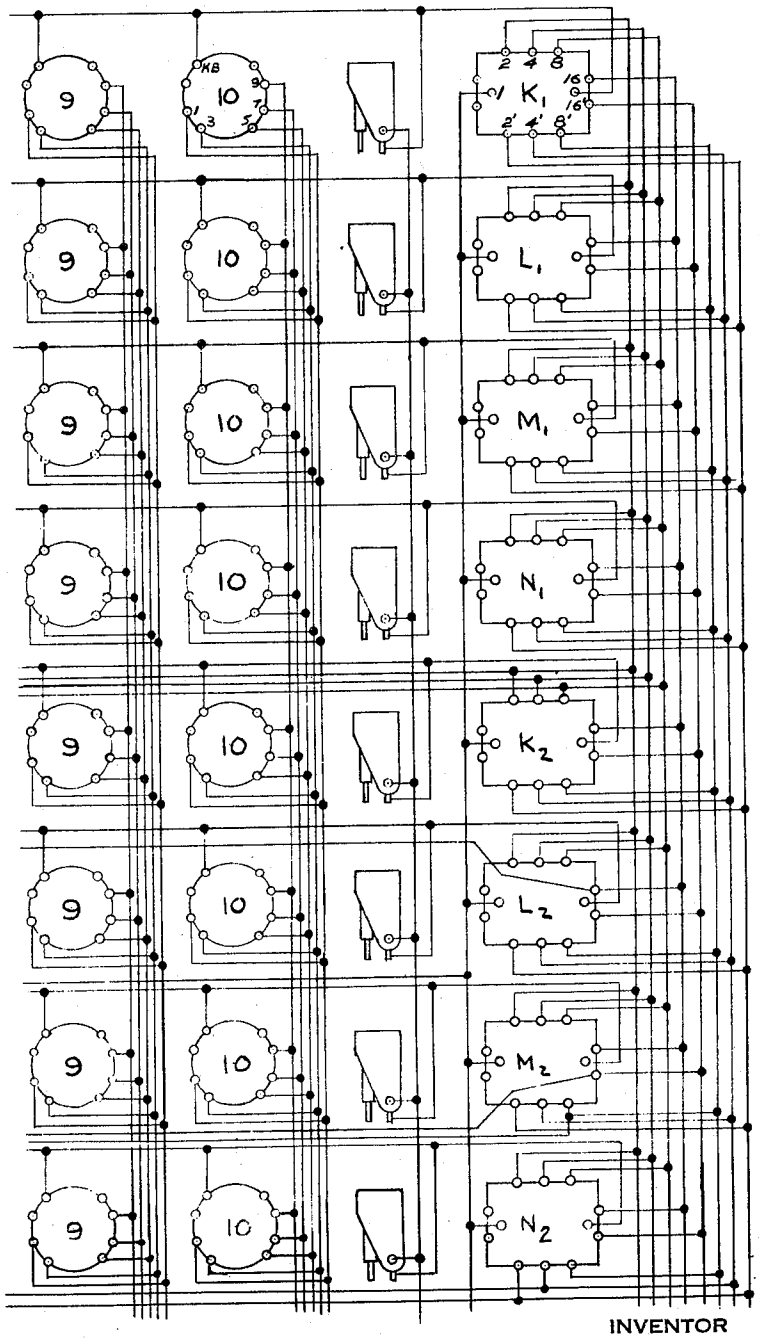


FIG. 46c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 187

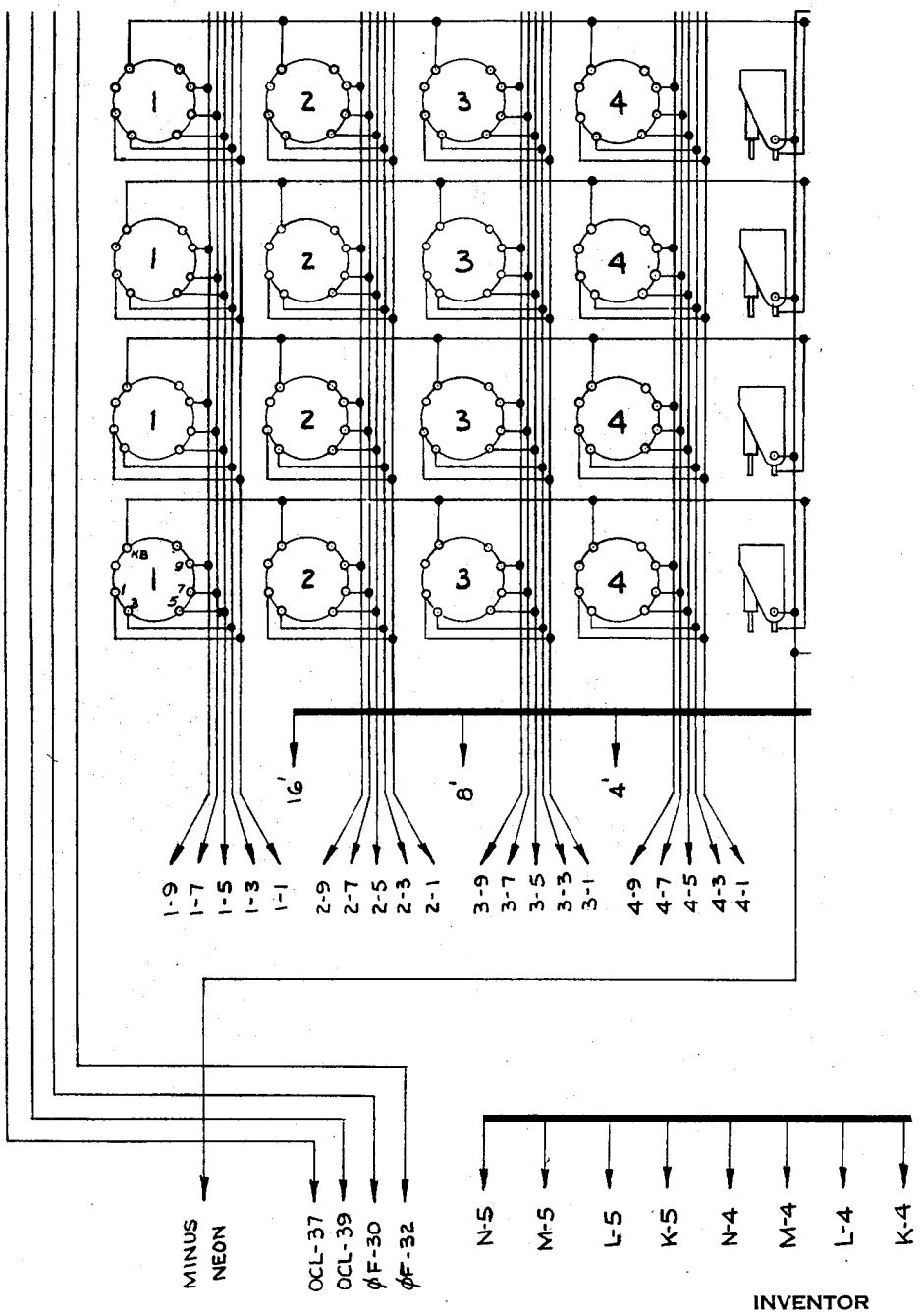


FIG. 46d

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 188

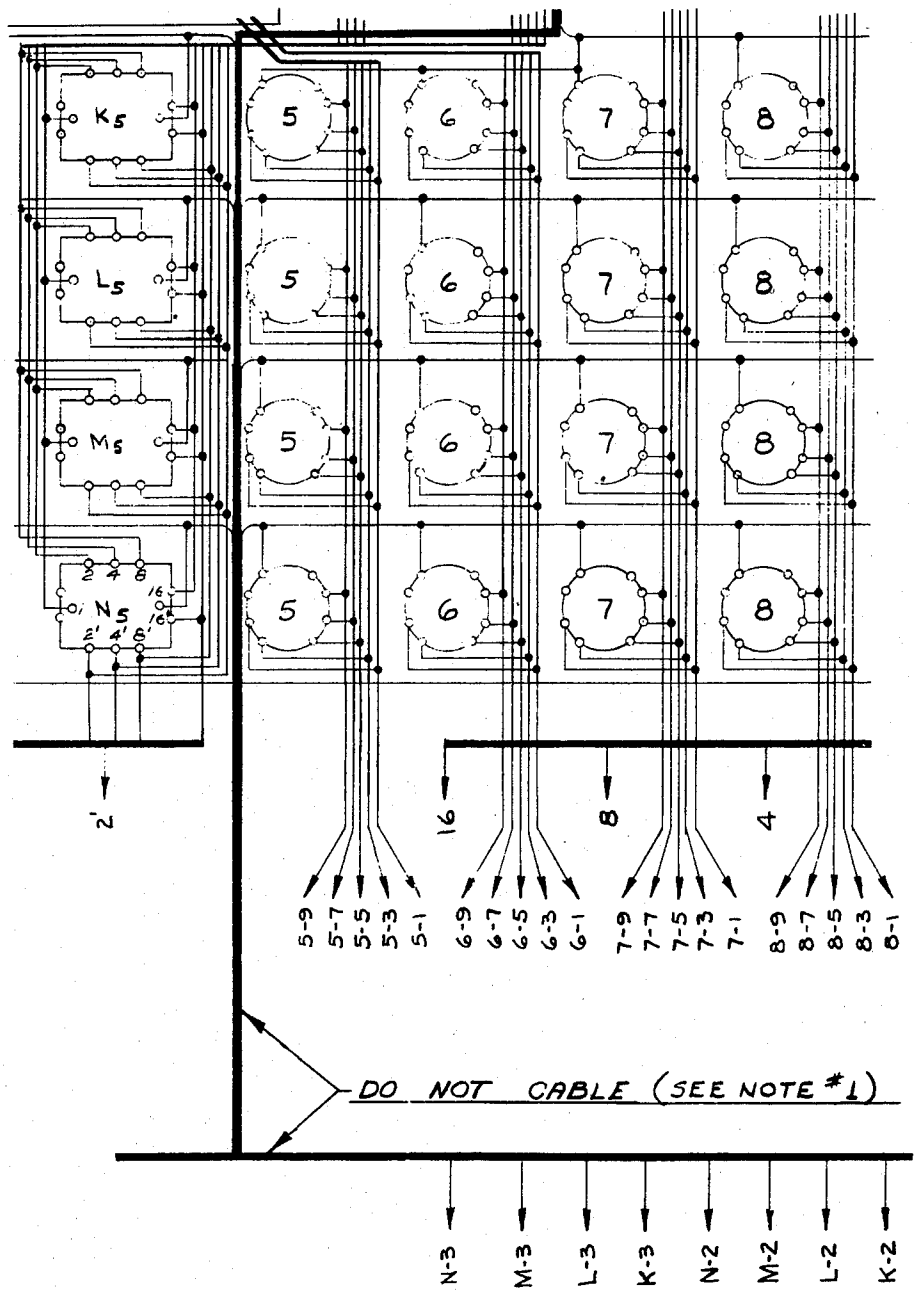
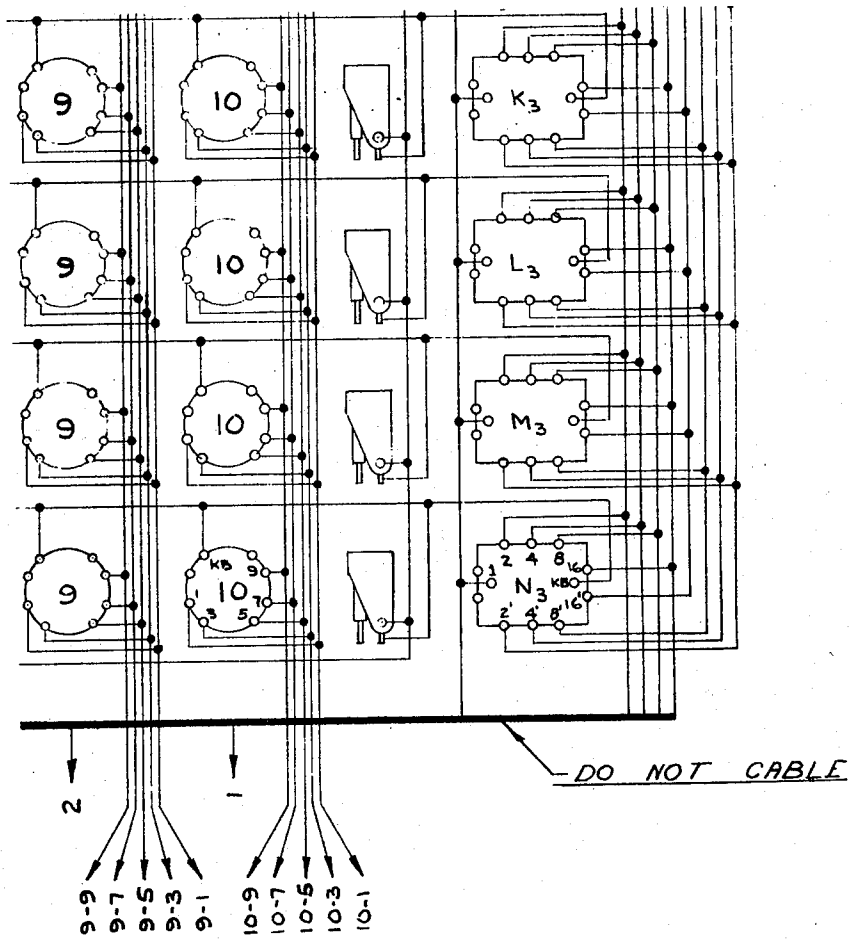


FIG. 46e

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 189



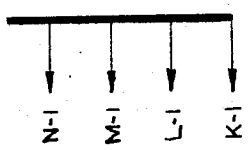


FIG. 46f

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

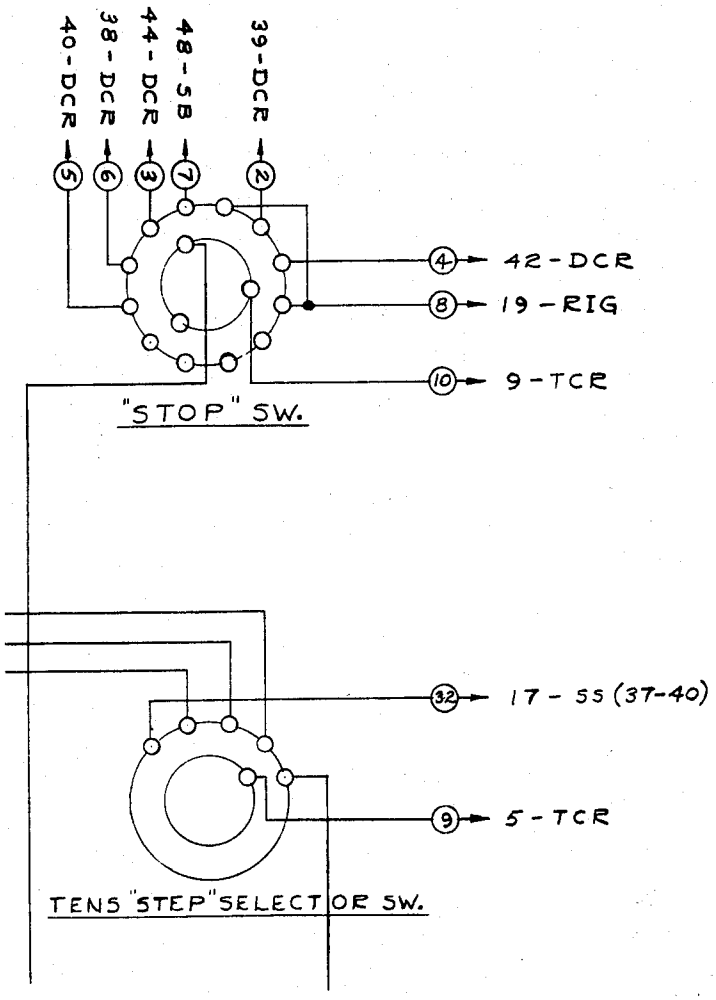


FIG. 47a

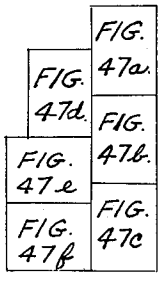


FIG. 47g

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BY George V. Eltgroth
ATTORNEY

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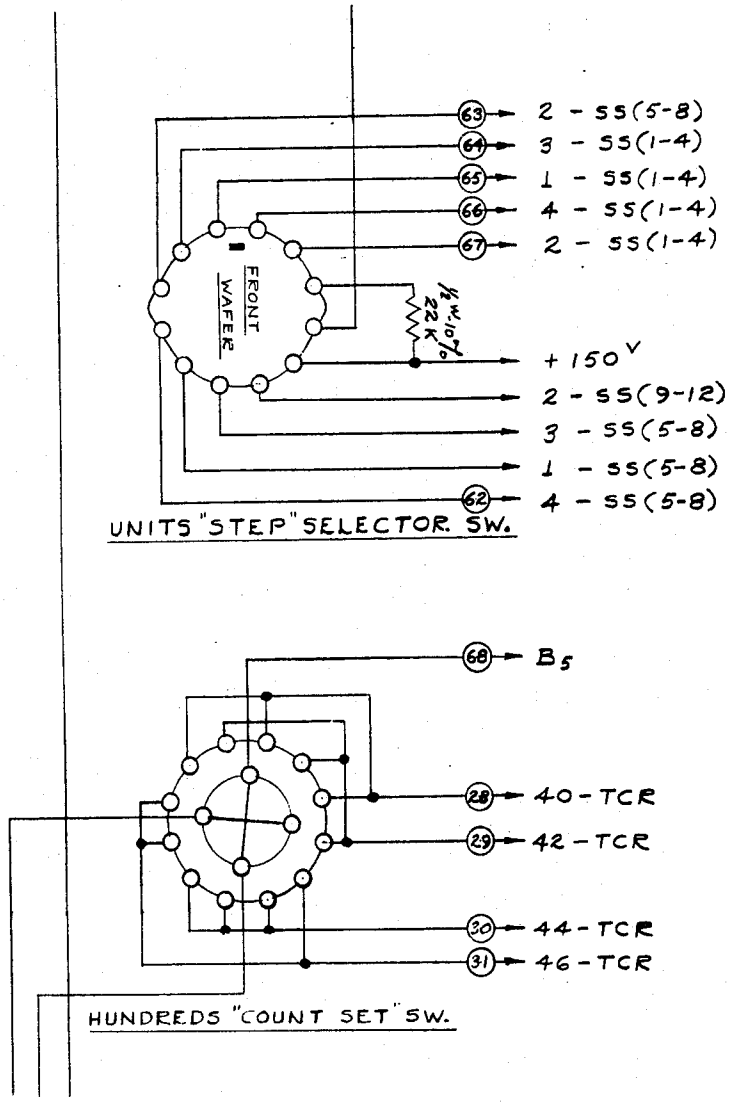


FIG. 47b

INVENTOR
LORING P. CROSMAN
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ATTORNEY

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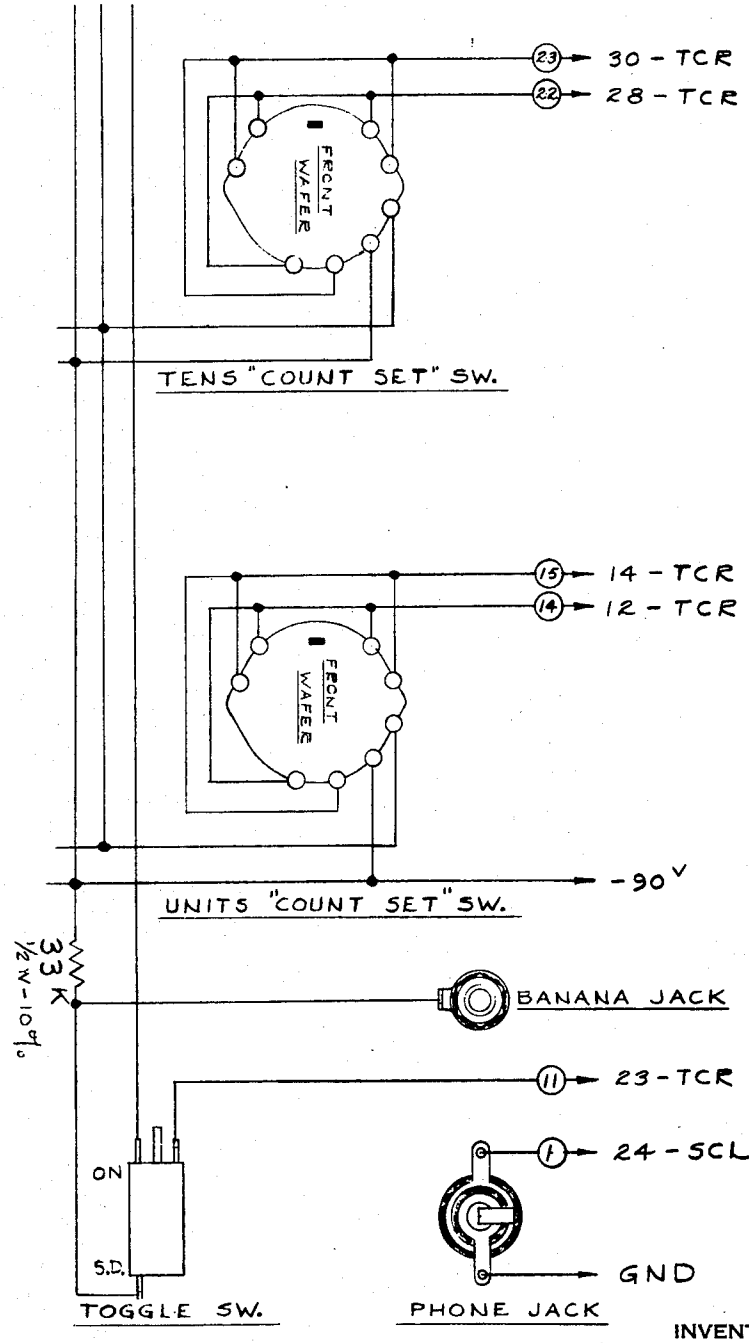


FIG. 47c

INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

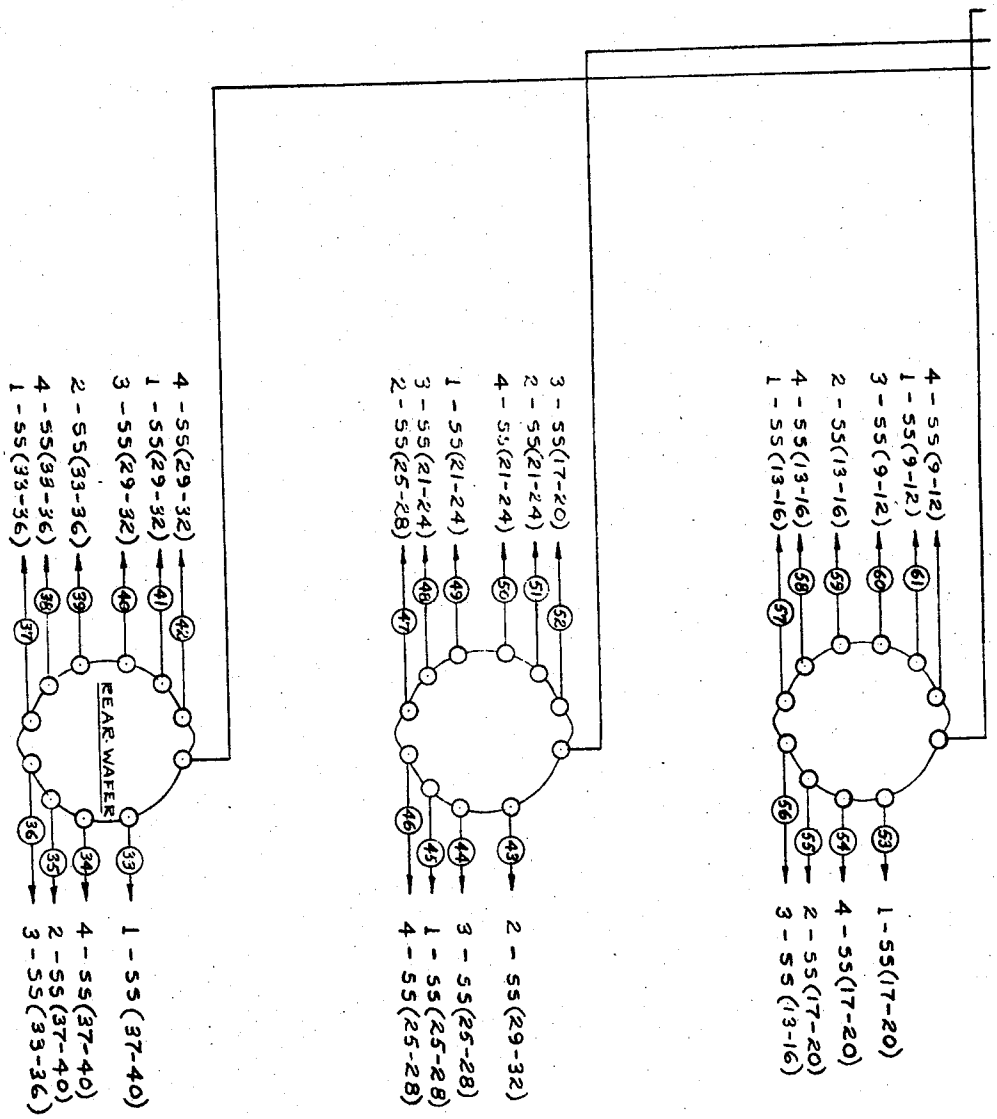


FIG. 47d

INVENTOR
LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

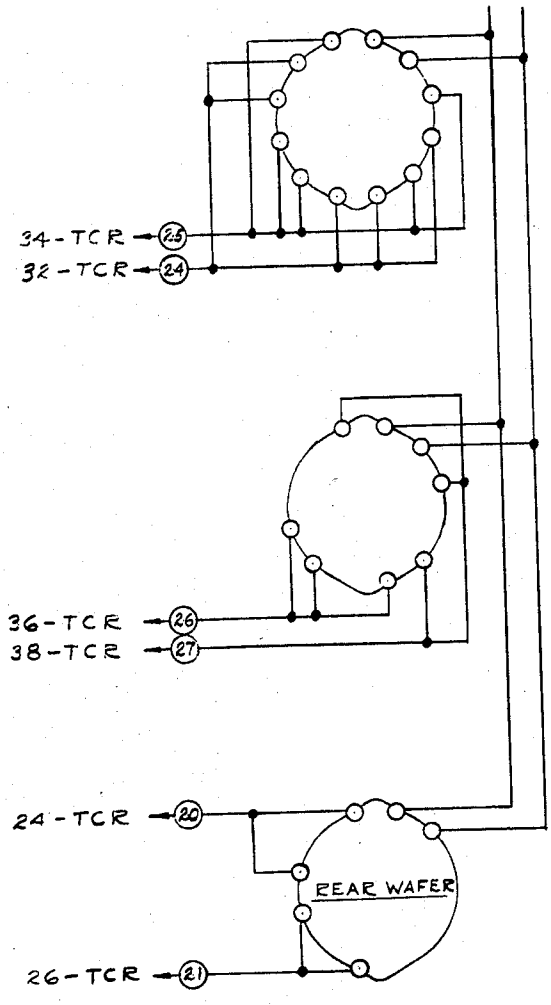


FIG. 47a

INVENTOR
LORING P. CROSMAN
BY George V. Ellgroth
ATTORNEY

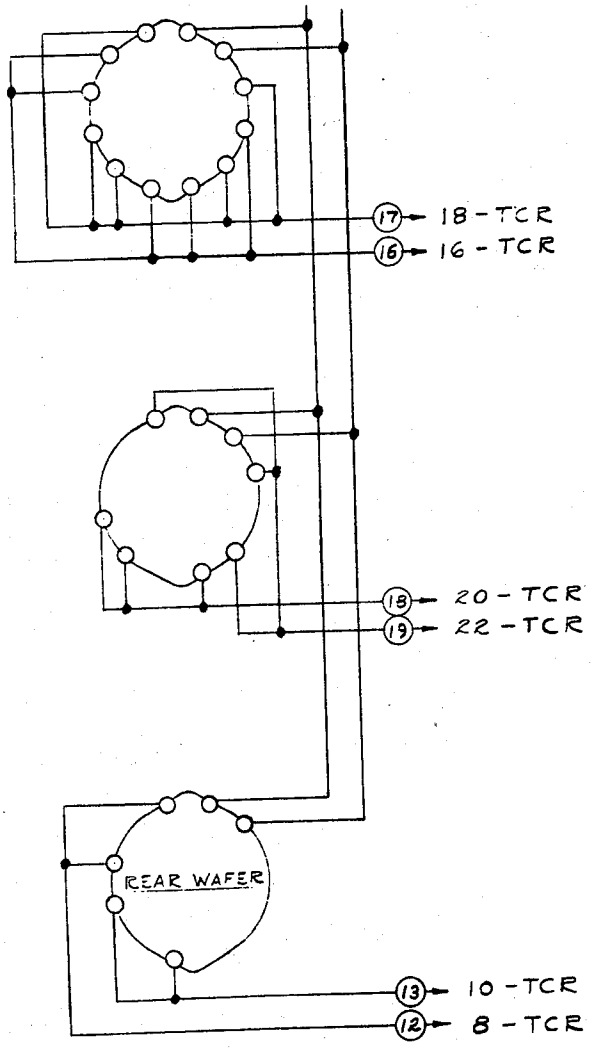


FIG. 47B

INVENTOR
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Oct. 4, 1960 L. P. CROSMAN 2,954,926

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Filed Jan. 13, 1953 242 Sheets-Sheet 196

FIG. 48a

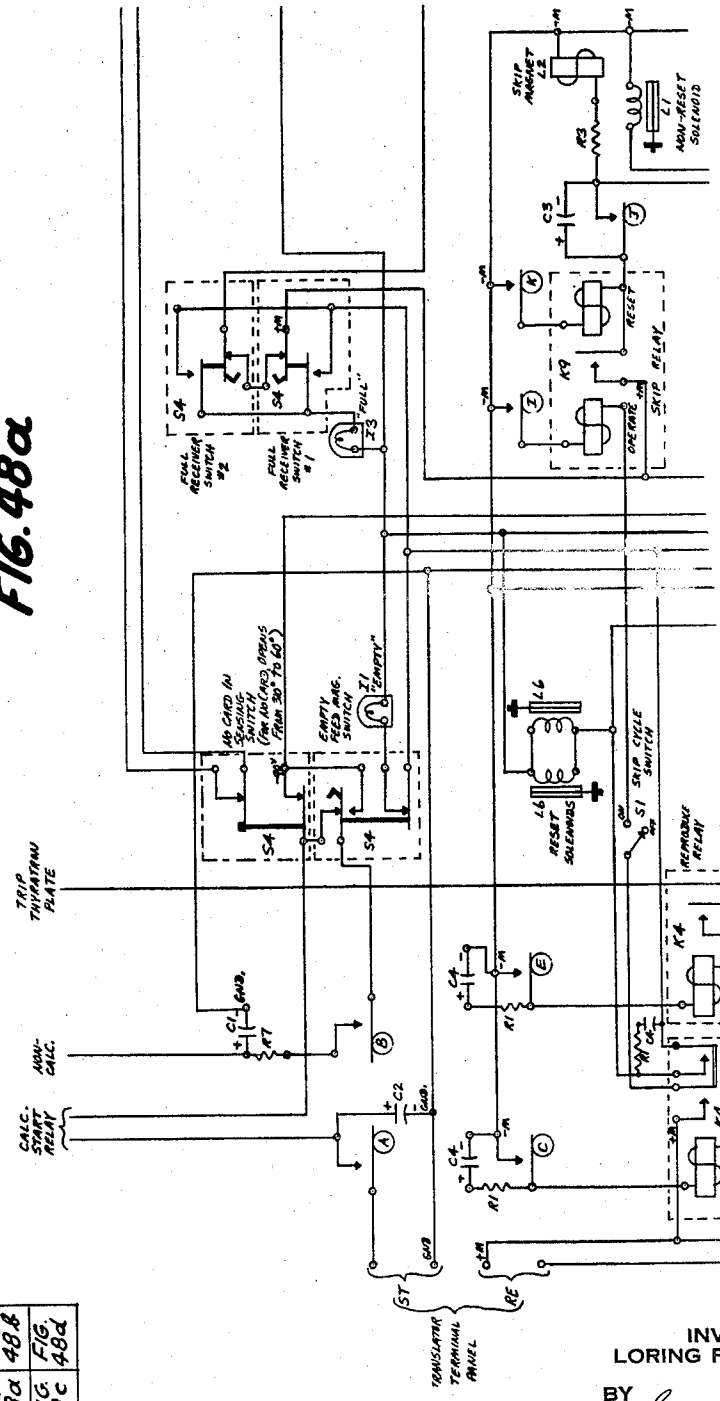


FIG. 48e

FIG. 48a	FIG. 48b
FIG. 48c	FIG. 48d

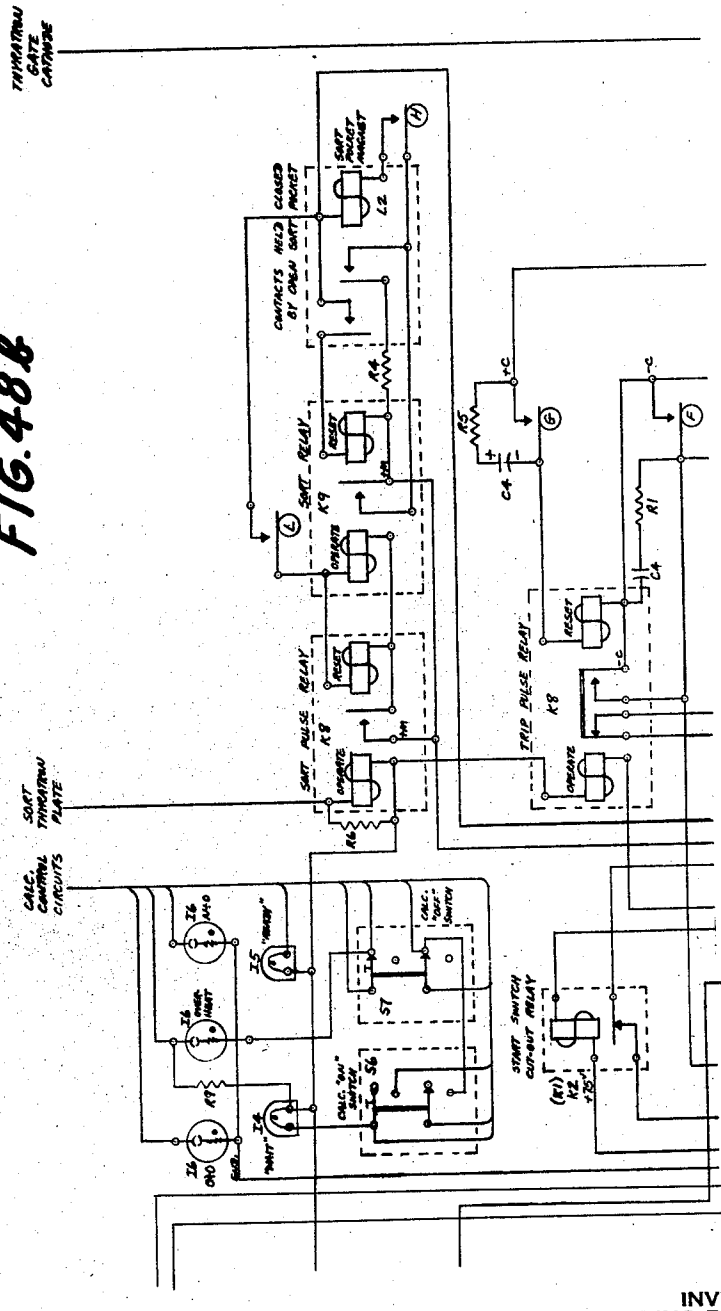
INVENTOR
LORING P. CROSMAN
BY George V. Eltgroth
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

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FIG. 488



INVENTOR
LORING P. CROSMAN

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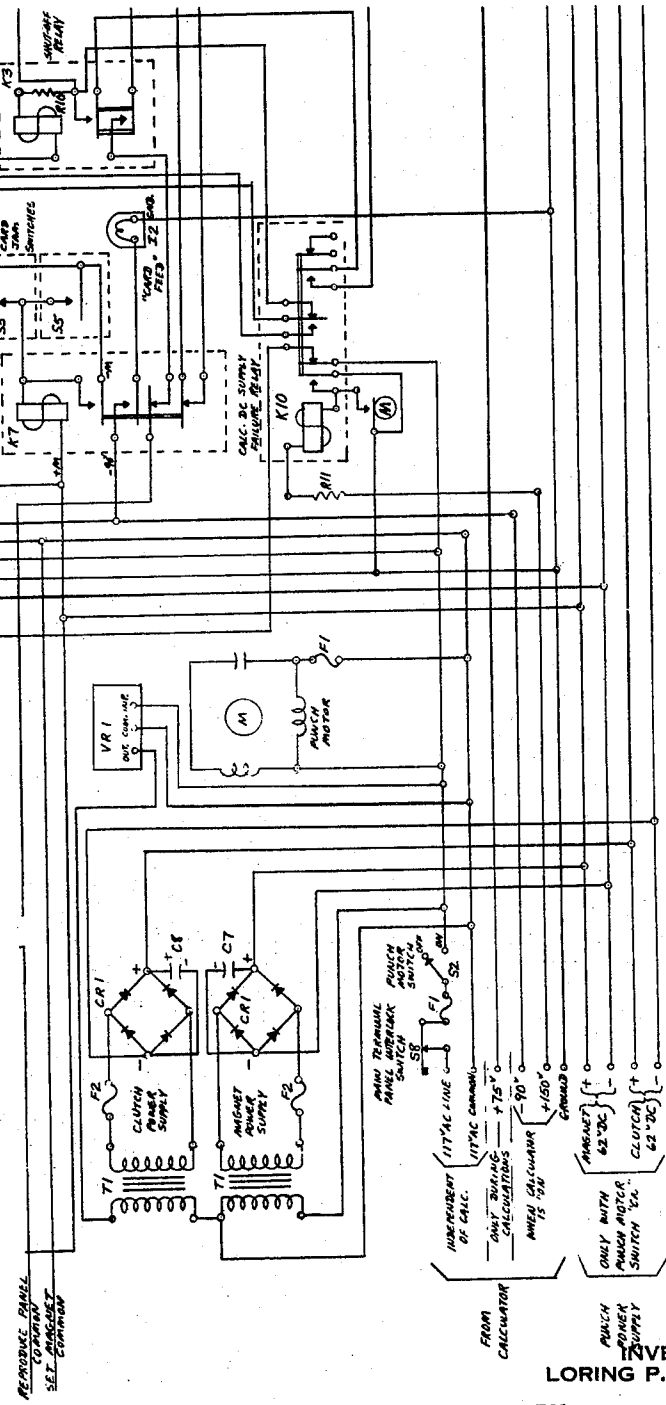


FIG. 48c

INVENTOR
LORING P. CROSMAN

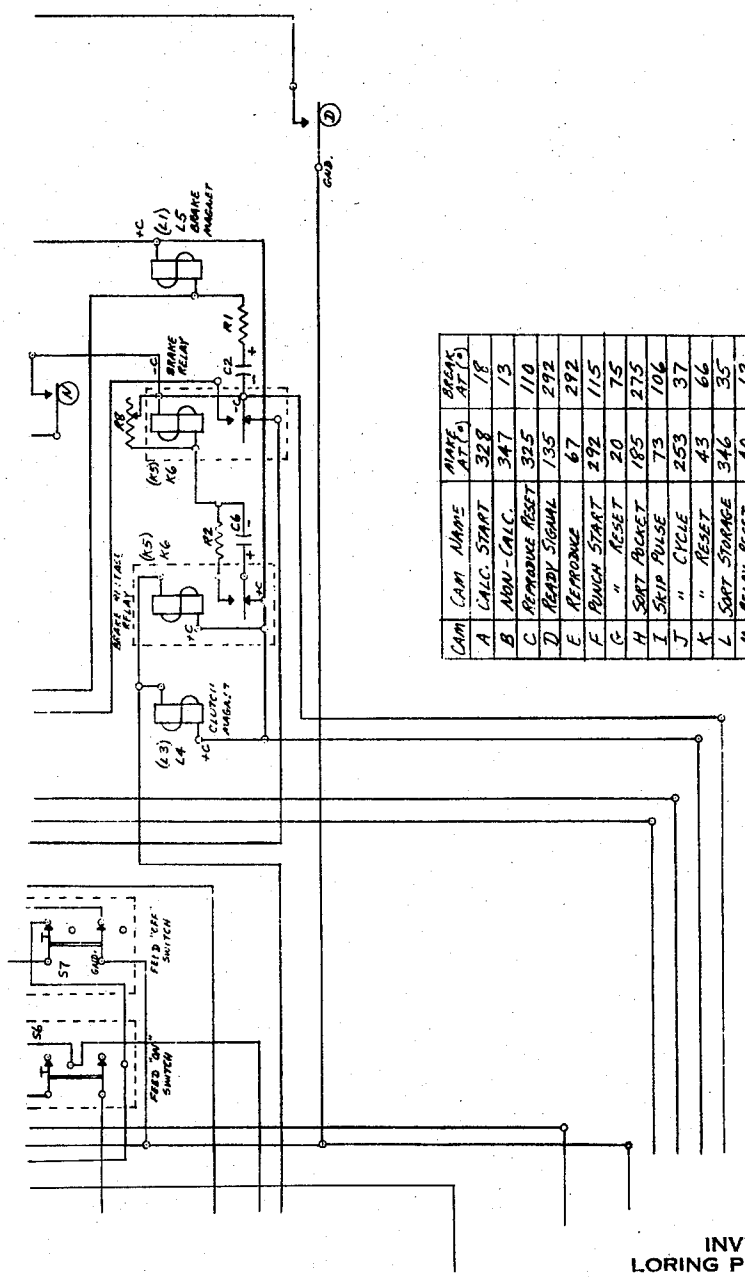
BY George V. Eltgroth

ATTORNEY

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Filed Jan. 13, 1953 242 Sheets-Sheet 199

FIG. 48 d



CAM	CAM NAME	MAKE AT (°)	BREAK AT (°)
A	CALC. START	328	18
B	ADD-CALC.	347	13
C	REMOVE RESET	325	110
D	READY SIGNAL	135	292
E	RETRONIC	67	292
F	PUNCH START	292	115
G	" RESET	20	75
H	SORT PULSE	185	275
I	SKIP PULSE	73	106
J	" CYCLE	253	37
K	" RESET	43	66
L	SORT STORAGE	346	35
M	RELAY RESET	40	63
N	PUNCH STOP	12 *	196 *

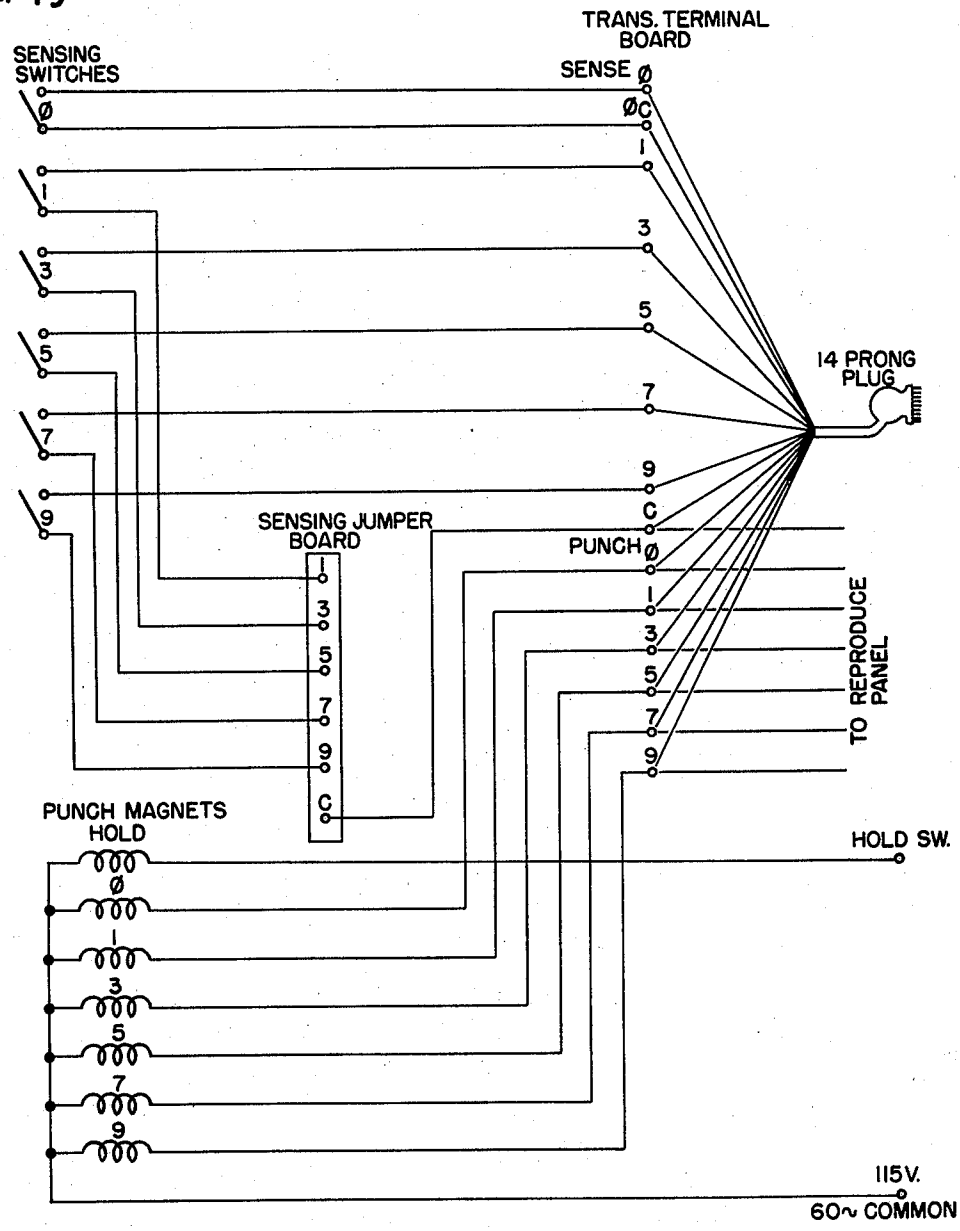
INVENTOR
LORING P. CROSMAN
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FIG. 49

CARD SENSING (TYPICAL COLUMN)



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FIG. 50

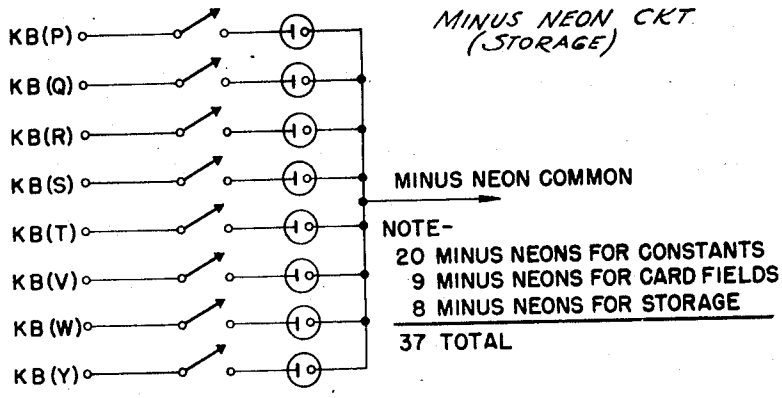


FIG. 51

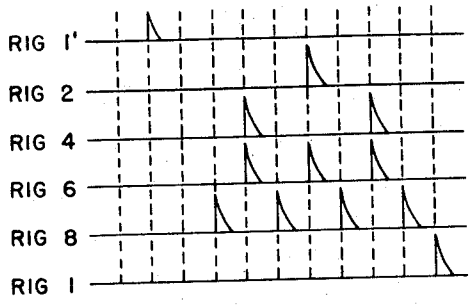


FIG. 52

DIGIT	90 COL. CODE	BI-Q CODE	PULSE REQUIRED ON ODD LINE	PULSES REQUIRED ON EVEN LINE
1	1	1,0	RIG 1	
2	1,9	2	RIG 1+1'	
3	3	1,2	RIG 1	RIG 2
4	3,9	4	RIG 1+1'	RIG 2
5	5	1,4	RIG 1	RIG 4
6	5,9	6	RIG 1+1'	RIG 4
7	7	1,6	RIG 1	RIG 6
8	7,9	8	RIG 1+1'	RIG 6
9	9	1,8	RIG 1'	RIG 8

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Filed Jan. 13, 1953 242 Sheets-Sheet 202

DIGIT	ME K	MO K	MI7 RIGHT K	MI7 RIGHT G	MI7 RIGHT P	MI3 LEFT K	MI3 LEFT G	M35 LEFT K	M35 LEFT G	M35 LEFT P	MI3 RIGHT K	MI3 RIGHT G	M57 LEFT K	M57 LEFT G	M35 RIGHT P	M35 RIGHT K	M35 RIGHT G	MI7 LEFT K	MI7 LEFT G	MI7 LEFT P	M57 RIGHT K	M57 RIGHT G	MA9 LEFT K	MA9 LEFT G	M9 RIGHT P	M9 RIGHT G	M9 LEFT G	M9 LEFT P	
0		L				L	H				L	H		H							L	H							
1	L							L	H	H			L			L	H	L	H									9
2		L								H	L	H	L	H		L	H						L	H					
3	L		L	H	H						L	H		H				H	H										
4		L											L	H									L	H					
5	L							L	H						H														5
6		L				L	H				L	H			H								L	H					
7	L		L	H				L	H							L	H			H	L	H							
8		L				L	H				L	H	L	H									L	H					3
9	L		L	H				L	H							L	H	L	H										

FIG. 53

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Filed Jan. 13, 1953 242 Sheets-Sheet 203

FIG. 54 a

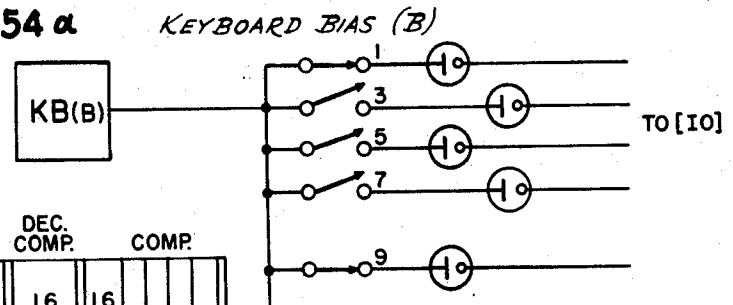
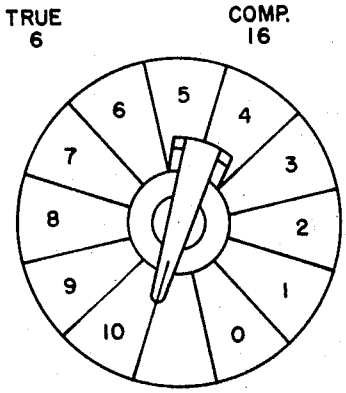


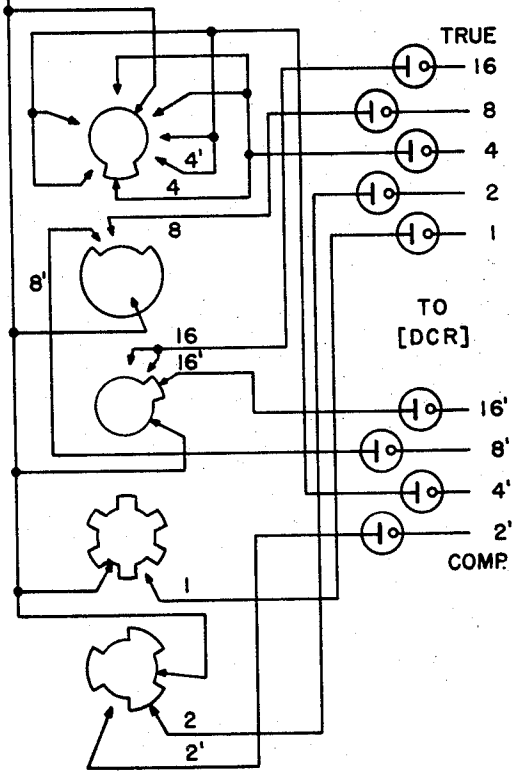
FIG. 54 b

DECIMAL	TRUE	DEC. COMP.	COMP.
6	4 2	16	16
7	4 2 1	15	8 4 2 1
8	8	14	8 4 2
9	8 1	13	8 4 1
10	8 2	12	8 4
11	8 2 1	11	8 2 1
12	8 4	10	8 2
13	8 4 1	9	8 1
14	8 4 2	8	8
15	8 4 2 1	7	4 2 1
16	16	6	4 2
17	16 1	5	4 1

FIG. 54c



DECIMAL SWITCH SETTING



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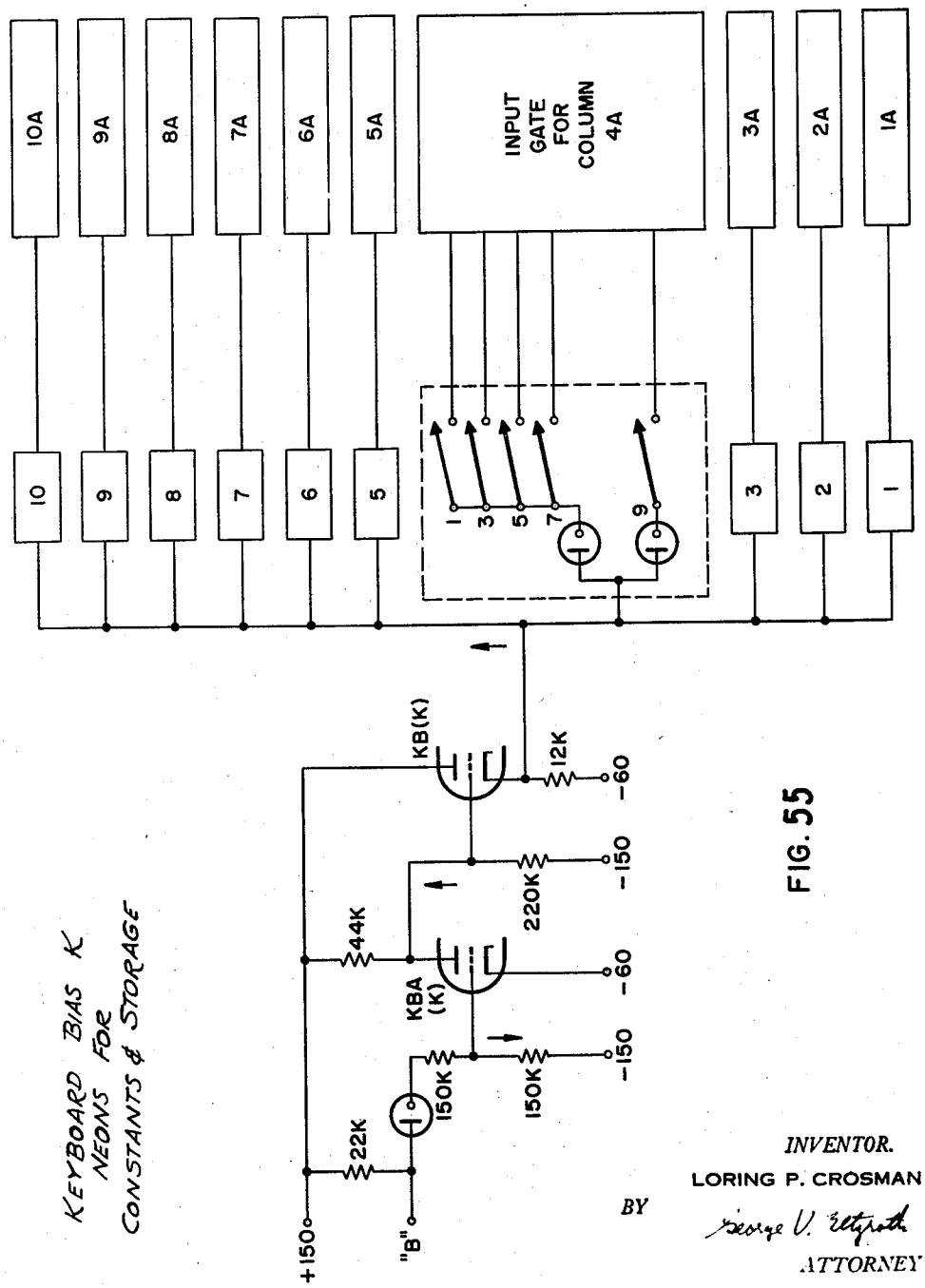
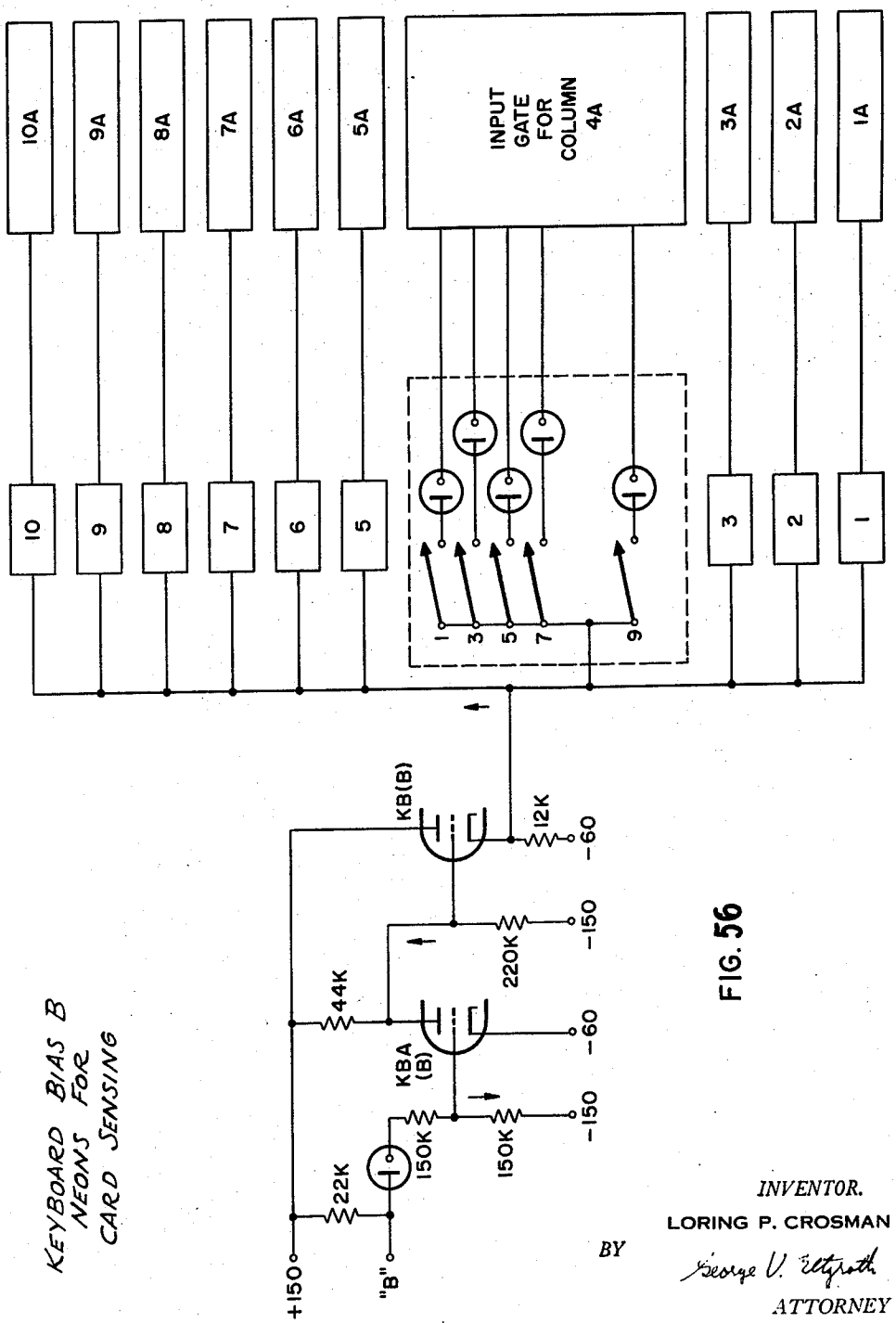


FIG. 55

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KEYBOARD BIAS B NEONS FOR CARD SENSING

FIG. 56

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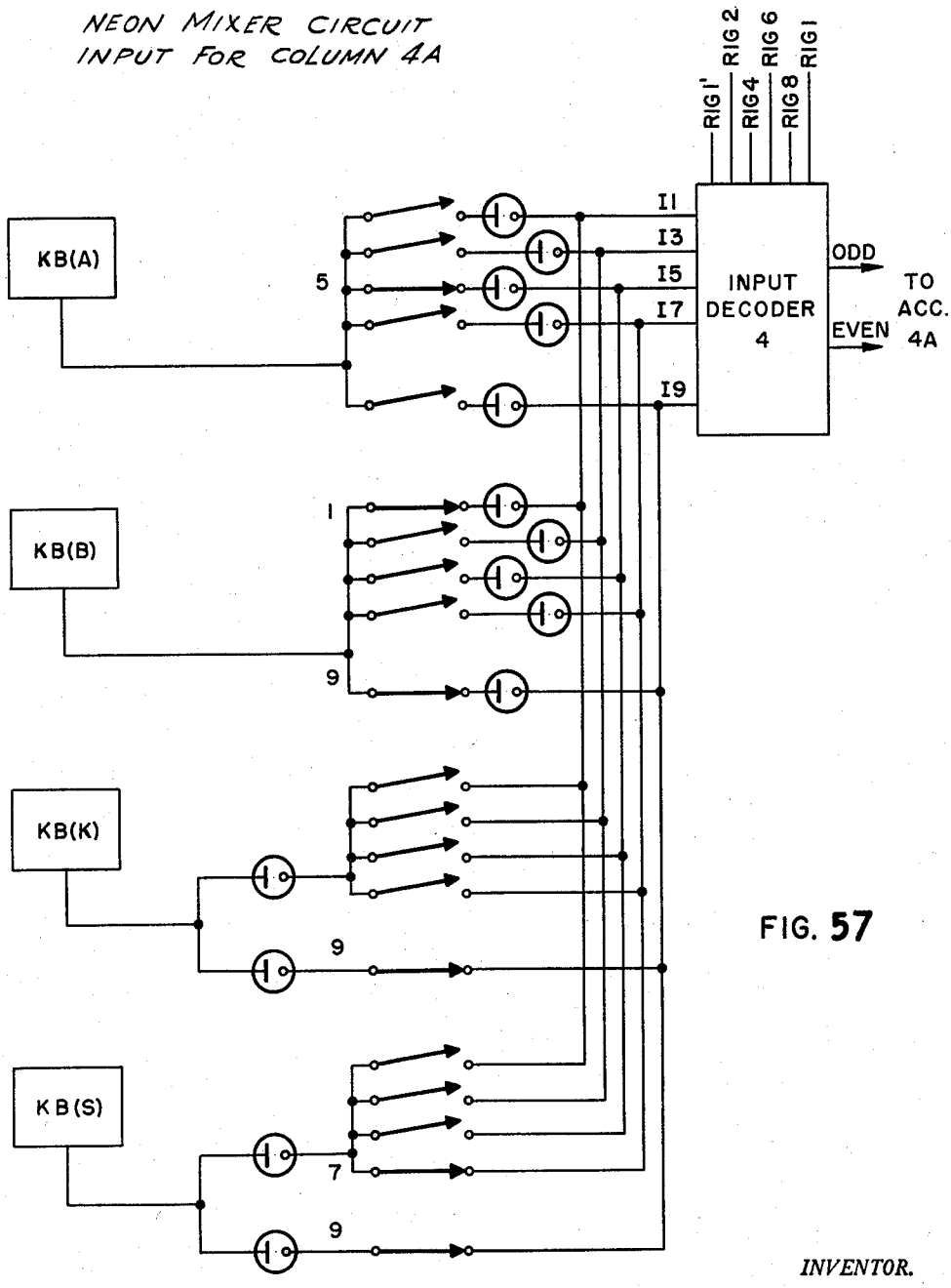


FIG. 57

INVENTOR.
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BY George V. Ectgroth

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FIG. 58

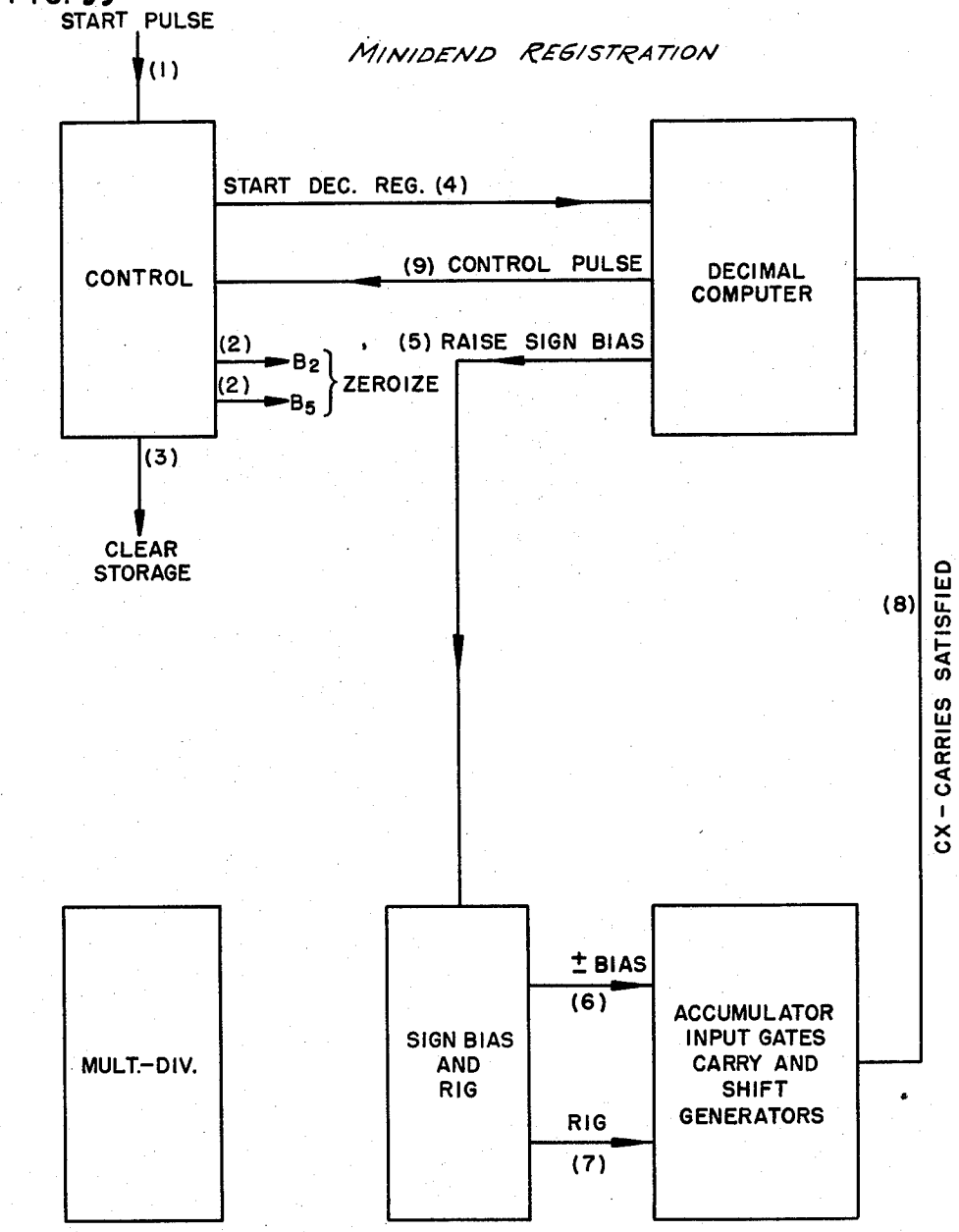
DEC. CTR.		16	-8	4	-2	1
0						
1						1
2				4	-2	
3				4	-2	1
4				4		
5				4		1
6		16	-8		-2	
7		16	-8		-2	1
8		16	-8			
9		16	-8			1
10		16	-8	4	-2	
11		16	-8	4	-2	1
12		16	-8	4		
13		16	-8	4		1
14		16			-2	
15		16			-2	1
16		16				
17		16				1
18		16		4	-2	
19		16		4	-2	1
20		16		4		
21		16		4		1
22			-8		-2	
23			-8		-2	1
24			-8			
25			-8			1
26			-8	4	-2	
27			-8	4	-2	1
28			-8	4		
29			-8	4		1
30					-2	
31					-2	1
32						
33						1
34				4	-2	
35				4	-2	1
36				4		
37				4		1
38		16	-8		-2	

INVENTOR.
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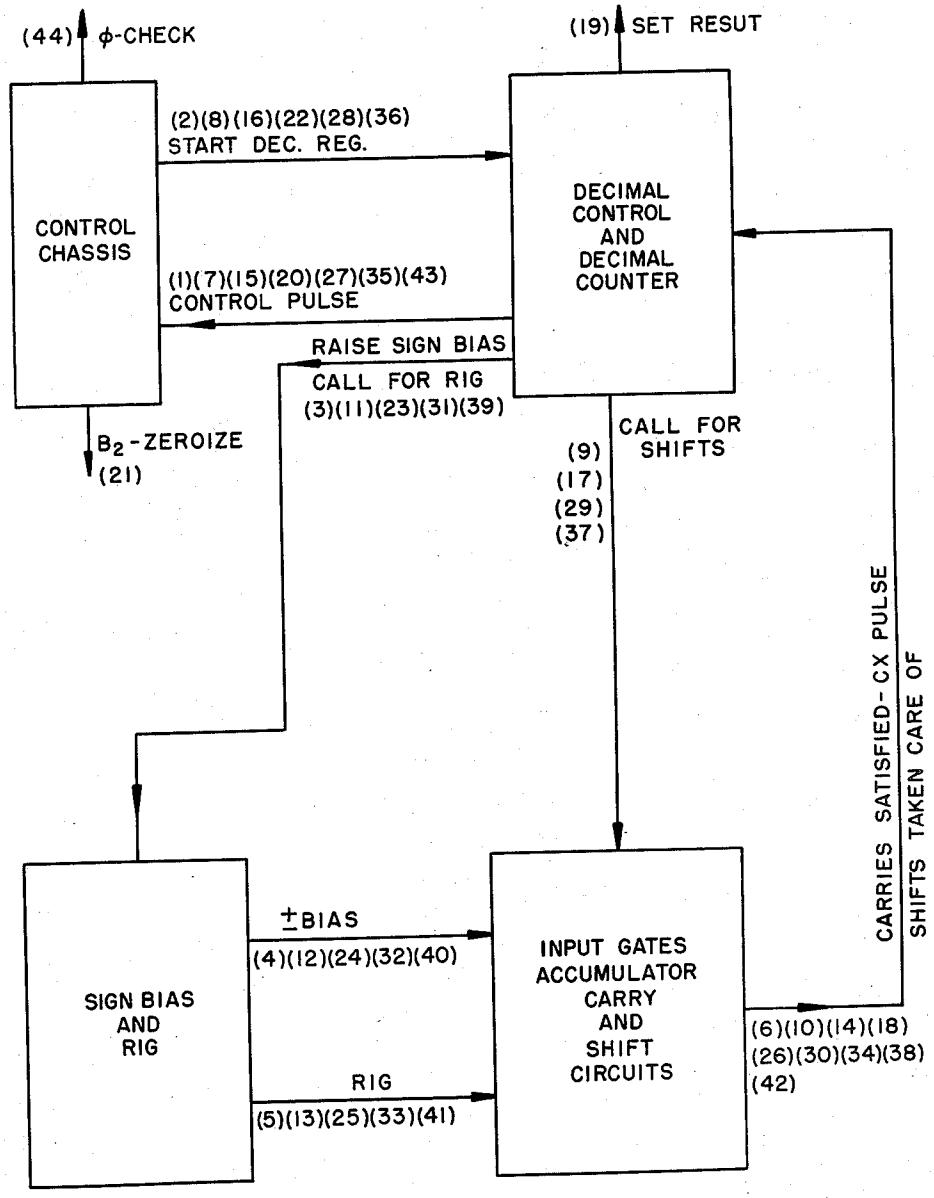
FIG. 59



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BY George V. Eltgroth
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FIG. 60

ADDITION & SUBTRACTION

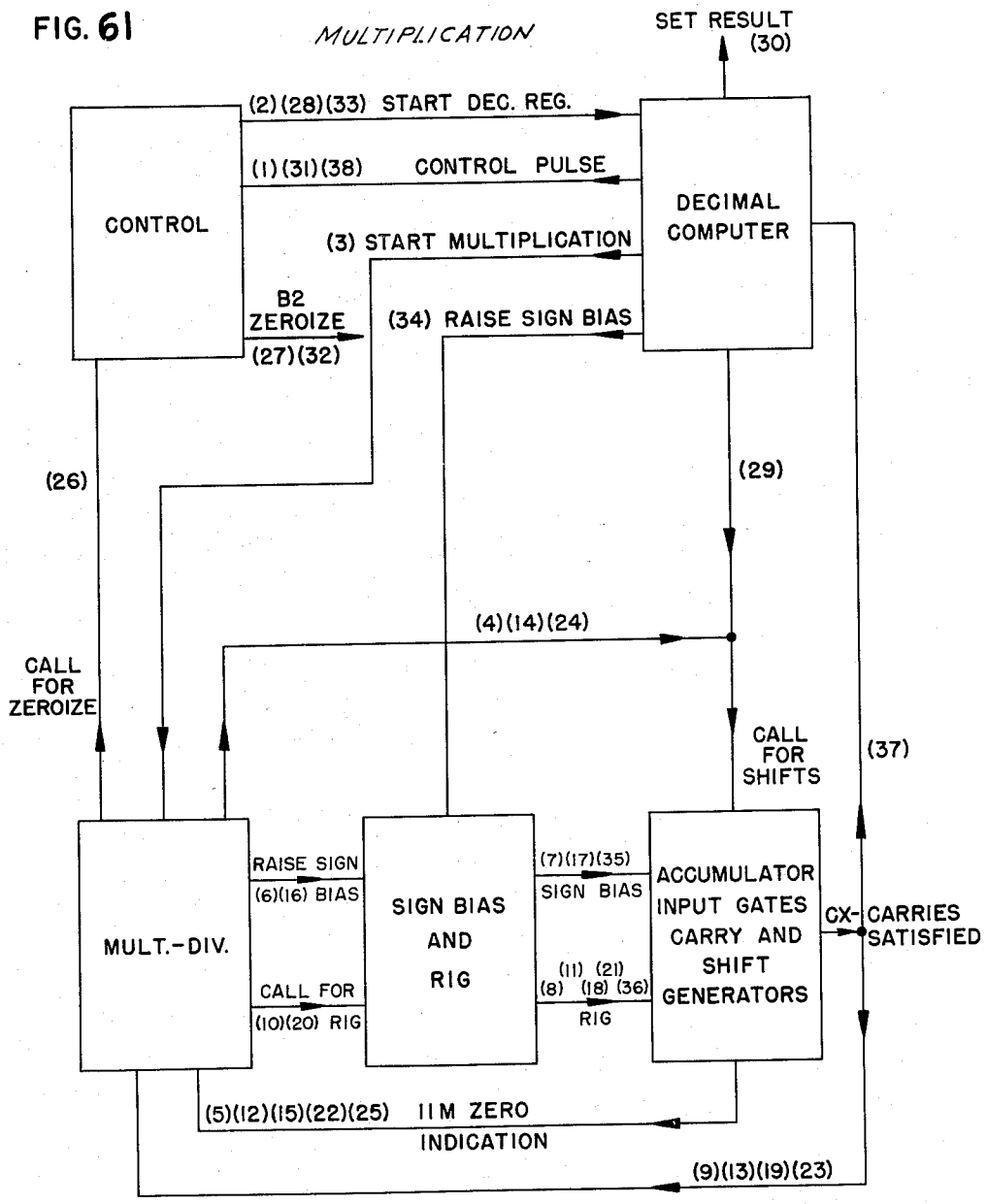


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FIG. 61

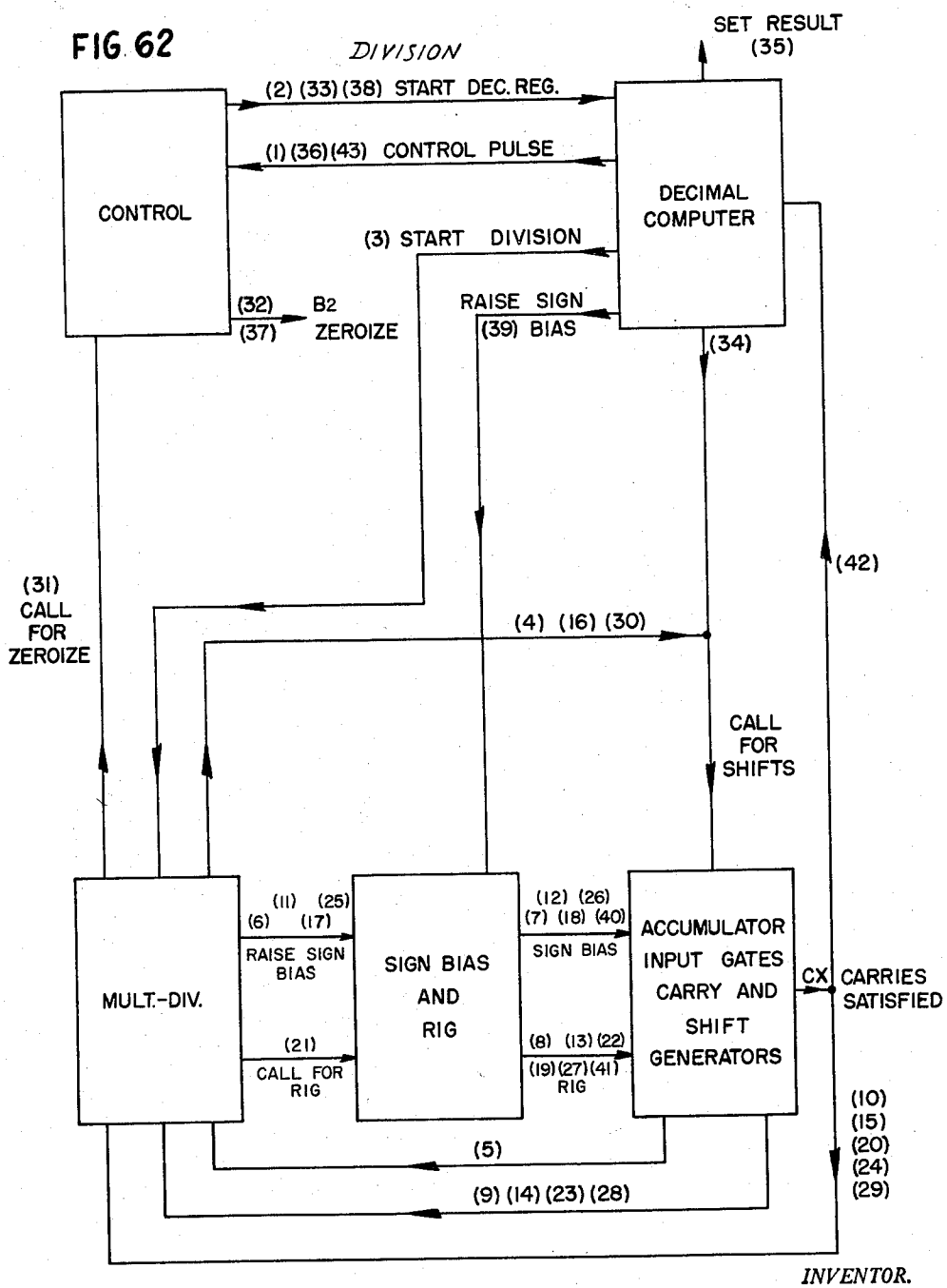


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FIG. 62



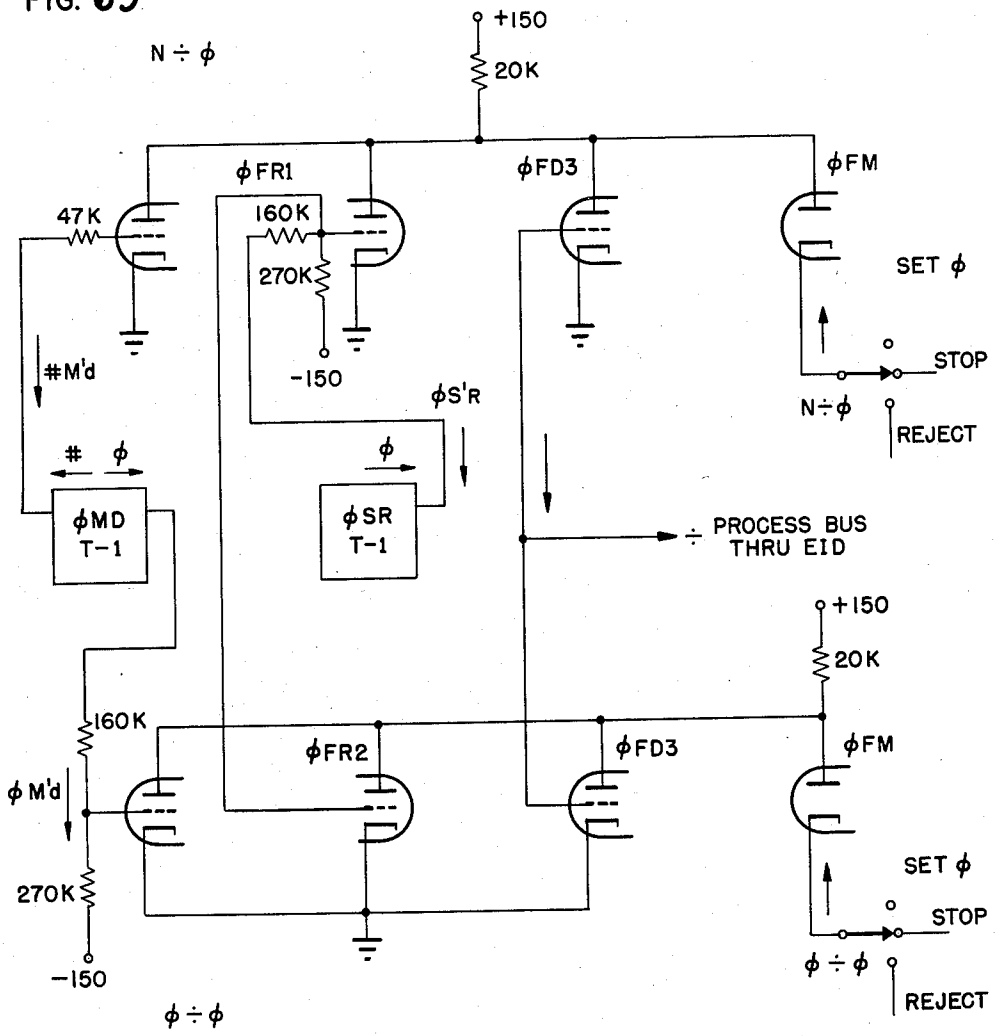
INVENTOR.
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FIG. 63

STOP & REJECT CKTS



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FIG. 64

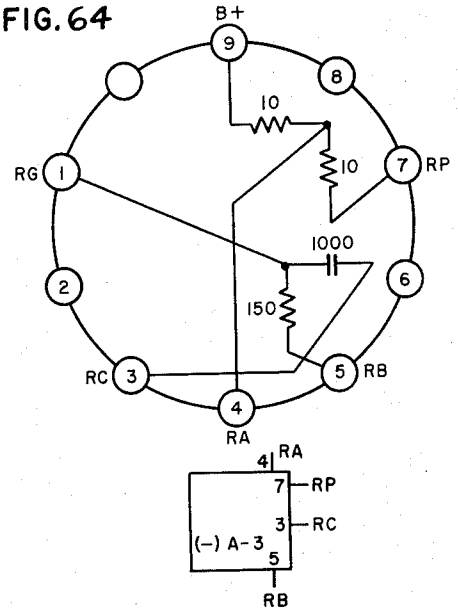


FIG. 65

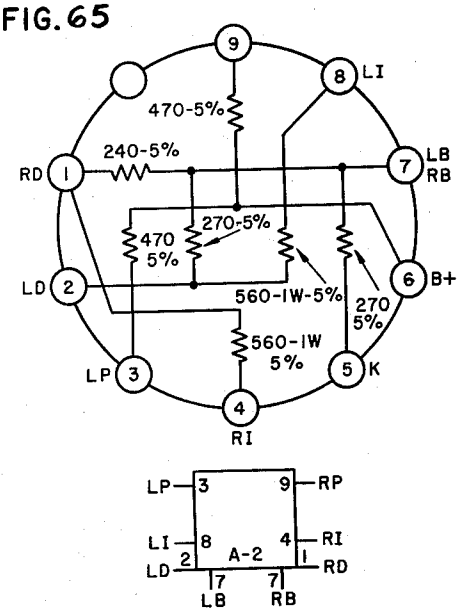


FIG. 66

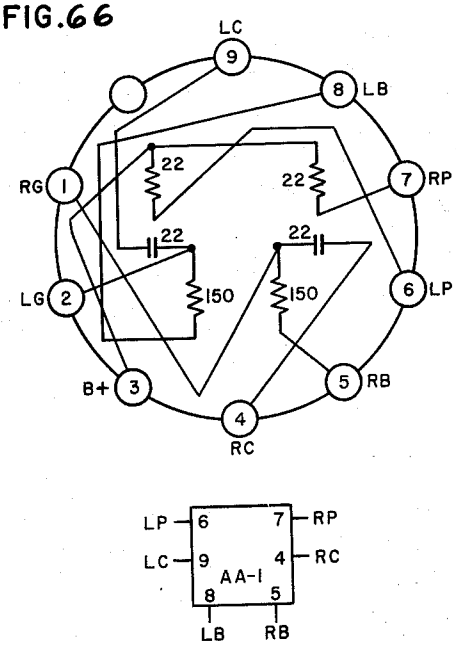
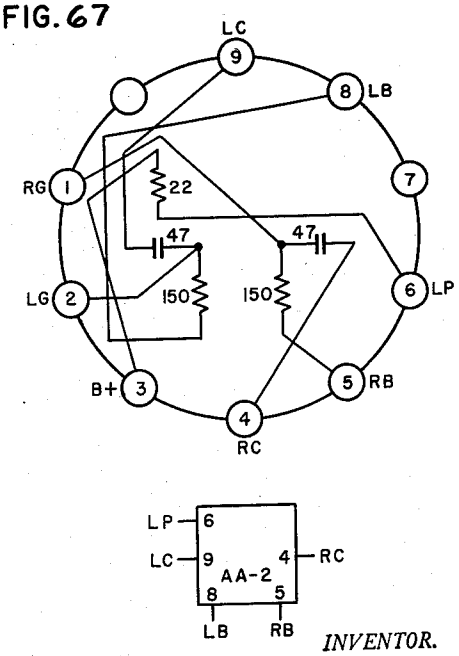


FIG. 67



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FIG. 68

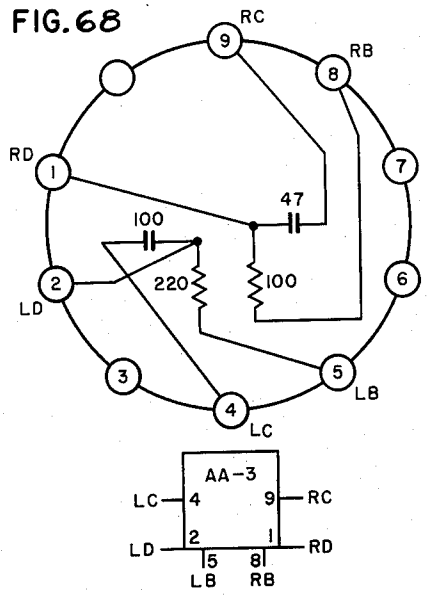


FIG. 69

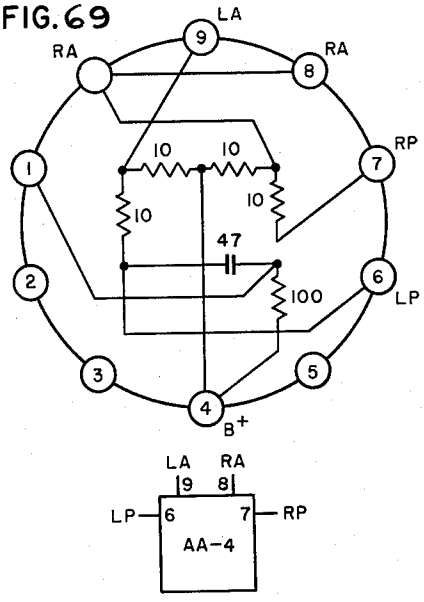


FIG. 70

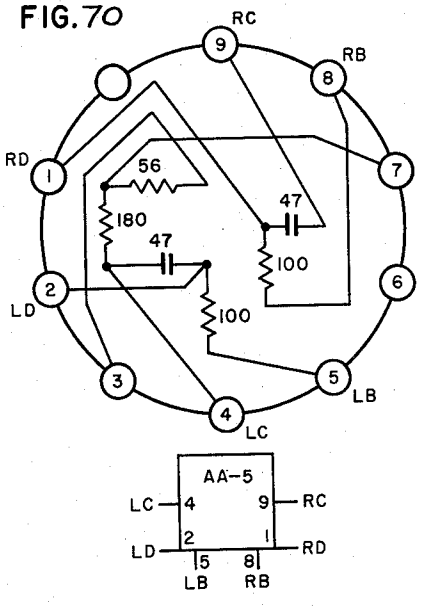
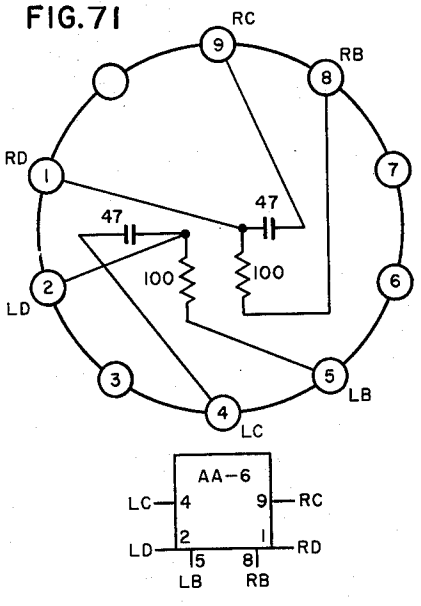


FIG. 71



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BY George V. Eltgroth

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FIG. 72

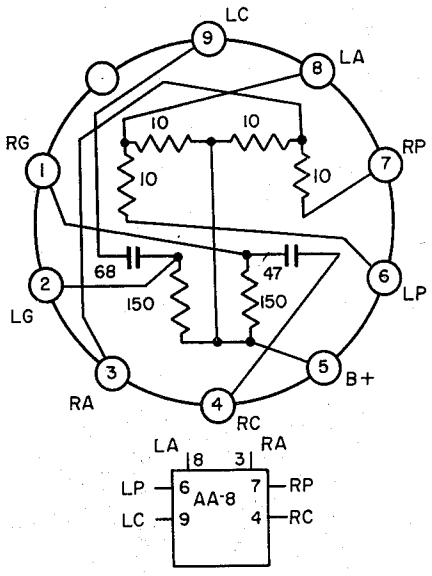


FIG. 73

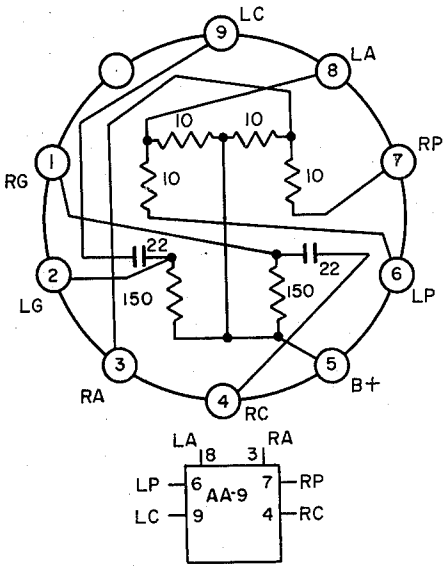


FIG. 74

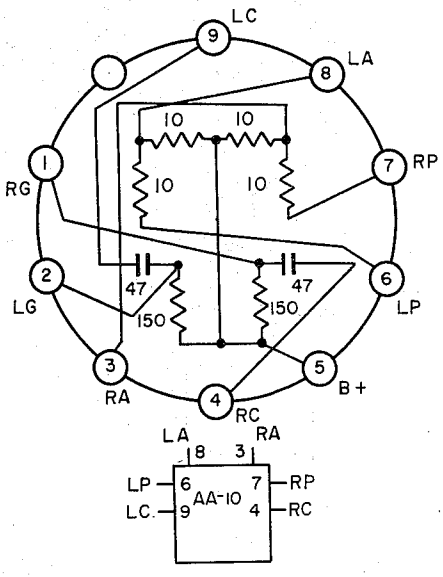
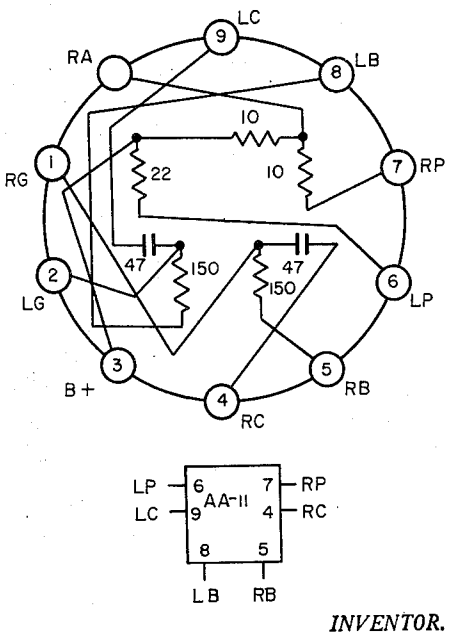


FIG. 75



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BY George V. Eltgroth

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FIG. 76

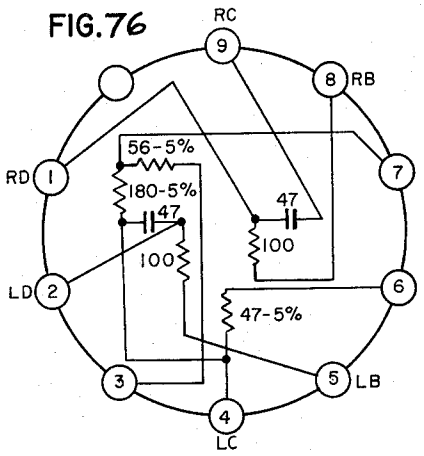


FIG. 77

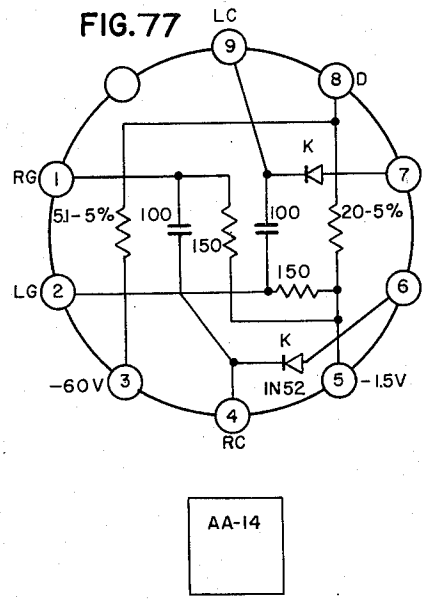


FIG. 78

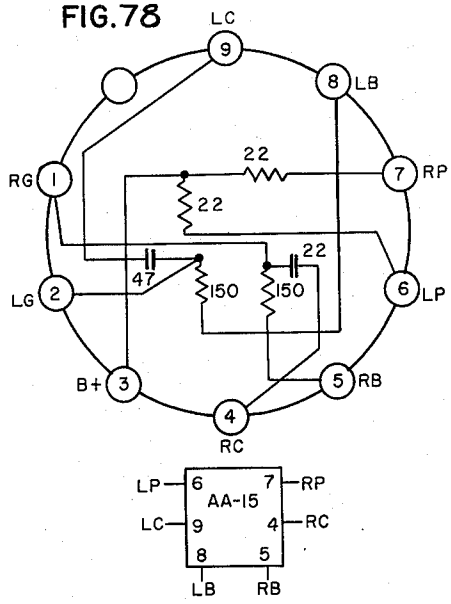
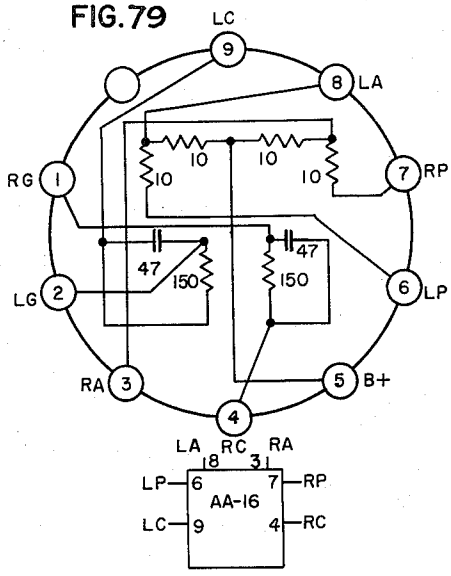


FIG. 79



INVENTOR.

LORING P. CROSMAN

BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 217

FIG. 80

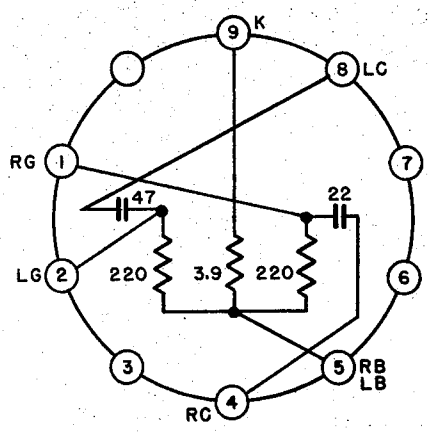


FIG. 81

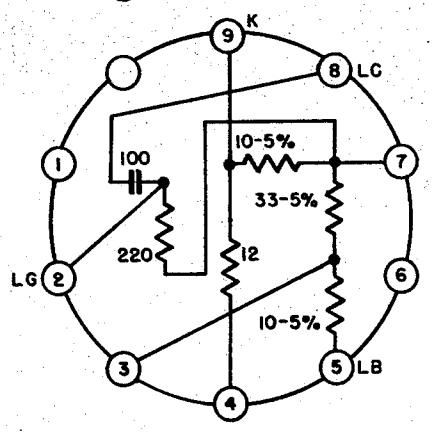


FIG. 82

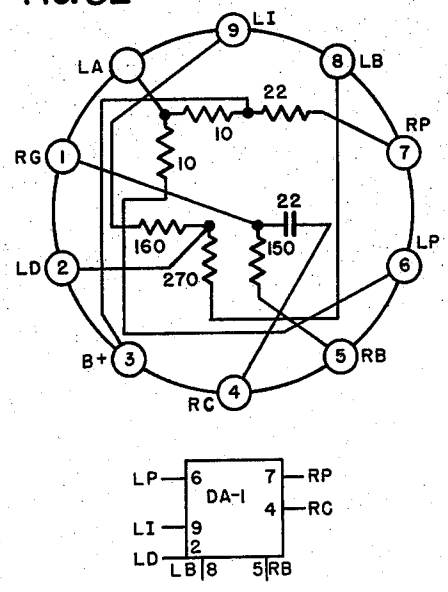
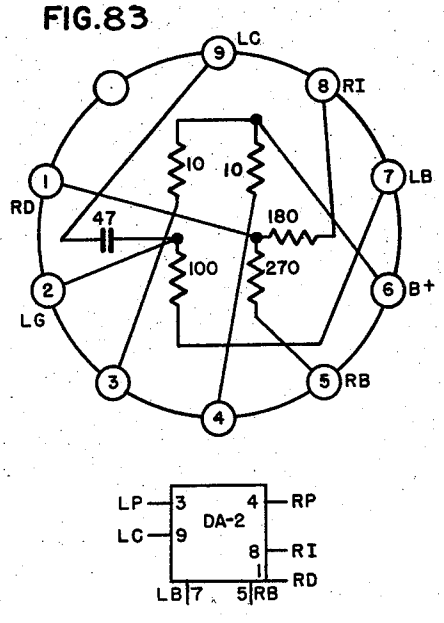


FIG. 83



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Filed Jan. 13, 1953 242 Sheets-Sheet 218

FIG. 84

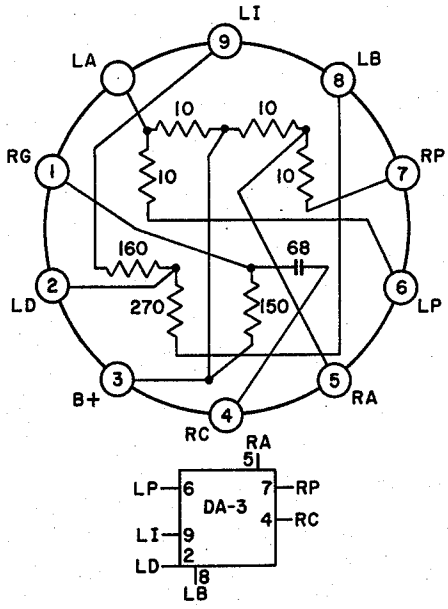


FIG. 85

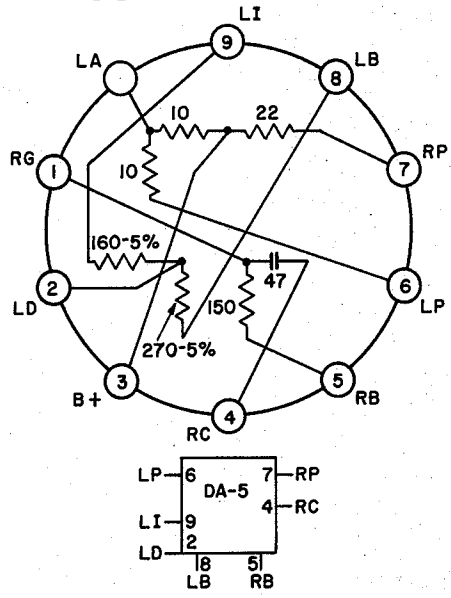


FIG. 86

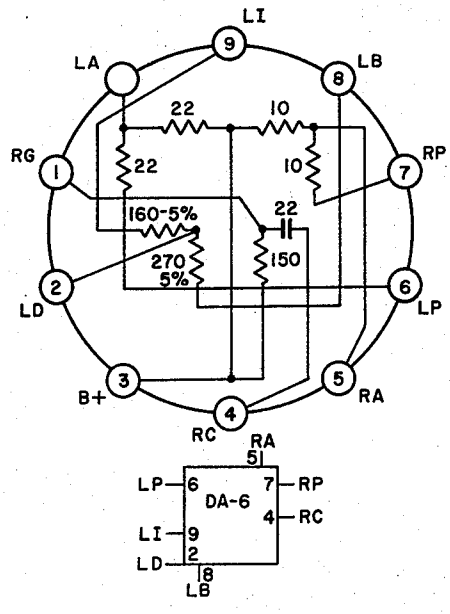
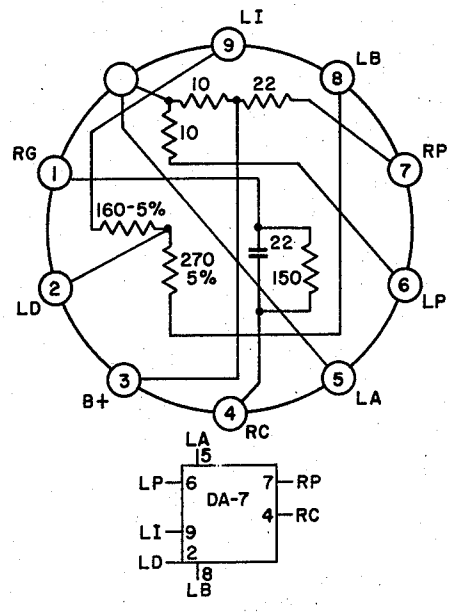


FIG. 87



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Filed Jan. 13, 1953 242 Sheets-Sheet 219

FIG. 88

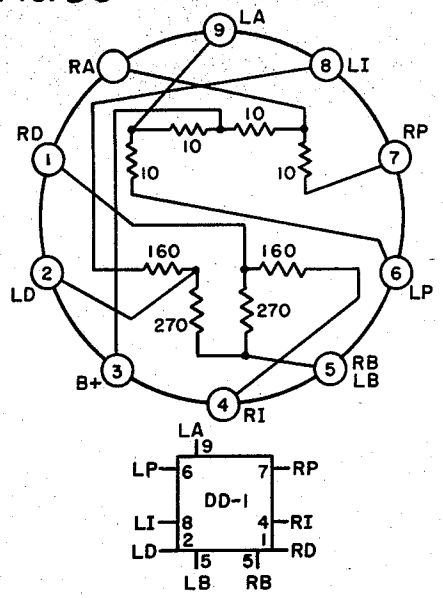


FIG. 89

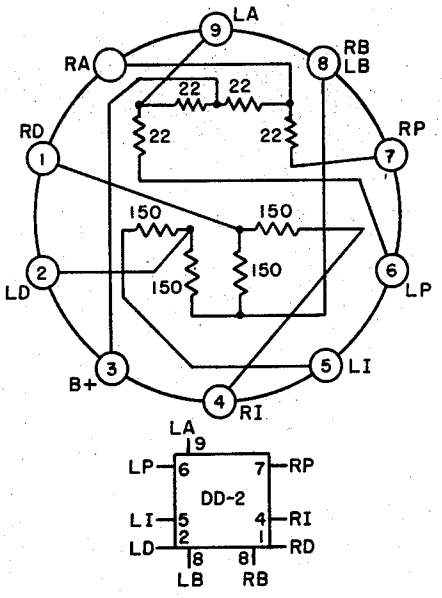


FIG. 90

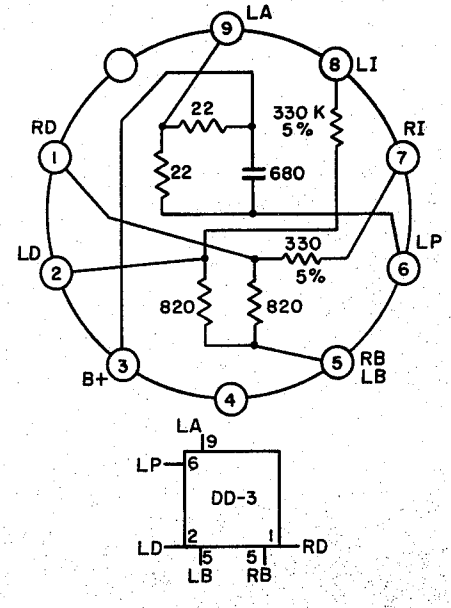
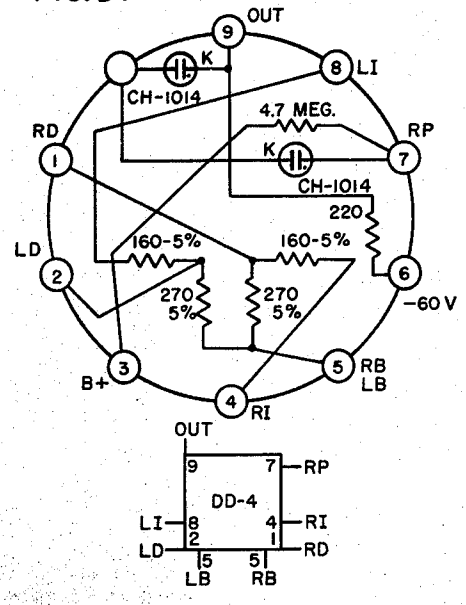


FIG. 91



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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 220

FIG. 92

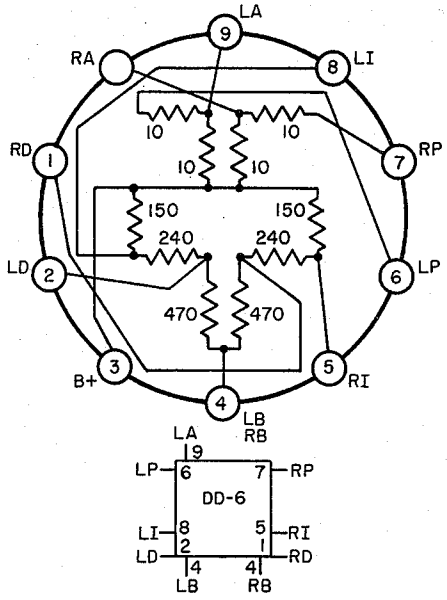


FIG. 93

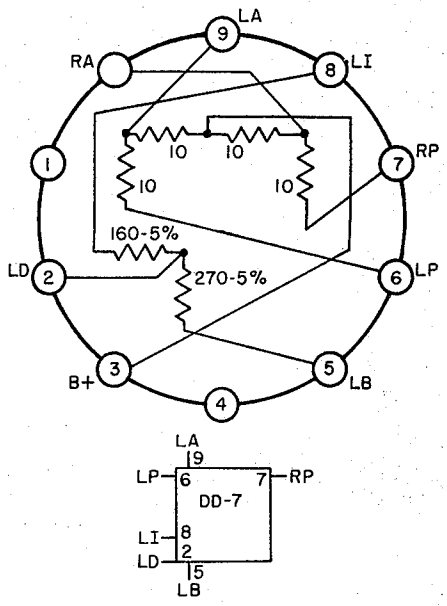


FIG. 94

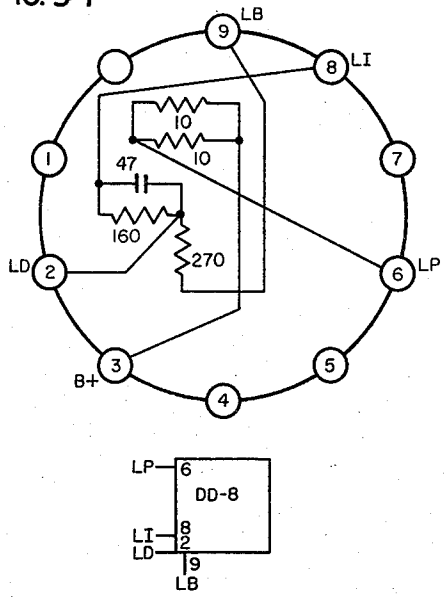
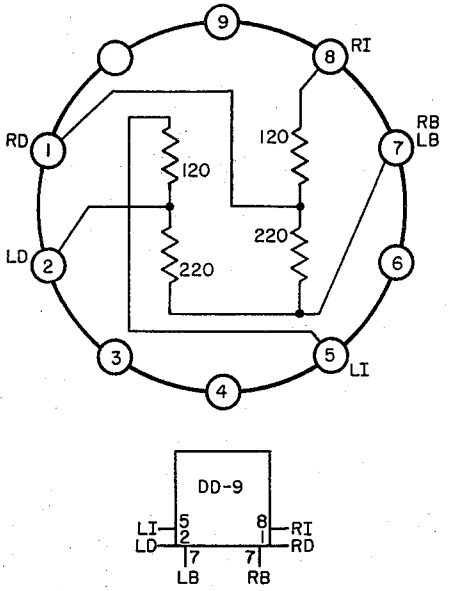


FIG. 95



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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 221

FIG. 96

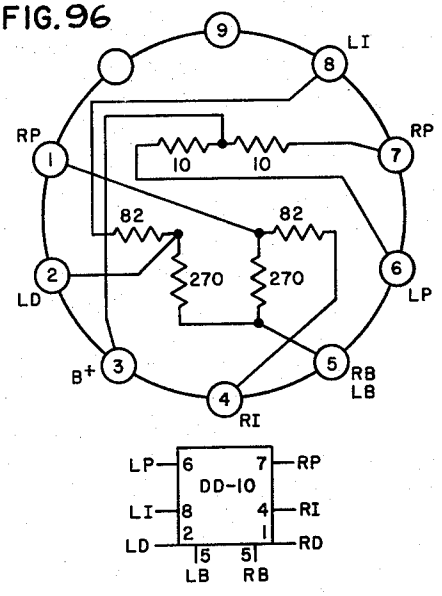


FIG. 97

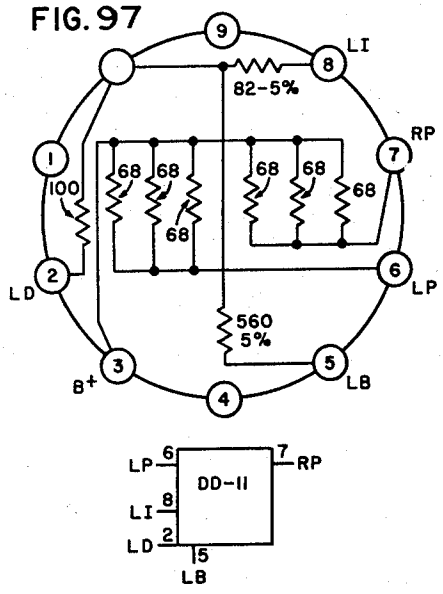


FIG. 98

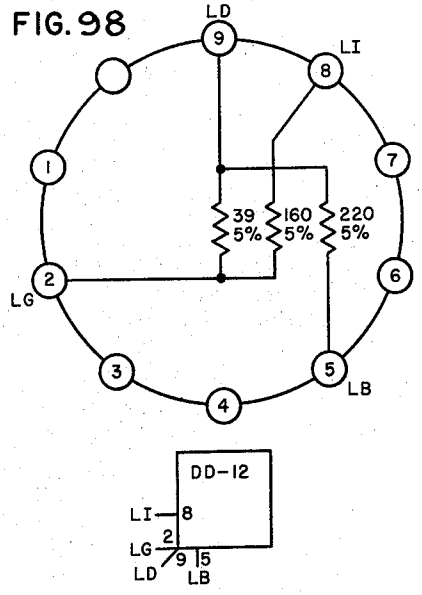
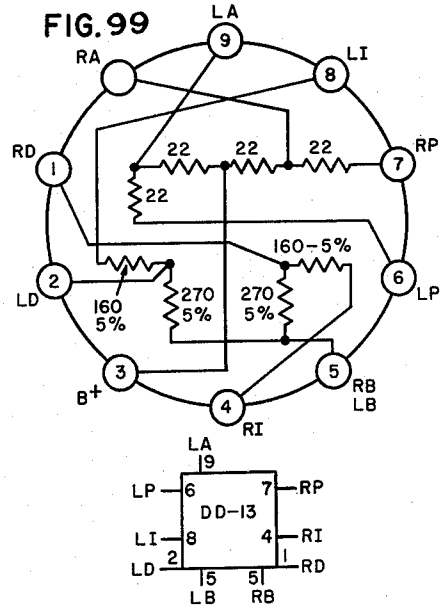


FIG. 99



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Filed Jan. 13, 1953 242 Sheets-Sheet 222

FIG. 100

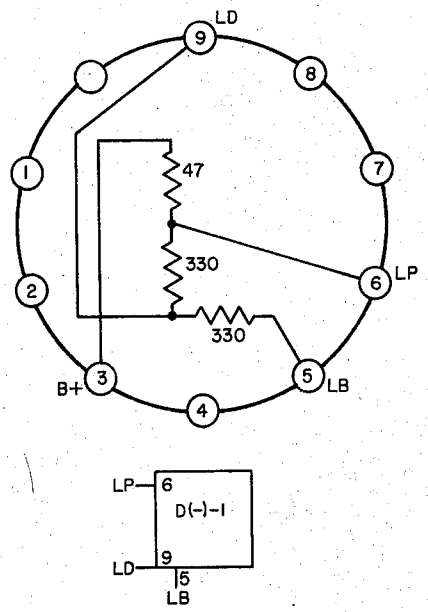


FIG. 101

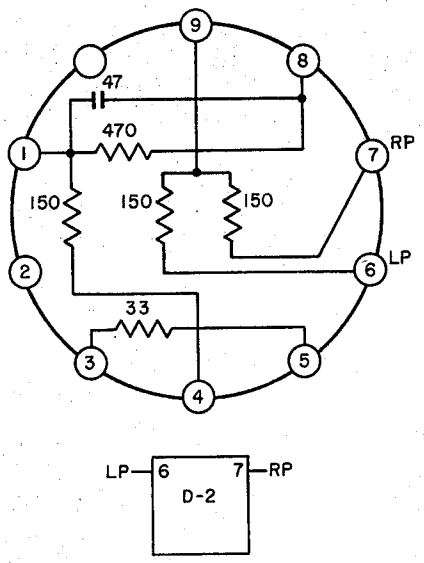


FIG. 102

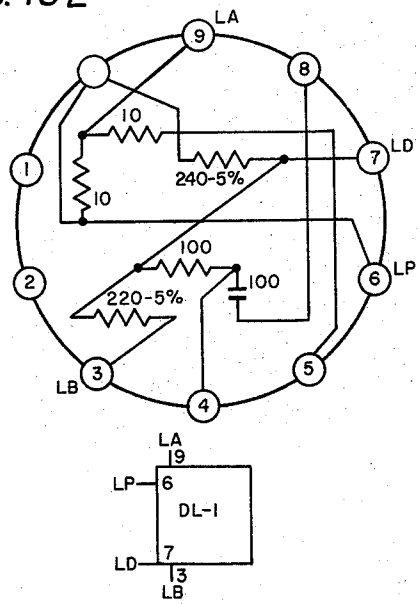
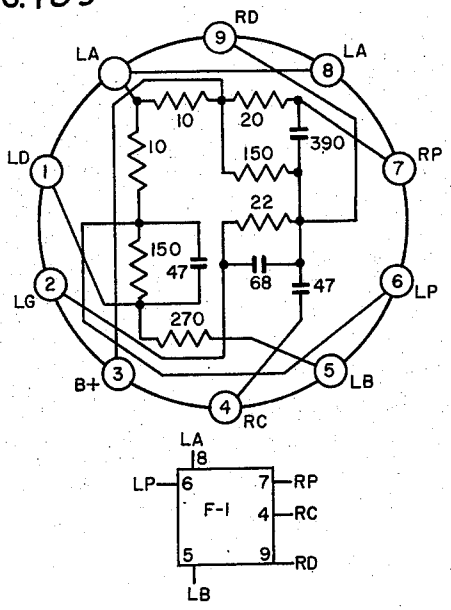


FIG. 103



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Filed Jan. 13, 1953 242 Sheets-Sheet 223

FIG. 104

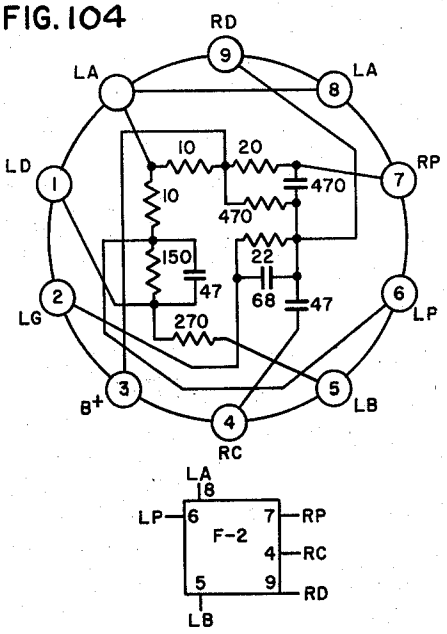


FIG. 105

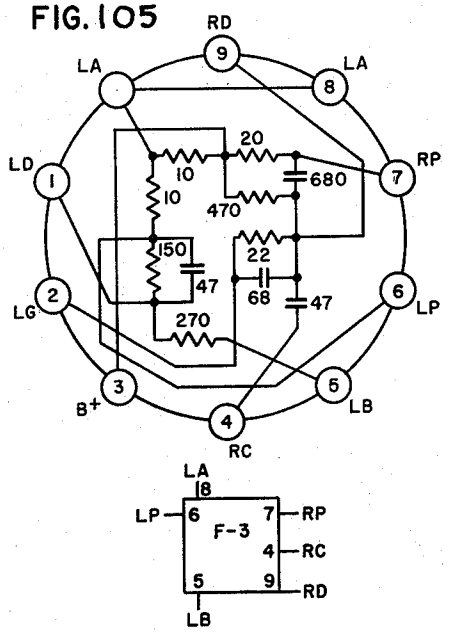


FIG. 106

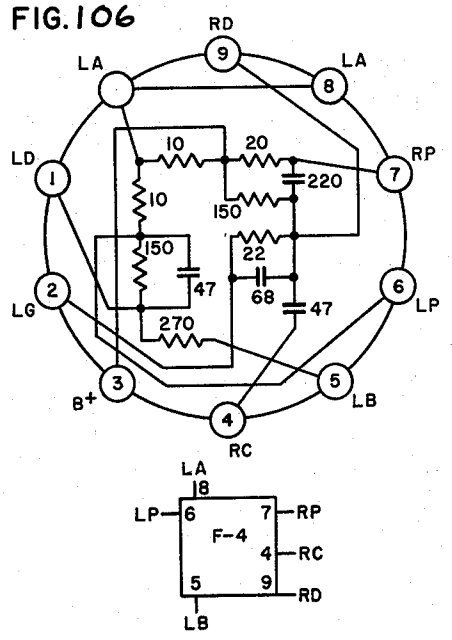
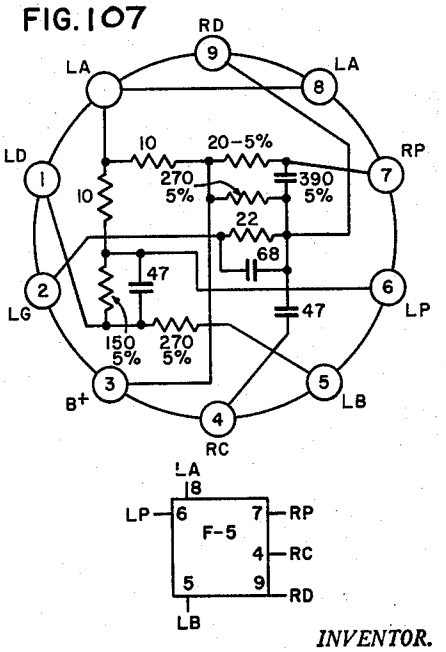


FIG. 107



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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 224

FIG. 108

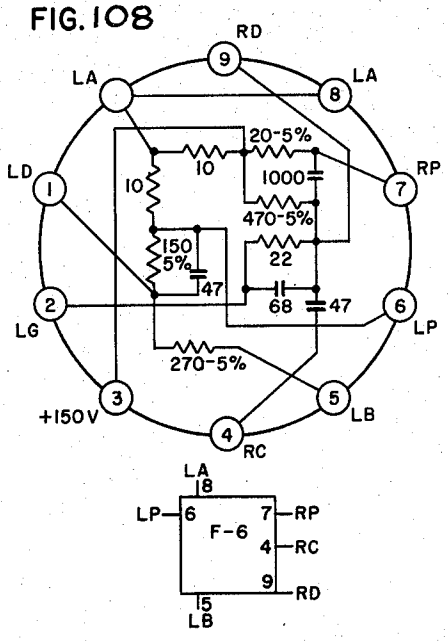


FIG. 109

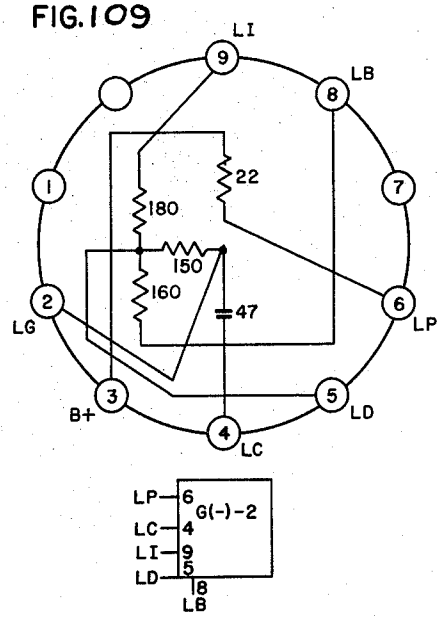


FIG. 110

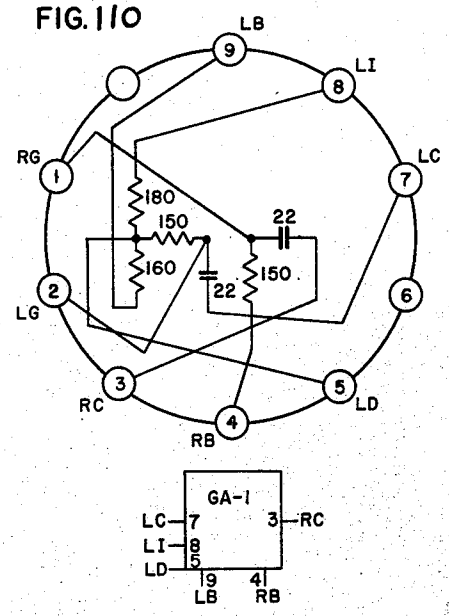
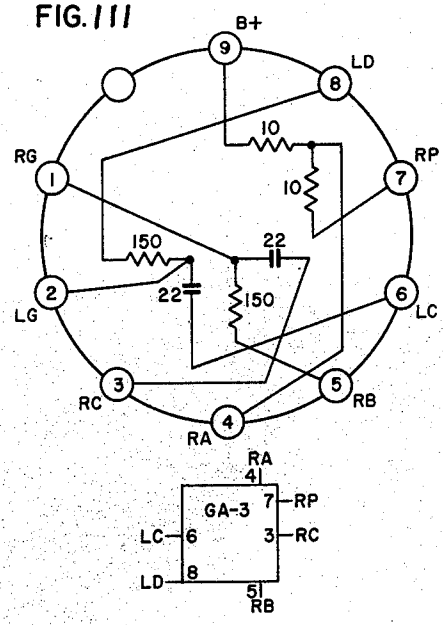


FIG. 111



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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 225

FIG.112

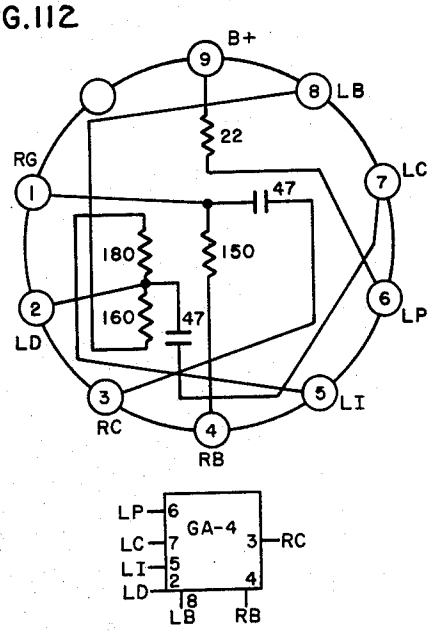


FIG.113

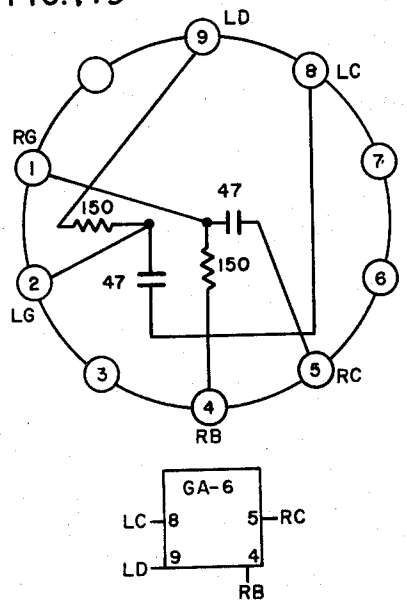


FIG.114

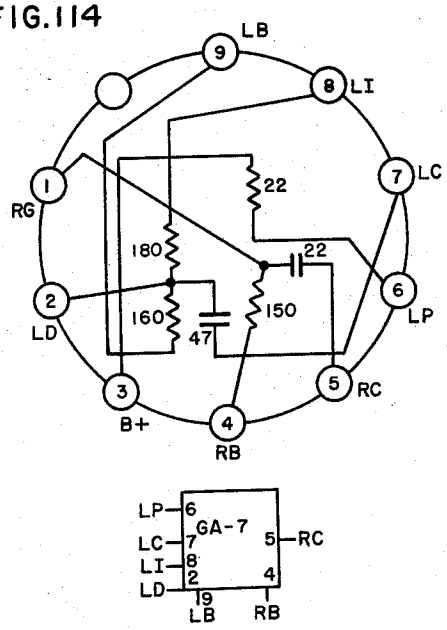
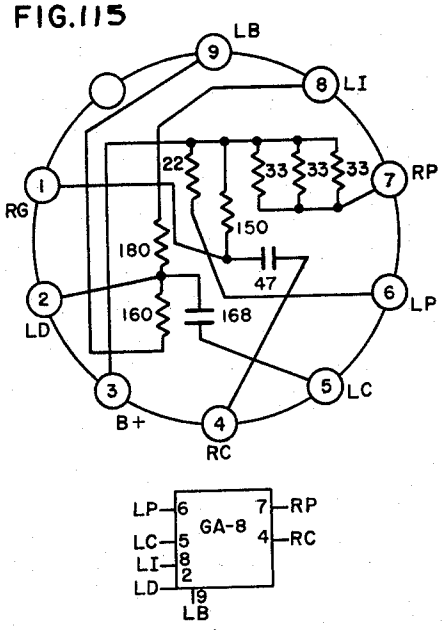


FIG.115



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Filed Jan. 13, 1953 242 Sheets-Sheet 226

FIG.116

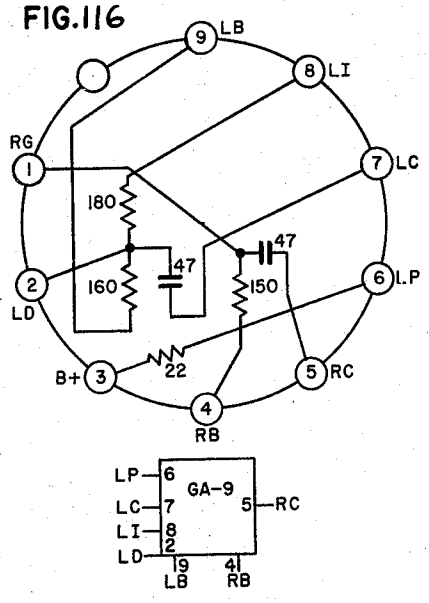


FIG.117

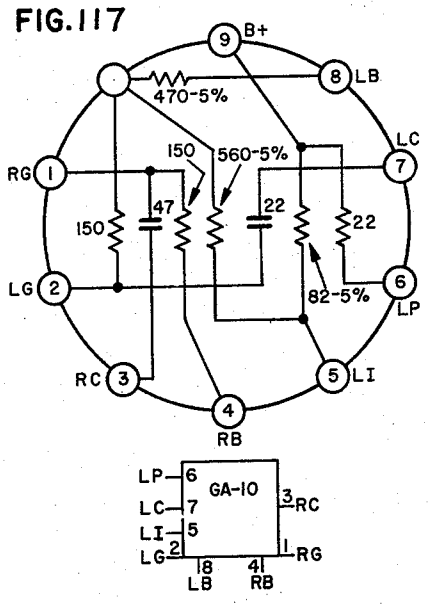


FIG.118

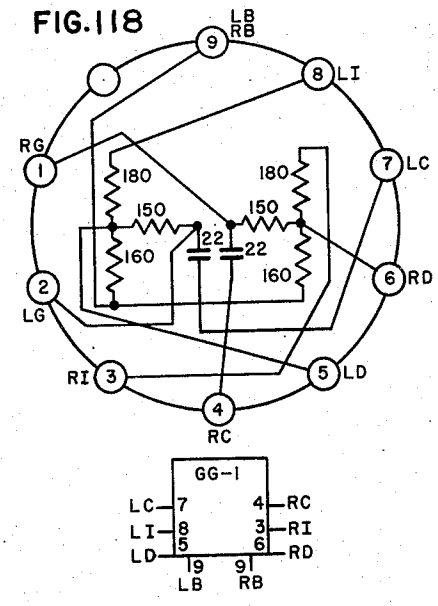
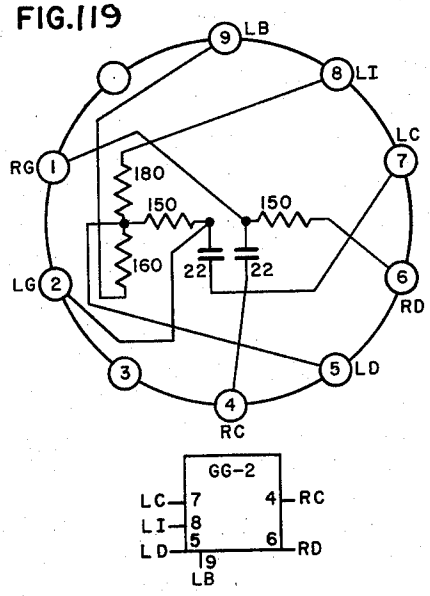


FIG.119



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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 227

FIG. 120

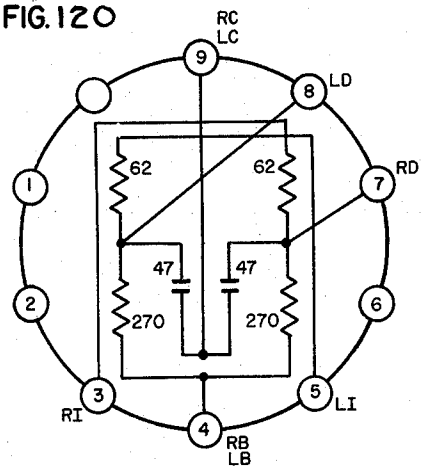


FIG. 121

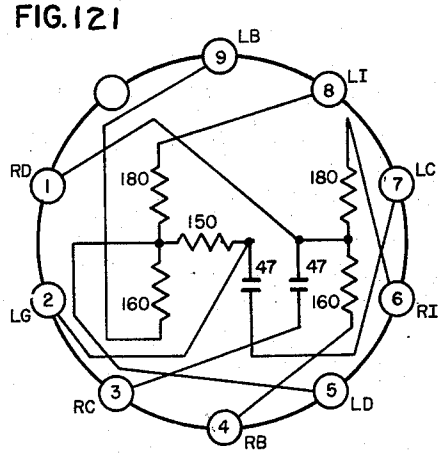


FIG. 122

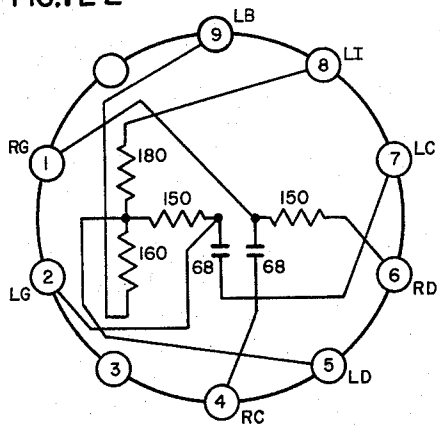
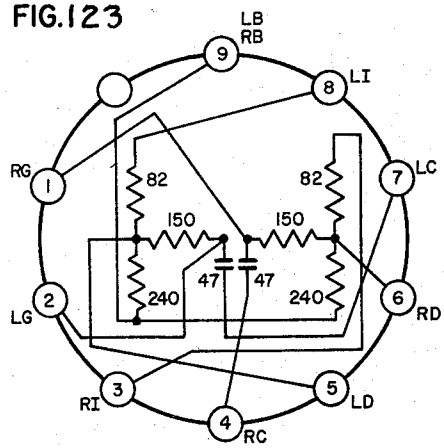


FIG. 123



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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 228

FIG. 124

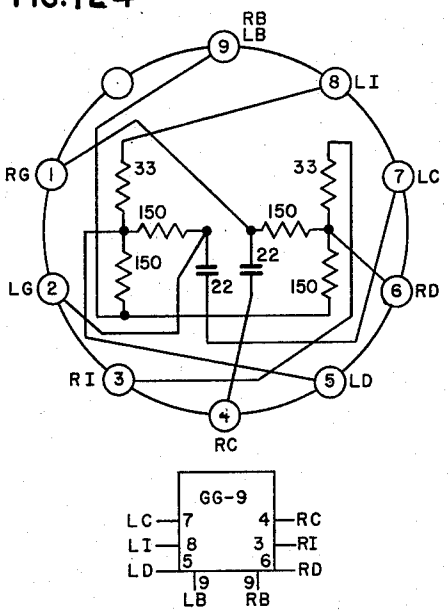


FIG. 125

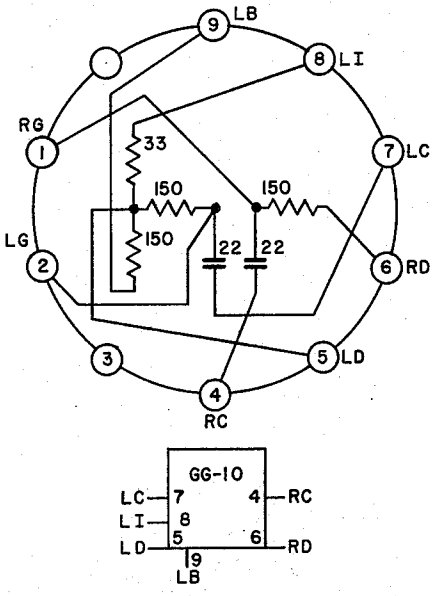


FIG. 126

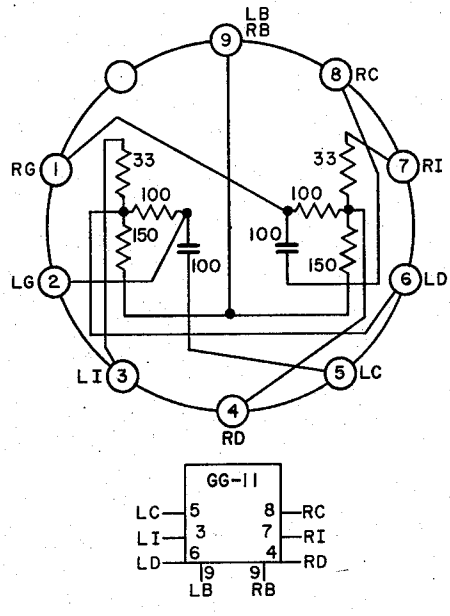
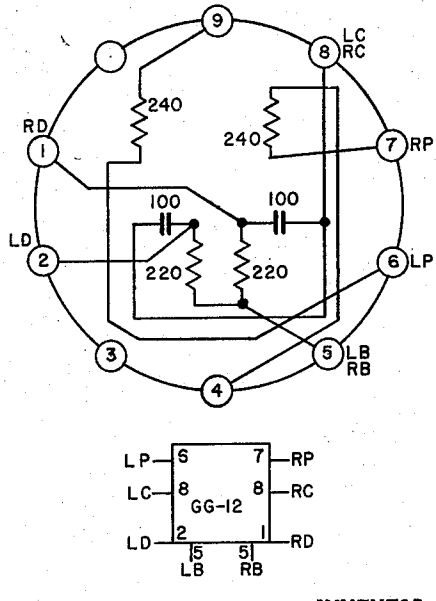


FIG. 127



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BY George V. Eltgroth

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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 229

FIG. 128

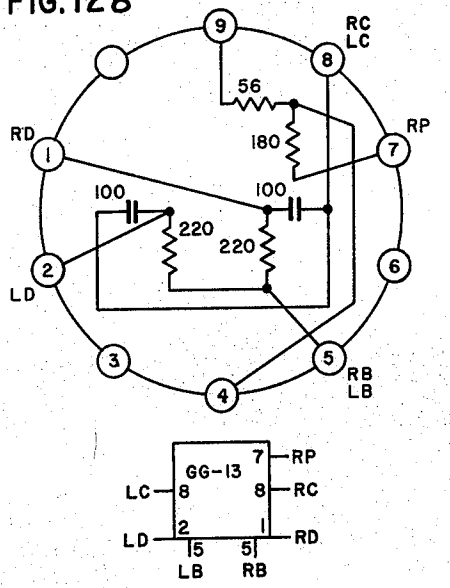


FIG. 129

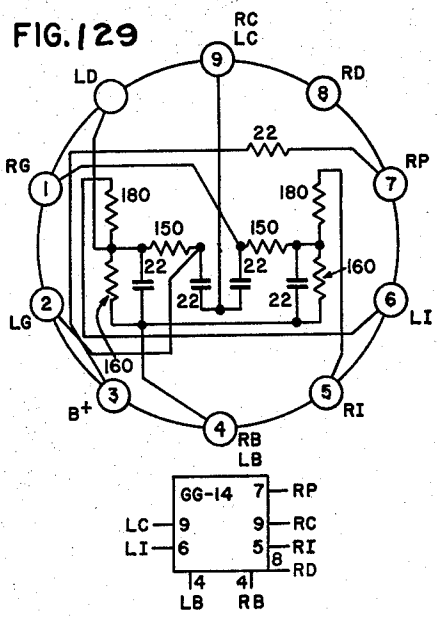


FIG. 130

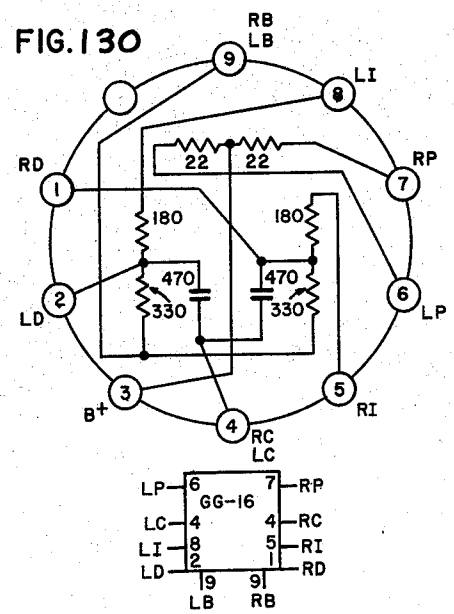
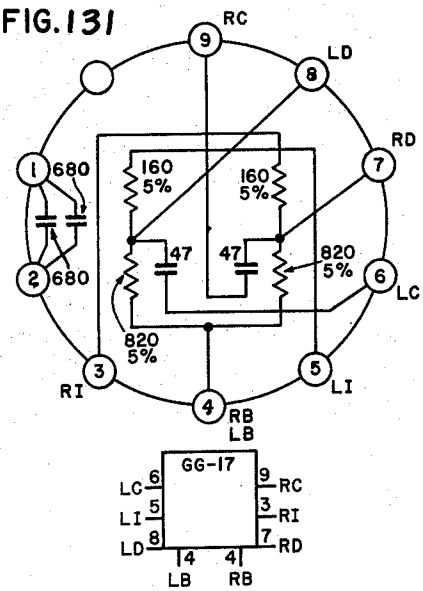


FIG. 131



INVENTOR.

LORING P. CROSMAN

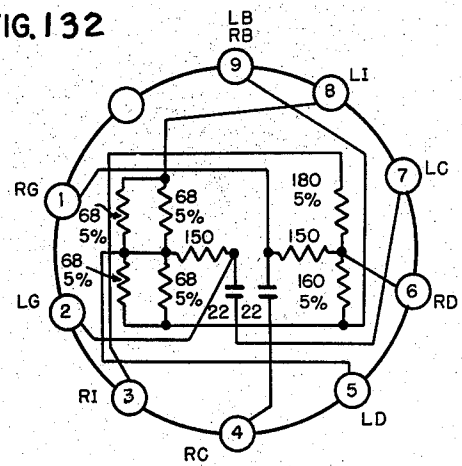
BY George V. Ectgroth

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ELECTRONIC DATA PROCESSING SYSTEM

Filed Jan. 13, 1953 242 Sheets-Sheet 230

FIG. 132



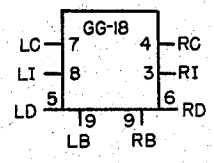
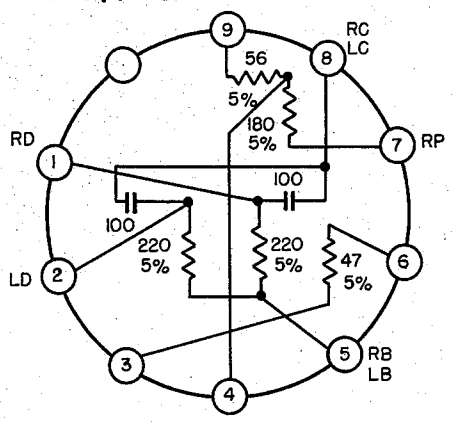


FIG. 133



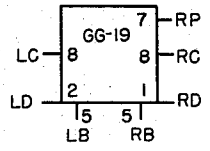
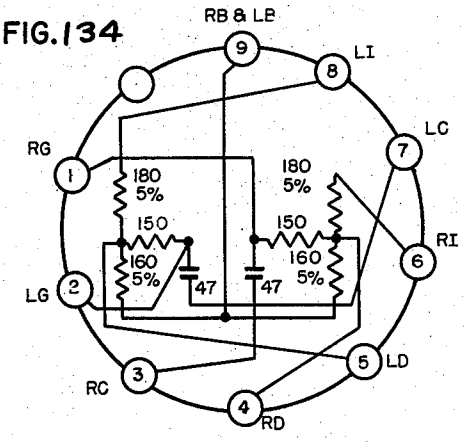


FIG. 134



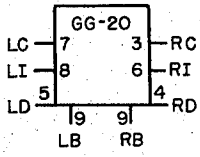
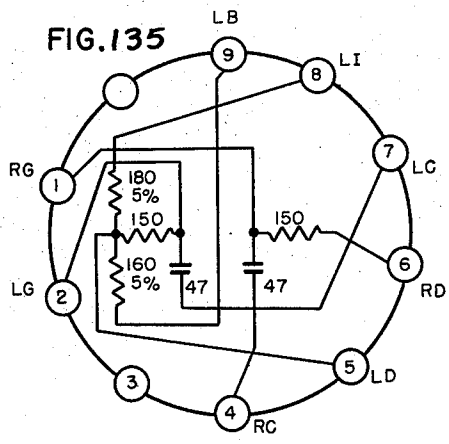
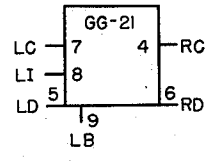


FIG. 135





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LORING P. CROSMAN

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Filed Jan. 13, 1953 242 Sheets-Sheet 231

FIG. 136

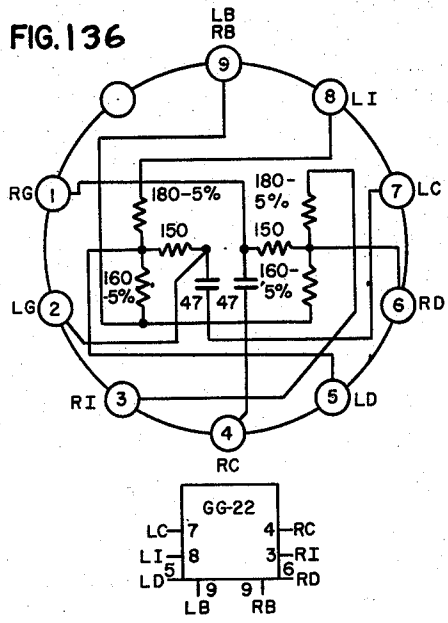


FIG. 137

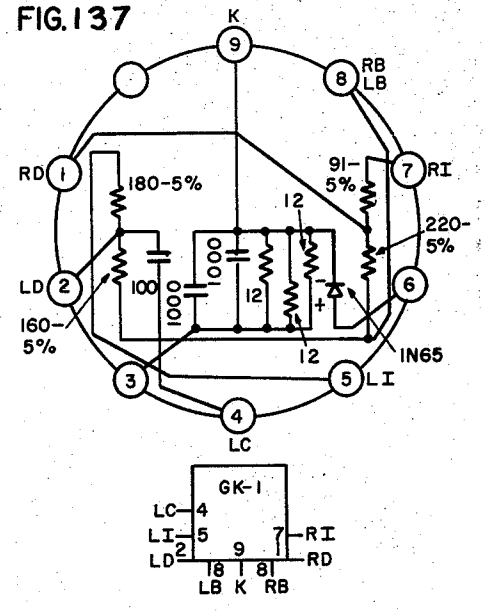


FIG. 138

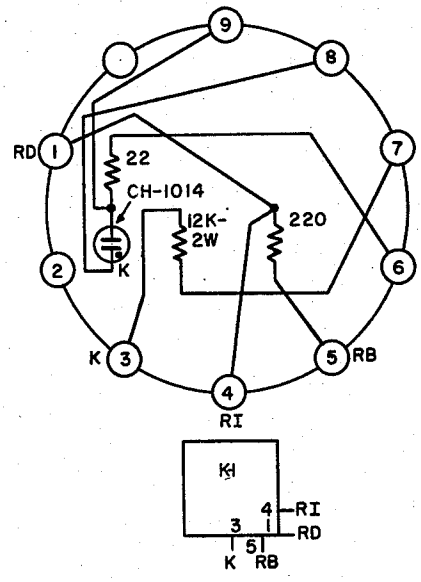
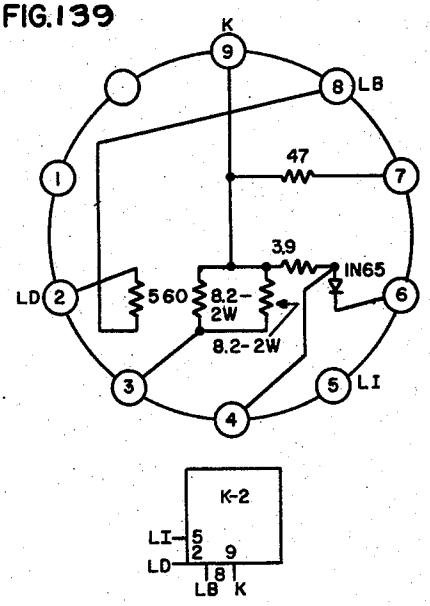


FIG. 139



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LORING P. CROSMAN

BY George V. Ectgroth

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Filed Jan. 13, 1953 242 Sheets-Sheet 232

FIG. 140

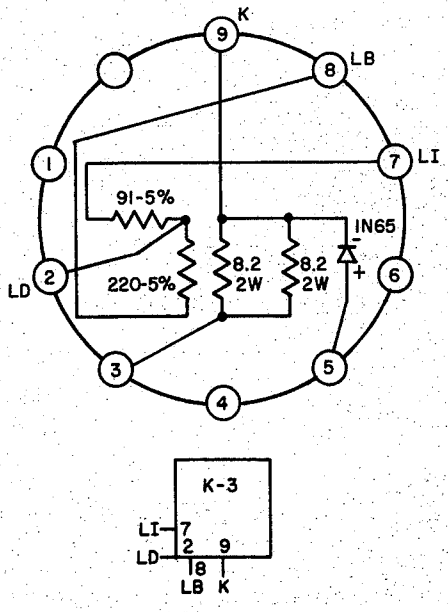


FIG. 141

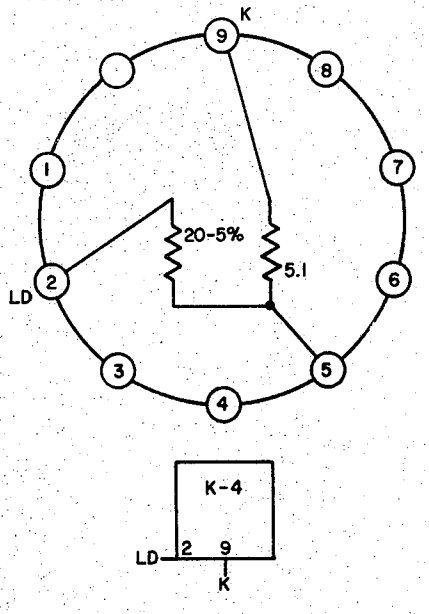


FIG. 142

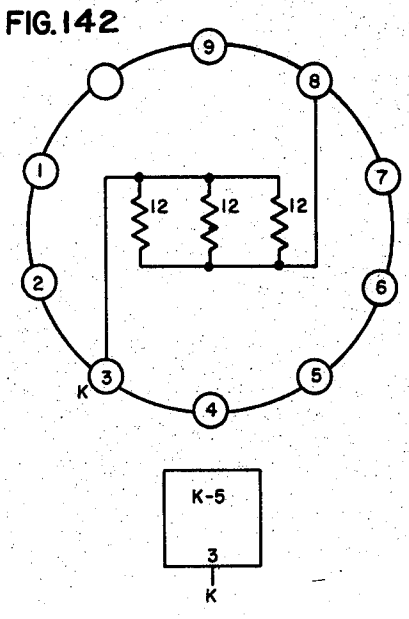
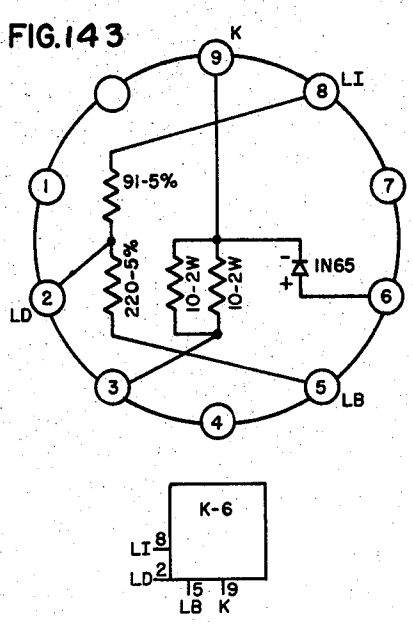


FIG. 143



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Filed Jan. 13, 1953 242 Sheets-Sheet 233

FIG. 144

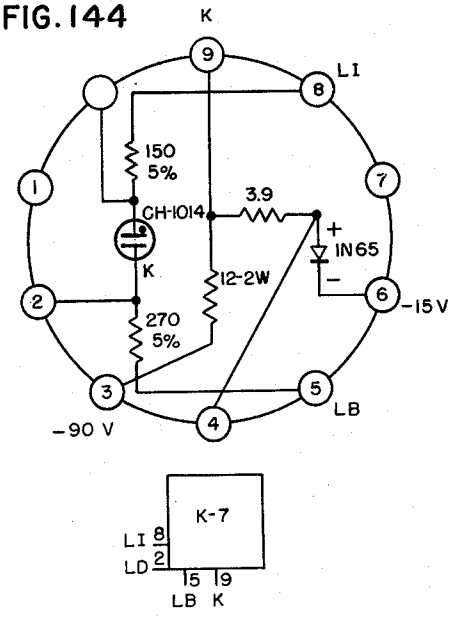


FIG. 145

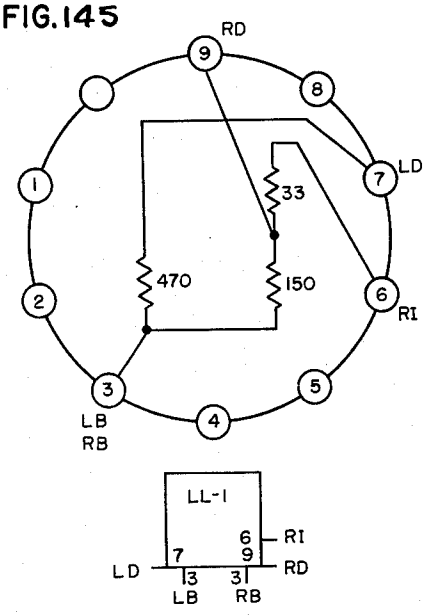


FIG. 146

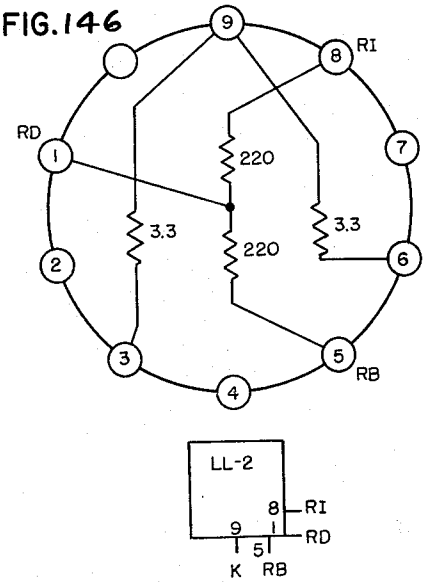
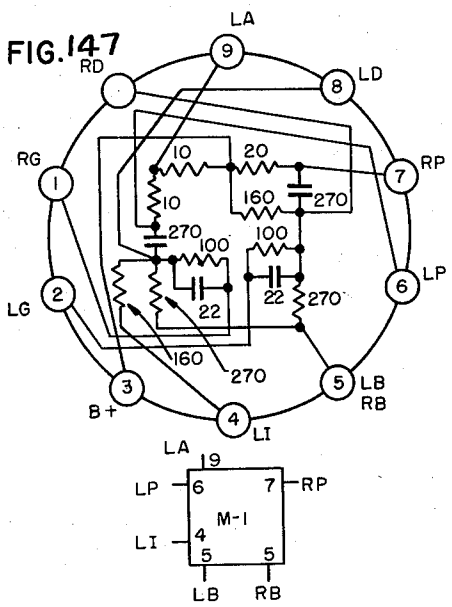


FIG. 147



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BY George V. Zetgrath

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Filed Jan. 13, 1953 242 Sheets-Sheet 234

FIG. 148

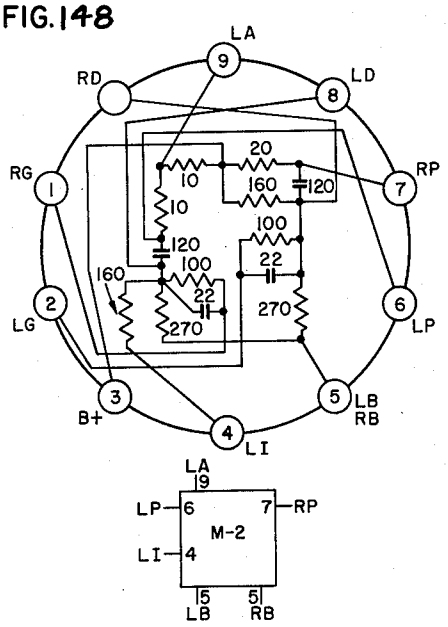


FIG. 149

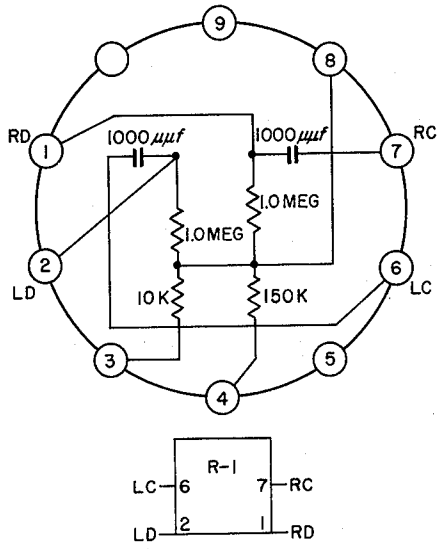


FIG. 150

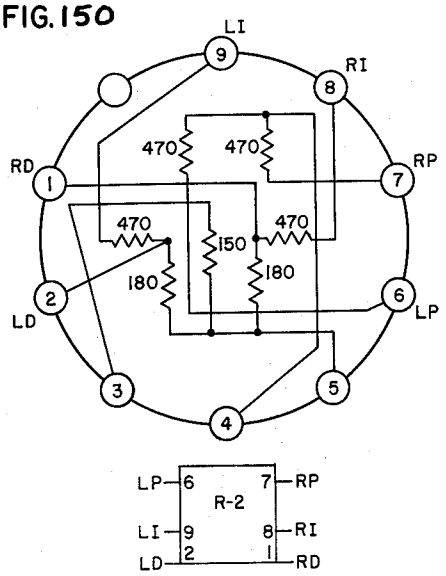
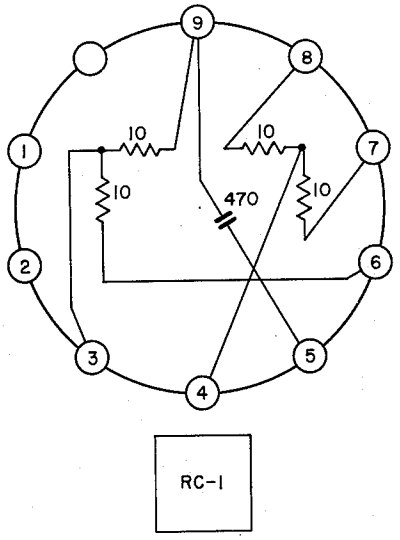


FIG. 151



INVENTOR.

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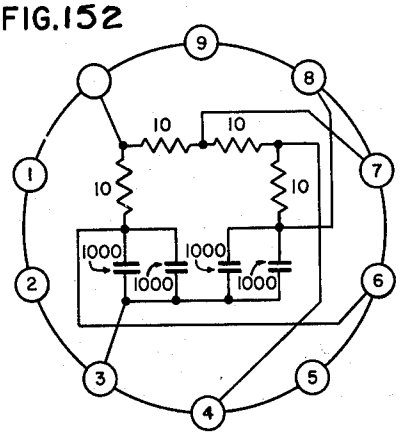
BY George V. Eltgroth

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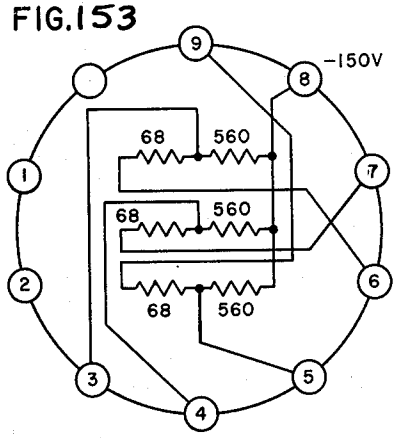
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FIG.152



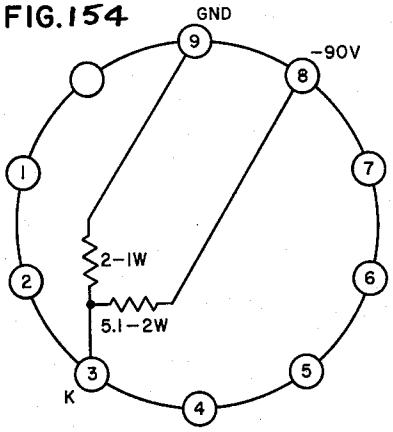
RC-2

FIG.153



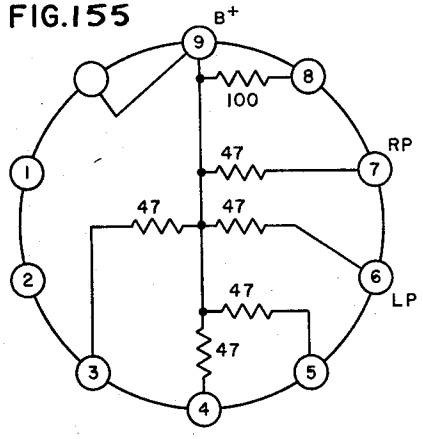
RC-3

FIG.154



RC-4

FIG.155



RC-5

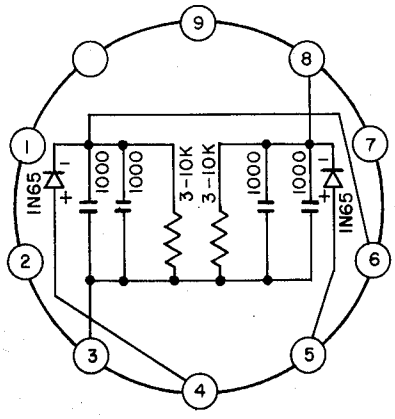
INVENTOR.

LORING P. CROSMAN

BY George V. Eltgroth

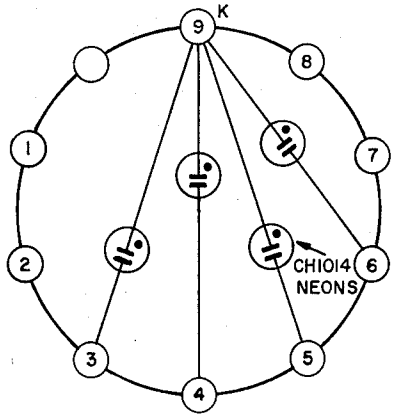
ATTORNEY

FIG. 156



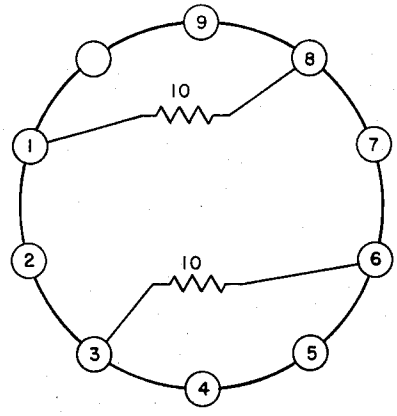
RC-6

FIG. 157



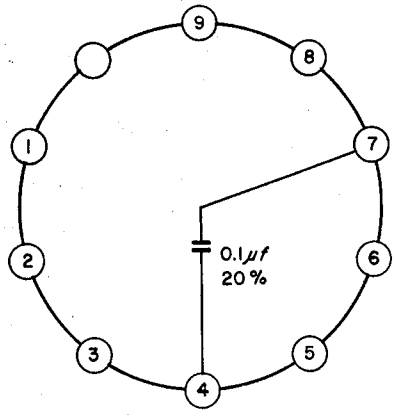
NEON
RC-7

FIG. 158



RC-8

FIG. 159



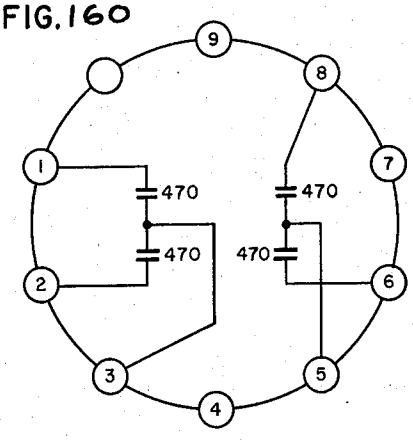
RC-9

INVENTOR.
LORING P. CROSMAN
BY George V. Ettgroth
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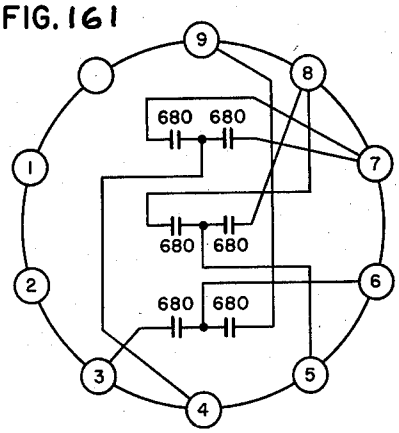
Filed Jan. 13, 1953 242 Sheets-Sheet 237

FIG. 160



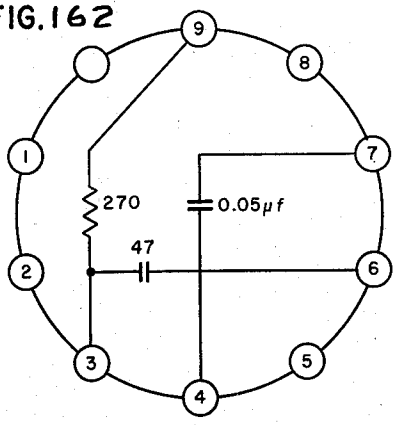
RC-10

FIG. 161



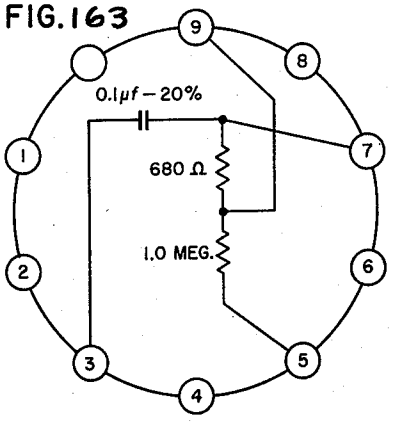
RC-11

FIG. 162



RC-13

FIG. 163



RC-14

INVENTOR.

LORING P. CROSMAN

BY George V. Zetgroth

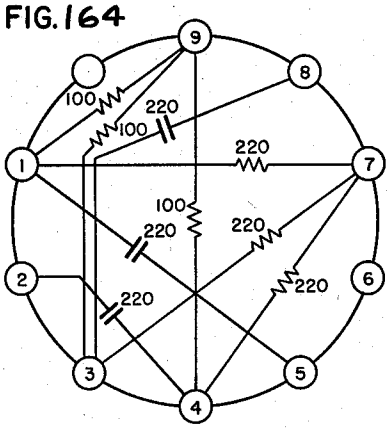
ATTORNEY

Oct. 4, 1960 L. P. CROSMAN 2,954,926

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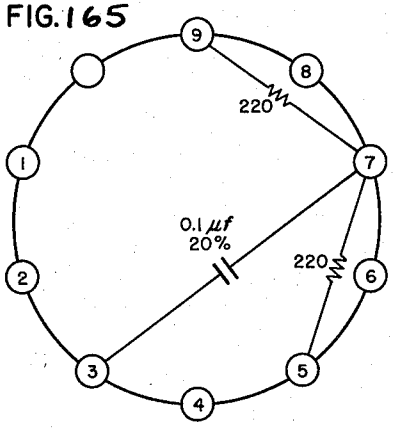
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FIG. 164



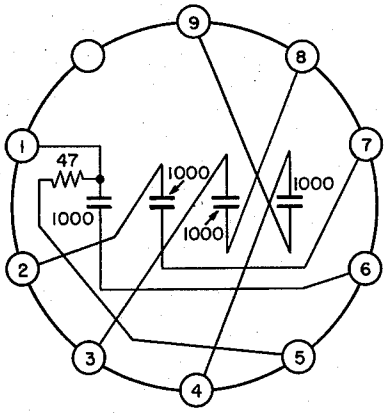
RC-15

FIG. 165



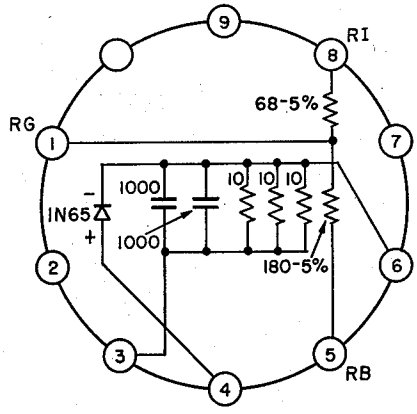
RC-16

FIG. 166



RC-17

FIG. 167



RC-18

INVENTOR.

LORING P. CROSMAN

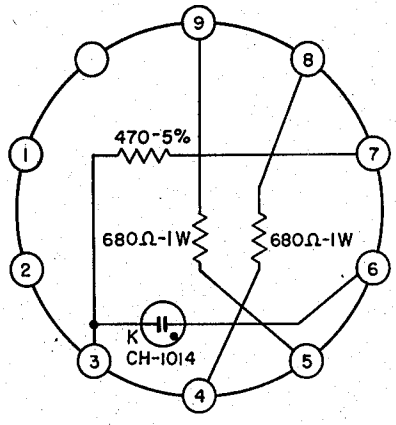
BY George V. Eltgroth

ATTORNEY

ELECTRONIC DATA PROCESSING SYSTEM

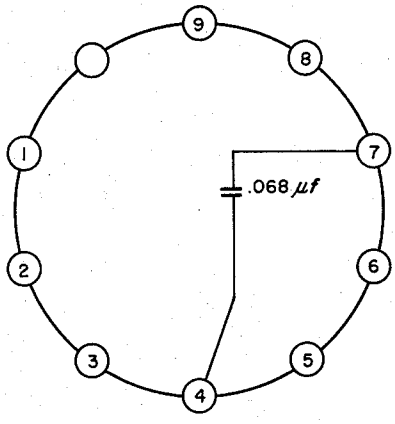
Filed Jan. 13, 1953 242 Sheets-Sheet 239

FIG. 168



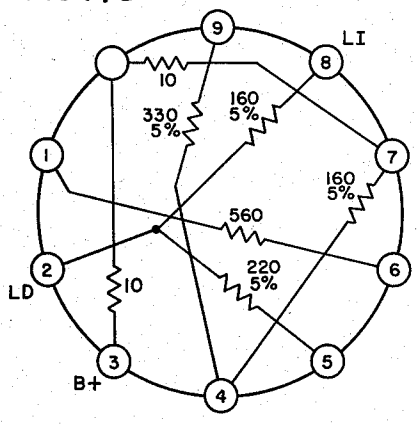
RC-20

FIG. 169



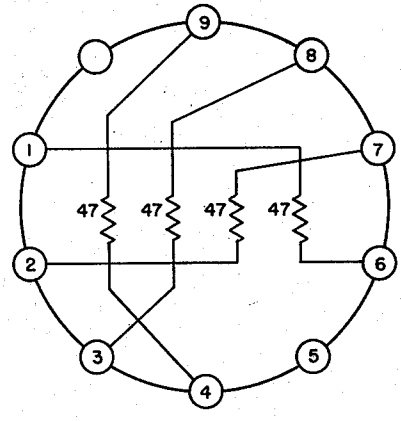
RC-21

FIG. 170



RC-22

FIG. 171



RC-23

INVENTOR.

LORING P. CROSMAN

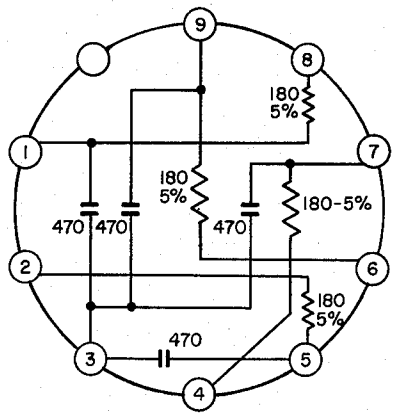
BY George V. Eltgroth

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ELECTRONIC DATA PROCESSING SYSTEM

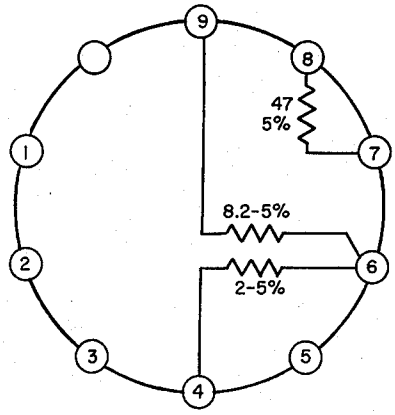
Filed Jan. 13, 1953 242 Sheets-Sheet 240

FIG. 172



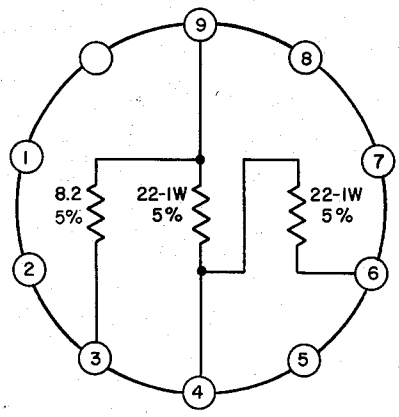
RC-24

FIG. 173



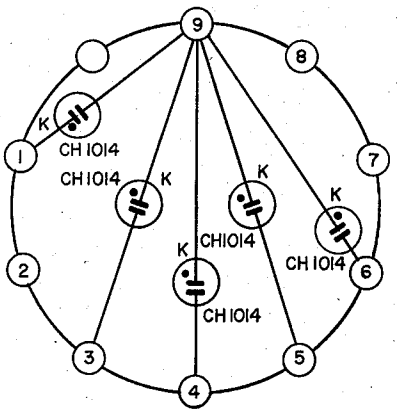
RC-25

FIG. 174



RC-26

FIG. 175



RC-27

INVENTOR.

LORING P. CROSMAN

BY George V. Ectgroth

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Filed Jan. 13, 1953 242 Sheets-Sheet 241

FIG.176

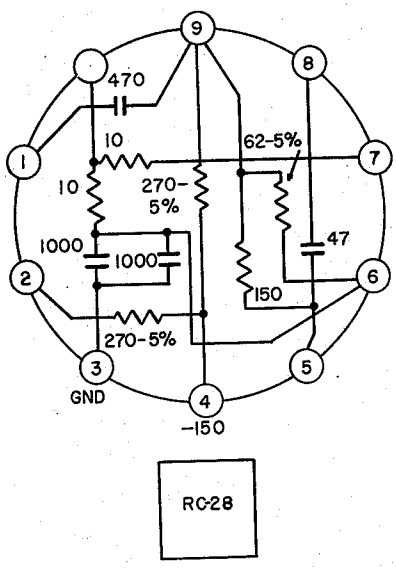


FIG.177

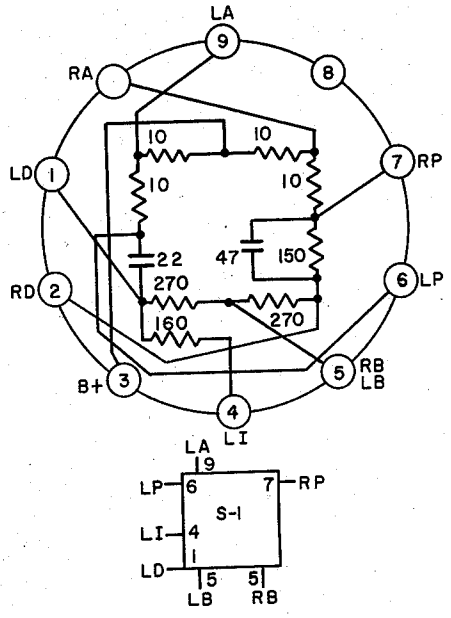


FIG.178

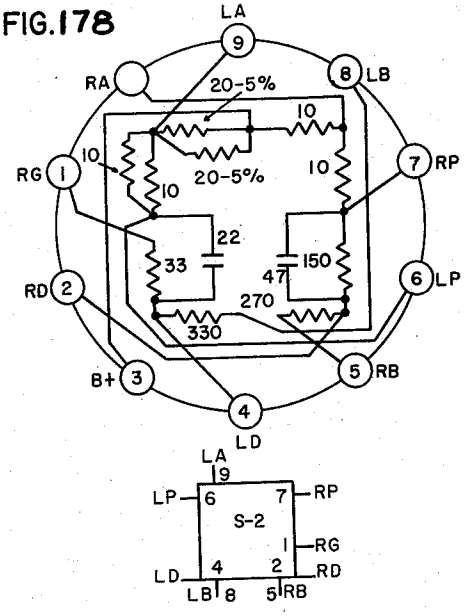
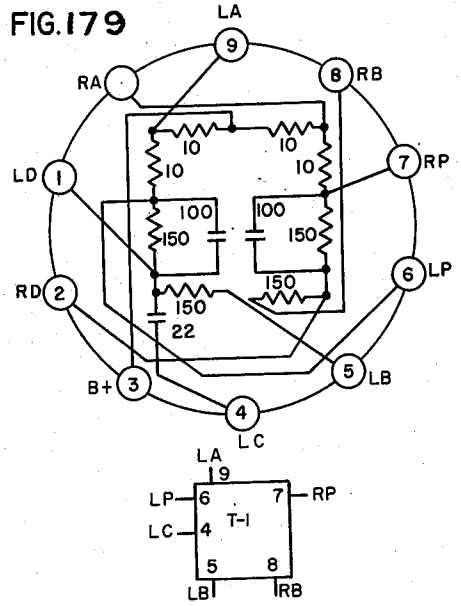


FIG.179



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Filed Jan. 13, 1953 242 Sheets-Sheet 242

FIG. 180

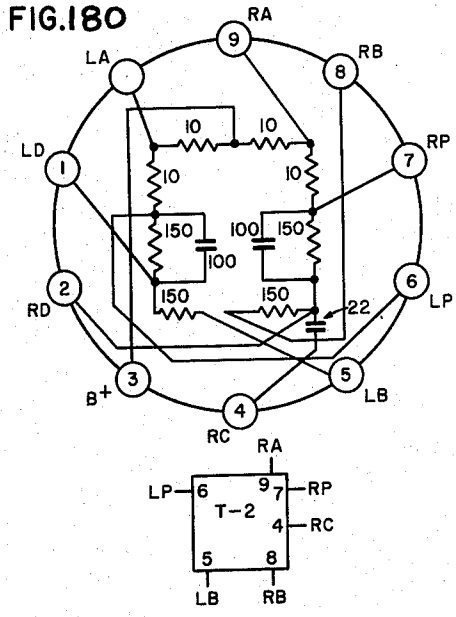


FIG. 181

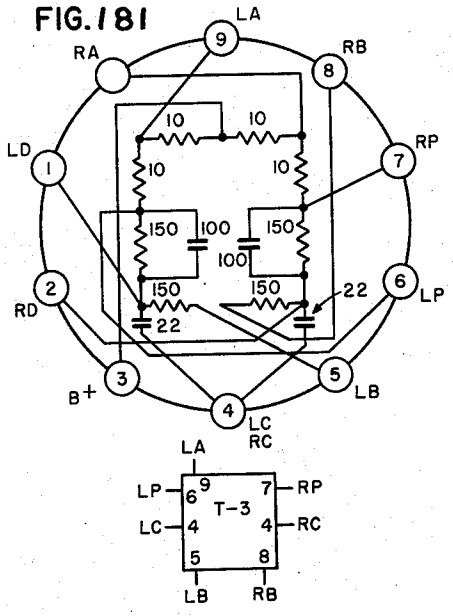


FIG. 182

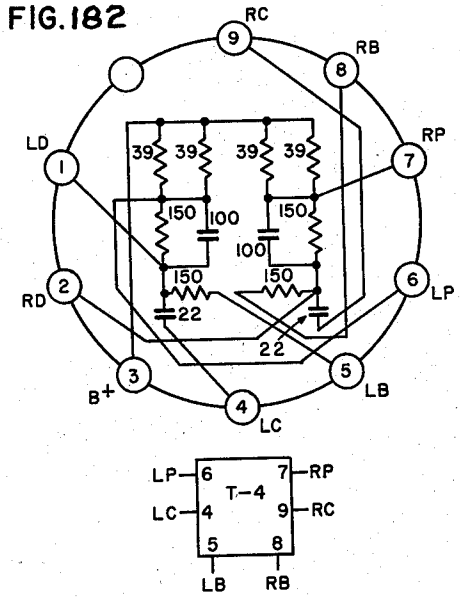
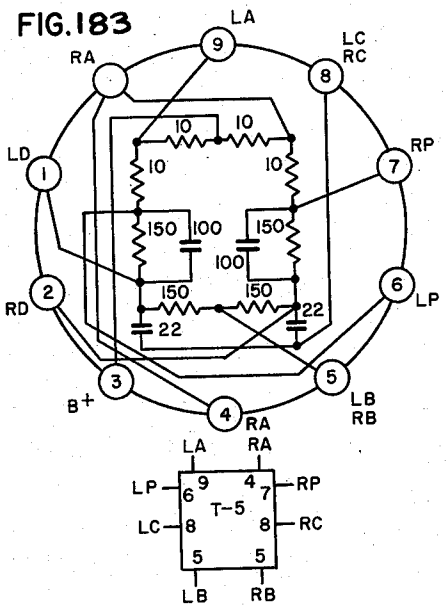


FIG. 183



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2,954,926

ELECTRONIC DATA PROCESSING SYSTEM

Loring P. Crosman, Wilton, Conn., assignor to Sperry Rand Corporation, a corporation of Delaware

Filed Jan. 13, 1953, Ser. No. 330,961

18 Claims. (Cl. 235—159)

The present invention relates to information processing apparatus and more specifically to an electronic calculator for performing various computational steps rapidly and in accordance with predetermined programs.

While the electronic computing art is relatively new, a number of electronic data processing systems have been designed and constructed during the past decade. Operational experience with these machines has established their great utility but has also disclosed a number of difficulties. Reliability has in many instances been lower than is necessary for commercial applications, and ease of programming and set-up has generally been sacrificed to achieve a high degree of flexibility.

It is a primary object of the present invention therefore, to provide an improved electronic data processing system that is highly flexible and versatile and is yet easy to program and set-up for various calculating operations.

Other objects of the invention are:

To provide an electronic calculator that will perform result checking operations as an integral part of each step without complicated programming on the part of an operator.

To provide a highly reliable electronic calculator which checks the result of each arithmetic calculation by performing a complementary operation using the result and both of the original factors.

To provide an electronic calculator having a novel means for maintaining decimal point control during calculating operations.

To provide an electronic calculating system wherein the location of decimal points within data storage locations can be established by simple switching operations.

To provide an electronic calculating system wherein any computational or output control step may be caused to follow any other computational or output control step by means of simple switching or plugging.

To provide an electronic calculating system with novel means for halting calculation at predetermined points.

To provide an electronic calculating system in which the data transfer rate to and from an input-output unit is variable and is controlled by the calculator.

To provide an electronic calculator wherein the isolating diodes comprising signal buffers have properties of amplitude discrimination.

Other objects of the invention will be apparent from the following description and from the drawings.

In the preferred embodiment disclosed herein, input data are received from punched cards and output data are recorded in punched cards. The invention is equally applicable, however, to computing systems using other forms of input and output such as, for example, magnetic or electrostatic storage.

Attention is directed to a number of patents and copending applications of Loring P. Crosman that disclose and claim certain improved equipment components employed in the present invention.

Patent No. 2,512,851 claims a novel pulse generator.

Patent No. 2,585,630 claims a novel digit shifting circuit.

Patent No. 2,563,102 claims an improved digit indicator.

Patent No. 2,579,174 claims a novel electronic accumulator.

Application, Serial No. 83,378, now Patent No. 2,706,597, claims an improved carry impulse generator.

Application, Serial No. 112,621, now Patent No. 2,676,249, claims a novel discharge tube isolation circuit.

Application, Serial No. 116,991, now Patent No. 2,750,114, claims a novel reversible accumulator.

Application, Serial No. 154,407, now Patent No. 2,700,503, claims an apparatus for multiplying.

Application, Serial No. 180,389, now Patent No. 2,693,593, claims a novel decoding circuit.

Application, Serial No. 233,002, now Patent No. 2,780,408, claims an improved electronic accumulator.

Application, Serial No. 248,013, now abandoned, claims an improved circuit for dividing.

In the drawings:

Fig. 1 is a block diagram of the system showing the various units comprising the calculator.

Fig. 2 shows the various chassis comprising what is referred to as the front of the calculator.

Fig. 3 shows the various chassis comprising what is referred to as the back of the calculator.

Fig. 4 is an aid in explaining the block schematic representation used in some of the following figures.

Fig. 5 is a schematic diagram of a typical D.C. amplifier used in the calculator.

Fig. 6 is a schematic diagram of a typical positive pulse amplifier used in the calculator.

Fig. 7 is a schematic diagram of a typical negative pulse amplifier used in the calculator.

Fig. 8 is a schematic diagram of a typical cathode follower used in the calculator.

Fig. 9 is a schematic diagram of a typical gate used in the calculator.

Fig. 10 is a schematic diagram of a typical Schmitt trigger used in the calculator.

Fig. 11 is a schematic diagram of a typical conventional trigger used in the calculator.

Fig. 12 is a schematic diagram of a typical flip-flop used in the calculator.

Fig. 13 is a schematic diagram of a typical flip-flop clamper used in the calculator.

Fig. 14 is a schematic diagram of a typical cathode clamper used in the calculator.

Fig. 15 is a schematic diagram of a typical step trigger and gate used in the calculator.

Figs. 16*a* to 16*f*, taken together in the manner of Fig. 16*g*, show schematically a typical Accumulator (ACC) chassis.

Figs. 17*a* to 17*d*, taken together in the manner of Fig. 17*e*, show schematically the Base Control (BCL) chassis.

Figs. 18*a* to 18*f*, taken together in the manner of Fig. 18*g*, are a block schematic of the Control (CTL) chassis.

Figs. 19*a* to 19*f*, taken together in the manner of Fig. 19*g*, are a block schematic of the Decimal Control (DCL) chassis.

Figs. 20*a* to 20*f*, taken together in the manner of Fig. 20*g*, are a block schematic of the Decimal Counter (DCR) chassis.

Figs. 21*a* to 21*d*, taken together in the manner of Fig. 21*e*, show schematically a typical Input-Output (I-O) chassis.

Figs. 22*a* to 22*d*, taken together in the manner of Fig. 22*e*, show schematically a typical Keyboard Bias (KB) chassis.

Figs. 23*a* to 23*f*, taken together in the manner of Fig. 23*g*, are a block schematic of the Multiplication-Division (MD) chassis.

Figs. 24*a* to 24*d*, taken together in the manner of Fig. 24*e*, are a block schematic of the Output Control (OCL) chassis.

Figs. 25*a* to 25*f*, taken together in the manner of Fig. 25*g*, are a block schematic of the Zero Factor (ϕF) chassis.

Fig. 26 is a block schematic of the Regulator (REG) chassis.

Figs. 27*a* to 27*c*, taken together in the manner of Fig. 27*d*, are a block schematic of the Registration Impulse Generator (RIG) chassis.

Fig. 27*e* shows the arrangement of Figs. 27*a* through 27*d*.

Figs. 28*a* to 28*c* taken together in the manner of Fig. 28*d*, are a block schematic of the Sign Bias (SB) chassis.

Figs. 29*a* to 29*d*, taken together in the manner of Fig. 29*e*, are a block schematic of the Step Control (SCL) chassis.

Figs. 30*a* to 30*f*, taken together in the manner of Fig. 30*g*, show schematically a typical Step Sequence (SS) chassis.

Figs. 31*a* and 31*b*, taken together in the manner of Fig. 31*c*, show schematically a typical Storage (ST) chassis.

Figs. 32*a* to 32*d*, taken together in the manner of Fig. 32*e*, are a block schematic of a typical Storage Set (STS) chassis.

Figs. 33*a* to 33*c*, taken together in the manner of Fig. 33*d*, are a block schematic of the Storage Zeroize (STZ) chassis.

Figs. 34*a* to 34*d*, taken together in the manner of Fig. 34*e*, are a block schematic of the Test Counter (TCR) chassis.

Figs. 35*a* to 35*p*, taken together in the manner of Fig. 35*q*, show the chassis units comprising the front of the accumulator and some of the interconnections between these chassis.

Figs. 36*a* to 36*l*, taken together in the manner of Fig. 36*m*, show other interconnections between the chassis units comprising the front of the accumulator.

Figs. 37*a* to 37*l*, taken together in the manner of Fig. 37*m*, show the chassis units comprising the back of the accumulator and some of the interconnections between these chassis.

Figs. 38*a* to 38*o*, taken together in the manner of Fig. 38*p*, show other interconnections between the chassis units comprising the back of the accumulator.

Figs. 39*a* to 39*l*, taken together in the manner of Fig. 39*m*, show still other interconnections between the chassis units comprising the back of the accumulator.

Figs. 40*a* to 40*l*, taken together in the manner of Fig. 40*m*, show some of the interconnections between the chassis units comprising the front and back of the accumulator.

Figs. 41*a* to 41*d*, taken together in the manner of Fig. 41*e*, are an aid to explaining the branching operation.

Figs. 42*a* and 42*b*, taken together in the manner of Fig. 42*c*, show the physical arrangement of the plugboard.

Figs. 43*a* and 43*b*, taken together in the manner of Fig. 43*c*, show some of the connections between the plugboard and the Keyboard Bias (KB) chassis.

Figs. 44*a* to 44*e*, taken together in the manner of Fig. 44*f*, show certain other connections between chassis units and the plugboard.

Figs. 45*a* and 45*b*, taken together in the manner of Fig. 45*c*, show the physical layout of the neon mixer board.

Figs. 46*a* to 46*f*, taken together in the manner of Fig. 46*g*, show certain interconnections between the constant switches and the neon mixer board.

Figs. 47*a* to 47*f*, taken together in the manner of Fig. 47*g*, show the test panel.

Figs. 48*a* to 48*d*, taken together in the manner of Fig. 48*e*, show schematically the punch control circuits.

Fig. 49 shows a typical set of sensing and punching connections.

Fig. 50 shows the minus neons associated with storage locations.

Fig. 51 shows the pulses generated by the Registration Impulse Generator (RIG) chassis.

Fig. 52 shows in tabular form, the functional requirements of the input translating apparatus.

Fig. 53 is an aid to explaining the operation of the output translating apparatus.

Fig. 54*a* shows the manner in which a decimal point location is associated with numbers.

Fig. 54*b* is a table useful in explaining Fig. 54*a*.

Fig. 54*c* shows a typical switch for establishing decimal point location.

Fig. 55 shows the means for selecting one of a number of storage locations.

Fig. 56 shows the means for selecting one of a number of groups of input data.

Fig. 57 shows the means for selecting a particular data storage location.

Fig. 58 is a table useful in explaining the operation of the Decimal Counter (DCR).

Fig. 59 is an aid in explaining the registration of the factor called the minidend at the beginning of each step.

Fig. 60 is an aid in explaining the addition and subtraction steps.

Fig. 61 is an aid in explaining the multiplication step.

Fig. 62 is an aid in explaining the division step.

Fig. 63 is an aid in explaining the operation of the zero factor check circuits.

Figs. 64 to 183 are schematic diagrams of the various types of component assemblies shown as blocks in the block schematic diagrams.

While the preferred embodiment described herein comprises two physical units, a calculator and a reproducing punch, with cable interconnections between the units, only the calculator unit is shown and described in detail. Only the control elements of the reproducing punch unit are shown in detail. The card handling, sensing and punching mechanisms are not shown since they are well known in the art. For the same reason, the details of power supplies used in the apparatus have not been shown.

Fig. 1 is a block diagram of the system showing the general interrelation between its various elements. The apparatus comprises three major units or groups of elements. In the input-output unit data are read from and result data are recorded in conventional punched cards. In the data processing and storage unit input data are received and result data generated and stored for transfer to output. In the control unit, control signals for all elements of the system are generated and the sequence of data transfers and processing operations is thereby controlled.

The input-output unit comprises a card sensing station, a card punching station, card handling means (not shown) and card control means. All hole positions in a card are sensed simultaneously by a plurality of sensing pins at the card sensing station and all holes to be punched are punched simultaneously at the punching station. Data are represented in cards by means of the well known code referred to as the "90 column code."

In the data processing and storage unit the basic component is an electronic accumulator capable of registering 22 decimal digits. Each order of the accumulator is of the biquinary type and the accumulator is conditionable either to add or subtract input data from its previous contents. Its entire contents may be shifted any desired number of places in the direction of ascending significance, data from the highest order being shifted back to the lowest order.

The accumulator receives input data from three different sources via an input buffer and input translator. Input data may be transferred to the accumulator either from the card sensing station, result storage, or from constant storage. Data from each of these sources appear at the input buffer as combinations of static potentials and

appear similarly at the input translator. In the input translator, input data are translated from static potentials in the 90 column code to pulse sequences in the bi-quinary code and transferred in parallel to the ten least significant accumulator orders. In the accumulator data are appropriately shifted, registered, added and subtracted to produce a result and check its accuracy. The accumulator contents are then translated to the 90 column code and transferred to result storage for eventual transfer to card punching or for reuse as a factor in a subsequent computational step.

In the control unit, each of the elements shown, except the plugboard, consists of a single chassis or a number of similar chassis. The primary function of each of the control elements is described in the following paragraphs.

The plugboard permits the manual establishment of a program of operational steps for any calculating run. Each step consists of performing one of the four basic arithmetic operations, checking the result, transferring the result to storage and initiating a next step or an output control operation appropriate to the algebraic sign of the result. Fig. 42 shows the physical arrangement of the plugboard and the connections for a typical step. Connection **4201** establishes that the computation will start with step 5. Connection **4202** establishes that the process in step 5 will be division. Connection **4203** establishes that the number in storage location B will be the divisor (storage locations A–J are card sensing). Connection **4204** establishes that the number in storage location K_4 will be the dividend (storage locations K–M are constant storage). Connection **4205** establishes that the result is to be stored in storage location S (storage locations P–Y are result storage). Connection **4206** establishes that step 6 is the next step if the result is positive. Connection **4207** establishes that the card should be sorted into a special receiving hopper when it is subsequently released from the sensing station. Connection **4208** establishes that step 11 is the next step in the program. Connection **4209** establishes that when the result of any step fails to check, that step, rather than the entire program, will be started again. The foregoing example illustrates the simplicity and flexibility of programming and will facilitate the explanation of the functions of the control elements. The elements of the control unit shown in Fig. 1, perform the many functions necessary to carry out the steps and card control operations specified by the plugboard connections.

The step sequence chassis are closely associated with the plugboard and serve to energize the input lines of the plugboard in order to give effect to the plugboard connections. The step sequence chassis contain among other things a series of triggers stages associated with each of the 40 plugboard steps. While any given step is in progress, its associated triggers in the step sequence chassis are set in sequence to sequentially energize the various input lines to that step on the plugboard. The outputs of these triggers are effective, via the plugboard connections, to control data transfers and shifts to produce, check, and transfer to storage the desired result.

The keyboard bias chassis perform the function of enabling data transfer from a selected one of the various data storage locations. These chassis receive signals (static outputs) from the plugboard calling for data from a particular storage location and in response thereto, establish enabling potentials at the selected storage location so that the desired data are caused to appear as combinations of static potentials at the input translator via the input buffer or mixer.

The keyboard bias chassis can select any one of 9 groups of digits from the card sensing switches (storage locations A–J), any one of 20 groups of digits from the constant storage switches (storage locations K_1–K_5, L–L_5, M_1–M_5, N_1–N_5) or any one of the 8 groups of digits from the result storage relays (storage locations P–Y) in response to output signals from the plugboard.

In addition to enabling the transfer of groups of digits from selected storage locations, the keyboard bias chassis also enable the transfer of decimal point location data from the decimal switches associated with each storage location to the decimal counter. Whenever the transfer of a number is enabled the transfer of the data specifying its decimal point location is also enabled.

The registration impulse generator supplies pulse groups to the input translator over six lines in response to actuating signals from other control elements. These actuating signals occur whenever a number is to be registered in the accumulator. First the storage location containing the number is selected by the plugboard output and keyboard bias chassis and then the registration impulse generator is actuated to effect the actual translation and registration.

The decimal counter chassis controls the shifting of the accumulator contents and the alignment of decimal points. It includes a shift impulse generator that furnishes shift numbers from the accumulator to result storage count. The counter is automatically pre-set by decimal point location data at the same time any data transfer is enabled.

The sign bias chassis conditions the various accumulator orders to add or subtract in combinations appropriate to the operations being performed. The 22 accumulator orders are designated **1A–11A** and **1M–11M** in order of ascending significance. Data transfer are always made to or from orders **1A–10A**. To add positive or subtract negative numbers, the sign bias chassis conditions all 22 accumulator orders to add. To subtract positive or add negative numbers all accumulator orders are conditioned to subtract. During multiplication all orders except the highest one, **11M**, are conditioned to add and **11M** which contains the multiplier digits in sequence is conditioned to subtract. During division, orders **1A** to **11A** are normally conditioned to subtract since the A section receives the dividend in the repeated division process and the other orders **1M** to **11M** are conditioned to add since these orders receive signals indicating each subtraction of the divisor. During restoration of the dividend after an unsuccessful subtraction, orders **1A** to **11A** are conditioned to add and orders **1M** and **11M** are conditioned to subtract.

The function of the sign bias element is to condition the accumulators appropriately as outlined above during each of the types of operation. To perform this function, it receives control signals from other of the control elements to specify the arithmetic process to be performed, the sign of operator involved and whether, in the case of division, subtraction or restoration of the divisor is to be made.

The storage set element controls the transfer of result data from result storage to the card punch actuators at the completion of calculations.

The storage zeroize elements control the clearing of the result storage relays.

The base control element exercises direct control over the card control element in the input-output unit. The base control element in turn, receives control signals from the plugboard outputs via the output control element.

The test counter controls the halting of calculation at predetermined points established by the setting of switches.

The zero factor chassis detects zero divisors during division and governs the card control in accordance with a switch setting.

The other chassis including control, step control, decimal control, multiplication-division, and regulator chassis perform other specialized control functions that will be explained in the course of the operational description to follow.

The chassis units comprising what is referred to as the front of the calculator are shown in Fig. 2 and those comprising what is referred to as the back of the calculator

are shown in Fig. 3. These chassis are listed alphabetically in the following table which shows the number of chassis in each type and the abbreviated chassis designation used in the following descriptions.

Name of Chassis	Abbreviated Designation	Number Required
Accumulator	ACC (1A) to ACC (11M)	22
Base control	BCL	1
Control	CTL	1
Decimal control	DCL	1
Decimal counter	DCR	1
Input output	IO-1 to IO-10	10
Keyboard bias	KB-1 to KB-4	4
Multiplication division	MD	1
Output control	OCL	1
Zero factor	ϕF	1
Regulator	REG	1
Registration impulse generator.	RIG	1
Sign bias	SB	1
Step control	SCL	1
Step sequence	SS (1-4) to SS (37-40)	10
Storage	ST (P-1) to ST (Y-5)	40
Storage set	STS-1 and STS-2	2
Storage zeroize	STZ	1
Test counter	TCR	1

The details of each of the above chassis are shown in Figs. 16–34. Where more than one of a particular type of chassis is used, a typical one is shown in detail.

Some of the chassis are shown schematically while others are shown in block schematic notation. In the block schematic notation, the smallest component element shown is a stage which consists usually of a double triode (type 5964) or a double diode (type 6AL5) and associated circuit elements housed in a common can assembly.

The block schematic system of notation is as follows:

STAGE TYPE DESIGNATION

A. One or two letters and a number are used to specify the stage types. The letters represent a general stage type and the number represents a variation of that general stage type. Schematic diagrams of each stage type are shown in Figs. 64 to 183 which are in alphabetical order according to stage type.

B. Letter definitions:

Letter	Stage	Notes
A	Pulse amplifier	Grid return to −15 v. unless otherwise specified.
C	A.C. cathode follower	
D	D.C. amplifier	Divider return to −150 v. unless otherwise specified.
F	Flip-flop	
G	Gate	Do.
K	D.C. cathode follower	Do.
L	Limiter	
M	Multivibrator	
R	Regulator	
RC	Miscellaneous	Any stage not defined by other stage types.
S	Schmitt trigger	
T	Trigger	
X	D	Designates a tube with no associated stage.
(−)		Designates unused stage section.

C. Combination of letters denote combinations of various stage types. Some examples follow:

(1) GG—double gate
(2) DA—D.C. amplifier and A.C. amplifier
(3) L(—)—single limiter
(4) (—)A—single A.C. amplifier
(5) S—Schmitt trigger

D. Left letter designates section of stage used with left tube section.

E. Right letter designates section of stage used with right section of tube.

F. Single letter with dash designates stage designed to be used with half section of tube.

G. Single letter designates both sections of stage and tube used for a single function.

H. Left and right sections of tube defined as follows:

Tube type	Left Section			Right Section		
	K	G	P	K	G	P
5964	7	5	2	7	6	1
6AL5	5	------	2	1	------	7

A. Standard notations on block schematics (see Fig. 4):

RP—right plate
LP—left plate
RA—tap point on RP resistor
LA—tap point on LP resistor
RC—righ capacitive input
LC—left capacitive input
RD—tap point on RI divider
LD—tap point on LI divider
RI—right D.C. input
LI—left D.C. input
RB—right bias
LB—left bias

B. A small "D" in upper left corner designates a diode tube is used.

C. A small "P" in upper left corner designates a pentode tube is used.

D. A small "N" in upper left corner designates no tube is used.

E. All numbers on block schematics refer to stage pin connection.

F. Tube pin numbers are not shown in block schematics.

G. A number in the RP, LP, or K location generally indicates a stage connection which also connects to the corresponding tube point.

H. Lack of a number in any location indicates a connection to the tube only.

I. If two leads connect to the same location, the numbered lead is the stage pin connection, and the unnumbered lead is the tube pin connetcion.

J. Any bias return to other than the standard voltage is specified at the bias position.

K. A small "T" in upper left corner designates a thyratron is used.

The individual stages comprising the various chassis are listed alphabetically in the following Alphabetical Index of Stages. The type designation shown opposite each stage name specifies the assemblage of electrical elements comprising the stage, each type being shown schematically in one of Figs. 64–183, which are arranged alphabetically by stage type. The chassis code opposite each stage name designates the chassis of which the named stage is a part, each chassis being shown schematically or in block schematic form in one of Figs. 16–34, which are arranged alphabetically by chassis designation.

For example, stage CA is seen to be of the type designated DD-8. In accordance with the stage type notation described above, this stage is a D.C. amplifier. The schematic diagram for the stage is shown in Fig. 94. The index also shows the stage to be a part of the decimal counter (DCR) chassis which is shown in block schematic form in Fig. 20.

Information regarding any stage named in the following descriptions may be found in a similar manner.

Alphabetical index of stages

Stage Name	Stage Type	Chassis Code
AC	DA-2	ACC
B11+	K-2	SB
B11−	K-2	SB
B11+1	RC-27	SB
B11−1	RC-27	SB
BA+	K-2	SB

Stage Name	Stage Type	Chassis Code
BA−	K-2	SB
BA+1	RC-27	SB
BA−1	RC-27	SB
BM	K-2	SB
BM−	K-2	SB
BM+1	RC-27	SB
BM−1	RC-27	SB
C09	X	10
C17	LL-1	10
C35	X	10
CA	DD-8	DCR
CA1	RC-1	DCR
CAP(1)	RC-14	STS
CAP(2)	RC-14	STS
CAP(3)	RC-14	STS
CAP(4)	RC-14	STS
CAP(5)	RC-14	STS
CAP(6)	RC-14	STS
CAP(7)	RC-14	STS
CAP(8)	RC-14	STS
CB	S-1	DCR
CD	F-5	RIG
CM	M-2	DCR
CMA	DA-1	DCR
CS	GG-2	DCR
CSK	C-1	DCR
CT	T-1	DCR
CX	GG-6	DCR
CDA	AA-10	RIG
D2-4C	GG-9	DCR
D2-4T	GG-9	DCR
D8-16C	GG-9	DCR
D8-16T	GG-9	DCR
DA1-16	AA-16	DCL
DAM	T-4	DCL
DAS	T-4	DCL
DAX	T-3	DCL
DB2	AA-1	DCR
DB4	AA-15	DCR
DB8	AA-1	DCR
DB16	GA-3	DCR
DBC	K-3	DCL
DBT	K-3	DCL
DC1	T-3	DCR
DC2	T-3	DCR
DC4	T-3	DCR
DC8	T-3	DCR
DC16	T-3	DCR
DCC	T-4	DCR
DCCD	F-1	DCR
DCCL	X	DCR
DEA	F-6	DCL
DEA1	AA-2	DCL
DEA2	AA-2	DCL
DEM	S-1	DCL
DG	GG-1	DCL
DI-1	GG-10	DCR
DIC	GA-7	DCR
DK	T-3	DCL (1, 2-39, 40)
DKG	GG-1	DCL
DMD	DD-1	DCL (1, 2-39, 40)
DMG	GG-1	DCL
DMP	S-1	DCL
DN2-16′	X	DCR
DN8-16	X	DCR
DN4′	X	DCR
DN1-2′	RC22	DCR
DN4-8′	X	DCR
DP1	F-1	DCR (1, 2-39, 40)
DP2	F-1	DCR
DP4	F-1	DCR
DP8	F-1	DCR
DP16	F-1	DCR
DPG1	GA-7	DCL
DPG2	GA-9	DCL
DRV	T-4	DCL
DRP	S-1	DCL
DRS	T-1	DCL
EAA	RC-2	OCL
EAB	RC-2	OCL
EAC	RC-2	OCL
EBAL	F-3	BCL
EBM	K-3	SCL
EBM	X	SS
EBP	K-3	SCL
EBP	X	SS
EBS	T-2	SCL
EC	RC-23	SS
ECS	GA-7	CTL
ECB1	DD-1	CTL
ECB2	K-7	CTL
ECF	F-3	OCL
ECG	DA-1	OCL
ED	GG-4	SS
EG	GG-6	SCL
EFP1	RC-24	OCL
EFP2	RC-24	OCL
EGϕ	GG-22	OCL
EGA	S-2	BCL
EGC1	T-1	OCL
EGC2	T-1	OCL
EGCA	AA-12	BCL
EGCB	DD-9	OCL
EGCD	CG-4	OCL
EGCG	GG-16	BCL
EGD	F-4	SCL
EGDC	DA-5	OCL
EGP	T-4	OCL
EGPG	GG-16	BCL
EGT1	AA-7	BCL
EGT2	AA-7	BCL
EIA	DD-7	DCL
EIA1	X	DCL
EIA2	X	DCL
EIA3	X	DCL
EID	DD-7	DCL
EID1	X	DCL
EID2	X	DCL
EIM	DD-7	DCL
EIM1	X	DCL
EIM2	X	DCL
EIS	DD-7	DCL
EIS1	X	DCL
EIS2	X	DCL
EIC1	T-1	OCL
EIC2	T-1	OCL
EICA	AA-12	BCL
ELCB	DD-9	OCL
ELCD	GG-4	ESD
ELCG	GG-16	BCL
ELCT	AA-7	BCL
EM	T-4	CTL
EMA	DD-7	CTL
EMDC	GA-4	CTL
EMDZ	F-3	CTL
EMF	RC-2	SS
EMK	K-3	CTL
EMZ	F-3	CTL
EMZ′	RC-21	CTL
ENC	T-1	OCL
ENCD	RC-28	OCL
ENCG	GG-16	BCL
ENM	AA-6	CTL
ENM1	AA-6	CTL
EP	F-3	SCL
EP′	RC-21	SCL
EP1	DD-7	DCL
EP2	DD-7	DCL
EP3	T-4	SCL
EP3C	RC-16	SCL
EP4	F-3	SCL
EP4′	RC-11	SCL
EP5	GG-11	SCL
EPC1	T-1	OCL
EPC2	T-1	OCL
EPCA	AA-12	BCL
EPCD	GG-4	OCL
EPCG	GG-16	BCL
EPCT	AA-7	BCL
EPF	X	SS
EPG	AA-11	CTL
EPM	T-4	CTL
EPMA	DA-1	CTL
EPP	T-4	CTL
EPP1	DD-7	DCL
EPP2	DD-7	DCL
EPPM	X	DCL
EPR	RC-14	SCL
EPS	T-4	CTL
EPX	DD-4	SCL
EPX′	RC-9	SCL
EPZ	F-3	CTL
EPZC	RC-11	CTL
ER	T-4	CTL
ERA	DD-1	CTL
ERAZ	DA-1	CTL
ERF	X	SS
ERK	K-3	CTL
ES	T-4	CTL
ES	T-1	SS
ESA	DD-1	CTL
ESB1	DD-1	SCL
ESD	F-3	SCL
ESF	DD-9	SS
ESI1	AA-2	SCL
ESI2	X	SCL
ESIA	AA-10	SCL
ESK	K-3	CTL
ESZ	AA-2	SCL
ESZA	AA-16	SCL
ESZ1	GA-10	SCL
ESZ2	AA-2	SCL
ETM1	X	BCL
ETM2	RC-15	BCL
ETM3	RC-15	BCL
ETM4	RC-13	BCL
EXCC	RC-21	OCL
EZ	F-3	CTL
EZB2	F-2	CTL
EZB5	F-2	CTL
EZB5′	RC-10	CTL
EZG	AA-2	CTL
EZS	GA-1	CTL
EϕC	GG-17	CTL
EϕCA	GA-6	SB
EϕCB	DD-12	SB
EϕCT	T-2	CTL
I09	AA-3	10
I1-i1	GG-7	RIG
135	GG-11	10
179	GG-11	10
19	AA-4	10
IA9	DL-1	10
KB(A-Y)	K-1	KB
KB(A-Y)	DD-2	KB
M9	RC-4	10

Stage Name	Stage Type	Chassis Code
M13	X	10
M17	RC-3	10
M35	RC-3	10
M57	RC-5	10
MA9	D(—)-1	10
MC1	GG-20	φF
MC2	T-1	φF
MC3	AA-2	φF
MC4	DD-7	φF
MCX	X	φF
MC4L	X	φF
MC5	DD-1	φF
MC6	DA-1	φF
MC7	DD-7	φF
MC7A	RC-3	φF
MC8	DD-7	φF
MCA	RC-13	STZ
MCB	RC-13	STZ
MCC	RC-13	STZ
MCD	RC-13	STZ
MCE	RC-13	STZ
MCR	RC-13	STZ
MCG	RC-13	STZ
MCH	RC-13	STZ
ME	K-5	10
MK(P-Y)	RC-25	STS
MO	K-5	10
MS	F-3	DCL
MS'	RC-13	DCL
MS(P-Q) (W-Y)	DD-10	STS—(4 stages)
MSA	DA-5	DCL
MSI	DD-1	DCL
MSK	K-6	DCL
MST	T-2	DCL
MZ'	F-3	STZ
MZ2	F-3	STZ
MZ3	F-3	STZ
MZ4	F-3	STZ
MZ5	F-3	STZ
MZ6	F-3	STZ
MZ7	F-3	STZ
MZ8	F-3	STZ
MZ(1-8)A	A-2	STS
MZA	CG-8	STZ
MZB	CG-8	STZ
MZC	CG-8	STZ
MZD	CG-8	STZ
MZK	C-1	STZ
MZR	DD-7	DCL
MZT	T-4	DCL
MφC	X	IO
Neon (1, 2)	RC-7	STS
P11C	DA-7	MD
P11G	K-3	MD
P11S	T-2	MD
PABA	DD-7	SB
PABA1	DD-7	SB
PABS	DD-7	SB
PABS1	DD-7	SB
PAC	T-3	φF
PAD	F-2	CTL
PAM	T-1	SB
PAMD	F-6	CTL
PAT	T-3	φF
PC1	T-3	MD
PC2	T-3	MD
PC4	T-3	MD
PC8	T-3	MD
PC16	T-3	MD
PCG	GA-7	MD
PD1	T-4	MD
PD1M	RC-1	MD
PD2	T-4	MD
PD2D	F-1	MD
PD3	T-1	MD
PDA	DD-13	MD
PDAM	F-1	SB
PDB	T-2	MD
PDM	GA-6	MD
PDM3	AA-9	MD
PDMS	GG-2	MD
PDN	T-2	MD
PDND	F-1	MD
PDP	S-1	MD
PDS	T-4	MD
PDT	T-4	MD
PDX	GG-2	MD
PGMD	GA-4	MD
PIAS	RC-17	φF
PIMD	RC-17	φF
PMφ	S-1	MD
PMφD	F-1	MD
PM1	T-2	MD
PM12	CG-6	MD
PM2	T-1	MD
PM22	DD-12	MD
PM23	DA-6	MD
PM3	F-1	MD
PMBT	T-1	MD
PMD1	F-4	MD
PMD2	F-1	MD
PMDR	GG-2	MD
PMDZ	T-4	MD
PMG	GG-1	MD
PMM	AA-2	MD
PMP	S-1	MD
PMS	DD-3	MD
PPI	DD-6	φF

Stage Name	Stage Type	Chassis Code
PS	GG-1	φF
PS11	S-1	MD
PSA	DD-1	SB
PSAC	LL-2	SB
PSG	DD-1	MD
PSGK	K-3	MD
PSφ	G(—)-2	φF
PX	X	RIG
PZG	GA-7	MD
Rφ	AA-6	ACC
R1	*AA-13	ACC
R1	T-4	RIG
R11	K-4	RIG
RIM	DA-3	RIG
R1'1'	K-4	RIG
R1'8	AA-8	RIG
R''	AA6	ACC
R''	T-3	RIG
R22	K-4	RIG
R4	AA-6	ACC
R4	T-3	RIG
R42	AA-10	RIG
R44	K-4	RIG
R6	AA-6	ACC
R66	K-4	RIG
R8	AA6	ACC
R8	M-2	RIG
R88	K-4	RIG
RB	AA-14	SB
RBK	RC-18	SB
RC	AA-6	ACC
RD	F-2	RIG
RES	RC-8	STS
RS	F-1	RIG
Sφ	GG-12	ACC
S1	*GG-10	ACC
S2	GG-12	ACC
S4	GG-12	ACC
S6	GG-12	ACC
S8	GG-12	ACC
SCK	RC-6	DCR
SCK1	RC-1	DCR
SG	GA-8	DCR
SI-1	RC-11	MD
SI-2	X	DCL
SK1	C-2	DCR
SK2	RC-20	DCR
SK3	X	DCR
SKP	X	REG
SKQ	X	REG
SKR	X	REG
SKS	X	REG
SKT	X	REG
SKV	X	REG
SKW	X	REG
SKY	X	REG
SM	M-1	DCR
SMA	(—)A-3	DCR
SMG	AA-1	DCR
SZB1	RC-26	STS
SZB2	RC-26	STS
Tφ	T-1	ACC
T1	T-3	ACC
T1	T-3	TCR
T1φ	T-3	TCR
T2	T-1	ACC
T2	T-3	TCR
T2φ	T-3	TCR
T2	T-1	TCR
T2φ	T-1	TCR
T4	T-1	ACC
T4	T-3	TCR
T4φ	T-3	TCR
T6	T-1	ACC
T8	T-1	ACC
TB	T-2	TCR
TC	T-1	ACC
TC1	T-3	TCR
TC2	T-3	TCR
TDG	GG-14	TCR
TG	GK-1	TCR
TK	K-3	TCR
TS	T-2	TCR
TSA	AA-1	TCR
TSAL	RC-1	TCR
TUG	GG-14	TCR
ZB2	X	REG
ZB5	X	REG
ZB52	R-1	CTL
ZBA2	R-2	CTL
ZBA5	R-2	CTL
ZBB2	D-2	CTL
ZBB5	D-2	CTL
φ9C	DD-11	φF
φ9C1	X	φF
φ9M	DD-1	φF
φ9SM	DD-1	φF
φ9SM1	DD-7	φF
φESP	AA-2	φF
φC1	F-2	φF
φC2	GA-7	φF
φEZ	GG-21	φF
φEZ1	GG-21	φF
φF1	T-1	φF
φF2	GA-1	φF
φF3	GA-1	φF
φF4	GG-18	φF
φF5	G(—)-2	φF

Stage Name	Stage Type	Chassis Code
φFD1	F-1	φF
φFD3	X	φF
φFM	RC-17	φF
φFR1	DD-1	φF
φFR2	DD-7	φF
φFS	F-1	φF
φFZD	F-3	φF
φFZT	RC-13	φF
φMD	T-1	φF
φRS	T-5	φF
φRSZ	AA-2	φF
φSR	T-1	φF

Figs. 5–15 show schematically a number of basic types of electronic components used in the calculator. While various circuit modifications of each type are described in the stage schematics (Figs. 64–183) the principles of operation of each type apply to modifications of the type as well and are described in the following paragraphs.

Fig. 5 shows a typical D.C. amplifier used in the calculator. The grid of this tube is returned to −150 and when the D.C. input is low the tube will be cutoff. As the D.C. input is raised the plate will conduct, causing a drop in plate voltage. This condition will exist as long as the D.C. input is raised. When the D.C. input is again lowered the grid will be cut off and the plate voltage will rise.

Fig. 6 shows a typical positive pulse amplifier used in the calculator. The positive pulse amplifier is used for isolation and polarity reversing. The grid is biased to cutoff. A positive pulse at the input will cause a pulse of current which will produce a negative pulse at the plate.

Fig. 7 shows a typical negative pulse amplifier used in the calculator. The negative pulse amplifier is used for isolation and polarity reversing. The grid is returned to +150 and because there is some grid current the grid will tend to stay at zero potential. An incoming negative pulse will drive the tube to cutoff and produce a positive pulse at the plate.

Fig. 8 shows a typical A.C. cathode follower used in the calculator. The cathode follower is used as an impedance changer to provide a low impedance driving source from a high impedance input. A positive pulse at the input will cause a pulse of current to flow producing a positive pulse at the cathode.

Fig. 9 shows a typical gate used in the calculator. A gate is a circuit which allows positive pulses to pass when the gate is open (D.C. input up) and blocks them when the gate is closed (D.C. input down). The output pulse from the plate is negative. With the gate closed the grid is biased way below cutoff through resistor R. If a positive pulse is applied to the grid it will not raise the grid voltage sufficiently to allow the plate to conduct. When the gate is open the D.C. input is raised and the grid voltage is held a little below cutoff. When a positive pulse is applied it will drive the grid voltage to zero and allow the plate to conduct, to give a pulse of current which will give a negative pulse at the plate.

Fig. 10 shows a typical Schmitt trigger used in the calculator. A Schmitt trigger circuit is a form of trigger circuit which is controlled by a D.C. input. Assume plate 1 conducting with the D.C. input sufficiently low to cutoff grid 5. As the D.C. input is raised a voltage will be reached where grid 5 allows plate 2 to conduct. Plate 2 conducting will pull down the voltage on the right divider and drive grid 6 negative. Grid 6 going negative will reduce the current through plate 1 and raise the voltage on the left divider. The A.C. component will be coupled through C to raise grid 5. This is a regenerative action which ends up with grid 6 cutoff and plate 2 conducting. This regenerative action, due to the constants of the circuit, will occur within a few microseconds. This condition will remain as long as the D.C. input remains up. When the D.C. input is dropped the circuit flips back into its original state with grid 5 cutoff and plate 1 conducting. This Schmitt trigger is used to form a slowing rising D.-C. input into a sharply rising wave front.

Fig. 11 shows a typical trigger circuit used in the calculator. A trigger circuit is one which has two stable states. When plate 1 is conducting it will maintain grid 5 below cutoff through the left hand voltage divider. Likewise plate 2 will maintain grid 6 at zero. In its other stable state plate 2 conducts, grid 6 is cutoff, and plate 1 maintains grids 5 at zero. A negative pulse applied to the input will cause the circuit to change from one stable state to the other. Magazine article in Electronics, July 1945, p. 110, will give more details as to the operation of this circuit.

Fig. 12 shows a typical flip-flop or univibrator used in the calculator. A flip-flop circuit is used as a pulse delay circuit, the delay being determined mainly by the time constant of R and C. In rest position plate 1 is conducting, since grid 6 is connected to +150 through R, and grid current through R holds the grid at zero potential. When a negative pulse comes in it will drive grid 6 negative. Grid 6 going negative will reduce the current through plate 1 and raise the voltage on the left divider. This will be coupled back to raise grid 5. Raising grid 5 will allow plate 2 to conduct. This will drop the voltage on plate 2 and since C cannot charge quickly the voltage on grid 6 will drop. This is a regenerative action which takes place in a few microseconds and ends up with grid 6 cutoff, plate 2 conducting and C with its original charge. C will now discharge through R at a rate determined by Time Constant until grid 6 becomes sufficiently positive to allow plate 1 to conduct and the circuit will flip back into its original state with grid 5 at cutoff and plate 1 conducting.

Fig. 13 shows a typical flip-flop clamp used in the calculator. Flip-flops EPZ, PAD, MS, DEA, DCCD, φFZD are clamped by EZ during B5, B2 zeroize to prevent accidental tripping by transient pulses caused by the zeroizing operation.

Fig. 14 shows a typical cathode clamping circuit used in the calculator. A type ING5 germanium diode is used to prevent the cathode of the triode from dropping below ground potential. The diode conducts whenever the cathode of the triode falls below the potential at which the anode of the diode is maintained.

Fig. 15 shows a typical step trigger and gate used in the calculator. The elements shown are part of a typical step sequence chassis. The ESI pulse through diode (1, 2)ED sets the trigger (2)ES causing it to conduct on the right providing the triode EBP, EBM is conducting when the pulse ESI arrives. This circuit is used extensively in the branching facilities of the step sequence chassis which will be described later.

Before proceeding to a description of the various chassis comprising the control unit (Fig. 1), the chassis comprising the data processing and storage unit will first be described and their relation to the card sensing and card punching apparatus will be discussed. Briefly, the functions and organization of these chassis are as follows:

All actual modifications of data occur as either additions or subtractions in the 22 order accumulator. Input data are transferred to the 10 least significant orders of the accumulator via an input buffer and input translator from three distinct data sources, namely, card sensing switches, constant storage switches, and result storage switches. Numbers are represented in each of these three groups of switches in the conventional "Powers" or "90 column" code (combinations of 5 bi-valued manifestations). The switches deliver combinations of static potentials representative of digits to an input translator via an input buffer which serves to isolate the various storage switches. In the input translator the static potentials representative of each digit are translated to a bi-

quinary pulse group. The pulse group representative of each digit is delivered over two lines (one binary and one quinary) to one order of the accumulator where it is either added to or substracted from the previous content of the accumulator order. Final result digits generated in the accumulator orders are delivered as static potentials to an output translator which translates the bi-quinary static potentials to "Powers" code static potentials. The translated potentials are delivered to result storage where they selectively energize result storage relays to store the digits of a result. Once stored in the result storage relay a number may be transferred to card punching actuators in the card handling unit or may be fed through the input buffer and input translator to the accumulator as a factor in a subsequent calculation.

ACCUMULATOR

Since the accumulator is the basic data processing element of the machine, it will be described first as a basis for subsequent descriptions of the other elements.

The accumulator consists of twenty-two separate chassis designated 1A to 11A and 1M to 11M (Fig. 3). Each of these chassis contains a reversible bi-quinary decade counter together with carry circuits, shift circuits, and indicator circuits. All twenty-two chassis are identical except for a few minor differences that will be pointed out later. A typical accumulator chassis will first be described with reference to Fig. 16 which is a schematic circuit diagram of chassis 2A.

The chassis contains 21 stages. Of these, seven stages designated T are bi-stable triggers comprising a portion of the bi-quinary counter and its associated carry trigger (TC). Seven other stages designated R are gating amplifiers which selectively interconnect the counting triggers T for adding or subtracting; each of these stages R includes two separate gating amplifiers one of which is enabled during addition and the other of which is enabled during subtraction. Six stages designated S are shift gates coupling their associated counting triggers T with corresponding counting triggers of the next lower order accumulator chassis; each of these gate stages S includes two separate gates—one for turning the associated trigger on and the other for turning it off. The remaining one of the 21 stages (AC) consists of a D.-C. amplifier and a pulse amplifier which perform carry functions that will be described later. Six indicator neons 1, 0, 2, 4, 6 and 8 are coupled respectively with the six counting triggers so as to glow when the associated triggers are on.

Before proceeding to a description of the interconnections between the various stages in the chassis and their operation, consider first the following table which shows the condition of the counting triggers for each of the digits 0–9. Triggers not indicated to be on are off.

Table 1

	T1	T0	T2	T4	T6	T8
0		On				
1	On	On				
2			On			
3	On		On			
4				On		
5	On			On		
6					On	
7	On				On	
8						On.
9	On					On.

Data signals are delivered to the counters over two input lines as combinations of pulses. Pulses delivered on one input line (via chassis terminal 18, Fig. 16) have a numeric value of one and are used to actuate the binary counter consisting of trigger T1. Pulses delivered on the other input line (via chassis terminal 36) have a numeric value of two and are used to actuate the quinary counter comprising the triggers T0, T2, T4, T6, and T8. By way of example, the digit 5 is delivered to an accumulator counter as two double valued pulses and one single valued pulse. The single valued pulse actuates T1 and the double valued pulses actuate the counting chain comprising T0, T2, T4, T6, and T8. Both single and double valued pulses are negative pulses and are generated in the input translator in a manner later to be explained.

Single valued pulses are delivered from terminal 18 to the common pulse input to trigger T1 so that T1 will change state (from off to on or from on to off) each time a single valued input pulse is delivered. Double valued input pulses are delivered from terminal 36 to the left pulse inputs of triggers T0, T2, T4, T6, and T8, so that whichever of these triggers is on, will be turned off by any double valued pulse.

Triggers T0, T2, T4, T6, and T8 are intercoupled through gating amplifier stages R0, R2, R4, R6, and R8 in such a way that when a trigger that was on is turned off, another trigger will be turned on; during addition the right sides of gating amplifiers R are enabled so that the next higher trigger will be turned on and during subtraction the left sides are enabled so that the next lower trigger will be turned on. Thus triggers T0, T2, T4, T6, and T8 are intercoupled by gating amplifiers R0, R2, R4, R6, and R8 to form a reversible quinary counting ring. Only one of these triggers is on at any given time and whichever trigger is on is turned off by a pulse (double valued and negative) over the common input line. The pulse generated by the trigger turning off turns on the next higher trigger (during addition) or the next lower trigger (during subtraction). The specific circuits intercoupling the quinary counter triggers Tϕ, T2, T4, T6, and T8 are described below.

The right plate of Tϕ is connected to the right capacitive input to R2 and to the left capacitive input to R8 so that when Tϕ is turned off during addition, T2 will be turned on through R2 and when Tϕ is turned off during subtraction, T8 will be turned on through R8. The right plate of Tϕ is also connected to the left capacitive input to gating amplifier RC so that when, during subtraction, T2 is turned off, the carry trigger TC will be turned on through RC. To this end the left bias input to RC is connected to terminal 50 which rises during subtraction and the common plate connection of RC is connected to the right plate of carry trigger TC.

The right plate of T2 is connected to the right capacitive input to R4 and to the left capacitive input to Rϕ so that when, during addition, T2 is turned off, T4 will be turned on through R2 and when, during subtraction, T2 is turned off, Tϕ will be turned on.

In a similar manner, the right plate of T4 is connected to the right capacitive input to R6 and to the left capacitive input to R2 so that when, during addition T4 is turned off, T6 will be turned on through R6 and when, during subtraction, T4 is turned off, T2 will be turned on through R2.

Similarly the right plate of T6 is connected to the right capacitive input to R8 and to the left capacitive input to R4 so that when, during addition, T6 is turned off, T8 will be turned on through R8 and when, during subtraction, T6 is turned off, T4 will be turned on through R4.

In the same manner, the right plate of T8 is connected to the right capacitive input to Rϕ and to the left capacitive input to R6 so that when, during addition, T8 is turned off, Tϕ will be turned on through Rϕ and when during subtraction T8 is turned off, Tϕ will be turned on through Rϕ. The right plate of T8 is also connected to the right capacitive input to RC so that when T8 is turned off during addition, carry trigger TC will be turned on through RC.

Trigger T1 is coupled with the quinary counter (comprising triggers T0, T2, T4, T6, and T8) through gating amplifier stage R1 in such a way that the quinary counter will receive an actuating pulse when binary counter trig-

ger T1 changes from 1 to 0 (is turned off) during addition and from 0 to 1 (is turned on) during subtraction. More specifically, the left plate of T1 is connected with the left capacitive input to gating emplifier R1 and the right plate of T1 is connected with the right capacitive input of R1. The common output of gating amplifier R1 is connected to the common input to the quinary counter stages T0, T2, T4, T6, and T8. The right bias of R1 is raised via terminal 49 during addition so that the positive pulse from the right plate of T1 when T1 changes from 1 to 0 will be amplified and inverted to actuate the quinary counter. During subtraction the left bias of R1 is raised via terminal 50 so that the positive pulse from the left plate of T1 when T1 changes from 0 to 1 will be amplified and inverted to actuate the quinary counter.

As will be explained later, the input pulses to an accumulator order over the binary and quinary input lines are so timed that pulses from the two lines never arrive simultaneously. This prevents the erroneous operation that would otherwise occur if a pulse over the quinary input line and a pulse from the binary counter trigger T1 coincided.

By way of illustrating how the counting triggers and gating amplifiers of an accumulator order operate, consider the sequence of events during the entry of the digit 5 to the accumulator order just described. Assume that prior to the entry of the digit 5, the accumulator has been cleared and stands at zero, and assume further that the accumulator order is conditioned to add. The clearing pulse (positive) which arrived over terminal 30 turned off triggers T1, T2, T4, T6, and T8 and turned on trigger Tϕ. The digit 5 arrives at the accumulator order from the input translator as one single valued pulse at the binary input terminal 18 and two double valued pulses at the quinary input terminal 36. These three pulses are separated in time as will be explained later in connection with the input translator; actually the order in which they arrive is of no importance providing no two arrive simultaneously. Assuming that the single valued pulse at binary input terminal 18 arrives first, it will turn on trigger T1. The negative pulse developed at the right plate of T1 will be ineffective to actuate the quinary counter through R1 since R1 is already cut off and its left grid will only be driven further negative. The lowered potential at the left plate of T1 will cause conduction in indicator neon 1 to which it is connected, however, since the other terminal of the neon is connected to the positive supply B+. The positive pulse developed at the left plate of T1 as it is turned on will not pass the left side of R1 since during addition the left sides of the gating amplifiers R are biased far enough below cutoff that positive pulses applied to left capacitive inputs will not cause conduction. Thus, the only effect of the single valued input pulse over binary input line 18 is to turn on T1 and light its associated indicator neon.

The arrival of the first of the two double valued pulses over quinary input terminal 36 will turn off trigger Tϕ but will not directly effect triggers T2, T4, T6, and T8 which were already off. The negative pulse developed at the left plate of Tϕ when Tϕ turns off does nothing. The positive pulse developed at the right plate of Tϕ causes momentary conduction in the right side of gating amplifier R2 since its right bias is reduced during addition. The resulting negative pulse at the common plate connection of R2 turns on T2 which in turn lights indicator neon 2. The positive pulse from the right plate of Tϕ does not turn on the carry trigger TC since the left side of gating emplifier RC is inhibited during addition. The effect of the first double valued input pulse is, then, to turn off Tϕ and turning off Tϕ turns on T2.

In a similar manner, the arrival of the second double valued input pulse at quinary input terminal 36 turns off T2 and this turns on T4. Triggers T1 and T4 are then conducting to manifest a registered value of 5 and the associated indicator neons 1 and 4 are conducting. All other triggers and indicator neons are off.

Consider now the sequence of events when a second number, say 8, is entered after a 5 has been entered as described above. Assume again that the process is addition and that consequently the right halves of gating amplifiers R are enabled by the raised potential at terminal 49 and that the left halves are inhibited by the lowered potential at terminal 50.

As will be described later, the digit 8 arrives at the accumulator order as a sequence of four double valued pulses at the quinary input terminal 36 and no pulses at the binary input terminal 18. Recall that the accumulator order initially registers 5 (triggers T1 and T4 on) before the pulses representing the new digit 8 arrive. The first of these pulses turns off T4 and the resulting pulse turns on T6 through R6. The second pulse turns off T6 and the resulting pulse turns on T8 through R8. The third pulse turns off T8 and the resulting pulse turns on Tϕ through Rϕ and also turns on carry trigger TC through RC. The fourth and last pulse turns off Tϕ and the resulting pulse turns on T2 through R2. Thus after all of the four pulses representing the digit 8 have arrived, trigger T1 is still on since it was not affected, trigger T2 is on, and carry trigger TC is on; T1 and T2 on indicate a registered value of 3, the second digit of the sum 13 (of 8+5) and the carry trigger TC on will enable a carry pulse to be applied to the next higher denominational order.

Carry pulses are not transferred to next higher accumulator orders at the instant the carry occurs (i.e. at the instant the carry trigger TC is turned on) but are handled after the registration of digits in the accumulator is complete. To understand how carries are handled, note first that carry pulses are delivered to the next higher accumulator order from carry output terminal 17 which is connected to the left plate of gate-amplifier AC. The left capacitive input to AC is connected to the right plate of carry trigger TC so that when TC is turned off, the resulting positive pulse at the right plate of TC will cause momentary conduction in the left half of AC and a consequent negative pulse at carry output terminal 17. The negative pulse developed at the right plate of TC when TC is turned on is ineffective to produce any signal at terminal 17 since the left side of AC is biased to cutoff. Thus, it is seen that a carry pulse is delivered to the next higher order when the carry trigger TC in a given order is turned off. The pulse is transmitted from carry output terminal 17 of the given order to the binary input terminal 18 of the next higher order.

The pulse that turns off carry trigger TC arrives at terminal 14 of each accumulator chassis. This terminal is connected to the left capacitive input to carry trigger TC. Pulses are delivered in common to terminal 14 of each accumulator chassis after the registration of each number providing the registration of the number caused any carry triggers TC to be turned on. Note that the left plate of TC is connected to the right input of AC so that when TC is on, the right plate of AC (and consequently terminal 9 to which it is connected) is low. A lowered potential at terminal 9 of any of the 22 accumulator chassis indicates that a carry has occurred and causes carry pulses to be delivered to terminals 14 in common after the number registration is complete. The carry impulse generator which receives the signal from terminals 9 and delivers carry pulses to terminals 14 will be described in detail later.

Recall that result digits generated in the various accumulator orders must be translated to the "Powers" code before delivery to result storage. These result digits appear in each accumulator order as static potentials at terminals 11, 13, 23, 25, 27, 39, 43, and 47. Terminal 11 is coupled with the right plate of T1 through a divider located in S1 so that the potential at terminal 11 is high when an even digit is registered and low when an odd digit is registered. Terminal 13 is coupled with the left plate of T1 through a divider located in R1 so that termi-

nal 13 is high when an odd digit is registered and low when an even digit is registered. Terminal 23 is coupled with the right plate of Tφ through a resistor located in Sφ so that terminal 23 is high whenever Tφ is off and low when Tφ is on. Terminal 25 is coupled with the left plate of T8 through a resistor located in S8 so that terminal 25 is high when T8 is on and low when T8 is off. Terminal 27 is coupled with the right plate of T8 through a resistor located in S8 so that terminal 27 is high when T8 is off and low when T8 is on. Terminal 39 is coupled with the right plate of T2 through a resistor located in S2 so that terminal 39 is high when T2 is off and low when T2 is on. Terminal 43 is coupled with the right plate of T6 through a resistor located in S6 so that terminal 43 is high when T6 is off and low when T6 is on. Terminal 47 is coupled with the right plate of T4 through a resistor located in S4 so that terminal 47 is high when T4 is off and low when T4 is on.

The high or low potentials at the above mentioned terminals serves to specify at all times, the digit registered in each accumulator order. These terminals are connected to terminals on the output translator (Input Output Chassis) in a manner later to be described.

The shift gates S1, Sφ, S2, S4, S6, and S8 in the accumulator chassis will now be described. These gates serve to transfer to one accumulator order the digit registered in the next lower order. Each shift gate stage has its left and right plates connected to the right and left plates respectively of its associated counter trigger; e.g. shift gate S1 has its left and right plates connected to the left and right plates respectively of trigger T1. The left and right grids of the shift gate stages in each accumulator order are coupled with the right and left plates respectively of the corresponding counter trigger in the next lower accumulator order; e.g. the left and right grids of shift gate S1 are coupled to the right and left plates respectively of trigger T1 in the next lower accumulator order via chassis terminals 16 and 20. The left and right capacitive inputs to all shift gates are connected in common to terminal 5. Shift pulses (positive pulses) are supplied to terminal 5 on all accumulator chassis from a shift impulse generator later to be described. When a shift pulse occurs either the left or right half of each shift gate is caused to conduct momentarily depending upon whether the associated counting trigger in the next lower accumulator order is on or off. If the lower order trigger is on when the shift pulse occurs, the right side of the associated shift gate in the higher order will conduct and cause its associated trigger in the higher order to be turned on. If the lower order trigger is off when the shift pulse occurs, the left side of the associated shift gate in the higher order will conduct and cause its associated trigger in the higher order to be turned off. Thus, it is seen that on the occurrence of a shift pulse, the contents of each accumulator order is transferred to the next higher accumulator order via the shift gates in the next higher order.

The gating potentials from the counting triggers in one order to the shift gates of the next higher order appear at chassis terminals 15, 19, 21, 23, 25, 27, 37, 39, 41, 43, 45 and 47 which are connected respectively with terminals 16, 20, 22, 24, 26, 28, 38, 40, 42, 44, 46, and 48 of the next higher order chassis. The successive pairs of connections in the listing above are related respectively to counting triggers T1, Tφ, T8, T2, T6 and T4.

For reasons that will be described later, it is sometimes necessary to prevent the normal carry operation. This is done by lowering the potential at terminal 12 which biases the left side of AC so far below cut-off that no conduction will occur even when a positive pulse is applied to its left capacitive input.

Also, for reasons to be explained later, it is necessary that accumulator order 11M, the highest order, signal the control portion of the machine when it contains a zero. To this end, terminal 1 is coupled with the left plate of T1 so that the potential at terminal will be low only when T1 is off and terminal 3 is coupled with the right plate of Tφ so that the potential at terminal 3 will be low only when Tφ is on. Thus, the potential at terminals 1 and 3 will be simultaneously low only when the accumulator order registers the value zero (Tφ on and T1 off). The use of these signals from terminals 1 and 3 will be discussed later in connection with the division process.

The complete accumulator comprises 22 chassis of the kind described in the foregoing. These are designated 1A to 11A and 1M to 11M in order of ascending significance. Each order shifts its contents to the next higher order when a shift pulse is applied and order 11M shifts its contents to order 1A. Recall that all input numbers are entered to orders 1A–10A and that all result data are delivered from these orders. An input-output (I-O) chassis associated with each of these accumulator orders 1A to 10A serves to translate input digits for entry to the accumulator and to translate output digits for transfer to result storage. A typical input-output chassis will be described with reference to Fig. 21.

INPUT-OUTPUT TRANSLATOR

The input translator portion of an I-O chassis comprises 8 stages, I9, I09, IA9, I79, C09, C17, I35, and C35. An input digit is received by the I-O chassis in the form of combinations of high and low potentials at terminals 9, 15, 23, 25, and 31. These terminals correspond respectively to the 7, 9, 1, 3, and 5 positions of the "Powers" or "90 column" code. Translated pulse sequences representing the input digit are delivered to the associated accumulator order from terminals 3 and 21. Terminal 3 delivers the single valued pulses to the binary input terminal of the associated accumulator order and terminal 21 delivers the double valued pulses to the quinary input terminal of the associated accumulator order.

Fig. 52 shows in tabular form the requirements met by the input translator portion of the I-O chassis. It is seen for example that the digit 6 will arrive at the I-O chassis (from one of the storages) as raised potential on the 5 and 9 input lines (terminals 31 and 15) and that in the accumulator the digit 6 will be represented simply as 6 (T6 on, all other triggers off). It is seen further that the digit 6 will be delivered from the input translator to the accumulator order as two single valued pulses over the binary or odd input line and two double valued pulses over the quinary or even input line.

The pulses delivered over the binary and quinary inputs to the accumulator orders are all derived from standard pulses over six lines from the Registration Impulse Generator (RIG) later to be described. Fig. 51 shows the pulses generated on these six lines and their designations RIG1', 2, 4, 6, 8, and 1. These six pulse sequences are applied to the I-O chassis at terminals 13, 27, 29, 11, 7, and 5 respectively, and are selectively gated to the binary and quinary translator output terminals 3 and 21 by the translator stages in accordance with the value of the input digit manifested by the combination of raised potentials at terminals 9, 15, 23, 25, and 31, in a manner now to be described.

The input translator and its operation can best be understood by considering the individual translating requirements and how each one is met. Reference to the table of Fig. 52 shows that RIG1' must be passed (gated out to the binary line) whenever the 9 input line (terminal 15) is high. This gating function is performed by the right half of gate I79 whose right plate is connected to the binary line (terminal 3). The right capacitive input to I79 is connected to the RIG1' input line (terminal 13) and the right bias to I79 is coupled to the 9 input (terminal 15) through a divider so that the RIG1' pulse will be gated out to terminal 3 when the 9 input is high and not otherwise. The bias potential is prevented from rising above about −15 volts by the right side of clamping

diode stage C09, the cathode of which is connected to −15 volts.

Further reference to the table of Fig. 52 shows that the RIG1 pulse must be passed for every digit except 9, or in other words whenever the 1, 3, 5, or 7 input lines (terminals 23, 25, 31, or 9 respectively) are high. To this end the RIG1 input line (terminal 5) is connected to the left capacitive input to positive pulse amplifier I09, the plate of which is connected to the binary output terminal 3. Thus, the RIG1 pulse will be gated to the binary output line except when the left bias input to I09 is low. This bias input is connected to the cathodes of buffer diode stages C17 and C35, the four plates of which are coupled respectively with the 1, 7, 3, and 5 input lines (terimnals 23, 9, 25, and 31). Thus, whenever any of these input lines is high, the common cathode potential of stages C17 and C35, and consequently the bias potential on the left side of amplifier I09 is raised to cause the RIG1 pulse to be passed. When the input digit is a 9, none of the 1, 3, 5 or 7 input lines is high and consequently the RIG1 pulse is blocked.

Having considered how the RIG1 and 1' pulses are gated to the binary output line in accordance with the requirements of Fig. 52, consider now how the RIG2, 4, 6 and 8 pulses are gated to the quinary output line. Note that the RIG2 pulse must be passed whenever the 3 input line (terminal 25) is high. This gating function is performed by the left side of gate I35, the plate of which is connected to the quinary output line (terminal 21). The RIG2 input line is connected to the left capacitive input to I35 and the 3 input line (terminal 25) is connected to the left bias input to I35. Thus, when the 3 input line is high, the left side of I35 delivers RIG2 pulses to the quinary output line. The bias potential is prevented from exceeding about −15 volts by the left sides of clamping diode stage C09 through the left side of diode buffer stage C35.

The RIG4 pulses must be passed whenever the 5 input line (terminal 31) is high (see Fig. 52). This gating function is performed by the right side of gate I35 in the same manner as described above for the left side. Here the RIG4 pulses are delivered from the right plate of I35 to the quinary output terminal 21 whenever the I5 input line is high. Clamping here is performed by the right side of C09 through the left side of C35.

The RIG6 pulses must be passed whenever the 7 input line (terminal 9) is high. This gating function is performed, in the same way as described above, by the left side of gate I79, the plate of which is connected to the quinary output line. Clamping of the left bias on I79 is performed by the left side of diode clamping stage C09 through the left side of diode buffer stage C17.

The RIG8 pulses must be passed only when the 9 input line is high and all other input lines 1, 3, 5 and 7 (terminals 23, 25, 31, and 9 respectively) are low. This gating function is performed by the right side of positive pulse amplifier I09, the right plate of which is connected to the quinary output line (terminal 21) acting in conjunction with stage IA9 and stage I9. The right bias input to I09 is coupled with the 9 input line (terminal 15) and is prevented from exceeding −15 volts by the right side of clamping diode stage C09. Thus, the right side of I09 is enabled to respond to a positive pulse input over its capacitive input line whenever the 9 input line is high. Stages I9 and IA9 serve to deliver such a positive pulse only when none of the 1, 3, 5, or 7 input lines are high. To accomplish this selectivity the cathodes of buffer diode stage C17 and C35 are connected in common to the left grid of IA9 so that the left side of IA9 will conduct when any of the 1, 3, 5 or 7 lines is high but not otherwise. Therefore when none of these lines is high, the left plate of IA9 is high. The potential at the left plate of IA9 is prevented from rising above about −15 volts by the right side of IA9 which is connected as a clamping diode (grid and plate jumpered). The left plate potential of IA9 is coupled to the left bias input to positive pulse amplifier IA9 and the left capacitive input to I9 (actually located in stage IA9) is connected to the RIG8 input line (terminal 7). Thus, the RIG8 pulses cause conduction in the left side of I9 only when that side is enabled by low potentials on all of the 1, 3, 5, and 7 input lines. The resulting positive pulse is inverted and amplified in the right side of I9 and delivered from the right plate of I9 to the right capacitive input to I09, where it is either passed or blocked depending upon whether the bias input (from the 9 input line) is either high or low.

Summarizing the gating of the RIG8 pulses, they are applied to the right side of I09 only when none of the 1, 3, 5, or 7 input lines is high and are passed by the right side of I09 only when the 9 input line is high. The requirement shown in Fig. 52 is thus seen to be met.

The foregoing has described how input digits from the various storage switches are translated from static potentials in the "Powers" or "90 column" code to bi-quinary pulse sequences to actuate the accumulator orders. Recall that there are 10 I-O chassis, each one associated with one of the accumulator chassis IA to 10A. Before considering the details of the storage switches, consider first the output portion of the I-O chassis.

OUTPUT TRANSLATOR

The output portion of the I-O chassis comprises 9 stages ME, MO, MA9, M9, M17, M57, M35, M13, and MφC. These stages receive static potentials from the trigger stages of the bi-quinary counter in an associated accumulator chassis and translate these static potentials to static potentials in the "Powers" code for delivery to result storage. The static potentials from the accumulator arrive at terminals 2, 4, 12, 14, 16, 28, 32, and 36 which are connected to accumulator chassis terminals 11, 13, 23, 25, 27, 39, 43, and 47 respectively.

The following table shows, for each of the digits 0 to 9 registered in the accumulator order, which input terminals to the output translator will be raised in potential.

Digit Registered	Input Terminal to Output Translator (x indicates raised potential)							
	2	4	12	14	16	28	32	36
0	x				x	x	x	x
1		x			x	x	x	x
2	x		x		x		x	x
3		x	x		x		x	x
4	x		x		x	x	x	
5		x	x		x	x	x	
6	x		x		x	x		x
7		x	x		x	x		x
8	x		x	x		x	x	x
9		x	x	x		x	x	x

Terminal 2, above, is connected to the common grid connection to cathode follower ME so that when an even digit is registered in the associated accumulator order, the cathode output of ME will be raised, thus inhibiting conduction in stages M17 and M35 to the cathodes of which the cathode of ME is connected.

Terminal 4 is connected to the common grid connection to cathode follower MO so that when an odd digit is registered, the cathode output of MO will be raised, thus inhibiting conduction in stages MA9, M57, and M13 to the cathodes of which the cathode of MO is connected.

The translated output potentials corresponding to the 1, 3, 5, 7 and 9 positions of the "90 column" code appear at I-O chassis terminals 22, 30, 34, 26, and 18 respectively. Each of these terminals is at low potential when the digit zero is translated and various ones of the terminals are raised in potential when other digits are translated. The operation of the translator is shown in the

table of Fig. 53. The 1 output line (terminal 22) is coupled to the right plate of stage M17 and the left plate of stage M13, so that the 1 output line will be raised only when conduction is cut-off in both the right side of M17 and the left side of M13. The right grid of M17 is connected (through terminal 12) to the right plate of trigger Tφ in the associated accumulator chassis so that conduction will be cut-off in the right side of M17 whenever the trigger Tφ is on (when the digits 0 and 1 are registered). The left grid of M13 is connected (through terminal 28) to the right plate of trigger T2 in the associated accumulator chassis so that conduction in the left side of M13 will be inhibited whenever the trigger T2 is on (when the digits 2 and 3 are registered). Thus it is seen that conduction will be cut off in both the right side of M17 and the left side of M13 only when either of the digits 1 or 2 are registered. When 0 is registered the left side of M13 will conduct and when 3 is registered the right side of M17 will conduct. Consequently the 1 output line (terminal 22) will be raised only when a 1 or a 2 is registered in the accumulator order.

In a similar manner the 3 output line (terminal 30) is raised only when the digits 3 or 4 are registered. This is accomplished by the left side of M35 and the right side of M13. In the same way the left side of M57 and the right side of M35 cooperate to raise the 5 output line (terminal 34) when the digits 5 or 6 are registered, and the left side of M17 and the right side of M57 cooperate to raise the 7 output line (terminal 26) when the digits 7 or 8 are registered.

The 9 output line (terminal 18) is raised when any even digit except zero is registered and also when a 9 is registered (triggers T1 and T8 on). This is accomplished as follows: The 9 output line (terminal 18) is even digit except zero is registered and also when a 9 line will be raised when conduction is cut off in the left side of M9. Conduction in the left side of M9 is cut off by lowering the grid potential whenever any of the digits 2, 4, 6, 8, or 9 are registered. This lowering of left grid potential on M9 is accomplished by the left side of MA9 and the right side of M9. The left side of MA9 conducts when any even digit except zero is registered (since its grid is coupled to the right plate of trigger Tφ and its cathode is coupled to the cathode of MO) and the right side of M9 conducts whenever the digits 8 or 9 are registered (since its grid is coupled with the left plate of trigger T8). Thus, the left side of M9 is cut off when any of the digits 2, 4, 6, 8 or 9 is registered, and thereby raises the potential on the 9 output line (terminal 18).

The table of Fig. 53 shows all significant conditions of high and low potential at various points in the output translator as each of the digits 0–9 is translated. Recall that an output translator identical to the one described in the foregoing is associated with each of the accumulator orders 1A to 10A. (See Figs. 2 and 3.) The output potentials (in the "90 column" code) from the output translator are connected to transfer busses which serve to selectively energize the storage relays of the result storage chassis now to be described.

RESULT STORAGE

Forty result storage chassis (see Fig. 2) each capable of storing two digits afford a result storage capacity of 80 digits or 8, 10 digit numbers. The 8, 10 digit storage locations are designated P, Q, R, S, T, V, W, and Y respectively. A typical storage chassis (with 2 digit capacity) is shown schematically in Fig. 31. Five relays R1, R3, R5, R7, and R9 serve as basic storage elements for the 1, 3, 5, 7, and 9 positions of the "90 column" code. One side of each of the relay windings is connected in common to a +300 volt supply line via terminal 34. The other sides of each of the windings are connected to the plate of an associated actuating triode S1, S3, S5, S7, or S9. The cathodes of these triodes are connected in common to terminal 36 and the grids are connected to the 1, 3, 5, 7, and 9 output lines from the output translator via storage chassis terminals 31, 25, 19, 13, and 7. Each of the ten output translators feeds eight storage digit locations in parallel; e.g. the output translator associated with column 4 (accumulator chassis 4) feeds the grids of the relay actuating triodes in all eight storage locations associated with column 4. (See Fig. 2.) Thus the grids of all relay actuating triodes constantly reflect the digit then registered in the associated accumulator order; e.g. whenever accumulator order 4A registered, say, 7, then the 7 input line (terminal 12 or 13) to each of the eight column 4 storage chassis will be raised in potential. This raising of grid potential alone does not, however, cause actuation of the associated relays R7 since the cathodes of all relay actuating triodes S1, S3, S5, S7 and S9 are normally held at a potential sufficiently high to prevent conduction. When it is desired to store a result number in one of the eight result storage locations P, Q, R, S, T, V, W, or Y, the cathodes of all relay actuating triodes (5×10 or 50 triodes) associated with that location are momentarily lowered so that conduction occurs in those triodes whose grids were high. Conduction in an actuating triode causes the associated relay to be actuated and its contacts to be closed. One pair of contacts H on each relay are holding contacts which effectively shunt the triode and cause the relay to remain actuated independently of conduction in the associated triode. A second pair of contacts P deliver energizing potentials to punch magnets 1, 3, 5, 7 and 9 via terminals 27, 21, 15, 9, and 3 or 28, 22, 16, 10, and 4 respectively. One side of all contact pairs P is connected to a common source of energizing potential through terminal 2.

A third set of contacts I serve to selectively energize input lines 1, 3, 5, 7, and 9 to the input translator via terminals 29, 23, 17, 11, and 5, or 30, 24, 18, 12, and 6 respectively. One side of each of the contact pairs I is connected to a source of energizing potential at terminal 1 through an indicating neon diode. The potentials representative of a result digit are therefore delivered to the input translator only when a selecting potential is applied at terminal 1. The terminals 1 of all storage chassis associated with one of the eight result storage locations P, Q, R, S, T, V, W, and Y are connected in common so that all digits stored in a given result storage location are transferred in parallel to the input translator. The manner in which particular storage locations are selected will be explained later in connection with the Keyboard Bias chassis. First the other two data sources, card sensing storage and constant storage, will be described.

CARD SENSING STORAGE

All 90 card columns are sensed simultaneously by 540 (6×90) sensing pins each of which closes a switch if its associated hole position is punched. The switches which are closed when a card is sensed remain closed until all calculations related to that card are completed. Thus the sensing switches serve as storage for the data sensed. The 6 sensing switches (φ, 1, 3, 5, 7, and 9) associated with each of the 90 card columns and the punch magnets associated with each column are connected to a "card column cable" terminating in a 14 prong plug as shown in Fig. 49. Five prongs are connected to one side of the 1, 3, 5, 7, and 9 sensing switches respectively and the other sides of these switches are connected in common through a sensing jumper board and a common line C to a sixth prong. When the common line is energized the digit stored in the associated sensing switches appears as static potentials on the 1, 3, 5, 7, and 9 lines. A seventh prong is connected to one side of a zero sensing switch the other side of which is connected to an eighth prong. When the seventh prong is energized, the presence or absence of a hole in the

zero position is thus manifested as a static potential at the seventh prong. The other six prongs are connected to the ϕ, 1, 3, 5, 7, and 9 punch magnets which are selectively energized to control the punching of a card when it reaches the punching station after having been sensed.

Recall that one of the above described card column cables is provided for each of the 90 card columns. Data are transferred from the card sensing switches to the input translator and from the output translator to the punch magnets via the 14 prong plugs at the end of each card column cable. Each of these plugs is adapted to be inserted into any one of 127, 14 hole sockets provided in the card punching unit. The 90 card column plugs and 127 sockets are provided to permit flexibility in reading, punching, and reproducing data. 57 of the 127 sockets are designated calculator input sockets and are connected through input buffers to the input portions of the 10 Input-Output chassis. These 57 sockets are divided into two groups of 10 sockets (storage locations A and B of ten digits each), two groups of 8 sockets (storage locations C and D of eight digits each), two groups of six sockets (storage locations E and F of six digits each), two groups of four sockets (storage locations G and H of four digits each) and one socket (storage location I of one digit). Any one of these groups of sockets corresponding to a given input storage location A, B, C, D, E, F, G, H, or I, may be energized through the keyboard bias chassis, later to be described, so that the digits from the card column cables plugged into them will be transmitted to the input terminals of the input translator. Input sockets A and B of ten digits each are connected to feed all ten of the I-O chassis in parallel. Input sockets C and D of eight digits each are connected to feed I-O chassis 2 through 9. Input sockets E and F of six digits each are connected to feed I-O chassis 3 through 9. Input sockets G and H of four digits each are connected to feed I-O chassis 4 through 7, and input socket I of one digit is connected to feed I-O chassis 5.

The connections between the input sockets and the input buffers to the input translator tie the 1, 3, 5, 7 and 9 lines from a column cable plug to the 1, 3, 5, 7, and 9 inputs to the input translator via an input buffer later to be described. The socket hole receiving the common 1, 3, 5, 7, and 9 line is connected to an appropriate keyboard bias line which serves to selectively energize the sensing switches for the column whose column cable is plugged into the socket.

Normally, only a portion of the calculator input sockets would be plugged during a particular calculating run. Assume, for example, that a run involves the multiplication of a four digit number in card columns 6-9 by a ten digit number in columns 70–79. In this case the four digit number will be manifested over the card column cables associated with columns 6–9 and the ten digit number will be manifested over those associated with columns 70–79. Card column cables 70–79 must be plugged into the input sockets of either storage locations A or B since they alone have 10 digit capacity. Cables 6–9 may be plugged into the input sockets for any of the storage locations except I since H alone has less than a four digit capacity. Assume the four digit factor is plugged into location G and the ten digit factor is plugged into location A. Then whenever the processing program calls for the transfer of either of these numbers to the accumulator, the appropriate "keyboard bias" (A or G) will be raised to enable the transfer.

Eighty output sockets corresponding to the 80 digits of result storage capacity (10 digits each in storage locations P, Q, R, S, T, V, W, and Y) are also provided for delivery result numbers to the punch magnets associated with any desired card columns. Five holes of each of these output sockets are connected with the 1, 3, 5, 7, and 9 output lines of associated storage chassis. If, for example, a ten digit result to be stored in output storage location W is to be punched in card columns 55–64, then the card column cables for columns 55–64 are plugged into the ten output sockets for storage location W. This effectively connects the 1, 3, 5, 7, and 9 outputs from the storage chassis to corresponding 1, 3, 5, 7, and 9 punch magnets for the desired columns 55–64.

In addition to the input and output sockets described above, 90 "reproduce" sockets are provided. When it is desired to reproduce data from any columns in a card to any other columns, the card column cables associated with the columns from which the data are to be taken are plugged into the reproduce sockets associated with the columns into which it is desired to reproduce the data. This effectively connects the ϕ, 1, 3, 5, 7, and 9 sensing switch outputs from the card column cable with the ϕ 1, 3, 5, 7, and 9 punch magnets of the other column.

CONSTANT STORAGE

120 rotary switches shown in Fig. 46 are provided for the storage of 120 digits of constants to be used in calculations. These switches are grouped to afford 20 storage locations of various lengths each of which may be selectively energized by the keyboard bias chassis. All 12 switches in each of the 10 vertical columns are associated with a different storage location but feed the input translator portion of the same I-O chassis (1 to 10).

All ten switches in the first horizontal row constitute storage location K1; likewise, all ten switches in each of the second, third, and fourth rows constitute respectively the storage locations L1, M1 and N1. Locations K2, L2, M2, and N2 comprise the first four switches in the fifth, sixth, seventh, and eighth rows respectively. The last six switches in each of these rows constitute storage locations K4, L4, M4 and N4. The first six switches in the last four rows constitute locations K3, L3, M3, and N3 and the last four switches in the last four rows constitute locations K5, L5, M5 and N5.

All switches associated with a particular storage location have a common connection to the rotary contact and the five stationary output contacts on each switch in a vertical column are connected respectively to the 1, 3, 5, 7, and 9 inputs to the input translator portion of the associated I-O chassis.

Thus the switch settings serve to store numbers but are ineffective to transfer the stored digits to the accumulator (via the input translator) except when the keyboard bias of a particular storage location is energized.

INPUT BUFFERS

Recall that many storage digit locations feed data (as static potentials over 1, 3, 5, 7, and 9 input lines) to the input translator associated with each of the 10 accumulator orders. For example, the input translator for column 4 (accumulator order 4A) receives digits from any one of the column 4 digit storages in card sensing, constant, and result storage locations A, B, C, D, E, F, G, H, K1, L1, M1, N1, K4, L4, M4, N4, K5, L5, M5, N5, P, Q, R, S, T, V, W, and Y. The particular one of these stored digits fed to the column 4 input translator is determined by the keyboard bias circuits later to be described. Neon diodes are used as buffers to isolate the various storages feeding a common input translator and prevent undesired energization of an otherwise unenergized storage through its closed contacts when another storage location is regularly energized. Fig. 57 shows the buffer diodes isolating four typical digit storage feeding the column 4 input translator. The digit storages shown are the column 4 storage switches of storage locations A, B, K1, and S. The A and B switches are card sensing storage switches, the K switches are constant storage switches and the S switches are result storage switches. One side of each of the card sensing switches is con-

nected to the positive side of an associated neon diode, the negative side of which is connected to the associated **1, 3, 5, 7,** or **9** input to the column 4 input translator. The other sides of the card sensing switches are connected in common to the keyboard bias circuits for the particular storage location. When a program step calls for the transfer of a number from, say, storage location A to the accumulator, the KB(A) circuit raises the potential at the common side of all digit switches in location A and current flows through any closed contacts and related diodes to raise the appropriate input lines to the input translator. The neon diodes associated with other storage locations prevent the raised potential on any input bus from erroneously energizing another bus.

A separate diode is provided for each card sensing switch since it is possible for all switches to be closed simultaneously if all hole positions in a card column are punched. Only two diodes are provided for each set of constant and result storage switches, one serving the **1, 3, 5,** and **7** switches and the other serving the **9** switch since there only one of the **1, 3, 5,** and **7** switches can be closed at any given time, and consequently the current capacity of a single diode will never be exceeded.

It should be noted that while only four typical sets of digit storage switches are shown feeding the input translator for column 4 in Fig. 75, 24 other sets of switches in the storage locations listed earlier also feed this input translator and are connected in the same way through their own neon diodes.

The description thus far has covered the accumulator, the input and output translators, the three types of data storage (card sensing, constant, and result) and the buffer circuits coupling the data storages with the input translators. It has been explained that data from any of the storage locations is transferred to the accumulator via the input buffers and translators by selectively energizing the common switch connection of the desired storage location. The Keyboard Bias circuits which perform this selective energization will now be described.

KEYBOARD BIAS

Each of the 37 storage locations A through Y has associated with it a keyboard bias circuit comprising a cathode follower and a D.C. amplifier as shown in Figs. 55 and 56. Referring for example to Fig. 56, the cathode of the cathode follower KB(B) is connected to the common side of all switches in the 10 digits of card sensing storage location B so that when the cathode follower conducts the common connection to the switches will be raised in potential to deliver the 10 digit number in storage location B to the 10 input translators in parallel. The cathode follower KB(B) is in turn controlled by D.C. amplifier KBA(B) the plate of which is connected to the grid of KB(B) so that when conduction is cut off in KBA(B), the output of cathode follower KB(B) will be raised. The grid of KBA(B) is coupled, through a neon diode limiter and a voltage dividing network, to the "B" output from the control plugboard so that when the "B" output is lowered, conduction in KBA(B) will be cut off and the output of KB(B) raised. The manner in which the "B" output of the control plugboard is lowered to select storage location B will be described later.

Fig. 55 shows the same type keyboard bias circuit associated with a typical constant storage location. The same circuit is also used for result storage location selection. All of the keyboard bias circuits for the 37 storage locations are contained in four chassis KB(**1**), (**2**), (**3**) and (**4**). A typical chassis, KB(**1**), is shown schematically in Fig. 43. As is shown there, a cathode follower, e.g. KB(A), comprising an entire stage, is provided for each storage location. Each D.C. amplifier, e.g. KBA(AB) serves two storage locations and controls two cathode followers. The relation between the terminals of each of the four KB chassis and the various storage locations is set forth in the following table:

Input from Plugboard to Terminal	Output To Common Storage Switch Connection From Terminal	KB (1)	KB (2)	KB (3)	KB (4)
33	34	A	K1	M1	P
31	32	B	K2	M2	Q
29	30	C	K3	M3	R
27	28	D	K4	M4	S
21	22	E	K5	M5	T
19	20	F	L1	N1	V
17	18	G	L2	N2	W
15	16	H	L3	N3	Y
9	10	J	L4	N4	
7	8		L5	N5	

DECIMAL SWITCHES

A four deck twelve position rotary switch of the kind shown in Figs. 54*a* and 54*c* is provided for each of the 37 storage locations. The settings of these "decimal" switches establish the location of decimal points for each storage location and deliver combinations of static potentials representative of the location of the decimal point to the decimal counter (DCR) chassis (Fig. 20). The rotary contacts of each deck of a decimal switch are connected in common to the keyboard bias output for the associated storage location so that the rotary contacts will be raised in potential whenever the storage location is selected for data transfer. Nine lines designated **16, 8, 4, 2, 1, 16′, 8′, 4′,** and **2′** are connected through neon diodes to various stationary contacts which cooperate with the five rotary contacts. These nine lines deliver simultaneously to the DCR both the true and complementary representations of a number which specifies the decimal point location for which the switch is set.

Decimal locations are specified with reference to a reference position located between accumulator orders **6M** and **5M**. Thus, when a decimal switch is set to the right of column 10 (accumulator order **10A**) as shown in Fig. 54*c*, the decimal location is specified by the true value 6 or the 22's complement 16. As is seen from the table of Fig. 54*b*, these values are transferred from the decimal switch to the decimal counter as raised potentials on the **4** and **2** lines for the true value and as a raised potential on the **16′** line for the complement. When the switch of Fig. 54*c* is turned one position clockwise to locate the decimal point between accumulator orders **10A** and **9A**, the second line of the table of Fig. 54*b* applies, and so on.

The decimal location signals delivered from the decimal switches are employed in the Decimal Counter to control accumulator shifting in a manner to be explained later.

SIGN SWITCHES

The calculator is designed to handle both positive and negative numbers in any of the 37 storage locations. A switch associated with each storage location specifies whether the number in that location is positive or negative. When the number is positive the switch is open and when the number is negative the switch is closed. One side of each switch is connected to the associated keyboard bias line as shown in Fig. 50 so that the switch will be energized (raised in potential) only when the corresponding storage location is selected for data transfer. The other sides of all sign switches are connected through neon diodes to a common line called the minus neon common line. Thus, whenever a positive number is being transferred to the accumulator the minus neon common line will be at low potential and whenever a negative number is being transferred the line will be at a raised potential. The minus neon common line is connected to terminal **18** of the Zero Factor (ϕF) chassis and performs control functions explained later.

The sign switches for all constant storages (K to N) are located next to the constant digit switches as shown

in Fig. 46, and are manually set to specify whether a constant is positive or negative.

The sign switches for all result storages (P to Y) are, in fact, relay contacts on sign relays located in the Storage Set (STS) chassis. (See Fig. 32.) These relays are actuated by other parts of the control unit in accordance with the signs of the numbers entering into a calculating step in a manner explained later.

The sign switches for card sensing storage locations are somewhat differently organized and require a more extensive explanation. A number punched in any card field may be identified as positive or negative in a variety of ways. A common way would be to punch the zero position of the first digit if the number is negative. Any other position in the entire card might, however, be used to identify a particular number as positive or negative. For this reason, provision is made for selectively using any of the 540 card sensing switches to specify the sign of a number stored in any of the 9 card sensing storage locations. A pair of leads terminated in a two prong plug is provided for each of the nine card sensing storage locations A to J. One of these leads in each pair is connected to the associated keyboard bias line and the other is connected through a neon diode to the minus neon common line. Thus, by plugging the two prong plug to connect the two prongs with the two contacts of one of the 540 sensing switches, that particular sensing switch will be effective to specify the sign of the number in the storage location, just as the manual switches associated with the constant storage locations do. These leads and sockets are located in the card sensing and punching unit and, when plugged, are equivalent in every respect to the result sign arrangement shown in Fig. 50. If any pair of leads is not plugged, the number in its associated storage location will always be treated as positive since the raised keyboard bias potential on one lead cannot be transmitted to the other lead which feeds the minus neon common line.

Thus far, the accumulator, data storages, and translators have been described and it has been explained how data from the various storage locations are transferred to the accumulator. Recall that pulse sequences over six lines are delivered to each input translator whenever a number is to be transferred to the accumulator. These pulse sequences, shown in Fig. 51, are generated by the Registration Impulse Generator (RIG) chassis which will scribed have been shown schematically in the drawings, the RIG chassis and other chassis later to be described are shown in the block schematic notation which was defined in an earlier part of the specification. The following description and explanation of the RIG chassis will serve as a practical introduction to the block schematic notation.

REGISTRATION IMPULSE GENERATOR

Referring now to Fig. 27 the Registration Impulse Generator (RIG) chassis comprises 19 stages. Three stages, RD, RS, and CD are flip-flops (sometimes called univibrators). One stage, R8, is a multivibrator. Three stages, R1, R2, and R4 are bi-stable triggers. Six stages, R11, R1'1', R88, R66, R44, and R22 are cathode followers. Three stages, CDA, R1'8, and R42 are double negative pulse amplifiers and the right half of another stage R1M is a negative pulse amplifier. The left half of R1M is a D.C. amplifier. One stage I1–11 is a double gating amplifier and the remaining stage PX is a diode buffer.

The RIG cycle is initiated by a negative pulse applied at terminal 8 or by a negative pulse applied at terminal 18. Each time a negative pulse is applied at either of these terminals an RIG cycle commences and the six RIG pulse sequences (1', 2, 4, 6, 8, 1) shown in Fig. 51, are generated at terminals 19, 35, 31, 27, 23, and 15 respectively. (These terminals, it will be recalled, are connected to input terminals 13, 27, 29, 11, 7, and 5 respectively of each of the ten input translators.) The RIG pulses (positive pulses) are delivered to these terminals from the cathodes of cathode followers R1'1', R22, R44, R66, R88, and R11 respectively. The structure and the operations which produce the RIG pulses can best be described concurrently.

A negative pulse arrives at terminal 8 from the Sign Bias (SB) chassis each time the accumulator orders are selectively conditioned to add and/or subtract. This negative pulse is applied to the right plate of flip-flop RD and actuates RD. This causes the left plate of RD to rise (when RD is conducting on the right) and then fall (when conduction returns to normal, on the left). The left plate of RD is connected to the right capacitive input to another flip-flop, RS, that RS is actuated by the negative swing when RD returns left. (The positive swing when RD is initially actuated does not affect RS since it merely causes a positive pulse on the grid that is already positive. In this and following descriptions only significant pulses and static potentials will be referred to. Lack of references to a pulse or static potential may be taken to mean that no significant effect is produced.) The negative pulse developed at the right plate of RS is amplified and inverted by the left side of negative pulse amplifier R1'8 and the resulting positive pulse is fed to the RIG1' output (terminal 19) through cathode follower R1'1'. A short time later (determined by the time constant of flip-flop RS), the negative pulse developed at the left plate of RS turns on trigger R–1 through its right capacitive input. The drop in potential at the right plate of R–1 is inverted in the left side of R1M to energize multivibrator R8. R8 will thus continue to operate until trigger R–1 is turned off. Only negative swings of the two multivibrator outputs are significant since the right output is connected to the capacitive input of a negative pulse amplifier (right side of R1'8) and the left output is connected to the common capacitive inputs to trigger R–4. The first negative swing of the right output from R8 is inverted and amplified by the right side of R1'8 and the resulting positive pulse is delivered to the RIG8 output (terminal 23) through cathode follower R88. This is the first of the four RIG8 pulses.

The negative swing of the left output from R8 then turns trigger R4 on (since R4 was initially off). The resulting negative swing at the right plate of R4 is inverted and amplified in the left side of R42 and delivered to the RIG4 and RIG6 output (terminals 31 and 27 respectively) as positive pulses through cathode followers R22 and R66 respectively. These are the first of the RIG4 and RIG6 pulses.

The negative swing of the right output of multivibrator R8 then delivers another pulse to the RIG8 output (terminal 23) through the left side of R1'8 and cathode follower R88. This is the second of the four RIG8 pulses shown in Fig. 51.

Next the negative swing of the left output of R8 turns trigger R4 off and the negative swing at the left plate of R4 turns R2 on (R2 having been off initially). The resulting negative swing at the right plate of R2 is amplified and inverted in the right side of R42 and delivered to the RIG2 and RIG6 outputs (terminals 35 and 27) through cathode followers R22 and R66. These pulses are the single RIG2 and the second RIG6 pulse shown in Fig. 51. Note in this connection that the grids of R22 are connected to the left grid of R66 and that the grids of R44 are connected to the right grid of R66 so that a RIG6 pulse will be developed whenever either a RIG2 or a RIG4 pulse is developed. This is in accordance with the timing shown in Fig. 51.

Next the negative swing of the right output of multivibrator R8 is again inverted in the right side of R1'8 (terminal 23) through cathode follower R88. This is the third of the four RIG8 pulses.

When R8 goes left again, the negative swing at its left

plate turns R4 on again and the resulting negative swing at the right plate of R4 is inverted again in the left side of R42 and delivered to the RIG4 and RIG6 outputs (terminals 31 and 27) through cathode followers R44 and R66. These pulses are the last of the two RIG4 pulses and the last of the three RIG6 pulses.

Next the negative swing at the right plate of multivibrator R8 delivers the last of the four RIG8 pulses to the RIG8 output (terminal 23) through the right side of R'18 and cathode follower R88.

The next reversal in R8 causes a negative swing on its left plate and this turns off R4. The resulting negative swing at the left plate of R4 turns off R2 and the negative swing at the left plate of R2 does two things. It is inverted in the right side of R1M and delivered through cathode follower R11 to the RIG1 output (terminal 15) and it also turns off trigger R1 to stop the multivibrator R8 through D.C. amplifier in the left half of R1M. Thus, the RIG1 pulse which is the final pulse in the RIG sequence shown in Fig. 51 is delivered, the multivibrator R8 is stopped and the triggers R1, R2, and R4 are all off.

At the time trigger R1 is turned off to stop the multivibrator R8, the negative swing at the left plate of R1 actuates flip-flop CD which goes right and then returns left after a predetermined delay. The resulting negative swing at the left plate of CD is inverted and amplified in negative pulse amplifier CDA and delivered as a positive pulse to terminal 12. This pulse is referred to as the CX pulse and is seen to occur after each RIG cycle. It is used as a control signal in a manner later to be explained.

The time constants of the elements generating the complete RIG cycle are such that the time interval between the vertical dotted lines of Fig. 51 is 12.5 micro-seconds and the CX pulse occurs 25 micro-seconds after the RIG1 pulse. The time constant of flip-flop RD is such that 100 micro-seconds elapse between the initiating pulse over terminal 8 and the RIG1' pulse generated when RS returns left. Note, however, that when the RIG cycle is initiated by a pulse over terminal 18, the RIG1' pulse will occur immediately without the 100 micro-second delay, since terminal 18 is connected directly to the left capacitive input to negative pulse amplifier R1'8. The reason for this difference will be apparent later; it may be said here, however, that RIG initiating pulses at the beginning of a calculating step arrive over terminal 8 while subsequent RIG initiating pulses for repeated registrations during multiplication and division arrive over terminal 18.

Only two stages contained in the RIG chassis remain to be described. These are diode stage PX and double gate stage I1–11. These stages jointly perform the function of delivering, for each RIG cycle, a single pulse to the binary input line to accumulator order 11M during multiplication and to accumulator order 1M during division. To this end, the right and left capacitive inputs to gate I1–11 are connected to the RIG1' output line (terminal 19) so that the RIG1' pulse (positive) of each RIG cycle will be applied to both gates comprising I1–11. The right gate will be open only when its control line (terminal 18) is raised in potential. When this occurs (under control of the MD chassis) the RIG1' pulse will be gated to accumulator order 11M. The left side of the gate I1–11 will be opened to gate the RIG1' pulse to order 1M when either of two input lines (terminals 16 or 20) are raised. These lines are connected to the two plates of diode PX and the cathodes of PX are connected in common to the left control input to gate I1–11. Of the two lines (terminals 16 and 20) that control the left half of I1–11, one is raised during the repeated subtraction in division and the other is raised during the restoration after overcarry. This will be further explained in connection with the Multiplication-Division (MD) chassis.

DECIMAL COUNTER CHASSIS

The Decimal Counter (DCR) chassis contains 46 stages as shown in Fig. 20. Eleven of these stages comprise a Carry Impulse Generator (CIG) and related circuits for producing carry pulses. These stages are not related to the Decimal Counter and will be described here only because they are physically located on this chassis. Nine other stages comprise a Shift Impulse Generator (SIG) and related circuits which produce shift pulses for shifting the accumulator contents. The remaining 26 stages comprise the Decimal Counter which controls the shifting of accumulator contents. The CIG, SIG, and DCR will now be described in that order.

CARRY IMPULSE GENERATOR

The carry call line is connected from the various accumulator orders (terminal 9) to terminal 43. Recall that this line swings positive whenever overflow occurs in any accumulator order. This may occur at any time during the RIG cycle. The increased potential is delivered from terminal 43 to the input to Schmitt trigger CB and causes conduction in CB to shift to the left. This effectively closes the left sides of gates CX and CS and opens the right side of gate CX, since the left plate of CB is connected to the left inputs to CX and CS and the right plate of CB is connected to the right input to CX. The common capacitive input to gate CX is connected to terminal 33 which receives the CX pulse from the RIG chassis after the completion of each RIG cycle. Thus, when the carry call line (terminal 43) is high, the CX pulse passes the right side of gate CX to turn trigger CT on. The negative pulse that turns CT on has no effect on the right side of CMA since that side of CMA is biased below cut off. The lowered potential at the right plate of trigger CT reduces conduction in the left side of CMA, however, and causes its left plate to rise. This rise is delivered to the input to multivibrator CM and starts CM.

The positive pulse at the left plate of CM is inverted and amplified in amplifier CA (and CA1 which is connected in parallel with CA) and delivered to CIG output terminal 41 which is connected to the carry input terminals (terminals 14) of each of the accumulator orders. When multivibrator CM returns left, the positive swing at its right plate is gated through the left side of gate CS to turn off trigger CT. The raised potential at the right plate of CT is inverted in the left side of CMA to turn off multivibrator CM and the positive swing at the right plate of CT is also inverted and amplified in the right side of CMA and delivered to terminal 31. This negative pulse at terminal 31 indicates that all carries have been satisfied. When no overflow occurs during the registration of a number, the CX pulse following the RIG cycle is gated through the left side of gate CX to terminal 31.

Stages CSK, SCK, and SCK1 are used in connection with the Test Counter (TCR) which will be described later.

SHIFT IMPULSE GENERATOR

The Shift Impulse Generator (SIG) generates shift pulses for shifting the accumulator contents. These pulses (positive pulses) are delivered from the DCR chassis over terminal 39 to the SIG inputs to all accumulator chassis.

The basic element of the SIG is the shift multivibrator SM. SM operates whenever its enabling potential (terminal 11) is raised. Successive positive swings of its right plate are transmitted to the SIG output line (terminal 39) through the left side of pulse amplifier SMG, the right side of pulse amplifier SMA, the left and right sides of gating and amplifier SG, AC cathode follower SK1, and cathode followers SK2 and SK3 (in parallel). These pulses from SM continue to pass through gate SG until

trigger DCC is turned on (when the decimal counter passes from 21 to 22). At that time the lowered potential at the right plate of DCC inhibits the left side of gate SG to prevent further shift pulses.

DECIMAL COUNTER

The decimal counter proper comprises trigger stages DC1, DC2, DC4, DC8, and DC16 each provided with a common capacitive input line so that a negative pulse over any input line will change the conduction state of the associated trigger. These triggers are initially set up to represent a decimal location by negative pulses from gates D11, D2–4C, D2–4T, D8–16C, and D8–16T. These pulses originate in a decimal registration generator comprising flip-flops DP1, DP2, DP4, DP8, and DP16 and are gated through the aforementioned gates in accordance with gating inputs from the decimal switches described earlier. The 1, 2, 4, 8, 16, 2′, 4′, 8′, and 16′ inputs from the decimal switches arrive respectively at terminals 1, 3, 5, 7, 9, 14, 16, 18, and 20. Combinations of high and low static potentials appear on these lines in accordance with the setting of the decimal switch whose keyboard bias line has been raised. These lines are connected to the enabling inputs to gates D11, D2–4C, D2–4T, D8–16C and D8–16T so that when, for example, the 16 or 16′ inputs from the decimal switches are raised in potential, the pulse from flip-flop DP16 (of the decimal registertation generator) will be enabled to pass through related gates D8–16T or D8–16C and actuate (change the state of) decimal counter trigger DC16. Note in connection with this example that the 16 input line (terminal 9) is connected to the enabling input to the left side of gate D8–16T and that the capacitive input to this side of D8–16T is connected to the left output from flip-flop DP16. Note further that the left output from D8–16T is connected to the common input to trigger DC16 so that when the 16 line is high and flip-flop DP16 is actuated, the positive pulse from the left plate of DP16 will be inverted and gated by the left side of D8–16T to reverse the state of DC16. This will occur, however, only if the cathode of gate D8–16T is sufficiently low to permit conduction; this cathode potential (as well as that of gate D2–4T) is controlled by the potential appearing at terminal 21. Terminal 21 receives a low potential from another chassis whenever the true (rather than complementary) value of the decimal switch setting is to be effective; this enables gates D8–16T and D2–4T which are associated with the true outputs from decimal switches. When a complementary value is to be effective, on the other hand, terminal 19 is lowered in potential to enable gates D8–16C and D2–4C which are associated with the complementary outputs from the decimal switches. The 1 signal gated by D11 is the same for both true and complement values and therefore D11 has no cathode enabling connection.

No decimal registration can occur until the decimal registration generator is actuated. Whenever a decimal registration is to take place, a negative pulse is delivered from another chassis (DCL) to terminal 37. This pulse actuates flip-flop DP1 to commence the decimal registration cycle. The positive pulses developed at the left plate flip-flops DP1, DP2, DP4, DP8, and DP16 when these flip-flops are actuated are delivered to the capacitive inputs the decimal gates as described above. The way in which the flip-flops are actuated in sequence is as follows: The negative pulse from the left plate of DP1 when DP1 returns left is delivered to terminal 25 and from thereto the DCL chassis. Except under certain conditions later to be described the pulse going out at terminal 25 will be substantially immediately returned to terminal 23 to actuate flip-flop DP2. When DP2 returns left, the negative pulse at its left plate actuates DP4. DP8 and DP16 are similarly actuated by the negative pulses developed when DP4 and DP8 return left.

The decimal counter triggers receive actuating pulses from pulse amplifiers DB2, DB4, DB8 and DB16 as well as from the decimal registration generator described above. The left side of DB2 delivers an actuating pulse to trigger DC2 whenever trigger DC1 is turned off, and the right side of DB2 delivers an actuating pulse to DC2 whenever flip-flop DCCD returns left (the function of DCCD will be explained later). The left side of DB4 delivers an actuating pulse to trigger DC1 whenever a shift pulse is delivered to Shift Impulse Generator (SIG) output terminal 39, and the right side of DB4 delivers an actuating pulse to trigger DC4 whenever trigger DC2 is turned on. The left side of DB8 delivers an actuating pulse to trigger DC8 whenever trigger DC4 is turned off, and the right side of DB8 delivers an actuating pulse to trigger DC8 whenever trigger DCC is turned off (as will be explained later). The left side of DB16 delivers the 16 pulse from the decimal registration generator to actuate trigger DC16 whenever an enabling potential is raised at terminal 29 (from DCR), and the right side of DB16 delivers an actuating pulse to trigger DC16 whenever trigger DC8 is turned on.

Summarizing the interaction between triggers, DC2 turning on actuates DC4, DC8 turning on actuates DC16, DC4 turning off actuates DC8, and DC1 turning off actuates DC2. This interaction gives rise to the counter action shown in the table of Fig. 58. The table shows which triggers are on and off after each one of a sequence of 38 pulses applied to trigger DC1. Note that the counting sequence is such that if triggers DC2 and DC8 are regarded as manifesting negative values of 2 and 8 respectively when on, then the value registered by the counter at any time is equal to the algebraic sum of the digits manifested by the triggers that are on. For example, after the 13th pulse, triggers DC16, DC8, DC4, and DC1 are on; the value registered is, accordingly, 16−8+4+1 or 13.

The reason for the rather unusual counting arrangement is to facilitate the detection of the passage of the counter from a count of 21 to a count of 22 when shift pulses are being counted. It is necessary to detect this condition since the logic of the counter and related circuits is such that shifting must be stopped then. If the conventional binary counting arrangement were used the criteria for detection would be the change from the binary representation 10101 (for 21) to 10110 (for 22) in the decimal counter where the 1's and 0's represent the on and off conditions of triggers DC16, DC8, DC4, DC2, and DC1. Sensing this condition would obviously require a number of logical gates. In the counting arrangement used, however (Fig. 58), the change from 21 to 22 is positively identified by the turning off of trigger DC16. Thus no special sensing gates are needed and the signal can be taken directly from trigger DC16.

Recall that the decimal counter is actuated in two different ways; by shift pulses during shifting (SIG pulses to DC1) and by decimal registration generator pulses gated by decimal switch outputs during the preliminary decimal registration. The gating outputs of decimal switches for each of the twelve possible switch settings are shown in the table of Fig. 54*b*. Note, for example, that with the switch set to locate the decimal point between columns 7 and 8 the decimal location which is specified by the digit 9 (location is 9 columns to left of reference point between 5M and 6M) is delivered from the decimal switch as raised potentials on the 8, 1 (true), and 8′, 4′, and 1′ (complement) lines. Assuming the decimal counter is initially zeroized (all triggers off) and the true gates are open, consider how the decimal counter finally reaches the value 9 as shown in the table of Fig. 58. First the 1 pulse turns on trigger DC1. This has no effect on any of the other triggers. Next the 8 pulse turns on trigger DC8. This in turn turns on trigger DC16 in the manner explained earlier. The 2, 4, and 16 pulses from the decimal registration generator have

no effect on the counter triggers since the related gating inputs are low. Thus after the decimal registration generator completes its cycle, triggers DC16, DC8 and DC1 are on and triggers DC4 and DC2 are off. This is in agreement with the conduction pattern shown for the value 9 in Fig. 58. Other true or complementary values are registered from the decimal switches in a similar manner.

While the decimal counter is never actuated beyond the count of 22 by shift pulses (since it prevents further shifting after the count 22), it is often actuated beyond the count of 22 during decimal registration from the decimal switches. In an extreme case (as seen in Fig. 54*b*) a true value as high as 17 might be registered initially, followed by the registration of a complementary value as high as 16. The modulo 22 value of the sum of the two values registered is the significant value rather than the modulo 32 value that will be registered in accordance with the table of Fig. 58. That is, after the two decimals have been registered (those of an operator and an operand, as will be explained later) the decimal counter must register the modulo 22 value of their sum rather than the modulo 32 value as would normally be the case in a 5 stage counter such as the decimal counter is.

Modulo 22 values could be obtained by arranging the counter to zeroize itself when the trigger DC16 is turned off (indicating passage from 21 to 22). It is somewhat more economical of equipment in the present design, however, to permit the counter to continue counting modulo 32 as shown in Fig. 58, record the passage of the counter from 21 to 22 during registration if it occurs, and then correct the final registration from modulo 32 to modulo 22 after the decimal registration cycle is completed. This correction is easily accomplished merely by delivering an actuating pulse to triggers DC2 and DC8 after the decimal registration cycle whenever the registration caused the counter to exceed 21. If for example, registration left the counter reading 24 (DC8 on, all others off) pulsing DC8 will turn it off, pulsing DC2 will turn it on, and turning on DC2 will also turn on DC4 to change the modulo 22 value, 24 to its correct modulo 22 value, 2 (triggers DC2 and DC4 on, all others off).

The fact that the decimal counter has passed 21 during decimal registration is recorded by trigger DCC which is turned on whenever trigger D16 is turned off. The signals generated when DCC turns on do nothing. DCC is turned off, however, by the positive pulse from the right plate of flip-flop DP16 (following the 16 pulse at its left plate) which is inverted and amplified in the right side of DIC. The positive pulse at the right plate of DCC when DCC turns off actuates trigger DC8 through the right side of pulse amplifier DB8 and also actuates flip-flop DCCD through the right side of pulse amplifier SMG. The positive pulse at the right plate of DCCD when DCCD returns left actuates trigger DC2 through the right side of pulse amplifier DE2. Note that if registration does not cause the decimal counter to pass 21, trigger DCC will not be turned on and the actuating signals will not then be sent to triggers DC2 and DC8.

RESULT STORAGE SETTING AND CLEARING (STORAGE SET, STORAGE ZEROIZE AND REGULATOR CHASSIS)

The Storage Set and Storage Zeroize chassis jointly control the transfer of data to selected result storage locations and the clearing or zeroizing of selected result storage locations. Two identical Storage Set chassis (1 and 2) are provided, one (1) serving result storage locations P, Q, R and S, and the other (2) serving locations T, V, W and Y. These Storage Set chassis also contain the algebraic sign relays for the 8 result storage locations. The Storage Set (1) chassis is shown in detail in Fig. 32. One Storage Zeroize chassis, shown in Fig. 33 serves all 8 result storage locations. The Regulator chassis shown in Fig. 26 also cooperates with the Storage Set and Storage Zeroize chassis in setting and clearing the result storage locations. Eight stages SKP to SKY in the Regulator chassis are associated with the 8 result storage locations respectively.

The description of the Storage Set, Storage Zeroize, and Regulator circuits will be confined to those circuits associated with one storage location P since the circuits for the other locations are identical in structure and operation.

First, recall that in each of the forty storage chassis (see Fig. 31) one side of each storage relay is connected in common to +300 volts (at terminal 34). The other side of each relay is connected via two alternate paths (through the relay control tube or through the relay holding contacts) to terminal 36. Terminal 36 on each of the five Storage chassis in a particular result storage location are connected to the plate of an associated regulator stage. For example, terminals 36 on each of the five P storage chassis are connected to the plates of regulator stage SKP in the Regulator chassis via Regulator chassis terminal 13. The regulator stage normally maintains the potential across the relay-control tube circuits at 150 volts; i.e., maintains the potential at terminals 36 at +150 volts (+300 minus +150 equals 150). This potential is sufficient to hold in any relays (through their holding contacts) that have previously been actuated, but is insufficient to actuate a relay initially even if its control tube grid potential is raised by the output translator, since the grids are never raised above +110 volts.

When it is desired to transfer data from the accumulator (via the output translator) to storage location P it is necessary merely to reduce the potential at terminals 36 on the P storage chassis to a point below the +110 volts applied to selected control tube grids by the output translator. (This reduced potential may be, say, +75 volts.) This will cause the selected relays to be actuated. After actuation, the potential at terminals 36 may be reduced again to its normal value of +150 volts since this is sufficient to hold the actuated relays through their holding contacts.

When it is desired to clear or zeroize storage location P, it is necessary merely to raise the potential at terminals 36 to +300 volts (the potential to which the other sides of the relays are connected) so that the potential across the relay circuits is reduced to zero. This will reduce the holding current to zero and cause all relays that were actuated to drop out. As soon as drop-out has occurred, the potential at terminals 36 may be returned to its normal value of +150 volts since this is higher than control tube grid potential ever reaches and no actuation of relays can occur.

Summarizing, a regulator stage (e.g. SKP) associated with each result storage location (P–Y) directly controls the setting-up, holding, and clearing of its storage relays by lowering, maintaining or raising the potential at terminals 36 of the Storage chassis. The means by which the regulator stages (e.g. SKP) are controlled by the Storage Set and Storage Zeroize chassis will now be explained. Here again, the explanation will be confined to the circuits associated with result storage location P since those associated with the other seven locations (Q–Y) are identical. The Storage Zeroize chassis may be regarded as comprising eight identical sets of circuits (except, of course, for terminal numbers and stage designations) and each of the two Storage Set chassis may be regarded as comprising four identical sets of circuits.

The grids of regulator stage SKP are connected via Storage Set chassis terminal 28 to the left plate of stage MZ(1)A and the right plate of stage CAP(1). Both of these plates share a common plate resistor. Normally the right plate of CAP(1) does not conduct, since its grid is tied to −375 volts through a 1 megohm resistor,

but the left plate of MZ(DA) does conduct normally to maintain the grid of SKP at a potential that will hold its plate (and consequently terminals **36** of the P storage chassis) at +150 volts. The manner in which this regulation is obtained will be explained later. First, note that if conduction in the left side of MZ(1)A is reduced by pulsing its grid negatively, the grids of SKF will be raised, and the potential at terminals **36** of the P storage chassis will be lowered to actuate any selected relays. If, on the other hand, the right side of CAP(1) is caused to conduct by pulsing its right grid positively, the grids of SKF will be lowered, the potential at terminals **36** of the P storage chassis will be raised and any relays that were previously actuated will drop out. Thus, storage location P is "set" by pulsing the left grid of MZ(1)A negatively, or "cleared" by pulsing the right grid positively. Still neglecting for the moment the way in which regulation of the holding potential is achieved, consider the circuits that pulse the grids of MZ(1)A and CAP(1) to cause setting and clearing of P storage.

The left grid of MZ(1)A is pulsed negatively by the left plate of MS(P–Q) (through a dividing resistor located in MK(P) whenever the left side of MS(P–Q) conducts. Conduction in the left side of MS(P–Q) occurs only when the P Keyboard Bias line is raised (at chassis terminal **9**) and the cathode of MS(P–Q) is pulsed negatively by a storage set pulse (over chassis terminal **19**) from the Decimal Counter chassis. This pulse occurs whenever, during a program, it is desired to transfer data from the accumulator to one of the result storage locations, and it occurs only after the appropriate Keyboard Bias line has been raised.

When a storage location is to be cleared, the right input to CAP(1) is pulsed positively as explained earlier. This pulse arrives over chassis terminal **27** from terminal **12** (for P storage) of the Storage Zeroize chassis. The pulse is generated at the left plate of flip-flop MZ1 whenever MZ1 is actuated. MZ1 may be actuated to clear P Storage either as part of a program step or dividing the Clear output operation. When the clearing is part of a program step MZ1 is actuated through the left side of gate MZA. This gate is enabled by raised potential on the P Keyboard Bias line at terminal **13** and receives a positive pulse input via terminal **43** and cathode follower MZK from the Control chassis (right plate of EPG) each time it is desired to clear a result storage location. The pulse from EPG is applied to the gates (like the left side of MZA) for all eight result storage locations but is passed only by the one gate whose related Keyboard Bias line is raised. The negative pulse from the left plate of MZA is delivered to the right plate of MZ1 to actuate MZ1. Diodes in MCC prevent the grids of MZA from rising above about −15 volts. A capacitor between connections **4** and **7** of MCA is used merely to increase the time constant of flip-flop MZ1.

During a Clear output operation, MZ1 is not actuated by MZA since no Keyboard Bias line is raised. Instead, the storage locations to be cleared are designated by manually set switches associated with each storage location. The output from the P switch, for example, arrives at the Storage Zeroize chassis at terminal **8** which is connected through the right diode of MCA to the right input to MZ1. When the clear P switch is closed and a clear operation is called for, the potential at terminal **8** is lowered, but not lowered enough to cause conduction in the right diode of MCA and thus actuate MZ1. The ESI (advance step triggers) signal is delivered to terminal **17** of the Storage Zeroize chassis from the Step Control chassis. This signal is coupled through a capacitor in the left side of MCC (between connections **6** and **3**) to the cathode of the diode in the right side of MCA so that when the cathode is lowered by the clear P line (terminal **8**) the negative ES1 pulse will be sufficient to cause conduction in the diode and thus actuate flip-flop MZ1.

Summarizing the clearing operation, clearing of a particular result storage location during a program step is caused by the combination of raised keyboard bias and a positive pulse from EPG in the Control chassis; during a Clear operation, clearing is caused by the combination of a lowered potential on a clear selection switch line and the negative ES1 pulse from the Step Control chassis.

The preceding has explained how the grids of Regulator stage SKP (for example) are raised or lowered to set or clear result storage location P. It remains now to consider how the potential on these grids are regulated normally to maintain the holding potential across the relay circuits at 150 volts (i.e. to maintain the potential at terminals **36** of the result Storage chassis at +150 volts).

The right side of stage MK(P) is the basic regulator control stage. Its plate is connected through a resistor to the +300 relay supply potential, its cathode is connected to the cathodes of the storage relay control tubes and to the plates of regulator stage (SK(P), and its grid is connected to the left plate of MS(P–Q). Except when the left side of MS(P–Q) is conducting to set P storage, the right grid of MK(P) is high and the tube is conducting. Thus the right plate of MK(P) will rise and fall with the potential at the relay control tube cathodes and provide a regulation control signal. This signal from the right plate of MK(P) is connected to the right grid of MZ(1)A so that when the cathode potential of the relay control tube rises conduction in the right side of MZ(1)A will be increased and the potential at the common cathode of MZ(1)A will rise. This in turn will reduce conduction in the left side of MZ(1)A, raising both the left plate of MZ(1)A and the grids of SK(P) to which it is connected. This rise in grid potential will increase the current through SK(P) (part of which flows through the right side of MK(P)) to lower the relay control tube cathode potential. A fall in this potential will have just the reverse regulating effect. In this way the potential at terminals **36** of the storage chassis is maintained at +150 volts except during setting and clearing of storage. During setting the regulator control tube (right half of MK(P)) is effectively disabled by the reduced potential from the left plate of MS(P–Q) which cuts off conduction in the right side of MK(P). During clearing this disabling is not required since even though the left side of MZ(1)A is completely cut off, still CAP(1) will still be able to lower the SK(P) grids sufficiently to cause clearing.

Relay #**1** in the Storage Set chassis is the minus sign relay for storage location P. It is controlled through the left side of MK(P) and is actuated whenever a number stored in result storage location P is negative. The left side of MK(P) performs the same function for the sign relay #**1** as the relay control tubes do for the storage relays in the Storage chassis. The left plate of MK(P) is connected to +300 through the actuating coil of relay #**1** and the cathode is connected to the plate of Regulator stage SKP via Storage Set chassis terminal **16**. The left grid of MK(P) is controlled via terminal **37** by a "negative result" signal from the Zero Factor chassis (terminal **38**). This line is raised whenever a result in the accumulator is negative. Thus, if the number is transferred to result storage location P, the associated minus sign relay #**1** will be actuated.

The lower contacts on relay #**1** are the holding contacts, one being connected through the right resistor in RES(2) to the low end of the relay actuating coil and the other being connected with the plates of regulator stage SK(P) through chassis terminal **16**.

The right hand contacts on relay #**1** deliver a signal from terminal **21** to the card punching unit via terminal **12** to control punching of a special hole to designate negative numbers. This signal appears at terminal **21** only when a selector switch associated with the storage loca-

tion is set to permit the punching of a sign designating hole.

The left hand contacts of negative sign relay #1 serve to deliver a signal via a "minus neon" and terminal 17 to the Zero Factor chassis (terminal 18) when the P Keyboard Bias is raised (terminal 9). This signal is used to control the arithmetic process accordingly in a manner to be explained later.

The minus sign relays for the other seven storage locations and their related control circuits are identical with those just described in connection with storage location P.

GENERAL DESCRIPTION OF PROGRAM STEPS

Thus far the input-output unit, the data processing and storage unit, and certain parts of the control unit have been described (see Fig. 1). Recall that the control unit causes the system to perform a series of program steps determined by the plugboard wiring. The various chassis of the control unit, other than those already described, can best be understood after a preliminary description of the sequence of operations that occur in a program step.

As was stated earlier, a program step involves the performance of one of the four arithmetic operations upon two numbers, checking the result by a complementary operation, delivering the result to a result storage location, and initiating the next program step in accordance with the algebraic sign of the result. Neglecting for the moment the operations necessary to handle algebraic signs and to align and otherwise handle decimal points, the other basic operations performed for each of the four types of program steps will now be described. In each case the accumulator is preliminarily cleared.

In an addition program step the augend is first transferred from one of the 37 storage locations to the accumulator. Then the addend is transferred from another one of the 37 storage locations to the accumulator, the accumulator being conditioned to add. This produces the result in the accumulator. Next the result is transferred to one of the 8 result storage locations. While this completes the calculation called for by the program step, the step continues to check or prove the accuracy of the result before proceeding to the next step. First the A section (order 1A to 11A) of the accumulator is cleared or zeroized. Then the result which was just transferred to result storage is read back into the accumulator, the accumulator still being conditioned to add. Next the accumulator is conditioned to subtract and the addend is transferred from its storage location to the accumulator. This leaves in the accumulator the difference between the result (sum) and the addend, which difference should be equal to the augend if the calculation was properly performed. Next the augend is transferred from its storage location to the accumulator while the accumulator is still conditioned to subtract. This should leave the accumulator standing at zero. (Augend+addend=result; result—addend—augend=0.) If so, the next program step is commenced.

A subtraction program step involves the same series of operations as the addition step described above with the minuend replacing the augend and the subtrahend replacing the addend, except that the accumulator is conditioned to subtract when the subtrahend is entered to produce the result and to add when the subtrahend is entered during proof. (Minuend—subtrahend=result; result+subtrahend— minuend=0.)

A division step involves the following sequence of operations, again neglecting for the moment the operations incidental to handling algebraic sign and decimal point location. The general method employed for division is repeated subtractions with restoration after overcarry. First the dividend is entered with the accumulator conditioned to add. The dividend is then shifted to the left until its most significant digit is in the highest accumulator order (11M). Next the divisor is repeatedly entered with the accumulator conditioned to subtract and a one is added to order 1M (which is specially conditioned to add and initially stands at zero) each time the divisor is entered. When an overcarry occurs into order 11A the repeated subtractions are stopped, the divisor is entered once more with the accumulator conditioned to add (restoration after overcarry) and a one is subtracted from order 1M (specially conditioned to subtract). The accumulator contents are then shifted one place to the left (11M is fed back to 1A) and the repeated subtraction cycle commenced as before until overcarry occurs into order 11A. The divisor is then restored again, the accumulator contents shifted one place to the left again and subtractions are recommenced.

The above cycle is repeated for ten shifts after the first successful subtraction to produce an eleven digit quotient (the remainder being cleared). The quotient is then transferred to one of the 8 result storage locations (after decimal alignment). Next the A section of the accumulator is cleared and the proof operations are begun. The quotient is transferred from the result storage location to the accumulator and is multiplied by the divisor to produce a product that should equal the original dividend. The dividend is then subtracted from this result and if the result is zero, the next program step is commenced.

Multiplication is performed by repeated additions. In a multiplication step the multiplier is first transferred from one of the 37 storage locations to the accumulator and shifted to the left until a digit other than zero appears in order 11M. The multiplicand is then transferred repeatedly from its storage location to the accumulator and a one is subtracted from order 11M each time the multiplicand is entered. Whenever the digit in order 11M is reduced to zero, the multiplicand entries are temporarily halted and the entire accumulator contents are shifted to the left until another multiplier digit other than zero arrives in 11M. The multiplicand entries are then begun again and this sequence of repeated additions is continued until 11 shifts have occurred after the first digit other than zero was sensed in 11M. The product is then transferred to result storage. The proof operation consists of dividing the product by the multiplicand and subtracting the multiplier from the result. This should give zero and if so, the next program step is commenced.

Before proceeding to a more detailed description of the four types of program steps outlined above, the method of handling decimal point location will be described.

All addition and subtraction operations involved transfers of an operator to the accumulator which already contains an operand. The operator always comes from the card sensing unit or from the constant storage unit or from the result storage unit. No matter where the operator comes from, it is transferred without any shifting in transit; that is, the contents of each of the denominational orders of the source (1–10) are transferred to the corresponding denominational orders of the accumulator (A1–A10) regardless of where the decimal points lie in the operator and operand. Clearly then it is necessary during addition and subtraction steps to align the operand in the accumulator before the operator is transferred in so that the decimal point of the operand will be in the same position as the decimal point of the operator to be transferred in. This alignment of the operand in the accumulator is done by shifting the operand appropriately before the operator is registered.

The shifting is always done in the same direction since the accumulator can only shift in one direction. That direction is the direction of ascending significance or to the "left" in conventional number representation. If the orders of the accumulator are numbered 1–22 in order of ascending significance then a shift transfers the contents of each order to the next higher order except the contents of order 22 which are transferred to order 1. It is

apparent that 22 shifts would take a number through every position and back to its original position and that the operand may require anywhere from 0 to 21 shifts to bring its decimal point into registration with that of the operator subsequently to be transferred in. The number of shifts required to effect proper registration depends upon where the operand's decimal point is relative to the operator's decimal point.

The way in which this determination is made and proper registration of the operand effected will now be explained. Each operator and operand in any arithmetic step must ultimately come from one of a number of storage or sensing locations. Each of the locations has a capacity of up to 10 decimal digits. The position of the decimal point within each of the storage or sensing locations is established by switching done manually during machine set-up; consequently the location of the decimal point for any storage location remains unchanged during any given calculating run. To understand what these switching connections do it is necessary first to consider the Decimal Counter and its function.

The Decimal Counter is a binary counter that controls the number of shifts during the registration of an operand. It counts each shift during alignment after registration and terminates the shifting when it reaches capacity (22). Obviously, in order that it reach capacity after the proper number of shifts, it must be pre-set to a count that is a function both of the decimal point location in the operand and of the decimal point location in the operator. More specifically, the decimal counter must be pre-set to the number which is the 22's complement of the number of times the operand must be shifted left to align its decimal point with that of the operator subsequently to be transferred in. If the counter is thus pre-set to the 22's complement of the required number of shifts, then it will read 22 after the required number of shifts and shifting will be terminated.

As a basis for discussing the manner in which the counter is pre-set, let us assume that the location of decimal points within numbers is designated by a number equal to the number of shifts to the left necessary to align the decimal point with an arbitrary reference position. Let X be the number of left shifts required to align the operand's decimal point with the arbitrary reference point and let Y be the number of left shifts required to align the operator's decimal point with the arbitrary reference. Then $X-Y$ is the number of shifts to the left required to align the operand's decimal point with the operator's decimal point. The number that must be pre-set in the decimal counter is the 22's complement of this number or $22-(X-Y)$ or, expressed another way, $22-X+Y$. From the last expression we see that if the 22's complement of X is entered to the counter and then Y is added, the counter will be pre-set to the desired number. Thus, whenever it is required to align a number in the accumulator so that its decimal point, the location of which is designated by the number X, aligns with the location designated by the number Y, first the 22's complement of X is entered to the Decimal Counter and then Y is added. This pre-sets the counter so that it will read 22 after the exact number of shifts required for alignment.

The decimal location numbers corresponding to X and Y above and their complements are transferred to the decimal counter from the decimal switches associated with each storage and card sensing location. Their transfer from the switches is enabled by the keyboard bias elements in the same way that regular data transfer is enabled. The switches establish connections for both the true and complementary values of the numbers designating decimal point location; either the true or complementary connections are energized by the control unit depending upon nature of the number to be registered.

Recall that in addition and subtraction the operand must be aligned so that its decimal point is in the same position as that of the operator subsequently to be registered. Then the result after operator registration will have its decimal point located at the same position as that of the operator. A similar problem arises in connection with the transfer of results to storage. Since each storage location has its decimal point location established by a switch setting, results must be aligned prior to transfer to storage so that decimal point locations will coincide. This alignment is accomplished in the same way as the alignment made prior to operator registration in addition and subtraction. First the number representing the 22's complement of the result decimal location is registered in the decimal counter and then the true value of the number representing the decimal location in the result storage is added. The result is then shifted the number of times required to bring the decimal counter to capacity. When shifting is completed the result is aligned for direct transfer to the result storage location.

In multiplication and division the initial alignment is different than in addition and subtraction but the end result desired is the same, namely to eventually align the result decimal point with that of the storage location to which the result is to be transferred. Since multiplication and division require the initial registration of the multiplier or dividend and involve multiple registrations of the multiplicand or divisor with intervening shifts, maintaining decimal point control is somewhat more complex than in addition and subtraction. The manner in which the control is effected will be explained in detail in connection with the division and multiplication examples. It should be noted here however, that in both multiplication and division, the object is to wind up the calculation with the complement of the number designating the result decimal location registered in the decimal counter.

As stated previously, the various chassis comprising the control unit (see Fig. 1) and the sequence of control signals during the execution of typical program steps can best be explained after a preliminary description of the detailed functions performed in each of the four types of program steps. Accordingly, a typical example of each type will now be described in detail so that the functions to be performed by the various elements of the control unit will be understood.

The terms "minidend" and "subvisor" are used for convenience in the following descriptions instead of the conventional terms "operator" and "operand." The minidend is the factor registered first in the accumulator during any arithmetic operation and the subvisor is the factor registered subsequently. The minidends in addition and subtraction are respectively the augend and the minuend (both operands) while in multiplication and division the minidends are respectively the multiplier (an operator) and dividend (an operand). The subvisors in the four arithmetic operations are respectively the addend, subtrahend (both operators), multiplicand (an operand) and divisor (an operator).

The terms minidend (abbreviated M'd) and subvisor (abbreviated S'r) are used in the following descriptions in accordance with the preceding definition.

The manner in which the basic arithmetic and checking operations are performed by the calculator is described in the following sections. Tables illustrating typical examples of addition, division, and multiplication are included. An understanding of certain properties of the Accumulator and subsidiary counters is prerequisite to a study of the examples shown in the tables to follow.

The Accumulator: Each column of the accumulator is a counter which counts forward when its + bias is raised and backward when its — bias is raised. Three independent pairs of bias lines are used, as follows:

(1) 1A through 11A inclusive, called A
(2) 1M through 10M inclusive, called M
(3) 11M

These lines are raised as shown in the following table:

	A	M	11M
To add a pos. number or subtract a neg. number	+	+	+
To subtract a pos. number or add a neg. number	−	−	−
To add S'r in multiplication	+	+	−
To subtract S'r in division	−	+	+
To add S'r back in division	+	−	−

Numbers may be entered in columns 1A through 10A inclusive. In multiplication, a 1 is entered in column 11M whenever the RIG is operated to register the S'r. In Division, a 1 is entered in column 1M whenever the RIG is operated to register the S'r.

A carry in any column adds 1 to the next column to the left. The accumulator normally carries as a ring, with column 11M carrying to column 1A. There are two exceptions to this:

(1) In making the Proof Subtraction, the carry from 11M is blocked.

(2) In adding a "1" to Acc. 1A after "9" check, the carry from 11M is blocked.

In shifting, the accumulator always operates as a ring, with 11M shifting into 1A. Each shift pulse moves every digit in the accumulator one column to the left.

The Decimal Counter: The Dec. Counter counts forward only. Negative dec. indications are entered as complements on 22.

In the Dec. Counter, 22 and zero have the same meaning. In other words, the 22nd count in effect resets the Dec. Counter to zero.

In addition to the dec. registrations indicated, the Dec. Counter counts all shifts.

The M.D. Counter: The M.D. Counter is similar to the Dec. Counter, but counts only shifts. It is gated in a manner indicated in the example.

After the M.D. Counter has indicated the completion of the multiplication or division process, it continues to count, but has no further effect on the program.

The Accumulator is to be treated as a ring, with column 1A adjacent to column 11M.

Decimals are measured to the right from the reference position between column 5M and column 6M.

Example.—The decimal between column 3A and column 4A is 13.

Complements of decimals are formed by subtracting the decimal from 22.

Example.—The complement of the decimal between column 3A and column 4A is 9.

When it is desired to indicate a decimal position independently of the reference position, it is shown thus; (3A, 4A) indicating the decimal position between column 3A and column 4A.

In addition to receiving decimal registrations, the Decimal Counter counts all shifts in the Accumulator.

Addition and Subtraction: In addition and Subtraction, the Decimal Counter must be "preset" in such a way that the M'd shifts will bring it to 22 when the M'd decimal aligns with the S'r decimal. To do this, we first enter the M'd decimal complement and the S'r decimal. This is effectively a subtraction of the M'd and S'r decimal positions, and gives "S'r decimal minus M'd decimal." This is the "complement of the number of places the M'd decimal is to the right of the S'r decimal." Since the M'd is shifted to the left, the number of shifts required for alignment is "the number of places the M'd decimal is to the right of the S'r decimal." Since these numbers will always add to 22, the desired result is obtained.

Since the same method is used to align the Result for storage, in Addition and Subtraction it is necessary to enter the decimal complement of the Result after the above alignment has been made. In this case, the Result has been formed at the S'r decimal position, so it is the complement of the S'r decimal which we actually enter. Then, when the Storage decimal is entered, the alignment of the Result with Storage will be again indicated by the Decimal Counter reaching 22.

The following example shown in tabular form will illustrate a complete addition step. Subtraction is performed in a similar manner. Note that where no digit content of an accumulator order is shown, the content is zero. Decimal point locations are shown as an aid to understanding how they are handled.

Addition

	"M" section										"A" section										Dec. Ctr.	M.D. Ctr.
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1		
THE PROBLEM																								
The M'd is:														5	2.	3	4							
The M'd decimal is:											8													
The S'r is:																	1	3	5	7.				
The S'r decimal is:											13													
The Storage decimal is:											10													
STEP ZEROIZE																								
The calculator is zeroized																								
M'd REGISTRATION																								
The M'd decimal complement is entered in the Dec. Ctr.																								1
The M'd numerical registration is made														5	2.	3	4							14
ADDITION PROCESS																								
The S'r decimal is entered in the Dec. Ctr.														5	2.	3	4							5
The M'd is shifted to align with the S'r, as indicated by the Dec. Ctr. reaching 22																	5	2.	3	4				22
The S'r decimal complement is entered in the Dec. Ctr.																	5	2.	3	4				9
The S'r numerical registration is made													1	4	0	9.	3	4						9
ALIGN AND STORE																								
The storage decimal is entered in the Dec. Ctr.													1	4	0	9.	3	4						19

Addition—(Cont'd.)

"M" section											"A" section										Dec. Ctr.	M.D. Ctr.
11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	

The result is shifted to align with Storage, as indicated by the Dec. Ctr. reaching 22

1 4 0 9. 3 4 — 22

The Result is now transferred to Storage

PROOF ZEROIZE

The "A" Section is zeroized

PROOF M'd REGISTRATION

The Proof M'd (Storage) decimal complement is entered in the Dec. Ctr. — 12

The Proof M'd (Storage) numerical registration is made

1 4 0 9. 3 4 — 12

ADDITION PROOF PROCESS (SUBTRACTION)

The Proof S'r (S'r) decimal is entered in the Dec. Ctr.

1 4 0 9. 3 4 — 3

The Proof M'd (Storage) is shifted to align with the Proof S'r, as indicated by the Dec. Ctr. reaching 22

1 4 0 9. 3 4 — 22

The Proof S'r (S'r) decimal complement is entered in the Dec. Ctr.

1 4 0 9. 3 4 — 9

The Proof S'r (S'r) numerical registration is made

5 2. 3 4 — 9

PROOF SUBTRACTION

The M'd decimal is entered in the Dec. Ctr.

5 2. 3 4 — 17

The Proof Result is shifted to align with the M'd, as indicated by the Dec. Ctr. reaching 22

5 2. 3 4 — 22

The M'd is subtracted: — 22

The 0–9 Check Circuit on columns 1A through 10A shows all zeros, to indicate a good answer

Multiplication:
Method—

S'r	1 7 6.5 3 1
M'd	9 7.1
	1 5 8 8.7 7 9
	1 2 3 5 7 1 7
	1 7 6 5 3 1
Result	1 7 1 4 1.1 6 0 1

Note that the decimal of the first partial product falls in the same position as that of the S'r. Also, the Result decimal is to the right of this by "one less than the number of M'd places to the left of the decimal." We could obtain this figure by subtracting the M'd shifts from the M'd decimal position with respect to (10M, 11M). But the figure we want in the Decimal Counter is the complement of this, as explained under Addition and Subtraction. If, instead, we add the M'd shifts to the M'd decimal complement, we will obtain the desired result. Fortunately, this allows us to make the M'd decimal registration in the same manner as in Addition and Subtraction, and to count shifts in the normal manner. The number in the Decimal Counter is now the complement of "one less than the number of M'd places to the left of the decimal." By adding to this the S'r decimal complement, we will have the complement of the Result decimal with reference to (10M, 11M) at the time of the first S'r registration.

We may say then, with reference to (10M, 11M), that the Result decimal position at the time of the first S'r registration is:

M'd decimal complement+S'r decimal complement +M'd shifts

The Result will now be shifted 11 places to the left in the process of completing Multiplication. However, the Decimal Counter will also count these shifts, and will continue to indicate the complement of the Result decimal position. This is also true while the Result is shifted to 11M prior to zeroizing the A Section of the Accumulator. The preceding has assumed a decimal reference at (10M, 11M). Since the calculator reference is at (5M, 6M), we must correct the M'd complement and S'r complement, which were entered with reference to (5M, 6M). We must also correct the Result, which must be made to indicate with reference to (5M, 6M).

To correct the M'd, we must subtract 5, or add its complement	17
To correct the S'r, we must subtract 5, or add its complement	17
To correct the Result, we must add	5
	39

In the Decimal Counter, 39=17. This is the correction we must add to the Decimal Counter to bring its final Result into reference with the calculator decimal. After the Multiplication process is completed, the Decimal Counter indicates the complement of the Result decimal. To align the Result with Storage, it is now only necessary to register the Storage decimal and shift until the Decimal Counter reaches 22, as shown under Addition and Subtraction.

The following example shown in tabular form will illustrate a complete multiplication step.

Multiplication

"M" section	"A" section	Dec. Ctr.	M.D. Ctr.
11 10 9 8 7 6 5 4 3 2 1	11 10 9 8 7 6 5 4 3 2 1		
THE PROBLEM			
The M'd is:	3 0 0. 0 0 1		
The M'd decimal is: 13			
The S'R is:	1 1 1 2 2. 3 3 5 5		
The S'r decimal is: 11			
The Storage decimal is: 14			
STEP ZEROIZE			
The calculator is zeroized			
M'd REGISTRATION			
The M'd decimal complement is entered in the Dec. Ctr.			
The M'd numerical registration is made	3 0 0. 0 0 1	9	
MULTIPLICATION PROCESS			
The S'r decimal complement is added in the Dec. Ctr.	3 0 0. 0 0 1	20	
The M.D. constant of 17 is added in the Dec. Ctr.	3 0 0. 0 0 1	15	
The M'd is shifted until its first digit appears in column 11M. Each of these shifts is counted in the Dec. Ctr. The first 11 are counted in the M.D. Ctr.			
3 0 0. 0 0 1		9	11
The first S'r addition is now made			
2 0 0. 0 0 1	1 1 1 2 2 3 3. 5 5 5	9	11
The RIG now continues to run until the digit in 11M reaches zero			
0 0 0. 0 0 1	3 3 3 6 7 0 0. 6 6 5	9	11
The M'd is again shifted until a number arrives in 11M. These shifts are counted in both the Dec. Ctr. and the M.D. Ctr.			
1	3 3 3 6 7 0 0. 6 6 5	14	16
The S'r is again added until Column 11M reaches zero			
	3 3 3 6 7 1 1. 7 8 7 3 3 5 5 5	14	16
The above process is repeated until the M.D. Ctr. reaches 22, indicating the completion of multiplication			
3 3 3 6 7 1 1. 7 8 7 3 3 5 5 5		20	22
The Result is now shifted until its first digit is in 11M			
3 3 3 6 7 1 1. 7 8 7 3 3 5 5 5		21	--
The "A" Section is zeroized, leaving 11 digits of Result			
3 3 3 6 7 1 1. 7 8 7 3		21	
ALIGN AND STORE			
The Storage decimal is added in the Dec. Ctr.			
3 3 3 6 7 1 1. 7 8 7 3		13	
The Result is shifted to align with Storage, as indicated by the Dec. Ctr. reaching 22			
7 3	3 3 3 6 7 1 1. 7 8	22	
The Result is now transferred to Storage			
PROOF ZEROIZE			
The "A" Section is zeroized			
7 3		22	
PROOF M'd REGISTRATION			
The Proof M'd (Storage) decimal complement is entered in the Dec. Ctr.			
7 3		8	
The Proof M'd (Storage) numerical registration is made			
7 3	3 3 3 6 7 1 1. 7 8	8	
MULTIPLICATION PROOF PROCESS (DIVISION)			
The Proof S'r (S'r) decimal is added in the Dec. Ctr.			
7 3	3 3 3 6 7 1 1. 7 8	19	
The M.D. constant of 17 is added in the Dec. Ctr.			
7 3	3 3 3 6 7 1 1. 7 8	14	
The Proof M'd (Storage) is shifted until its first digit appears in Column 11M. Each of these shifts is counted in the Dec. Ctr. The first 11 shifts and one extra count are entered in the M.D. Ctr.			
3 3 3 6 7 1 1. 7 8 7 3		5	12
The first trial Proof S'r (S'r) subtraction is now made, at same time adding a one in 1M (subtractive carry from 11A is also added in 1M)			
3 3 3 6 7 1 1. 7 8 7 5 9 8 8 8 7 7 6 6 4 4 5		5	12

Multiplication—(Cont'd.)

	"M" section											"A" section												
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	Dec. Ctr.	M.D. Ctr.
The overcarry from 11A to 1M indicates an unsuccessful trial Subt. so the proof S'r (S'r) is added back, at same time subtracting a one from 1M (additive carry from 11A is also subtracted from 1M)																								
	3	3	3	6	7	1	1.	7	8	7	3												5	12
The Proof M'd (Storage) is shifted until the next number appears in column 11M																								
	3	3	6	7	1	1.	7	8	7	3												3	6	12
This process continues until a successful trial subtraction is made																								
	3										1		2	2	2	4	4	7	8.	2	3	2	15	12
The RIG now continues to run until an overcarry from 11A to 1M occurs. (One is added in 1M for each RIG cycle and when subtractive carry occurs from 11A)																								
	3										5	9	8	8	8	7	7	7	7.	5	6		15	12
The Proof S'r (S'r) is added back. (1M is reduced by one during the RIG cycle and by one more due to additive carry from 11A)																								
	3										3							1	1.	1	2	2	15	12
The M.D. Ctr. now starts to count shifts again and the above process is repeated until the M.D. reaches 22 indicating the completion of Proof of Multiplication (Division)																								
	3	0	0.	0	0	0	9	9	9	9	9			7	5	6	7	3	3	5	5	5	3	22
The "A" Section is zeroized leaving 11 digits of Proof Result																								
	3	0	0.	0	0	0	9	9	9	9	9												3	--

PROOF SUBTRACTION

	"M" section											"A" section												
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	Dec. Ctr.	M.D. Ctr.
The M'd decimal is entered in the Dec. Ctr.																								
	3	0	0.	0	0	0	9	9	9	9	9												16	
The Proof Result is shifted to align with the M'd as indicated by the Dec. Ctr. reaching 22																								
	9	9	9	9	9												3	0	0.	0	0	0	22	
The M'd is subtracted																								
	9	9	9	9	8	9	9	9	9	9	9	9	9	9	9	9	9	9	9.	9	9	9	22	
The 0–9 Check Circuit on columns 1A through 10A shows all 9s, to indicate a good answer																								

Division:

(1M, 11A)

Method—

```
                 1 4 1 2.6 - -  Result
    S'r  .9 5 4/1 3 4 7.6 8 0 0   M'd
                9 5 4 0 0 0 0
                -------------
                3 9 3 6 8 0 0
                3 8 1 6 0 0 0
                -------------
                  1 2 0 8 0 0
                    9 5 4 0 0
                  -----------
                    2 5 4 0 0
                    1 9 0 8 0
                    ---------
                      6 3 2 0
                      5 7 2 4
                      -------
                        5 9 6
```

At the time of the first successful trial subtractions, the first digit of the Result is formed in column 1M. There will be an additional digit of Result to the left of the Result decimal for each place between the M'd decimal and the S'r decimal. Since the first digit of the Result is in 1M, the Result decimal will be to the right of the (11A, 1M) point by the difference between the M'd and S'r decimal positions. It is necessary, at this time, for the Decimal Counter to indicate the displacement between M'd and S'r decimals. To do this, the S'r decimal is added to the M'd decimal complement to give the complement of the original displacement. The subsequent shifts of the M'd, prior to the first successful trial subtraction, are added in the Decimal Counter to the original difference complement. This has the same effect as decreasing the difference. Thus, the Decimal Counter indicates, at the time of the first successful trial subtraction, the Result decimal complement with respect to the (11A, 1M) point.

In the process of completing Division, the Result will be shifted until its first digit is in 11M. However, these shifts will be counted in the Decimal Counter, which will continue to indicate the Result decimal complement with respect to (11A, 1M). The preceding has assumed a decimal reference at (11A, 1M). However, the calculator reference is at (5M, 6M), and we must correct the Result to indicate with respect to this reference. Since the M'd and S'r decimals were effectively subtracted, their corrections cancel and need not be considered. The Result is corrected by subtracting 5, or adding its complement, 17. After the Division process is completed, the Decimal Counter indicates the complement of the Result decimal. To align the Result with Storage, it is now only necessary to register the Storage decimal and shift until the Decimal Counter reaches 22, as shown under Addition and Subtraction.

The following example shown in tabular form will illustrate a complete division step.

Division

	"M" section											"A" section												
	11	10	9	8	7	6	5	4	3	2	1	11	10	9	8	7	6	5	4	3	2	1	Dec. Ctr.	M.D. Ctr.
THE PROBLEM																								
The M'd is:																		4	3	4	3·	2.		
The M'd decimal is: 16																								
The S'r is:													1	7.	9	3	1							
The S'r decimal is: 8																								

Division—(Cont'd.)

"M" section	"A" section	Dec. Ctr.	M.D. Ctr.
11 10 9 8 7 6 5 4 3 2 1	11 10 9 8 7 6 5 4 3 2 1		
The Storage decimal is:	11 0 0 0 0 0. 0 0 0 0 0		
STEP ZEROIZE			
The claculator is zeroized			
M'd REGISTRATION			
The M'd decimal complement is entered in the Dec. Ctr.			
		6	
The M'd numerical zegistration is made			
	4 3 4 3 2.	6	
DIVISION PROCESS			
The S'r decimal is added in the Dec. Ctr.			
	4 3 4 3 2.	14	
The M.D. constant of 17 is added in the Dec. Ctr.			
	4 3 4 3 2.	9	
The M'd is shifted until its first digit appears in Column 11M. Each of these shifts is counted in the Dec. Ctr. The first 11 shifts and one extra count are entered in the M.D. Ctr.			
4 3 4 3 2.		4	12
The first trial S'r subtraction is now made			
4 3 4 3 2.	2 9 8 2 0 6 9	4	12
The overcarry from 11A to 1M indicates an unsuccessful trial subtraction, so the S'r is added back			
4 3 4 3 2.		4	12
The M'd is shifted until the next number appears on Column 11M			
3 4 3 2.	4	5	12
This process continues until a successful trial subtraction is made			
	1 2 5 5 0 1.	14	12
The RIG now continues to run until an overcarry from 11A to 1M occurs			
	4 9 8 9 6 3 9.	14	12
The S'r is added back			
	2 7 5 7 0.	14	12
The M.D. Ctr. now starts to count shifts again, and the above process is repeated until the M.D. Ctr. reaches 22, indicating the completion of division			
2 4 2 2. 1 7 3 8 8 8 7	1 7 2 0 3	2	22
The "A" Section is zeroized, leaving 11 digits of Result			
2 4 2 2. 1 7 3 8 8 8 7		2	--
ALIGN AND STORE			
The Storage decimal is added in the Dec. Ctr.			
2 4 2 2. 1 7 3 8 8 8 7		13	
The Result is shifted to align with Storage, as indicated by the Dec. Ctr. reaching 22			
8 7	2 4 2 2. 1 7 3 8 8	22	
The Result is now transferred to Storage			
PROOF ZEROIZE			
The "A" Section is zeroized			
8 7		22	
PROOF M'd			
The Proof M'd (Storage) decimal complement is entered in the Dec. Ctr.			
8 7		11	
The Proof M'd (Storage) numerical registration is made			
8 7	2 4 2 2. 1 7 3 8 8	11	
DIVISION PROOF PROCESS (MULTIPLICATION)			
The Proof S'r (S'r) decimal complement is added in the Dec. Ctr.			
8 7	2 4 2 2. 1 7 3 8 8	3	
The M.D. constant of 17 is added in the Dec. Ctr.			
8 7	2 4 2 2. 1 7 3 8 8	20	
The Proof M'd (Storage) is shifted until its first digit appears in column 11M. Each of these shifts is counted in the Dec. Ctr. The first 11 are counted in the M.D. Ctr.			
2 4 2 2. 1 7 3 8 8 8 7		11	11
The first Proof S'r (S'r) addition is now made			
1 4 2 2. 1 7 3 8 8 8 7	1 7 9 3 1.	11	11
The RIG now continues to run until the digit in 11M reaches zero			
0 4 2 2. 1 7 3 8 8 8 7	3 5 8 6 2.	11	11

Division—(Cont'd.)

"M" section	"A" section	Dec. Ctr.	M.D. Ctr.
11 10 9 8 7 6 5 4 3 2 1	11 10 9 8 7 6 5 4 3 2 1		
The Proof M'd (Storage) is again shifted until a number arrives in 11M. These shifts are counted in both the Dec. Ctr. and the M.D. Ctr.			
4 2 2. 1 7 3 8 8 8 7	3 5 8 6 2.	12	12
The Proof S'r (S'r) is again added until Column 11M reaches zero			
0 2 2. 1 7 3 8 8 8 7	4 3 0 3 4. 4	12	12
The above process is repeated until the M.D. Ctr. reaches 22 indicating the completion of Proof of Division (multiplication)			
4 3 4 3 1. 9 9 9 9 9 8	2 7 9 7	22	22
The Proof Result is now shifted until its first digit is in 11M			
4 3 4 3 1. 9 9 9 9 9 8	2 7 9 7	1	--
The "A" Section is zeroized leaving 11 digits of Proof Result			
4 3 4 3 1. 9 9 9 9 9 8		1	
PROOF SUBTRACTION			
The M'd decimal is entered in the Dec. Ctr.			
4 3 4 3 1. 9 9 9 9 9 8		17	
The Proof Result is shifted to align with the M'd as indicated by the Dec. Ctr. reaching 22			
9 9 9 9 9 8	4 3 4 3 1.	22	
The M'd is subtracted			
9 9 9 9 9 7 9 9 9 9 9 9	9 9 9 9 9 9 9 9	22	
A "1" (one) is entered in col. 1A of no zero check			
9 9 9 9 9 8 0 0 0 0 0 0	0 0 0 0 0 0 0 0	22	
The zero check circuit on columns 1A thru 10A shows all zeros to indicate a good answer			

Note that each of the four types of program steps just described consists essentially of what may be regarded as eight separate operational phases as follows:

Step Zeroize
M'd Registration
Process (including S'r Registration)
Align and Store
Proof Zeroize
Proof M'd Registration
Proof Process (including Proof S'r Registration)
Proof subtraction

While the Step Zeroize and M'd Registration phases are the same for all types of program steps (addition, subtraction, multiplication and division) the other phases differ depending upon the type of program step or arithmetic "process" being performed. All phases of all steps are seen, however, essentially to involve merely transferring numbers from the various storage locations to the accumulator, conditioning the various accumulator orders to add or subtract, shifting accumulator contents, and transferring results from the accumulator to a result storage location.

The chassis comprising the Control unit (see Fig. 1) cooperate to control these transfers, conditionings, and shifts to perform the program called for by the plugboard connections. Of the chassis comprising the Control unit, the Storage Set, Storage Zeroize, Regulator, Keyboard Bias, Registration Impulse Generator, and Decimal Counter chassis have been previously described. The Step Sequence, Base Control, Output Control, Step Control, and Control chassis will now be described.

STEP SEQUENCE CHASSIS

The plugboard (Fig. 42) provides for setting up a calculating program comprising as many as 40 unique steps. The plugboard cooperates with 10 Step Sequence (SS) chassis (Fig. 30) in performing the program control function. Each of the 10 Step Sequence chassis are associated with 4 of the 40 program steps. For example, the typical chassis, shown in Fig. 30, is associated with program steps 1, 2, 3, and 4. It is apparent from Fig. 30 that the chassis actually comprises four identical portions each containing a trigger stage (e.g. (1)ES), a diode gating stage (e.g. left half of (1, 2)ED), and six triode gating stages (e.g. left halves of (1, 2)EMF, (1, 2)ESF, (1, 2)ERF, 1, 2)EPF, (1, 2)EBP, (1, 2)EBM).

The ES trigger is on whenever its associated step is in progress; thus only one of the forty ES triggers is on at any one time, all others being off. Each step trigger ES is turned on through its associated input gating stage ED (right or left half) in a manner to be explained later. When a step trigger ES is on, its left plate is raised in potential to enable its associated triode gates EMF, ESF, ERF, EPF, EBP, and EBM. These gates serve to control the energization of plugboard terminals associated with the step in progress. The gates and other step sequence stages associated with program step 1 will now be described; those for all other steps are the same. The designation (1)EMF (for example) will be used to designate the left half of stage (1, 2)EMF, so as to avoid constant reference to the "left half."

The plate of (1)EMF is connected to chassis terminal 28 which in turn is connected to the plugboard terminal in row 1, column V_1. Thus when (1)EMF conducts, the potential at the V_1 terminal of row 1 (program step 1) of the plugboard will be lowered. This terminal will be plugged (connected) to one of the storage location terminals A–Y to specify the M'd storage location for step 1. Thus, when (1)EMF conducts, the lowered potential at its plate will be transmitted through the plugboard to the Keyboard bias chassis for the storage location of the M'd in step 1. This effectively selects the M'd for step 1 from among the 37 storage locations.

Note that (1)EMF can conduct to select this M'd only during the progress of step 1 when trigger (1)ES is on. Also note that conduction in (1)EMF can occur only when its cathode, which is connected to chassis terminal 34, is at a lower potential than its grid. Terminal 34 is lowered in potential by the EMK signal from the Control chassis (terminal 12) only during the selected periods of a step when it is desired to transfer the M'd from its storage location to the accumulator.

In the same way, gate stage (1)ESF causes the S'r for step 1 to be selected from its storage location for transfer to the accumulator.

The plate of (1)ESF is connected via chassis terminal 24 to the V_2 plugboard terminal in row 1 and from there to the proper KB circuits via one of the A–Y storage location plugboard terminals; thus when (1)ESF conducts, the storage location containing the S'r for step 1 will be selected for transfer to the accumulator. The cathode of (1)ESF is lowered to permit conduction by the ESK signal (from the Control chassis terminal 14) over terminal 32 only during those periods in a step when the S'r is to be transferred to the accumulator. The EMK and ESK signals are always simultaneously applied to all Step Sequence chassis but permit conduction only in the gates of the step in progress since only their grids will be raised by the associated step trigger.

Result storage location for step 1 is selected in the same way by stage (1)ERF under the control of the ERK signal delivered at terminal 31 from the Control Chassis (terminal 16). The plate of (1)ERF is connected via chassis terminal 20 to plugboard terminal R in row 1 and from there via one of the P–Y storage location terminals to the appropriate Keyboard Bias circuit.

The process (addition, subtraction, multiplication, or division) to be performed in step 1 is established by gate stage (1)EPF which conducts whenever step 1 is in progress (since its cathode is permanently connected to ground potential). The plate of (1)EPF is connected via chassis terminal 16 to the plugboard terminal "Process" in row 1 and from there by a plugboard connection to the add, subtract, multiply or divide terminal. All terminals in each of these later rows of terminals are connected together and the rows are connected respectively to terminals 2, 4, 6, and 8 of the Decimal Control Chassis and to terminals 8, 10, 12, and 14 of the Zero Factor chassis.

During any step, one of these rows is lowered in potential by conduction in the ( )EPF stage and the plugboard connection and the consequent lowered potential at one of the aforementioned Decimal Control and Zero Factor chassis terminals determines the arithmetic operation to be performed.

The ( )EBM and ( )EBD stages determine, through their associated plugboard connections, which step will be commenced after completion of the step in progress. Stage (1)EBM, for example, conducts at the conclusion of step 1 when the result is negative, as indicated by a lowered potential at chassis terminal 5, connected to the cathode of (1)EBM. If the result is positive terminal 5 will remain high to prevent conduction in (1)EBM but terminal 6 will be lowered to cause (1)EBP to conduct. Terminals 5 and 6 are connected to terminals 3 and 5 respectively of the Step Control chassis (Fig. 29) which are raised or lowered depending upon whether a result is positive or negative.

The plate of (1)EBM is connected through chassis terminal 8 to the plugboard "From-minus" terminal in row 1 and the plate of (1)EBP is connected through chassis terminal 12 to the "From-plus" terminal. Thus, the "From-minus" terminal will be lowered in potential when a result of step 1 is negative and the "From-plus" terminal will be lowered when a result is positive. Each of these "From" terminals may be connected to the same or different "To" terminals so that, on completion of step 1, the program will branch to say step 7 if the result was negative or to step 2 if the result was positive. As will be seen later, branching from any step can be to any other step.

While the foregoing description of the role of the Plugboard and Step Sequence Chassis in program control has used program step 1 and its associated circuits as examples, all other program steps are controlled in the same way. To summarize, the process to be performed in any step, the storage locations of the factors involved, the storage location for the result, and the next step for both positive and negative results, are all established by plugboard connections. These plugboard connections are energized, or rendered effective by the Step Sequence circuits. During each step only the plugboard connections specifying that step are energized and then only during the periods within the step when they are needed.

BASE CONTROL AND OUTPUT CONTROL CHASSIS

In addition to the four types of arithmetic program steps, four types of output operations may be performed. These are designated Set, Sort, Clear, and Trip.

The Set operation transfers numbers from all or selected result storage locations to the punch actuating storage in the card punching operation without clearing the result storage locations. Two such operations Set I and Set II are provided, either of which may be programmed to follow and be followed by any other program step or output operation.

The Sort operation delivers a signal to the card punching unit to cause the card being operated upon to be sorted into a special hopper after it is subsequently punched and ejected. Two of these operations, Sort I and Sort II are provided, either of which, again, may be programmed to follow and be followed by any other program step or output operation.

The Clear operation clears all or selected output storage locations and may also be programmed to follow and be followed by any program step or output operation.

The Trip operation delivers a signal to the card punching unit to cause the card to be moved from the reading station to the punching station, and, after punching, to be delivered to an output hopper (a regular hopper if the Trip operation was preceded by a Sort operation). Simultaneously, the next input card is moved to the reading station. The Trip operation causes the first program step to be commenced and can therefore be followed by no other program step or output operation.

Signals for controlling the above output operations are delivered to the card punching unit (not shown) from the Base Control chassis shown in Fig. 17. The Sort I and Sort II operations are controlled by two solenoids in the card punching unit which are energized by thyratrons EGT1 and EGT2, respectively, through Base Control chassis terminals 8 and 10 respectively. Thyratrons EGT1 and EGT2 are in turn controlled by the left halves (in parallel) and the right halves (in parallel) of gating amplifiers EGCG respectively. Both halves receive a positive pulse over their common capacitive input from the left plate of Schmitt trigger EGA at each positive half cycle of line voltage. Both halves are normally biased to cut off, however, and do not conduct in response to the positive pulse from EGA. The left and right biases are controlled by the potentials applied at terminals 1 and 3 respectively. When a Sort I operation is to be performed, terminal 1 will be raised in potential by the Output Control chassis so that the left halves of EGCG will conduct in response to the positive pulse from EGA. As a result, the transformer connected in the left plate circuit of EGCG will deliver a positive pulse to the grid of Thyratron EGT1, causing it to fire. This will in turn actuate the Sort I solenoid as explained above. In summary, when a Sort I operation is to be performed, the potential at terminal 1 will be raised by the Output Control chassis and as a result, the Sort I solenoid will be actuated through the Sort I thyratron EGT1 on the next positive half cycle of line voltage (which also supplies the thyratron through the solenoid). The Sort II operation will be performed similarly by thyratron EGT2 when the potential at terminal 3 is raised.

The Set I and Set II operations are similarly controlled by the left and right halves respectively of ELCA and ELCG (in parallel) when the potentials at terminals 5 or 7 are raised. The thyratrons for these operations are not shown since they are located in the card punching unit; their grids, however, are controlled by the potentials on terminals 14 and 16 respectively which are trans-

former coupled with the left and right plate circuits of ELCA and ELCG.

The Trip I and Trip II thyratrons (not shown) are controlled by the potentials at terminals **26** and **28** respectively. Terminal **26** is transformer coupled with the left plates of EPCA, EPCG, EGPA, and EGPG, and with both plates of ENGG. Thus, when any of these plates conduct, the Trip I thyratron will be fired. The left grids of EPCA and EPCG are controlled by the potential at terminal **9** which in turn is raised by the Output Control chassis whenever a Trip I operation is called for by the plugboard. The left grids of EGPA and EGPG are controlled by the potential at terminal **15** which in turn is raised by the Output Control chassis whenever a card is to be rejected; i.e., Tripped and Sorted. Note that the raised potential at terminal **15** will also cause the right halves of EGPA and EGPG to conduct thereby actuating the Sort I thyratron to which their plates are coupled through the left sides of EGCG. The grids of ENCG are controlled by the potential at terminal **13** which is, in turn, raised by the Output Control chassis whenever a zero factor is detected and a selector switch is set for "non-calculate" in this situation.

Diode stages **ETM1, ETM2,** and **ETM3** serve as buffers or mixers to actuate flip-flop EBAL whenever any of the Sort, Set, or Trip operations occur, and thus send a negative pulse over terminal **25** to the Step Control chassis, to signal completion of an output operation. The plates of these buffer stages are connected in common to the input to flip-flop EBAL so that when any of them conducts, EBAL will be actuated and deliver the required negative pulse to terminal **25** when it returns to normal. The cathodes of the buffer stages are coupled capacitively with the output operation thyratron plates so that conduction will be momentarily increased in one of the buffer halves whenever an output operation thyratron is fired. Connection to the thyratron plates is via chassis terminals **8, 10, 18, 20, 30** and **32.**

Buffer diode stage **ETM4** delivers a negative pulse over its common plate connection and chassis terminal **23** to the Step Control chassis whenever the Trip I or Trip II thyratrons are fired. Its cathodes are coupled with the thyratron plates in the same way as explained above for the other buffers (via terminals **18** and **20**).

As now understood, the Base Control chassis receivers signals from the Output Control chassis designating which output operations are to be performed and actuates control thyratrons accordingly. It also delivers to the Step Control chassis, signals indicating the completion of output operations.

The Output Control chassis shown in Fig. 24 receives from the plugboard and other controls, signals designating which output operations are to be performed and delivers appropriate signals to the Base Control chassis just described. The Output Control chassis contains six triggers which are associated with Sort, Set, and Trip operations and may be regarded as the functional equivalents of the step triggers ( )ES described earlier in connection with the Step Sequence chassis.

Trigger **EGC1** is in effect the "step trigger" for the Sort I operation and is turned on when that operation is called for. Similarly **EGC2** is associated with Sort II, **ELC1** with Set I, **ELC2** with Set II, **EPC1** with Trip I and **EPC2** with Trip II. Each of these triggers is turned on by the output of an associated diode gate; for example, **EGC1** is turned on through the left side of EGCD whenever the potential at terminal **6** is lowered and a negative ESI pulse arrives at terminal **10.** The ESI pulse occurs at the completion of each program step or output operation and is fed in common to each of the six gates controlling the output operation triggers. The other inputs to each of the gates (e.g. the terminal **6** input to the left side of EGCD) come from the "next step" or "to" busses energized by the "from" terminals of the plugboard. Thus, whenever a given program step or output operation is completed and the plugboard connections call for the next step to be a Sort, Set, or Trip operation, the appropriate output operation "step trigger" will be turned on through its associated input gate by the ESI pulse.

In addition to raising the potential at the appropriate Base Control chassis terminal to initiate the operation, the operation step triggers also deliver a lowered potential to their respective "from" terminals on the plugboard so that the next following program step or output operation may be selected. For example, when **EGC1** is on, indicating that a Sort I operation is to be performed, the raised potential at the left plate of **EGC1** is inverted in the left side of EGCB and delivered to the Sort I "from" terminal on the plugboard via chassis terminal **7,** so that the next program step or output operation may be selected. Also, the raised left plate potential at **EGC1** is delivered through a resistor in **EFP1** to the Base Control chassis via terminal **1** to fire the Sort I thyratron. Each of the other five output operation step triggers **EGC2, ELC1, ELC2, EPC1,** and **EPC2** serve the same functions in the same way for their respective output operations.

The Sort II, Set I, Set II, Trip I, and Trip II signals from the "to" terminals of the plugboard arrive at the Output Control chassis at terminals **4, 16, 14, 22** and **20** respectively. In the same order, the signals to the "from" terminals of the plugboard depart over terminals **5, 15,** and **13** (no "from" signals are delivered for the Trip operations since they are always followed by the first program step on the next card). In the same order, signals to the Base Control chassis for firing the output operation thyratrons are delivered over terminals **9, 11, 17, 21** and **23.**

Three diode buffer stages **EAA, EAB,** and **EFP2** receive cathode potentials from the Sort, Set and Clear "to" terminals on the plugboard via chassis terminals **6, 4, 16, 14,** and **41** and deliver a lowered potential to the Step Control chassis over their common plate connections via terminal **19** when ever any of these output operations are in progress. This signal is used to inhibit the normal program step cycle which is not needed during output operations. The same inhibition is effected by triode buffer stage **EAC** (right plate) whenever a zero factor stop occurs (terminal **39** to common grids) or when a Trip I (right input) or Trip II (left input) occurs.

The Clear "to" terminal on the plugboard is connected to Output Control chassis terminal **41** so that terminal **41** will be lowered in potential whenever a Clear operation is called for. In addition to lowering terminal **19** through the right side of **EFP2** as previously explained, the reduced potential at terminal **41** also raises the storage clearing potential at terminal **34** through ENCD and enables the right gate of ENCD so that the next step advance pulse **ES1** (over terminal **10**) will actuate flip-flop ECF. The resulting raised potential at the left plate of ECF is inverted in the left side of ECG and delivered to the Clear "from" terminal on the plugboard via chassis terminal **43** to energize the next step "from" terminal through the plugboard connection.

When ECF returns to normal the positive pulse at its right plate is inverted and amplified in the right side of ECG and delivered to the Step Control chassis (terminal **32**) via chassis terminal **25** to initiate the step advance cycle.

The ENC trigger is actuated by a reduced potential at terminal **35** through the left diode of ENCD. Terminal **35** is connected to the non-calculate switch which lowers the potential at terminal **35** whenever there is no card in the sensing station and whenever a card control hole indicates that the card should not be calculated. When either of these conditions causes ENC to be turned on, the potential at terminal **33** is raised to initiate a Trip I operation as explained earlier in connection with the Base Control chassis.

When a zero factor occurs during a division step and

the zero factor selector switch is set for "reject," the potential at terminal 37 of the Output Control chassis is raised and as a result, trigger EGP is turned on through the left side of EGϕ. The resulting raised potential at the left plate of EGP is delivered to terminal 29 and from there to the Base Control chassis to initiate the firing of the Sort I and Trip I thyratrons, thus causing the card to be rejected and the program on the next card begun.

STEP CONTROL CHASSIS

The Step Control chassis shown in Fig. 29 performs the general function of advancing the machine from step to step during the execution of a program. The chassis that control the machine during output operations and Clear operations (Base Control and Output Control chassis) have just been explained. The chassis that control the machine during the program steps will be explained later.

Referring now to Fig. 29, the Step Control chassis delivers ESZ and ESI pulses from terminals 33 and 35 to the Step Sequence chassis previously described. Recall that the ESZ pulse turns off whichever step trigger was on and the ESI pulse turns on another step trigger depending upon the algebraic sign of the result of the step just completed. The ESZ pulse (negative) is developed by stages ESZ and EP' in parallel whenever either the left or right capacitive inputs to ESZ are pulsed positively. The ESI pulse (negative) is developed by stages ESI1, ESI2, and EPX' in parallel whenever either the left or right capacitive inputs to ESI1 are pulsed positively.

The left and right sides of ESZA deliver positive pulses to the left and right capacitive inputs to ESZ to cause ESZ pulses and the left and right sides of ESIA deliver positive pulses to the left and right capacitive inputs to ESI1 to cause ESI pulses. Consider now how and when negative pulses are applied to the inputs to ESZA and ESIA to cause ESZ and ESI pulses.

A program is initiated by a negative swing at terminal 24 from the start and restart switches. This swing actuates flip-flop EP. The positive swing at the left plate of EP is inverted in the right side of ESB1 to actuate flip-flop ESD. The resulting negative pulse at the right plate of ESD is delivered to the right capacitive input to ESZA to cause an ESZ pulse at terminal 33. The positive swing at the left plate of ESD when ESD is actuated is inverted in the left side of ESB1 and delivered as a negative pulse from terminal 37 to the Step Sequence chassis to enable the step trigger associated with the first program step. The positive swing at the left plate of ESD is also delivered via terminal 30 to the Zero Factor chassis, and inverted and amplified in the right side of ESZ1. The resulting negative pulse at the common plates of ESZ1 is delivered to the left input to ESZA and the right input to ESIA to cause ESZ and ESI pulses and is also delivered via terminal 44 to the Control chassis to initiate a step cycle. The negative swing at the right plate of ESD when ESD is actuated pulses the right side of ESZA at the same time the left side is being pulsed through ESZ1. Recall, however, that pulsing either side of ESZA negatively will cause the ESZ pulse to zeroize step triggers.

When ESD returns left the negative swing at its left plate causes the ESI pulse at terminal 36. This pulse turns on the step trigger for the first program step the gate to which was previously enabled via terminal 37 by the left side of ESB1. The signal (from the left plate of EP) that actuates ESD through ESB1 also is delivered to the right input to ESZ2 to cause a negative pulse at terminal 28. This pulse is delivered to the Output Control chassis and serves to turn off any output operation trigger that was on.

Summarizing the foregoing, the net result of actuating flip-flop EP is seen to be as follows: Any output operation triggers that were on are turned off by a negative pulse at terminal 28. The step trigger for the first program step has its gate enabled over terminal 37 so that it will be turned on by the next ESI pulse. Any step trigger that was on is turned off by an ESZ pulse over terminal 33. Finally an ESI pulse over terminal 35 causes the step trigger for the first program step to be turned on. Also a negative pulse is delivered over terminal 44 to the Control chassis to initiate program step operations.

The first step in a program is initiated by flip-flop EP as described above. Subsequent steps are initiated by flip-flop EGD, in a manner now to be explained. EGD is actuated after the successful completion of any program step or output operation. When a program step (add, subtract, multiply or divide) has been successfully completed and proven the right plate of EGD is pulsed negatively through the right side of EG by a positive pulse over terminal 42 from the Control chassis (enabled by a raised potential over terminal 36 from the Zero Factor chassis). After an output operation (Set, Sort, or Trip) the right capacitive input to flip-flop EGD is pulsed negatively over terminal 26 from the Base Control chassis. After a Clear operation the right plate of EGD is negatively pulsed over terminal 32 from the Output Control chassis. Any of these three situation will cause EGD to be actuated and will result in a positive swing at the left plate of EGD. This positive swing is inverted and amplified in the left side of ESZ2 and delivered over terminal 28 to the Output Control chassis to turn off output operation triggers. The positive swing from the left plate of EGD is also inverted and amplified in the left side of ESZ1 to cause ESZ, ESI and a negative pulse over terminal 44 (to initiate step operations in the Control chassis) as was previously explained.

Potentials indicating the algebraic sign of a result are delivered to the plugboard from terminals 3 and 5 of the Step Control chassis. These terminals are connected to the minus result and plus result terminals of the plugboard respectively. Terminal 3 is lowered in potential by cathode follower EBM when a result is negative and terminal 5 is lowered by cathode follower EBP when a result is positive. EBM is controlled by the left plate of trigger EBS and EBP by the right plate. Trigger EBS is normally off (indicating a positive result) holding terminal 3 high and terminal 5 low. As long as result numbers are positive this condition obtains. When a result is negative the potential at terminal 38 (from the Zero Factor chassis) rises to enable the left side of EG and a positive pulse over terminal 40 (from the Decimal Control chassis) is inverted and passed to turn on trigger EBS. This reverses the relative potentials on terminals 3 and 5 to cause the next step to be the one plugged to follow a negative result.

The stages of the Step Control chassis that remain to be described constitute a recycling control which causes the calculator to restart either the step or the entire program whenever for any reason a step is not successfully completed and proved within an allotted time.

Trigger EP3 is turned on at the beginning of each calculation of flip-flop EP through the right side of ESB1. This lowers the right input to EPX, cuts off conduction in EPX and permits a capacitor (located in EPX') connected between the plates of EPX and +150 volts to begin discharging. This capacitor is recharged at the beginning of each program step when flip-flop EP4 is actuated and the left side of EPX is consequently caused to conduct. Thus, as long as the program continues successfully the capacitor will not have time to become much discharged. Should the result of any step fail to prove, however, no "step completed" signal will arrive over terminal 36 and consequently no "step start" signal will be delivered from ESZ1 to actuate flip-flop EP4. When the capacitor in EPX' discharges sufficiently two neons in the plate circuit of EPX will conduct to deliver a positive pulse to both capacitive inputs to EPS. One or the other of the two sides of EP5 will be enabled to pass the pulse depending upon whether the restart switch is set to restart the step or to restart the entire problem.

If it is set to restart the step terminal 10 will be high and if it is set to restart the problem terminal 14 will be high.

In the first case (restart step) the negative pulse at the right plate of EP5 will have the same effect as the output from ESZ1, namely, to cause ESI, ESZ, initiate the step operations, (over terminal 44) and actuate EP4 to recharge the timing capacitor.

In the second case (restart problem) the negative pulse from the left plate of EP5 will actuate flip-flop EP to initiate the calculator operation at the first program step as previously explained.

CONTROL CHASSIS

The Control chassis shown in Fig. 18 performs basic control functions during the execution of any program step. An important control function performed by the Control chassis is that of selectively lowering the potentials on the EMK line (terminal 12), ESK line (terminal 14) and ERK line (terminal 16) to select the M'd, S'r, and Result storage locations as required during any program step. These three terminals are connected respectively with terminals 34, 32, and 31 of all 10 Step Sequence chassis and serve to enable the EMF, ESF and ERF gates in those chassis (by lowering cathode potential) as previously explained.

The enabling potentials at terminals 12, 14 and 16 of the Control chassis are delivered from cathode followers EMK, ESK and ERK respectively. The circuits delivering input signals to these cathode followers serve to lower the input potential to only one at a time. For example, the input to EMK is lowered only during those periods in a program step when it is desired to transfer the M'd from its storage location to the accumulator or when it is desired to transfer the M'd decimal location (or its complement) to the Decimal Counter.

Cathode followers EMK, ESK, and ERK are controlled mainly by the states of six triggers, EM, ES, ER, EPP, EPS, and EPM through D.C. amplifiers EMA, ESA, and ERA. The input to EMK is lowered only when either side of EMA conducts, the input to ESK is lowered only when either side of ESA conducts, and the input to ERK is lowered when either side of ERA or the left side of ERAZ conducts.

EMA conducts to lower the EMK line (terminal 12) whenevert rigger EM is on and whenever trigger EPP is on. ESA conducts to lower the ESK line (terminal 14) whenever trigger ES is on and whenever trigger EPS is on. ERA conducts to lower the ERK line (terminal 16) whenever trigger ER is on and whenever trigger EPM is on. The left side of ERAZ conducts to lower the ERK line whenever flip-flop EZ is in its actuated condition.

The left inputs to each of the six triggers EM, ES, ER, EPP, EPS, and EPM are coupled with the left plate of EPG, the right plate of EMDC and terminal 34, so that a negative pulse at any of these points will turn off all of the above triggers. This negative pulse to turn off the triggers will occur whenever a positive pulse arrives at terminal 27 (from the Decimal Control chassis) or when a negative pulse arrives at terminal 34 from the Decimal Control chassis, or when flip-flop EMDZ returns left after being actuated. The significance of these conditions will be understood after reading the subsequent description of the sequence of operations and signals during each of the four types of program steps.

Trigger EM is turned on by the negative swing on the left plate of flip-flop EZ when EZ returns left after being actuated at the beginning of each program step. Note that while EZ is actuated the raised potential at its left plate lowers the ERK line (for selecting the result storage location to be zeroized). When EM is turned off the negative swing at its left plate turns on ES. ER is turned on by a negative pulse over terminal 18 from the Zero Factor chassis. When ER is turned off the negative swing at its left plate actuates flip-flop EPZ and the negative swing at the left plate of EPZ when EPZ returns left turns on EPM. When EPM is turned off, the negative swing at its left plate turns on EPS and when EPS is turned off the negative swing at its left plate turns on EPP. Thus it is seen that the triggers EM, ES, ER, EPM, EPS and EPP, which may be regarded as storage selection triggers, are turned on one at a time in sequence during a program step, so that the EMK, ESK, and ERK enabling lines to the Step Sequence chassis will be lowered in potential at appropriate times during a step.

Another important function of the Control chassis is the generation of zeroizing or clearing pulses for triggers throughout the calculator. The B5 clearing pulse is delivered from terminal 39 and the B2 clearing pulse from terminal 42. The B5 pulse is generated at the beginning of each program step and it sets the M section of the accumulator to zero and turns off many other triggers throughout the calculator. The B2 pulse is generated at the beginning of each program step and just before the proof portion of each program step and it sets only the A section of the accumulator to zero. B5 is generated each time flip-flop EZB5 is actuated and B2 is generated each time flip-flop EZB2 is actuated.

Flip-flop EZB5 is actuated by a negative pulse over terminal 22 from the Step Control chassis; this negative pulse also actuates flip-flop EZ and occurs at the beginning of each program step. Flip-flop EZB2 is actuated by a negative pulse at the common plates of pulse amplifier EZG. The left plate of EZG conducts to actuate EZB2 whenever EZB5 is actuated and the right plate of EZG conducts to actuate EZB2 whenever flip-flop EPZ is actuated (at the beginning of each proof operation). EZB2 is also actuated each time ECS conducts, i.e., when flip-flop EMDZ is actuated (during multiplication and division, on positive signal over terminal 38 from Multiplication-Division chassis).

Since both the B5 line (terminal 39) and the B2 line (terminal 42) are connected to many triggers throughout the machine, it is important that the potential on these lines be carefully regulated in order to prevent spurious clearing of triggers. Regulation of the B5 line, as well as the generation of the positive B5 pulse, is performed by the left side of ZB52, and both sides of ZBB5, ZBA5, and the regulator stage ZB5 in the Regulator chassis. The plates of ZB5 are connected to terminal 39 of the Control chassis and the grids of ZB5 are connected to terminal 43 of the Control chassis. Regulation of the B2 line and generation of the B2 pulse are performed by the right side of ZB52 and both sides of ZBB2, ZBA2, and regulator stage ZB2 (connected between terminals 42 and 45 of the Control chassis). Since the regulating circuits for B2 are identical with those for B5, only those for B5 will be described in detail.

The left plate of ZB52 is supplied through resistors in ZBB5 (between connections 4 and 8) by the B5 line (terminal 39). The right grid of ZBB5 is connected to a point between these resistors so that the right side of ZBB5 will conduct more heavily if the B5 line rises and will conduct less if the B5 line drops. The resulting fall and rise at the right plate of ZBB5 controls the right grid of ZBA5 and the resulting rise and fall at the right plate of ZBA5 controls the grids of Regulator stage ZB5 in the Regulator chassis (over terminal 43). Thus, if the B5 line potential rises above its normal value the right side of ZBB5 will conduct more, the right side of ZBA5 will consequently conduct less, and ZB5 will consequently conduct more to lower the B5 line potential to its normal value. The reverse occurs if the B5 line potential falls below its normal value.

The left sides of ZBB5 and ZBA5 serve to increase the sensitivity of the regulators by counteracting the tendency of the cathodes of ZBB5 and ZBA5 to follow the rises and falls of the right grid potentials as much as would otherwise be the case. For example, the current

through the common cathode resistor of ZBB5 consists of a component from both the right and left halves of ZBB5. When the B5 line rises above its normal value and conduction is consequently increased in the right side of ZBB5 the cathode potential rises due to the increased current. Any rise, however, tends to diminish the current in the left side of ZBB5 and consequently prevents the cathode from rising as much as it otherwise would. Thus, the right side of ZBB2 will be more sensitive to changes in grid potential than it would be without the cathode regulation provided by the left side.

When EZB5 is actuated to produce the B5 pulse, the positive swing at the left plate of EZB5 causes increased conduction in the left side of ZB52. This in turn reduces conduction in the right side of ZBB5, increases conduction in the right side of ZBA5 and consequently reduces the grid potential on Regulator stage ZB5. The sharply reduced conduction in ZB5 raises its plate potential to deliver a B5 pulse.

As previously stated the regulating circuits for the B2 line are identical with those for the B5 line just described.

The stages in the Control chassis that remain to be described perform functions that will best be understood when the sequence of control signals during the four types of program steps is explained. Their general function and relationship to the other parts of the Control chassis will be described now, however.

Stage ECB2 is a cathode follower that serves to block carries from accumulator order 11M during the proof process. It delivers a reduced potential to terminal 37 whenever the trigger EPP is on (during the proof process). Its input potential is received from the left plate of ECB1 which also lowers the potential at terminal 15 during the proof process.

Flip-flop PAMD is actuated through diode gates ENM and ENM1 whenever either the EM, ES, EPM, EPS, or EPP triggers are turned on. The output from the right plate of PAMD is gated to terminal 24 by the left side of EZS through the right side of ERAZ. The left side of EZS is enabled (over terminal 29) only when a negative number is being operated upon.

Flip-flop PAD, trigger EϕCT and diode gates EϕC perform functions related to the zero check after proof subtraction. The CX pulse occurring after each number registration is applied from terminal 20 to the right and left pulse inputs to EϕC. The left side of EϕC is enabled when trigger EϕCT is on and the right side is enabled when trigger EPP is on. The output from the common plates of EϕC actuates flip-flop PAD. When PAD returns left after being actuated, it delivers a positive pulse via terminal 7 to the Step Control chassis (terminal 42) and a negative actuating pulse to turn on trigger EϕCT. When trigger EϕCT is on, its left plate raises the potential at terminal 5. The significance of these signals will be understood later when the zero check operation is explained.

Stage EPZC contains the time constant capacitors for flip-flops EZ, EPZ, and EMDZ and also contains a pair of clamping triodes with a common grid connection coupled (through ERAZ) with the output from flip-flop EZ. When EZ is actuated the clamping triodes conduct to prevent actuation of EPZ and to block the right side of EZG. The EPZC grid potential is also delivered over terminal 32 to a number of similar clamping triodes in other chassis to prevent spurious actuation of flip-flops during zeroizing cycles (B5 and B2).

OPERATION DURING EXECUTION OF PROGRAM STEPS

The sequence of control signals during arithmetic operations is described in the following sections. Stages are referred to by their abbreviated designations; details of stages and interconnections between stages may be found in the stage schematics and block schematics through an initial reference to the Alphabetical Stage Index.

Minidend registration.—The sequence of control signals during minidend registration is illustrated in Fig. 59. This sequence is the same for all four types of program steps.

The negative start pulse (1) from the Step Control kicks EZ right; EZ going right kicks EZB5 right. EZ, through ERAZ, pulls ERK down to indicate, through the plugboard and Keyboard Bias, which Storage is to be zeroized. EZB5 produces the B5 zeroize pulse (2) through regulator stages ZBB5, ZBA5 and ZB5. EZB5 initiates the B2 zeroize pulse (2) through the left side of EZG. EZB2, ZB52, ZBB2, ZBA2, and ZB2 are the regulator stages for B2. When EZB5 returns left, the negative pulse from its left plate produces a positive pulse through EPG and, through MZK, kicks the appropriate zeroize flip-flop (3) to clear the Storage indicated by the keyboard bias. EZB5 returning left also operates the guard flip-flop EMZ for clearing of storage. When EZ returns left, it kicks EM right. EM going right pulls the EMK line down through EMA and EMK, and pulls DMP right. The EMK line selects, through the plugboard and keyboard bias, the M'd factor. DMP going right opens the left side of gate DMG and raises the left input of PSA through EIA3. DMP also pulls DEM right through DMD to set decimal complement biases and call for decimal registration (4) through DEA1. The end of decimal registration, indicated by a positive pulse from the right plate of DP–16, kicks DRB right through DIC DA1–16, and the left side of DMG. DRB going right unclamps PSA (5) through PSAC to raise the sign bias (6) and call for a cycle of RIG (7). After the carries have been called for and satisfied, the CX pulse (8) kicks DRB left, which gives a control pulse (9) through EPG. This returns EM and brings ES right.

Addition and subtraction.—The sequence of control signals during addition and subtraction is illustrated in Fig. 60.

The return of DRB produces a positive pulse at the left grid of EPG (1), and a negative pulse on the control ring common line, to return EM and kick ES right. The left plate of ES raises the left grid of ESA to drop the grids of ESK and the ESK line, to select, through the plugboard and Keyboard Bias, the S'r factor. The right plate of ES also drops the grids of EP1 and EP2 (2). In addition, this allows the left plate of EIA to rise and bring up, through EIA2, the left input of PSA. In Subtraction, the left plate of EIS rises to bring up, through EIS2, the right input of PSA. The rise of the left plate of either EIA or EIS opens, through EIA2 or EIS2, the left side of DPG2 and produces a pulse at the left input of amplifier DEA2, initiating a cycle of DEA and a decimal registration is indicated by the positive pulse from the right plate of DP16, which, through DIC amplifier DA1–16 and gate DPG–2, kicks DAX right. DAX going right kicks DAS right. The left plate of DAS raises, through SI–2, the left input of multivibrator SM (3), to produce shift pulses through SMG, SMA, SG, and cathode follower SK1, SK2, SK3. Decimal alignment is indicated by the return of DC16 kicking DCC right which kicks DAS left to stop SM, and kick DAM right through the right side of DG which is held open by LP–ECB1. The left plate of DAM pulls DEM right to lower cathodes of decimal complement gates through DBC and initiate decimal registration through DEA1. The end of decimal registration is indicated by the right plate of DP16 through DIC, DA1–16 and DPG2, to return DAM and DAX to the left. DAM going left kicks DRB right to unclamp the grids of PSA through PSAC (4). In addition, this allows the left grid to conduct. In subtraction, the right grid conducts. The state of PSA, in conjunction with PAM, determines the sign biases for the Accumulator. The raising of either the + or — bias to the A section of the Accumulator,

(5), drops the common plate line of RB to produce an RIG cycle (6). After carries are satisfied, the CX pulse (7), returns DRB to the left, dropping the sign biases and producing, through EPG, a control pulse (8).

The control pulse returns ES to the left. The positive pulse from RP–ES goes through the right or left side of MC1 depending on the state of PAC. If the result is positive PAC is on the left, opening the right side of MC1 allowing ER to be kicked right. ϕC1 is also kicked right but ϕC2 is closed so it has no effect. If the result is minus PAC will be on the right and the complementizing process takes place. ER, through ERA and ERK, drops the ERK line, to select, through the plugboard and Keyboard Bias, the Storage position for the Result. ER also brings DRP to the right (9), which calls for decimal registration through DPG1 to DEA, and opens the right side of gate DMG. At the end of decimal registration, the pulse from the right plate of DP16, via DIC DA1–16 and DMG, kicks DRS to the right. This calls for shifts through SI–2 (10). Decimal alignment is indicated by the left plate of DC16 kicking DCC right which returns DRS to the left to stop shifting, and kick MST right. The plates of MSI go high only when EMZ has returned left and MST on the right. Thus a positive pulse occurs at the plates of MSI coincident with the latter of these events, which may occur in either order. The positive pulse from MSI is inverted by MSA, and kicks MZT right. The positive pulse from LP–MZT in inverted in MZR to lower the LP–PSA to raise the — bias in all sections and call for an RIG. This RIG will add a number into the accumulators should the storages not be cleared correctly. The CX pulse at the end of the RIG kicks MBZ left to kick MS right. MS going right registers the Result (11) in the Storage position indicated by the ERK line through the plugboard and Keyboard Bias. MS going right also provides a pulse to set, when required, the negative indication trigger EBS through the left side of EG. MS returning to the left provides, through the right side of amplifier DPG2, a pulse to advance the control ring from ER to EPZ (12). As EPZ goes right it initiates EZB2 through amplifier EZG.

ZB2 provides the zeroize pulse to the B2 line (13). After EZB2 returns, the remainder of EPZ allows all circuits time to stabilize. The return of EPZ kicks EPM right. EPM, through ERA and ERK, again drops the ERK line to select, through the plugboard and Keyboard Bias, the Proof M'd (Result). EPM also initiates a decimal complement registration (14) through EPMA, DMP, DMD, DEM, and DEA1. DMP also opens the left side of gate DMG and raises the left input of PSA through EIA3 to prepare the sign bias stages. DEM also sets the decimal input gates for a complement registration. At the end of decimal registration, the negative pulse from the left plate of DP16 kicks DRB right through DA1–16 and DMG. DRB, through PSAC (15), allows the sign biases to rise (16), and initiate a cycle of RIG (17). After carries have been satisfied, the CX pulse (18) returns DRB to the left. DRB going left produces, through RPG, a control ring pulse (19). EPM going left kicks EPS right. EPS, through ESA and ESK, drops the ESK line to select, through the plugboard the Keyboard Bias, the Proof S'r (S'r). The right plate of EPS drops the grids of EPP1 and EPP2 (20). In Proof of Addition, this allows the right plate of EIA to rise and bring up, through EIS1, the right input of PSA. In Proof of Subtraction, the right plate of EIS rises to bring up, through EIA1, the left input of PSA. The rise of the right plate of either EIA or EIS opens, through EIA1 or EIS1, the left side of gate DPG2 and produces a pulse at the left input of amplifier DEA2, initiating a cycle of DEA and a decimal registration. Completion of the decimal registration is indicated by the negative pulse from the left plate of DP16, which, through amplifier DA1–16 and gate DPG2, kicks DAX right. DAX going right kicks DAS right. The left plate of DAS raises, through SI–2, the left input of multivibrator SM (21) to produce shift pulses through SMG, SMA, SG, and SK1, SK2, SK3. Decimal alignment is indicated by the return of DC16 kicking DCC right which kicks DAS left to stop SM and kick DAM right. The left plate of DAM raises the left side of DEM to lower cathodes of decimal complement gates through DBC and initiate decimal registration through DEA1.

The end of decimal registration, as indicated by the right plate of DP16, through DIC amplifier DA1–16 and DPG2, returns DAX and DAM to the left. DAM going left kicks DRB right to unclamp the grids of PSA, through PSAC (22). In Proof of Addition, this allows the right grid to conduct. In Proof of Subtraction, the left grid conducts. The state of PSA, in conjunction with PAM, determines the sign biases for the Accumulator. The raising of either the + or — bias (23) to the A section of the Accumulator drops the common plate line of RB to produce an RIG cycle (24). After carries have been satisfied, the CX pulse (25) returns DRB to the left, dropping the sign biases, and producing, through EPG, a control pulse (26). This returns EPS to the left, which kicks EPP right. The left plate of EPP, through ECB1, EMA and EMK drop the EMK line to select, through the plugboard and Keyboard Bias, the M'd for the Proof Subtraction. EPP also blocks carries out of 11M through ECB1 and ECB2 and, through the right side of ECB1, opens left side of gate DG, and, through EPPM, raises the right input of PSA, opens gate DPG2, and provides a pulse to DEA2 to initiate decimal registration (27). The end of decimal registration, indicated by a positive pulse from the right plate of DP16, via DIC DA1–16 and DPG2, kicks DAX right, which kicks DAS right to start shifting through SI–2 (28). Decimal alignment, indicated by a negative pulse from the left plate of DC16 kicking DCC right returns DAS to the left. DAS going left stops shifting and kicks DRB right, through the left side of DG. DRB going right unclamps PSA through PSAC (29) to allow sign biases to rise (30) and initiate a cycle of RIG (31). After carries have been satisfied, the CX pulse (32) returns DRB left to provide a control pulse through EPG (33). The control pulse returns EPP left.

Multiplication.—The sequence of control signals during multiplication is illustrated in Fig. 61.

The return of DRB produces a positive pulse at Left Grid-EPG (1) and then a negative on the common control ring line, returning EM which, kicks ES right. The left Plate of ES raises the Left Grid of ESA to drop grids of ESK and the ESK line to select, through the plugboard and keyboard bias, subvisor factor. The right plate of ES drops the grids of EP1 and EP2 (2). In multiplication, this allows the left plate of EIM to rise. Through EIM1 this opens the left side of gate DPG1, raises the right input of DMD and pulls PMP right. DMD pulls DEM right to set decimal complement biases and initiate a decimal registration through DEA1. At the end of subvisor decimal registration the return of DP16, thru DIC, DA1–16, and DPG–1 kicks DK to the right to set biases for the registration of the multiplication division decimal constant of 17. At the same time, DK going right initiates that registration through DEA1. The completion of this registration is signalled through DA1–16 and DPG1 again to return DK to the left. DK, going left, provides a pulse through PMM to kick PMD2 right (3). The return of PMD2 to the left kicks PM1 right to call for shifting through SI–1 (4). When PMP was pulled right above, it lowered the cathode control line on PGMD through PSG and PSGK and opened gates PMG–R, PDX–R, PDMS–R and PZG–R. The gate PGMD–L is now open, since its cathode is held low by PSG and its grid returns high from PDB, which is now on the left. The counter PC1 through PC16 will now count the shifts of the minidend until 11 have been made. At this time, the counter drops the cathode of the stop-

shift gate PDMS through P11G by kicking P11S right. The right grid of PDMS being high, as indicated above, the next 11M number indications from PMS and PMφ (5) will stop shifting by returning PM1 left through PDMS. At the same time that the counter opens the stop-shift gate, it kicks PDB right to close the left side of gate PGMD to prevent further shifts from being counted. When the number indication from 11M occurs it produces a pulse at the grids of PDMS and the RG of PDX through PMS and PMφ. This stops shifting as described above and returns PDB to the left to reopen the left side of gate PGMD, and allow further shifts to be counted.

When PM1 goes left, above, the positive pulse from its RP, through the right side of PMG, kicks PMD1 right. The positive pulse from the LP–PMD1 through MPG kicks PMBT right. This opens the right side of gate PM12 so that the return of PMD1 will through left side PDM3 and PM12, kick PM2 right. PM2 going right opens the left side of gate PMDR and the right side of 11—11 and drops the left grid of PM23 to raise the input of BA+1 (6) to raise the + bias in the A section, + bias in the M section except 11M, and — bias in 11M (7). This initiates an RIG (8). The CX pulse (9) following the first subvisor registration kicks PM3 right. The return of PM3, through negative amplifier PM23 and PMDR, calls for (10) another RIG (11) thru LS–PMDR and RS. We will assume that the left hand digit of the minidend is a 2, in which case, this second registration reduces 11M to zero, as indicated by PMφ going right (12). CX again kicks PM3 right (13). The positive pulse from LP of PM3, through the left side of gate PM12, which is opened by the left plate of PMφ, kicks PM2 left and drops the accumulator biases through BA–1. PM2 going left also kicks PMD2 right through PMM. The return of PMD2 kicks PM1 right to call for shifts through SI–1 (14). The next number indication from 11M (15) allows PMφ to go left to kick PM1 left again through the right side of PDMS. When PM1 goes left, above, the positive pulse from its RP, through the right side of PMG, kicks PMD1 right. The return of PMD1 will through the left side PDM3 and the right side of PM12 (held open by PMBT), kick PM2 right. PM2 going right opens the left side of gate PMDR and the right side of 11—11 and drops the grid of PM23 to raise the left side of BA+1 (16) to raise the — bias in the A section, + bias in the M section except 11M, and — bias in 11M (17). This initiates an RIG(18). The CX pulse (19) following the first subvisor registration kicks PM3 right. The return of PM3, through amplifier PM23 and PMDR, calls for (20) another RIG (21) directly through RS.

We have assumed the second digit also to be a 2 so that 11M is again reduced to zero (22), followed by the CX pulse (23), and further shifting (24). This process is repeated until the shift counter reaches 22. When PC16 goes left to indicate the count of 22 its left plate kicks PMBT left, PMDZ right, and closes the left side of gate PMG. The next number indication from PMφ (25) again stops shifting as described above, but this time, since the left side of PMG is now closed, PMBT is not kicked right. This prevents the raising of the accumulator biases and calling for RIG which would normally occur. PMφ going left also kicks PMφD right, through RS–PZG. The return of PMφD to the left kicks PMDZ left. PMDZ going left kicks EMDZ through EMDC (26) to produce a B2 pulse (27) to zeroize the A section. The return of EMDZ produces, through EMDC, a step pulse to return ES. The positive pulse from RP–ES goes through the right or left side of MC1 depending on the state of PAC. If the result is positive PAC is on the left opening the right side of MC1 allowing ER to be kicked right. φC1 is also kicked right but φC2 is closed so it has no effect. If the result is minus PAC will be on the right and the complementizing process takes place. ER, through ERA and ERK, drops the ERK line, to select, through the plugboard and Keyboard Bias, the Storage position for the Result. ER also brings DRP to the right (28), which calls for decimal registration through DPG1 to DEA, and opens the right side of gate DMG. At the end of decimal registration, the pulse from the left plate of DP16, through DA1–16 and DMG, kicks DRS to the right. This calls for shifts through SI–2. (29). Decimal alignment is indicated by the left plate of DC16 kicking DCC right which returns DRS to the left to stop shifting, and kick MST on the right. Thus a positive pulse occurs at the plates of MSI coincident with the latter, of these events, which may occur in either order.

The positive pulse from MSI is inverted by MSA, and kicks MZT right. The positive pulse from LP–MZT is inverted in MZR to lower the LP–PSA to raise the — bias in all sections and call for an RIG. This RIG will add a number into the accumulators should the storages not be cleared correctly. The CX pulse at the end of the RIG kicks MZT left to kick the MS right. MS going right registers the Result (30) in the Storage position indicated by the ERK line through the plugboard and Keyboard Bias. MS going right also provides a pulse to set, when required, the negative indication trigger EBS thru the left side of EG. MS returning to the left provides, through the right side of amplifier DPG2, a pulse to advance the control ring from ER to EPZ (31). As EPZ goes right it initiates EZB2 through amplifier EZG. ZB2 provides the zeroize pulse to the B2 line (32). After EZB2 returns, the remainder of EPZ allows all circuits time to stabilize. The pulse from the left plate of EPZ kicks EPM right. EPM, through ERA and ERK, again drops the ERK line to select, through the plugboard and Keyboard Bias, the proof M'd (Result). EPM also initiates a decimal complement registration (33) through EPMA, DMP, DMD, DEM, and DEA1. DMP also opens the left side of gate DMG and raises the left input of PSA through EIA3 to prepare the sign bias stages. DEM also sets the decimal registration, the positive pulse from the right plate of DP16 kicks DRB right thru DIC, DA1–16, and DMG. DRB through PSAC (34) allows the sign biases to rise (35) and initiate a cycle of RIG (36). After carries have been satisfied, the CX pulse (37) returns DRB to the left. DRB going left produces, through EPG, a control pulse (38). This pulse returns EPM, which brings EPS right. With EPS right the proof of Multiplication, division, takes place. This is similar to the write up for division except for being initiated thru diode mixer stage EID1 instead of EID2.

Division.—The sequence of control signals during division is illustrated in Fig. 62.

The return of DRB produces a positive pulse on the LG–EPG (1) and a negative of the control ring line, returning EM, which kicks ES right. The LP of ES raises the LG of ESA to drop the grids of ESK and the ESK line to select through the plugboard and keyboard bias, the subvisor factor. The RP of ES drops the grids of EP1 and EP2. In division, this allows the LP of EID to rise. This opens the left side of DPG1 through EID2 and through EID2 pulls PDP right, and initiates a decimal registration through DEA2 (2). The end of decimal registration is indicated by the rise of the LP–DP16 which kicks DK right via DIC DA1–16 and DPG1. DK going right sets decimal biases to allow entering the decimal constant of 17, and initiates a decimal registration through DEA1. The end of this registration kicks DK left again via DIC, DA1–16 and DPG1. DK going left kicks PMD2 right through PMM (3). The return of PMD2 to the left kicks PM1 right to call for shifts through SI–1 (4). When PDP was pulled right above, it lowered the cathode control line on PGMD through PSG and PSGK and opened the left side of gate PDMS. The left side of gate PGMD is now open, since its cathode is held low by PSG and its grid held high by PDB, which is on the left. The counter PC1 through PC16 will now count shifts until 11 have been made. At this time, the counter drops

the cathode of the stop shift gate PDMS through P11G. The left grid of PDMS being high, as indicated above, the next 11M number indication (5) will kick PDN right through the left side of PDMS. PDN going right kicks PM1 left through the right side of PCG to stop shifts. The 11M number indications, through PDMS, also kicks PDND right. PDN going right supplies, through the right side of PGMD, the extra pulse to the shift counter necessary to insure the proper number of shifts, to complete division. PDND returning left kicks PD1 right through the right side of PDM.

PD1 going right drops the right input of PDA to raise the left input of BM+1 (6) and raise the — bias in the A section and the + bias in the M section M (7). PD1 also, through PDIM, opens the odd line gate to 1M, I1–11 through PX. The rise of the A section bias initiates an RIG cycle (8). The first subvisor registration in division will always produce an overcarry (except in case of a zero subvisor). The overcarry indication from the RP–11AC thru PS11 (9), kicks PDS right. The CX pulse (10) then kicks PM3 right. PM3 going right kicks PDS left again. PDS going left, kicks PD1 left, which kicks PD2 right. PD1 going left drops the accumulator biases through PDA. PD2 going right drops the left side of PDA to raise the input of B11–1 (11) to raise the + bias in the A section and the — bias in the M section (12). Again the rise of the A section bias starts the RIG (13) to remove the result of the first trial registration. Another overcarry (14) will result, to kick PDS right again. CX (15) again returns PDS left, which kicks PD2 left. PD2 going left kicks PD2D right. The return of PD2D kicks PD3 right through the left side of PDM and right side of PDM3. The left side of PDM is held open by PC16 of the M–D counter, and is open from counts 6 through 22. PD3 going right calls for shifts through SI–1 (16). The first shift pulse, from LP–SG kicks PD3 left again to stop shifting. PD3 going left kicks PD1 right again. PD1 going right drops the right input of PDA to raise the input of BM+1 (17) and raise the — bias in the A section and the + bias in the M section (18). PD1 also, through PD1M, opens the odd line gate to 1M, I1–11 through PX. The rise of the A section bias initiates the RIG cycle (19). This trial subtraction may be successful in which case no overcarry will result. This is the assumption made here.

In this case the CX (20) pulse again kicks PM3 is initiated in the right side of PM23 to call for (21) another RIG (22) through the right side of PMDR and RS, the right side of PMDR being held open by PD1. At the same time, the pulse from PM23 kicks PDB left through the left side of gate PGMD to allow further shifts to be counted in PC1–16. We will assume that this RIG has produced an overcarry. The overcarry indication from the RP–11AC thru PS11 (23), kicks PDS right. The CX pulse (24) then kicks PM3 right. PM3 going right kicks PDS left again. PDS going left, kicks PD1 left, which kicks PD2 right. PD1 going left drops the accumulator biases through PDA. PD2 going right drops the left side of PDA to raise the left input of B11+1 (25) to raise the — bias in the A section and the — bias in the M section (26). Again the rise of the A section bias starts the RIG (27) to remove the result of this unsuccessful registration. Another overcarry (28) will result, to kick PDS right again. CX (29) again returns PDS left, which kicks PD2 left. PD2 going left kicks PD2D right. The return of PD2D kicks PD3 right again through the left side of PDM and right side PDM3. The left side of PDM is held open by PC16 of the M–D counter, and is open from counts 6 through 22. PD3 going right calls for shifts through SI–1 (30). This process continues until the M–D counter reaches 22. This is indicated by the return of PC16 to the left. This closes the left side of gate PDM to prevent PD3 from being pulled right to call for further shifts. PC16 also opens the left side of gate PZG. When PD2D returns left after the S'r is added back this time, the pulse from its left plate goes through the left side of PZG, instead of PDM, to kick PMDZ left. PMDZ, going left kicks EMDZ right through EMDC (31) to produce a B2 pulse (32) to zeroize the A section.

The return of EMDZ produces, through EMDC, a step pulse to return ES. The positive pulse from RP–ES goes through the right or left side depending on the state of PAC. If the result is positive PAC is on the left opening the right side of MC1 allowing ER to be kicked right. ϕC1 is also kicked right but ϕC2 is closed so it has no effect. If the result is minus PAC will be on the right and the complementizing process takes place. ER, through ERA and ERK, drops the ERK line, to select, through the plugboard and Keyboard Bias, the Storage position for the Result. ER also brings DRP to the right (33), which calls for decimal registration through DPG1 to DEA, and opens the right side of gate DMG. At the end of decimal registration, the pulse from the left plate of DP16, through DA1—16 and DMG, kicks DRS to the right. This calls for shifts through DI–2 (34). Decimal alignment is indicated by the left plate of DC16, kicking DCC right which returns DRS to the left to stop shifting, and kick MST right. The plates of MSI go high only when EMZ is on the left and MST on the right. Thus a positive pulse occurs at the plates of MSI coincident with the latter of these events, which may occur in either order. The positive pulse from MSI is inverted by MSA, and kicks MZT right. The positive pulse from LP–MZT is inverted in MZR to lower the LP–PSA to raise the + Bias in all sections and call for an RIG. This RIG will add a number into the accumulators should the storages not be cleared correctly. The CX pulse at the end of the RIG kicks MZT left to kick MS right. MS going right registers the result (35) in the Storage position indicated by the ERK line through the plugboard and Keyboard Bias. MS going right also provides a pulse to set, when required, the negative indication trigger EBS through the left side of EG. MS returning to the left provides through the right side of amplifier DPG2, a pulse to advance the control ring from ER to EPZ (36).

As EPZ goes right it initiates EZB2 through amplifier EZG. ZB2 provides the zeroize pulse to the B2 line (37). After EZB2 returns, the remainder of EPZ allows all circuits time to stabilize. The pulse from the left plate of EPZ kicks EPM right. EPM, through ERA and ERK, again drops the ERK line to select, through the plugboard and Keyboard Bias, the Proof M'd (Result). EPM also initiates a decimal complement registration (38) through EPM*a*, DMP, DMD, DEM, and DEA1. DMP also opens the left side of gate DMG and raises the left input of PSA through EIA3 to prepare the sign bias stages. DEM also sets the decimal input gates for a complement registration. At the end of decimal registration, the positive pulse from the right plate of DP16 kicks DRB right through DIC, DA1–16, and DMG. DRB, through PSAC (39), allows the sign biases to rise (40), and initiate a cycle of RIG (41). After carries have been satisfied, the CX pulse (42) returns DRB to the left. DRB going left produces, through EPG, a control ring pulse (43). This pulse returns EPM, which brings EPS right. With EPS right the proof of division, multiplication with the exception that the program is initiated through the diode mixer stage EIM2 instead of through diode mixer stage EIM1 as in the original multiplication write up.

PROGRAM BRANCHING

The method by which program branching is accomplished is described in the following paragraphs which refer to Fig. 41. The description is in terms of a typical example which would be set-up by plugging as follows:

Plug "Start" to step 1
Step 1:
If result is plus go to step 2
If result is minus go to step 39

Step 39:
If result is plus go to step 40
If result is minus go to step 1
Step 40:
If result is plus go to step set I
If result is minus go to step set II
Step 2: If result is plus go to step Trip II
Set I: Go to Trip I
Set II: Go to step 2

The start switch kicks EP right to give only one pulse per closing should contact bounce be present. The left plate of EP kicks ESD right thru the right side of ESB1. The left plate of ESD thru the left side of ESB1 lowers the start line, while the RP of ESD thru ESZA and ESZ pulses the LC points of all the step triggers 1 thru 40 ES. The LP of EP also produces ESZ2 to return all OCL triggers while ESZ returns any step triggers which may be on the right. (EZ is also kicked at this time to start calculation by left plate of ESD thru right side ESZ1.)

ESD returning to the left allows the start line to go high but the rise of all the step busses horizontal lines on the branching board is delayed by capacity loading. The Step busses when pulled down by the plugs to the branching board lines (verticals) open their respective diode gates ( ) ED, ELCD, EPCD and ECCD. The left plate of ESD thru the left side of ESIA passes a negative pulse ESI to all the diode step gates mentioned above, and since the left gate of (1, 2) ED is delayed in closing, the ESI pulse will pass to kick (1) ES right. The LP of (1) ES raises the left grids of (1,2) EBM and (1, 2) EBP (thru the divider of 1, 2 ESF).

When the calculation started by EZ reaches the point where the sign of the result is present the left bias of EG is set accordingly, left closed for a positive result and opened for a negative result. Assuming that the result is negative the cathodes of (1, 2) EBM thru (39, 40) EBM will be low, and since (1) ES is holding the left grid high, the step 39 bus will be pulled low by the left plate of (1, 2) EBM. This opens the left gate of (39, 40) ED.

If the calculation is completed correctly EGD will be kicked right thru the right side of EC. The right plate of EGD through EGDC, EGϕ, ESZA, and ESZ kicks (1) ES left, lowering the left grid of (1, 2) EBM allowing the left plate of (1, 2) EBM and the step 39 bus to rise (delayed by the capacity on the bus). EGD also, in going right, thru EGDC, EGϕ, ESIA, and ES1 produces the negative step advance pulse ESI on the step gates input capacitors. Since the left side of (39, 40) ED is delayed in closing the pulse will pass to kick (39) ES is right. The left plate of (39) ES raises the left grids of (39, 40) EBP and (39, 40) EBM thru the left divider of (39, 40) ESF. The lowering of the cathode of (39, 40) EBP or (39, 40) EBM by the sign of the result determines which step will be next (1 or 40). Assuming that the result is plus, step 40 is next. Step 40 is plugged on a plus result to Set I and it is assumed that the result of step 40 is plus. The step trigger (40) ES thru the right side of (39, 40) EBP thru the divider of (39, 40) ESF pulls down the left input of ELCD. The completion of step 40 causes an ESZ pulse to return (40) ES allowing the left input of ELCD to rise slowly. The ESI pulse occurs before the gate closes, therefore, ELC1 is kicked right.

ELC1 opens the left gate of ELCG and raises the left grid of ELCB to open the left gate of EPCD thru the branching board. When the ready switch has closed, the left gate of ELCG passes the next 60 cycle pulse from EGA which is properly phased to fire the Set I thyratron when its A.C. cathode potential is at its nega-

The sharp negative excuration of the thyratron plate when it fires feeds a negative pulse thru the right side of ETM2 to operate EGD via EBAL. EGD going right produces a negative pulse thru ESZ2 which returns ELC1 allowing the capacity loaded left bias of EPCD to rise. EGD going right also produces the step advancing pulse ES1 which passes thru the left side of EPCD, before it closes, to kick EPC1 right.

EPC1 when on the right opens the left gate of EPCG. The next 60 cycle pulse (provided that the ready switch is closed) passes thru the left side of EPCG to fire the "Trip I" thyratron. The firing of the thyratron pulses thru the right side of ETM4 to kick EP3 left which stops the automatic restart circuit. The "Trip I" thyratron also operates EGD via EBAL thru diode ETM1. EGD produces the step zeroize ESZ, ESZ2 and step advance ESI pulses again which return EPC1 left and complete the calculation since no other bus is pulled down.

If step 40 is plugged to Set II on a minus result and the result is minus the right side of ELCD is opened. The ESZ pulse returns the step 40 trigger (40) ES and the ES1 pulse passes thru the right side of ELCD to kick ELC2 right which raises the Set II bias at the right gate of ELCG. The "Set II" line is pulled down thru the right side of ELCB. The "Set II" thyratron fires and kicks EGD via EBAL again to return ELC2 to the left on the ESZ2 pulse and branch to step 2 on the ESI pulse.

Step 2 is shown plugged to the "Trip II" bus on both plus and minus results but could be plugged to continue calculation steps which use storage already used for "Set I" results it can further be used for calculation but cannot be used for both "Set I" and "Set II" on the same set-up. Likewise, if a storage is used for "Set II" it can be used for storage of intermediate results which may be held during the time of setting the I latches in the punch. A switch is provided which allows each storage to be placed on the "Set I" or "Set II."

If a "Non-Calculate" signal occurs by reason of no card in the punch sensing station or a non-calculate control hole indication, the diode ENCD passes a negative pulse to kick ENC right. ENC opens the gate ENCG which causes a "Trip I" signal. The trip I thyratron operates EGD via EBAL, as before.

In the case of a "Stop Indication" from the zero factor selector switch the left side of EAC closes the right side of EGθ to prevent EGD from producing ESZ and ESI pulses. Since the calculation is not completed the automatic restart circuit will continue to start the step or problem over and over until the punch is tripped to pass the card manually. Each time the stop signal is given the "Stop" indication light flashes to indicate that the cause of stoppage is a zero factor.

If a "Reject" signal is given from the zero factor selector switch EGD, thru left side of EGθ, kicks EGP right which in turn opens both gates of EGPG, EGPG then calls for both a "Sort I" and "Trip I" signal.

ALGEBRAIC SIGN

The algebraic sign of a computational result is determined as described in the following paragraphs.

The keyboard bias through the negative input switches (or relay contacts) and the mixer neons, raises the minus neon common line which through MC, and MCX raises the left bias of EZS when a negative factor is present and MC2 is left. This allows the output of PAMD to pass through the left side of EZS, right side of ERAZ and through the right or left side of PS to kick either PAT or PAM. PAMD operates when EM, ES, EPN, EPS, or EPP go right. The right side of PS is held open during multiplication and division by the multiplication or the division bus through PIMD and LS–PPI to permit PAMD to kick PAT; the final state of PAT during ER determines the sign of the result. The left side of PS is opened during addition and subtraction by the addition or the subtraction bus through PIAS and RS–PP1 and permits PAMD to kick PAM in sign bias; the final state of PAM for each factor determines the bias of the accumulator during subsequent registrations.

The multiplication or division bus brings down one cathode of PIMD to allow PPI to open the right gate of PS. If the M'd is negative the return of PAMD kicks PAT RIGHT through the right side of PS. If the S'r is negative the return of PAMD kicks PAT left again and since in multiplication and division the result of one minus factor and one plus factor is minus, the result of two minus factors is plus, PAT being on the right after the M'd and S'r keyboard biases have operated indicates a negative result. The numerical value is unchanged in multiplication and division by negative signs.

PAT when on the right raises the left input of EG through θ9SM, MC8, MC7 to allow MS to set the branching sign trigger EBS to the right to indicate a minus result. (See step Control Chassis.) PAT also through NC7A raises the grids of the minus storage input tubes, and the left of MK (P through Y). The setting of the minus branch trigger and minus storage occurs when NS operates to set the storage.

Now that the sign has been stored PAT must be returned to the left to keep track of the sign during proof. This is done by the right plate of ER on its return normalizing PAT through the right side of EZS.

In the proof if the result is negative then either the S'r or M'd will have to be negative. PAT will kick right on the proof M'd operation and left again on either the proof S'r or Proof subtraction step. If the result is positive because of two negative factors PAT will go right on the prove S'r and left on the prove subtraction. If PAT does not stand on the left at the time of completion of the equation then its left plate causes the right grids of θ9SM and θ9SM1 to be high holding the "Check Line" low.

The *add or subtract* bus lowers one cathode of PIAS to drop the right grid of PPI which in turn opens the left gates of PSO and PS. The return of PAMD for a negative passes through the left side of PS to kick PAM right and set the sign biases for a negative input. (See Sign Bias Chassis.)

The sign of the result is indicated by the number of carrys out of column 11A in the accumulator, signalled by the right plate of 11AC going high when this stage is returned by the carry generator. PSO pulses PAC for each overcarry from 11A to IM, therefore a negative result is indicated by PAC being on the right when the M'd and S'r operations have been completed.

PAC when on the right raises the left plate of MC7 through MC8 to raise the left input of EG to allow setting of the branching sign trigger EBS to indicate a minus branch and left grids of MK (P through Y) to set the minus sign storage relay. PAC also sets the biases on MC1 for the complementing of negative results on addition and subtraction.

PAC operates during proof but has no effect on the check as an incorrect sign input will cause an arithmetic incorrect proof, causing the accumulator to read other than a row of zeros or nines in the A section.

The operation of the carry circuits is as follows:

When there is no overcarry indication from the accumulator, then at the end of the RIG cycle a positive pulse from LP–CDA will go through the left side of CX (left side opened by CB being on the right for no carry indication) to kick DRB left.

A carry indication from the accumulator kicks CB left by lowering the II point. CB left opens the right side of CX. The positive pulse from CDA goes through the right side of CX to kick CT right lowering the LI of CMA. This raises the LI of CM to start the multivibrator. CM going right makes its LP high and through CA, kicks the carry trigger TC, in the accumulator left. This kicks CB right again to eliminate the carry indication and closes the right side of CX and opens the left side of CS. The multivibrator CM returns left to send a pulse through the left side of CS to kick CT left. This lowers the LI of CM through the left side of CMA to cut off the multivibrator. At the same time CT also sends a pulse through the right side of CMA to kick DRB left.

ZEROS OR NINES CHECK

The proof subtraction operation performed at the conclusion of each step may result in either all zeros or all 9's in orders 1A through 10A of the accumulator. Either of these results indicates that the calculation being checked was performed correctly. The operation of the zero check circuit is described in the following paragraphs.

Assume a row of nines to be the result after the final subtraction during EPP. EPP being on the right opens the right side of diode gate EφC. The CX pulse following the final subtraction returns DRB (which produces a control ring pulse to return EPP) and also operates PAD through the right side of gate EφC. The return of PAD kicks EφCT right and also tests the right side of the φ check gate, EG, for possible advance to the next step. As mentioned previously, however, final subtraction had resulted in 9's and gate EG is closed. EφCT, after being kicked right by the return of PAD, opens the left side of diode gate EφC and the left side of gate EφCA and, through EφCB, drops the left plate of PSA to raise the add biases in all sections and call for a cycle of RIG, RIG1' feeds through the left side of open gate EφCA onto the odd line of ACC 1A. After carries are satisfied (the "A" section is now reduced to zeros) the CX pulse passes through the left side of EφC (held open by EφCT) and again operates PAD. The return of PAD this time passes through the right side of φ check gate EG to operate EGD for advance to the next step.

If the final (proof) subtraction results in zeros then PAD returning the first time will pass a pulse through φ check gate EG to operate EGD for step advance. In either case EφCT is kicked right but will be returned by the zeroize operation in the following step.

If, after the second time PAD operated, there was no zero check the step or problem would be repeated by the automatic restart circuit after the timer ran out.

All zeros in accumulators 1A through 10A is indicated by the right side of φ check gate EG being open. This is accomplished by the zero check circuit comprised of stage φ9C, φ9C1, φ9M, φ9SM, and φ9SM1 in the Zero Factor chassis and the zero check diodes, MφC, in each of the ten I-O chassis. A zero number indication from accumulators 1A through 10A will have all φ check diodes (MφC) with low plates. This will allow the common cathode return of the diodes (which is tied to LI and RI of φ9C and φ9C1) to be low. The common plates of φ9C and φ9C1 will rise and bring up the II of φ9M. The left plate of φ9M will fall and cut off the left grids of φ9SM and φ9SM1. Provided now that trigger PAT is on the left (as described in the write-up on the Zero Factor chassis) the common plates of φ9SM and φ9SM1 will rise to open the right side of the zero check gate EG.

COMPLEMENTIZING PROCESS

When a calculating step produces a negative result, the result will initially appear in the accumulator orders as the complement of the true value of the negative result. Since it is desired to record all output results as true values rather than complements the procedure described below is employed. The stages referred to in the description appear in a number of chassis and may be located by reference to the alphabetical stage index.

When a negative result is reached during an addition or subtraction the step is started over again with the sign of each input inverted and the minus relay set to indicate that the result is negative.

At the completion of the ES control ring step, the add-subtract sign trigger PAC will be on the right if the result is negative allowing the return of ES to kick MC2 right through the left side of MC1. The left plate of

MC2 through the right side of MC6 operates EZ to start the step again.

The stages MC4, MC5, MC6 (left side) and MCX form the negative input circuit which when MC2 is on the left cause the minus gate EZS to be closed on a plus input and open on a minus input. When MC2 is on the right as is the cause of a negative result the above stages serve to invert the sign input to EZS causing it to be high on a plus sign and low on a negative sign.

Following is a table of plate levels for the four conditions:

	MC2		MC4		MC5		MC6		MCX		Minus Neon Common	LI-EZS
	LP	RP	LP	RP	LP	RP	LP	RP	LP	RP		
Plus	L	H	H	L	L	L	L	------	L	L	L	L
Result	L	H	L	L	H	H	L	------	L	H	H	H
Minus	H	L	H	Ⓗ	L	L	Ⓗ	------	Ⓗ	L	L	H
Result	H	L	L	Ⓛ	L	L	Ⓛ	------	Ⓛ	L	H	L

○+□ indicates common plates.

The second time through the step the result will appear to PAC as positive allowing the right gate of MC1 to be open (and the left gate closed). ER is then operated by the return of ES. Since MC2 is already right indicating that the result is minus its left plate causes the right plate of MC7 to be low and the left plate of MC7 high. This enters a minus indication to the branch gate EG, left side, and minus relay set tubes LD–MK (P–Y). MC3 zeorizes MC2 at the problem start or branch to another step, from LP ESD or RP EGDC.

If the result sign is minus and the numerical result zero it may be desirable to prevent a minus zero result from setting and branching minus in certain installations, such as the result of:

$$-A+A=-P$$
$$-2+2=-\phi$$

Entering the −2 as the M'd causes one overcarry to PAC while entering 2 as the S'r causes the accumulator to read nines, the complement of zero. Restarting the step with inverted signs gives 2 (−2) or ϕ, but since MC2 is on the right, the left side of MC7A is cut off. The accumulator reads zero allowing the right side of MC7A to be cut off. The gate of ϕC2 is open allowing the return of ϕC1, which was operated by ER going right, to kick ϕFS which gives a control ring pulse to return ER and a second which does nothing because of the longer delay of EPZ. ϕFZD allows the relays to clear before registration of the prove M'd. The delay of ϕC1 is necessary to allow the bias of ϕC2 to rise. ER initiates a decimal RIG but no keyboard bias is raised therefore nothing is entered in the decimal counter. Since the result is zero the skipping of the result decimal registration does not cause any difficulty.

The left side of MC4L prevents any possibility of MC2 being kicked right during the normal zeorize time by closing the left side of MC1. MC2 is not zeroized normally but rather by the stage MC3 operated from ESD, EGD or EPY.

In using the test counter the counter will only enable the calculation to be stopped during the first operation of EM and ES. Since the test counter is zeroized at the second time that EZ operates.

ZERO FACTOR CHASSIS

Referring now to Figs. 25*a*–25*f* which are related in the manner of Fig. 25*g*, the operation of the Zero Factor chassis will be described.

In a multiplication or division problem PIMD has one cathode pulled low by the process bus to cut off the left side of PP1 allowing its left plate to open the gate of ϕF2. Just following the RIG cycle of M'd registration CD goes left to pass a pulse through ϕF2 to kick ϕF1 right. The EMK line holds the cathode of ϕF3 low during M'd registration and should the M'd be zero the gate bias of ϕF3, left side of ϕF4, and ϕF5 is open, therefore ϕF3 will kick ϕMD right. ϕMD through the right side of ϕF3 pulses the 11A odd line to enter an artificial M'd in column 11A and at the same time raises the right bias of ϕF4, left grid of ϕFR1 and bias of ϕEZ. At the completion of the M'd control step EPG kicks ϕF1 left again through the delay ϕFD1.

The cathode of ϕF4 is lowered by the ESK bus and again CD operates ϕF1 through ϕF2. Should the S'r be a number and ϕMD is right because of a zero M'd ϕFS is kicked right through the right side of ϕF4 is again high and the input from LP ϕF1 will kick ϕSR right. ϕSR opens the gates of ϕEZ1 and lowers the right grids of ϕFR1 and ϕFR2 and also kicks ϕFS right through the right side of ϕF2. If the M'd is a number and the S'r Zero then ϕFS is kicked by ϕSR through, the right side of ϕF2.

ϕFS going right gives a control ring step pulse through the left side of ϕESP which returns ϕF1 and ES. ER is kicked by the return of ES and is quickly returned by the return of ϕFS through the right side of ϕESP. The control ring now calls for clearing of the A section in normal manner and then steps to EPM to lower the ERK line. Upon operation of ϕFS to the right, ϕFZD is triggered right. This clamps DMP left (DMP is normally operated right by EPM through the left side of EPMA) through right side of ϕ9M so that the decimal registration call from EPM will not take place. ϕFZD also prevents continued RIG cycles from occuring due to the interruption of the division or multiplication by raising the cathodes of PB and PMDR through RBK. Since the relays may not have been cleared by the time EPM operates, ϕFZD is used to delay decimal registration and subsequent prove M'd RIG until the relays are cleared. Unclamping DMP allows the decimal registration and RIG cycle to take place. ϕFZD has a time delay of relay clear (MZ).

ERK lowered the cathode of ϕF5. The result in the relays must now be zero and operation of ϕF1 by CD passes through ϕF5 to kick ϕRS right. Either or both gates ϕEX and ϕEZ1 are open if the M'd or S'r or both were zero allowing the left plate of ϕRS to kick EZ and start the equation step over again as a check. This time ϕRS goes left, the right plate through ϕEZ or ϕEZ1 gives the signal that zero factor operation has been completed by kicking EGD in the step control chassis. The cathodes of ϕF3, ϕF4, and ϕF5 are delayed by RC circuits to prevent their rising before the signals are applied to their grid.

On multiplication either or both zero M'd and S'r should give a zero result. On division a zero M'd number S'r should give a zero result, but a number M'd and zero S'r should be a choice of Set, Stop, or Reject. The latter case is controlled by the grids of ϕFD3 being lowered by the division bus (through the divider of EID), the lowering of the right grid of ϕFR1 by ϕSR and the left grid of ϕFR1 remaining low from ϕMD; allowing the common plates to raise the N÷ϕ switch common through

the right side of ϕFN. In the case of zero divided by zero the same choice of Set, Stop or Reject is allowed by the lowering of the right grid of ϕFD3 by the division bus, and the lowering of the right and left grids of ϕFR2, by the ϕSR and ϕMD stages allowing their common plates to raise the $\phi \div \phi$ switch common lead through the left side of ϕFM.

The purpose of the right side of ϕRSZ is to insure that ϕRS, which is not zeroized is always on the left at the start of an equation step.

TEST COUNTER

The test counter which is shown in Fig. 34 is a predetermined counter that has a capacity of 399, 400 being equal to zero. (It is now set up for use to 299.) The machine works on complements of 399 so that the tens and units digits are the same, thus making the wiring for both digits identical. (Otherwise in subtracting a number from 400 the units digit is subtracted from ϕ and the tens digit from 9.) This is why at the beginning of TCR operation a 1 is registered that has no relation to the counting of pulses. (If in a problem the 33rd shift is wanted for observation, the counter switches are turned to 33 but the number registered in the counter is 366.) This number is registered by B5 in the counter by means of the two lines going from each counter stage's left and right bias. Normally the left bias is connected to —90 v. and the right to B5. However, through the switches in the TCR panel the B5 and —90 bias points are reversed at will so that the B5 pulse will kick all triggers left except those indicated by the TCR panel, which will be pulled right.

The low from LP–DEA besides initiating decimal registration kicks TS right in TCR. TS going right opens the left side of TG from LP–TS and kicks T1* right through the right side of TSA. T1 going right does nothing. A pulse from either CSK (which goes low every time CM is right; thus counting each carry) in DCR, the SIG bus (for shifts from SM), or RIG1′ for Post- and Pre-RIG, depending upon which one is switched to through the TCR panel, will pulse the left side of TG. The first high pulse kicks T1 left which kicks $T\bar{2}$ right through the left side of TUG opened by $T\bar{2}$ being left. If $T\bar{2}$ is already right, the pulse from T1 kicks T2 right or left depending upon its original position through the right side of TUG.

When the counter reaches 399, TC2 goes left to pull TB right. This raises the cathode of TK to block SMG (shift gate), CM through SCK1 (carry MV), PMDR and RB (RIG calls), and CX (carried satisfied, depending upon whether the switch was set to Pre-SIG, Pre-CIG, Pre-RIG, or Post-RIG. When the circuit is blocked in this manner, the automatic timer will restart the step or the problem.

While interconnections between the various chassis are shown in Figs. 35–40, the following Tables of Connections afford a ready reference to interconnection information.

A separate table is provided for each chassis and the tables are arranged in alphabetical order according to chassis designation. Each table shows connections to the various terminal points of a particular chassis. Terminal numbers are arranged in the same way as they are shown in Figs. 16–34 which are the schematic and block schematic diagrams of each of the chassis.

Table of connections to Accumulator (ACC) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(MD-43)LD-PMS. Lugs 1 and 3 used in ACC 11M only.	2	
3	(MD-45)RD-PMS.	4	
5	Shift input.	6	Fil. A, F.
7	Overcarry.	8	Fil. B, E.
9	CIG. call.	10	Fil. C, D.
11	To (2)ME.	12	Carry block Bias — 15 v.
13	To (2)MO.	14	CIG in.
15	To LG(3)S1.	16	From RPD(1)S1.
17	Carry out.	18	Carry and odd input.
19	To RG(3)S1.	20	From LPD(1)S1.
21	To RG(3)Sϕ.	22	From LPD(1)Sϕ.
23	To LG(3)Sϕ, LG(2)MA9 and RG(2)M17.	24	From RPD(1)Sϕ.
25	To RG(3)S8 and RG(2)M9.	26	From LPD(1)S8.
27	To LG(3)S8 and RG(2)M57.	28	From RPD(1)S8.
29		30	B_2 ("A" Section). B_5 ("M" Section).
31	Gnd.	32	—90 v.
33		34	—150 v.
35	B+.	36	Even input.
37	To RG(3)S2.	38	From LPD(1)S2.
39	To LG(3)S2, LG(2)M13 and LG(2)M35.	40	From RPD(1)S2.
41	To RG(3)S6.	42	From LPD(1)S6.
43	To LG(3)S6, LG(2)M57 and LG(2)M17.	44	From RPD(1)S6.
45	To RG(3)S4.	46	From LPD(1)S4.
47	To LG(3)S4, RG(2)M13 and RG(2)M35.	48	From RPD(1)S4.
49	+ Bias.	50	— Bias.

Table of connections to Base Control (BC) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(OCL)-LP-EGC1.	2	Fil. "M."
3	(OCL)-LP-EGC2.	4	Fil. "L."
5	(OCL)-LP-ELC1.	6	Fil. "M."
7	(OCL)-LP-ELC2.	8	Sort I solenoid.
9	(OCL)-LP-EPC1.	10	Sort II solenoid.
11	(OCL)-LP-EPC2.	12	Fil. "L."
13	(OCL)-LP-ENC.	14	Set I thyratron grid.
15	(OCL)-LP-EGP.	16	Set II thyratron grid.
17		18	Trip I thyratron plate.
19	"Ready" SW.	20	Trip II thyratron plate.
21		22	115 v. 60~A.C. Line.
23	(SCL)-LD-EP3.	24	Thyratron bias.
25	(SCL)-RC-EGD.	26	Trip I thyratron grid.
27	Gnd.	28	Trip II thyratron grid.
29	—150 v.	30	Plate set I thyratron.
31	+150 v.	32	Plate set II thyratron.
33	—15 v.	34	Fil. S—connect to pin 3. EGT1 and EGT2.
35	60~ phasing supply.	36	Fil. T—connect to pin 4. EGT1 and EGT2.

Table of connections to Control (CTL) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "D."	2	Fil. "D."
3	Fil. "F."	4	Fil. "E."
5	(SB-28)LI-EϕCB. (DCR-2)SK2.	6	Fil. "F."
7	(SCL-42)RC-EG.	8	Gnd.
9	(DCI-43)RP-DMP.	10	—150 v.
11	(DCL-15)RI-MSI.	12	(SS-34)EMK. (ϕF-11)K-ϕF3.
13	(DCL-31)LI-DG.	14	(SS-32)ESK. (ϕF-13)K-ϕF4.
15	(DCL-29)RI-DG. (SB-30)LP-EϕCB.	16	(SS-31)ERK. (ϕF-15)K-ϕF5.
17	(DCL-13)LI-EP2.	18	(ϕF-17)RP-MC1.
19	(DCL-45)D-DMP.	20	(ϕF-7)LC-MC3. (DCR-31)LP-CX.
21	(DCL-17)LI-EPP2.	22	(SCL-44)P-ESZ1. (ϕF-21)LP-ϕEZ.
23	(DCL-41)D-DRP.	24	(ϕF-23)C-PS.
25	—Gov.	26	(ϕF-25)MC1.
27	(DCL-39)RP-DRB. (SB-12)RI-PSAC.	28	(ϕF-27)LP-PAT.
29	(ϕF-36)K-MCX.	30	
31		32	(ϕF-31)LD-MC4L. (DCR-37)LD-SMA. (DCL-2)LD-MS′.
33		34	(ϕF-33)P-ϕ. (DCL-33)RP-DPG2.
35		36	(STZ-43)RC-MZK.
37	(11M-12)LB-AC.	38	(MD-44)RP-PMDZ.
39	(REG-8)B5.	40	+150 v.
41	—375 v.	42	(REG-7)B2.
43	(REG-10)I-ZB5.	44	—90 v.
45	(REG-)I-ZB2.	46	—15 v.
47	Fil. "O."	48	Fil. "Q."
49	Fil. "P."	50	Fil. "R."

Table of connections to Decimal Control (DCL) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(EQ.BD). (φF-8)+.	2	(CTL-32)LD-ERAZ. (DCR-37)LD-SMA.
3	(EQ.BD). (φF-10)−.	4	Gnd.
5	(EQ.BD). (φF-12)x.	6	B5.
7	(EQ.BD). (φF-14)÷.	8	−90 v.
9	LP-PSA. (SB-9).	10	(φF-20)LD-φFD3.
11	(φF-45)RP-φ9M.	12	(DCR-11)I-SM. (MD-10)K-SI1.
13	(CTL-17)RP-ES.	14	(DCR-13)RP-DP16.
15	(CTL-11)LP-EMZ.	16	(DCR-15)LP-DP16.
17	(CTL-21)RP-EPS.	18	(DCR-17)RP-DCC.
19	(STS 1-19)K-MS(T-V). (STS 2-19)K-MS(P-Q).	20	(DCR-19)K-D8-16C.
21		22	(DCR-21)RP-DP2.
23	(φF-16)LC-MC2. (SCL-40)LC-EG.	24	(DCR-23)RP-DP2.
25	(SB-18)RI-PSA.	26	(DCR-25)LP-DP1.
27	(SB-16)LI-PSA.	28	(DCR-27)C-DP1. (TCR-7)RC-TS.
29	(CTL-15)LP-ECPL.	30	(DCR-29)RD-DI1.
31	(CTL-13)RP-ECB1.	32	(DCR-31)RP-CX. (MD-12)RC-PM3.
33	(CTL-34)LP-EPG. (φF-33)LC-φF1.	34	+150 v.
35	(MD-9)LI-PDP.	36	−150 v.
37	(MD-7)LD-PMP.	38	−60 v.
39	(CTL-27)LC-EPG. (SB-12)RI-PSAC.	40	−15 v.
41	(CTL-23)LD-ERA.	42	(SB-14)RC-PDAM.
43	(CTL-9)LP-EPMA.	44	(MD-11)LC-PMM.
45	(CTL-19)LD-EMA.	46	Fil. "I."
47	Fil. "I."	48	Fil. "H."
49	Fil. "G."	50	Fil. "G."

Table of connections to Decimal Counted (DCR) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Dec. input Sw. 1.	2	(CTL-5)LP-EφCT. (SB-28)LI-EφCB.
3	Dec. input Sw. 2.	4	
5	Dec. input Sw. 4.	6	
7	Dec. input Sw. 8.	8	
9	Dec. input Sw. 16	10	
11	(MD-10)K-S11. (DCL-12)K-S12.	12	
13	(DCL-14)LP-DKG.	14	Dec. input Sw. 2'.
15	(DCL-16)RC-DA1-16.	16	Dec. input Sw. 4'.
17	(DCL-18)LC-DRS.	18	Dec. input Sw. 8'.
19	(DCL-20)K-DBC.	20	Dec. input Sw. 16'.
21	(DCL-22)K-DBT.	22	
23	(DCL-24)RP-DKG.	24	−15 v.
25	(DCL-26)LC-DA1-16.	26	B5.
27	(DCL-28)LP-DEA.	28	−90 v.
29	(DCL-30)LD-DKG.	30	GND.
31	(DCL-32)LC-DRB. (MD-12)RC-PM3.	32	−60 v.
33	(φF-9)LC-φF2. (RIG-12)LP-CDA.	34	−150 v.
35	(MD-14)LC-PD3.	36	+150 v.
37	(CTL-32)D-EPZC. (φF-31)LD-MC4L.	38	(Test panel "Stop" Sw.) pre-SIG-output.
39	((1A-11M)-5)SIG BUS. (MD-8)LC-PGMD.	40	(Test panel "Stop" Sw.) (of-19)K-φF2 post-rig output.
41	((1A-11M)-14)CIG.	42	(Test panel "Stop" pre-CIG input.
43	((1A-11M)-9) carry call.	44	(Test panel "Stop" Sw.) pre-CIG output.
45		46	Fil. "I."
47	Fil. "I."	48	Fil. "H."
49	Fil. "G."	50	Fil. "G."

Table of connections to Input-Output (I-O) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	−15 v.	2	RPD(2)S1.
3	Carry input and Odd input.	4	LPD(2)R1.
5	RIG1.	6	Fil. "M."
7	RIG8.	8	Fil. "L."
9	(2)17.	10	Fil. "M."
11	RIG6.	12	RPD(2)Sφ.
13	RIG1'.	14	LPD(2)S8.
15	(2)19.	16	RPD(2)S8.
17	−90 v.	18	(2)09.
19	−150 v.	20	Gnd.
21	(2) Even input.	22	(2)01.

Table of connections to Input-Output (I-O) chassis—Continued

Terminal No.	Connects To—	Terminal No.	Connects To—
23	(2)I1.	24	+150 v.
25	(2)I3.	26	(2)07.
27	RIG2.	28	RPD(2)S2.
29	RIG4.	30	(2)O3.
31	(2)I5.	32	RFD(2)S6.
33	−60 v.	34	(2)O5.
35	φ check.	36	RPD(2)S4.

Table of connections to Keyboard Bias (KB) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "A."	2	
3	Fil. "B."	4	
5	Fil. "C."	6	
7	(−).	8	KB(−).
9	(J).	10	KB(J).
11		12	
13		14	
15	(H).	16	KB(H).
17	(G).	18	KB(G).
19	(F).	20	KB(F).
21	(E).	22	KB(E).
23	+150 v.	24	−150 v.
25	−60 v.	26	
27	(D).	28	KB(D).
29	(C).	30	KB(C).
31	(B).	32	KB(B).
33	(A).	34	KB(A).

Table of connections to Multiplication-Division (MD) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "G."	2	Fil. "G."
3	Fil. "I."	4	6.3 v. A.C. fil. "H"; common.
5		6	6.3 v. A.C. fil. "I."
7	(DCL-37)RD-DMP.	8	(DCR-39)SIG bus. ((1A11M)5)SIG.
9	(DCL-35)RK-EID2.	10	(DCR-11)I-SM. DCL-12)K-S1-2.
11	(DCL-44)RP-DK.	12	(DCR-31)RP-CX. (DCL-32)LC-DRB. (φF-7)LC-MC3.
13	(RIG-14)RD-I1-11.	14	(DCR-35)LP-SG.
15	(RIG-16)LP-PX.	16	
17	(RIG-18)RP-RS.	18	B2.
19	(RIG-20)RP-PX.	20	−90 v.
21		22	Gnd.
23		24	+150 v.
25		26	−150 v.
27		28	−15 v.
29		30	−60 v.
31	(SB-34)LI-BA+1.	32	
33	(SB-36)LI-BM+1.	34	
35	(SB-38)LI-B11-1.	36	
37		38	
39		40	
41	(11M-9)11A Carry Call.	42	
43	(11M-1)LP-T1. (Thru series Res).	44	(CTL-38)LC-EMPC.
45	(11M-3)RP-Tφ. (Thru series Res).	46	Input-Output Sw. (SB-48)K-RB.
47	(φF-41)LC-PSO.	48	
49	(11A-9)RP-AC.	50	

Table of connections to Output Control (OCL) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(BCL-1)LI-EGCG.	2	
3		4	Sort II bus.
5	Sort II Line.	6	Sort I bus.
7	Sort I Line.	8	
9	(BCL-3)RI-EGCG.	10	ESI.
11	(BCL-5)LI-ELCG.	12	(φF-24)RC-φRSZ.
13	Set II Line.	14	Set II bus.
15	Set I Line.	16	Set I bus.
17	(BCL-7)RI-ELCG.	18	
19	(SCL-20)LI-ESZ1.	20	Trip II bus.
21	(BCL-9)LI-EPCG.	22	Trip I bus.
23	(BCL-11)RI-EPCG.	24	
25	(SCL-32)RP-EGD.	26	
27	(SCL-28)ESZ2.	28	

81

Table of connections to Output Control (OCL) chassis—Continued

Terminal No.	Connects To—	Terminal No.	Connects To—
29	(BCL-15)I-EGPG.	30	−15 v.
31	(SCL-34)RC-ESIA.	32	+150 v.
33	(BCL-13)LI-ENCG.	34	Clear selector Sw. common.
35	Non-calculate Sw.	36	−90 v.
37	"Reject" position. ϕ factor selector Sw.	38	−150 v.
39	"Stop" position. ϕ factor selector Sw.	40	Gnd.
41	Clear bus.	42	
43	Clear line.	44	
45		46	Fil. "I."
47		48	Fil. "H."
49		50	Fil. "G."

Table of connections to Zero Factor (ϕF) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "D."	2	Fil. "D."
3	Fil. "F."	4	Fil. "E."
5	Gnd.	6	Fil. "F."
7		8	(DCL-1)+Bus (EQ'B'D).
9	(DCR-33)C-CX. (RIG-12)LP-CDP.	10	(DCL-3)−Bus (EQ'B'D).
11	(CTL-12)K-EMK. (SS-34)EMR.	12	(DCL-5)×Bus (EQ'B'D).
13	(CTL-14)K-ESK. (SS-32)ESK.	14	(DCL-7)÷Bus (EQ'B'D).
15	(CTL-16)K-ERK. (SS-31)ERK.	16	
17	(CTL-18)RP-ER.	18	(STS(2)-17. Minus Neon Common.
19	(PCR-40)K-SCK.	20	(DCL-10)LD-E1D.
21	(CTL-22)RP-EZ. (SCL-44)P-ESZ1.	22	(SCL-30)LP-ESD.
23	(CTL-24)RP-ERAS.	24	(OCL-12)RP-EGDC.
25	(CTL-26)RP-ES.	26	(SCL-32)RP-EGD.
27	(CTL-28)RP-EZS.	28	(SCL-36)RI-EG.
29	(SCL-12)LP-EP4'.	30	N÷ϕSw. Common.
31	(CTL-32)LD-ERAZ. (DCR-37)LD-SMA.	32	ϕ÷ϕSw. Common.
33	(CTL-34)LP-EPG. (DCL-33)RP-DPG2.	34	(SCL-38)L1-EG.
35		36	(CTL-23)L1-EZS.
37	(SB-10)RP-PAM.	38	(STS 1,2-37) LD-MK(P-Y).
39	(11A-18)Odd Line.	40	+150 v.
41	(MD-47)LP-P11C.	42	−150 v.
43	(10-35)ϕ check.	44	B5.
45	(DCL-11)LP-DMP.	46	−90 v.
47	(SB-40)R1-RBK.	48	−15 v.
49		50	−60 v.

Table of connections to Regulator (REG) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "C."	2	Fil. "C."
3	Fil. "B."	4	Fil. "B."
5	Fil. "A."	6	Fil. "A."
7	(REG42)B2.	8	(B5 CTL-39).
9	(CTL-45)RP-ZBA2.	10	RP-ZBA5(CTL-43).
11	(STS2-28)P-MZ1A.	12	P-MZ5A(STS1-28).
13	(ST(P)-36). (STS2-16)K-MKP.	14	(ST(T)-36). (STS1-16)K-MKT.
15	Gnd.	16	−150 v.
17	(STS2-30)P-MZ2A.	18	P-MZ6A(STS1-30).
19	(ST(Q)-36). (STS2-18)K-MKQ.	20	(ST(V)-36). (STS1-18)K-MKV.
21	(STS2-32)P-MZ3A.	22	P-MZ7A(STS1-32).
23	(ST(R)-36). (STS1-20)K-MKR.	24	(SF(W)-36). (STS1-20)K-MKW.
25	(STS2-34)P-MZ4A.	26	P-MZ28A(STS1-34).
27	(ST(S)-36). (STS2-22)K-MKS.	28	(ST(Y)-36). (STS1-22)K-MKY.

82

Table of connections to Registration Impulse Generator (RIG) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "M."	2	Fil. "L."
3		4	Fil.
5		6	Fil. "L."
7	(11M-18) Odd line.	8	P-RS(SS-5C).
9	(1M-18) Odd Line.	10	
11		12	(C-CX(DCR-33). (LC-ϕF2(ϕF2-9).
13		14	LD-PMDR(MD-13).
15	(IO-5)RIG1.	16	LP-PD1M(MD-15).
17		18	P-PMDR(MD-17).
19	(IO-13)RIG1.	20	RP-PD1M(MD-19).
21		22	
23	(IO-7)RIG8.	24	
25		26	
27	(IO-11)RIG6.	28	
29		30	+150 v.
31	(IO-29)RIG4.	32	
33		34	
35	(IO-27)RIG2.	36	
37	−150 v.	38	
39	Gnd.	40	B5.
41		42	− 90 v.

Table of connections to Sign Bias (SB) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(11M-49)B11+.	2	Fil. "D."
3	(11M-50)B11−.	4	Fil. "E."
5	((1M-10M)-49)BM+.	6	Fil. "F."
7	((1M-10M)-50)BM−.	8	
9	(DCL-9)LP-MZR.	10	(ϕF-37)LP-PS.
11		12	(DCL-39)RP-DRB. (CTL-27)LC-EPG.
13		14	(DCL-42)LP-DRB.
15		16	(DCL-27)LK-E1A3(+).
17		18	(DCL-25)RK-E1S1(−).
19		20	B5.
21		22	−90 v.
23		24	−60 v.
25		26	Gnd.
27		28	(CTL-5)LP-EϕCT. (DCR-2)SK2.
29		30	(CTL-15)LP-ECB1.
31		32	LA-Odd Line.
33		34	(MD-31)LP-PM23.
35		36	(MD-33)RP-PDA.
37		38	(MD-35)LP-PDA.
39		40	(ϕF-47)LP-ϕFZD.
41		42	−150 v.
43	(RIG-19)RIG1.	44	−15 v.
45		46	+150 v.
47	((1A-11A)-49)BA+.	48	Input Output Sw. (MD-46)K-PMDR.
49	((1A-11A)-50)BA−.	50	(RIG-8)RP-RD.

Table of connections to Step Control (SCL) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1		2	
3	(SS-5)−Result.	4	
5	(SS-6)+Result.	6	
7		8	
9		10	(Restart Sw.) "step."
11		12	(ϕF-29)LC-MC2.
13	Clear restart Sw. (set clear Sw. panel).	14	(Restart Sw.) "problem."
15		16	
17		18	(BCL-23)P-ETMY.
19	"Calc. in progress" "relay."	20	(OCL-19)P-EAA.
21		22	
23		24	(Clear restart Sw. and Calc. start relay. (Set clear Sw. Panel).
25		26	(BCL-25)LP-EBAL.
27		28	(OCL-27)ESZ2.
29		30	(ϕF-22)LC-ϕRSZ.
31	Gnd.	32	(ϕF-26)RP-OEZ. (OCL-25)RC-EGDC.
33	(SS-35)ESZ.	34	(OCL931)RP-EGϕ.
35	(SS-36)ESI.	36	(ϕE-28)P-ϕ9SM.
37	(SS(1-4)-38 start line.	38	(ϕF-34)LP-MC7.
39	−15 v.	40	(DCL-23)LP-MS. (ϕF-16)LC-MC2.
41	B5.	42	(CTL-7)RP-PAD.
43	−90 v.	44	(CTL-22)RP-EZ. (ϕF-21)LP-ϕEZ.
45	−150 v.	46	Fil. "I."
47	+150 v.	48	Fil. "H."
49	−60 v.	50	Fil. "G."

Table of connections to Step Sequence (SS) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(TCR) step sel. Sw. Step 3.	2	Step Sel. Sw. Step 1 (TCR).
3	(TCR step sel. Sw. Step 4.	4	Step Sel. Sw. Step 2 (TCR).
5	—Result.	6	+Result.
7	(3)—.	8	(1)—.
9	(4)—.	10	(2)—.
11	(3)+.	12	(1)+.
13	(4)+.	14	(2)+.
15	(3)PROC.	16	(1)PROC.
17	(4)PROC.	18	(2)PROC.
19	(3)R.	20	(1)R.
21	(4)R.	22	(2)R.
23	(3)S'r.	24	(1)S'r.
25	(4)S'r.	26	(2)S'r.
27	(3)M'd.	28	(1)M'd.
29	(4)M'd.	30	(2)M'd.
31	ERK.	32	ESK.
33	—90 v.	34	EMK.
35	ESZ.	36	ESI.
37	(3)Step.	38	(1)Step.
39	(4)Step.	40	(2)Step.
41	+150 v.	42	—150 v.
43	Gnd.	44	
45	Fil. "L."	46	
47	Fil. "H."	48	
49	Fil. "G."	50	

Table of connections to Storage (ST) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	KB(P).	2	(P) Set Sw. common.
3	(1–P)L9.	4	(2–P)L9.
5	(1)I9.	6	(2)I9.
7	(1)O9.	8	(2)O9.
9	(1–P)L7.	10	(2–P)L7.
11	(1)I7.	12	(2)I7.
13	(1)O7.	14	(2)O7.
15	(1–P)L5.	16	(2–P)L5.
17	(1)I5.	18	(2)I5.
19	(1)O5.	20	(2)O5.
21	(1–P)L3.	22	(2–P)L3.
23	(1)–I3.	24	(2)I3.
25	(1)O3.	26	(2)O3.
27	(1–P)L1.	28	(2–P)L1.
29	(1)I1.	30	(2)I1.
31	(1)O1.	32	(2)O1.
33	Fil. "J."	34	+300 v.
35	Fil. "K."	36	(REG–13). P.SK(P). (STS2–16)K–MK(P).

Table of connections to Storage Set (STS 2,1) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	(KB4–30,18)KB(R, W).	2	
3	(KB4–28,16)KB(S, Y).	4	
5		6	Minus Punch (R, S).
7		8	Minus Punch (S, Y).
9	(KB4–34,22)KB(P, T).	10	
11	(KB4–32,20). B(Q, V).	12	Minus Punch (P, T).
13		14	Minus Punch (Q, V).
15	"(Q, V) set" selector Sw. Common.	16	(REG.13,14)P–SK(P, T). (ST(P, T)—36,36).
17	Minus Neon Common (φF–17)LD and RD MC4.	18	(REG—19,20)P–SK (Q, V). (ST(Q, V)–36,36).
19	(DCL–19)K–MSK.	20	(REG–23,24)P–SK (R, W). ST(R, W)–36,36).
21	"(P, T)Set" selector Sw.Common.	22	(REG–27,28)P–SK (S, Y). (ST(S,Y)–36,36).
23	"(S, Y)Set" Selector Sw.Common.	24	+300 v.
25	"(R, W)Set" Selector Sw. Common.	26	
27	L(STZ–12,28)LP–MZ (1,5).	28	(REG–11,12)I–SK(P,T).
29	(STZ–16,32)LP–MZ (2,6).	30	(REG–17,18)I–SK(Q,V).
31	(STZ–20,36)LP–MZ (3,7).	32	(REG–21,22)I–SK (R, W).
33	(STZ–24,40)LP–MZ (4,8).	34	(REG–25,26)I–SK (S, Y).
35		36	Gnd.
37	(φF–38)MC7A.	38	+150 v.
39		40	—150 v.
41		42	—375 v.

Table of connections to Storage Set (STS 2,1) chassis—Continued

Terminal No.	Connects To—	Terminal No.	Connects To—
43	MZ(1–4)A. Tube Pin 3. Fil. "O."	44	MK(P). MK(Q). MK(R). MK(S). Tube Pin 3. Fil. "J."
45	MZ(1–4)A. Tube pin 4. Fil. "P."	46	MK(P). MK(Q). MK(R). MK(S). Tube pin 4. Fil. "K."
47	MS(P, Q). MS(R, S). Tube pin 4. Fil. "L."	48	Cap (1) and Cap (2). Tube pin 3. Fil. "Q."
49	MS(P, Q). MS(R, S). Tube pin 3. Fil. "M."	50	Cap (1) and Cap (2). Tube pin 4. Fil. "R."

Table of connections to Storage Zeroize (STZ) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "M."	2	Fil. "L."
3		4	Fil. "M."
5	Gnd.	6	Fil. "L."
7	+150 v.	8	Clear P.
9	NOTE.—150 v. is supplied to STZ Chassis thru clear-restart Sw. located on set-clear control panel. } 150 v.	10	Clear Q.
11	—15 v.	12	(STS2–27)P.
13	(KB4–34)KBP.	14	Clear R.
15	(KB4–32)KBQ.	16	(STS2–29)Q.
17	(OCL–10)ESI.	18	Clear S.
19		20	(STS2–31)R.
21	(KB4–30)KBR.	22	
23	(KB4–28)KBS.	24	(STS2–33)S.
25		26	
27		28	(STS1–27)T.
29	(KB4–22)KBT.	30	
31	(KB4–20)KBV.	32	(STS1–29)V.
33		34	
35		36	(STS1–31)W.
37	(KB4–18)KBW.	38	
39	(KB4–16)KBY.	40	(STS1–33)Y.
41		42	
43	(CTL–36)RP–EPG.	44	Clear T.
45		46	Clear V.
47		48	Clear W.
49		50	Clear Y.

Table of connections to Test Counter (TCR) chassis

Terminal No.	Connects To—	Terminal No.	Connects To—
1	Fil. "D."	2	Fil. "D."
3	Fil. "F."	4	Fil. "E."
5	Step Switch.	6	Fil. "F."
7	(DCL–28)LP–DEA.	8	A to counter switches.
9	Input-Output Sw.	10	B to counter switches.
11	—15 v.	12	D to counter switches.
13	+150 v.	14	Do.
15	Gnd.	16	E to counter switches.
17	B5.	18	F to counter switches.
19	—150 v.	20	G to counter switches.
21	—90 v.	22	H to counter switches.
23	Input-Output Sw.	24	J to counter switches.
25		26	K to counter switches.
27		28	L to counter switches.
29		30	M to counter switches.
31		32	N to counter switches.
33		34	O to counter switches.
35		36	P to counter switches.
37		38	Q to counter switches.
39		40	R to counter switches.
41		42	S to counter switches.
43		44	T to counter switches.
45		46	U to counter switches.

What is claimed is:

1. In digital computing apparatus, means for executing a plurality of digital computations in a parallel mode, means responsive to the operation of said first means for executing a complementary computation on the result thereof and at least one of the electric manifestations of numbers contributing to said result, parallel comparing means for comparing the result of said complementary operation with another of the electric manifestations of numbers contributing to said result, and means responsive to the result of said comparison for reperforming said digital computations when said comparison departs from zero.

2. In combination, means for executing a first digital computing operation and invariantly thereafter performing a complementary digital computing operation, means for executing a second different digital computing operation and invariantly thereafter performing a complementary digital computing operation with respect to said second operation, means for arbitrarily selecting which of said first and second means shall operate, input apparatus supplying information signals to the foregoing combination, and output apparatus responsive to the output thereof.

3. In combination, means for executing a first digital computing operation and invariantly thereafter performing a complementary digital computing operation, means for executing a second different digital computing operation and invariantly thereafter performing a complementary digital computing operation with respect to said second operation, means for arbitrarily selecting which of said first and second means shall operate, input apparatus supplying information signals to the foregoing combination, and output apparatus responsive to the output thereof under the control of the active means performing the complementary operation.

4. In combination, a first storage register, means for controlling the denominational reference point in said register, a second storage register, means for transferring in a parallel mode the content of said second storage register to said first storage register, means for transferring in a parallel mode at least a part of the content of said first storage register to said second storage register, and means adjusting the denominational reference point in said second register to a predetermined position ancillary to such transferrals.

5. In combination, a storage register, means for controlling the position of the denominational reference point in said register, an accumulator, means responsive to said denominational reference point position control means for governing the position of the denominational reference point in said accumulator, and means for transferring in a parallel mode at least a part of the content of said accumulator to said storage register.

6. In combination, a storage register, means for controlling the position of the decimal point in said register, an accumulator, means responsive to said decimal point position control means for governing the position of the decimal point in said accumulator, and means for transferring in a parallel mode at least a part of the content of said accumulator to said storage register after the creation of a predetermined relationship between decimal point positions.

7. In combination an accumulator for performing arithmetic operations on electric manifestations of first and second values, said accumulator accommodating a predetermined number of denominational orders, a plurality of information storage locations selectively connected to said accumulator, parallel order input means associated with said accumulator for causing the representation of said first value from one of said information locations into said accumulator by electric signals in appropriate ones of said denominational orders, counter means for recording the location of a reference position of said first value relative to a reference position of said second value prior to the entry of said second value, said parallel order input means causing the representation of said second value in said accumulator, a circuit developing shift controlling signals, means jointly responsive to said shift controlling signals and said counter to shift said first value in a parallel mode order by order prior to the entry of said second value whereby said reference positions of said first and second values are in a chosen relationship, parallel output means associated with said accumulator for delivering the result of said arithmetic operation to an information storage location in a parallel mode and means responsive to the completion of said arithmetic operation for aligning the reference position of said result relative to a chosen denominational order of said accumulator prior to the operation of said output means.

8. In combination an accumulator accommodating a predetermined number of denominational orders, said accumulator arranged and constructed to perform a chosen one of a plurality of groups of sequential arithmetic operations in a parallel mode on electric manifestations of first and second values entered therein, a circuit developing shift controlling signals, a counter circuit, means for entering into said counter circuit values representative of the position of reference points associated with said first and second values prior to the entry of said second value, and means jointly responsive to said shift controlling signals and said counter circuit for automatically shifting electric manifestations of said first and second values directly from order to order in said accumulator in a parallel mode prior to the performance of said arithmetic operations, said shifting being in the ascending direction, whereby said reference positions of said first and second values will bear a chosen relationship to one another prior to the performance of said arithmetic operations.

9. In a divider utilizing trial subtraction, a storage register for numerical information signals embracing a plurality of denominational orders adapted to selectively additively and subtractively accommodate signals representing numbers, means for conditioning a plurality of higher denominational orders for one type of said accommodation and for conditioning a plurality of lower denominational orders for the other type of accommodation during trial subtraction, and means responsive to an overdraft occurring as a result of said trial subtraction for interchanging the type of accommodation displayed by said groups of denominational orders.

10. In combination, an electronic accumulator comprising a plurality of denominational orders, shift means for shifting electric manifestations of numbers registered in the orders of the accumulator directly from order to order in a parallel mode, storage means for storing electric manifestations of numbers to be transferred to the accumulator, registration means for registering data representative of the location of denominational reference points of electric manifestations of numbers stored in the storage means, and shift controlling means comprising a counter operatively coupled with and jointly responsive to the registration means and the shift means for controlling the shifting of electric manifestations of numbers registered in the accumulator in a parallel mode.

11. In digital computing apparatus, means for dividing a first electric manifestation of a number by another electric manifestation of a number and storing the result in a register of finite capacity wherein the most significant digits are stored and the least significant digits are discarded when the capacity of said register is exceeded, means for invariantly thereafter multiplying the stored quotient by one of said electric manifestations of numbers, and subtractively combining the product so derived and the other of said electric manifestations of numbers, and means responsive to the departure of the result of

said subtractive combination from zero as a consequence of the discarding of the least significant digits of said result for adding a unit quantity to the least signified denominational order of the result of said subtracted combination.

12. In a computing apparatus, data processing means, means for providing static potentials representing input data in a parallel mode to said data processing means, means for receiving static potentials representing output data in a parallel mode from said data processing means, said data processing means including an accumulator, means for translating said parallel input static potentials to parallel pulse sequences in a chosen code and for applying said pulse sequences as parallel inputs to said accumulator, result storage means, means for translation parallel output static potentials from said accumulator in a chosen code to static potentials in another code and for applying said last named static potentials as a parallel input to said result storage means, means for providing a program of operational steps, each of said steps comprising the performing of an arithmetic operation, checking the result of said operation by executing a complementary computation on said result, transferring said result to said result storage means and initiating a next step, and means responsive to said program means for enabling data transfer in a parallel mode from said storage means to said input translating means and means for transferring data contained in said result storage means to said output data receiving means in a parallel mode at the completion of said program.

13. In a computing apparatus, data processing means, means for providing static potentials representing input data to said data processing means, means for receiving static potentials representing output data from said data processing means, said data processing means including an accumulator, means for translating said input static potentials to pulse sequences in a chosen code and for applying said pulse sequences as an input to said accumulator, result storage means, means for translating output pulse sequences from said accumulator in a chosen code to static potentials and for applying said static potentials as an input to said result storage means, means for providing a program of operational steps, each of said steps comprising the performing of an arithmetic operation, checking the result of said operation, transferring the result to said result storage means, and initiating a next step, means for storing an electric manifestation of an arithmetic operation, enabling means responsive to said program means for causing said electric manifestation of said operations to appear as combinations of static potentials at said input translating means, means for shifting the contents of said accumulator in accordance with chosen decimal point location data, means associated with said storage means for setting the decimal point location therein and means for transferring the data contained in said result storage means to said output data receiving means at the completion of said program.

14. In a computing apparatus as defined in claim 13 wherein said enabling means includes means for supplying chosen pulse groups to said input translating means in response to actuating signals from said program means.

15. In a computing apparatus as defined in claim 13 wherein there is further included means responsive to said program means for conditioning said accumulator to add or subtract.

16. In a computing apparatus as defined in claim 13 and further including means for zeroizing said result storage means.

17. In a computing apparatus as defined in claim 13 where there is further included means for the halting of a calculation at a predetermined point therein.

18. In a computing apparatus as defined in claim 13 wherein there is included means associated with said program means for sequentially enabling each step in an operation.

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