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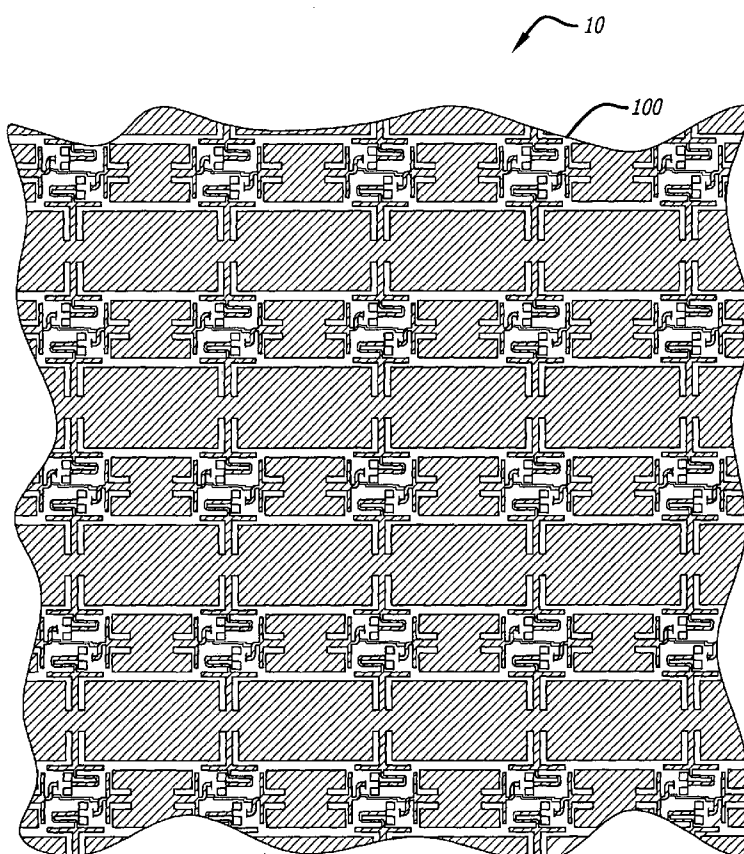
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(54) Title: AMPLIFIED PATCH ANTENNA REFLECT ARRAY



(57) Abstract: A reflect array antenna including a plurality of unit cells. Each cell includes first, second, third and fourth patch antenna segments. An amplifier is coupled between said first patch segment and the second patch segment or the third patch segment and the fourth patch segment. At least one of the patch antenna segments of a first unit cell is electrically connected to a patch antenna segment of a second unit cell. The first patch antenna segment of a first unit cell is electrically connected to a third patch segment of a second unit cell. Each patch segment of each unit cell is electrically connected to a patch segment of a neighboring cell. The first and third patch segments are the input terminals of each cell and the second and fourth patch segments of each cell are the output terminals. The output terminals of each cell are coupled to the output terminals of neighboring cells. This provides an output patch antenna, of greater area, fed by multiple cells.

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AMPLIFIED PATCH ANTENNA REFLECT ARRAY

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BACKGROUND OF THE INVENTION

Field of the Invention:

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The present invention relates to antennas. More specifically, the present invention relates to millimeter wave reflect patch antennas and arrays thereof and components therefor.

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Description of the Related Art:

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As noted by the Institute of Electrical and Electronic Engineers (IEEE): "The millimeter-wave region of the electromagnetic spectrum is usually considered to be the range of wavelengths from 10 millimeters (0.4 inches) to 1 millimeter (0.04 inches). This means they are larger than infrared waves or x-rays, for example, but smaller than radio waves or microwaves. The millimeter-wave region of the electromagnetic spectrum corresponds to radio band frequencies of 30 GHz to 300 GHz and is sometimes called the Extremely High Frequency (EHF) range. The high frequency of millimeters waves as well as their propagation characteristics (that is, the ways they change or interact with the atmosphere as they travel) make them useful for a variety of applications including transmitting large amounts of computer data, cellular communications, and radar." See <http://www.ieee-virtual-museum.org/collection/tech.php?id=2345917&lid=1>.

For current more demanding applications, such as 'active denial', higher
30 power millimeter waves, i.e. waves in the range of tens to thousands of watts, are
required. Prior attempts to produce high power millimeter wave energy with solid-
state devices have included waveguide and microstrip power combining. At
millimeter wave frequencies, this method of combining typically produces
unsatisfactory results due to heavy losses in the waveguide and/or microstrip medium.

35 Another approach is a spatial array technique. This technique has shown some
promise. However, spatial arrays have not yet produced the power density levels that
are required for the more demanding applications mentioned above.

One current approach involves the use of a reflect array amplifier. The reflect
array has independent unit cells, each containing its own input antenna, power
40 amplifier, and output antenna. These unit cells are then configured into an array of
arbitrary size. Reflect arrays overcome feed losses by feeding each element via a
nearly lossless free-space transmission path. As disclosed and claimed in U.S. Patent
Application entitled REFLECTIVE AND TRANSMISSIVE MODE MONOLITHIC
MILLIMETER WAVE ARRAY SYSTEM AND IN-LINE AMPLIFIER USING
45 SAME, filed 12/12/2003 by K. Brown *et al.* (Atty. Docket No. PD 01W176A), the
teachings of which are hereby incorporated herein by reference, reflect arrays differ
from conventional arrays in that the input signal is delivered to the face of the array
via free space, generally from a small horn antenna.

An active reflect array consists of a large number of unit cells arranged in a
50 periodic pattern. Each reflect array element is equipped with two orthogonally-
polarized antennas, one for reception and one for transmission. That is, reflect arrays
typically receive one linear polarization and radiate the orthogonal polarization, e.g.,
the receive antenna receives only vertically-polarized radiation and the transmit
antenna transmits only horizontally-polarized radiation.

55 When integrated with the power-generating electronics on a thin
semiconductor substrate, such antennas tend to have narrow bandwidths and high
losses due to large surface currents. The size of each unit cell is constrained by the

need to avoid grating lobes; for a fixed array whose main beam is in the broadside direction, each unit cell may be no more than approximately 0.8 wavelengths on a side.

Higher power levels are attained by combining the outputs of multiple transistors. The drawback of this approach is that the power combiners themselves take up valuable area on the semiconductor wafer that could otherwise be occupied by power-generating circuitry.

Hence, a need remains in the art for improved systems and methods for generating high power millimeter wave beams. Specifically, a need remains in the art for a reflect array antenna capable of generating high power millimeter wave energy without significant loss.

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SUMMARY OF THE INVENTION

The need in the art is addressed by the reflect array antenna of the present invention. In the illustrative embodiment, the array includes a plurality of unit cells. Each cell includes first, second, third and fourth patch antennas. An amplifier is coupled between said first patch and the second patch or the third patch and the fourth patch. At least one of the patch antennas of a first unit cell is electrically coupled to a patch antenna of a second unit cell.

In a more specific embodiment, the first patch antenna of a first unit cell is electrically coupled to a third patch of a second unit cell. Each patch of each unit cell is electrically coupled to a patch of a neighboring cell. In the illustrative embodiment, the first and third patches are the input terminals of each cell and the second and fourth patches of each cell are the output terminals. In accordance with the invention, the output terminals of each cell are coupled to the output terminals of neighboring cells. This provides an output antenna, of greater area, fed by multiple cells.

In the illustrative embodiment, the amplifiers are implemented with MHEMT (Metamorphic High Electron Mobility Transistor) transistors. Direct current for the amplifiers is supplied via the output terminals (the second and fourth patch antennas) of neighboring cells. Input bias for each amplifier is supplied to each cell via the first or third patches of neighboring cells.

The amplifier and patches of each cell are optimized as one unit to mitigate interference between the power amplifier and the patches. In accordance with the invention, the array antenna is terminated to appear as an infinite antenna.

The inventive array operates in reflection mode. That is, the inventive array receives a low power radio frequency (RF); microwave or millimeter wave signal, amplifies it, and then re-radiates it at a much higher power level. This technique is used to generate high power at millimeter wave frequencies without suffering the debilitating losses one gets when using a waveguide or microstrip line feed network.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a topological view of a reflection mode amplified patch antenna unit cell array constructed in accordance with an illustrative embodiment of the present teachings.

Figure 2 is a schematic diagram of a unit cell of the array of Figure 1.

Figure 3 is a schematic diagram of an alternative embodiment of the unit cell of Figure 2 using MHEMT technology.

Figure 4 is a topological view of a reflection mode amplified patch antenna array using unit cells illustrated in Figure 3 constructed with MHEMT technology.

Figure 5 is a magnified view of a corner of the array of Figure 4 illustrating patch termination and use for DC bias.

115 Figure 6 shows an amplified patch antenna array unit cell topology in accordance with an alternative embodiment of the present teachings.

DESCRIPTION OF THE INVENTION

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Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

125 While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present
130 invention would be of significant utility.

Figure 1 is a topological view of a reflection mode amplified patch antenna unit cell array constructed in accordance with an illustrative embodiment of the present teachings. The amplified patch antenna array 10 of the present invention is comprised of many unit cells 100 combined together to form an array. By
135 combining unit cells 100, an array 10 of arbitrary size is implemented.

Figure 2 is a schematic diagram of a unit cell 100 of the array 10 of Figure 1. Each unit cell is fabricated in a conventional manner by depositing a layer of metallization (such as gold or other suitably conductive material) on a substrate (of Gallium Arsenide or other suitable dielectric) to provide a circuit. The unit cell 100
140 has two opposing input patch antenna segments 102 and 104, two opposing amplifiers 106 and 108 and two opposing output patch antenna segments 110 and 112. The first input patch antenna segment 102 is coupled to an input (gate) terminal of the first amplifier 106. In the illustrative embodiment, the first

amplifier is a MHEMT transistor coupled with appropriate bias and matching
145 networks. The output (source) terminal of the transistor 106 is connected to the first
output patch 106. The drain terminal is connected to the backside ground plane
through metalized via holes. The second input patch 104, second amplifier 108 and
second output patch 112 mirror the arrangement of the first input patch 102, first
amplifier 106 and first output patch 110. The gate terminals of the first and second
150 amplifiers 106 and 108 are coupled via a gate bias resistor 114. This allows the gate
bias voltage to propagate to the next unit cell through the shared input patch
antenna.

Notches (such as 116 and 118) change input impedance and are therefore
provided for impedance matching as is common in the art.

155 The array of Figure 1 is formed by fabricating a plurality of unit cells and
combining the patch antenna segments thereof. That is, each patch segment of each
unit cell is electrically coupled to a patch of a neighboring cell to form the overall
patch antenna. As illustrated in Figure 1, adjacent unit cells in a row share input
patch segments and output patch segments. Hence, the input patch segments in this
160 topology double in size to form an input patch antenna and the output patch
segments combine into large multiple-terminal patch antennas (depending upon the
size of the array), one for each row. For example, in the illustrative embodiment, in
accordance with the present teachings, cells in adjacent rows in the array share a
large single output patch antenna. As an alternative, the large output patch could
165 be implemented via columns instead of rows without departing from the scope of
the present teachings.

The large size of the output patches is very advantageous in that it should
have very low loss and a high bandwidth. The input patch antenna is smaller and
thus has more loss and a narrower bandwidth. Note that the larger patch could be
170 possibly used for the input. However, since the output is high power, the efficiency
of the array is optimal if the large patch is used for the output. A lower efficient

input patch antenna can be compensated for by including an additional gain stage in the amplifier without significantly detracting from the overall unit cell efficiency.

Also note that the amplifier drain bias comes directly through the output
175 patch antenna. The amplifier gate bias comes through the input patch antennas. That is, each input patch antenna along a row in the array is DC interconnected through the gate bias resistor 114. Thus the array 100 may be fed with DC along the left, right, or both sides of the chip.

While each cell is shown in Figure 2 with dual amplifiers, those skilled in
180 the art will appreciate that the invention is not limited thereto. One or more cells may be implemented with a single amplifier or multiple amplifiers. With a single amplifier design, one input patch may feed one or more output patches of a cell. In the array of Figure 1, the unused input patches in a cell could be used by an adjacent cell. Likewise, any unfed output patches could be fed by other cells in the shared
185 row. Although the unit cell shown in Figs. 2 and 3 include a pair of single stage amplifiers, multiple stage amplifiers can also be utilized within the scope of this invention.

In the best mode, the amplifier and patches of each cell are optimized as one unit to mitigate interference between the power amplifier and the patches. In
190 accordance with the invention, the array antenna is terminated to appear as an infinite antenna.

Figure 3 is a schematic diagram of an alternative embodiment of the unit cell of Figure 2 using MHEMT (Metamorphic High Electron Mobility Transistor) technology. MHEMT technology is known in the art. For more on MHEMT
195 technology, see the following illustrative sites <http://en.wikipedia.org/wiki/MHEMT> and <http://www.compoundsemiconductor.net/articles/news/5/9/39/1>. In Figure 3, the first and second transistors 206 and 208 are implemented in MHEMT. Note the inclusion of tuning elements 214 in this embodiment.

Figure 4 is a topological view of a reflection mode amplified patch antenna array 10' using unit cells illustrated in Figure 3 constructed with MHEMT technology.

Figure 5 is a magnified view of a corner of the array of Figure 4 illustrating patch termination and use for DC bias. Figure 5 shows how the array is DC biased and how the patch antennas are terminated in accordance with the present teachings. Note that the patch antennas receive and radiate RF (radio frequency) energy and transport DC bias. Therefore, the patch antennas must be connected to the DC bias in such a way as to not disrupt the RF functionality thereof. In addition, from an RF perspective, the array is designed as an infinite array using a conventional design tool such as HFSS (High Frequency Structure Simulated) or Designer both by Ansoft Inc. of Pittsburgh, Pennsylvania.

For example, the output patch 210 along the top of the chip is terminated into an RF ground with multiple RF shorts 216. The patch antennas in this invention are fed on both sides. In order to properly combine the powers going into the patch, the amplifier output voltages (feeding the patch antenna inputs on opposing sides of the patches) are 180 degrees out-of-phase. Due to this 180 degree out-of-phase feeding arrangement, a virtual short exists along the centerline of each patch antenna. Therefore, in order to properly terminate the patch antenna array, an RF grounded half-length patch antenna is used along the top (and bottom) ends of the chip for the output patches.

The input patches are terminated in a likewise fashion at the left and right side of the chip with multiple RF shorts 218. In addition, the input patches on the left and right sides of the chip are fed with a DC gate bias voltage.

Finally, the output patch 212 at the left and right side of the chip is terminated into an RF open circuit via a termination 220. This is accomplished by connecting a quarter-wavelength shorted line at each end of the output patch. This line is also used to feed the output patch 212 with DC drain bias. Note that the output patches of one

row of cells 210 and the output patches of a lower row of cells 212 are DC electrically and, in the illustrative embodiment, physically coupled.

This topology offers more room for the amplifiers by sharing antennas
230 between unit cells. It offers the potential to produce more power than previous reflect array topologies.

Figure 6 shows an amplified patch antenna array unit cell topology in accordance with an alternative embodiment of the present teachings. Here the input patch antennas 302 and 304 are also long and continuous (as per the output patch
235 antennas 310 and 312). The input (or output) patch antennas are deployed over the output (or input) patch antennas via “air bridges” 316 – 322 (even numbers only) so they do not electrically touch each other. In this alternate topology, the gate bias resistor would not be needed, since the input patch is continuous as shown.

The inventive array operates in reflection mode. That is, it receives a low
240 power RF, microwave or millimeter wave signal, amplifies it, and then re-radiates it at a much higher power level. This technique is used to generate high power at millimeter wave frequencies without suffering the debilitating losses associated with use of a waveguide or microstrip line feed network.

Thus, the present invention has been described herein with reference to a
245 particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present
250 invention.

Accordingly,

WHAT IS CLAIMED IS:

[EUROSTYLE] CLAIMS

1. A reflect array antenna (10) characterized by:
a plurality of unit cells (100), each cell comprising:
 - a first patch antenna segment (102);
 - a second patch antenna segment (110);
 - 5 a third patch antenna segment (104);
 - a fourth patch antenna segment (112); and
 - an amplifier (106) coupled between said first patch (102) and said second patch (110) or said third patch (104) and said fourth patch (112);wherein at least one of said patch antenna segments of a first unit cell is
10 electrically coupled to a patch antenna segment of a second unit cell.
2. The invention of Claim 1 wherein said first patch antenna segment (102) of a first unit cell is electrically coupled to a third patch (104) of a second unit cell.
3. The invention of Claim 1 wherein each patch antenna segment of each unit cell is electrically coupled to a patch antenna segment of a neighboring cell.
4. The invention of Claim 3 wherein the second patch antenna segment (110) of each cell is an output terminal thereof.
5. The invention of Claim 4 wherein the fourth patch antenna segment (112) of each cell is an output terminal thereof.
6. The invention of Claim 5 wherein the output terminals of each cell are electrically coupled to the output terminals of neighboring cells.

7. The invention of Claim 1 wherein an input terminal of said first amplifier (106) of each cell is coupled to said first patch antenna segment (102) thereof.

8. The invention of Claim 7 wherein an output terminal of said first amplifier (106) of each cell is coupled to said second patch antenna segment (110) thereof.

9. The invention of Claim 8 wherein an input terminal of said second amplifier (108) of each cell is coupled to said third patch antenna segment (104) thereof.

10. The invention of Claim 9 wherein an output terminal of said second amplifier (108) of each cell is coupled to said fourth patch antenna segment (112) thereof.

11. The invention of Claim 10 wherein said first and said third patches (102, 104) of each cell are input patches and said second and fourth patches (110, 112) of each cell are output patches.

12. The invention of Claim 11 further including a tuning element (214) between at least one of said patches and at least one of said amplifiers.

13. The invention of Claim 12 wherein each of said amplifiers includes a field-effect transistor.

14. The invention of Claim 13 wherein said input terminals of said amplifiers are coupled.

15. The invention of Claim 14 wherein said input terminals of said amplifiers are coupled via a resistor (114).

16. The invention of Claim 1 wherein a first bias current for said amplifier (106) is applied to each cell via the second or fourth patches thereof from second and/or fourth patches of neighboring cells.

17. The invention of Claim 1 wherein a first bias current for said amplifier (106) is applied to each cell via the second and fourth patches from second and/or fourth patches of neighboring cells.

18. The invention of Claim 1 wherein a bias voltage for said amplifiers (106) is applied to each cell via the first or third patches thereof via first and/or third patches of neighboring cells.

19. The invention of Claim 1 wherein a bias voltage for said amplifier (106) is applied to each cell via the first and third patches thereof from first and/or third patches of neighboring cells.

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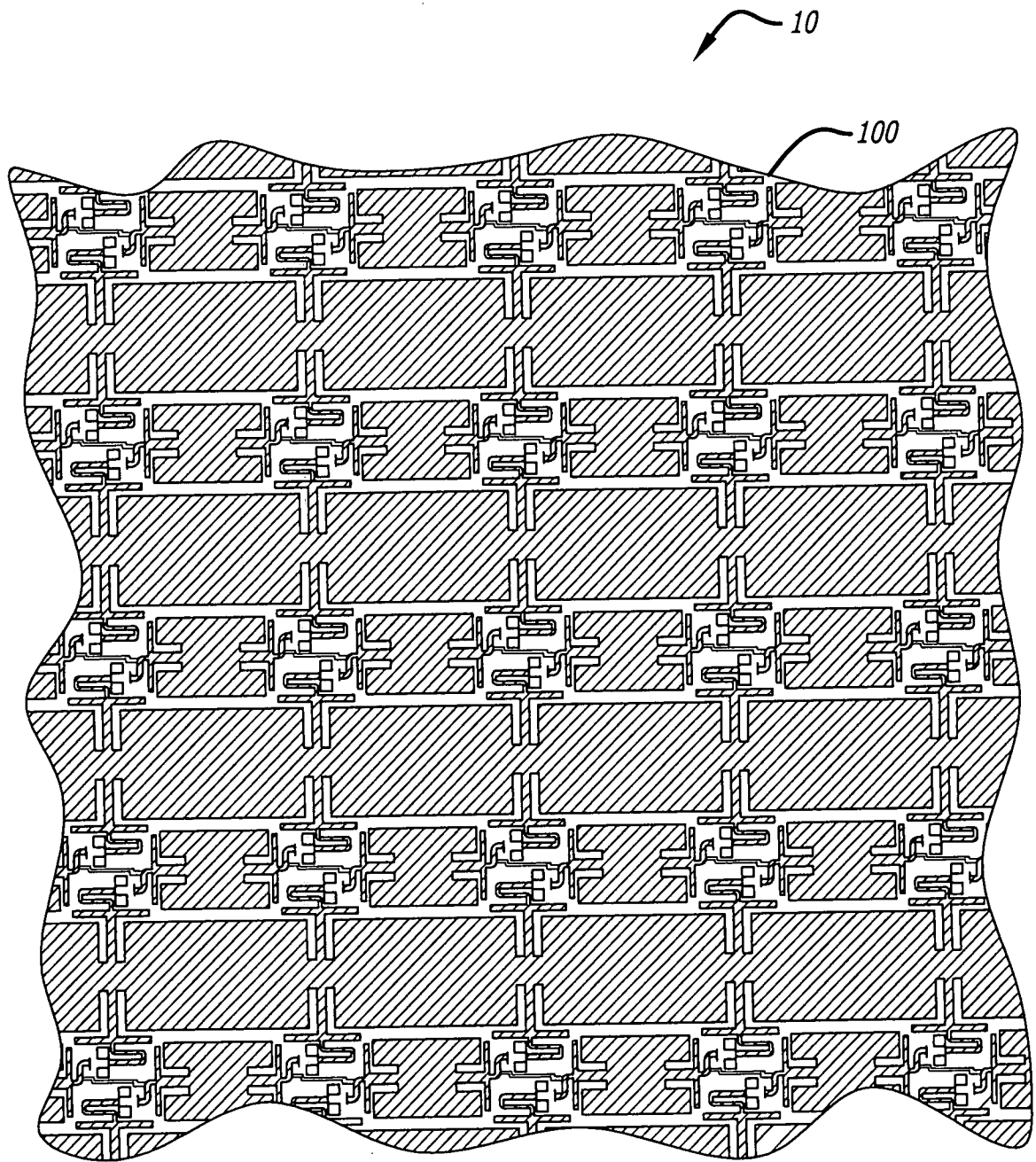
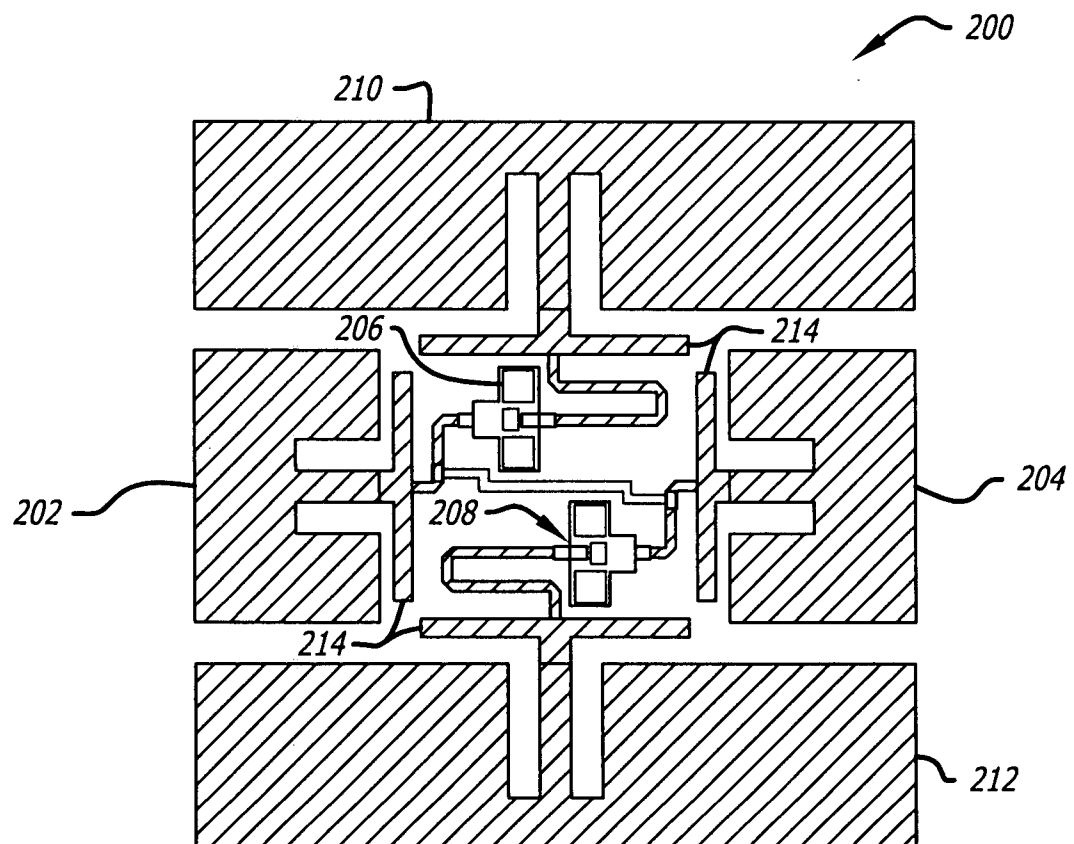
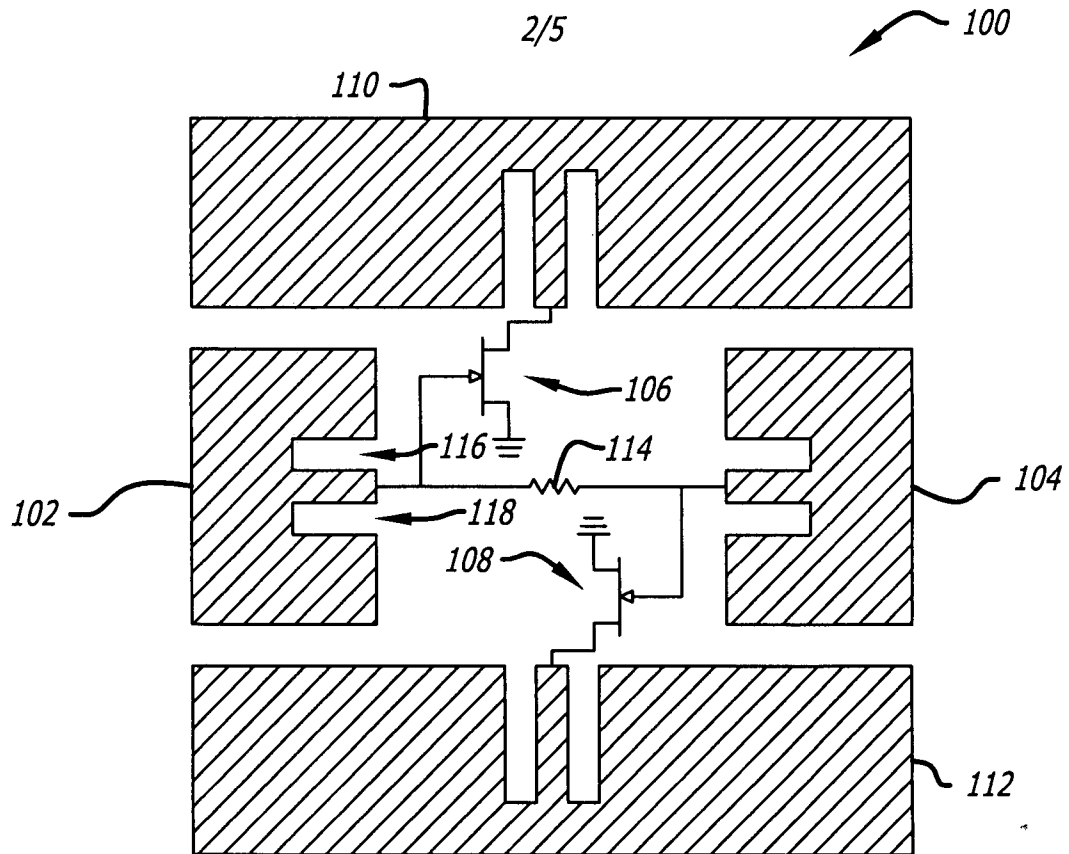


FIG. 1



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10'

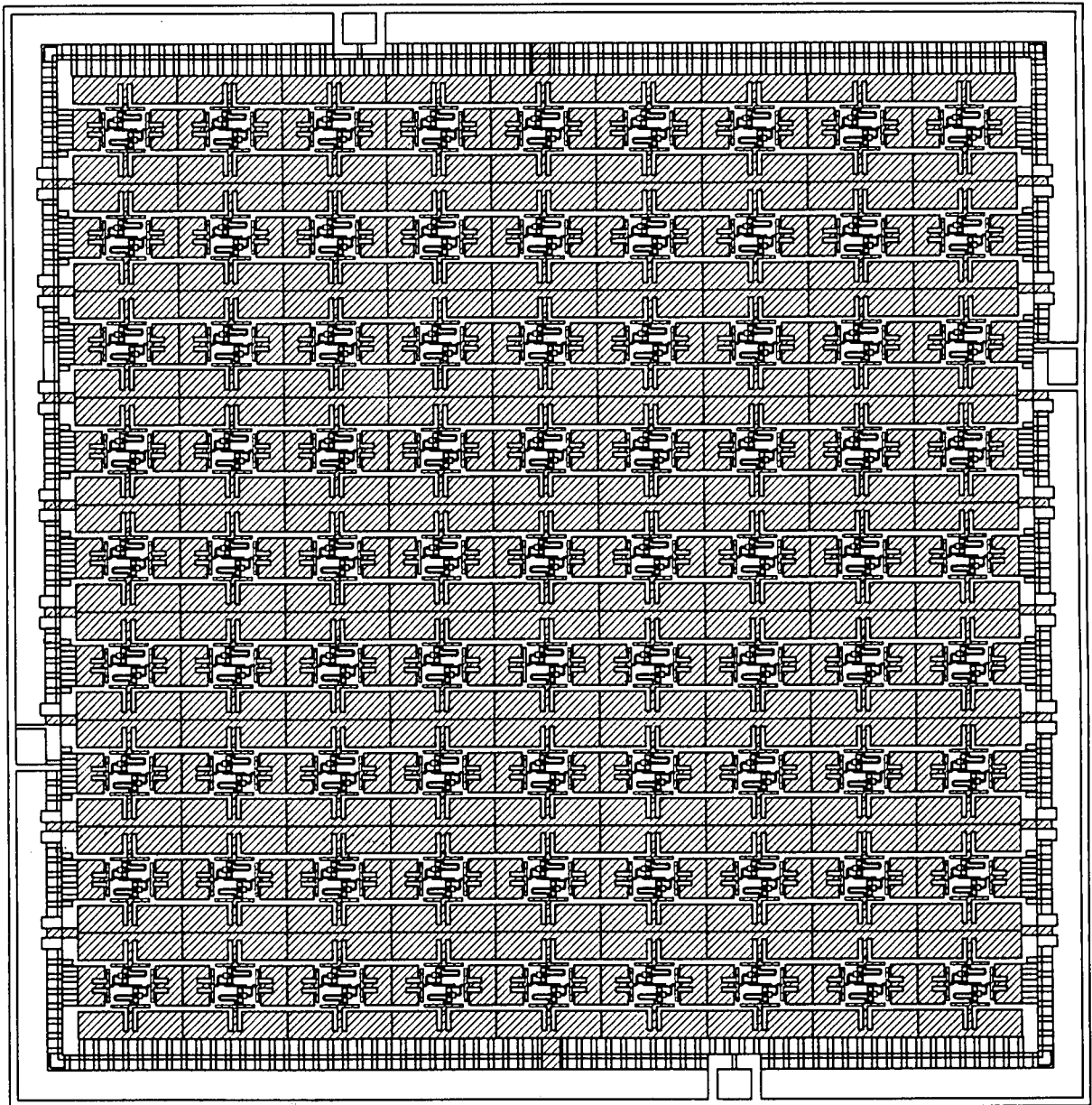


FIG. 4

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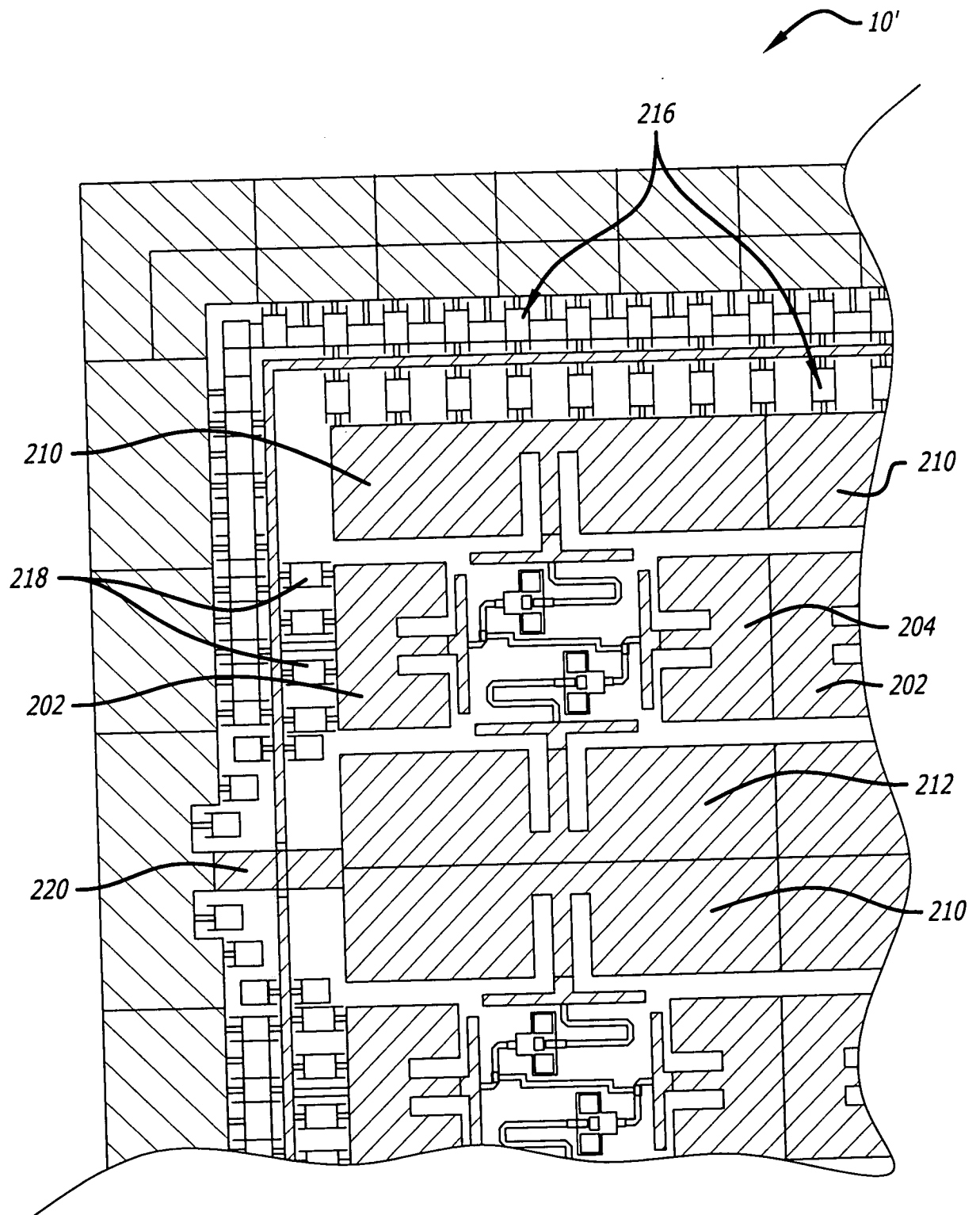


FIG. 5

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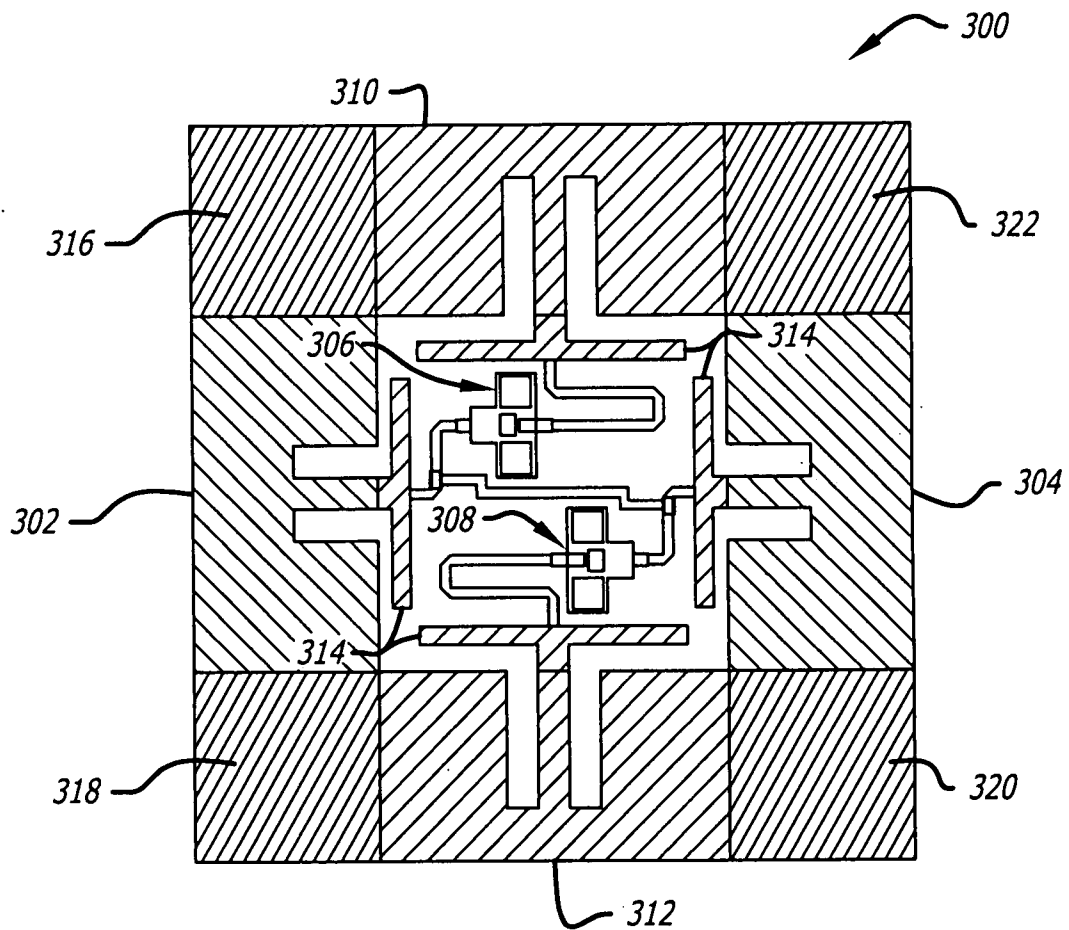


FIG. 6