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(54) **Title:** METHOD IN ELIMINATING POLYCIDE STRINGER IN DOUBLE POLY ANALOG MIXED SIGNAL (AMS) DEVICE

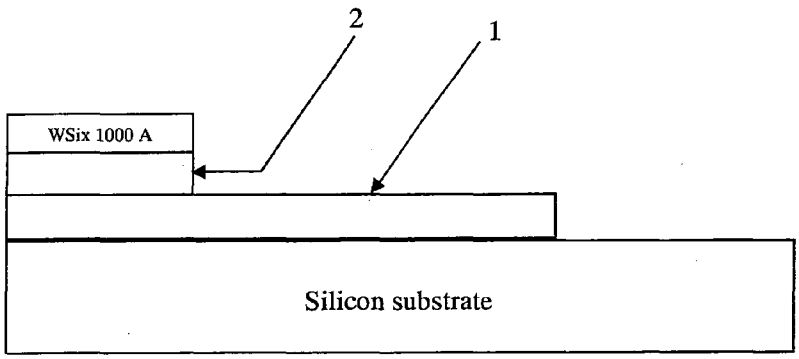

Figure 2b

(57) **Abstract:** The invention relates to a method of eliminating stringers (3) formed during a fabrication of poly-insulator-poly (PIP) Analog Mixed Signal (AMS) device using 0.35μm CMOS process technology. Using 1500A polyl (1) thickness with fine tuning of poly2 (2) etch process condition in the tungsten silicide and poly etch steps had been proven successful in eliminating the stringer (3) completely. The tungsten overetch was increased from 30% to 80%. The poly and WSix etch rates in the poly etch step were made about equal by increasing pressure from 4mTorr to 12mTorr and RF power was increased from 480 Watt to 620 Watt. In addition, the poly overetch step was increased from 90 to 130 seconds.

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METHOD IN ELIMINATING POLYCIDE STRINGER IN DOUBLE POLY ANALOG MIXED SIGNAL (AMS) DEVICE

1. TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to elimination of polycide stringer, and more particularly to a method of eliminating the polycide stringer formed during the fabrication of Poly-Insulator-poly (PIP) Analog Mixed Signal (AMS) device using 0.35 μm CMOS process technology.

2. BACKGROUND OF THE INVENTION

A memory device for storing data has a great significance in a data processing system. Memory devices, such as random access memory (RAM), read-only memory (ROM), and the like, are known in the art. Non-volatile memory devices, and particularly so-called "flash" memory devices, have become increasingly more popular in data storage applications. A flash memory is a non-volatile memory, which can preserve data within the memory even when an external power supply is lost. Recently, because flash memory is re-writable and re-erasable, it has been widely applied in the fabrication of electrical products, such as mobile phones, digital cameras, video players, personal digital assistants (PDA) or system on a chip (SOC).

In the fabrication of PIP AMS devices using 0.35um CMOS process technology, the top plate capacitor (poly2) is formed by depositing polysilicon and tungsten silicide (WSix) sequentially, which is then patterned and etched using reactive ion etching (RIE) method. A type of residue was found alongside the PIP capacitor structure after the poly2 etching process. An electron microscope (FESEM) cross-sectional view (Figure 1) of the capacitor and Energy dispersive X-ray spectroscopy (EDS) analysis confirmed that the residue consisted of poly and tungsten silicide material, hence called the polycide stringer. It was understood that the stringer was left unetched during poly2

etching process due to high topography of the PIP structure. The presence of polycide stringer may cause resistive short or unwanted electrical connection within the device, which will consequently deteriorate the operational characteristics and reliability of the PIP AMS devices.

In US-A-5,342,801, there is disclosed a fabrication of EPROM devices in a way which avoids the creation of polysilicon stringers. More specifically, the plasma etching process of the invention, where instead of providing only vertical or anisotropic etching, it also provides controlled isotropic etching. In other words, horizontal etching can take place simultaneously with vertical etching, however, at a controlled and therefore, slower rate. Therefore, the polysilicon are eliminated during the row space forming etching process because material removal occurs in the horizontal direction as well as the vertical direction.

In US-A-5,723,374, it is disclosed a method of forming dielectric spacer along the slope of the bit line contact hole edge to prevent poly stringers in DRAM technology.

US-A-5,933,729 disclosed method of preventing the formation of poly stringers during the fabrication of a memory device by reducing the height of the ONO (oxide-nitride-oxide) fence during a self-aligned etch ("SAE") step. The shortened ONO fence provides reduced lateral shielding of polysilicon material during a subsequent polysilicon etch, thereby preventing poly stringers from being formed and improving the manufacturability of the memory device. According to one aspect of the invention, a new ONO etch recipe is utilized which exhibits a substantially greater ONO-to-polysilicon selectivity. Consequently, a longer overetch of the ONO layer may be conducted without substantially impacting the underlying polysilicon. The overetch reduces the height of the ONO fence and thereby reduces its lateral shielding of polysilicon. The reduced lateral shielding prevents the formation of poly stringers during a subsequent etch of the polysilicon.

There are quite a number of other US patent documents disclosing methods of eliminating stringers which formed during fabricating of memory devices. However, the proposed prior methods are either exceedingly complicated that require various steps thus raised the issue of complexity and cost, or difficult to perform thus raised the issue of reliability. The present invention overcomes such problems mentioned above by optimizing polysilicon gate etching condition.

3. SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method of fabricating an analog mixed signal (AMS) using CMOS technology to solve the above-mentioned problems.

It is another object of the present invention to provide a method of fabricating a stringerless analog mixed signal (AMS) to achieve better reliability.

These and other objects of the present invention are achieved by,

A method for eliminating formation of stringers in an analog mixed signal (AMS) device comprising the steps of:-

forming of poly-insulator-poly capacitor having first polysilicon (poly1) (1) layer set at the bottom and second polysilicon (poly2) (2) layer set at the top;

a dielectric layer sandwiched between said poly1 (1) and said poly2 (2) layer, said dielectric layer includes an oxide-nitride-oxide (ONO);

characterized in that,

said polysilicon bottom layer (poly 1) (1) having height of not more than 1500A, said polysilicon top layer (poly2) (2) is subjected to that etching process comprises of tungsten overetch increased to at least 80 %, maintaining the etching

rate of said poly2 (2) and tungsten silicide material (WSix) while increasing pressure from 4mTorr to 12mTorr, increasing RF power from 480 Watt to 620 Watt and poly overetch step increased from 90 seconds to 130 seconds.

Preferably, poly1 (1) is undoped polysilicon film deposited on top of the Field Oxide after Sacrificial Oxidation.

More preferably, poly 2 (2) is a combination of doped poly and tungsten silicide films.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Other aspect of the present invention and their advantages will be discerned after studying the Detailed Description in conjunction with the accompanying drawings in which :

FIG 1 shows FESEM cross-section image of poly stringer defects.
FIG 2 shows FESEM cross-section image of stringer completely eliminated.

5. DETAIL DESCRIPTION OF THE DRAWINGS

A poly-insulator-poly (PIP) Analog Mixed Signal (AMS) device using 0.35μm CMOS technology features has been fabricated. The advantage of a PIP capacitor as compared to the other types of capacitor is its higher capacitance density value. The PIP capacitor consists of a thin oxide-nitrite-oxide (ONO) film sandwiched between two polysilicon films. The bottom polysilicon (poly1) layer (1) is the capacitor bottom plate, the thin ONO film stack acts as a dielectric layer and the capacitor top plate (poly2) (2) is a combination of doped poly and tungsten silicide films.

The fabrication of the PIP module starts with a layer of undoped polysilicon film deposited on top of the Field Oxide after Sacrificial Oxidation, to

form the bottom plate capacitor. Then, the poly layer is implanted with phosphorus to achieve the targeted sheet resistance. The implanted poly is then annealed at 800°C for 30 minutes to activate the dopants. The next process step is the formation of the dielectric, ONO layer. 40A of thermal oxide is grown on the poly1 film followed by deposition of 200A LPCVD silicon nitride. The final oxide layer is formed on the nitride surface during the gate oxidation process. The next step is to pattern and etch the polysilicon bottom plate (poly1) (1). The top ONO layer is then etched away using dry oxide etcher followed by polysilicon reactive ion etch. The subsequent process step is to form the capacitor top plate (poly2) (2). The capacitor top plate will also function as the Logic Gate material in the CMOS area. A layer of LPCVD polysilicon film is deposited over the patterned poly1 (1) structure. A PECVD tungsten silicide (WSix) film is then deposited followed by deposition of a thin PECVD silicon oxynitride (SiON). The SiON film acts as an anti-reflective coating (ARC) during the polysilicon gate patterning (lithography) process. The poly2 (2) film is then patterned and etched using a polysilicon reactive ion etcher. The process flow continues with a standard logic CMOS process.

An electron microscope (FESEM) cross-section (Figure 1) of the capacitor and EDS analysis confirmed that stringer (3) was formed during the poly2 (2) etching process due to topography of the PIP structure. The stringer (3) was consisted of poly and tungsten silicide material. The presence of poly stringer (3) defect could deteriorate the operational characteristics and reliability of the AMS device. Therefore, several experimental approaches were performed to find a solution to this issue. However, processing on both PIP module and CMOS device simultaneously is challenging. A process which avoids the formation of poly stringer (3) as well as maintaining a good polysilicon gate profile has to be developed.

Several experiments were conducted in order to solve the above mentioned problems. The first technique attempted in eliminating the stringer (3) was by increasing the overetch time in the tungsten etch recipe. Initial test using a

50% tungsten overetch step had resulted in undercut of polycide gate profile in logic area. Therefore, the etch selectivity of WSix:Poly is improved from the current selectivity of 1:1. The current baseline recipe for tungsten etch uses a combination of Cl_2, O_2 and N_2 gases at 1400 Watt RF power and 8mTorr pressure. A few experiments had been performed varying some factors such as gas flow, pressure, and power setting in search of a good parameter combination to improve the WSix:Poly selectivity. Additional gas such as SF_6, CF_4 and Ar were also tested to check their effect on WSix and Poly etch rate.

The second approach was aimed at reducing the WSix thickness by tapering the poly1 sidewall profile to an angle of about 75°. The current etching recipe for the poly1 (1) etch produced a near vertical sidewall profile. The baseline etch recipe consisted a combination of Cl_2 and HBr gases at 1:1.6 ratio, 480 Watt RF source power, 80 Watt RF bias power and 8mTorr pressure. Three factors i.e. Cl_2 and HBr gas flow and pressure were varied. The sidewall angle produced was then calculated based on FESEM cross-section. The best poly1 (1) taper profile achieved was then integrated with the standard tungsten etch recipe and the height of the stringer remained was then measured from the FESEM cross-section.

Another technique to reduce the WSix thickness at the poly1 sidewall is by reducing the thickness of the poly1 (1) itself. In order to find the optimum poly thickness to be used, three thicknesses were experimented. Three types of PIP stack structure were prepared having poly1 (1) thickness 2500A, 2000A and 1500A. The baseline poly2 (2) etch recipe was used in the experiment for all three types of structures. In order to verify the effectiveness of each technique in eliminating the stringer, FESEM cross-section were carried out to measure the remaining height of the stringer (3).

Another approach gave a better result in term of reducing the height of the stringer (3). Using 1500A poly1 (1) thickness with baseline poly2 (2) etch recipe, the height of the stringer (3) was reduced by 66%. A new optimized poly2 (2)

etch process was developed. The tungsten overetch was increased from 30% to 80%. The poly and WSix etch rates in the poly etch step were made about equal by increasing pressure from 4mTorr to 12mTorr and RF power was increased from 480 Watt to 620 Watt. In addition, the poly overetch step was increased from 90 to 130 seconds. FESEM cross-section view (Figure 2) of the PIP stack verified that the stringer (3) is no longer exists. A FESEM cross-section of the poly gate profile at the CMOS area also showed no poly undercut. The experimental results from the three types of approaches are summarized in Figure 3.

Figure 3 shows a summarization table of experiments undertook in optimizing the etching process for elimination of the stringers as mentioned above. The figures clearly show the improvement made on the etching process had resulted in reduction of the height of the stringers until the last process which the stringers had completely eliminated.

While a particular form of the present invention has been illustrated and described, it will be apparent that many varying embodiments with various modification can be made without departing from the scope of the invention. Therefore, it is understood that the detail herein are to be interpreted as illustrative and not in a limiting sense.

CLAIM

1. A method for eliminating formation of stringers in an analog mixed signal (AMS) device comprising the steps of:-

forming of poly-insulator-poly capacitor having first polysilicon (poly1) (1) layer set at the bottom and second polysilicon (poly2) (2) layer set at the top;

a dielectric layer sandwiched between said poly1 (1) and said poly2 (2) layer, said dielectric layer includes an oxide-nitride-oxide (ONO);

characterized in that,

said polysilicon bottom layer (poly 1) (1) having height of not more than 1500A, said polysilicon top layer (poly2) (2) is subjected to that etching process comprises of tungsten overetch increased to at least 80 %, maintaining the etching rate of said poly2 (2) and tungsten silicide material (WSix) while increasing pressure from 4mTorr to 12mTorr, increasing RF power from 480 Watt to 620 Watt and poly overetch step increased from 90 seconds to 130 seconds.

2. A method for eliminating formation of stringers in a memory device as claimed in Claim 1, further characterized in that said poly1 (1) is undoped polysilicon film deposited on top of the Field Oxide after Sacrificial Oxidation.

3. A method for eliminating formation of stringers in a memory device as claimed in Claim 1, further characterized in that said poly 2 (2) is a combination of doped poly and tungsten silicide films.

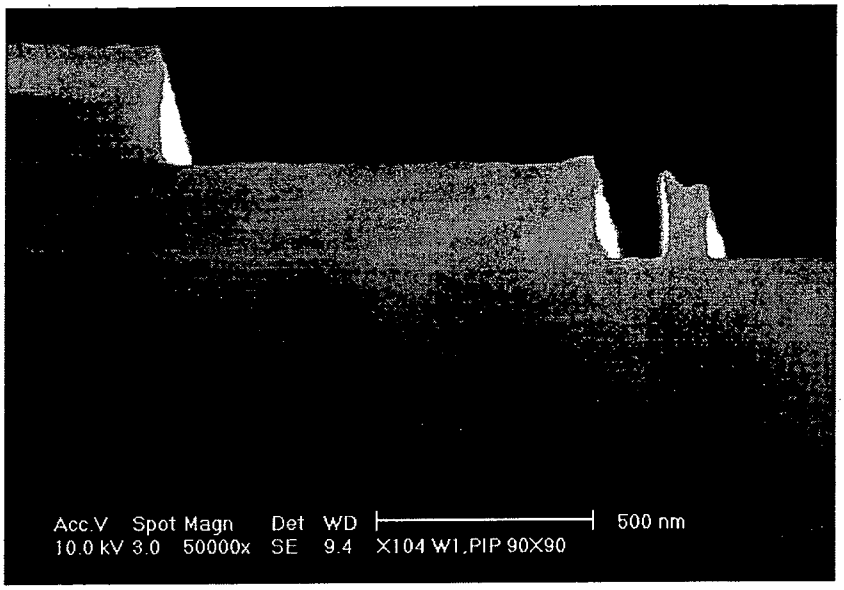

Figure 1a

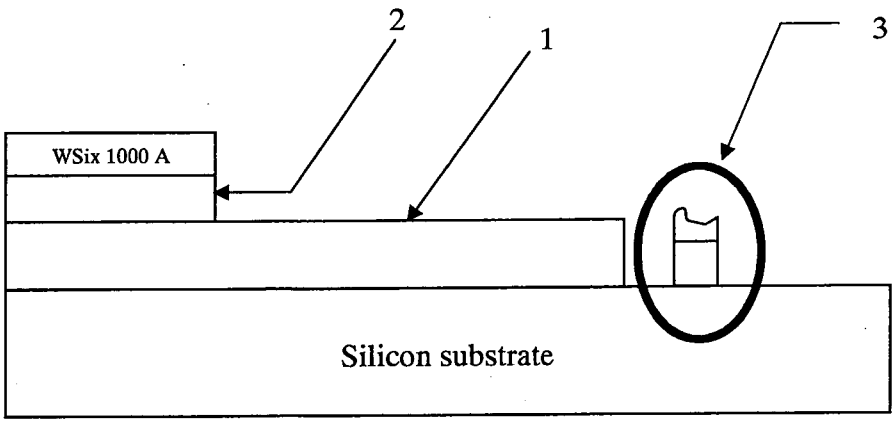

Figure 1b

Figure 1

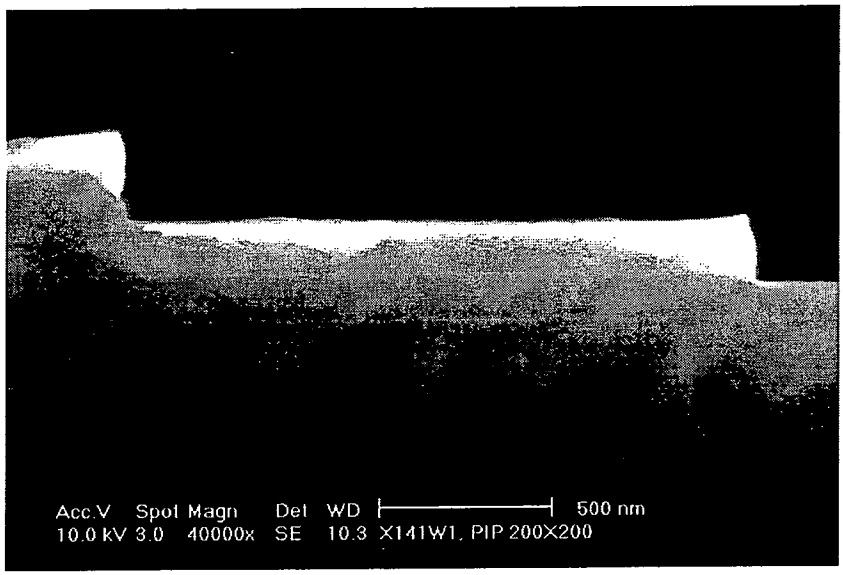

Figure 2a

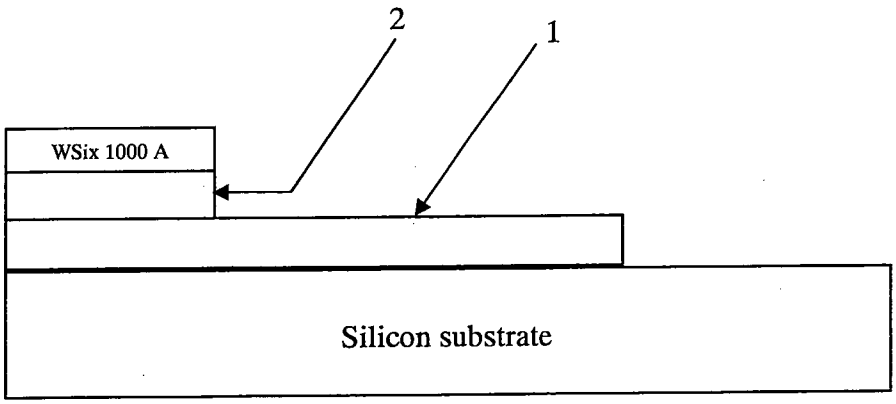

Figure 2b

Figure 2

Method	Height of Stringer (A)		
	1	2	3
Approach 1	3590	3410	3520
Approach 2	2880	2920	2850
Approach 3 (Poly1 2500A)	2483	2513	2456
Approach 3 (Poly1 2000A)	1882	1920	1915
Approach 3 (Poly1 1500A)	1170	1240	1150
Approach 3 (Poly1 1500A) + Poly2 etch optimization	0	0	0

Figure 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2008/000105

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/8247(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC : H01L 21/8247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utilitty Models and applications for Utility Models since 1975
Japanese Utilitty Models and applications for Utility Models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) & keywords : PIP, etch, WSix, ONO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6548406 B2 (Lai et al.) 15.April 2003 See the whole documents See Figure 2G See column 4, line 60 - column 5, line 44	1-3
A	KR 10-0650860 B1(DONGBU ELECTRONICS CO., LTD.) 27.November 2006. See the whole documents See Figure 2F See page 2, line 20 - page 2, line 55	1-3
A	KR 10-1999-026509 A(SAMSUNG ELECTRONICS CO., LTD.) 15. April 1999 See the whole documents See Figure 4 See page 2, line 47 - page 5, line 17	1-3
A	JP 10-209309 A(Hyundai Electronics Industries Co., Ltd.) 07 August 1998 See the whole documents See Figure 4 See paragraph [0011]-[0026]	1-3

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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