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(54) **PROCESS FOR PRODUCING A SEMICONDUCTOR WAFER WITH POLISHED EDGE**

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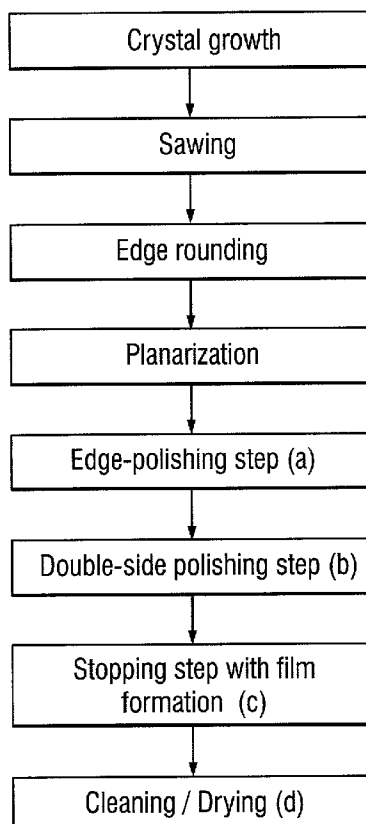
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(57) **ABSTRACT**

There is a process for producing a semiconductor wafer having a front surface and a back surface and a polished edge, in which the semiconductor wafer is subjected to polishing on both sides. The process includes the following temporal sequence of steps: (a) polishing of the edge of the semiconductor wafer using a polishing cloth, with an alkaline polishing abrasive being supplied continuously; (b) simultaneous polishing of the front surface and the back surface of the semiconductor wafer, with an alkaline polishing abrasive being supplied continuously, between two rotating, lower and upper polishing plates which are both covered with a polishing cloth, both polishing cloths substantially comprising a porous, homogeneous, fiber-free polymer foam, and the polishing cloth of the lower polishing plate having a smooth surface and the polishing cloth of the upper polishing plate having a surface which is interrupted by channels; immediately followed by: (c) complete wetting of the front surface and the back surface and the edge of the semiconductor wafer with a film of liquid; and (d) cleaning and drying of the semiconductor wafer. There is also a semiconductor wafer which has been polished on both sides, having a front surface and a back surface and a polished edge and a maximum local flatness value $SFQR_{max}$ of less than or equal to $0.13\text{ }\mu\text{m}$, based on partial regions of a surface grid on the front surface of the semiconductor wafer, which has been produced in accordance with this method.



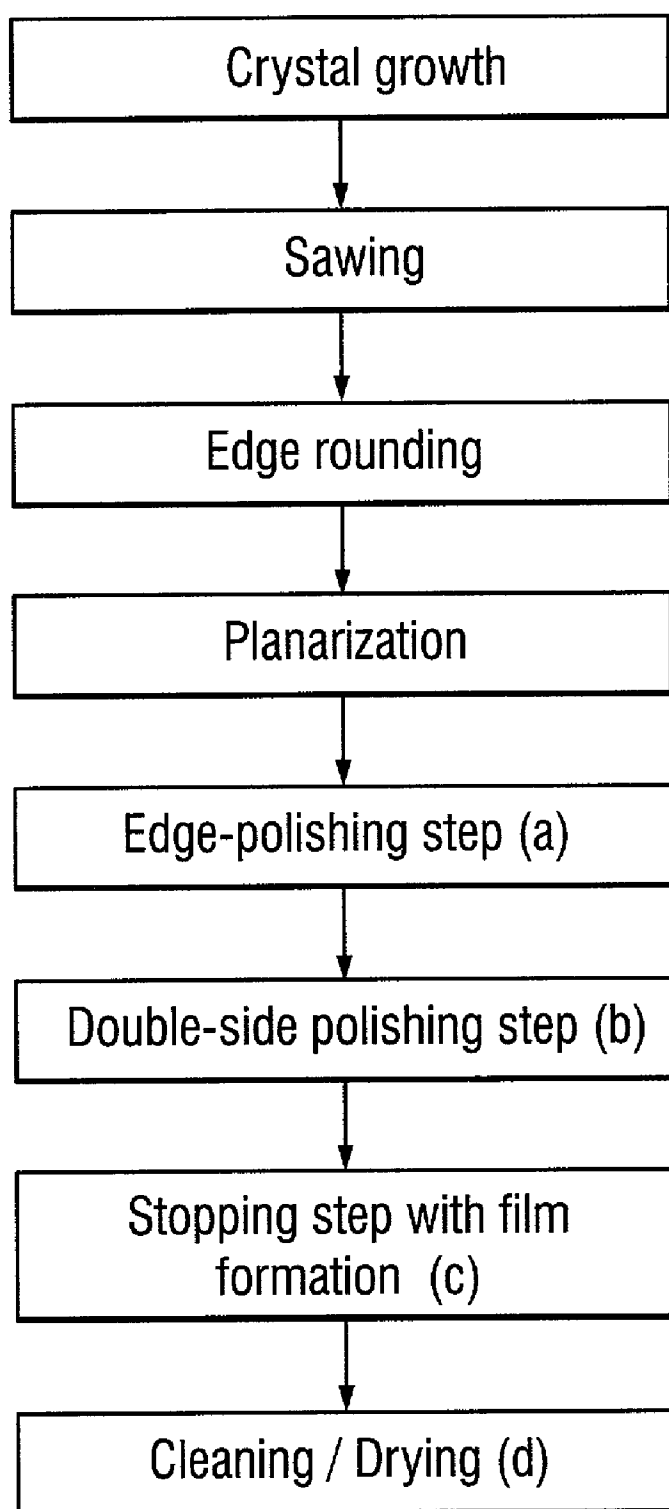


Fig. 1

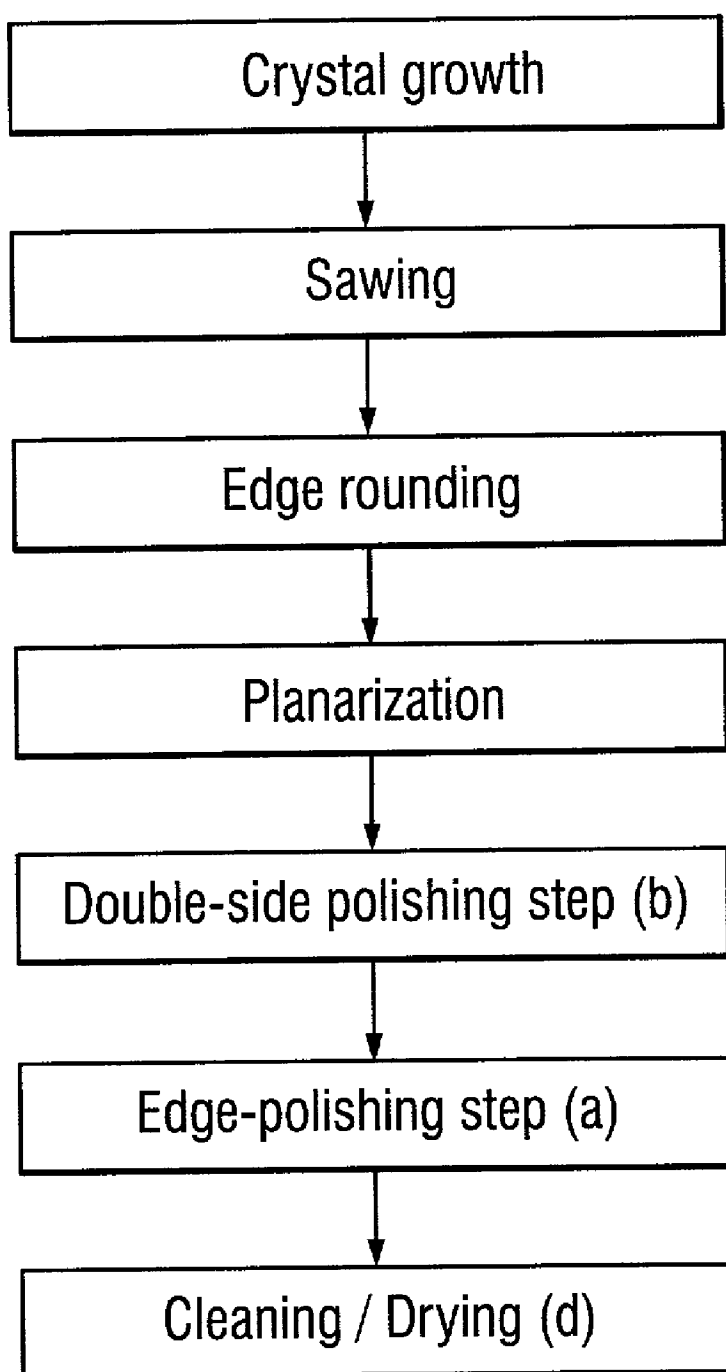


Fig. 2

(Prior art)

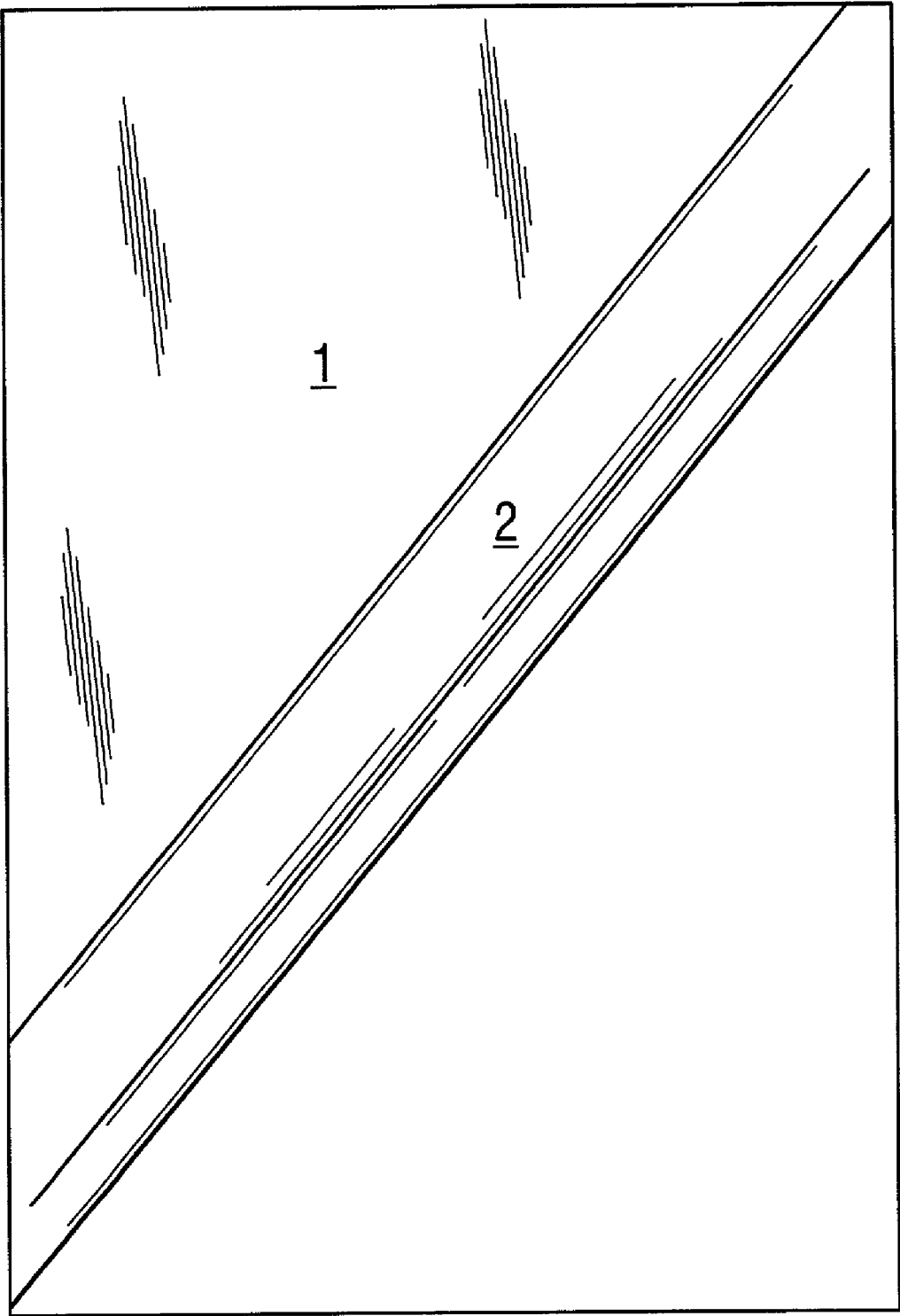
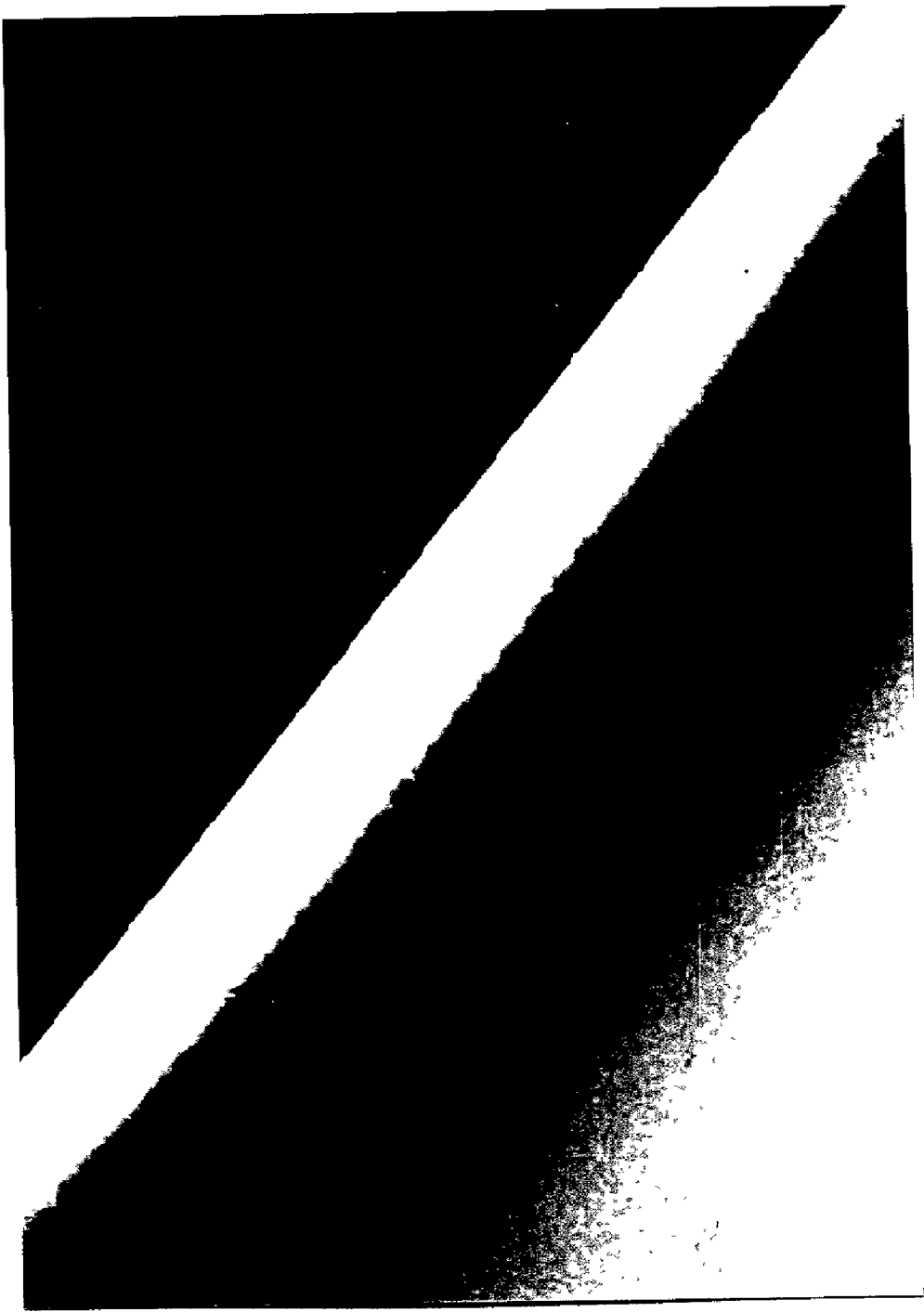
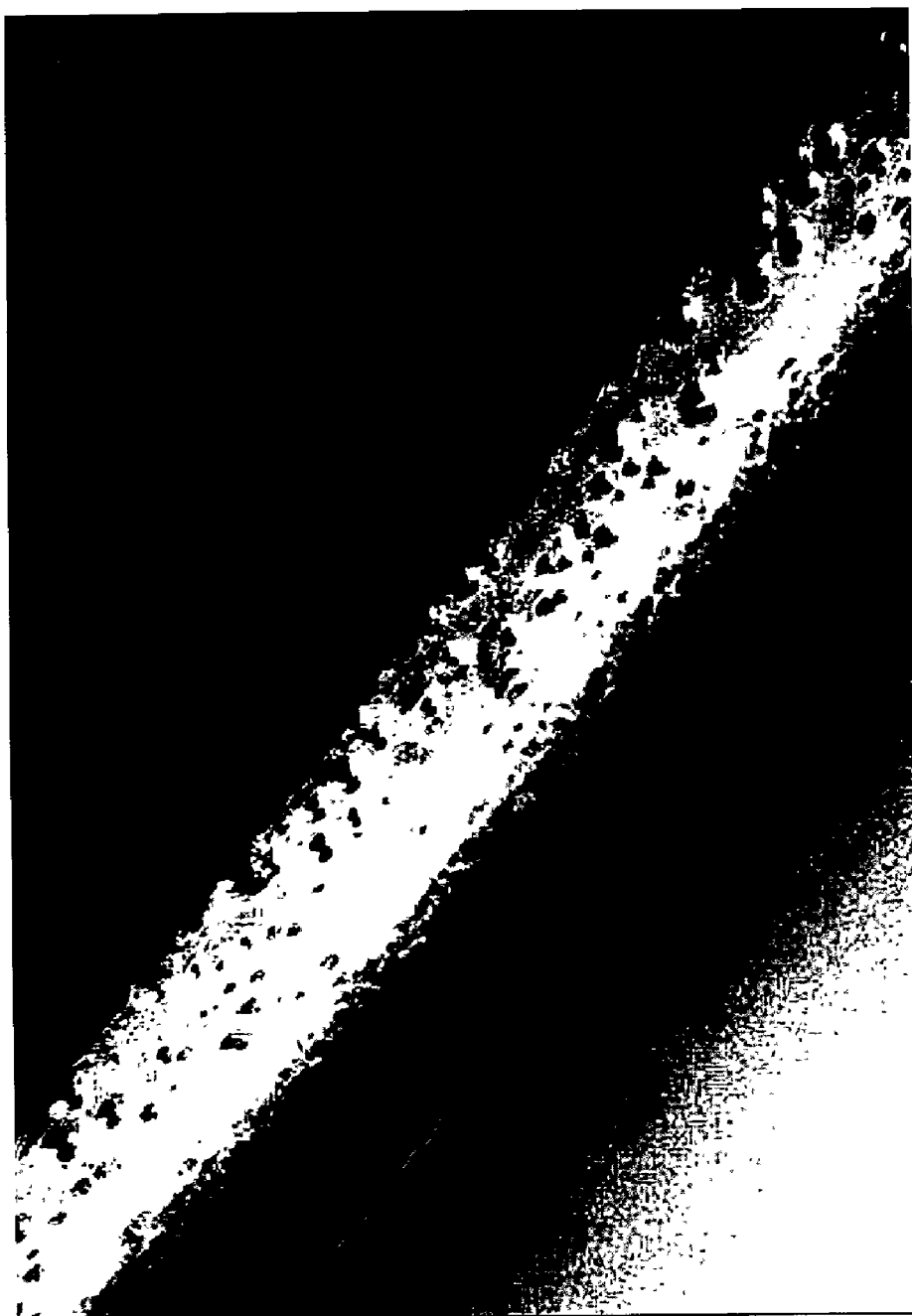


Fig. 3



0.1 mm

Fig. 4



┌ 0.1 mm

Fig. 5

(Prior art)

PROCESS FOR PRODUCING A SEMICONDUCTOR WAFER WITH POLISHED EDGE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a process for producing a double-side polished semiconductor wafer with polished edge in high yields, and to a semiconductor wafer of this type. Double-sided polished semiconductor wafers with a polished edge are suitable for use in the semiconductor industry, in particular for the fabrication of electronic components with line widths of less than or equal to $0.13\ \mu\text{m}$.

[0003] 2. The Prior Art

[0004] A semiconductor wafer which is to be suitable in particular for the fabrication of electronic components with line widths of less than or equal to $0.13\ \mu\text{m}$ has to have a high local flatness in all partial regions, expressed, for example, as SFQR_{max} less than or equal to $0.13\ \mu\text{m}$, which takes into account the way in which modern steppers operate. High flatness levels of this nature can be achieved by means of what is known as double-side polishing as the abrasive polishing step. An apparatus which is suitable for the double-side polishing of semiconductor wafers is described, for example, in DE 19 14 082 B2, U.S. Pat. No. 3,691,694 and EP 8 360 B1. According to one embodiment of double-side polishing, which is described in EP 208 315 B1, semiconductor wafers are moved along a path which is predetermined by the machine and process parameters in carriers. These carriers are made from metal and have suitably dimensioned, plastic-lined cutouts, between two rotating polishing plates, which are each covered with a polishing cloth, in the presence of a polishing abrasive, and are thus polished. The production of a semiconductor wafer with local flatness values which are suitable for $0.13\ \mu\text{m}$ component technology forms the subject-matter of DE 199 05 737 A7 and which discloses an improved double-side polishing process by maintaining tightly defined thickness relationships between carrier thickness and the thickness of the semiconductor wafer after the polishing process.

[0005] Numerous variations of polishing cloths for mechanically assisting the predominantly chemical polishing of semiconductor wafers ("chemo-mechanical polishing", CMP) are known and commercially available. In such cloths, a porous side which faces the semiconductor wafer to be polished is generally securely affixed to a supporting substructure. The layer which is active in the polishing process may comprise a homogeneous polymer foam, for example a polyurethane foam. A cloth of this type is described, for example, in U.S. Pat. No. 4,841,680 and is referred to in the field as being of the "foam type". A further variant is a polishing cloth which comprises polymer foam, for example polyurethane foam, reinforced with polymer fibers, for example with polyester fibers ("velour type"). Polishing cloths of this type, which are described, for example, in U.S. Pat. No. 4,728,552 and U.S. Pat. No. 4,927,432, are produced by impregnating a felt consisting of the fibers with a polymer solution and crosslinking. This leads to the felt being completely filled and covered by a porous, soft and elastic polymer layer. An example of a polishing cloth of this type is a polyester felt which is filled and covered with polyurethane.

[0006] EP 8 360 B1 states that both types of polishing cloths can be used for double-side polishing. The use of homogeneous polyurethane cloths for the double-side polishing of sawn but not edge-polished semiconductor wafers is known from EP 754 785 A1. The geometry values which are attained do not allow wafers of this type to be used for semiconductor components belonging to the technology generations of $0.13\ \mu\text{m}$ and smaller. The significantly more widespread use of polyester-fiber-reinforced polyurethane cloths in double-side polishing is described, for example, in the applications DE 39 26 673 A1, EP 208 315 B1, EP 711 854 B1, U.S. Pat. No. 5,821,167 U.S. Pat. No. 5,827,395, DE 199 057 737 A1, DE 199 38 340.5, DE 199 56 250.4 and DE 199 58 077.4. According to the prior art it is possible and described, for example, in EP 8 360 B1 and the German Patent Applications Ser. Nos. DE 199 58 077.4 and DE 199 62 564.6, for one or both polishing cloths to be textured by, for example, holes or channels being formed, in order to adjust the friction and/or adhesion forces during the double-side polishing. A significant shortcoming of the use of polyester-fiber-reinforced polyurethane cloths in double-side polishing is the rapid abrasion of the uppermost polyurethane layer on account of the mechanical attack from the carriers. This leads to the lower cloth layers being exposed and consequently to scratched wafer surfaces and edges, which in turn leads to a low cloth service life and therefore high process costs. Polishing cloths which have been improved, for example, by the incorporation of polymeric microelements, as described in U.S. Pat. No. 5,900,164, likewise only withstand the attack from the carriers to a limited extent. Also they can only be produced by complex, expensive production methods.

[0007] In particular in order to avoid the adhesion of particles which, during the fabrication of integrated circuits, may lead to the failure of entire components or component assemblies, semiconductor wafers which are to be used for components from the technology generation of $0.13\ \mu\text{m}$ and less must have polished edges. The production of double-side polished semiconductor wafers with polished edges is likewise known. A double-side polishing process with simultaneous polishing of the wafer edge is described in EP 776 030 A2 and EP 940 219 A2. However, it is known to the person skilled in the art that a procedure of this type involves making compromises in terms of throughput and yield. In U.S. Pat. No. 5,882,539 and U.S. Pat. No. 5,899,743 it is disclosed that the edge polishing be carried out after the double-side polishing. In this case too, mechanical and chemical deterioration to the double-side polished wafer surfaces leads to huge losses of yield during the edge polishing. This deterioration requires poor-quality wafers of this type to be discarded or expensively remachined, for example as described in the German Patent Application Ser. No. DE 199 56 250.4.

SUMMARY OF THE INVENTION

[0008] It is an object of the present invention to provide a process for producing double-side polished semiconductor wafers with polished edges in high yields.

[0009] The present invention provides a process for producing a semiconductor wafer having a front surface and a back surface and a polished edge, between said front and back surface, in which the semiconductor wafer is subjected to polishing on both sides, which comprises the following temporal sequence of steps:

[0010] (a) polishing of the edge of the semiconductor wafer using a polishing cloth, with an alkaline polishing abrasive being supplied continuously;

[0011] (b) simultaneous polishing of the front surface and the back surface of the semiconductor wafer, with an alkaline polishing abrasive being supplied continuously, between two rotating, upper and lower polishing plates which are both covered with a polishing cloth, both polishing cloths substantially comprising a porous, homogeneous, fiber-free polymer foam, and the polishing cloth of the lower polishing plate having a smooth surface and the polishing cloth of the upper polishing plate having a surface which is interrupted by channels; immediately followed by:

[0012] (c) complete wetting of the front surface and the back surface and the edge of the semiconductor wafer with a film of liquid; and

[0013] (d) cleaning and drying of the semiconductor wafer.

[0014] The present invention also relates to a semiconductor wafer which has been polished on both sides, having a front surface and a back surface and a polished edge and a maximum local flatness value $SFQR_{max}$ of less than or equal to $0.13 \mu m$, based on partial regions of a surface grid on the front surface of the semiconductor wafer, which has been produced as described in this process.

[0015] An essential feature of the invention is that to produce the semiconductor wafer according to the invention, the edge-polishing step (a) is carried out prior to the double-side polishing step (b). A further essential feature of the invention is that during the double-side polishing in accordance with step (b), polishing cloths made from a porous, homogeneous, fiber-free polymer foam are used. Also the polishing cloth which is stretched over a lower polishing plate has a smooth surface, and the polishing cloth which is stretched over an upper polishing plate has a surface which is interrupted by channels. A third essential feature of the invention is that the semiconductor wafer, in accordance with step (c), is completely wetted with a film of liquid. The fact that the provision of double-side polished semiconductor wafers with polished edges is possible with a considerably increased yield and therefore at reduced manufacturing costs only when all three features are complied with was surprising and not foreseeable.

[0016] The starting material for the process is a semiconductor wafer which has been separated from a crystal in a known way, for example from a silicon single crystal which has been cut to length and cylindrically ground. Also the edges of the wafer have been rounded and whose front and/or back surface has/have, if appropriate, been planarized by means of grinding, lapping and/or etching processes.

[0017] The end product of the process is a double-side polished semiconductor wafer with a polished edge which satisfies the requirements for use as a starting material for semiconductor component processes with line widths of less than or equal to $0.13 \mu m$. Because of the high yield, the wafer of the invention is an improvement on the double-side polished semiconductor wafers with polished edge produced according to the prior art in terms of its production costs.

[0018] In principle, the process according to the invention can be used to produce disk-like bodies which consist of a material which can be machined using the chemi-mechanical edge polishing and double-side polishing processes employed. Materials of this type include, for example, silicon, silicon/germanium and so-called III-V semiconductors, such as gallium arsenide. The process is particularly suitable for the production of monocrystalline silicon wafers with diameters of in particular 200 mm, 300 mm, 400 mm and 450 mm and thicknesses of a few hundred μm to a few cm, preferably of $400 \mu m$ to $1200 \mu m$. The semiconductor wafers may either be used directly, as starting material for the fabrication of semiconductor components. Or these wafer may be supplied for their intended purpose after a final polishing step according to the prior art has been carried out and/or after the application of layers, such as back surface seals. Or these wafers may be supplied after an epitaxial coating on the wafer front surface, for example with silicon, and/or after a heat treatment, for example under a hydrogen or argon atmosphere. In addition to the fabrication of wafers from a homogeneous material, the invention can also be used for the fabrication of semiconductor substrates of multilayer structure, such as SOI (silicon-on-insulator) wafers.

[0019] The method will be described further with reference to the example of the production of a silicon wafer.

[0020] A silicon wafer which has been sawn, for example, using an annular or wire sawing method, in order for the initially sharp and therefore mechanically highly sensitive wafer edges to be rounded, is machined with the aid of a suitably profiled grinding wheel made from metal- or resin-bonded diamonds. In this case, the edge can be rounded in one step. In the case of a two-step edge rounding being preferred for throughput reasons, a grinding wheel with diamond grains of 400 mesh (grain size range $30-50 \mu m$) to 600 mesh (grain size range $20-30 \mu m$) is used first. This is followed by a grinding wheel with diamond grains of 1000 mesh (grain size range $8-15 \mu m$) to 2000 mesh (grain size range $4-6 \mu m$).

[0021] In order to improve the geometry and partially abrade the destroyed crystal layers, a planarization step is preferred at this point. It is thus possible to subject the semiconductor wafer to a mechanical abrasion step, such as lapping or grinding, followed by a wet-chemical or plasma etching process, in order to reduce the material abrasion in the double-side polishing step (b). Sequential surface grinding of the wafer front surface and back surface using a grinding wheel comprising metal- or resin-bonded diamond grains of 400 mesh (grain size range $30-50 \mu m$) to 1000 mesh (grain size range $8-15 \mu m$) is used. This is carried out in combination with an acid etching step in a mixture of concentrated aqueous nitric acid and concentrated aqueous hydrofluoric acid, and is particularly preferred. A particularly preferred starting material is a semiconductor wafer made from silicon with a diameter of greater than or equal to 200 mm. This wafer is produced by wire-sawing of a silicon single crystal followed by edge-rounding, sequential surface grinding of both sides of the wafer, with from $10 \mu m$ to $100 \mu m$ of silicon being removed on each surface, and wet-chemical etching in an acid etching mixture with from 5 to $50 \mu m$ of silicon being removed from each surface.

[0022] In the text which follows, steps (a) to (d) of the process according to the invention for converting the starting

material into a double-side polished silicon wafer with a polished edge in high yields which satisfies the requirements imposed on semiconductor wafers as starting material for semiconductor component processes with line widths of less than or equal to $0.13\ \mu\text{m}$ are described in more detail.

[0023] Edge-polishing step (a)

[0024] Commercially available edge-polishing machines, the design of which depends on the diameter of the wafers to be polished, are available for carrying out the edge-polishing step (a). Polishing is preferably carried out using a commercially available polyurethane polishing cloth with a hardness of from 30 to 70 (Shore A), which may contain reinforcing polyester fibers; suitable polishing cloths are likewise marketed commercially. The procedure may be such that, by rotation of the silicon wafer using an obliquely positioned polishing plate covered with a polishing cloth, firstly one flank, for example the lower flank, of the wafer edge is polished, and then the other flank, for example the upper flank, of the wafer edge is polished. A process of this type is described, for example, in U.S. Pat. No. 5,866,477. However, it is also possible for the entire rounded edge to be polished in one step, as is described for example, in EP 687 524 B1.

[0025] The edge-polishing process takes place with a polishing abrasive with a pH of between 9 and 12 being supplied continuously. Suitable polishing abrasives include aqueous suspensions or colloids of a multiplicity of inorganic substances which have an abrasive action, for example silicon dioxide, in the presence of alkaline substances and, if appropriate, further additives. An alkaline polishing abrasive which is particularly preferred for step (a) of the invention has a pH of from 10 to 11.5 and consists of 1 to 5% by weight SiO_2 in water. The polishing time required to generate a polished edge which is free from defects all the way around depends on the wafer diameter and, for example for 300-mm silicon wafers, is between 0.5 and 5 min. In the process, preferably 0.5 to $15\ \mu\text{m}$ and particularly preferably 2 to $10\ \mu\text{m}$ of silicon, based on the surface of an edge, are abraded.

[0026] Double-side polishing step (b)

[0027] To carry out the double-side polishing step (b), it is possible to use a commercially available double-side polishing machine of suitable size. For cost reasons, it is sensible for a multiplicity of silicon wafers to be polished simultaneously. The polishing machine substantially comprises a lower polishing plate, which can rotate freely in a horizontal plane, and an upper polishing plate, which can rotate freely in a horizontal plane. Both plates are covered with a polishing cloth, and, with a polishing abrasive which preferably has a similar composition to the polishing abrasive used for step (a) being supplied continuously. The machine allows abrasive polishing of semiconductor wafers, in this case of silicon wafers, on both sides.

[0028] In this case, the silicon wafers, during the polishing, are held on a geometric path which is determined by machine and process parameters by driven carriers which have adequately dimensioned cutouts for holding the silicon wafers. Carriers made from steel or from fiber-reinforced plastics are preferred. Carriers made from stainless chromium steel are particularly preferred, on account of their high dimensional stability and chemical resistance. To pre-

vent damage to the polished wafer edge by the inner edge of the cutout in the carrier during polishing, it is therefore preferred for the inner side of the cutouts to be lined with a plastic coating of the same thickness as the carrier, for example by an extrusion process, as described in EP 208 315 B1. Examples of suitable plastics include polyamide, polyethylene, polypropylene, polyvinyl chloride, polytetrafluoroethylene or polyvinylidene difluoride, which are all equally preferred. With a view to maintaining the quality of the edge, it is also preferable for the plastic coating in all the cutouts to be checked for damage prior to each double-side polishing operation and for it to be replaced after a defined period of use, for example of between 100 and 200 polishing runs.

[0029] Within the context of the invention, the double-side polishing step (b) is carried out using a polishing cloth made from homogeneous, porous polymer foam with a hardness of from 60 to 90 (Shore A). This side facing toward the wafer which is to be polished is, if appropriate, joined to a mechanically more stable supporting layer, which is not active in the polishing process and does not form part of the invention. A polymer foam belonging to the elastomers group or a mixture of polymer foams of this type is preferable for the abrasion of silicon in step (b). Examples of such foams include polyurethane, polyamide, polyether, polyvinyl alcohol, polyvinyl chloride and polycarbonate in different chain lengths and degrees of crosslinking. A polymer foam substantially comprising polyurethane is particularly preferred. In the context of the work aimed at achieving the object of the invention, it was discovered that only homogeneous polymer foams of this type are suitable for providing defect-free wafer surfaces and edges. By contrast, if, for example, polyester-fiber-reinforced polishing cloths were used under the conditions prevailing during double-side polishing, the uppermost polymer foam layer was worn away even after only a few polishing runs. This leads to roughening of the wafer edges and to the wafers affected being lost, and to the need to exchange cloths of this type after only a few polishing runs, for example 10 to 20 polishing runs. By contrast, polishing cloths made from polymer foam achieve a service life of from 100 to 200 double-side polishing runs, and in exceptional cases even greater numbers of runs. Polishing cloths made from polymer foam within the preferred hardness range are now also commercially available. With modern double-side polishing machines with a large diameter, for example of 2 m, it may be necessary to compose the covering for the lower and upper polishing plates of a plurality of pieces, for example two or four pieces: This is described in the German Patent Application Ser. No. DE 199 62 564.6.

[0030] In accordance with the invention, it has proven necessary to add a network of channels to the polishing cloth which is stuck to the upper polishing plate and to leave the polishing cloth which sticks to the lower polishing plate with a smooth surface, without texturing of this nature. The upper polishing plate, once the double-side polishing is complete, is sometimes lifted off while rotating. This means that a step of this type, which was originally introduced in order to prevent silicon wafers from sticking to the upper polishing plate, can be dispensed with. The improved distribution of the polishing abrasive used as a result of this texturing is necessary in order to maintain the quality of the polished wafer edges. The channels can be made on the polishing cloth by, for example, a material-removing milling opera-

tion. The upper polishing cloth preferably has a regular arrangement of channels, which resembles a chess board, with a square size of from 5 mm×5 mm to 50 mm×50 mm and a channel width and depth of from 0.5 to 2 mm. With this arrangement, polishing is carried out under a polishing pressure of preferably from 0.1 to 0.3 bar. The silicon abrasion rate is preferably between 0.1 and 1.5 $\mu\text{m}/\text{min}$, and particularly preferably between 0.4 and 0.9 $\mu\text{m}/\text{min}$. The total amount of silicon abraded in step (b) is preferably between 2 and 100 μm , particularly preferably between 20 and 50 μm .

[0031] The thickness of the carriers for the double-side polishing step (b) is preferably from 400 to 1200 μm . In order to have silicon wafers with a high local flatness after step (b), in particular when using a polishing cloth made from homogeneous, porous polymer foam, in accordance with the invention, a double-side polishing process as described in DE 199 05 737 A7 is particularly preferable. In this process the thickness selected for the carriers depends on the desired final thickness of the silicon wafers after step (b) and is dimensioned to be from 2 to 20 μm less than the final thickness of the silicon wafers.

[0032] Stopping step with film formation (c)

[0033] After the double-side polishing step (b) has ended, the hydrophobic wafer surface, which is very chemically reactive, has to be passivated. In accordance with the invention, this is achieved by supplying one or more liquids, so that the polished front surface, the polished back surface and the polished edge of the silicon wafers are completely wetted with a film of liquid, so that the liquid acts as a stopping agent. If there is no film formation during the stopping step, the polished edges inevitably become much rougher, even if all the measures described above are carried out. Liquids in which ultrapure water is the principal constituent are preferable for the stopping step with film formation (c), for purely practical considerations. A film-forming agent is contained in the liquid supplied, or a plurality of film-forming agents are contained in one or more liquids of different composition. The concentration used is dependent on the nature of the film-forming agent and lying between 10^{-4} and 50% by volume. A concentration range of between 0.1 and 10% by volume is generally preferred. Essentially two demands are imposed on the film of liquid. (1) It must protect the surface and the edge of the silicon wafer after step (b) has ended from continued etching attack from the polishing abrasive. (2) It must be completely removable by cleaning in step (d).

[0034] The supply of the liquid or a plurality of liquids replaces the supply of the polishing abrasive described above. The polishing machine remains closed, so that the front surface, back surface and edge of the silicon wafer are simultaneously treated with the stopping agent between the rotating polishing plates. There is no interim exposure of the reactive wafer surfaces to atmospheric oxygen. To reduce frictional forces, it is preferable to reduce the polishing pressure to from 0.02 to 0.10 bar while the stopping agent is being supplied.

[0035] The chemical composition of the film-forming agent or agents may in principle be selected as desired, provided that the two criteria outlined are fulfilled and that the regulations and standards which apply to safety at work can be satisfied without particularly high outlay. It is pref-

erable to use compounds which are easy to mix with the liquid, preferably ultrapure water, if appropriate with the addition of a phase compatibilizer, without the viscosity of the liquid being seriously increased. The use of one or more substances selected from the group of compounds which are available for the production of semiconductor wafers of sufficient purity and consisting of polyhydric alcohols, polyalcohols and surfactants is particularly preferred within the context of the invention. In this context, the term surfactant is understood as meaning a surface-active inorganic or organic substance, which is also referred to in the specialist literature as a "wetting agent".

[0036] Examples of suitable polyhydric alcohols are ethylene glycol (1,2-ethanediol), propylene glycols (1,2- and 1,3-propanediol), butylene glycols (1,3- and 1,4-butanediol) and glycerol (1,2,3-propanetriol). The use of these substances as stopping agents for double-side polishing is described in the German Patent Application Ser. No. DE 199 38 340.5.

[0037] One example of a polyalcohol is polyvinyl alcohol, which is supplied, for example, by Wacker Chemie, under the trade name Vinnapas. A further example of a polyalcohol is a representative from the group consisting of the polyether polyols, which are supplied, for example, by Union Carbide, under the trade name Polyoxy. The use of polyether polyols as stopping agents for double-side polishing is described in EP 684 634 A2.

[0038] One example of a surfactant is a preparation based on alkylbenzenesulfonic acid and amine ethoxylate, which is supplied by ICB, under the trade name Silapur.

[0039] Moreover, the stopping agent may contain short-chain, monohydric alcohols, such as i-propanol and n-butanol, in concentrations of from 0.01 to 2% by volume. The addition of strongly acidic or strongly basic components is not desirable, since in the former case SiO_2 particles may form as a result of uncontrolled changes in pH, leading to scratched wafer surfaces and edges, while in the latter case etching spots on the wafer surface and edge may result.

[0040] An alternative embodiment of the stopping step with film formation (c) which is also particularly preferred is as follows.

[0041] Firstly, the supply of the polishing abrasive used in step (b) is replaced by the supply of a polishing abrasive which has a pH of between 9 and 11. It substantially comprises an aqueous mixture of from 0.5% to 4% by weight SiO_2 and 10^{-4} to 50% by volume, in particular 0.1 to 10% by volume, of one or more substances from the list of compound classes consisting of polyhydric alcohols, polyalcohols and surfactants, small proportions of further additives possibly also being present in the mixture. Mixtures of this type are known and are in general used as polishing abrasives for the surface polishing of silicon wafers and structured wafers during component fabrication in which very low abrasion rates are desired. The use of a polishing abrasive containing polyvinyl alcohol is described in DE 22 47 067 B2. A polishing abrasive which contains a polymeric additive and a surfactant as film former is known, for example, from U.S. Pat. No. 5,861,055. In the context of the invention, by way of example a commercially available polishing abrasive bears the trade name Glanzox 3900. It is marketed by Fujimi, which according to the manufacturer's

information contains colloidal SiO_2 , ammonia and a surfactant, which is not described in more detail, and is used, for example, in a preferred embodiment of EP 684 634 A2, is suitable. While this mixture is being supplied, the polishing pressure is reduced to 0.05 to 0.15 bar while rotation is maintained. This process state is maintained for a period of between 1 and 10 min, with the result that a film of liquid comprising polyvalent alcohol and/or polyalcohol and/or surfactant is formed on the surface and edge of the silicon wafers. Then, in order to wash polishing abrasive off the silicon wafers while at the same time maintaining the film on the surfaces and edges, ultrapure water is supplied, while rotation is continued and while the pressure is reduced further to from 0.02 to 0.10 bar, for a period of from 1 to 10 min.

[0042] After the stopping step with film formation (c) has ended, the upper polishing plate of the double-side polishing machine is lifted off while rotating and is pivoted away. The removal of the silicon wafers and transfer into a preferably aqueous bath can be carried out manually, using gloved fingers, or by means of a manually guided vacuum nozzle or an automatic unloading device. Gentle removal of the wafers by means of a vacuum nozzle holder as described in the German Patent Application Ser. No. DE 199 58 077.4 is preferred according to the invention. This is because this procedure allows a double-side polishing machine holding, for example, 30 200-mm wafers or 15 300-mm wafers to be unloaded within 2 minutes and at the same time involves acceptable production costs and wafer yields. The silicon wafers picked up by suction in this way are transferred into a receiving device which is situated in an aqueous bath or into a wet tray filler designed for the diameter of the wafers to be received. The aqueous bath used or the wet tray filler may be filled with ultrapure water or with ultrapure water which has been provided with small added quantities of acids and/or oxidizing substances and/or surfactants, in order to further optimize the preservation of the wafer surfaces.

[0043] Cleaning/driving step (d)

[0044] After step (c), the silicon wafers are subjected to cleaning and drying according to the prior art. The cleaning may be carried out either as a batch process, in which a multiplicity of wafers are cleaned simultaneously in baths or using spray methods, or as a single-wafer process. Bath cleaning with simultaneous cleaning of all the wafers from one polishing operation is preferred within the context of the invention. For example it is possible to use the sequence of aqueous hydrofluoric acid (HF)-ultrapure water-TMAH/ H_2O_2 ultrapure water, megasound assistance in the TMAH/ H_2O_2 bath being advantageous for the purpose of improving the removal of particles. Appliances which operate, for example, using the centrifugal drying, hot water, Marangoni or HF/ozone principle are commercially available and all equally preferred for drying without spots. The double-side polished and edge-polished wafers obtained in this way are dry and hydrophilic and no longer carry with them any residues of the film of liquid applied in step (c).

[0045] Desirably, after the process according to the invention, with the sequence of steps (a), (b), (c), (d), the silicon wafers are assessed according to predetermined quality criteria, as is sensible and necessary in operating practice, although this does not form part of the invention. For

example, it is possible to measure the geometry. Measurements carried out on a commercially available geometry-measuring unit, which operates, for example, on a capacitive or optical principle, for component surfaces of 25 mm×25 mm, indicate local geometry values SFQR_{max} of less than or equal to 0.13 μm . This is a precondition for these wafers to be used for the fabrication of semiconductor components with line widths of less than or equal to 0.13 μm .

[0046] At this point, a visual assessment of front surface, back surface and edge of all the silicon wafers which have been processed in accordance with the invention, is carried out. This occurs in a darkened assessment chamber under haze light, and is at this point customary and sensible with a view to removing faulty wafers. During this assessment, defects which would prevent further processing of the wafer in the component fabrication, for example scratches and spots, are discovered. Particularly for the fabrication of the edge-polished semiconductor wafer according to the invention, it is advisable to subject the edge to microscopic inspection. This is done in order to be able to identify and quantify any deviations which may be present in the polished wafer surface, for example as a result of roughening. A commercially available optic microscope with a resolution of between 10 times and 100 times, which can be used to vertically assess the wafers, which are generally arranged in a lying position, in the edge region is suitable for this purpose.

[0047] When the invention is used, the yield of double-side polished silicon wafers with a polished edge which are suitable for the 0.13 μm component generation is over 96%, while with a procedure according to the prior art it is below 85%.

[0048] Depending on its further use, it may be necessary for in each case the front surface of a silicon wafer produced using the process according to the invention to be subjected to a final polishing step in accordance with the prior art. For example it is possible to use a soft polishing cloth with the aid of an alkaline polishing abrasive based on SiO_2 . To maintain the very low local geometry values, the amount of silicon abraded from each wafer in this step should be relatively low, for example between 0.1 and 1 μm .

[0049] If necessary, further machining steps carried out on the silicon wafer may be added at suitable points through the process, taking into account a specific profile of demands for the component fabrication. For example there can be a heat treatment step in order to eliminate thermal donors; a laser marking step for wafer identification; the application of back-surface coatings or epitaxial layers; and cleaning and drying steps.

[0050] Semiconductor wafers produced according to the invention, in particular silicon wafers, satisfy the requirements for the production of semiconductor components with line widths of less than or equal to 0.13 μm . The process according to the invention has proven to be an optimum solution for reducing the production costs for double-side polished silicon wafers with polished edges by increasing the yield of wafers which comply with the specifications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0051] Other objects and features of the present invention will become apparent from the following detailed descrip-

tion considered in connection with the accompanying drawing which discloses several embodiments of the present invention. It should be understood, however, that the drawing is designed for the purpose of illustration only and not as a definition of the limits of the invention.

[0052] In the drawing, wherein similar reference characters denote similar elements throughout the several views:

[0053] FIG. 1 shows the process sequence for the fabrication according to the invention of a double-side polished semiconductor wafer of silicon with a polished edge in accordance with Examples 1 and 2.

[0054] FIG. 2 shows the process sequence for the production of a double-side polished semiconductor wafer of silicon with a polished edge according to the prior art in accordance with Comparative Example 1.

[0055] FIG. 3 diagrammatically depicts the arrangement of a double-side polished and edge-polished semiconductor wafer of silicon during the examination under an optical microscope (plan view), the results of which examination are illustrated in FIG. 4 and FIG. 5; 1 represents a section of the surface of the semiconductor wafer and 2 represents a section of the projection of the flank of the semiconductor wafer.

[0056] FIG. 4 shows a photograph under an optical microscope of a section of a double-side polished and edge-polished semiconductor wafer of silicon produced in accordance with Example 1, in the arrangement illustrated in FIG. 3.

[0057] FIG. 5 shows a photograph taken under an optical microscope of a section of a double-side polished and edge-polished semiconductor wafer of silicon produced in accordance with Comparative Example 2, in the arrangement illustrated in FIG. 3.

[0058] All the examples and comparative examples outlined below relate to the production of monocrystalline silicon wafers of orientation (100) with a diameter of 300 mm. Double-side polished and edge-polished wafers with flawless surfaces and edges were desired. The single crystals required for this purpose were pulled, cut to length, cylindrically ground and cut, on a commercially available wire saw, into wafers with a thickness which was tailored to the final product, in accordance with the prior art. After the edges had been rounded, a surface grinding step took place on a rotary grinding machine, using diamond grains of 600 mesh (grain size range 20-30 μm), with in each case 30 μm of silicon being removed in succession from the wafer front surface and wafer back surface. This was followed by an acid etching step using the flow etching process, with in each case 10 μm of silicon being abraded from each wafer surface simultaneously as a result of the rotating wafers being immersed in a mixture of 90% by weight concentrated nitric acid (70% by weight in aqueous solution), 10% by weight concentrated hydrofluoric acid (50% by weight in aqueous solution) and 0.1% by weight ammonium lauryl sulfate. The temperature of the etching mixture was controlled at 20° C., and gaseous nitrogen flowed through the mixture. At this point in the process sequence, the thickness of the wafers was 815 μm . The continuation of the process is described below, in which text, in all the examples and comparative examples, where specified, the edge-polishing step is denoted by (a), the double-side polishing step is denoted by

(b), the stopping step with film formation is denoted by (c) and the cleaning/drying step is denoted by (d). The material of the upper and lower polishing cloth in the double-side polishing step (b) was in each case identical for each specific example and comparative example, and in all cases it is specified whether or not the upper polishing cloth was textured by channels. All the silicon wafers produced in accordance with the examples and comparative examples had a local flatness SFQR_{max} of less than or equal to 0.13 μm for component surfaces of dimensions 25 mm×25 mm.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

EXAMPLE 1

[0059] Edge-polishing step (a)

[0060] The edges of the edge-rounded, ground and etched wafers were polished on a commercially available edge-polishing unit for 300-mm wafers, of type EP 300-IV from SpeedFam, using an aqueous polishing abrasive of type Levasil 200 from Bayer, with an SiO_2 solids content of 3% by weight and a pH which was set to 10.5 by the addition of potassium carbonate, a polyethylene-fiber-reinforced polyurethane polishing cloth of hardness 50 (Shore A) being used. Initially the lower flank and then the upper flank of the wafer edge were successively polished by rotation of the silicon wafer with an obliquely arranged polishing plate bearing a polishing cloth.

[0061] Double-side polishing step (b)

[0062] Five carriers made from stainless chromium steel with a lapped surface and a thickness of 770 μm were available, which each had three circular cutouts which were arranged at regular intervals on a circular path, were lined with polyamide and had an internal diameter of 301 mm, allowing the simultaneous polishing of 15 300 mm silicon wafers on a double-side polishing machine of type AC2000 produced by Peter Wolters.

[0063] The double-side polishing step was carried out using a commercially available polishing cloth which was not fiber-reinforced and was made from porous polyurethane foam of hardness 80 (Shore A), in each case attached to the upper and lower polishing plate by means of a pressure adhesive, using an aqueous polishing abrasive of type Levasil 200 from Bayer, with an SiO_2 solids content of 3% by weight and a pH which was set to 10.8 by the addition of potassium carbonate and potassium hydroxide, under a pressure of 0.15 bar. The polishing cloth stretched over the lower polishing plate had a smooth surface; the surface of the polishing cloth stretched over the upper polishing plate had a chessboard-like pattern of milled channels with a width of 1.5 mm and a depth of 0.5 mm, with the profile of a segment of a circle, which were arranged at an even spacing of 30 mm. The polishing took place with the upper and lower polishing plates at a temperature of in each case 40° C. and led to an abrasion rate of 0.68 $\mu\text{m}/\text{min}$. 20 μm of silicon was abraded from each wafer surface.

[0064] Stopping step with film formation (c)

[0065] The supply of the polishing abrasive was terminated after the thickness of the polished wafers reached 775 μm and was replaced, for a period of 3 min, by the supply of a stopping agent which comprised an aqueous solution of

1% by volume glycerol, 1% by volume n-butanol and 0.07% by volume of a commercially available surfactant sold under the trade name Silapur (preparation based on alkylbenzene-sulfonic acid and amine ethoxylate; produced by ICB). After the upper polishing plate had been raised and pivoted away, the front surfaces of the fully polished silicon wafers positioned in the carrier cutouts were completely wetted with stopping liquid.

[0066] A vacuum nozzle which was provided with a handle, consisted of polypropylene and had three suction cups made from soft PVC was available for removing the silicon wafers from the double-side polishing machine. Moreover, a commercially available 300-mm wet tray filler for receiving the polished silicon wafers was available and filled with ultrapure water. The procedure was that the carriers were left in position during the removal of the wafers, and the wafers were removed and transferred into the wet tray filler individually with the aid of the vacuum nozzle.

[0067] Cleaning/Driving step (d)

[0068] The silicon wafers which had been treated in this way were cleaned in a batch-cleaning unit using the following bath sequence: aqueous hydrofluoric acid-ultrapure water-TMAH/H₂O₂/megasound-ultrapure water and were dried in a commercially available dryer which operates using i-propanol according to the Marangoni principle. There followed a visual examination of the front surface, back surface and edge of all the wafers which had been processed in this way, in a darkened assessment chamber under haze light, and assessment of the wafer edge under an optical stereomicroscope with 20 times magnification and oblique illumination of the wafer edges. From a statistically relevant quantity of wafers processed in this way, 97% satisfied the quality criteria in terms of the absence of scratches, spots and light point defects required for further processing. The examination under an optical microscope did not reveal any impermissible defects on the wafer edges.

EXAMPLE 2

[0069] The procedure was as described in Example 1, except that the stopping step with film formation (c) was carried out as follows: the supply of the polishing abrasive supplied in step (b) was once again terminated after the polished wafers reached a thickness of 775 μm and was replaced, for a period of 3 min, with the supply of a stopping agent which consisted of a mixture of the polishing abrasive Glanzox 3900 from Fujimi with ultrapure water and, at an SiO₂ solids content of 2% by weight, had a pH of 10.0, with the lower polishing plate, upper polishing plate and carriers continuing to be moved and the pressure being reduced to 0.10 bar. This was followed by rinsing with ultrapure water for 2 minutes while maintaining rotation and with a further pressure reduction to 0.05 bar. After the upper polishing plate had been raised and pivoted away, in this case too complete wetting of the silicon wafers was observed. The yield of wafers which satisfied the specifications was 98%. The examination under an optical microscope once again did not reveal any impermissible defects on the wafer edges.

COMPARATIVE EXAMPLE 1

[0070] The experiment used as Comparative Example 1 corresponded to the experiment described in Example 7 of

the German Patent Application Ser. No. DE 199 56 250.4, which as its characteristic feature involves the edge-polishing step (a) being carried out only after the double-side polishing step (b).

[0071] The double-side polishing step (b) was carried out as described in Example 1, but with a commercially available, polyethylene-fiber-reinforced polyurethane polishing cloth of hardness 74 (Shore A) being used, which once again was attached to in each case the upper and lower polishing plates by means of a pressure adhesive. The upper polishing cloth was likewise provided with a chessboard-like pattern of channels in accordance with Example 1. At 0.64 $\mu\text{m}/\text{min}$, the abrasion rate did not differ significantly from the abrasion rate specified in Example 1. The supply of the polishing abrasive was terminated after the thickness of the polished wafers reached 775 μm and was replaced, for a period of 3 min, by the supply of a stopping agent which consisted of a mixture of 3% by weight Levasil 200 and 1% by volume n-butanol in water, with the lower polishing plate, the upper polishing plate and the carriers continuing to be moved and the pressure being reduced to 0.05 bar. After the upper polishing plate had been raised and pivoted away, the front surfaces of the fully polished silicon wafers positioned in the carrier cutouts had some regions which were wetted with the stopping mixture and some regions which were dry. This was a sign that the stopping agent used did not satisfy the requirements for complete wetting of the semiconductor wafer. After removal of the five carriers, the silicon wafers were removed from the polishing machine using fingers protected by latex gloves. Then, the edge-polishing step (a) was carried out as described in Example 1, followed by cleaning and drying in accordance with step (d) of Example 1. Of a statistically relevant amount of wafers processed in this way, 5% failed to satisfy the quality criteria in terms of the absence of scratches, spots and light point defects required for further processing; in addition, impermissible incipient local etching attributable to the edge-polishing process (a) was established on a further 11% of the wafers. The examination under an optical microscope did not reveal any impermissible roughening of the wafer edges.

COMPARATIVE EXAMPLE 2

[0072] The process steps (a) to (d) were carried out in the same order as that given in Example 1, but unlike in Example 1 the double-side polishing step (b), as described in Comparative Example 1, was carried out using a polyethylene-fiber-reinforced polyurethane polishing cloth of hardness 74 (Shore A) and the upper polishing cloth was also provided with a chessboard-like pattern of channels in accordance with Example 1. After the double-side polishing step (b) had ended, the mixture of Levasil 200 and n-butanol in water described was added, as described in Comparative Example 1, and the silicon wafers, after removal of the carriers, were manually removed from the polishing machine, followed by cleaning and drying of the silicon wafers in accordance with Example 1. All the wafers examined under an optical microscope presented considerable roughening of the wafer edges which was not acceptable for further processing.

COMPARATIVE EXAMPLE 3

[0073] The procedure was as described in Example 1, except that instead of the polyurethane cloth, the polyeth-

ylene-fiber-reinforced polyurethane polishing cloth described in Comparative Example 1, with the texturing of the upper cloth outlined, was used. 5% of the wafers presented scratches, spots and/or light point defects; a further 47% of the wafers failed to comply with specifications on account of roughened edges which were detectable under an optical microscope.

COMPARATIVE EXAMPLE 4

[0074] The procedure was as described in Example 2, except that the polyethylene-fiber-reinforced polyurethane polishing cloth described in Comparative Example 1 with the texturing of the upper cloth outlined was used instead of the polyurethane cloth. 3% of the wafers presented scratches, spots and/or light point defects; a further 36% of the wafers failed to satisfy the specifications on account of roughened edges which were detectable under an optical microscope.

COMPARATIVE EXAMPLE 5

[0075] The procedure was as described in Comparative Example 2, except that the polyurethane polishing cloth described in Example 1, with the texturing of the upper cloth outlined, was used instead of the polyethylene-fiber-reinforced polyurethane cloth. All the wafers examined under an optical microscope once again presented considerable roughening of the wafer edges, which was not acceptable for further processing.

COMPARATIVE EXAMPLE 6

[0076] The procedure was as described in Example 1, the only difference being that the upper polyurethane cloth was not textured at all. 4% of the wafers were unacceptable on account of scratches, spots and/or light point defects, and a further 17% of the wafers were unacceptable on account of roughened edges which were detectable under an optical microscope.

[0077] Consequently, the examples of the invention (E1 and E2) and comparative examples (C1 to C6) carried out can be distinguished according to the features listed in the Table below. In this Table, PU means porous polyurethane foam, and PE/PU means polyester-fiber-reinforced polyurethane foam; (a) corresponds to the edge-polishing step, (b) corresponds to the double-side polishing step, (c) corresponds to the stopping step with film formation, and (d) corresponds to the cleaning/drying step.

TABLE

	Re (a): Edge polishing	Re (b): Type of polishing cloth	Re (b): Channels in upper cloth	Re (c): Film formation	Re (c): Vacuum removal	Re (d): Yield in spec.
E1	yes	PU	yes	yes	yes	97%
E2	yes	PU	yes	yes	yes	98%
C1	After (b)	PE/PU	yes	no	no	84%
C2	yes	PE/PU	yes	no	no	0%
C3	yes	PE/PU	yes	yes	yes	48%
C4	yes	PE/PU	yes	yes	yes	61%
C5	yes	PU	yes	no	no	0%
C6	yes	PU	no	yes	yes	79%

[0078] The high performance of the process according to the invention in terms of the yield of double-side polished

semiconductor wafers of silicon with a polished edge which were able to satisfy the specification “flawless surface and edge” is clear from the table.

[0079] Accordingly, while a few embodiments of the present invention have been shown and described, it is to be understood that many changes and modifications may be made thereunto without departing from the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. A process for producing a semiconductor wafer having a front surface and a back surface and a polished edge, between said front and back surface, in which the semiconductor wafer is subjected to polishing on both sides, which comprises the following temporal sequence of steps:

- (a) polishing of the edge of the semiconductor wafer using a polishing cloth, with an alkaline polishing abrasive being supplied continuously;
- (b) simultaneous polishing of the front surface and the back surface of the semiconductor wafer, with an alkaline polishing abrasive being supplied continuously, between two rotating, lower and upper polishing plates which are both covered with a polishing cloth, both polishing cloths substantially comprising a porous, homogeneous, fiber-free polymer foam, and the polishing cloth of the lower polishing plate having a smooth surface and the polishing cloth of the upper polishing plate having a surface which is interrupted by channels; immediately followed by:
- (c) complete wetting of the front surface and the back surface and the edge of the semiconductor wafer with a film of liquid; and
- (d) cleaning and drying of the semiconductor wafer.

2. The process as claimed in claim 1, comprising

resting semiconductor wafer in a cutout in a carrier during steps (b) and (c).

3. The process as claimed in claim 2,

wherein the carrier has a thickness which is 2 to 20 μm less than a thickness of a fully polished semiconductor wafer.

4. The process as claimed in claim 1,

wherein step (b) reduces thickness of the semiconductor wafer by 2 to 100 μm .

5. The process as claimed in claim 1,

wherein the alkaline polishing abrasive used in step (a) and step (b) substantially comprises a suspension of silicon dioxide particles and a base selected from the group consisting of an inorganic base and an organic base and a mixture thereof in ultrapure water, which is at a pH of from 9 to 12.

6. The process as claimed in claim 1,

wherein the polishing cloths of the lower and upper polishing plate substantially comprise polyurethane and have a Shore A hardness of from 60 to 90.

7. The process as claimed in claim 1,

wherein the polishing cloth of the upper polishing plate has a regular arrangement of channels, resembling a

chessboard, with a square size of from 5 mm=5 mm to 50 mm=50 mm and a channel width and depth of from 0.5 mm to 2 mm.

8. The process as claimed in claim 1,

wherein the film of liquid generated in step (c) is completely removed in the subsequent cleaning step (d).

9. The process as claimed in claim 1,

wherein the film of liquid generated in step (c) contains a compound selected from the group consisting of polyhydric alcohols, polyalcohols, surfactants, and a mixture thereof.

10. The process as claimed in claim 9,

wherein the film of liquid contains glycerol.

11. The process as claimed in claim 9,

wherein the film of liquid comprises a compound selected from the group consisting of polyether polyol, polyvinyl alcohol and a mixture thereof.

12. The process as claimed in claim 9,

wherein the film of liquid contains a surfactant, and said film of liquid is generated by feeding the semiconductor wafer initially with a mixture of aqueous polishing abrasive and the surfactant and then, for a brief period, feeding with ultrapure water.

13. The process as claimed in claim 1, comprising

removing the semiconductor wafer, after step (c), from a polishing machine with a vacuum nozzle holder.

14. The process as claimed in claim 1,

wherein, after steps (a) to (d) have been carried out, applying a semiconductive, epitaxial coating to the front surface of the semiconductor wafer.

15. The process as claimed in claim 1,

wherein, after steps (a) to (d) have been carried out, final polishing is carried out on the front surface of the semiconductor wafer; and the semiconductor wafer is cleaned and dried; and a semiconductive, epitaxial coating is applied to the front surface of the semiconductor wafer.

16. A semiconductor wafer which has been polished on both sides, having a front surface and a back surface and a polished edge between said front and back surface and a maximum local flatness value $SFQR_{max}$ of less than or equal to $0.13 \mu m$, based on partial regions of a surface grid on the front surface of the semiconductor wafer, which has been produced according to the process of claim 1.

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