

[54] SYSTEMS INVOLVING DIVISION

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[52] U.S. Cl.....235/196, 307/251, 328/161,
235/151.3

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73/336.5

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[57] ABSTRACT

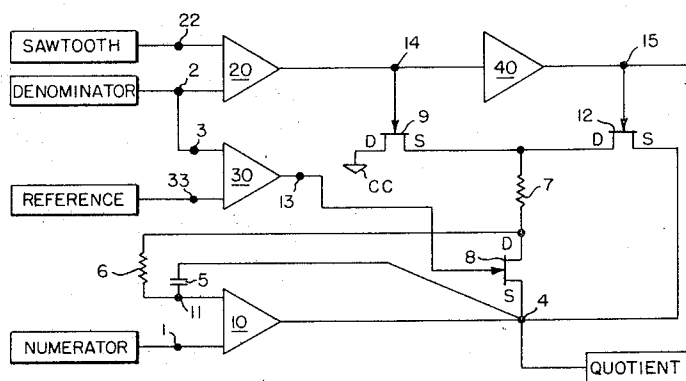
A system wherein division by zero is avoided. A numerator voltage is applied to a high gain amplifier having a negative feedback loop controlled by a denominator voltage which if zero disables part of the feedback loop. The effect of this is avoided by, in effect, replacing this part of the loop in response to the denominator becoming zero.

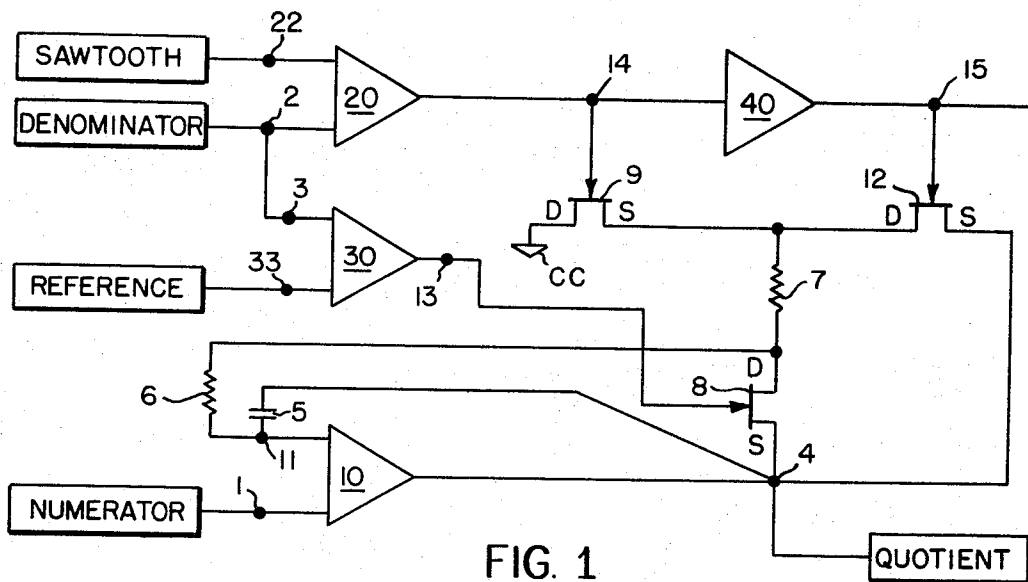
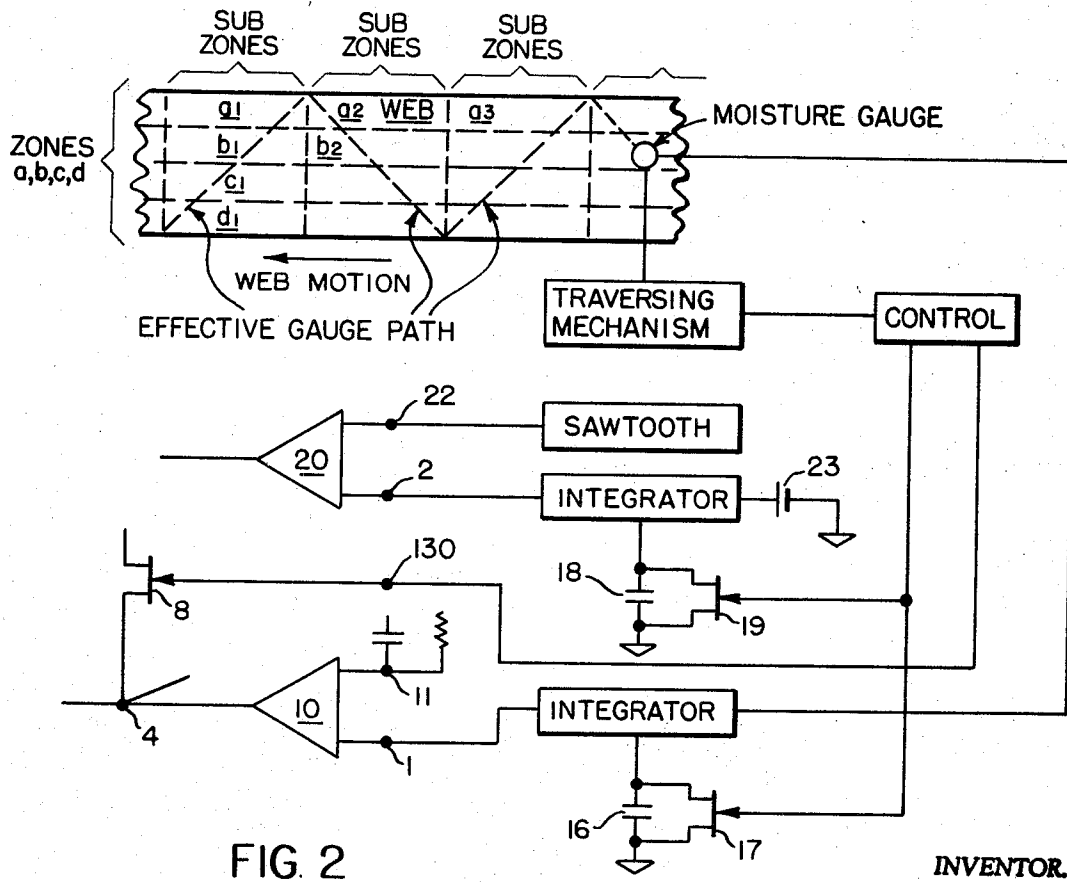
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7 Claims, 2 Drawing Figures





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SYSTEMS INVOLVING DIVISION

BACKGROUND OF THE INVENTION

1. The field of the invention is in the art of computing instruments the functioning of which involves performing the operation of division, i.e., dividing a denominator into a numerator to obtain a quotient. Frequently, the numerator and denominator represent physical variables such as pressure, temperature, characteristics of materials, time, or the like, which may for one reason or another become zero. In particular, averaging a variable over time may involve division, and, where the averaging is performed piece-wise for a series of intervals, dividing by zero may be involved at the beginning of each interval.

2. Description of the Prior Art: In some forms of prior art computing instruments, the means providing the dividing operation includes a high-gain amplifier for amplifying a numerator voltage, and there is a negative feedback loop around the amplifier which makes the amplifier output reflect the numerator voltage. The loop is controlled ultimately by a denominator voltage to make the feedback proportional to denominator voltage. As a result the amplifier's output voltage represents the numerator voltage divided by the denominator. When the denominator voltage is sufficiently small, it in effect makes the feedback zero, and as a result, the amplifier output can no longer correspond to its input.

Summary: A computing instrument according to the present invention, is generally of the above-described type but, unlike the prior art, that part of the feedback loop controlled by the denominator voltage is in effect replaced by an element that maintains feedback in response to the denominator becoming zero or sufficiently small. The invention finds particular use in systems for averaging the moisture content over the width of a moving web of paper. In brief, a suitable moisture content measuring instrument scans across the paper, transversely of the direction of its motion. The average moisture content of a fraction of the width is obtained by integrating moisture content across the width of the fraction. This average is divided by the time which elapsed while moisture content was being measured in this fraction, and the resulting quotient here is the average moisture content of a strip of web, the width of which is proportional to the time of measurement. This process is repeated for the next fraction of web width, and then for the next and the next, and so on. Consequently, there results a set of moisture content averages for a series of strips of web. However, each time averaging is begun in a strip, elapsed time is zero, so the division of the moisture content integrals by time is provided for in accordance with the present invention.

In particular, the elapsed time is determined by means of a capacity-type integrator, the capacity of which is discharged at the beginning of each strip, so for a brief interval corresponding to the beginning of a strip, feedback is maintained by the aforesaid element.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 represents a dividing system according to the invention;

FIG. 2 represents an averaging system according to the invention.

In FIG. 1, numerator voltage e_1 and denominator voltage e_2 are connected to non-inverting input terminals 1 and 2, respectively, of high gain differential amplifiers 10 and 20 respectively. A feedback voltage e_{11} , and a sawtooth voltage e_{22} are connected to the inverting terminals 11 and 22, respectively, of amplifiers 10 and 20. It will be observed that the connections specified here contemplate that all four voltages are negative in polarity.

Feedback voltage e_{11} is derived from the output voltage e_0 at output terminal 4 of amplifier 10, via a negative feedback loop consisting essentially of capacitor 5 in parallel with the resistance between terminals 4 and 11, made up of resistors 6 and 7, and FET's 8, 9 and 12.

The gate electrodes of FET's (field effect transistors) 8, 9 and 12 are connected to output terminals 13, 14 and 15, respectively, of amplifiers 30, 20 and 40. FET's 9 and 12 are connected together, source to drain, with the drain of FET 9 being connected to circuit common CC, and the source of FET 12 being connected to output terminal 4. One end of each of resistors 6 and 7 is connected to the drain electrode of FET 8, the other end of resistor 6 is connected to output terminal 11, the other end of resistor 7 is connected to the source-drain connection of FET's 9 and 12, and the source electrode of FET 8 is connected to output terminal 4.

Amplifier 30 is a high gain differential amplifier having non-inverting input terminal 3 and inverting input terminal 33, the former being connected to input terminal 2, and the latter being connected to a source of reference voltage.

Amplifier 40 is a unitary gain, inverting amplifier, the input terminal of which is the same as the output terminal 14 of amplifier 20.

The sources of the several input voltages are shown as boxes labeled SAWTOOTH, DENOMINATOR, REFERENCE and NUMERATOR. The output voltage e_0 at terminal 4 is applied to some utilization apparatus (shown as a box labeled QUOTIENT and connected to terminal 4) which may be suitable control, indicating, or like apparatus, the exact nature of which is not relevant here.

The purpose of SAWTOOTH, amplifiers 20 and 40, and FET's 9 and 12 is to make feedback voltage e_{11} correspond to the denominator voltage e_2 . For this purpose e_{22} is to be supposed to be a "ramp" beginning at zero, its magnitude increasing linearly to a given magnitude equal to or greater than the highest magnitude that e_2 can be expected to take on, and repeating at a given rate that is much greater than any rate at which e_2 can be expected to vary its magnitude. Voltage e_{22} may on the other hand, be the output of some measuring device which senses a condition such as temperature, characteristics of materials, or the like, and causes the voltage e_2 to have some predetermined quantitative relationship to said condition. The voltage e_1 may be of substantially the same character as voltage e_2 .

Since amplifier 20 is a high gain differential amplifier, its response to e_2 and e_{22} is to produce an output voltage e_{14} terminal 14, the sign of which depends on which of voltages e_2 and e_{22} is larger. If at a given instant e_2 is larger than e_{22} then e_{14} will be positive, whereas if e_{22} is the larger voltage, then e_{14} will be negative. Further, the output voltage e_{15} of amplifier 40 will always be opposite in sign too, but of the same order of magnitude as voltage e_{14} .

The amplifier 20 is designed so that the voltages e_{14} and e_{15} always have magnitudes greater than the cutoff voltages of FET's 9 and 12. Because of this, and since e_{14} and e_{15} are always opposite in sign, one of the FET's will be on and the other off, at all times, though which is on and which is off will depend on which of e_2 and e_{22} is the larger in magnitude.

When FET 12 is on, there will be a feedback loop consisting of capacitor 5 in parallel with the series resistances of resistor 6, resistor 7 and the drain/source resistance of FET 12. When FET 12 is off, then input terminal 11 is grounded to circuit common via the series resistance of resistor 6, resistor 7, and the drain/source resistance of FET 9.

Supposing e_2 to have a value greater than zero but less than the maximum value attained by the ramp, then the instant at which ramp voltage becomes just slightly greater than e_2 corresponds to the magnitude of e_2 . Therefore, during any given ramp, the amount of time FET 12 is on is proportional to the magnitude of e_2 . Further, the overall gain of amplifier 10 is proportional to the reciprocal of that amount of time. Accordingly, e_0 at terminal 4 is proportional to e_1/e_2 .

The foregoing operation is known in the prior art, but it is also known in the prior art that such operation will not admit of e_2 becoming zero, or indeed of decreasing to some minimum value not zero. The reason for this is that when e_2 is less than e_{22} , the charge of capacitor 5 is no longer under control of e_2 . At this point, since FET 9 is on, amplifier 10 and

capacitor 5 act as an integrator, and cause voltage e_0 to reflect only the peculiarities of amplifier 10, such as its off set voltage, bias current, and so on, as will be recognized by those skilled in the art. While the time constant of discharge of capacitor C_5 is fixed by choosing value of capacitor 5, and resistors 6 and 7 such that capacitor 5 cannot discharge enough during any given ramp to matter, e_2 varies slowly enough in comparison to the sawtooth voltage at e_{22} that if e_2 becomes zero or nearly zero, it will likely remain so long enough to discharge capacitor 5 to the point where there is, in effect, no feedback at terminal 11, at which point amplifier 10 will saturate.

The above-described effect of e_2 becoming zero or too nearly zero is prevented by amplifier 30 and FET 8. During normal operation, i.e., e_2 not equal to zero, or different therefrom by at least a predetermined amount, amplifier 30 is producing e_{13} with such magnitude and sign that FET 8 is cut-off, in which condition its drain/source resistance is for practical purposes infinite, and therefore does not affect the operation of amplifier 10. As shown, a reference voltage source (shown as a box labeled REFERENCE and connected to input terminal 33) provides a fixed reference voltage e_{33} , which is set to just such value that when e_2 is zero, or such non-zero minimum value such as will have the effect of zero, e_{13} will switch FET 8 on. Accordingly, when e_2 becomes just slightly larger than e_{33} , then e_{13} will change sign and switch FET 8 off. When FET 8 is on, there is feedback to terminal 11 via capacitor 5 in parallel with the series resistance of resistor 6 and the drain/source resistance of FET 8. While terminal 11 can still connect to circuit common via FET 9, resistor 7 is chosen to have such value in relation to the drain/source resistance of FET 8 that there is sufficient feedback voltage, at such times as FET 9 is on, at the connection between resistor 7 and the drain electrode of FET 8 to control the output of amplifier 10, making e_0 some convenient, predetermined fixed multiple e_1 . In particular, it is convenient to choose R_7 to be sufficiently large that e_0 is substantially equal to e_1 at this time. Additionally, resistor 7 limits current drain to acceptable levels whenever FET's 8 and 9 are both on.

Various modifications in the system of FIG. 1 will be evident to those skilled in the art. For example, various reversals in the polarities indicated previously, or implied by the illustrated nature of the components, could be adopted. Thus, e_2 and e_{22} could be positive voltages. In this case, terminals 2 and 22 would have to be the amplifier's inverting and non-inverting input terminals, or FET's 9 and 12 would have to be P-type, instead of N-type as shown.

Again, FET 12 could be replaced by a P-type FET in which case the amplifier 40 could be eliminated since the gate of the replacement could be connected directly to terminal 14.

The role of FET's is to be essentially on-off switches having on-resistance negligibly small in comparison to the resistors 6 and 7, but having off-resistances large enough to be effectively open-circuits when gated off. In FIG. 1, drain and source electrodes are distinguishable, but this is not essential, especially since FET's are available in which drain and source are interchangeable.

In FIG. 2, MOISTURE GAUGE is moved by TRAVERSING MECHANISM moving at right angles to the web and the direction of WEB MOTION. The gauge is therefore moving in a zigzag effective path along which the moisture content is measured. Supposing web and gauge to move at constant rates, then it will be evident that the web may be viewed as being divided up into longitudinal ZONES a, b, c and d, each of which is divided up into SUBZONES, e.g., subzones a_1, a_2, a_3, a_4 , and so on, of zone a, each of which subzone corresponds to a single determination of average moisture content. While zoning and subzoning depend in part on considerations such as intended use, interpretation, etc., of the averages, they also may depend on the nature of the averaging process, as will be explained later on below.

Supposing the web to be moving and the moisture gauge to be traversing and measuring the web moisture, averages are

determined, and zones and subzones are defined by means of what is essentially the divider system of FIG. 1, plus certain modifications. In order to avoid repetition, only so much of the FIG. 1 system is shown in FIG. 2, as is necessary to show the aforesaid modifications and the use of the FIG. 1 system in web moisture measurement. Insofar as FIG. 2 reproduces parts of FIG. 1, these parts are identified by the same reference numerals as in FIG. 1.

The moisture gauge is shown as connected to a box labeled INTEGRATOR replacing the box NUMERATOR of FIG. 1, and the DENOMINATOR box of FIG. 1 has been similarly replaced. The integrating function of the integrators is represented by capacitors 16 and 18, having FET's 17 and 19 connected across them. The voltages at terminals 1 and 2 in this arrangement, represent the voltages, with respect to circuit common, to which the capacitors 16 and 18 charge.

The integrator having capacitor 16 is connected to the moisture gauge to integrate a voltage from the gauge, which voltage represents the moisture content of the web as seen by the gauge. Accordingly, the voltage at terminal 1 represents the time integral of the moisture gauge output voltage.

The integrator having capacitor 18 is connected to a fixed DC voltage source, shown as cell 23, to integrate the voltage of cell 23. Accordingly, the voltage at terminal 2 is the time integral of the voltage of cell 23. As the voltage of the cell is fixed, its time integral simply represents elapsed time, or, ultimately, length of path of the moisture gauge with respect to the web.

It is evident that the quotient at terminal 4 represents an average value of moisture content in the paper web. However, the integrators cannot integrate indefinitely, due to the properties and practical parameters of real integrators. Therefore, periodically the capacitors must be discharged. This is provided for by CONTROL which, for example, is connected to the traversing mechanism to determine suitable instants during the travel of the moisture gauge, at which to discharge the capacitors. In this case, CONTROL emits a turn-on voltage pulse to FET's 17 and 19 at substantially the instant one subzone has been traversed by the gauge. This pulse lasts just long enough to discharge the capacitors 16 and 18 to the potential of circuit common. After this pulse disappears, the FET's 17 and 19 revert to their off-resistances, and the integrators begin to integrate again.

When the capacitors discharge, the voltages at terminals 1 and 2 become zero or very small, so simultaneously with the capacitor discharging pulse, CONTROL emits a pulse which is applied to the gate of FET 8 via a terminal 130, for turning on FET 8. In FIG. 2, therefore, CONTROL and terminal 130 correspond to amplifier 30 and terminal 13 of FIG. 1, and perform the same function with respect to FET 8.

The difference between the two Figures is ultimately how denominator voltage gets to be zero or sufficiently nearly so. Thus, in FIG. 1, the occurrence of zero denominator voltage, however caused, is detected. In FIG. 2, zero denominator voltage is an incident of the averaging operation. As in practice, in FIG. 2, zero denominator voltage is not expected to occur except by reason of discharging capacitor 18, it is more convenient to have CONTROL provide for turning FET 8 on, than to provide distinct zero detecting means such as amplifier 30.

Preferably, the firing pulse on terminal 130 occurs slightly before the firing pulse for FET's 17 and 19, and expires a little while after them. The reason for this is that the time integrator is essentially a ramp generator which is supposed to produce a voltage beginning at zero, increasing from there at a constant rate to a given value, and becoming instantaneously zero again upon achieving that given value. Actually, capacitor 18 does not discharge instantaneously to zero, and there is some uncertainty about the point at which the voltage on capacitor 18 thereafter begins to follow the desired ramp configuration. In effect, therefore, there is an interval overlapping the end of one ramp and the beginning of the next ramp, in which the voltage at terminal 2 may get to zero, but otherwise deviates

from the ideal. In the present invention, FET 8 is on during this interval (which is marked at terminal 4, so to speak, by e_0 having the predetermined value determined by resistor 7, namely, substantially the value of e_1 , which will be zero at some point in said interval) so no division occurs except when the voltage e_2 has the desired ramp configuration. The importance of this is that to the extent that e_2 deviates from the ideal, to corresponding extent there will be an error in the measure of elapsed time.

The successive ramps produced by the integrator including capacitor 18 form in effect a sawtooth voltage at the frequency of discharging the capacitors 16 and 18, and this frequency must be small in comparison to the sawtooth frequency at terminal 22, analogous to the restriction placed on variation in the denominator voltage in FIG. 1.

As is evident from the foregoing, the zoning of the web is basically due to the limited capacity of the integrators. For example, there are limits on the magnitudes of voltages involved in the operation of the practical instrumentalities making up the moisture gauge, integrators, and so on, so the maximum voltage that can be placed on capacitors 16 and 18 will be something less than one or another of those limits. However, the zoning is actually an advantage, because the output voltage wave form at terminal 4 is correlated with both the zones and the subzones. Accordingly, by examining the wave form at terminal 4, a wet spot on the web will be detected and can be localized to the zone or subzone in which it occurred. Also, if the use of the averages is to determine the overall moisture content of a large quantity of web, wet spot effect can be filtered out since the normal moisture content will be a few percent by weight of the paper in a normal subzone, whereas a wet spot in a subzone will produce a short peak, which will be all the more pronounced, the smaller the subzone.

The entities referred to as TRAVERSING MECHANISM, MOISTURE GAUGE, SAWTOOTH and INTEGRATOR are individually well-known in the art, so their particulars have not been described herein. As for CONTROL, it may be any sort of device which emits the appropriate control signals, e.g., pulses, at appropriate points along the moisture gauge's travel. Given the program of operation described herein for CONTROL, one skilled in the art, will be able to devise to specific forms thereof routinely, without exercising invention.

Having set forth my invention as commanded in Title 35 of the United States Code, I claim:

1. In a system involving division, wherein said system has an amplifier having high gain before feedback and a negative feedback loop interconnecting said amplifier's input and output for causing said amplifier to produce a first signal at its said output substantially in proportion to a second signal applied to its said input, said feedback loop having an element therein variable in response to a third signal applied thereto for causing said amplifier to produce said first signal in proportion to the magnitude of said second signal divided by the magnitude of said third signal,

and wherein said feedback loop has the property of providing no feedback as a result of variation of said feedback element in response to said third signal having substantially zero magnitude, and wherein said system has signal

producing means connected to said feedback element for applying said third signal to said feedback element, and said signal producing means has the property of, on occasion, providing said third signal at substantially zero magnitude,

the improvement comprising a second feedback element connected between said output and input of said amplifier independently of said first feedback element, said second feedback element being actuable between first and second states, said first state being one in which said second feedback element is ineffective to provide feedback of said output to said input, and said second state being one in which said second feedback element is effective to provide DC feedback of output to input, said second feedback element being normally in said first state; and

control means operative when the magnitude of said third signal is substantially zero to actuate said second feedback element to said second state.

2. The invention of claim 1, wherein said control means is responsive to said third signal's magnitude becoming substantially zero, for actuating said second feedback element to said second state.

3. The invention of claim 1, wherein said control means is operative to periodically effectively cause said third signal's magnitude to become substantially zero, and, substantially simultaneously, to actuate said second feedback element to said second state.

4. The invention of claim 3, wherein said signal producing means includes a ramp generator for producing a ramp signal, and a sawtooth generator for producing a sawtooth signal, said ramp signal being said third signal, and said first feedback element being jointly controlled by said ramp signal and said sawtooth signal to such affect as to be substantially ineffective to provide feedback whenever said ramp signal is substantially zero.

5. The invention of claim 4, wherein said control means actuates said second feedback element to said second state for a time interval beginning before said ramp signal decreases to substantially zero and ending after said ramp signal has next begun to increase from substantially zero.

6. The invention of claim 1, wherein said signal producing means includes an integrator having capacity for having fourth signal stored therein such that the magnitude of said third signal represents the time integral of said fourth signal, and said system includes means for removing stored fourth signal from said capacity to such extent as to make said third signal have substantially zero magnitude.

7. The invention of claim 1 wherein said element responsive to said third signal is an FET and gating means connected to the gate of said FET for causing said FET to be cut-off except when said third signal's magnitude is substantially zero; said gating means being responsive to said third signal's magnitude becoming substantially zero for causing said FET's drain/source resistance to take on a value capable of providing said predetermined amount of negative feedback, said drain/source resistance being connected across the first said feedback element, whereby to provide said second feedback element.

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