

**Declaration under Rule 4.17:**

- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for the following designation CN*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *with international search report*

Fast cascaded class AB output stage with FET devices

This invention relates to high voltage and power output circuits, and more particularly, to an improved cascaded configuration for a class AB MOS output stage.

5 High voltage and high power output circuits may be manufactured from bipolar output stages or MOS structures. A typical class AB output stage utilizing MOS structures is shown in Fig. 1.

Usually, there are several important parameters relevant to the design of a output stage. Crossover distortion should be minimized in order to provide an accurate noise-free output signal. Additionally, it is desirable to reduce static power consumption of the
10 output stage.

Over the years, numerous variations of cascaded class AB configurations have been developed. With respect to the large number of available such configurations, each has its own advantages and/or disadvantages. Several such prior art examples are discussed
15 below.

Fig. 1 depicts a cascaded class AB buffer utilizing bipolar transistors and several diodes as shown. Notably, there are four static current paths 201-204, leading to increased power consumption. As stated above, minimization of power consumption is a goal in class AB output stages. Thus, the arrangement of Fig. 1 is suboptimal.

20 Fig. 2 shows a class C Darlington output stage with biasing resistors utilizing FET technology. The arrangement of Fig. 2 would appear to consume less power than that of Fig. 1, owing to the fact that there are less current paths. It is noted however, that in the arrangement of Fig. 2, transistors M3 and M4 see the load through biasing resistors R1 and R2. For purely capacitive loads, transistors M3 and M4 must be sized properly to prevent
25 slowing down of the circuit. Often, this means utilizing larger transistors, with higher power consumption, than desirable. Thus, the larger transistors can make up for the reduction in current paths, and a relatively high power consuming device still results.

In addition to the foregoing power consumption problem, another problem in output stages is that of crossover distortion. A prior art known technique of minimizing

crossover distortion is to utilize a feedback loop to cancel such distortion. However, the implementation of such a feedback loop also results in added power consumption.

In view of the above, there exists a need in the art for an improved circuit for minimizing required current and thus power consumption of the Class AB output stage while at the same time eliminating crossover distortion.

The above and other problems with the prior art are overcome in accordance with the present invention. The present invention includes a circuit having cascaded output stages utilizing three sets of FET devices. Of the three sets of FET devices, in a preferred embodiment, a first set includes four FETs, a second set includes a different four FETs, and a third set includes two FETs. Two of the transistors from the second set and the two transistors from the third set comprise one class AB stage, and the remaining two transistors from the second set and all four transistors from the first set comprise the second class AB stage. The two stages are cascaded in a manner that reduces the required size for the transistors as well as eliminating crossover distortion. The arrangement avoids such crossover distortion without the need for a feedback loop, thereby eliminating the additional components that would otherwise be required and also minimizing power dissipation.

The circuit has the further advantage of minimizing current paths, and thus power consumption, while permitting smaller size transistors to be used, even to drive relatively highly capacitive output loads.

Further advantages of the present invention will become clear from the following detailed description and drawings.

Fig. 1 shows an exemplary prior art arrangement;

Fig. 2 depicts an additional prior art arrangement having the drawback of relatively high power consumption; and

Fig. 3 shows an exemplary embodiment of the present invention utilizing ten FET devices.

Fig. 3 shows an exemplary embodiment of the present invention utilizing ten FET devices. It is understood that the particular transistors utilized are not critical to the present invention, and that other types of active devices may be utilized.

The exemplary embodiment of Fig. 3 comprises four FET devices 601-604 connected to the input power source. The source of FET 601 is connected as shown to the gate of FET 605, and the drain of FET 604 is connected to the gate of FET 608 as also shown. FETs 608, 605 and 601-604 constitute the equivalent of a single stage of a class AB output circuit. The remaining FETs 606, 607, 609 and 610 constitute a second output stage. The two output stages are connected at a junction between FET 605 and 606, and are also connected at the junction between FETs 607 and 608.

By driving the gates of FETs 606, 607, 609 and 610 from a common source as shown, the aforementioned four transistors act as a single output stage. Moreover, since FETs 605 and 608 have their respective gates tied to the gates of FETs 601 and 604 respectively, FETs 605 and 608 are part of the first stage.

Note also that in the first stage, the gates of FETs 605, 601 and 602 are connected but the gates of the remaining FETs are connected in common to a second point. In the second stage however, the gates of all of the transistors of the stage are tied to a single common point. In summary, of the ten transistors shown, six constitute a first class AB output stage, and the remaining four constitute a second outputs stage connected in a cascaded fashion.

In operation, the power is provided to the system from source 600 through series FET devices 601-604. The signal to be amplified is provided at point 615 as shown. The signal is then amplified through the consecutive AB stages and an output is seen at point 616.

Notably, unlike the prior art arrangement of Fig. 3C, FETs 605 and 608 do not see the output through biasing resistors, since the connection 305 in Fig. 3 is not present in Fig. 4. Accordingly, the arrangement of Fig. 4 permits smaller transistors utilized in the prior art arrangements or circuits with the same response times. The use of such smaller transistors provides for reduced input capacitance and thus, lower delay.

Additionally, the circuit does not generate significant crossover distortion, thereby eliminating the need for a feedback loop in most applications. This mode of operation thus reduces power consumption. It is also noted that the system has at most three current paths, unlike some prior art arrangements that include at least four such paths.

It is understood that the above describes only the preferred embodiments and is for exemplary purposes only. Other types of active devices may be utilized, and the invention is not limited to the embodiments disclosed herein. The device may be powered by a voltage source or a current source.

CLAIMS:

1. Apparatus comprising at least a first output stage (601-605, 608) and a second output stage (606-607, 609-610), said first output stage comprising plural FET devices (601-605, 608) having gates, said plural FET devices being divided into first and second subsets, FET devices in said first subset (601, 605) being connected at their gates to a first common point, FET devices in said second subset (604, 608) being connected at their gates to a second common point (615), and all FETs in said second stage (606, 607, 609, 610) being connected at their gates to a single common point.
2. Apparatus of claim 1 wherein said first stage includes more FET devices than said second stage.
3. Apparatus of claim 2 further comprising a voltage source (601) for providing power.
4. Apparatus of claim 2 further comprising a current source (600) for providing power.
5. Apparatus of claim 4 wherein said circuit is driven with a voltage input (615).
6. A method of amplifying a signal through a cascaded output stage comprising the steps of connecting a first set of plural FETs to form a first output stage (601-605, 608), connecting a second set of FETs to form a second output stage (606, 607, 609, 610), connecting said first output stage to said second output stage at least two points, and connecting all gates of said second set of FETs to a common point.
7. The method of claim 6 wherein all gates of said first set of FETs (601-605, 608) are not connected to a common point.

8. The method of claim 7 wherein said gates of said first set are divided into two subsets, and further comprising connecting all gates in each of said subsets to a separate common point.

5 9. The method of claim 8 wherein said first set includes more FETs than said second set.

10. The method of claim 9 wherein further including connecting the source to the gate for at least two of the FETs (601, 602) in said first set.

10

11. The method of claim 10 further comprising connecting the gate to the drain for at least two of said FETs in said second set (606, 607).

12. method of claim 11 further comprising connecting the gate to the drain for at
15 least two FETs in said first set (603, 604).

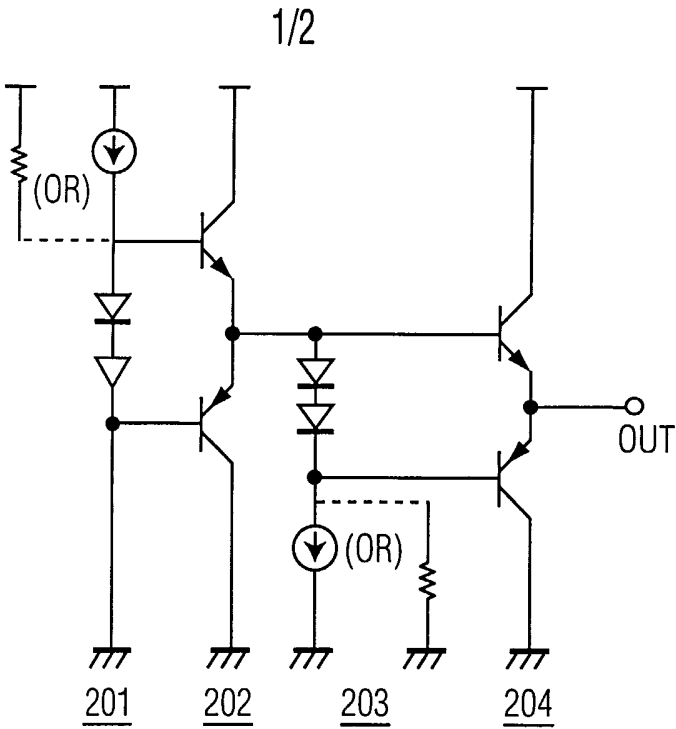


FIG. 1

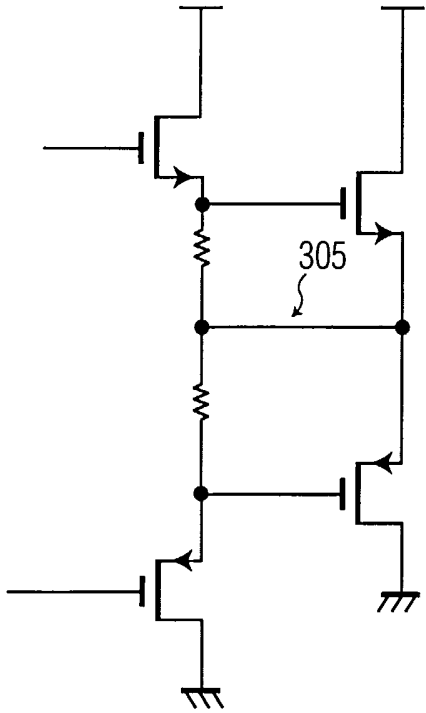


FIG. 2

2/2

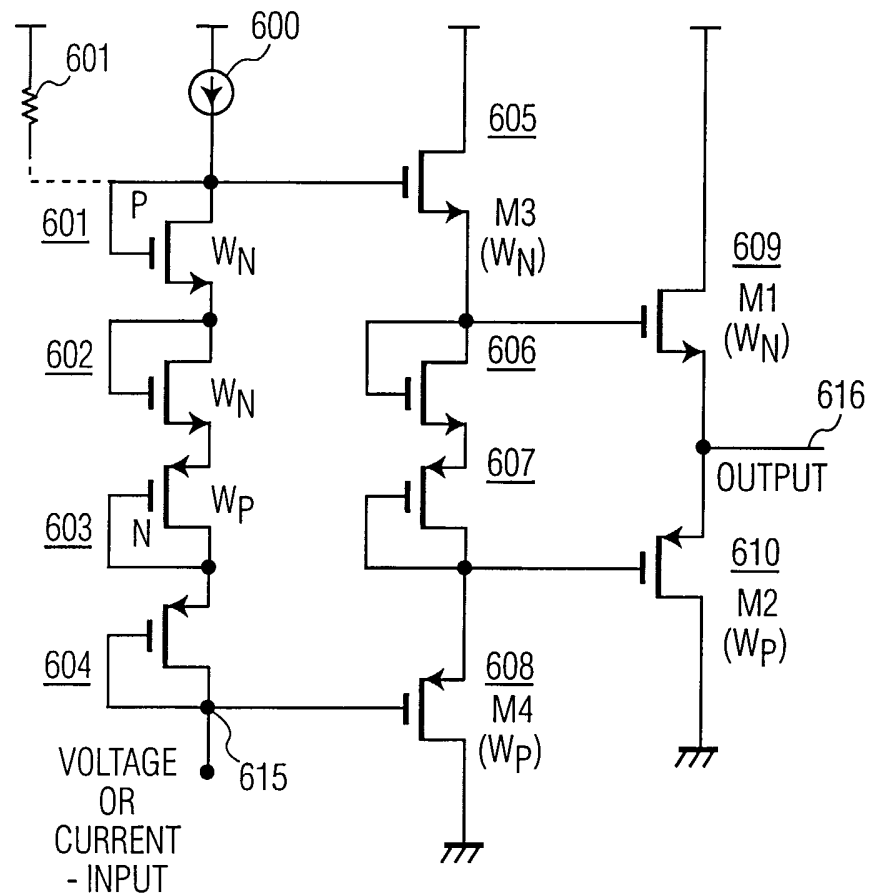


FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 03/01708

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/16 H03F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 973 563 A (SEVEN KAZIM) 26 October 1999 (1999-10-26) column 3, line 28 -column 4, line 21 abstract	1-12
P,A	US 6 466 093 B1 (YAN SHOULI) 15 October 2002 (2002-10-15) column 1, line 52 -column 2, line 10	1-12
A	US 6 175 277 B1 (MAVENCAMP DANIEL) 16 January 2001 (2001-01-16) column 1, line 7 -column 2, line 46	1-12
	--- -/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

16 July 2003

Date of mailing of the international search report

01 09. 2003

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

ANNA FLODMAN/MN

INTERNATIONAL SEARCH REPORT

Intern I Application No
PCT/IB 03/01708

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 09, 30 September 1997 (1997-09-30) & JP 09 114531 A (SEIKO EPSON CORP), 2 May 1997 (1997-05-02) abstract -----	1-12

INTERNATIONAL SEARCH REPORT

Intern I Application No
PCT/IB 03/01708

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5973563 A	26-10-1999	US 6154094 A	28-11-2000
US 6466093 B1	15-10-2002	NONE	
US 6175277 B1	16-01-2001	NONE	
JP 09114531 A	02-05-1997	NONE	