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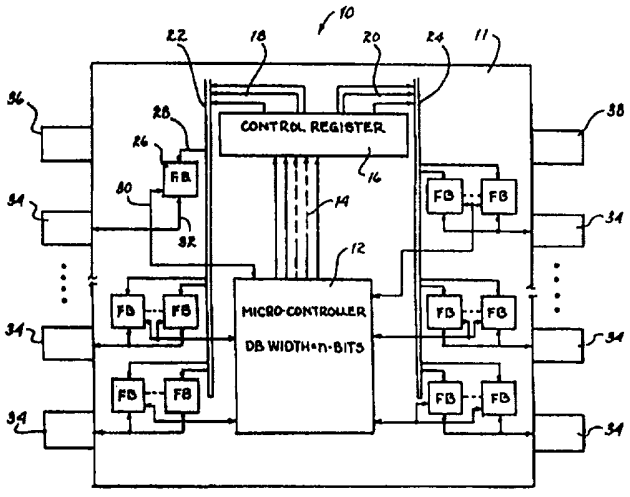
(54) Title: A MICROCONTROLLER HAVING AN N-BIT DATA BUS WIDTH WITH LESS THAN N I/O PINS AND A METHOD THEREFOR



(57) Abstract

An Integrated Circuit (IC) (10) package is disclosed comprising an IC chip (11) with a microcontroller (12) therein having an n-bit data bus, and up to n pins (34-38) electrically coupled to the microcontroller (12). The IC package also includes a control register coupled to the microcontroller for receiving enable and disable signals from the microcontroller. One or more of the pins have one or more functional blocks associated thereto. Each functional block defines a specified function for its corresponding pin. Thus, each pin having a plurality of corresponding functional blocks has a number of potential functions equal to the number of corresponding functional blocks. The specific function for a given pin is selected by the enable signal from the control register which selects the appropriate functional block upon appropriate command from the microcontroller. By using pins with multiple functions, the instant invention permits an n-bit architecture microcontroller to use less than or up to n pins.

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A MICROCONTROLLER HAVING AN N-BIT DATA BUS WIDTH WITH LESS THAN N I/O PINS AND A METHOD THEREFOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention is in the field of microcontrollers and methods therefor and, more particularly, is a microcontroller having an n-bit architecture (i.e., data bus width) with less than n Input/Output (I/O) pins and a method therefore.

2. Description of the Related Art

Microcontrollers are widely known and used in many different applications. A typical architecture used in microcontrollers today is the 8-bit architecture (i.e., the data bus width of the microcontroller is 8 bits wide). One problem with this and other sizes of microcontrollers is that to support an n-bit architecture, greater than n pins are required to be connected to the microcontroller. By reducing the number of pins required to support an n-bit, or more particularly, an 8-bit microcontroller, the overall cost of using the device is reduced, and limited space is conserved. Therefore, there existed a need to provide a microcontroller having an n-bit architecture with less than or equal to n pins and a method therefor.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a microcontroller having an n-bit architecture with less than or equal to n pins coupled to the microcontroller and a method therefor.

Another object of the present invention is to provide a microcontroller having an n bit architecture with the number of I/O pins less than n and a method therefor.

Yet another object of the present invention is to provide a microcontroller package with pins for performing multiple functions and a method therefor.

Still another object of the present invention is to provide a microcontroller with n-bit data processing capability and fewer than n I/O pins and a method therefor.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to the present invention, an Integrated Circuit (IC) package is disclosed comprising, in combination, an IC chip with a microcontroller therein having an n-bit data bus, and up to n pins electrically coupled to the microcontroller. The IC package further comprises control register means coupled to the microcontroller for receiving enable and disable signals. Pin function configuration means are also included coupled to the control register means for determining a function for a corresponding one of the n pins. The pin function configuration means comprises at least one functional block means coupled to the control register means for determining a function for a corresponding pin. The pin function configuration means may comprise a plurality of the functional block means each coupled to the control register means and to a corresponding pin of the n pins for determining a different function for the corresponding one of the n pins. The control register means provides independent control line means to each functional block means for transferring to each function block means one of the enable and the disable signals. Only one of the functional block means per pin is enabled at a time by the enable signal to configure a corresponding pin for a function associated with the enabled functional block means. Each functional block means is coupled to a corresponding one of the n pins and to the microcontroller for transferring data between the corresponding pin and the microcontroller when a particular one of the functional blocks is enabled. Additionally, the n pins include a number of Input/Output (I/O) type pins less than n.

Alternatively, a method of operating an Integrated Circuit (IC) package is disclosed comprising the steps of providing an IC chip with a microcontroller therein having an n-bit data bus, and providing up to n pins electrically coupled to the microcontroller.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiments of the invention, as illustrated in the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a simplified block diagram view of the IC microcontroller package having an n-bit data bus and n pins.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, the IC package or package of the instant invention is shown and generally designated by reference number 10. IC package 10 comprises an IC chip 11 with a microcontroller core or simply microcontroller 12 therein having an n-bit Data Bus (DB), and up to n pins 34-38 electrically coupled to the microcontroller 12. The manner of fabricating IC packages 10, chips 11, and microcontrollers 12 are well known to those skilled in the art. Microcontroller 12 has, in general, an n-bit wide data bus, but more specifically here an 8-bit architecture or data bus width. Note that the data bus itself is not shown in detail for simplification of the drawing.

The IC package 10 further comprises a control register 16 coupled to the microcontroller 12 via a control signal bus 14 for receiving enable and disable signals from the microcontroller 12. Control registers are well known to those skilled in the art. The control register 16 can be any element that can hold a known state (i.e., charge, current, or voltage) such as SRAM, DRAM, EPROM, EEPROM, ROM, Combinational Logic, PROM, or the like. The control register 16 provides sufficient memory capacity to store and transfer the enable and disable signals sent from the microcontroller 12 to the functional blocks 26, which will be described later. The communications protocol for sending the enable and disable signals from the microcontroller 12 to the functional blocks 26 via the control register 16 is well known to those skilled in the art. The enable and disable signals are routed from the control register 16 to the appropriate functional blocks 26 via buses 18-24. From buses 22 and 24, each functional block 26 is coupled via connector 28 to receive the enable or disable signal sent from the control register 16. Note also that each functional block 26 has a connection 32 to a respective pin 34 to transfer data to or from the pin 34. Additionally, each functional block 26 has a connection 30 to the microcontroller 12 to transfer to or receive from the microcontroller 12 the appropriate data.

Note that pins 36 and 38 have no functional blocks 26 coupled thereto. This is because these pins 36 and 38 are the power and ground supply pins for the package 10, and therefore, they require no functional blocks 26. Note that the individual power and ground lines from pins 36 and 38 are not shown for simplification of the drawing. Pins 34 represent either input only or I/O type pins, both of which are well known in the art. Which of pins 34 are input only and which are I/O type depends on the user's application. Note that the second pin 34 from the top left corner of the package 10 only has one functional block 26 coupled to it. Thus, this particular pin 34 has only one function associated with it. Note that this single function depiction is shown only for the purpose of demonstrating how a single function pin 34 would look. Thus, any of the pins 34 could be single function pins, or multiple function pins 34. Additionally, note that the other pins 34 are shown with two functional blocks 26 per pin 34, and therefor these pins 34 have two functions. In other words, the number of functions per pin 34 equals the number of functional blocks associated with that pin 34. Accordingly, any of the pins 34 could have one, two, or more functional blocks 26 associated thereto. This is represented in the drawing by the dashed lines between the functional blocks 26. Additionally note the dashed lines between pins 34, which indicate that this package 10 could have more or less than eight pins 34-38, but the key is that the number of pins 34-38 is less than or equal to the data bus width of the microcontroller 12.

The pin function configuration portion of the package 10 is defined as simply one or more functional blocks 26. The internals of the functional blocks 26 are not shown for simplification of the drawing. The functions that pins 34-38 must support for a microcontroller 12 are well known to those skilled in the art such as a Bi-Directional I/O Port pin, a Serial Programming Data pin, a Serial Programming Clock pin, and the like. The point is that there are many functions that pins 34-38 support for a microcontroller 12, they are all well known, and need not be specifically designated. Further, functional blocks 26, which enable a particular pin 34-38 to behave as required for a given function, are also well known in the art, and therefore need not be shown in detail. A key feature of the instant invention is that

because pins 34 are multi-functional, only n pins 34-38 are required and all data control commands for the microcontroller 12 having an n-bit (i.e., 8-bit) data bus use the full n-bit bus.

OPERATION

Referring to Figure 1, when executing an instruction, the microcontroller 12 sends appropriate control signals to the control register 16, which enables and disables the appropriate functional blocks 26 for a given pin 34. Note that since several functional blocks 26 can be used per pin 34, only one functional block can be enabled at a time. Data travels into the package 10 from a pin 34, through a corresponding connector 32, the enabled functional block 26, a corresponding connector 30, and to the microcontroller 12. The reverse path sends data from the microcontroller 12 out of a particular pin 34 of the package 10. Whether the flowpath of data be into or out of the microcontroller 12, the microcontroller 12 sends appropriate enable and disable signals to the appropriate functional blocks 26 in order to operate the desired pins 34 as required.

Although the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is Claimed is:

1. An Integrated Circuit (IC) package comprising, in combination:

an IC chip with a microcontroller therein having an n-bit data bus; and

up to n pins electrically coupled to said microcontroller.

2. The IC package of Claim 1 further comprising control register means coupled to said microcontroller for receiving enable and disable signals.

3. The IC package of Claim 2 further comprising pin function configuration means coupled to said control register means for determining a function for a corresponding one of said n pins.

4. The IC package of Claim 3 wherein said pin function configuration means comprises at least one functional block means coupled to said control register means for determining a function for a corresponding pin.

5. The IC package of Claim 4 wherein said pin function configuration means comprises a plurality of said functional block means each coupled to said control register means and to a corresponding pin of said n pins for determining a different function for said corresponding one of said n pins.

6. The IC package of Claim 4 wherein said control register means provides independent control line means to each functional block means for transferring to each function block means one of said enable and said disable signals.

7. The IC package of Claim 6 wherein only one of said functional block means per pin is enabled at a time by said enable signal to configure a corresponding pin for a function associated with said enabled functional block means.

8. The IC package of Claim 6 wherein each of said functional block means is coupled to a corresponding one of said n pins and to said microcontroller for transferring data between said corresponding pin and said microcontroller when a particular one of said functional blocks is enabled.

9. The IC package of Claim 1 wherein said n pins include a number of Input/Output (I/O) type pins less than n.

10. The IC package of Claim 1 wherein a plurality of said n pins each perform a plurality of functions.

11. A method of operating an Integrated Circuit (IC) package comprising the steps of:

providing an IC chip with a microcontroller therein having an n-bit data bus; and

providing up to n pins electrically coupled to said microcontroller.

12. The method Claim 11 further comprising the step of providing control register means coupled to said microcontroller for receiving enable and disable signals.

13. The method Claim 12 further comprising the step of providing pin function configuration means coupled to said control register means for determining a function for a corresponding one of said n pins.

14. The method of Claim 13 wherein the step of providing said pin function configuration means comprises the step of providing at least one functional block means coupled to said control register means for determining a function for a corresponding pin.

15. The method of Claim 14 wherein the step of providing said pin function configuration means comprises the step of providing a plurality of said functional block means each coupled to said control register means and to a corresponding pin of said n pins for determining a different function for said corresponding one of said n pins.

16. The method Claim 14 wherein the step of providing said control register means provides independent control line means to each functional block means for transferring to each function block means one of said enable and said disable signals.

17. The method of Claim 16 wherein only one of said functional block means per pin is enabled at a time by said enable signal to configure a corresponding pin for a function associated with said enabled functional block means.

18. The method of Claim 16 wherein each of said functional block means is coupled to a corresponding one of said n pins and to said microcontroller for transferring data between said corresponding pin and said microcontroller when a particular one of said functional blocks is enabled.

19. The method of Claim 11 wherein the step of providing up to said n pins includes the step of providing a number of Input/Output (I/O) type pins less than n.

20. The IC package of Claim 1 wherein data control commands of said microcontroller operate upon n-data bits.

AMENDED CLAIMS

[received by the International Bureau on 29 October 1997 (29.10.97);
original claims 1-20 replaced by
new claims 1-20 (5 pages)]

1. An Integrated Circuit (IC) package comprising, in combination:

an IC chip with a microcontroller therein having an n-bit data bus; and

up to n pins electrically coupled to said microcontroller wherein at least one of said n pins is a multiple function pin.

2. The IC package of Claim 1 further comprising control register means coupled to said microcontroller for storing enable and disable signals from said microcontroller and for transferring said enable and disable signals to said at least one of said n pins which is a multiple function pin to enable and disable a desired function of said at least one of said n pins which is a multiple function pin.

3. The IC package of Claim 2 further comprising pin function configuration means coupled to said control register means for determining a function for a corresponding one of said n pins.

4. The IC package of Claim 3 wherein said pin function configuration means comprises at least one functional block means coupled to said control register means and to a corresponding pin of said n pins for determining a different function for said corresponding pin.

5. The IC package of Claim 4 wherein said pin function configuration means comprises a plurality of said functional block means each coupled to said control register means and said at least one of said n pins which is a multiple function pin wherein each of said plurality of said function block means provides a different function for said at least one of said n pins which is a multiple function pin.

6. The IC package of Claim 4 wherein said control register means provides independent control line means to each functional block means for transferring to each function block means one of said enable and said disable signals.

7. The IC package of Claim 6 wherein only one of said functional block means per pin is enabled at a time by said enable signal to configure a corresponding pin for a function associated with said enabled functional block means.

8. The IC package of Claim 6 wherein each of said functional block means is coupled to a corresponding one of said n pins and to said microcontroller for transferring data between said corresponding pin and said microcontroller when a particular one of said functional blocks is enabled.

9. The IC package of Claim 1 wherein said n pins include a number of Input/Output (I/O) type pins less than n.

10. The IC package of Claim 1 wherein a plurality of said n pins each perform a plurality of functions.

11. A method of operating an Integrated Circuit (IC) package comprising the steps of:

providing an IC chip with a microcontroller therein having an n-bit data bus; and

providing up to n pins electrically coupled to said microcontroller wherein at least one of said n pins is a multiple function pin.

12. The method Claim 11 further comprising the step of providing control register means coupled to said microcontroller for storing enable and disable signals from said microcontroller and for transferring said enable and disable signals to said at least one of said n pins which is a multiple function pin to enable and disable a desired function of said at least one of said n pins which is a multiple function pin.

13. The method Claim 12 further comprising the step of providing pin function configuration means coupled to said control register means for determining a function for a corresponding one of said n pins.

14. The method of Claim 13 wherein the step of providing said pin function configuration means comprises the step of providing at least one functional block means coupled to said control register means for determining a function for a corresponding pin.

15. The method of Claim 14 wherein the step of providing said pin function configuration means comprises the step of providing a plurality of said functional block means each coupled to said control register means and said at least one of said n pins which is a multiple function pin wherein each of said plurality of said function block means provides a different function for said at least one of said n pins which is a multiple function pin.

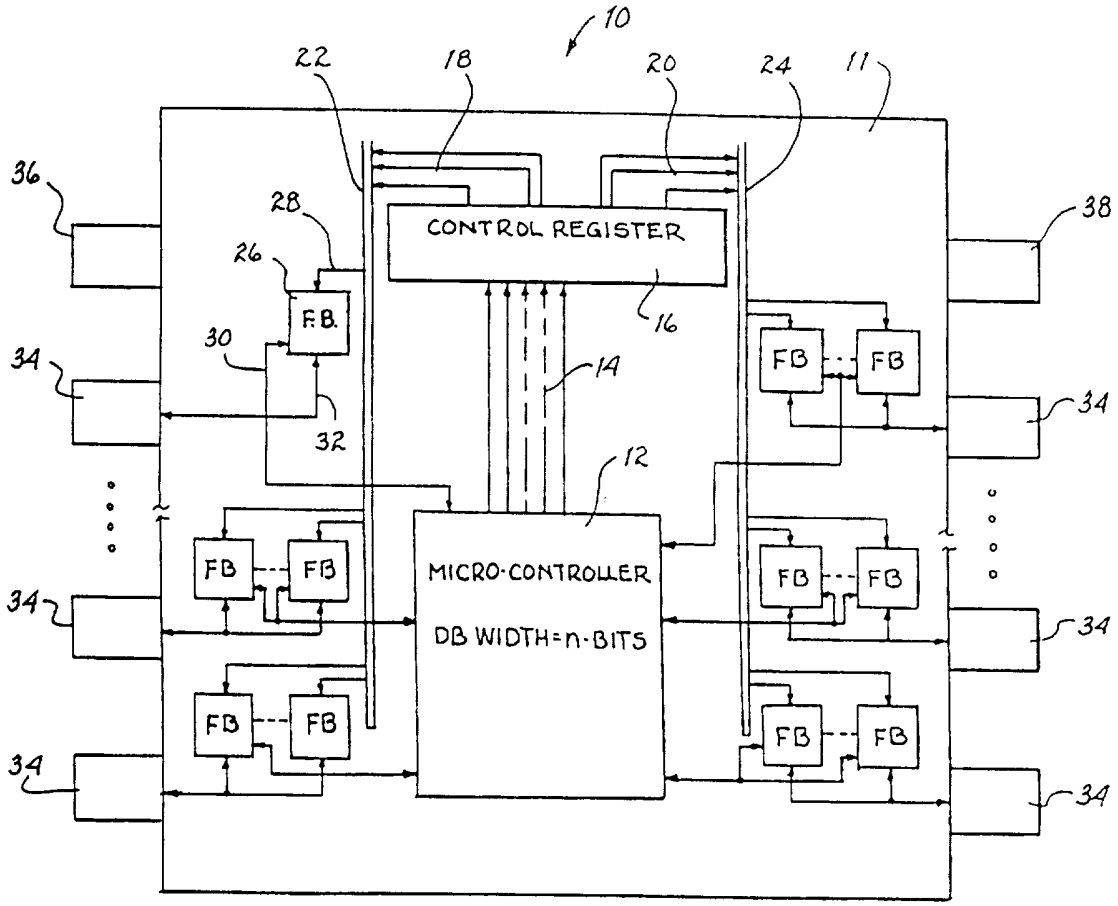
16. The method Claim 14 wherein the step of providing said control register means provides independent control line means to each functional block means for transferring to each function block means one of said enable and said disable signals.

17. The method of Claim 16 wherein only one of said functional block means per pin is enabled at a time by said enable signal to configure a corresponding pin for a function associated with said enabled functional block means.

18. The method of Claim 16 wherein each of said functional block means is coupled to a corresponding one of said n pins and to said microcontroller for transferring data between said corresponding pin and said microcontroller when a particular one of said functional blocks is enabled.

19. The method of Claim 11 wherein the step of providing up to said n pins includes the step of providing a number of Input/Output (I/O) type pins less than n.

20. The IC package of Claim 1 wherein data control commands of said microcontroller operate upon n-data bits.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18
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11
36
28
CONTROL REGISTER
26
F.B.
16
38
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14
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34
32
12
FB
FB
MICRO-CONTROLLER
DB WIDTH=n-BITS
34
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FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/07243

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L/23/48, 23/34, 21/60
US CL : 257/692, 697, 723, 724; 437/209, 205
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/692, 697, 723, 724; 437/209, 205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,463,249 A (SHINBO ET AL) 31 October 1995 (31-10-95), see entire document	1 - 20
Y	US 4,866,508 A (EICHELBERGER ET AL) 12 September 1989 (12-09-89), see Figure 4.	1 - 20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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