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Essex

(54) **Conference bridge**

(57) A conference bridge for a digital time division multiplex pulse code modulation telecommunication exchange in which for simplicity of operation each conference is allocated a unique channel number and each party within a conference is allocated a unique party number thus allowing any party to join any conference at any time.

GB 2 134 751 A

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

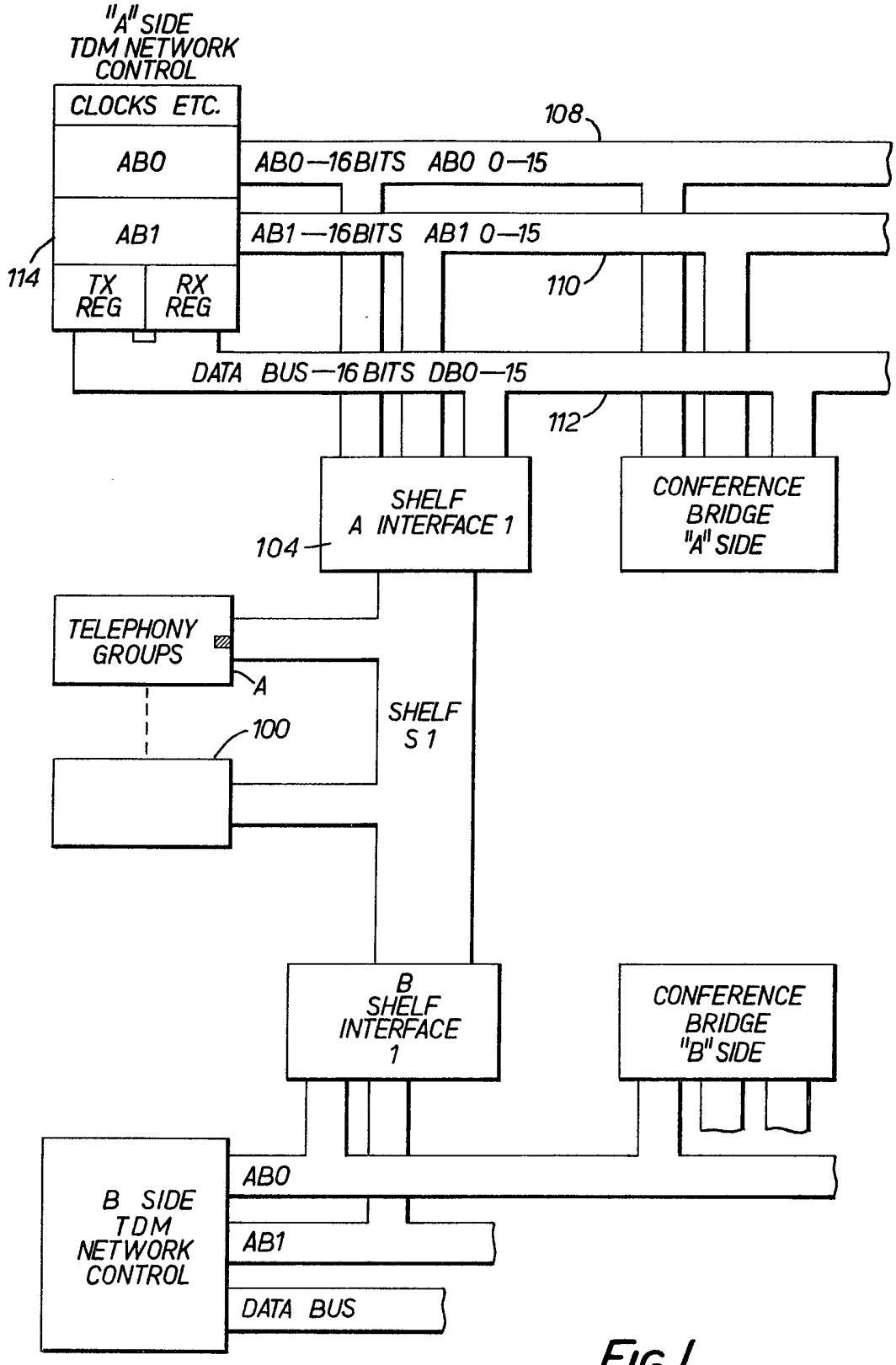

"A" SIDE
TDM NETWORK
CONTROL
CLOCKS ETC.
AB0
AB1
TX
REG
RX
REG
114
108
AB0—16BITS AB0 0—15
AB1—16BITS AB1 0—15
110
DATA BUS—16 BITS DB0—15
112
SHELF
A INTERFACE 1
104
CONFERENCE
BRIDGE
"A" SIDE
TELEPHONY
GROUPS
A
100
SHELF
S 1
B
SHELF
INTERFACE
1
CONFERENCE
BRIDGE
"B" SIDE
B SIDE
TDM
NETWORK
CONTROL
AB0
AB1
DATA BUS

FIG. 1.

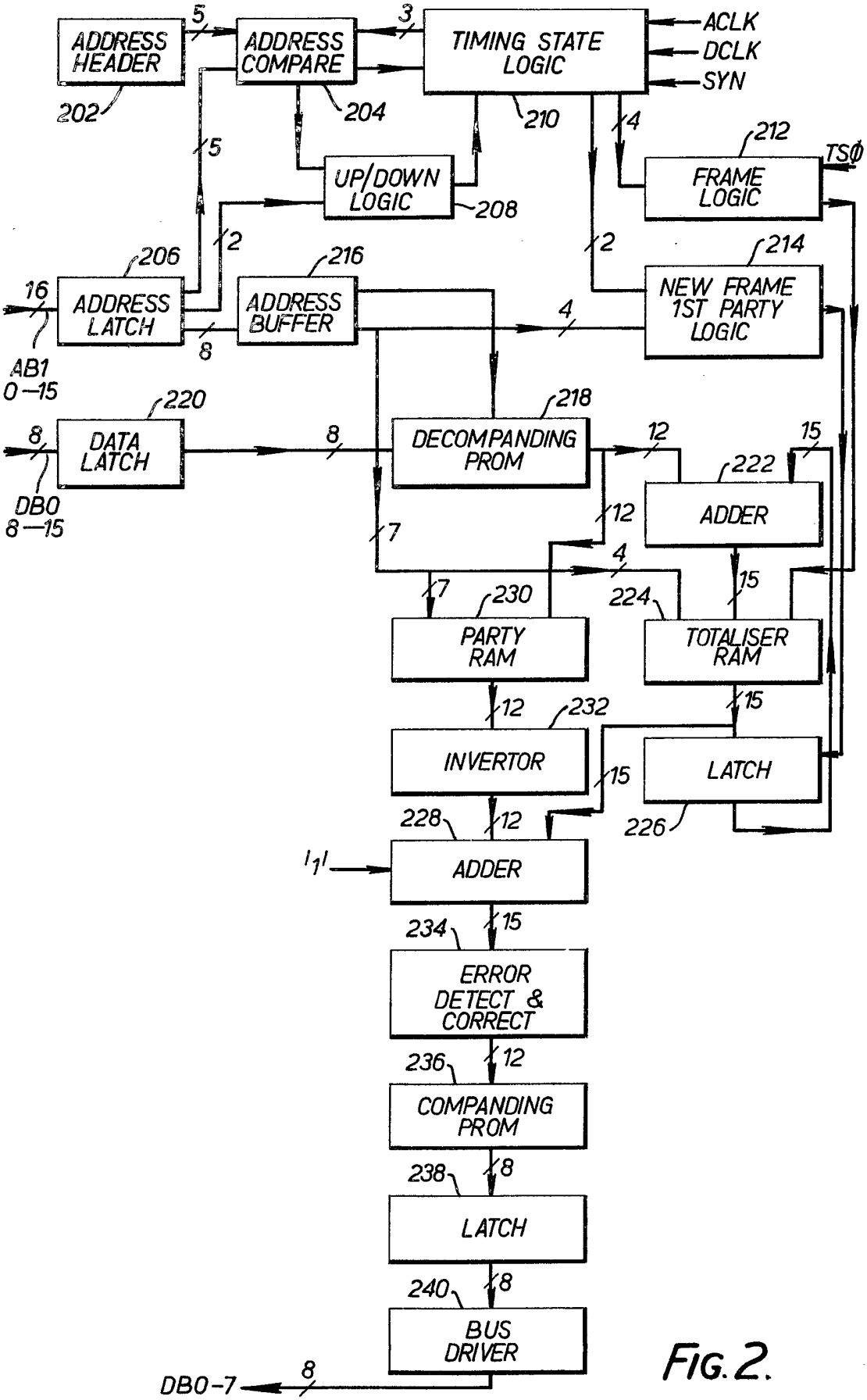

ADDRESS HEADER
202
ADDRESS COMPARE
204
TIMING STATE LOGIC
210
ACLK
DCLK
SYN
UP/DOWN LOGIC
208
FRAME LOGIC
212
TSØ
ADDRESS LATCH
206
ADDRESS BUFFER
216
NEW FRAME 1ST PARTY LOGIC
214
AB1 0—15
DATA LATCH
220
DBO 8—15
DECOMPANDING PROM
218
ADDER
222
PARTY RAM
230
TOTALISER RAM
224
INVERTOR
232
LATCH
226
'1'
ADDER
228
ERROR DETECT & CORRECT
234
COMPANDING PROM
236
LATCH
238
BUS DRIVER
240
DBO-7

FIG. 2.

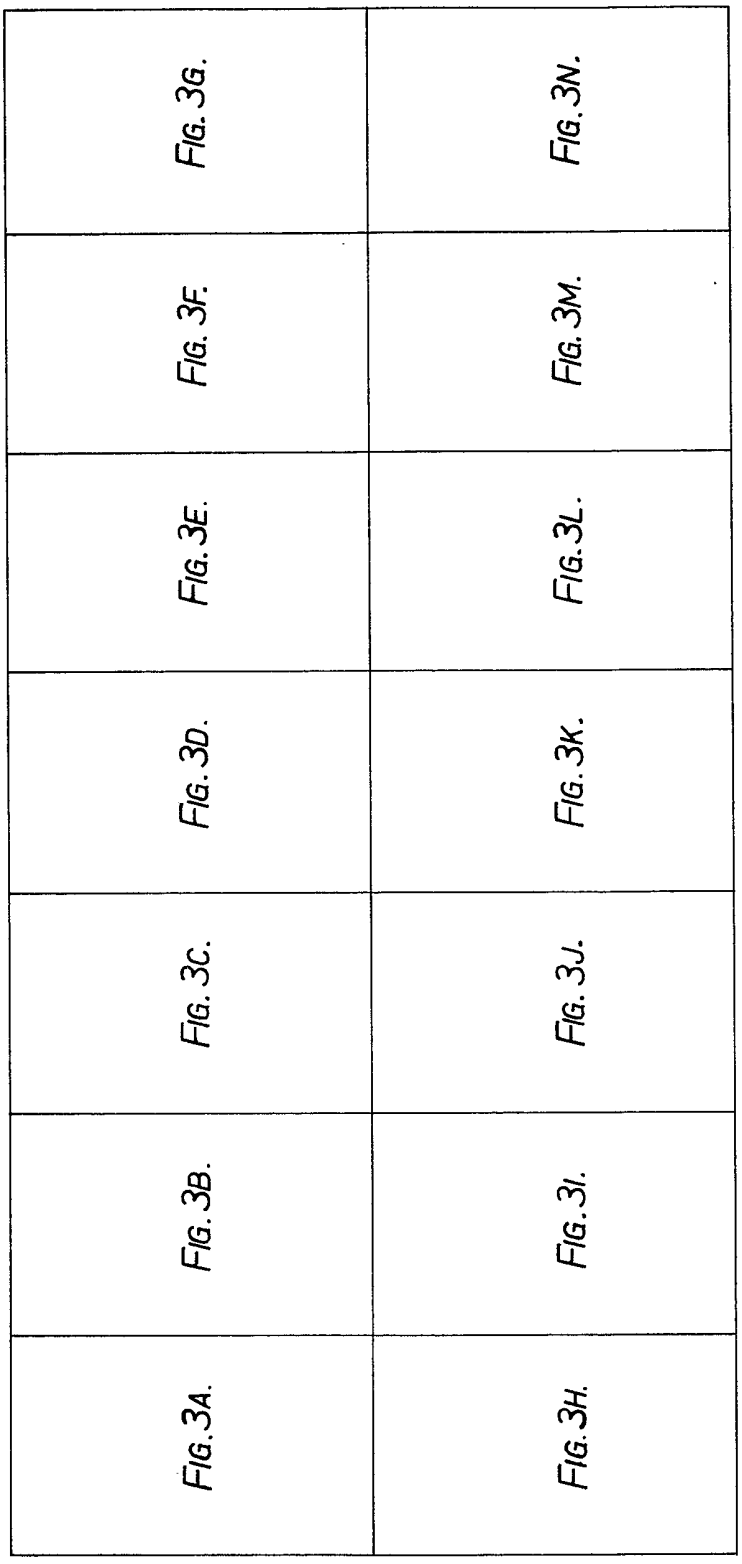

FIG. 3A.
FIG. 3B.
FIG. 3C.
FIG. 3D.
FIG. 3E.
FIG. 3F.
FIG. 3G.
FIG. 3H.
FIG. 3I.
FIG. 3J.
FIG. 3K.
FIG. 3L.
FIG. 3M.
FIG. 3N.

FIG. 3.

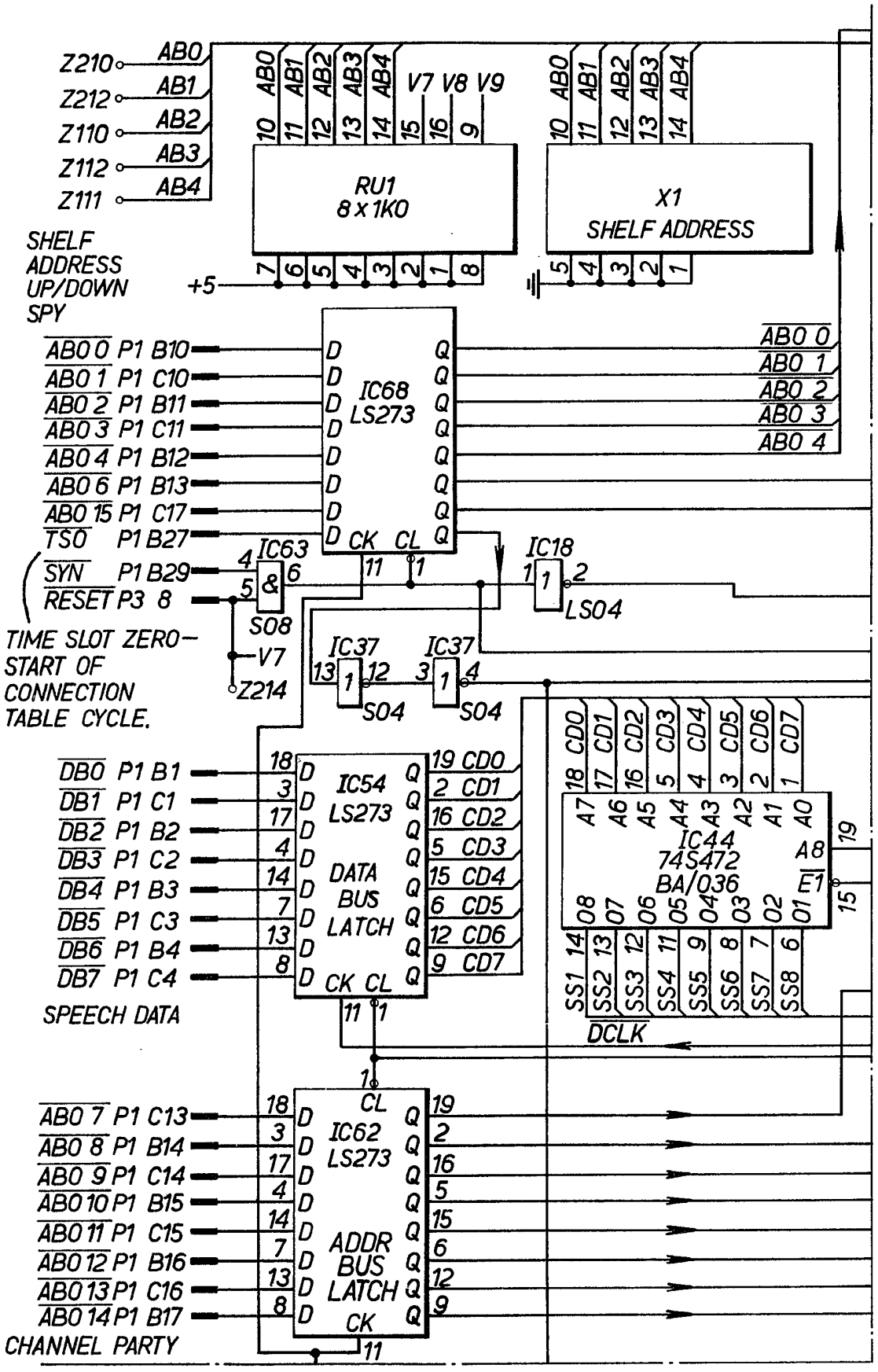

Z210
Z212
Z110
Z112
Z111
AB0
AB1
AB2
AB3
AB4
SHELF ADDRESS UP/DOWN SPY
+5
RU1
8 x 1KO
V7 V8 V9
X1
SHELF ADDRESS
IC68
LS273
IC63
S08
IC18
LS04
IC37
S04
TIME SLOT ZERO— START OF CONNECTION TABLE CYCLE.
V7
Z214
IC54
LS273
DATA BUS LATCH
SPEECH DATA
IC44
74S472
BA/036
DCLK
IC62
LS273
ADDR BUS LATCH
CHANNEL PARTY

FIG. 3A.

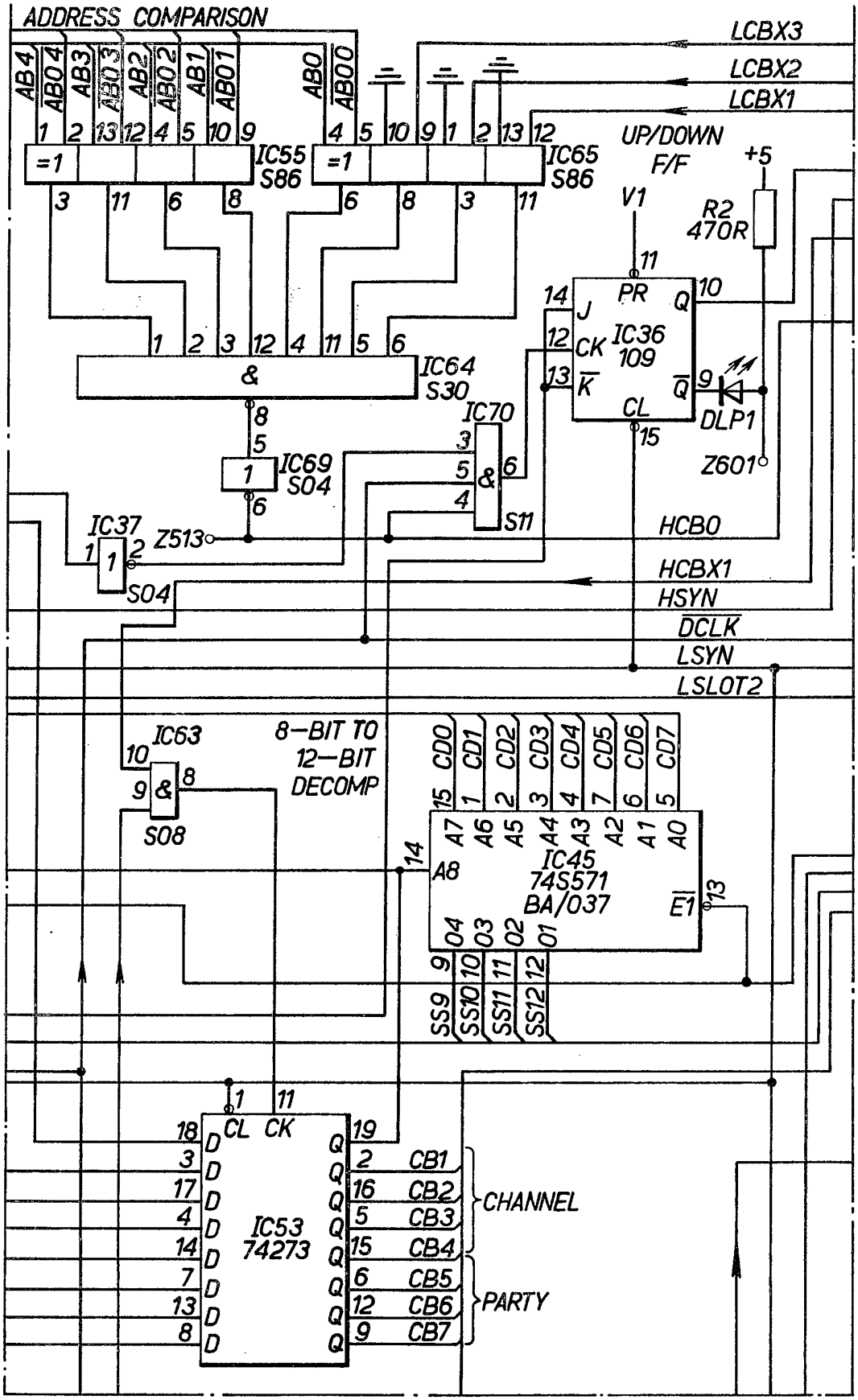

ADDRESS COMPARISON
LCBX3
LCBX2
LCBX1
AB4
AB04
AB3
AB03
AB2
AB02
AB1
AB01
AB0
AB00
IC55
S86
IC65
S86
UP/DOWN
F/F
+5
V1
R2
470R
IC36
109
PR
J
CK
K
CL
Q
DLP1
Z601
IC64
S30
IC70
S11
IC69
S04
IC37
S04
Z513
HCB0
HCBX1
HSYN
DCLK
LSYN
LSLOT2
IC63
S08
8-BIT TO
12-BIT
DECOMP
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
IC45
74S571
BA/037
A8
E1
SS9
SS10
SS11
SS12
IC53
74273
CB1
CB2
CB3
CB4
CB5
CB6
CB7
CHANNEL
PARTY

FIG. 3B.

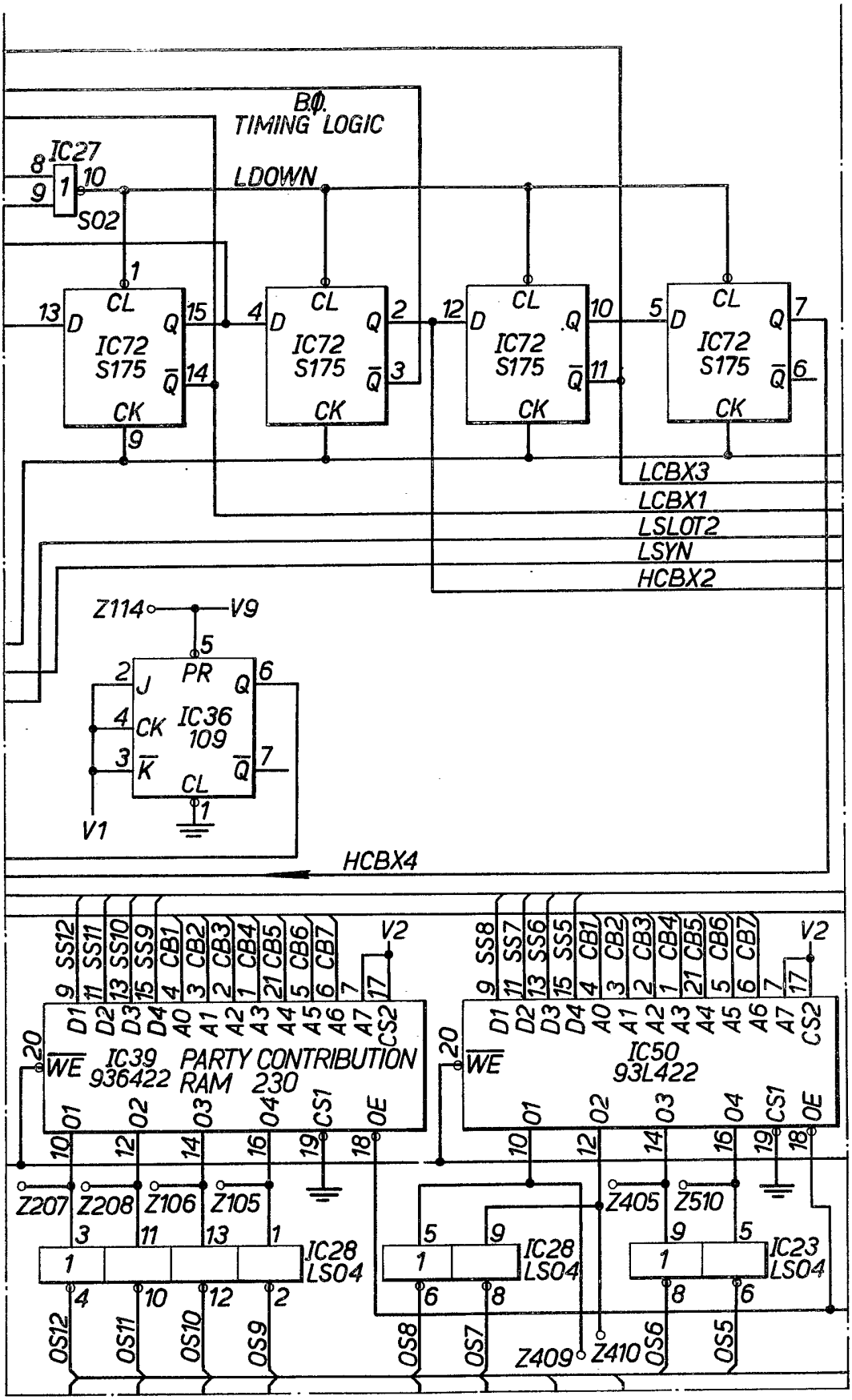

BØ.
TIMING LOGIC
IC27
LDOWN
SO2
IC72
S175
CL
D
Q
CK
LCBX3
LCBX1
LSLOT2
LSYN
HCBX2
Z114
V9
IC36
109
PR
J
K
V1
HCBX4
V2
IC39
936422
RAM 230
PARTY CONTRIBUTION
IC50
93L422
WE
Z207
Z208
Z106
Z105
Z405
Z510
IC28
LS04
IC23
OS12
OS11
OS10
OS9
OS8
OS7
OS6
OS5
Z409
Z410

FIG. 3C.

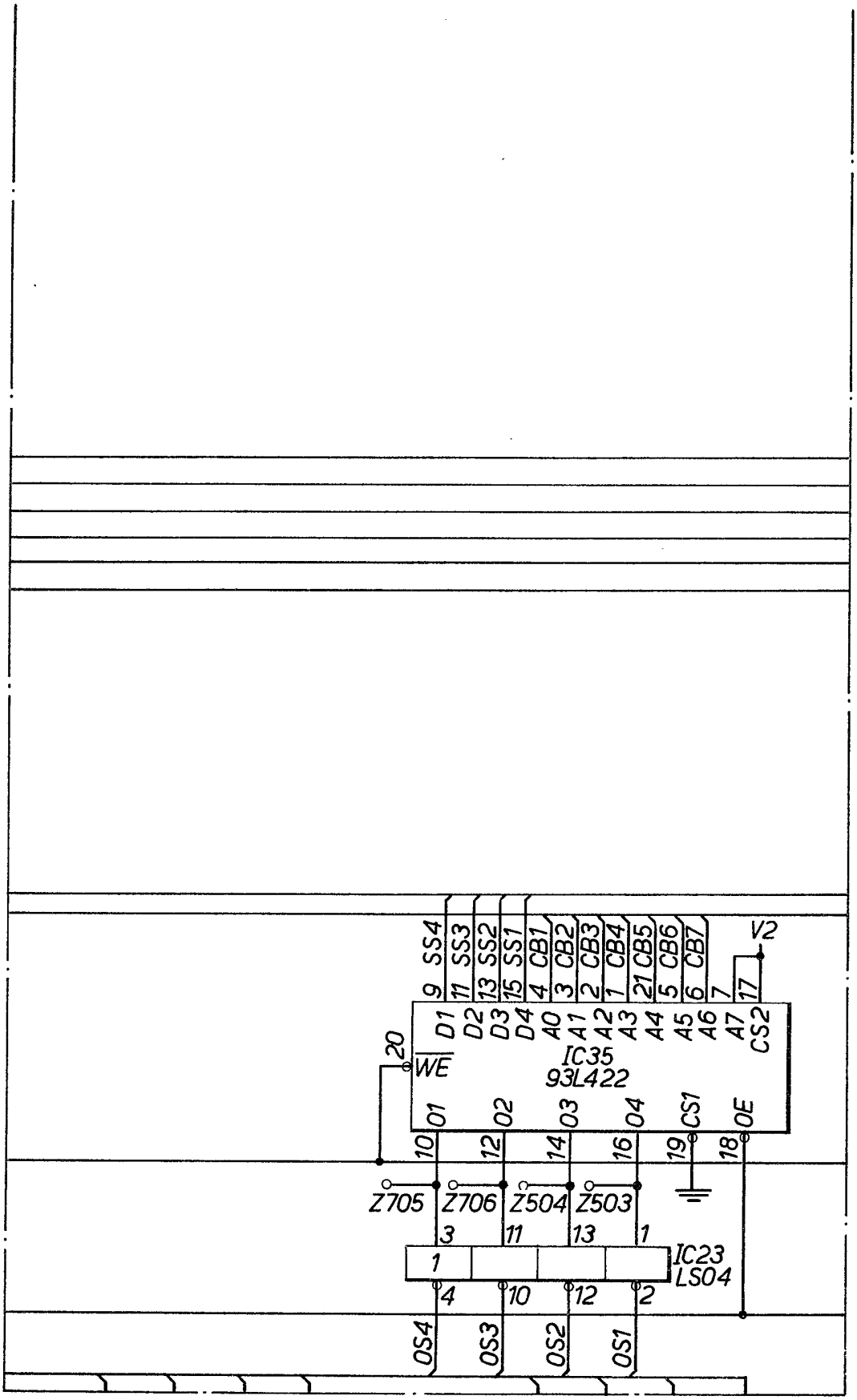

SS4
SS3
SS2
SS1
CB1
CB2
CB3
CB4
CB5
CB6
CB7
V2
9
11
13
15
4
3
2
1
21
5
6
7
17
D1
D2
D3
D4
A0
A1
A2
A3
A4
A5
A6
A7
CS2
20
WE
IC35
93L422
O1
O2
O3
O4
CS1
OE
10
12
14
16
19
18
Z705
Z706
Z504
Z503
3
11
13
1
1
IC23
LS04
4
10
12
2
OS4
OS3
OS2
OS1

FIG. 3D.

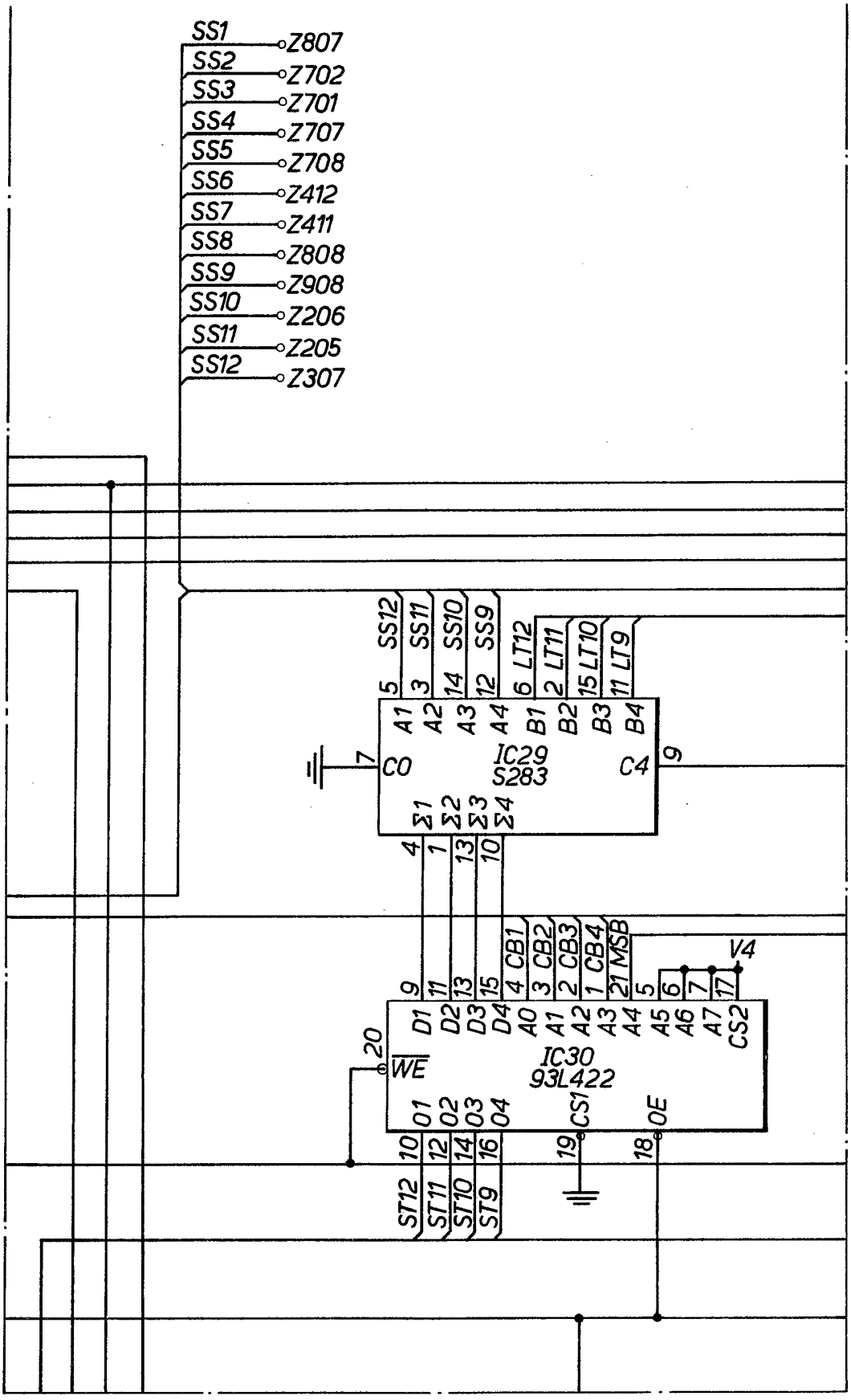

SS1
SS2
SS3
SS4
SS5
SS6
SS7
SS8
SS9
SS10
SS11
SS12
Z807
Z702
Z701
Z707
Z708
Z412
Z411
Z808
Z908
Z206
Z205
Z307
IC29
S283
C0
C4
IC30
93L422
WE
CS1
CS2
OE
V4
MSB

FIG. 3E.

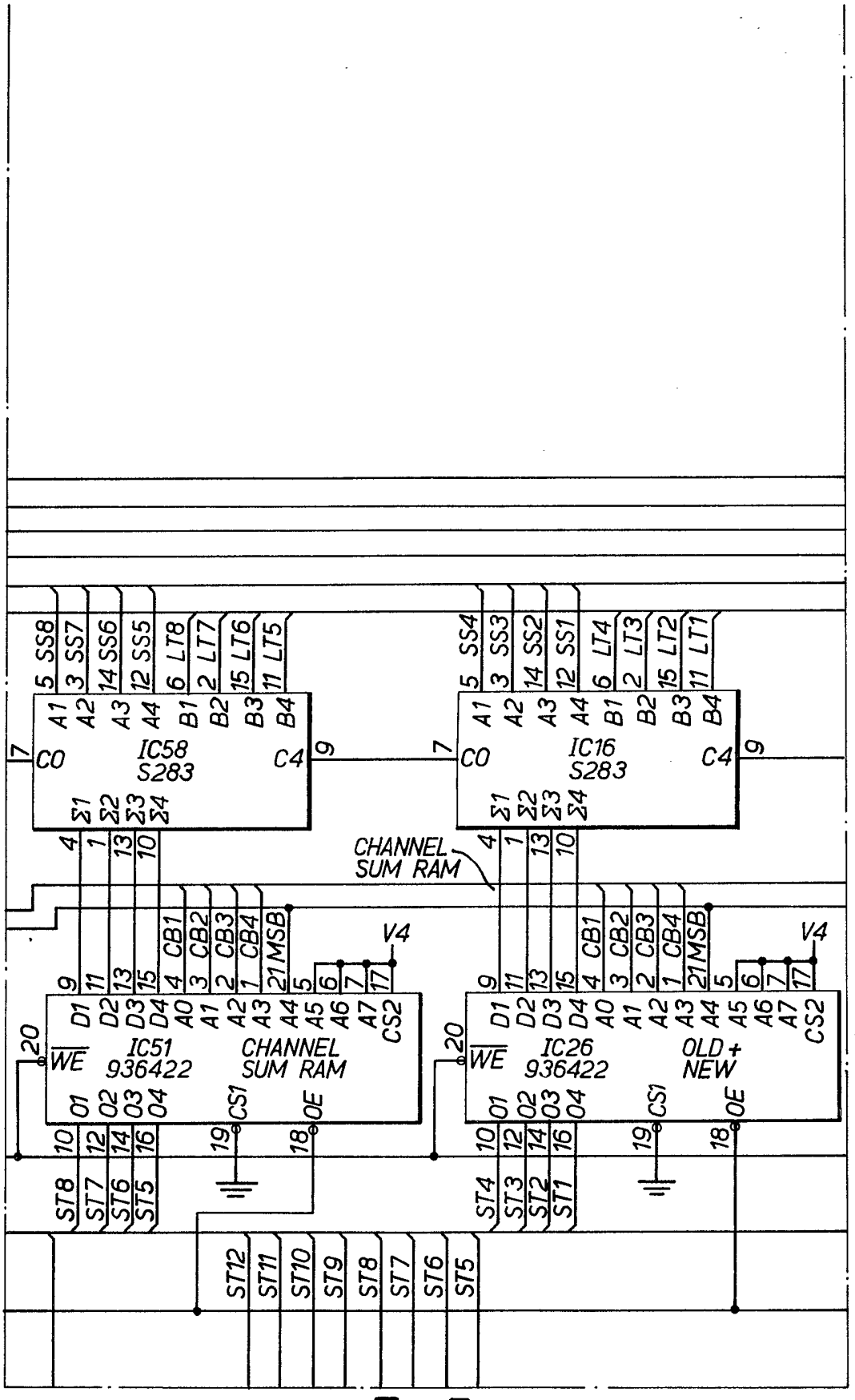

IC58
S283
IC16
S283
CHANNEL
SUM RAM
IC51
936422
CHANNEL
SUM RAM
IC26
936422
OLD +
NEW
V4
V4
WE
WE
CS1
OE
CS2

FIG. 3F.

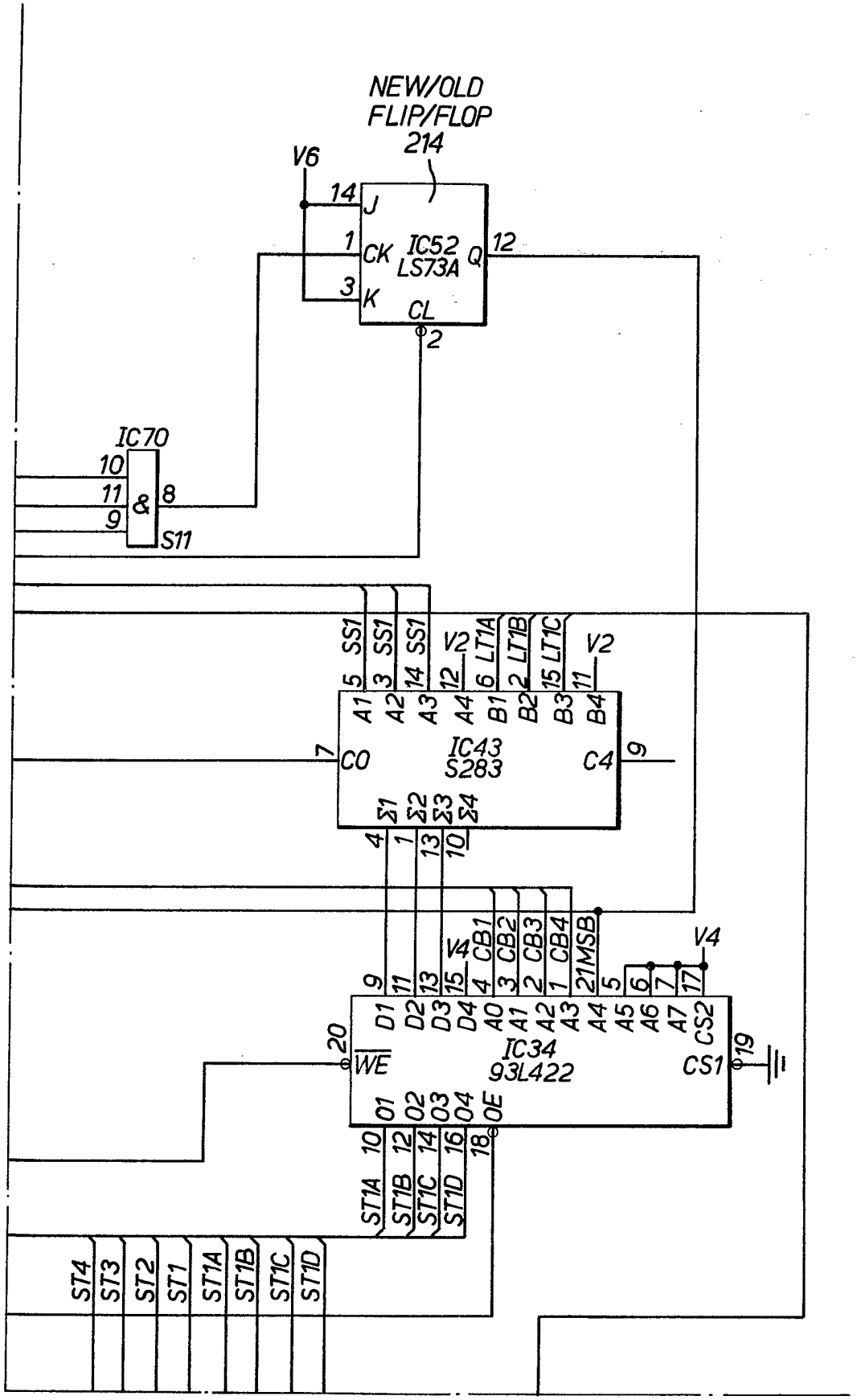

NEW/OLD
FLIP/FLOP
214
V6
14
J
1
CK
IC52
LS73A
Q
12
3
K
CL
2
IC70
10
11
9
&
8
S11
SS1
SS1
SS1
V2
LT1A
LT1B
LT1C
V2
5
3
14
12
6
2
15
11
A1
A2
A3
A4
B1
B2
B3
B4
7
CO
IC43
S283
C4
9
Σ1
Σ2
Σ3
Σ4
4
1
13
10
V4
CB1
CB2
CB3
CB4
21MSB
V4
9
11
13
15
4
3
2
1
21
5
6
7
17
D1
D2
D3
D4
A0
A1
A2
A3
A4
A5
A6
A7
CS2
20
WE
IC34
93L422
CS1
19
O1
O2
O3
O4
OE
10
12
14
16
18
ST1A
ST1B
ST1C
ST1D
ST4
ST3
ST2
ST1
ST1A
ST1B
ST1C
ST1D

FIG. 3G.

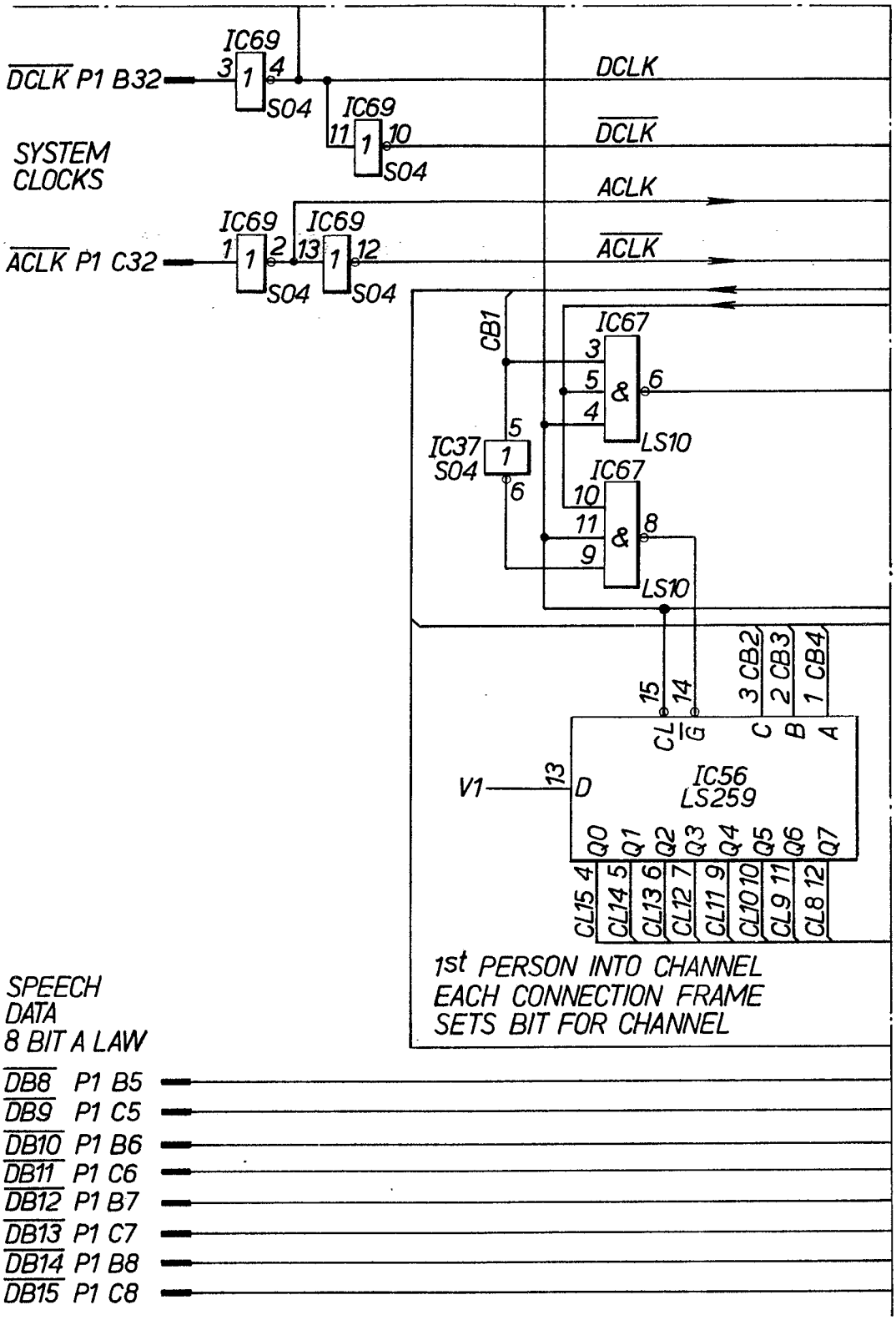

IC69
DCLK P1 B32
3
1
4
S04
IC69
11
1
10
S04
SYSTEM CLOCKS
DCLK
DCLK
ACLK
ACLK
IC69
IC69
ACLK P1 C32
1
1
2
13
1
12
S04
S04
CB1
IC67
3
5
&
6
4
5
IC37
S04
1
6
LS10
IC67
10
11
&
8
9
LS10
15
14
CL
G
3 CB2
2 CB3
1 CB4
C
B
A
V1
13
D
IC56
LS259
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CL15 4
CL14 5
CL13 6
CL12 7
CL11 9
CL10 10
CL9 11
CL8 12
1st PERSON INTO CHANNEL
EACH CONNECTION FRAME
SETS BIT FOR CHANNEL
SPEECH DATA
8 BIT A LAW
DB8 P1 B5
DB9 P1 C5
DB10 P1 B6
DB11 P1 C6
DB12 P1 B7
DB13 P1 C7
DB14 P1 B8
DB15 P1 C8

FIG. 3H.

12/18

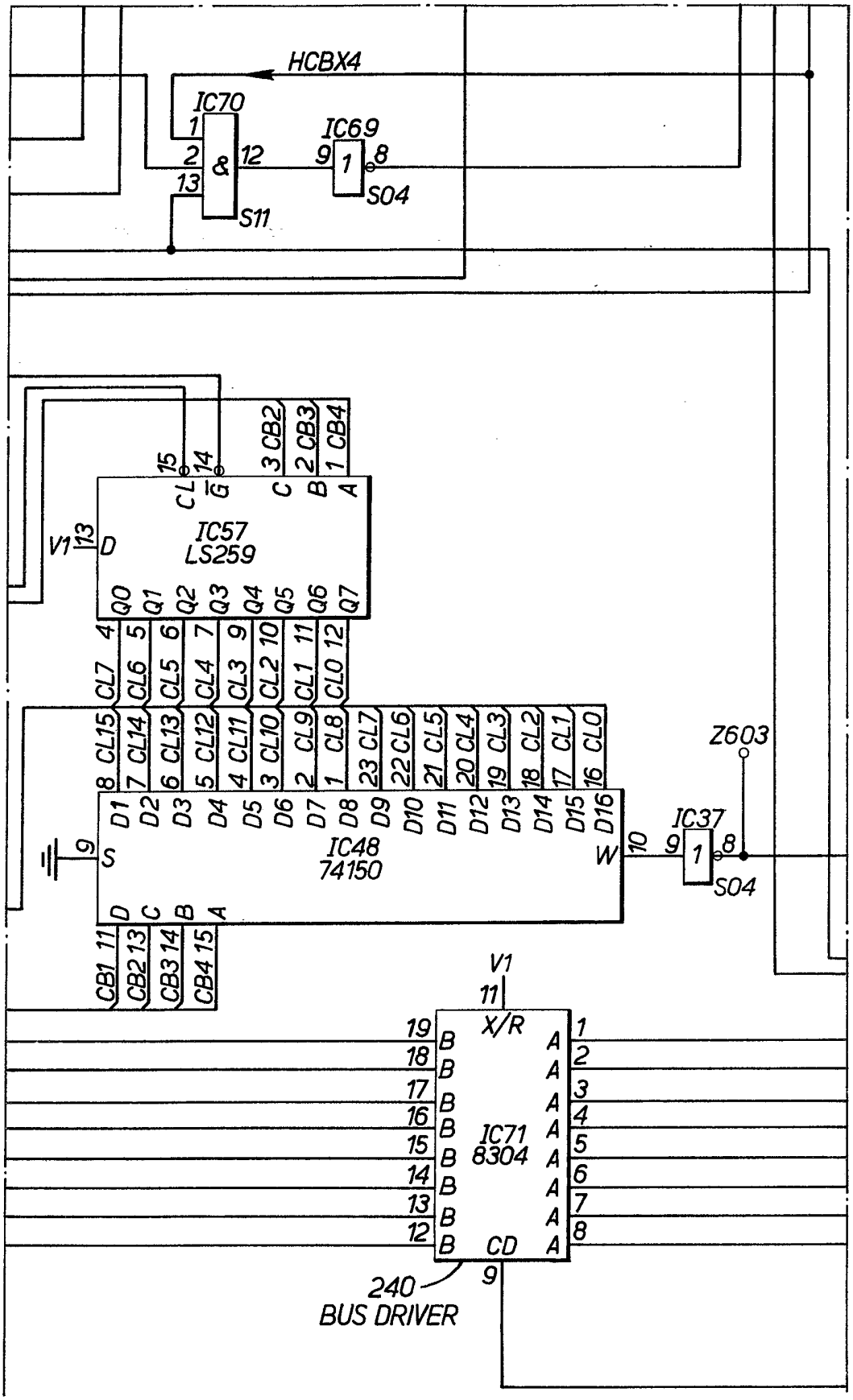

HCBX4
IC70
IC69
S11
S04
IC57
LS259
V1
CL
G
CB2
CB3
CB4
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CL7
CL6
CL5
CL4
CL3
CL2
CL1
CL0
CL15
CL14
CL13
CL12
CL11
CL10
CL9
CL8
CL7
CL6
CL5
CL4
CL3
CL2
CL1
CL0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
IC48
74150
W
Z603
IC37
CB1
CB2
CB3
CB4
V1
X/R
IC71
8304
CD
240
BUS DRIVER

FIG. 31.

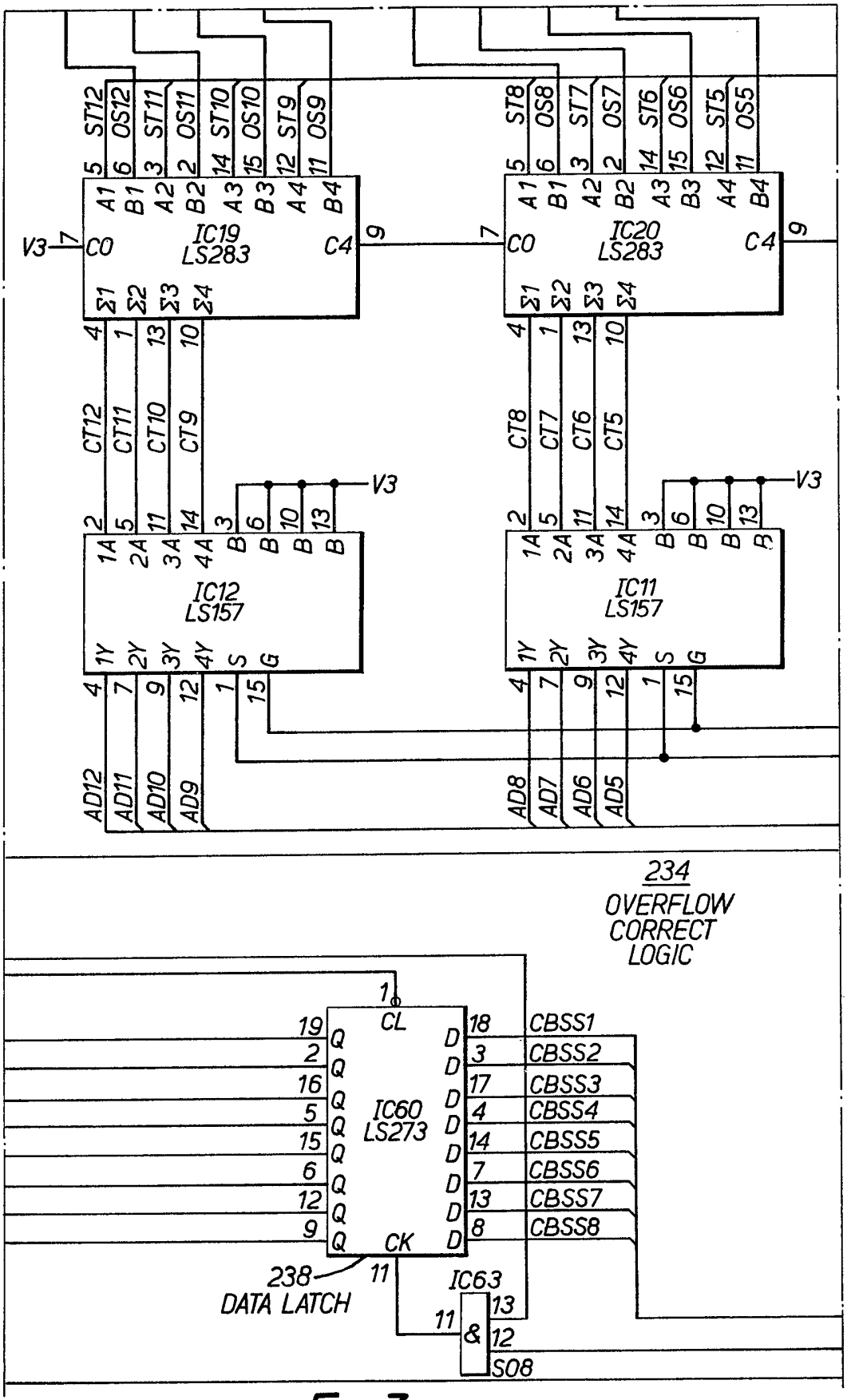

IC19
LS283
IC20
LS283
IC12
LS157
IC11
LS157
IC60
LS273
IC63
V3
234
OVERFLOW
CORRECT
LOGIC
238
DATA LATCH
CBSS1
CBSS2
CBSS3
CBSS4
CBSS5
CBSS6
CBSS7
CBSS8
S08

FIG. 3J.

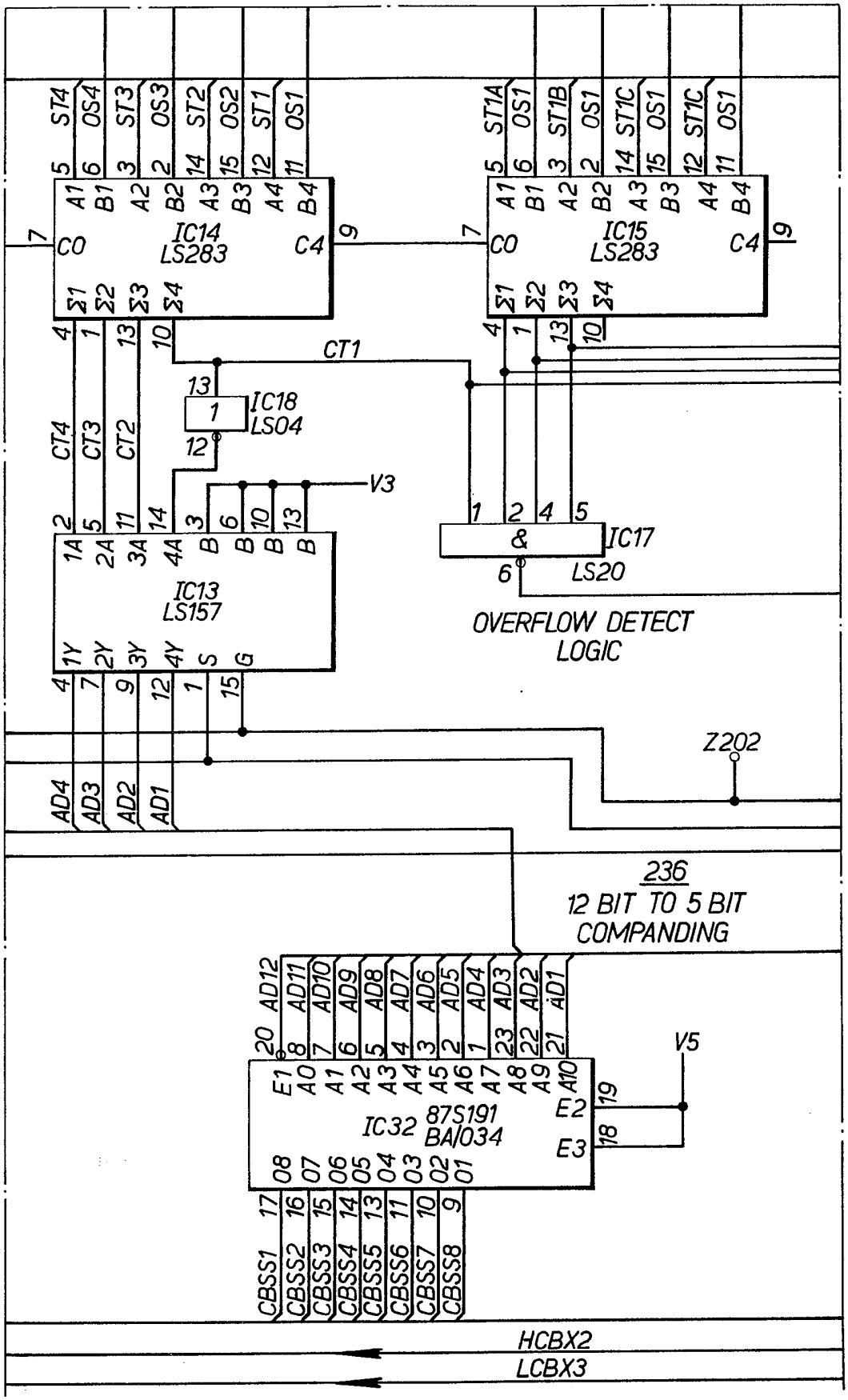

IC14
LS283
IC15
LS283
IC18
LS04
IC13
LS157
IC17
LS20
OVERFLOW DETECT
LOGIC
CT1
V3
Z202
236
12 BIT TO 5 BIT
COMPANDING
IC32 87S191
BA1034
V5
HCBX2
LCBX3

FIG. 3K.

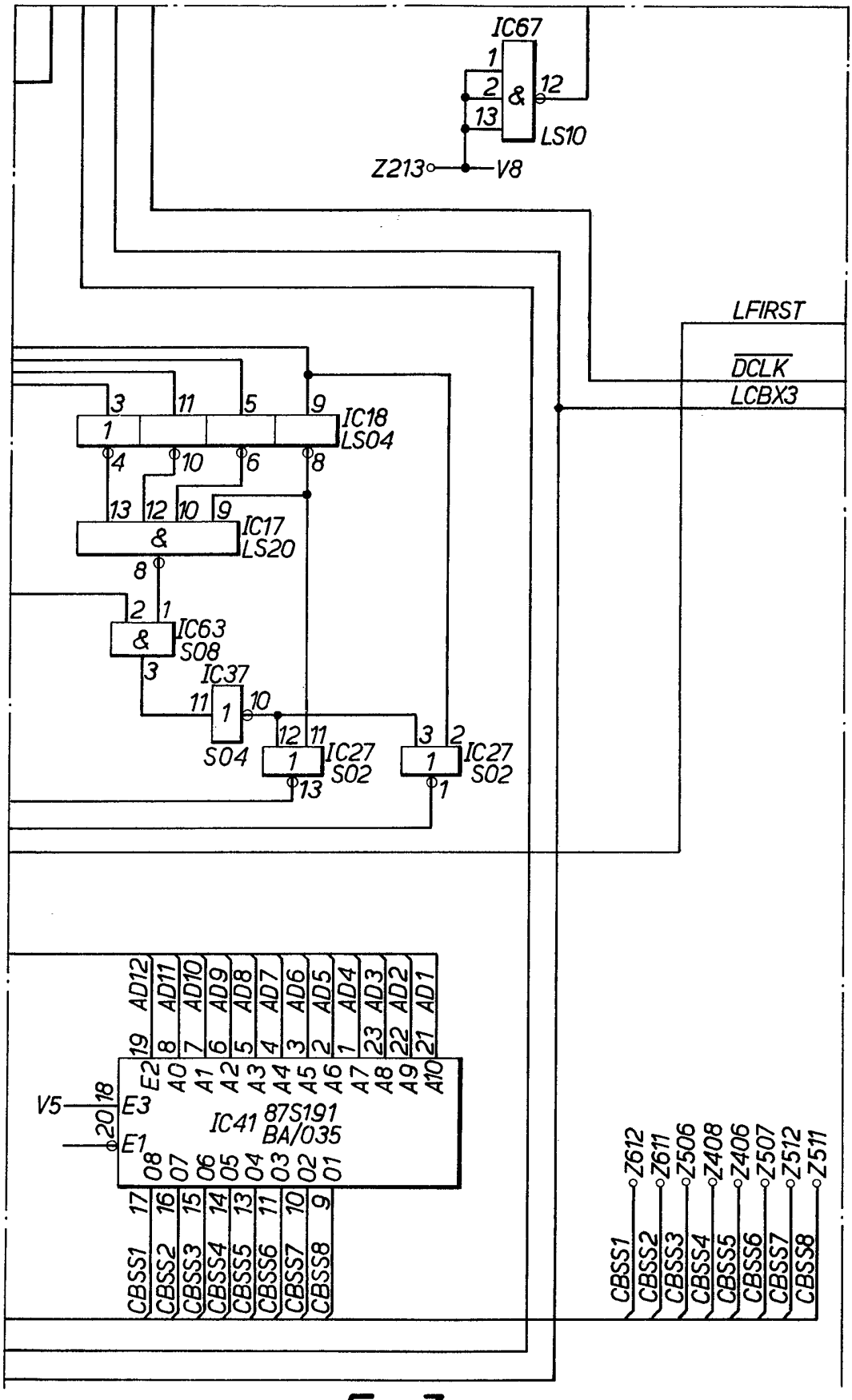

IC67
LS10
Z213
V8
LFIRST
DCLK
LCBX3
IC18
LS04
IC17
LS20
IC63
S08
IC37
S04
IC27
S02
IC27
S02
IC41 87S191
BA/035
V5
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
CBSS1
CBSS2
CBSS3
CBSS4
CBSS5
CBSS6
CBSS7
CBSS8
Z612
Z611
Z506
Z408
Z406
Z507
Z512
Z511

FIG. 3L.

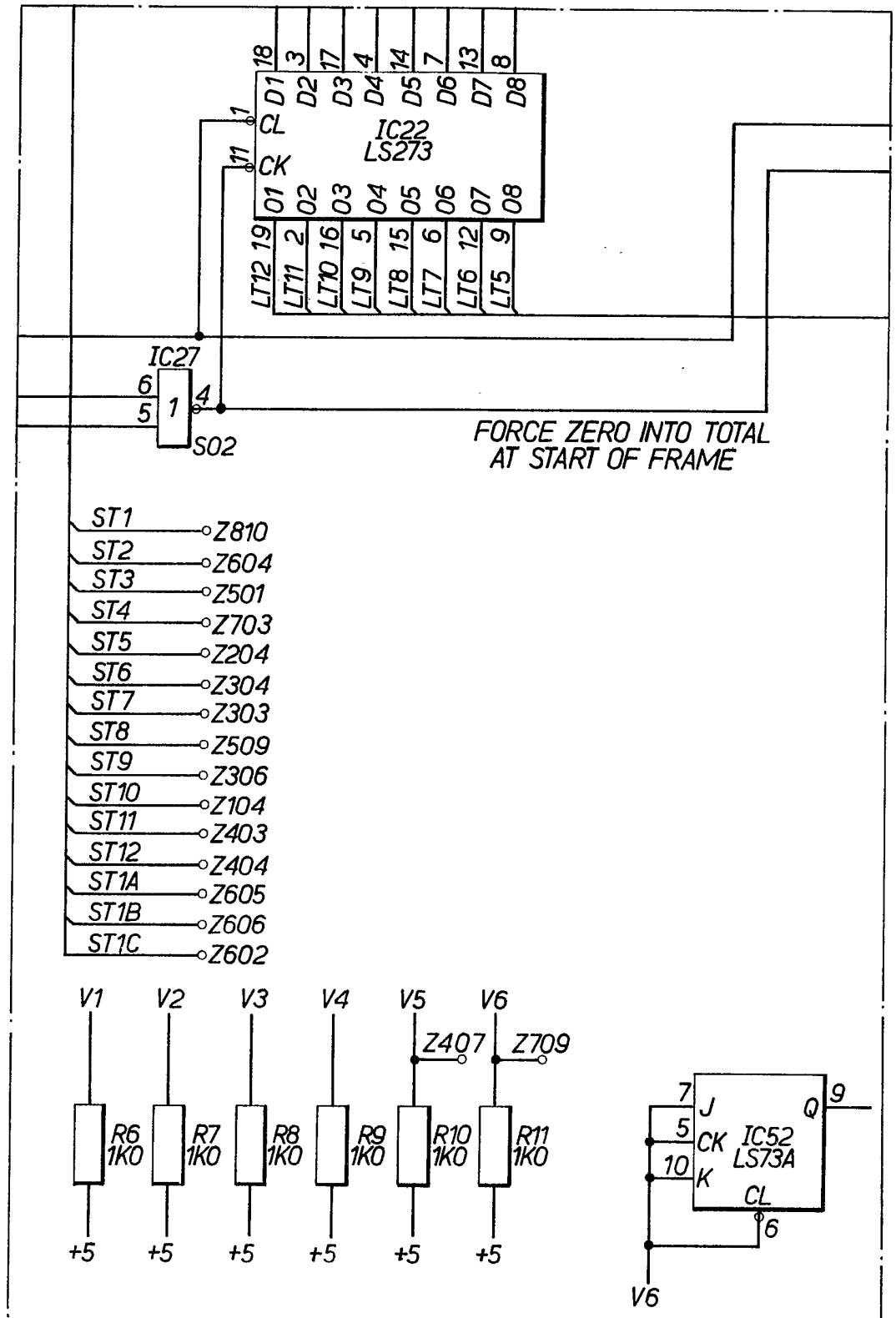

IC22
LS273
CL
CK
D1 D2 D3 D4 D5 D6 D7 D8
O1 O2 O3 O4 O5 O6 O7 O8
LT12 LT11 LT10 LT9 LT8 LT7 LT6 LT5
IC27
S02
FORCE ZERO INTO TOTAL
AT START OF FRAME
ST1 Z810
ST2 Z604
ST3 Z501
ST4 Z703
ST5 Z204
ST6 Z304
ST7 Z303
ST8 Z509
ST9 Z306
ST10 Z104
ST11 Z403
ST12 Z404
ST1A Z605
ST1B Z606
ST1C Z602
V1 V2 V3 V4 V5 V6
Z407 Z709
R6 1K0
R7 1K0
R8 1K0
R9 1K0
R10 1K0
R11 1K0
+5
IC52
LS73A
J CK K CL Q
V6

FIG. 3M.

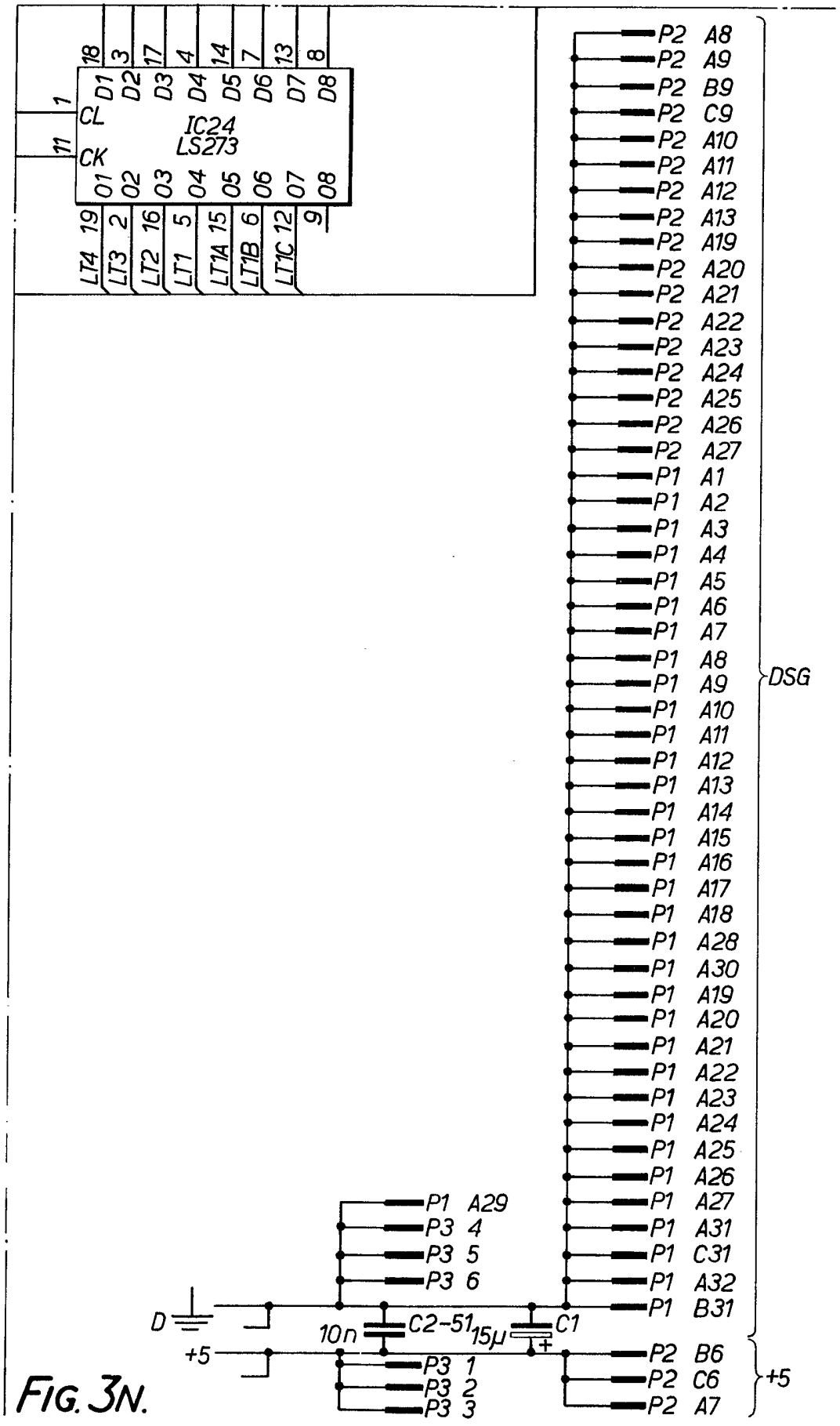

IC24
LS273
CL
CK
D1 D2 D3 D4 D5 D6 D7 D8
O1 O2 O3 O4 O5 O6 O7 O8
LT4 LT3 LT2 LT1 LT1A LT1B LT1C
P2 A8
P2 A9
P2 B9
P2 C9
P2 A10
P2 A11
P2 A12
P2 A13
P2 A19
P2 A20
P2 A21
P2 A22
P2 A23
P2 A24
P2 A25
P2 A26
P2 A27
P1 A1
P1 A2
P1 A3
P1 A4
P1 A5
P1 A6
P1 A7
P1 A8
P1 A9
P1 A10
P1 A11
P1 A12
P1 A13
P1 A14
P1 A15
P1 A16
P1 A17
P1 A18
P1 A28
P1 A30
P1 A19
P1 A20
P1 A21
P1 A22
P1 A23
P1 A24
P1 A25
P1 A26
P1 A27
P1 A31
P1 C31
P1 A32
P1 B31
DSG
P1 A29
P3 4
P3 5
P3 6
D
10n
C2-51
15µ
C1
+5
P3 1
P3 2
P3 3
P2 B6
P2 C6
P2 A7
+5

FIG. 3N.

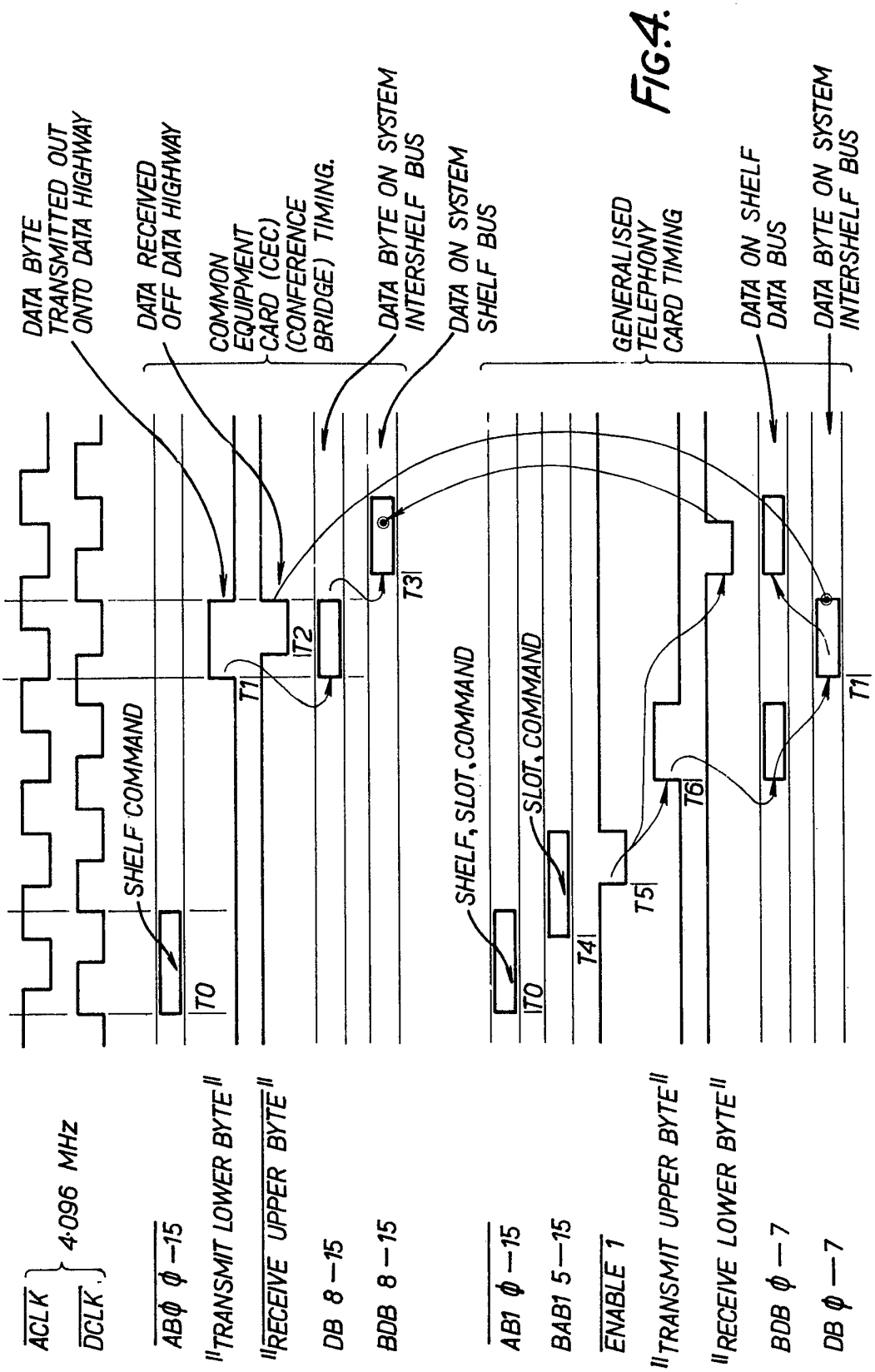

ACLK
DCLK
4·096 MHz
SHELF COMMAND
T0
T1
T2
T3
T4
T5
T6
DATA BYTE TRANSMITTED OUT ONTO DATA HIGHWAY
DATA RECEIVED OFF DATA HIGHWAY
COMMON EQUIPMENT CARD (CEC) (CONFERENCE BRIDGE) TIMING.
DATA BYTE ON SYSTEM INTERSHELF BUS
DATA ON SYSTEM SHELF BUS
GENERALISED TELEPHONY CARD TIMING
DATA ON SHELF DATA BUS
DATA BYTE ON SYSTEM INTERSHELF BUS
ABϕ ϕ –15
"TRANSMIT LOWER BYTE"
"RECEIVE UPPER BYTE"
DB 8–15
BDB 8–15
AB1 ϕ –15
BAB1 5–15
ENABLE 1
"TRANSMIT UPPER BYTE"
"RECEIVE LOWER BYTE"
BDB ϕ –7
DB ϕ –7
SHELF, SLOT, COMMAND
SLOT, COMMAND

FIG.4.

SPECIFICATION

Conference bridge

The present invention relates to conference bridges and more particularly to conference bridges for use in digital time division multiplex PCM telecommunication exchanges. The conference bridge conferences 8 bit PCM data channels.

The conference bridge of the present invention has been designed for use in the electronic switching system as described in our co-pending British Patent Application No: 8323782. The conference bridge can be configured to conference 8 bit PCM voice samples which have been encoded linearly or to A law standards or μ law standards. (All 8KHz sampling rates).

Embodiments of the present invention will now be described, by way of example with reference to the accompanying drawings, in which:—

Figure 1 shows the electronic switching system shown in the above co-pending application and including a conference bridge according to the present invention,.

Figure 2 shows in block diagrammatic form a conference bridge according to the present invention,

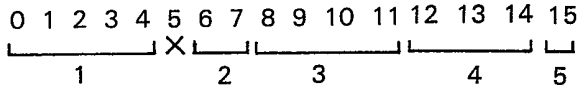
Figure 3 shows the circuit of Figure 2 in greater detail and,

Figure 4 shows an exemplary generalised timing system for a conference bridge of Figure 2.

With reference to Figure 1, the conference bridge 10 is equivalent to a whole shelf and hence has a shelf address within the system of Figure 1. It is addressable by the control computer (not shown) via the TDM network controller 114 and address bus AB0 and data bus DB0. Data is transmitted by the bridge on the lower byte of the bus (bits 8—15) and received on the upper byte (bits 0—7)—see Figure 2.

In the telephone system such as described in our co-pending British Patent Application No: 8323782 the exchange for security has two separate control systems A and B and a conference bridge is allocated to each of the sides as shown. The operation of both bridges is identical.

The Address bus command structure is the form



1) Shelf address
2) Up/down control
3) Conference channel number
4) Conference Party number
5) Transmit only. Function Control. See timing diagram for detailed timings.

Each conference is allocated a unique channel number and each party within a conference a unique party number, the resulting seven bit address thus defines the individual contributions to a conference. This contribution may consist of 8 bit linearly encoded PCM voice or data samples or A law or μm law encoded PCM samples. The remaining bit is sued to enable an operator or other party to listen on a conference without providing contributions to the conference. Thus enabling call monitoring functions to be performed.

The conference bridge provides a two way connection by accumulating speech samples in the present time frame and supplying speech samples from the previous time frame's calculations. The output of the conference bridge in a given time frame is the algebraic sum of the previous frame's samples (for a given conference channel) less the contribution of the party receiving the output. (A time frame is 125 us long in the system described).

The conference bridge must not be addressed more often than once every four time slots each time slot being 144 n sec long. That is if time slot n contains a conference bridge entry then time slots n+1, n+2, n+3 must not contain any conference bridge entry. These connection constraints are needed in order for the conference bridge to receive and transmit data onto the system data bus at the required time. The timing of signals can be seen from Figure 4 in which the upper set of waveforms and time slots CEC represent the timings for the Common Equipment Card—in this case the conference bridge and the lower set of waveforms and time slots represent the timings for examples for the telephony cards which require conference facilities. At time TO a shelf command to operate the conference bridge is transmitted on AB0. At time T1 a data byte is transmitted out onto the parallel data highway and at time T2 after a short delay the data byte is received off the data highway. Also at time T1 a data byte is transmitted on the system intershelf bus on DB0 8—15 and at time T3 data is transmitted on the system shelf bus.

For the telephony card a similar set of timings is required with a shelf slot command being given a time T0 genreating a slot command at time T4 which in turn generates an enable signal at time T5 causing data to be transmitted at time T6 at which time data on shelf data bus DB0 bits 0—7 may be received from the conference bridge. At time T1 the data is present on the intershelf bus.

Thus is may be seen that in a telephone exchange system correct synchronisation is necessary to ensure that data (voice samples) are received by the conference bridge at the correct time and that sufficient time is allowed to enable the conferencing to be carried out prior to the receipt of the conferenced signals by each subscriber associated with a telephony card.

Bits 6 and 7 control the updown function, if the conference bridge has been 'downed' it will ignore any commands sent to it on the address bus.

Bit 6	Bit 7	
0	X	Normal conference bridge usage
1	0	Down command
1	1	Up command

Because the commands sent to the bridge define the conference channel number (up to sixteen 0—15) and the party number in each conference (0—7) uniquely the order of command connections in the connection table does not matter. Thus as each party joins a conference he is merely allocated the next slot in the connection table.

If the speech samples in any conference channel on addition cause overflow to occur then the output is forced to plus or minus full scale.

With reference now to Figure 2 the conference bridge comprises an address header circuit 202 which defines which shelf in the system the conference bridge appears to be. As the bridge occupies a whole shelf only a shelf address is required. The connections within the conference bridge are normally PCM coded signals fed in parallel over paths whose width is indicated by the numerals giving the number of parallel paths.

The output of the address header is connected to a first input of an address comparison circuit 204 which checks to see if the address bus AB0 (0—15) is addressing the conference bridge. The address input from the system address bus AB0 (0—15) is latched into a latch circuit 206. A card enable up/down logic circuit 208 is included to enable the particular conference bridge to be enabled or disabled. In the latter case the alternative (B side) conference bridge will take over.

The up/down logic circuit 208 is connected to enable a timing state logic circuit 210 which controls the reception and transmission timings of data onto and off the system bus.

One output of the timing state logic circuit 210 is fed to a frame logic circuit 212 which controls the switching over at each time frame boundary of the running totals of each conference to give a total for a given time frame.

A second output from the timing state logic circuit 210 is fed to a new frame first party logic circuit 214 which allows a first person into a conference to be written in and then every other party to be added to the conference.

Eight bits of the output of the address latch 206 are fed to an address buffer 216. A first output of buffer 216 is used to identify in the new frame first party logic circuit 214 that a conference is required. A second output is used to initiate a decompanding PROM 218 which converts incoming 8 bit linear, A law or μ law speech samples received from the upper byte of the system data bus DB0 (bits 8—15) via latch 220 into 12 bit linear PCM signals for addition in an adder 222. The adder 222 produces a 15 bit output signal to a totaliser RAM 224 which calculates the total contributions for each conference as controlled by the frame logic circuit 212 and identified by the output from the address buffer 216.

The 15 bit output from adder 222 is necessary to allow the addition of more than one 12 bit number. Each output of the totaliser RAM 224 is fed back to the adder 222 via a latch 226 for addition to the next parties contribution and also to an adder 228.

Each incoming parties contribution is stored in a party RAM 230 which stores each parties contribution in the last time frame. This contribution is accessed when the conference total is output from the totaliser RAM 224 and is subtracted therefrom by inverting it in an inverter 232 and adding the two sums together in adder 228 to give an effective subtraction.

The output of adder 228 is fed to an error detect and correct circuit 234 which detects if the remaining total (which is equal to the sum of all the parties contributions less the addressed party's own contribution) is still greater than the maximum permitted value and if it is it forces full scale output (either positive or negative as required) to avoid any over/under flow to the companding PROM 236 which recompands the now 12 bits linear to A law, μ law or to 8 bits linear. The output of PROM 236 is fed to a latch circuit 238 which stores the finalised PCM sample prior to transmission onto output data bus DB 0—7 via a bus driver 240.

Claims

1. A conference bridge for use in a digital time division multiplex pulse code modulation telecommunication exchange including a party RAM which stores individual party's contributions to a conference and a totaliser RAM which stores the calculated total contributions for each conference, means for subtracting each party's individual contribution to a conference from the calculated total contribution to the conference prior to the individual party receiving the conference total, in which each conference is allocated a unique channel number and each party within a conference is allocated a unique party number thus allowing each party to join a conference in any order.

2. A conference bridge as claimed in claim 1 in which a time slot is allocated in each conference to allow an operator to listen in to a conference without contributing to the conference.

3. A conference bridge as claimed in claim 2 in which each party contributes an 8 bit PCM coded signal to the conference, in which each 8 bit signal is converted to a 12 bit linear PCM signal prior to being added to each other signal in the

conference, in an adder and in which following said addition a 15 bit PCM signal is created to allow for the expanded sum.

4. A conference bridge substantially as described with reference to the accompanying drawings.

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