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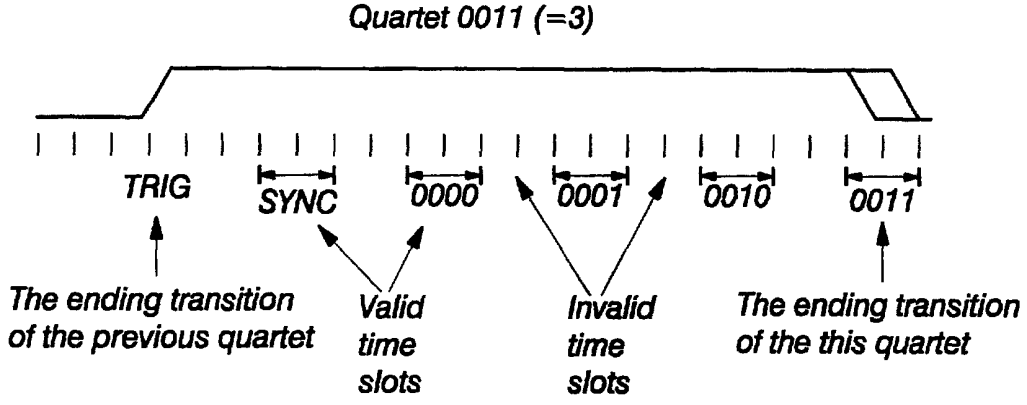
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND SYSTEM FOR DATA TRANSMISSION



(57) Abstract: Method for data transmission via a data bus from a transmitter to a receiver or between several transceivers, the transmitter generating data signal transitions to the transmission bus. The method comprises the steps of modulating the delay between successive transitions; predetermining the number of bits to be represented by each modulated delay; using the desired binary value of each predetermined number of bits to adjust the modulated delay; and measuring by the receiver the modulated delays between the successive transitions and converting each modulated delay back to the original binary value data on the basis of the measured time of the modulated delay. Each modulated delay may be predetermined to represent four data bits, i.e. a bit quartet.

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Method and system for data transmission

The present invention relates to a method and system for data transmission via a data bus from a transmitter to a receiver or between several transceivers, the transmitter generating data signal transitions to the transmission bus.

The present invention can be applied instead of any traditional data transmission protocol, such as CAN-protocol, in Intelligent Wiring Systems (IWS) for vehicles, such as described in the applicants patent applications WO 99/25585, WO 99/25586, WO 99/26331, WO 95/15594, WO 97/4901 and PCT/FI98/00710. Of course, the invention can be applied also in intelligent wiring systems for building automation in homes and offices.

In the prior art methods and systems a number of successive signal states "1" or "0" is used to represent the desired binary value data. The ordinary bit-wise transfer of data messages is sensitive to EMI-interference which is one of the main problems in implementations of data transmission systems for automotive industry. Another problem is overcrowded data bus when data collision must be prevented in a system wherein several tens of intelligent load supply terminals (intelligent nodes) must communicate with each other and/or with a central control unit via a data bus.

It is prior known from patent specification US-4,429,384 a communication system for the transmission of digital information over a bus channel using pulses having a considerably different pulse length for the transmission of "0" and "1" bits, respectively. In this prior art the message is based also on successive signal states "1" and "0" to be separated from each other and therefore this system suffers from the same problems as described above.

The object of the present invention is to achieve an improved method for data transmission such that the above mentioned problems can be substantially reduced.

This object can be achieved by a method according to the features of claim 1. The object can also be achieved by a system according to the features of claim 14.

In the following the preferred embodiments of the invention will be illustrated in more detail by reference to the enclosed drawings wherein

Fig. 1 shows an example of a data bit quartet composed transferred by the method of modulating the time delay between successive transitions;

Fig. 2 shows an example of a message sent by several data bit quartets in packet format, each bit quartet being composed according to the principle of Fig. 1;

Fig. 3 shows an example of a part of an Intelligent wiring system (IWS) wherein the new method for data transmission can be advantageously applied.

Fig. 4 shows an example of a message composed of several transition delay modulated bit quartets according to the principle of Fig. 1, the message being planned to be applied in the system part according to Fig. 3.

Fig. 5 shows an example of a driver unit (transceiver) operating under the new IWS protocol.

Physical media and device (Fig. 3 and Fig. 5)

- Unshielded, floating, differential two wire mixed topology data transmission cable without termination
- Master junction unit with an independent line condition supervisory circuit for both data wires.

- Slew rate limited push-pull complementary output transmitters with high impedance state
- Differential analog receivers with anti alias filter and window discriminator
- Digital signal conditioner for received analog signal

At the end of the specification the transceiver device is explained in more detail with reference to Fig. 5.

Modulation method (Fig. 1)

IWS data transfer is based on pulse width modulation of bit quartets. Each quartet contains or represents four data bits. The binary value of each quartet is used to adjust the delay between successive output transitions. A receiver measures delays between transitions and converts them back to the original data.

This modulation method generates less transitions and less EMI-interference than ordinary bit-wise transfer methods when sending random data at the same average bit rate, because every transition in signal path can transfer one quartet (four bits) of data.

Transitions (Figures 1, 2 and 4)

The modulation method depends on signal transitions instead of signal states. There is no high / low or dominant / recessive states or bits as needed for prior data transportation implementations for automotive industry. A transition in the IWS (Intelligent Wiring System) cable is signaled by complementing the electric charge of signal wires and then leaving the new state of electric charge passively or using only a weak output driver to maintain the signal state in the cable.

Synchronization (Figures 1, 2 and 4)

A special synchronization pattern is used to find the start and the end of each data frame. The synchronization pattern contains two successive transitions. The time delay between synchronization transitions is one transmit clock cycle. Because all other quartets and heart beat signals have longer delay between transitions no transmitted signal can interfere with the synchronization signal. This signal is possible to insert and detect at any time during the data transfer. Every synchronization pattern starts a new data frame reception.

Supervisory

When no data transmission is needed, the charge of signal wires is refreshed by a special heartbeat signal. Every unit is responsible for generating the heartbeat signal at specified periods.

The heartbeat signal is also used for detecting the condition of the transmission line. If, for some reason, the heart beat signal does not work in proper way the supervisory system can immediately alert the user about the damage and change the data transmission protocol into emergency mode.

In the emergency mode the transmission speed is slower and data transmitters does not work in complementary mode as normally. Transitions in emergency mode are energy pulses instead of alternating charges.

The master junction unit disconnects all data lines which can not generate proper heartbeat signals to get the rest of the system to working condition. All supervisory elements are doubled independently. Every single data cable fault will be detected and corrected without major functional disadvantages.

Collision prevention

If two (or more) transmitters decide to send a transition exactly at the same or

almost at the same time, the result will always be a single transition because both transmitters set the same new electric charge to the signal cable to generate a new and exactly same type of transition.

A transmitter is not allowed to send a new transition immediately after detection of a new transition. This safeguard delay prevents the possibility that two or more transmitters could simultaneously set different charges to the signal cable and cause a true collision situation.

Due to presented method there is no possibility for collision of two or more transmitters. Instead, every transmitter have an opportunity to send new transitions without a risk of signal contamination to unpredictable state.

Bus arbitration

Any transmitter can start transmitting when it detects the synchronization signal. In the case, that there is no active transmissions running, the transmitter can start transmitting of a new synchronization signal itself.
When an active transmitter detects at any time an extra transition in the signal cable, it should stop transmission immediately. This happens normally during the first quartets of the data packet. The transmitter, which have shorter quartet, sends the transition of the quartet earlier than transmitters with a longer message. The transmitter with the shorter message quartet can continue without interruption and the transmitter with the longer message quartet gives up. The extra transition situation may also happen when a very high priority transmitter breaks a transmission of a low priority transmitter by sending a new synchronization pattern in the middle of the low priority data frame.

Transmit signal timing (Fig. 1)

Transmit signal timing is depending on chosen transmit clock frequency. This frequency sets the step value for transmitter delay unit. The shortest delay of one transmit clock is reserved for the synchronization signal. Multiple of trans-

mit clock cycles are used to send transitions for data quartets. Two cycles are used for the first binary data value 0000 (=0) and three cycles are used for the next binary data value 0001 (=1)... Finally 17 transmit clock cycles delay before the ending transition of the quartet is used for the largest binary data value 1111 (=15). Any longer delay between transitions means heart beat and bus idle state.

Receive signal timing

The receiver uses a receive clock frequency which is a multiple of the transmit signal frequency. This allows the receiver to measure the delay between transitions more precisely and to perform a digital signal conditioning before actual reception of the transition event.

After a reception of a transition, the receiver evaluates the time delay value measured from the last successive transition and decides how to translate the received time information. Only narrow time windows are allowed for possible data quartets. Between allowed signal width windows there is a fail safe areas for detecting incorrect random transitions. If the measured delay value is not belonged to any allowed signal windows, it is discarded by the receiver. This procedure prevents efficiently a random signal pattern to be accidentally received as a valid data packet.

If a receiver detects an illegal transition when it is actively receiving a message, it may generate an extra synchronization signal to break this transmission and to start the retransmission immediately.

IWS message format (Figures 2 and 4)

All messages have same basic format. 32 data bits delivered either to all receivers or to a single receiver with an acknowledge. All unused bit space (zero value quartets) will be spontaneously optimized to the shortest length during the modulation.

A message contains following parts:

- Synchronization from the transmitting unit
- Priority selection field
- Data field (8/32 bits)
- Error check field
- Synchronization from the transmitting unit
- Acknowledge field
- Synchronization from the receiving unit

Priority selection field (Figures 2 and 4)

This part of the message starts from the synchronization signal of the previous message or a new synchronization signal generated by the transmitter itself. All active transmitters may then start transmitting of message priority selection quartet. Possible values for the priority quartet are from 1 to 15. Zero value is reserved for acknowledge field. Many transmitters may have the same message priority. All transmitters start sending of their messages simultaneously. During the transmission any transmitter trying to send a longer message quartet than others will be efficiently eliminated due to collision prevention mechanism. At the end of the packet only one transmitter should be actively transmitting.

In the special case that more than one message have exactly the same ad dress and data fields then all these messages will be properly delivered at the same time.

Target address field (Figures 2 and 4)

This part of the message contains two quartets which uniquely selects the receiver for the message. If both target quartets have zero value then every receiver should receive a broadcast message. All receivers must have an unique pair of address quartets. This limits the maximum number of receivers to 255 units leaving one address for the broadcast.

Data field (Figures 1, 2 and 4)

This part of the message contains eight quartets used for actual data. Maximum data bits in one message packet is 32-bits. Unused space will be spontaneously optimized to the shortest length during the modulation.

Error check code field (Figures 2 and 4)

This part of the message contains two quartets representing a 8-bit ECC value calculated from the target address field and the data field. The error check can detect unusual errors passed from other error checking procedures.

Acknowledge field (Figures 2 and 4)

This part of the message contains three quartets followed by a synchronization pattern sent by the receiver of the message. The first quartet is zero and next two quartets contains the address of the acknowledging receiver.

If any of these transitions are missing the transmitter should immediately send a new synchronization signal to restart transmitting of the message. If no correct acknowledge has received after three retries the transmitter should delay the message and try again later. Messages which are addressed to every receiver are not acknowledged.

Error checking

Quality of the received signal timing is checked during the reception. This quality detection is important to prevent a random noise signal to be recognized to a valid message. No error checking methods used for short messages is reliable enough to withstand a pure random signal without the signal quality check.

When transmitting a message the transmitter compares the transmitted signal to received signal. If there is any difference between those two signals the transmitter stops sending the message before it will be received.

When receiving a message the receiver checks the ECC code from the end of the data packet to confirm that the contents is logically correct and not messed up during the transmission.

All these precautions are made to confirm that no message could be acciden tally recognized in wrong way due to noise or interference in the IWS cabling.

In the case that some special signal needs a very special care for error detection the signal can be selected to contain a bit pattern which is not near to any other used bit pattern. This way the probability of accidental reception of this specially selected signal is highly decreased.

Example of system for application the method

The system according to Fig. 3 includes IWS (Intelligent Wiring System) cable which includes two wires for power supply and two wires for data bus. There may be several cable branches, each starting from a master junction unit, which is optional and may be replaced by a ring cable for connecting the cable branches with each other. The block of master junction units is in data communication with adaptation and monitoring block, through which any external programming of the system can be made, which monitors the "heart beat" and fault messages from the system and which controls the on-line display to show the use the status of the system. Each cable branch has been provided by several intelligent sockets, which control the power supply from the IWS-cable to various loads, such as trunk light L1, in response to various inputs, such as closing the trunk hatch switch S1, from any socket of the system. The number of sockets in the whole system for vehicle implementation, for instance, is typically between 30-50, but may vary substantially depending on the application (e.g. in busses, ships, homes and offices).

The operation of system part of Fig. 3 takes place in view of Fig. 4 according to following steps:

- Trunk hatch opens and closes the trunk light switch S1
- Input pin I1 connects to the ground and wakes up the CPU of socket 11
- Socket 11 starts evaluating the new input signal using the virtual schematics of the vehicle stored in the flash memory of the socket
- Socket 11 founds that it does not have all information about the wiring of this signal number 51
- Socket 11 sends a priority class 4 message to socket 10 about virtual connection number 51 which has changed to 1 (unused data fields are 00000)
- Socket 10 receives the message and checks the error check code 5220
- Socket 10 acknowledges by inserting an OK message after successful receiving of the message from socket 11
- Socket 10 starts evaluating the new input message using the virtual schematics of the vehicle stored in the flash memory of the socket
- Socket 10 founds that the signal 51 goes to output pin O1 and activates it
- Finally the trunk light switches on.

Transceiver device according to Fig. 5

The contents and/or tasks of the transceiver blocks A-L are as follows:

A Transmit line driver contains a complementary slew rate limited push pull type line driver

B Pulse width modulator converts binary quartets to delayed transitions

C Bus arbitration detector stops the transmitter when the bus arbitration has lost

D Transmit control logic contains a state machine which controls all transmit logic units

E IDLE delay detector detects long delays needed for the heart beat generation

F Short edge filter utilizes 2 µs delay line to remove signal noise

G Sync signal detector restarts both transmit and receive logic when new sync is detected

H CRC control logic is used for error detection calculations during transmit and receive

I Receive line driver contains a differential low pass filterering amplifier and a Schmitt trigger

J Long edge filter utilizes 4 µS delay line to remove signal noise

K Pulse width demodulator converts delayed transitions back to binary quartets

L Receive control logic contains a state machine which controls all receive logic units.

Claims

1. A method for data transmission via a data bus from a transmitter to a receiver or between several transceivers, the transmitter generating data signal transitions to the transmission bus, **characterized** by the steps of

- modulating the delay between successive transitions;
- predetermining the number of bits to be represented by each modulated delay;
- using the desired binary value of each predetermined number of bits to adjust the modulated delay; and
- measuring by the receiver the modulated delays between the successive transitions and converting each modulated delay back to the original binary value data on the basis of the measured time of the modulated delay.

2. A method according to claim 1, **characterized** in that each modulated delay is predetermined to represent four data bits, i.e. a bit quartet.

3. A method according to claim 1 or 2, **characterized** in that a data packet composed of several modulated delays is preceded and followed by a predetermined short duration time delay between two synchronization transitions used to find the start and the end of each data packet, whereby one of the transitions of the two synchronization transitions is either the starting or the ending transition of the data packet.

4. A method according to claim 3, **characterized** in that the time delay between two synchronization transitions is shorter than any modulated delay.

5. A method according to any of the claims 1-4, the transitions being generated by applying different stages of charge on the data bus, **characterized** in that the charge of the data bus signal wires is refreshed by a "heart beat" signal when no data transmission is needed, the time delay between transitions of the "heart beat" signal being longer than a modulated delay used for the largest

binary data.

6. A method according to any of the claims 1-5, **characterized** in that the modulated delay contains valid time slots and invalid time slots in respect of appearance of the ending transition of the modulated delay.

7. A method according to claim 3, **characterized** in that the first modulated delay within the data packet defined between the two pairs of synchronization transitions is determined to represent the priority level of the data packet.

8. A method according to any of claims 1-7, **characterized** in that two of the modulated delays are determined to represent an address of a target receiver.

9. A method according to any of claims 1-3, **characterized** in that the receiver uses a receive clock frequency which is a multiple of the transmit signal frequency, which sets a step value for the modulated delay.

10. A method according to any of claims 1-9, **characterized** in that after the synchronization transitions for ending the transmission, a receiver sends an acknowledge field including a first transition with a predetermined delay after the synchronization transition, and a second and a third transition having their delays adjusted to correspond to the address of the acknowledging receiver.

11. A method according to any of claims 1-10, **characterized** in that each data package is ended by an error checking code (ECC) composed of at least two transition delays of predetermined lengths.

12. A method according to any of claims 1-11, **characterized** in that each transmitter, when transmitting the signal, compares the transmitted signal to received signal and stops sending the message if there is any difference between those two signals.

13. A method according to any of claim 12, **characterized** in that any

transmitter can start transmitting when it detects a synchronization signal sent by any transmitter, including a synchronization signal transmitted by itself, and two or several transmitters can continue simultaneous transmission as far as any of the two or several transmitters detects an extra transition not sent by the transmitter itself, whereby the latter transmitter, having detected the extra transition, stops transmitting and one or more transmitters with a shorter modulated delay continue transmitting without interruption until only one transmitter with shortest modulated delays is transmitting.

14. A system for data transmission via a data bus from a transmitter to a receiver or between several transceivers, the transmitter generating data signal transitions to the transmission bus, the system including a cable with at least one wire for power supply and at least one wire for the data bus, and several intelligent sockets (10, 11) connected to the wires of the cable, each intelligent socket including a transmitter and a receiver for the data transmission between the intelligent sockets, **characterized** in that the transmitting sockets are arranged to modulate the delay between successive transitions of the data signal in response to desired binary value of the modulated delay and the receiving sockets are arranged to measure the modulated delays of the received signal and to convert each modulated delay back to the original binary value data on the basis of the measured time of the modulated delay.

15. A system according to claim 14, **characterized** in that any socket is simultaneously transmitting and receiving and immediately stops transmitting if it detects a transition which is not transmitted by itself.

16. A system according to claim 15, **characterized** in that any transmitter is allowed to start transmitting when it detects a synchronization signal sent by any transmitter, including a synchronization signal transmitted by itself, and two or several transmitters can continue simultaneous transmission as far as any of the two or several transmitters detects an extra transition not sent by the transmitter itself, whereby the latter transmitter, having detected the extra

transition, stops transmitting and one or more transmitters with a shorter modulated delay continue transmitting without interruption until only one transmitter with shortest modulated delays is transmitting.

17. A system according to claim 15 or 16, **characterized** in that a synchronization pulse with a predetermined length is used to cut off a pending transmission of a message.

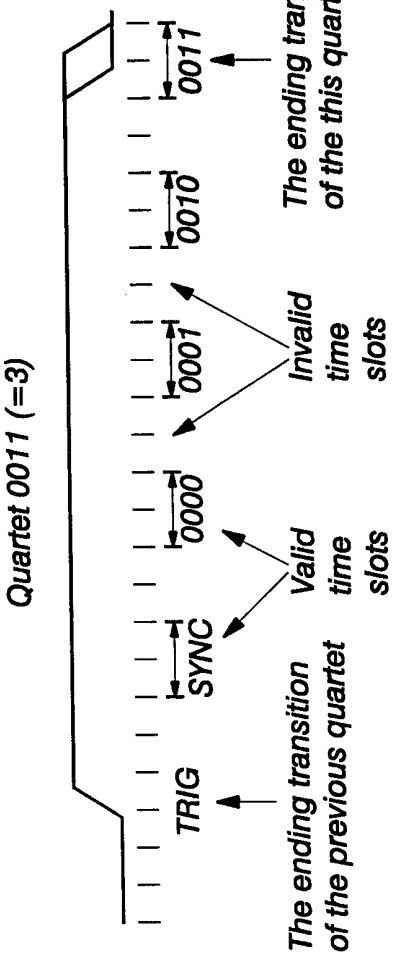

Quartet 0011 (=3)
TRIG
SYNC
0000
0001
0010
0011
Valid time slots
Invalid time slots
The ending transition of the previous quartet
The ending transition of the this quartet

Fig.1

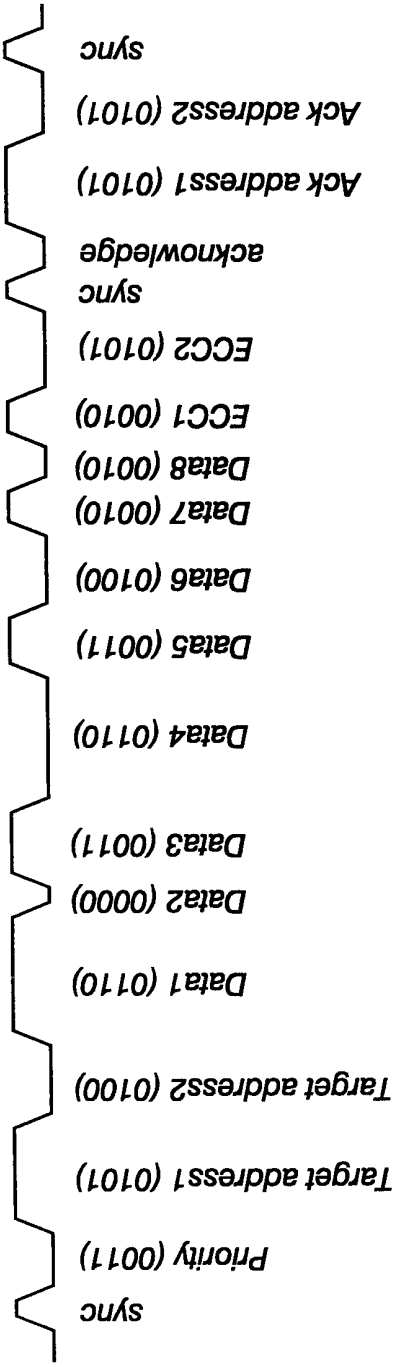

sync
Priority (0011)
Target address1 (0101)
Target address2 (0100)
Data1 (0110)
Data2 (0000)
Data3 (0011)
Data4 (0110)
Data5 (0011)
Data6 (0100)
Data7 (0010)
Data8 (0010)
ECC1 (0010)
ECC2 (0101)
sync
acknowledge
Ack address1 (0101)
Ack address2 (0101)
sync

Fig.2

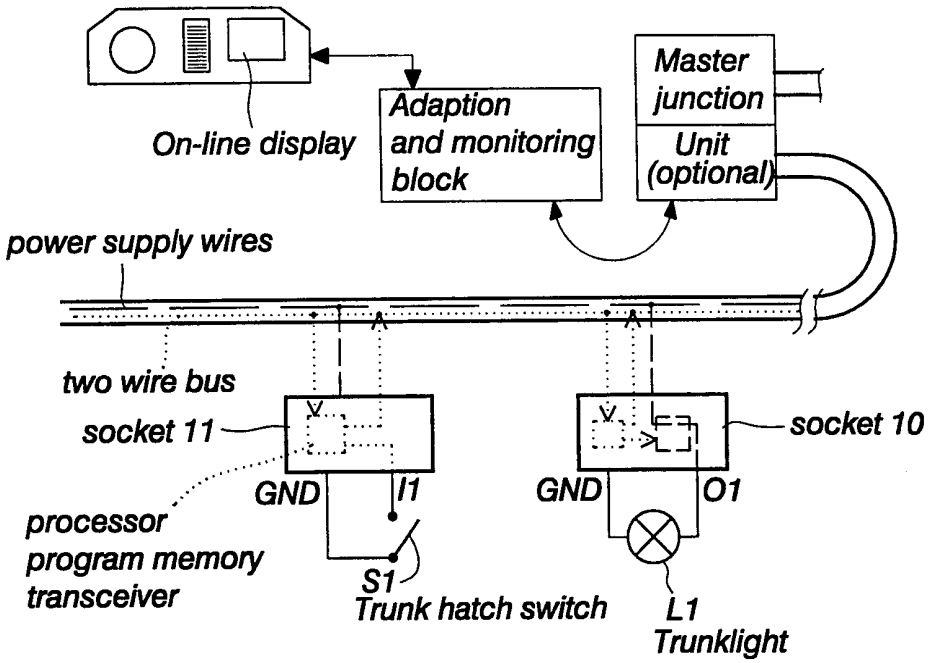

On-line display
Adaption and monitoring block
Master junction Unit (optional)
power supply wires
two wire bus
socket 11
socket 10
GND
I1
GND
O1
processor program memory transceiver
S1
Trunk hatch switch
L1
Trunklight

Fig.3

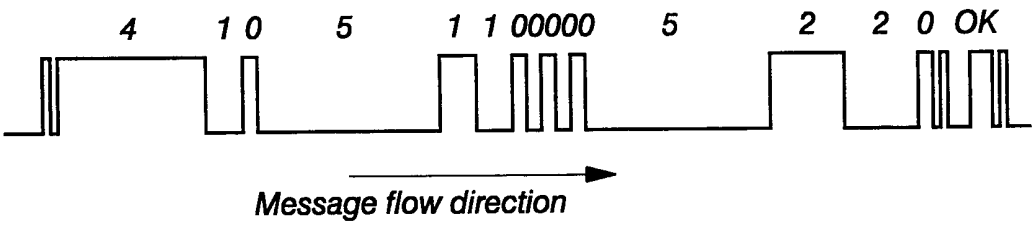
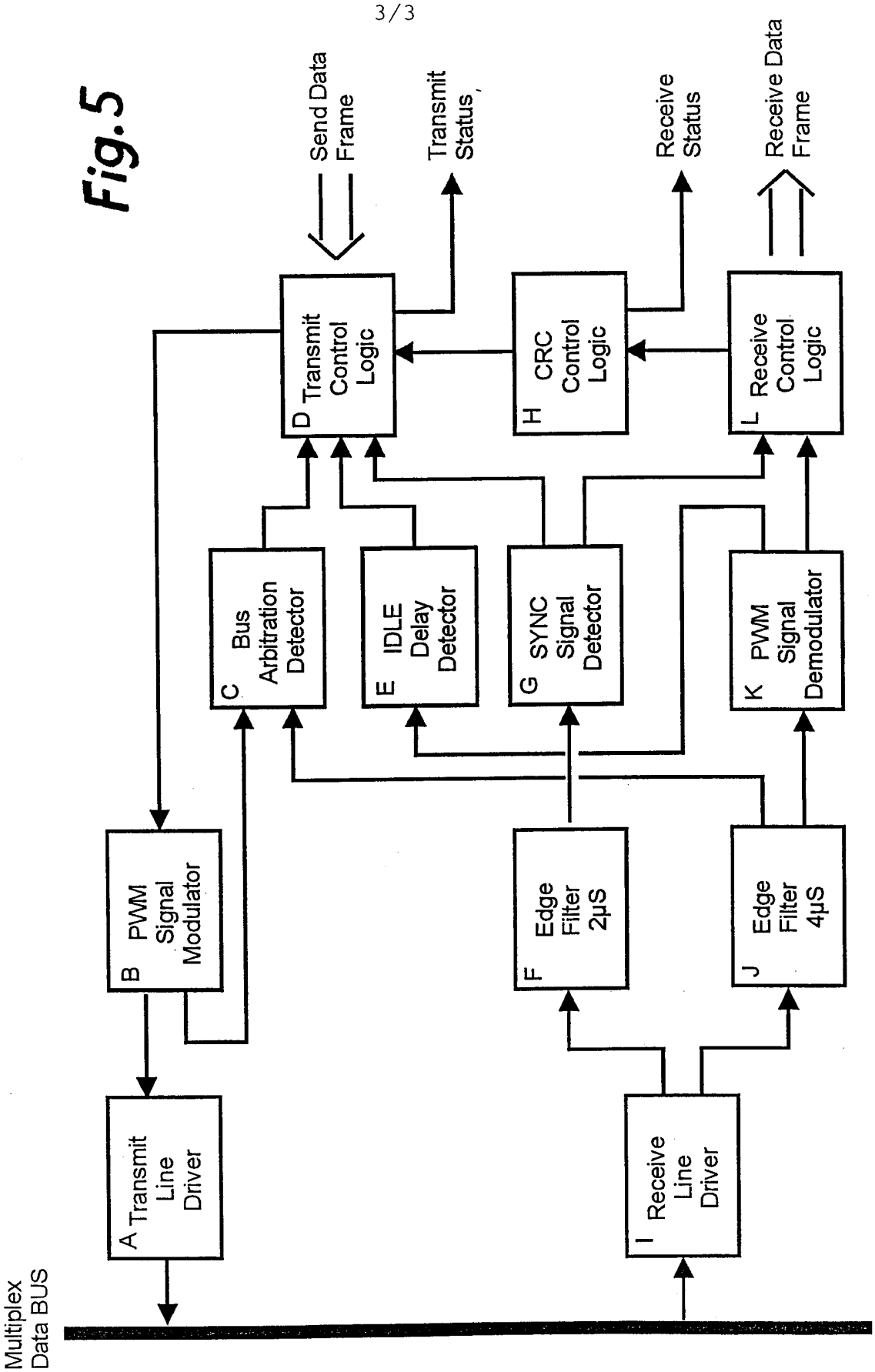

4
1 0
5
1 1 00000
5
2
2 0 OK
Message flow direction

Fig.4

Fig.5


Send Data Frame
Transmit Status
Receive Status
Receive Data Frame
D Transmit Control Logic
H CRC Control Logic
L Receive Control Logic
C Bus Arbitration Detector
E IDLE Delay Detector
G SYNC Signal Detector
K PWM Signal Demodulator
B PWM Signal Modulator
F Edge Filter 2µS
J Edge Filter 4µS
A Transmit Line Driver
I Receive Line Driver
Multiplex Data BUS

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 00/00725

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H03K 7/08, G06F 13/38
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H03K, G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5588023 A (K.-F. HO), 24 December 1996 (24.12.96), column 1, line 35 - column 2, line 26; column 6, line 28 - column 7, line 12; column 28, line 64 - column 29, line 63	1-11,14
Y	--	12-13,15-17
Y	US 5363405 A (R. HORMEL), 8 November 1994 (08.11.94), column 6, line 29 - column 7, line 2, figures 3A-3F	12-13,15-17
	--	
A	US 5303348 A (W. BOTZENHARDT ET AL), 12 April 1994 (12.04.94), column 9, line 37 - column 12, line 40, abstract	3,4,7,8, 10-11
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2000	21 -12- 2000
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Erik Veillas/LR Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 00/00725

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5140611 A (B. JONES ET AL), 18 August 1992 (18.08.92), column 2, line 34 - column 3, line 52	3-4
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A	US 5751770 A (H. TATARA), 12 May 1998 (12.05.98), column 1, line 1 - line 33, figure 5, abstract	7
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A	US 5640160 A (K. MIWA), 17 June 1997 (17.06.97), column 3, line 4 - line 40; column 4, line 45 - column 5, line 4; column 5, line 59 - column 6, line 8	1
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INTERNATIONAL SEARCH REPORT

Information on patent family members

04/12/00

International application No.
PCT/FI 00/00725

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		US 4809299 A	28/02/89
		US 4972435 A	20/11/90
US 5363405 A	08/11/94	NONE	
US 5303348 A	12/04/94	DE 3506118 A,C	28/08/86
		DE 3546662 C,R	07/03/91
		DE 3546664 C,R	07/03/91
		DE 3546683 C	07/03/91
		DE 3546684 C	07/03/91
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		JP 1989253 C	08/11/95
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