(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 March 2007 (15.03.2007)

PCT

(10) International Publication Number
WO 2007/029051 A1

(51) **International Patent Classification:**
G06F 17/50 (2006.01)

(21) **International Application Number:** PCT/IB2005/052912

(22) **International Filing Date:** 7 September 2005 (07.09.2005)

(25) **Filing Language:** English

(26) **Publication Language:** English

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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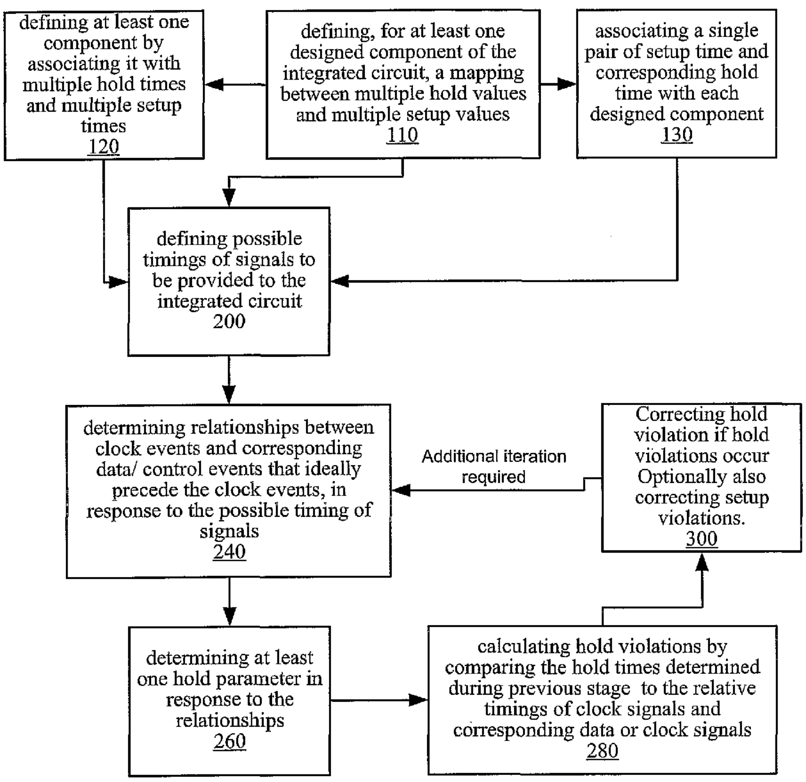
(54) **Title:** METHOD AND A COMPUTER READABLE MEDIUM FOR ANALYZING A DESIGN OF AN INTEGRATED CIRCUIT



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(57) Abstract: A method (100) for analyzing an design of an integrated circuit, the method includes defining (200) possible timings of signals to be provided to the integrated circuit and calculating (280) hold violations; characterized by including a stage of determining (240) relationships between clock events and corresponding data/control events that ideally precede the clock events, in response to the possible timing of signals; and determining (260) hold parameters in response to the relationships. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to define at least one internal delay of a designed component, characterized by causing the processor to define a cell that is characterized by multiple hold times and multiple setup values for a certain clock skew value.

WO 2007/029051 A1

Published:
— *with international search report*
— *with amended claims*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

METHOD AND A COMPUTER READABLE MEDIUM FOR ANALYZING A DESIGN OF AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The present invention relates to a method and a computer readable medium for analyzing a design of an integrated circuit and especially for static timing analysis.

BACKGROUND OF THE INVENTION

Modern integrated circuits include a very large amount of logic circuits such as flip flops, logic gates and the like. The design process is relatively long and includes multiple stages such as high level description, synthesis, placement and routing, extraction, static timing analysis and the like.

Various vendors provide software tools capable of performing static timing analysis. These tools include, for example, Quartus® II of Altera™, of California U.S.A.; Timer™ of Actel™ of California, U.S.A., and PathMill® and PrimeTime™ of Synopsys™ of California, U.S.A.

Various verification and re-design stages are required before the design process is completed. Typically, the synthesis is responsive to design constraints (including timing constraints) and to the characteristics of designed components. The characteristics of multiple designed components are usually gathered in a cell library. Various vendors offer standard cell libraries, including Libra-Visa of Synopsys.

The following U.S. patent applications, all being incorporated herein by reference, illustrate various prior art cell libraries: U.S. patent application publication number 20050006670 of Zounes, U.S. patent application publication number 20040237059 of Chen et al., U.S. patent application publication number 20040218831 of Liu, U.S. patent application publication number 20040195690 of Flohr, U.S. patent application publication number 20040143797 of Nguyen et al., U.S. patent application publication number 20040040004 of Sakiyama et al., and U.S. patent application publication number 20030149953 of Whitaker et al.

In general, it is harder to correct design errors during later stages of the design process, and especially after the placement and routing stages.

Static timing analysis usually includes analyzing, debugging and validating the timing performance of a design of an integrated circuit. During this stage the timing associated with the propagation of signals through a designed integrated circuit are calculated. Especially, this analysis checks whether the delay of a component fits the clock frequency requirements, and whether hold and setup violations occurred.

U.S patent 6591407 of Kaufman et al., U.S. patent 5768159 of Belkadi et al., U.S. patent 6237127 of Craven et al., U.S. patent application publication number 2001/007144 of Terazawa, and PCT patent application publication number WO0075815 titled "An arrangement and a method relating to design of circuits", all being incorporated herein by reference, provide an overview of static timing analysis.

A hold violation is determined by checking if a data or a control input signal that is provided to a certain component was steady for at least a predefined period (referred to as a worst case hold time) relative to a corresponding clock event occurred. A clock event is usually a rising or falling edge of the clock signal.

A setup violation is determined by checking if a data or a control input signal that is provided to a certain component was steady for at least a predefined period (referred to setup period) before a corresponding clock event occurred.

The worst case hold time guarantees that regardless of the setup time the component will operate in a proper manner.

There is a need to provide an effective method for static timing analysis.

SUMMARY OF THE PRESENT INVENTION

A method and a computer readable medium for analyzing a design of an integrated circuit, as described in the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

FIG. 1 illustrates an exemplary circuit;

FIG. 2 illustrates a method for analyzing a design of an integrated circuit, according to an embodiment of the invention;

FIG. 3 illustrates various timing diagrams, according to an embodiment of the invention;

FIG. 4 illustrates a method for analyzing a design of an integrated circuit, according to an embodiment of the invention;

FIG. 5 illustrates a method for defining a cell library, according to an embodiment of the invention;

FIG. 6 illustrates an integrated circuit design process, according to an embodiment of the invention;

FIG. 7 illustrates a design station, according to an embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The following figures illustrate exemplary embodiments of the invention. They are not intended to limit the scope of the invention but rather assist in understanding some of the embodiments of the invention. It is further noted that all the figures are out of scale.

FIG. 1 illustrates an exemplary circuit 10. Circuit 10 includes multiple components such as D-type flip-flops 20, 22 and 24, as well as additional circuitries 30 and 32 that are connected between the flip flops. It is assumed that all flip flops 20, 22 and 24 receive the same clock signal and that the clock signals provided to the different flip flops are not skewed. This is not necessarily so. It is further noted that components other than flip flops can be analyzed and that the cell library can include cells other than flip flops. Typically such a library also includes logic gates.

Each flip flop can be characterized by multiple pairs of setup times and hold times. Conveniently, longer hold times are associated with shorter setup times. For example, the inventors found that very long setup times are associated with relatively short hold times. Conveniently, the sum of one pair of setup time and its associated hold time differs from a sum of another pair of setup time and its associated hold time.

It is noted that flip flops 20, 22 and 24 can be characterized by the same mapping between multiple setup times and hold times, but this is not necessarily so.

It is further noted that multiple setup time and hold time pairs of a certain component can be fed into a design station in various manners.

Multiple circuits such as circuit 10 are usually included within an integrated circuit that can be, for example, a processor, a system on chip. The integrated circuit can be included within a large range of systems of objects such as but not limited to a stationary device or a mobile device, such as but not limited to a cellular phone, a personal data accessory, a computer, a vehicle, a satellite, and the like.

It is further noted that circuit 10 can be a part of a boundary scan register that is activated by a relatively slow clock in which hold violation (rather then setup violation) occur, but this is necessarily so.

FIG. 2 illustrates a method 100 for analyzing a design of an integrated circuit, according to an embodiment of the invention.

Method 100 conveniently starts by stage 110 of defining, for at least one designed component of the integrated circuit, a mapping between multiple hold values and multiple setup values. Many (or all) components can be associated with such a mapping, while other components can be characterized by a single setup time and a single hold time.

Conveniently, the overall period during which a control or data signal has to be stable is not fixed. A sum of first setup time and a corresponding hold time is not necessarily the same as another sum of another setup time and a corresponding hold time. Conveniently, the relationship between the setup times and the hold times is non-linear.

According to various embodiments of the invention, once the mapping is defined it can be associated with a certain component in various alternative ways. According to one embodiment of the invention stage 110 can be followed by stage 120 of defining at least one component by associating it with multiple hold times and multiple setup times. Thus, in a cell library at least one cell definition can include these multiple setup and hold times.

According to another embodiment of the invention stage 110 is followed by stage 130 of associating a single pair of setup time and corresponding hold time with each designed component. Thus, if there are K different pairs of setup time and hold time, K different components are defined in the cell library. It is noted that according to yet a further embodiment of the invention M cells can be defined wherein K>M.

Either one of stage 110-130 is not executed for any design process. These stages are rather preliminary stages that are executed during the definition of a cell library. The cell library can be used during multiple design processes of multiple integrated circuits.

Either one of preliminary stages 110-130 is followed by stage 200 of defining possible timings of signals to be provided to the integrated circuit. This stage includes defining possible time windows during which signals can be provided to the integrated circuit. Typically, there are timing limitations imposed upon the provision of signals to the integrated circuit. The amount of typical scenarios can be very large but finite.

It is noted that the setup times and hold times can be responsive to additional parameters such as voltage, temperature and the like. The cell library can also include this relationship. According to another embodiment of the invention the cell library can include the worst setup time and/or the worst hold times for a range of possible temperatures values. The cell library can also include the worst setup time and worst hole times for a range of possible voltage supply values, and/or a combination of voltage supply and temperature values. Alternatively, the dependency between voltage and/or temperature and a range of possible setup times and/or hold times can be represented by few (even a single) setup times or hold times. This representation does not necessarily include the worst case scenario.

Stage 200 is followed by stage 240 of determining relationships between clock events and corresponding data/ control events that ideally precede the clock events, in response to the possible timing of signals. A data/control event can be a control event or a data event or a combination of both. Such an event occurs when at least one data and/or control signal changes.

Stage 240 conveniently includes determining the timing of signal propagation through the designed integrated circuit and especially determining for at least one designed component, and for multiple possible signals arrival times, at least one shortest time period between an occurrence of a clock event and an occurrence of the corresponding data (or control) event.

Assuming, for example that: (i) flip flop 20 can receive a data signal from an integrated circuit pin during a first timing window, (ii) flip flop 20 is triggered by a rising edge of a clock signal that can occur during a second timing window, and (iii) a rising edge of the data signal has to precede the clock signal. Given these assumptions stage 240 can include calculating the shortest time period between the rising edge of that data signal and the rising edge of the data signal.

It is noted that in many cases a certain component can receive (i) a first data or control signal that propagates through a first path, (ii) a second data or control signal that propagates through a second path, and (iii) a clock signal that propagates through a third path. In this case stage 240 conveniently includes calculating the time period between the latest data or control signal change and the earliest clock event. Stage 240 can include determining the setup time of each component. This setup time is conveniently the shortest setup time of each component that is still longer than the shortest time period between the change of the control or data signal and the corresponding clock signal. If no such setup time if found then setup violation occurs and has to be corrected.

Stage 240 is followed by stage 260 of determining at least one hold parameter in response to the relationships. This stage conveniently includes using the mapping between multiple setup values and the multiple hold times and finding the hold time that corresponds to the setup time found in stage 240.

Stage 260 is followed by stage 280 of calculating hold violations by comparing the hold times determined during stage 260 to the relative timings of clock signals and corresponding data or clock signals. The relative timing can include the shortest period between a clock event and a following data or control change.

Stage 280 is followed by stage 300 of correcting hold violation. Conveniently, stage 300 also includes correcting setup violations.

Stage 300 can include at least one of the following stages: (i) replacing one component by another component from the cell library that differs by its setup time or its hold time from the replaced component, (ii) introducing a delay within the path of the data or control signal that caused a hold violation, (iii) introducing multi-cycle paths, and the like.

Stage 300 can be followed by stage 240 such that stages 240-300 are repeated until the timing violations are corrected. The repetition can also be responsive to another or to an alternative control criterion, such as the amount of iterations, and the like.

It is noted that usually the timing conditions of all components of a designed integrated circuit are checked, in view of all the possible timing constraints imposed on input signals to the designed integrated circuit.

FIG. 3 illustrates various timing diagrams 61, 62, 71 and 72, according to an embodiment of the invention. For simplicity of explanation the rising period and falling period of each signal was assumed to be negligible.

It is noted that in some cases the rising period and/or falling period are taken into account when determining setup an/or hold violations.

According to an embodiment of the invention there is provided a mapping between setup times, hold times and relevant rising or falling periods of the corresponding signals. If, for example a device is triggered by a rising edge of the clock and the corresponding data raises before the rising edge of the clock and is negated after the rising edge of the clock the setup violation is responsive to the rising period of the clock signal and the rising period of the data signal. A hold violation is determined in view of the setup period, the rising period of the clock signal and the falling period of the data signal.

The timing diagrams illustrate various timing windows of various clock and data signals that arrive to flip flop 20. Each timing window is illustrated by the earliest signal and the latest signal that define the timing window.

It is assumed that flip flop 20 is triggered by the rising edge of clock signal CLK 60 and that it also receives a data signal D 70. The rising edge of CLK 60 can arrive to the clock input of flip flop 20 between T3 and T4, as illustrated by lines 61 and 62. The rising edge of CLK 60 is a clock event.

The rising edge (data event) of data signal D 70 can arrive to the data input of flip flop 20 between T1 and T2, and can be negated (another data event) between T5 and T6, as illustrated by lines T1 and T2. It is noted that this signal can be first negated and the asserted.

Table 1 illustrates the multiple setup times and hold times that characterized flip flop 20:

Setup time	Hold time
SU1	H1
SU2	H2
SU3	H3
SU4	H4

These values are not responsive to clock skews. Clock skews can shift the timing of signals that are later compares to the setup and hold times. It is also assumed that: (i) SU1<SU2<SU3<SU4, (ii) H1<H2<H3<H4, (iii) that (SU1+H1) differs from at least one of the following sums: (SU2+H2), (SU3+H3) or (SU4+H4), and that (iv) the ratio (SU1/SU2) differs from at least one of the following ratios: (H1/H2), (H2/H3) or (H4/H3).

Given this set of assumptions stage 240 may include determining the shortest period between the assertion of the data signal D 70 and the rising edge of CLK 60. This period is T3-T2.

Stage 240 may also include calculating the shortest setup period out of SU1-SU4 that is still shorter than T3-T2. If such a setup period is not found that there is a need to correct this setup violation by various means including delays, cell replacement and the like. Assuming that such a set up period is found and that it is SU2 then stage 260, that follows stage 240, includes selecting H2 as the relevant hold time.

Stage 260 is followed by stage 280 of calculating hold violations by comparing the relevant hold time H2 to the timing difference between the latest possible CKL 60 rising edge (T4) and the earliest negation of D 70 (T5).

If (T5-T4) is shorter that H2 then a hold violation occurred. It is noted that if (T5-T4) is shorter than H4 but is longer than H2 than a hold violation does not occur, although prior art methods would determine that a hold violation occurred and perform an unnecessary hold violation correction stage.

FIG. 4 illustrates a method 400 for analyzing an design of an integrated circuit, according to an embodiment of the invention.

Method 400 starts by stage 110 of defining, for at least one designed component of the integrated circuit, a mapping between multiple hold times and multiple setup times. This mapping is not responsive to clock skews.

Conveniently, stage 110 can be followed by optional stage 120 or 130.

Either one of stages 110-130 can be followed by stage 280 of calculating hold violations in response to the mapping.

FIG. 5 illustrates method 500 for defining a cell library, according to an embodiment of the invention.

Method 500 starts by stage 510 of defining at least one internal delay of a designed component.

Stage 510 is followed by stage 520 of providing a cell that is characterized by multiple hold times and multiple setup values. The relationship between these times is not responsive to clock skews. Conveniently, the period during which a signal has to be stable is not fixed. A sum of first setup time and a corresponding hold time is not necessarily the same as a another sum of another setup time and a corresponding hold time. Conveniently, the relationship between the setup times and the hold times is non-linear.

According to various embodiments of the invention, once the mapping is defined it can be associated with a certain component in various alternative ways. Some of these ways are illustrated in relation to stage 110 of FIG. 2.

FIG. 6 illustrates an integrated circuit design process 600, according to an embodiment of the invention.

Process 600 starts by stage 610 of high level circuit design. This stage can include using a high level design language such as Verilog, RTL and the like. Stage 610 is followed by stage 620 of design synthesis, given various timing constraints (possible timings of signals to be provided to the integrated circuit), and given a cell library.

The cell library or at least some of the cells of the cell library can be defined by using stages 110-130 or stages 510-520. Some of the content of the cell library can be determined in prior art manners, such as receiving a standard cell library, using predefined cell libraries and the like.

Stage 620 is followed by stage 630 of performing placement and routing.

Stage 630 is followed by stage 640 of performing static timing analysis. According to an embodiment of the invention stage 640 can includes include various stages of method 100 or method 400. According to another embodiment of the invention these stages can be applied in combination with prior art static timing analysis stages.

According to yet another embodiment of the invention stage 640 can include stage 642 of performing a prior art static timing analysis based upon worst case hold time and setup time and receiving timing violations. Stage 642 is followed by stage 644 of determining, in response to the possible timing of signals arriving to the components, the appropriate setup times and the corresponding hold times. Stage 644 can include stage 240.

Stage 644 is followed by stage 300 of correcting timing violations.

FIG. 7 illustrates a design station 710, according to an embodiment of the invention.

The design station can be a stand-alone station or part of a network or a group of design station.

The design station is illustrated, for convenience of explanation as a desktop computer 710 that includes a processor 720 as well as a computer readable medium 700 that stores a set of instructions to be executed by the processor 720. The processor 720 can access a cell library 750 during the various design stages.

It is noted that many design station configurations are known in the art and can be applied. The design can be implemented by many designers that have access to multiple design stations that in turn can access remote storage devices that can store cell libraries, instructions, integrated circuit designs and the like.

According to various embodiments of the invention the mentioned above methods (100, 400, 500, 600) can be executed by a processor that executed a set of instructions that is stored within a computer readable medium. This medium can include magnetic storage devices (such as magnetic tape, diskettes, disk drives), optical storage devices (such as DVD, CD) and the like. The processor can execute the method in cooperation with other components such as storage unit, buses and the like.

According to an embodiment of the invention a computer readable medium is provided having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to define possible timings of signals to be provided to the integrated circuit, to determine relationships between clock events and corresponding data/control events that ideally precede the clock events, in response to the possible timing of signals, and determine hold parameters in response to the relationships and to calculate hold violations.

According to an embodiment of the invention a computer readable medium is provided having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to define, for at least one designed component of the integrated circuit, a mapping between multiple hold times and multiple setup values, and to calculate hold violations.

According to an embodiment of the invention a computer readable medium is provided having stored thereon a set of instructions, the set of instructions, when executed by a processor cause the processor to define cell that is characterized by multiple hold times and multiple setup times.

Variations, modifications, and other implementations of what is described herein will occur to those of ordinary skill in the art without departing from the spirit and the scope of the invention as claimed. Accordingly, the invention is to be defined not by the preceding illustrative description but instead by the spirit and scope of the following claims.

WE CLAIM

1. A method (100) for analyzing an design of an integrated circuit, the method comprises defining (200) possible timings of signals to be provided to the integrated circuit and calculating (280) hold violations;

characterized by comprising a stage of determining (240) relationships between clock events and corresponding data/control events that ideally precede the clock events, in response to the possible timing of signals, and determining (260) hold parameters in response to the relationships.

2. The method (100) according to claim 1 wherein the stage of determining (240) the relationships, comprises determining, for at least one designed component, and for multiple possible timings of signals, at least one shortest time period between an occurrence of a clock event and an occurrence of the corresponding data/control event.

3. The method (100) according to any claim out of claim 1 and 2 further comprising correcting (300) hold violations.

4. The method (100) according to claim 3 wherein the correcting (300) comprises replacing one component by another component that differs by its setup time or its hold time from the replaced component.

5. The method (100) according to claim 1 further comprising defining (110), for at least one designed component of the integrated circuit, a mapping between multiple hold values and multiple setup values.

6. The method (100) according to claim 5 wherein a sum of first setup time and a corresponding hold time differs

from another sum of another setup time and a corresponding hold time.

7. The method according to claim 5 wherein the relationship between the setup times and the hold times is non-linear.

8. The method according to claim 1 further comprising defining (120) at least one component by multiple hold times of the designed component and multiple setup times of the designed component.

9. The method according to claim 1 further comprising defining (130) associating a single pair of setup time and corresponding hold time with each designed component.

10. A method (400) for analyzing an design of an integrated circuit, the method comprises calculating (280) hold violations; characterized by defining (110), for at least one designed component of the integrated circuit, a mapping between multiple hold times and multiple setup values.

11. The method (400) according to claim 9 wherein a sum of first setup time and a corresponding hold time differs from another sum of another setup time and a corresponding hold time.

12. The method according to claim 9 further comprising defining (120) at least one component by multiple hold times values of the designed component and multiple setup times of the designed component.

13. The method according to claim 9 wherein the relationship between the setup times and the hold times of at least one designed component is non-linear.

14. A method (500) for defining a cell library, the method comprises defining (410) at least one internal delay of a designed component; the method characterized by providing (420) a cell that is characterized by

multiple hold times and multiple setup values for a certain clock skew value.

15. The method (500) according to claim 12 wherein a sum of first setup time and a corresponding hold time differs from another sum of another setup time and a corresponding hold time.

16. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to define possible timings of signals to be provided to the integrated circuit and calculate hold violations; characterized by causing the processor to determine relationships between clock events and corresponding data/control events that ideally precede the clock events, in response to the possible timing of signals; and determine hold parameters in response to the relationships.

17. The computer readable medium according to claim 16 wherein the set of instructions further cause the processor to determine, for at least one designed component, and for multiple possible timings of signals, at least one shortest time period between an occurrence of a clock event and an occurrence of the corresponding data/control event.

18. The computer readable medium according to claim 16 wherein the set of instructions further cause the processor to correct hold violations.

19. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to calculate hold violations; characterized by causing the processor to define, for at least one designed component of the integrated circuit, a mapping between multiple hold times and multiple setup values.

20. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to define at least one internal delay of a designed component, characterized by causing the processor to define a cell that is characterized by multiple hold times and multiple setup values for a certain clock skew value.

AMENDED CLAIMS

[received by the International Bureau on 31 May 2006 (31.05.2006) : original claims 1-20 replaced by amended claims 1-20]

1. A method (100) for analyzing a design of an integrated circuit, the method comprises

defining (200) possible timings of signals to be provided to the integrated circuit and

calculating (280) hold violations;

characterized by comprising:

defining (110), for at least one designed component of the integrated circuit, a mapping between multiple hold values and multiple setup values for a certain clock skew value;

determining (240) relationships between clock events and corresponding data/control events that ideally precede the clock events, in response to the possible timing of signals,

determining (260) hold parameters in response to the relationships; and

correcting (300) hold violations.

2. The method (100) according to claim 1 wherein the stage of determining (240) the relationships comprises determining, for at least one designed component, and for multiple possible timings of signals, at least one shortest time period between an occurrence of a clock event and an occurrence of the corresponding data/control event.

3. The method (100) according to any claim out of claims 1 and 2 wherein the defining (110) comprises defining a mapping between multiple hold values and multiple setup values, wherein the multiple setup times and the multiple hold times are responsive to a temperature parameter.

4. The method (100) according to claim 3 wherein the correcting (300) comprises replacing one component by another component that differs by its setup time or its hold time from the replaced component.

5. The method (100) according to any claim out of claims 1-4 wherein the defining (110) comprises defining a mapping between multiple hold values and multiple setup values, wherein the multiple setup times and the multiple hold times are responsive to a temperature parameter.

6. The method (100) according to claim 1 wherein the defining (110) comprises defining a mapping such that a sum of first setup time and a corresponding hold time differs from another sum of another setup time and a corresponding hold time.

7. The method according to claim 1 wherein the defining (110) comprises defining a mapping such that the relationship between the setup times and the hold times is non-linear.

8. The method according to claim 1 further comprising defining (120) at least one component by multiple hold times of the designed component and multiple setup times of the designed component for a certain clock skew value.

9. The method according to claim 1 further comprising defining (130) associating a single pair of setup time and corresponding hold time with each designed component.

10. A method (400) for analyzing a design of an integrated circuit, the method comprises calculating (280) hold violations;

characterized by defining (110), for at least one designed component of the integrated circuit, a mapping between multiple hold times and multiple setup values for a certain clock skew value;

wherein the defining (110) comprises defining a mapping such that the relationship between the setup times and the hold times is non-linear.

11. The method (400) according to claim 9 wherein the defining (110) comprises defining a mapping such that a sum of first setup time and a corresponding hold time differs from another sum of another setup time and a corresponding hold time.

12. The method according to claim 9 further comprising defining (120) at least one component by multiple hold times values of the designed component and multiple setup times of the designed component.

13. The method according to claim 9 wherein the relationship between the setup times and the hold times of at least one designed component is non-linear wherein very long setup times are associated with relatively short hold times.

14. A method (500) for defining a cell library, the method comprises defining (410) at least one internal delay of a designed component;

the method characterized by providing (420) a cell that is characterized by multiple hold times and multiple setup values for a certain clock skew value.

15. The method (500) according to claim 12 wherein the defining (410) comprises defining the mapping such that a sum of first setup time and a corresponding hold time differs from another sum of another setup time and a corresponding hold time.

16. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to

define, for at least one designed component of the integrated circuit, a mapping between multiple hold values and multiple setup values for a certain clock skew value;

define possible timings of signals to be provided to the integrated circuit and calculate hold violations; characterized by causing the processor to determine relationships between clock events and corresponding data/control events that ideally precede the clock events, in response to the possible timing of signals;

determine hold parameters in response to the relationships; and

correct hold violations.

17. The computer readable medium according to claim 16 wherein the set of instructions further cause the processor to determine, for at least one designed component, and for multiple possible timings of signals, at least one shortest time period between an occurrence of a clock event and an occurrence of the corresponding data/control event.

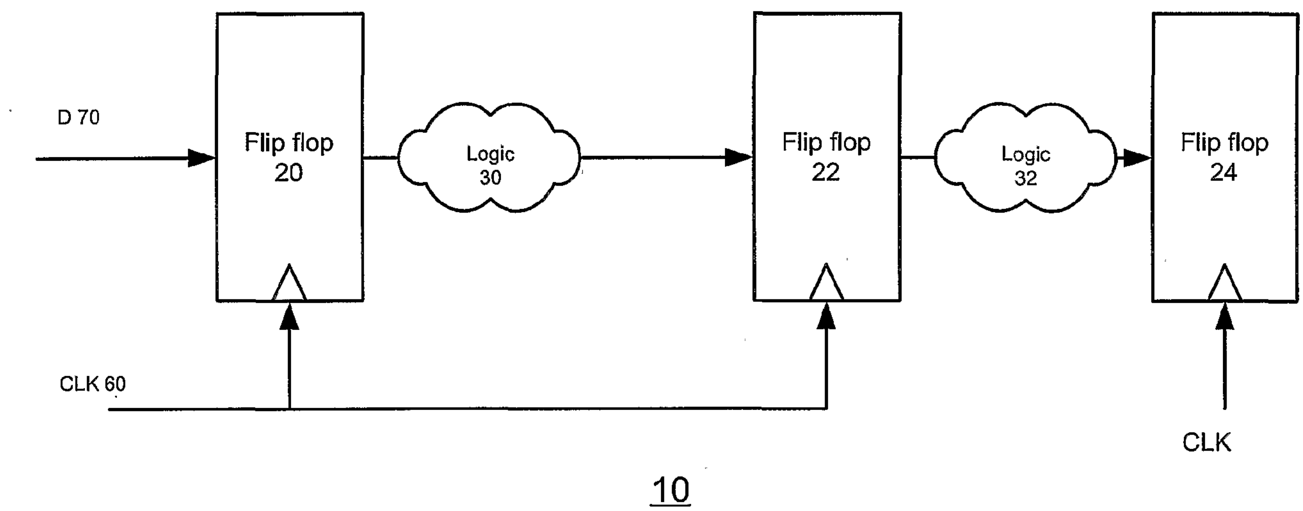
18. The computer readable medium according to claim 16 wherein the set of instructions further cause the processor to define a mapping such that the relationship between the setup times and the hold times is non-linear.

19. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to calculate hold violations;

characterized by causing the processor to define, for at least one designed component of the integrated circuit, a mapping between multiple hold times and multiple setup values for a certain clock skew value.

20. A computer readable medium (700) having stored thereon a set of instructions, the set of instructions, when executed by a processor, cause the processor to define at least one internal delay of a designed component,

characterized by causing the processor to define a cell that is characterized by multiple hold times and multiple setup values for a certain clock skew value.



PRIOR ART

FIG. 1

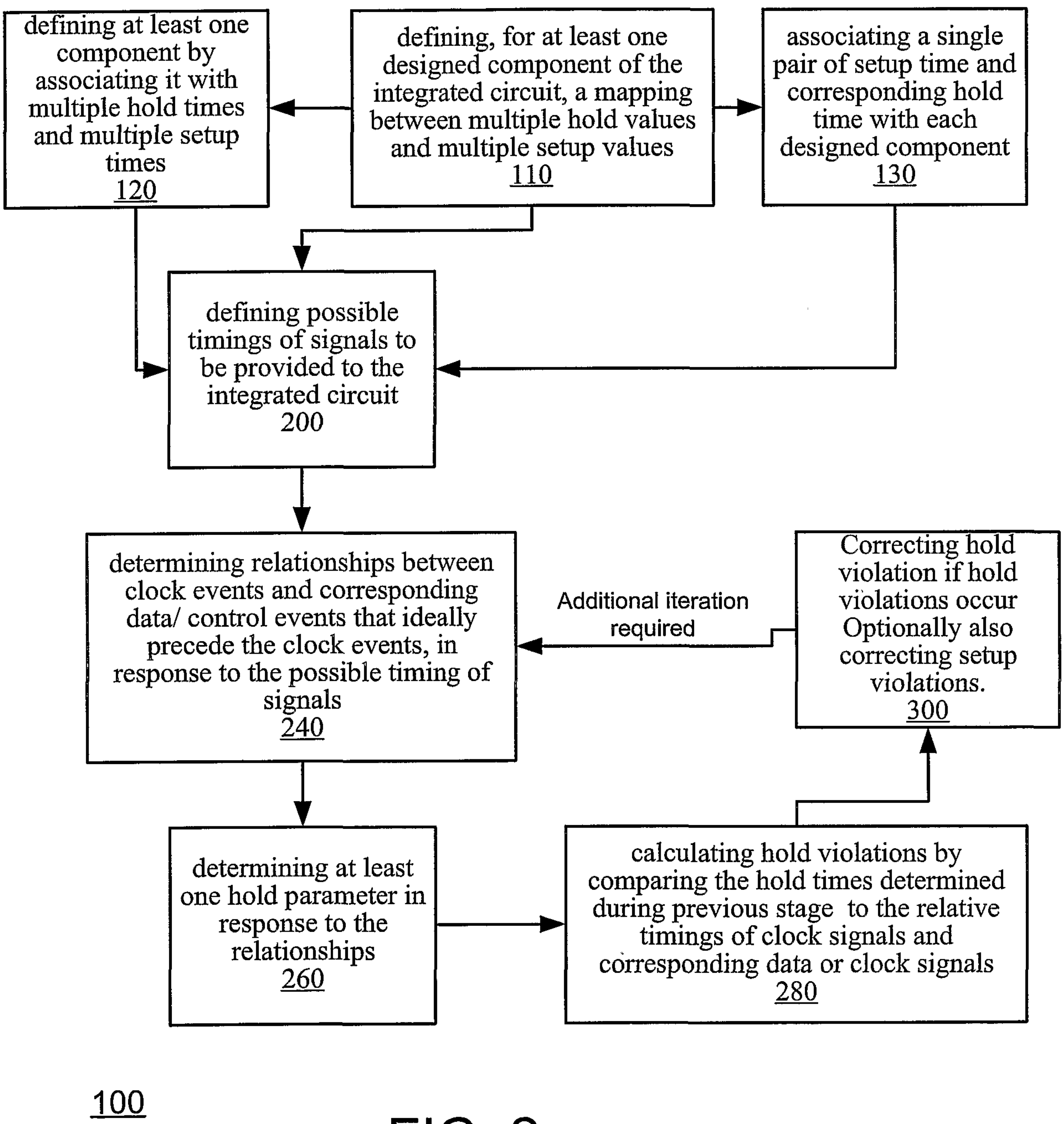

defining at least one component by associating it with multiple hold times and multiple setup times
120
defining, for at least one designed component of the integrated circuit, a mapping between multiple hold values and multiple setup values
110
associating a single pair of setup time and corresponding hold time with each designed component
130
defining possible timings of signals to be provided to the integrated circuit
200
determining relationships between clock events and corresponding data/ control events that ideally precede the clock events, in response to the possible timing of signals
240
Additional iteration required
Correcting hold violation if hold violations occur Optionally also correcting setup violations.
300
determining at least one hold parameter in response to the relationships
260
calculating hold violations by comparing the hold times determined during previous stage to the relative timings of clock signals and corresponding data or clock signals
280
100

FIG. 2

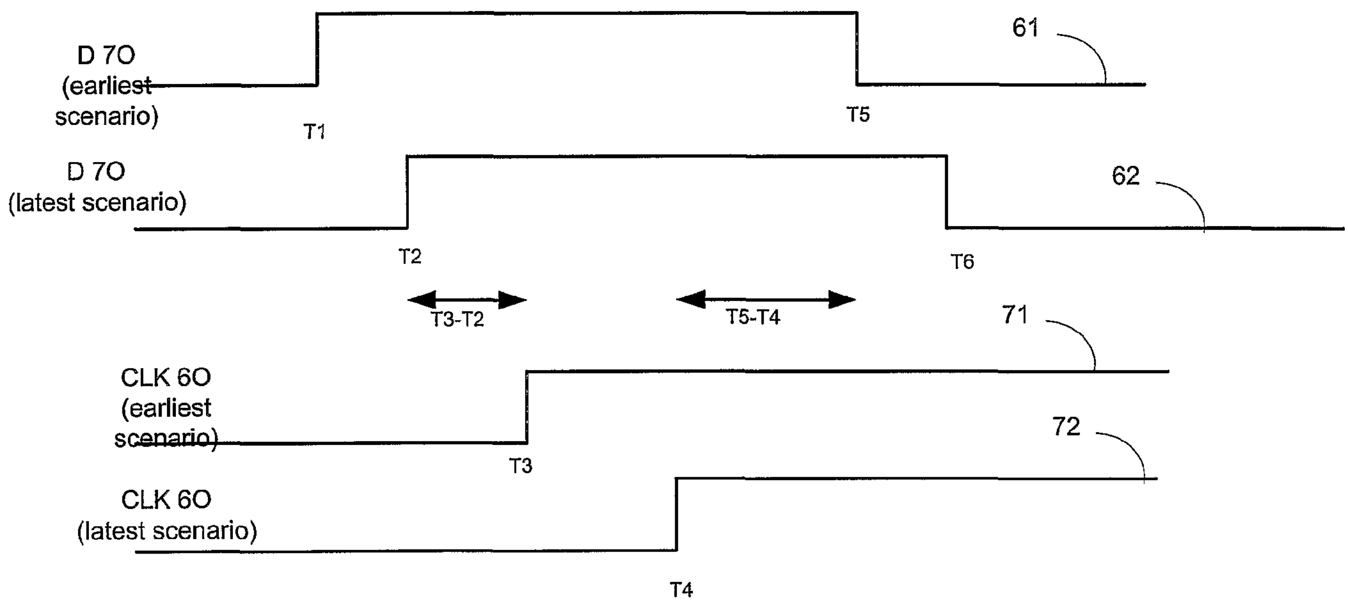

D 7O
(earliest
scenario)
T1
T5
61
D 7O
(latest scenario)
T2
T6
62
T3-T2
T5-T4
71
CLK 6O
(earliest
scenario)
T3
72
CLK 6O
(latest scenario)
T4

FIG. 3

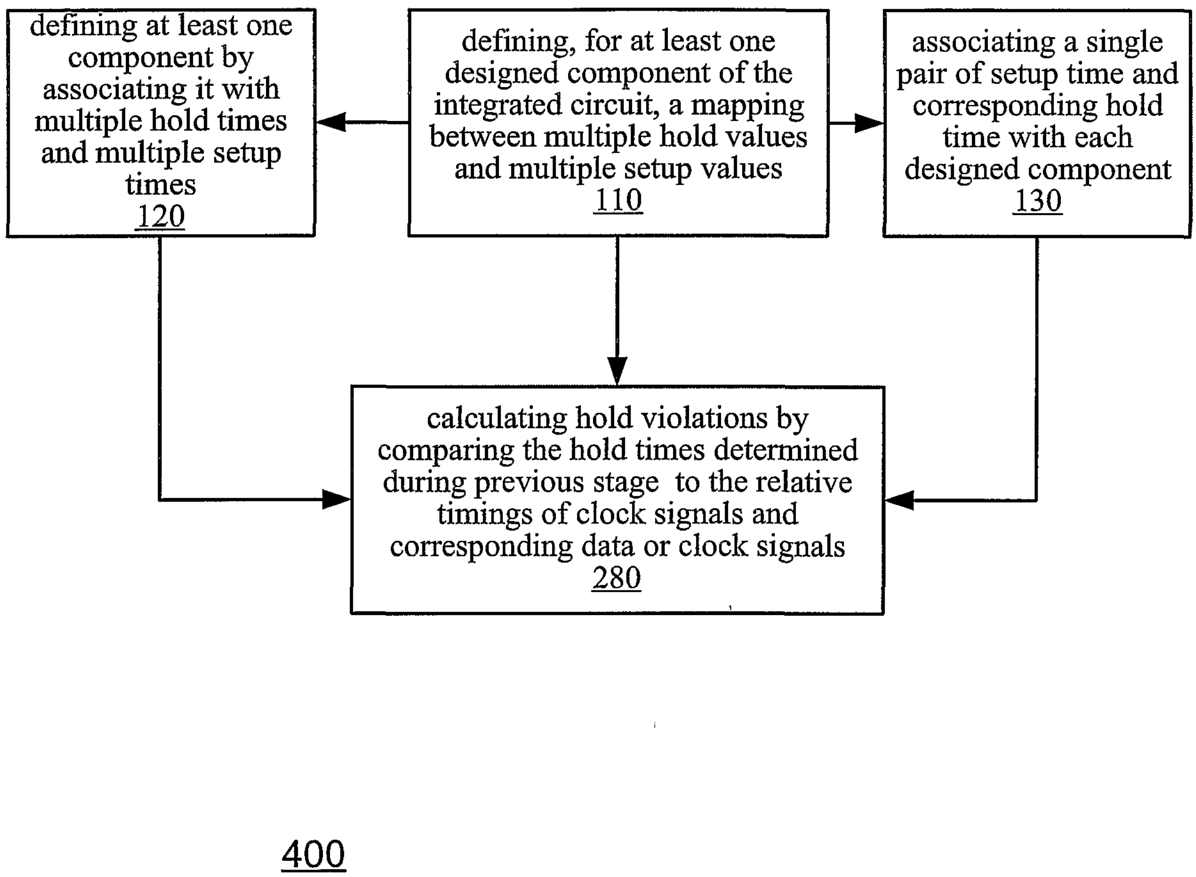
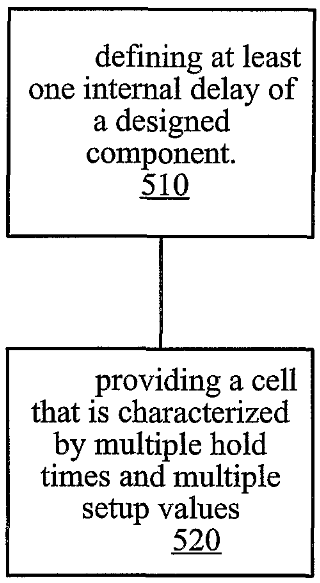

defining at least one component by associating it with multiple hold times and multiple setup times
120
defining, for at least one designed component of the integrated circuit, a mapping between multiple hold values and multiple setup values
110
associating a single pair of setup time and corresponding hold time with each designed component
130
calculating hold violations by comparing the hold times determined during previous stage to the relative timings of clock signals and corresponding data or clock signals
280
400

FIG. 4


defining at least one internal delay of a designed component.
510
providing a cell that is characterized by multiple hold times and multiple setup values
520

500

FIG. 5

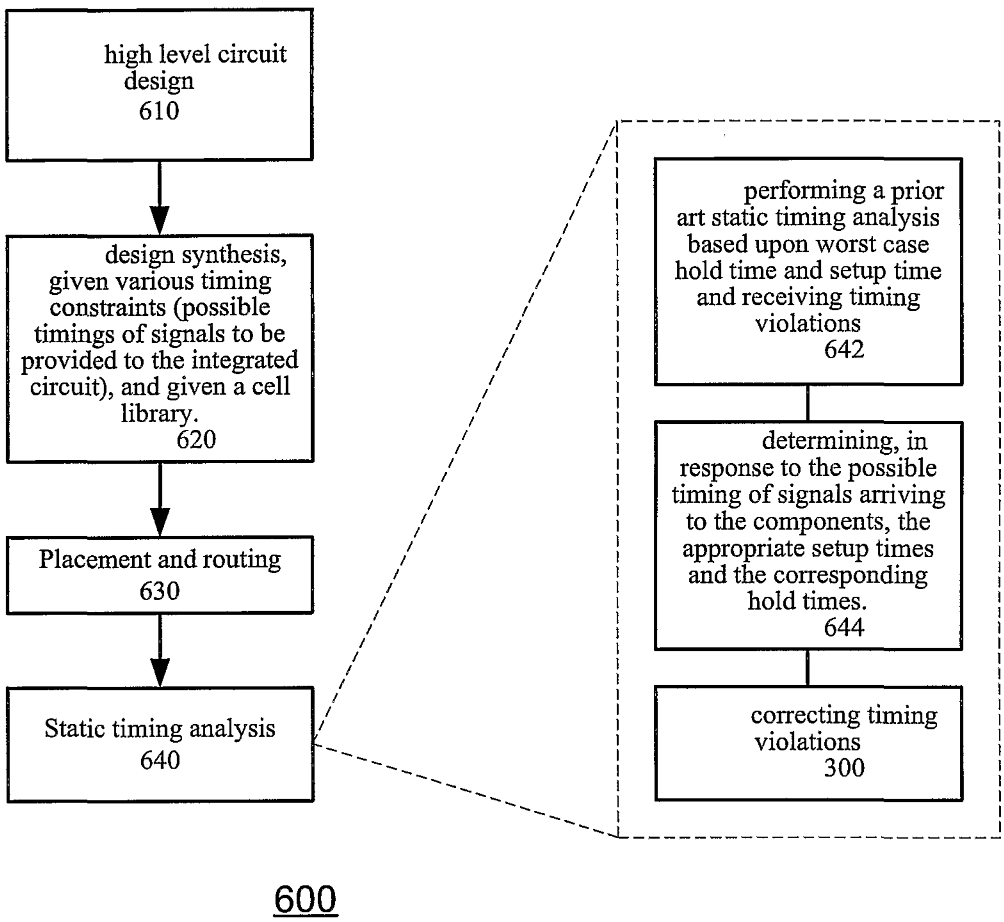

high level circuit design
610
design synthesis, given various timing constraints (possible timings of signals to be provided to the integrated circuit), and given a cell library.
620
Placement and routing
630
Static timing analysis
640
performing a prior art static timing analysis based upon worst case hold time and setup time and receiving timing violations
642
determining, in response to the possible timing of signals arriving to the components, the appropriate setup times and the corresponding hold times.
644
correcting timing violations
300
600

FIG. 6

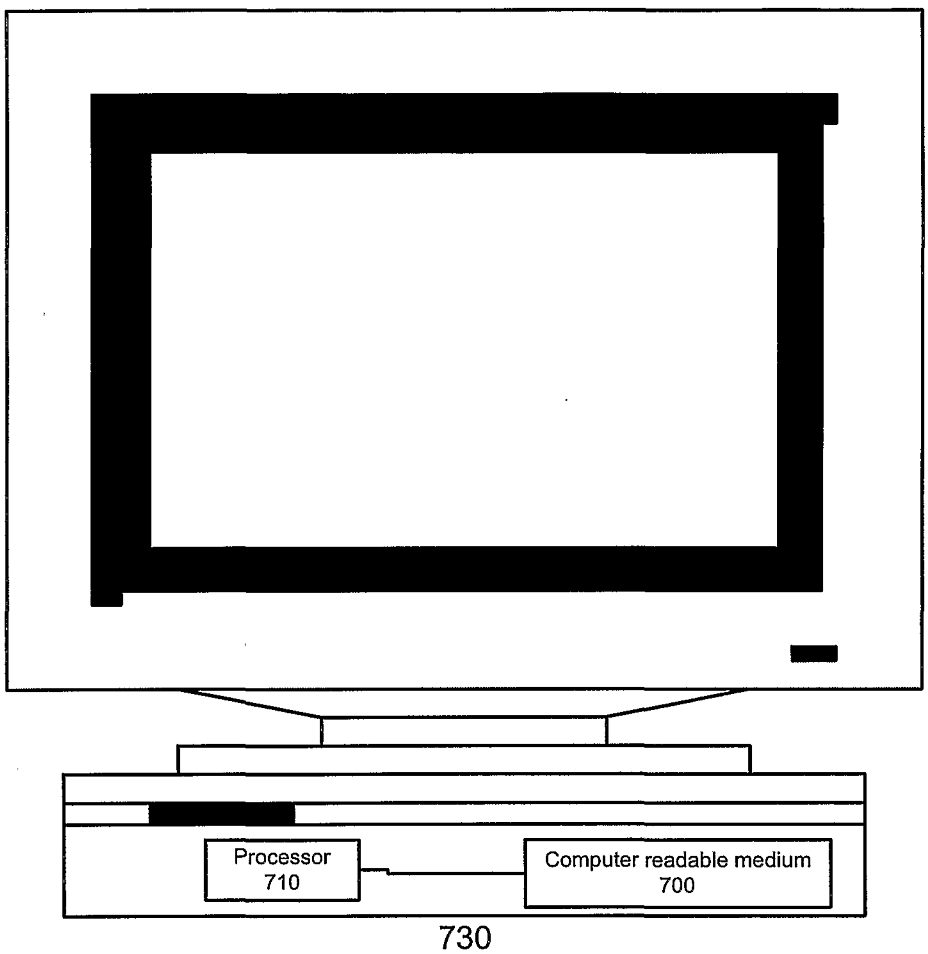


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2005/052912

A. CLASSIFICATION OF SUBJECT MATTER
G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/75815 A (TELEFONAKTIEBOLAGET LM ERICSSON) 14 December 2000 (2000-12-14) abstract page 5 - page 6 page 8 - page 10 page 11 - page 12 page 13 - page 15 -----	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2006	28/03/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Radev, B

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2005/052912

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
WO 0075815	A	14-12-2000	AU	5436200	A	28-12-2000
			SE	516166	C2	26-11-2001
			SE	9902079	A	05-12-2000