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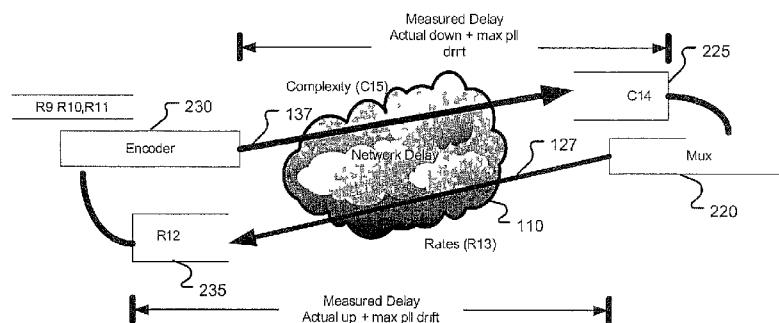


Figure 2

(57) **Abstract:** The present invention discloses methods and systems of statistical video multiplexing to improve the performance of video encoding by minimizing delay while achieving high video quality. The video encoders used in the system are capable of calculating the complexity of underlying video sources and communicating the complexity to the multiplexer. Furthermore, the video encoders are capable of estimating the look-ahead complexity, i.e. the future complexity and communicating the future complexity values to the multiplexer. A processor associated with the multiplexer allocates bit rates for the video encoders according to the received complexity values and future complexity values. The bit rate information is then communicated to the video encoders. Each video encoder will then exercise its coding control parameters to regulate the resulting bit rate to be within or close to the allocated bit rate.

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## U.S. Non-Provisional Patent Application

Title: SYSTEMS AND METHODS FOR VIDEO STATISTICAL MULTIPLEXING  
ADAPTING TO INTERNET PROTOCOL NETWORKS

## TECHNICAL FIELD

[0001] The invention relates to the field of digital video transmission. More particularly the invention relates to methods and systems of statistical video multiplexing adapted to Internet protocol networks.

## RELATED APPLICATION

[0002] This application claims the priority benefit of U.S. Provisional Patent Application No. 61/182,659, "Systems and Methods for Video Statistical Multiplexing Adapting to Internet Protocol Networks", filed May 29, 2009, the disclosure of which is incorporated by reference herein.

## BACKGROUND

[0003] Digital video multiplexing allows multiple encoded video bitstreams to be transmitted on a common digital channel. Concatenating a large amount of data on a safe channel has its benefits, but also presents significant challenges. Due to the inherent characteristics of video content, the bit rate of video data fluctuates. Video content with complex scenes and frequent motion has higher bit rates, whereas videos with simpler scenes have lower bit rates. However, the transmission channel often has a fixed bandwidth or fixed allocated bandwidth for a period of time. Consequently, if the total bit rate exceeds the available channel bandwidth, some of the encoded data is dropped or delayed for later transmission. This results in video quality degradation due to repeated drops and delays of encoded data. Video statistical multiplexing is a technique that takes the advantage of the statistical nature of unrelated video sources to improve video quality. For unrelated video sources, different sources will not always generate high bit rates or low bit rates at the same time. From a mathematical perspective , the aggregated bit rate

will statistically have a bell shaped probability distribution curve with a mean bit rate and a variance. When the number of video sources increases, the normalized variance becomes smaller. The aggregated bit rate is thus more "predictable" or "stable" for a larger number of video sources. As a result, the likelihood that the aggregated bit rate will exceed the channel bandwidth decreases. While the video source is addressed herein, video streams are accompanied by associated audio content that is transmitted synchronously. Audio content is often compressed using constant bit rate (CBR) coding or variable bit rate (VBR) coding. The quantity of compressed audio data is usually smaller than that of video data.

[0004] For the sake of simplicity, only video data is specifically referred to herein. However, it is understood that video data may include associated audio data. In addition, the terms "bitrate", "bit rate" and "rate" are often used interchangeably in the art to refer to units of video data per unit of time. Other terms maybe used herein to refer to technical jargon and well known terms of art. These terms are used for illustrations purposes.

[0005] While statistical video multiplexing takes advantage of the statistical behavior of underlying multiple video sources, the aggregated bit rate may still exceed the available bandwidth. In order to further improve video quality, the statistical video multiplexer can work in conjunction with the video encoders to reduce the aggregated bit rate to fit within the allocated overall bandwidth. The video statistical multiplexer may take a very conservative approach by allocating a relatively low bit rate to each encoder to reduce or duplicate data loss. In such a design, each encoder could use a coarse quantizer or other means to generate a compressed bit stream that fits within the allocated bit rate. As a consequence of the low bit rate, however, degradation in video quality may result. Those skilled in the art may adopt a general bit rate control strategy that allocates as high a bit rate as possible while keeping the aggregated bit rate within the allocated bandwidth.

[0006] If the multiplexer is located at a service head-end while the encoders are remotely located at different sites, the statistical video multiplexing is complicated by possible network delays between the multiplexer and encoders. Dynamic delay characteristics result when the multiplexer and video encoders are connected over internet protocol (IP) networks. In an IP network environment, packet delay can often occur during periods of high overall network

traffic. To account for this effect, the multiplexer may use a simple approach by always assuming the greatest possible delay for all encoders. However, this simple approach unnecessarily introduces more delay in transmitting the underlying video data generated by the video encoders.

[0007] Therefore, there is a need for methods and systems of video multiplexing that minimize delay while maintaining optimal video quality. These methods and systems should take into account the dynamic delay characteristics of IP networking and provide an adaptive solution for the changing network environment. Furthermore, the methods and systems should provide a mechanism for the multiplexer to function properly during the transition from one network delay to another network delay.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 shows a prior art video multiplexing system that always assumes the greatest possible network delay for all video encoders.

[0009] Figure 2 shows a video multiplexing system embodying the present invention.

[0010] Figure 3 shows a proration layer structure where the complexity and bit rate are prorated.

[0011] Figure 4A shows an example of complexity proration for the case  $p+PD < DT$ .

[0012] Figure 4B shows an example of complexity proration for the case  $DT < p+PD < 2DT$ .

[0013] Figure 4C shows an example of complexity proration for the case  $p+PD > 2DT$ .

[0014] Figure 5A shows an example of bit rate proration for the case  $p+PD < DT$ .

[0015] Figure 5B shows an example of bit rate proration for the case  $DT < p+PD < 2DT$ .

[0016] Figure 5C shows an example of bit rate proration for the case  $p+PD > 2DT$ .

[0017] Figure 6 shows a complexity data structure at the multiplexer.

[0018] Figure 7 shows a timeline for the events associated with the multiplexer.

[0019] Figure 8 shows the states of a sample video multiplexing system having three video encoders before the network delay for video encoder #1 increases from 0 to 4 DT periods.

[0020] Figure 9 shows the states of a sample video multiplexing system having three video encoders during a network delay increase.

[0021] Figure 10A shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 9.

[0022] Figure 10B shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 10A.

[0023] Figure 10C shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 10B.

[0024] Figure 10D shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 10C.

[0025] Figure 11 shows the states of a sample video multiplexing system having three video encoders during network delay change where the bit rates and complexity values are at the maximum network delay.

[0026] Figure 12A shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 11 during the transition of the network delay from 0 to 4 DT periods.

[0027] Figure 12B shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 12A during the transition of the network delay from 0 to 4 DT periods.

[0028] Figure 12C shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 of Figure 12B during the transition of the network delay from 0 to 4 DT periods.

[0029] Figure 12D shows the state of the sample video encoder #1 at 1 DT period after the state of the sample video encoder #1 in Figure 12C during the transition of the network delay from 0 to 4 DT periods.

[0030] Figure 13 shows the states of a sample video multiplexing system having three video encoders before the network delay for video encoder #3 decreases from 4 to 1 DT period.

[0031] Figure 14 shows the states of a sample video multiplexing system having three video encoders at 1 DT period after the network delay for video encoder #3 decreases from 4 to 1 DT period.

[0032] Figure 15 shows the states of the sample video encoder #3 during the transition of the network delay for video encoder #3 decreases from 4 to 1 DT periods.

[0033] Figure 16A shows the states of the sample video encoder #3 after the network delay change is stable.

[0034] Figure 16B shows the states of the sample video encoder #3 at 1 DT period after the state corresponding to Figure 16A.

[0035] Figure 16C shows the states of the sample video encoder #3 at 1 DT period after the state corresponding to Figure 16B.

## DETAILED DESCRIPTION

[0036] The present invention discloses methods and systems of statistical video multiplexing to improve performance by minimizing delay while maintaining high video quality. The video encoders used in the system are capable of calculating the complexity of underlying video sources and communicating said complexity to the multiplexer. Furthermore, the video encoders are capable of estimating the look-ahead complexity, i.e. the future complexity and communicating the future complexity values to the multiplexer. A processor associated with the multiplexer allocates bit rates for the video encoders according to the received complexity values and future complexity values. The bit rate information is then communicated to the video

encoders. Each video encoder will then exercise its coding control parameters to regulate the resulting bit rate to be within or close to the allocated bit rate.

[0037] The present invention can be applied to IP networks where the network delay varies depending on the traffic levels. Generally, longer delays occur during periods of high traffic and shorter delays during periods of low traffic. The present invention utilizes a queue at each video encoder to buffer the bit rates received from the multiplexer and utilizes a queue at the multiplexer for each video encoder to buffer the complexity values received from the video encoder. A mechanism to accommodate the dynamic network delay is provided to detect the delay changes, whether increasing or decreasing, and to cause the video encoders and multiplexer to adjust accordingly. The video encoder will determine an index according to the buffer status for the complexity value to be generated, and generate a main complexity value associated with the complexity index. The multiplexer will monitor the status of the corresponding queue for the video encoder and determine the bit rate based on the main complexity value or the look-ahead complexity value.

[0038] In one embodiment of the present invention, the multiplexer receives a main complexity value and one or more look-ahead complexity values from the video encoder. The multiplexer then allocates bit rates for the video encoders according to the received main complexity values and the future complexity values and communicates said bit rates to the video encoders. The video encoder will use a bit rate buffer for storing bit rates and monitoring the status, and will determine the index for the complexity value according to the status of the bit rate buffer. The multiplexer will use a complexity buffer for storing main and look-ahead complexity values and monitoring the status, and will determine the bit rate based on either the main complexity value or one of the look-ahead complexity values according to the status of the complexity buffer.

[0039] Although the present invention has been described in terms of specific embodiments it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alterations and modifications as fall within the true spirit and scope of the invention.

[0040] While "video" multiplexer and "video" encoders are referred to in the specification, it is understood that "video" is referring to video data as well as any associated audio data. The audio

portion is not explicitly described. However, those skilled in the art can practice the present invention on video data having associated audio data. A conventional video multiplexing system is shown in Figure 1 where the system always assumes all video encoders are continuously experiencing the worst possible network delay. While such an approach is simple in design, it unnecessarily introduces more delay, particularly to those video encoders that have shorter network delay. As shown in Figure 1, the multiplexer 120 and the video encoder 130 are connected through a network cloud 110. Only one of the multiple video encoders is shown in the drawing. However, it is understood that there are more video encoders of similar structure, not shown in Figure 1, connected to the multiplexer 120 through the network cloud 110. In this disclosure, the word "mux" may be used as an abbreviation for the multiplexer or the video multiplexer. Also the terms "multiplexer" and "video multiplexer" are used interchangeably in the disclosure. The multiplexer 120 and the encoder 130 can be co-located at the same site or can be far apart. For example, the multiplexer may be located at a cable head-end in New York city while the video encoder is located in Los Angeles. The video encoders need not be co-located and can be scattered around in various cities. Each video encoder has an associated buffer 135 to store the bit rates sent by the multiplexer 120 through a connection 127. The multiplexer also has a corresponding buffer 125 for each video encoder 130 to store the complexity values sent by the video encoder 130 through a connection 137.

[0041] The uplink delay is the delay from the multiplexer 120 to the video encoder 130 and the downlink delay is the delay from the video encoder 130 to the multiplexer 120. The delay model used by a conventional system always assumes the worst possible delay among all connections between the multiplexer and the video encoders. Additional delay is added to take into account the system clock drift. As a result, the system assumes fixed uplink and downlink delays where the uplink delay is the maximum uplink delay between the multiplexer and the video encoders plus the maximum system phase-lock-loop (PLL) clock drift and the downlink delay is the maximum downlink delay between the multiplexer and the video encoders plus the maximum system phase-lock-loop (PLL) clock drift. In one scenario where all video encoders are located in close proximity to the multiplexer except one which is very far away from the multiplexer, all video sources will be subject to long delay according to the delay.

[0042] Figure 2 shows a multiplexing system embodying the present invention where the buffer 225 in the multiplexer 220 and the buffer 235 associated with the encoder 230 are smaller. As a result, the video data delay is shorter than before. The system shown in Figure 2 estimates the actual delay for uplink and downlink and the estimated actual network delays are used in the roundtrip communication.

[0043] The statistical video multiplexer may be running at a different system clock from that of the video encoders. Furthermore, the statistical video multiplexer may adopt a time interval which is different from the inherent video interval of the video encoder such as a frame or field interval. The time interval or time period for the statistical video multiplexing is designated as the DT period throughout this specification. In order to hide the complexity of video frame and field times from the statistical video multiplexing system, the picture complexities are prorated to DT period complexity. When bitrate information is received, the DT period bitrate is prorated back to picture bitrate values. The relationship between the statistical video multiplexer 310, the proration layer 320, and the video encoder 330 is shown in Figure 3. The encoder 330 sends the picture complexity 325 to the proration layer 320 for proration. The proration layer 320 then prorates the picture complexity 325 into DT period complexity 315 and sends it to the multiplexer 310. The multiplexer 310 communicates the DT period bitrate 317 to the proration layer 320 where the DT period bitrate is converted to picture bitrate 327 for the encoder 330. The proration layer function can be implemented in each individual video encoder. However, it can also be implemented as a separate part associated with each video encoder.

[0044] The details of complexity proration are described as follows. The related parameters are defined first:

- a.  $j^{\text{th}}$  DT period starts before the end of  $i^{\text{th}}$  picture.
- b.  $d = \text{start time of } j^{\text{th}} \text{ DT period} - \text{start time of } i^{\text{th}} \text{ picture.}$
- c.  $DT = \text{duration of DT period.}$
- d.  $PD = \text{Picture Duration.}$
- e.  $CP_i = \text{Complexity for } i^{\text{th}} \text{ picture.}$

[0045] The prorated complexity value for the  $j^{\text{th}}$  DT period  $C_j$  is calculated using the following formula.

$$G = \begin{cases} CP_1 & d+DT < PD \\ \frac{CP_1 \cdot (PD-d) + CP_{i+1} \cdot (d+DT-PD)}{DT} & PD < d+DT < 2PD \\ \frac{CP_1 \cdot (PD-d) + CP_{i+1} \cdot PD + CP_{i+2} \cdot (d+DT-2PD)}{DT} & d+DT > 2PD \end{cases}$$

[0046] The above equation can be easily understood by referring to the drawings in Figures 4A to 4C. Figure 4A illustrates the case  $d+DT < PD$  where the upper row is according to the picture index and the lower row is according to the DT period index. Figure 4B illustrates the case  $PD < d+DT < 2PD$  and Figure 4C illustrates the case  $d+DT > 2PD$ .

[0047] The rate received from the multiplexer needs to be prorated back to picture rates. Similar to the complexity proration, the bitrate proration is described as follows. The related parameters are defined as:

$i^{\text{th}}$  picture starts before the end of  $j^{\text{th}}$  DT period.

$p$  = start time of  $i^{\text{th}}$  picture minus the start time of  $j^{\text{th}}$  DT period.

$DT$  = duration of DT period.

$PD$  = Picture Duration.

$R_j$  = Rate for  $j^{\text{th}}$  DT period.

[0048] The prorated bitrate value for the  $i^{\text{th}}$  picture  $RP_i$  is calculated using the following formula.

$$RP_i = \begin{cases} R_j & p+PD < DT \\ \frac{(DT-P) \cdot R_j + (p+PD-DT) \cdot R_{i+1}}{PD} & DT < p+PD < 2DT \\ \frac{(DT-p) \cdot R_j + DT \cdot R_{i+1} + (p+PD-2DT) \cdot R_{i+2}}{PD} & p+PD > 2DT \end{cases}$$

[0049] The above equation can be easily understood with the help of drawings in Figures 5A to 5C. Figure 5A illustrates the case  $p+PD < DT$  where the upper row is according to the picture

index and the lower row is according to the DT period index. Figure 5B illustrates the case  $DT < p+PD < 2DT$  and Figure 5C illustrates the case  $p+PD > 2DT$ .

[0050] Encoders send complexity messages to the multiplexer using a protocol defined elsewhere in this specification (infra). The picture statistics are prorated to DT period statistics. DT period complexity information is then assigned a complexity index value and sent to the multiplexer in DT period intervals. Based on round-trip delay between the encoder and the multiplexer, up to 4 more look-ahead complexity values can also be sent to the multiplexer in the same complexity message. While the maximum look-ahead information used here is 4 DT periods, it is understood that this is just one exemplary case to illustrate the operation of the statistical multiplexing system and that the present invention is not limited by this particular maximum DT look ahead number.

[0051] The multiplexer keeps queues of complexity information bins as shown in Figure 6 where each row represents the bins corresponding to a DT period. For example, row 601 corresponds to bins at the  $n^{th}$  DT period, row 611 corresponds to bins at the  $(n+1)^{*}$  DT period, and row 621 corresponds to bins at the  $(n-1)^{*}$  DT period. Each bin has space for complexity information from up to 64 encoders. When the complexities from all active encoders have been received for a bin, the rate can be calculated and sent to the encoders.

[0052] The complexity index is used to place the complexity information in the correct queue location.

[0053] The other queues keep information for future (look-ahead) complexities. For example, for the  $n^{th}$  DT period, bin 602 keeps the main complexity information, bin 604 keeps the first look-ahead information, bin 606 keeps the second look-ahead information, bin 608 keeps the third look-ahead information, and bin 610 keeps the fourth look-ahead information. Similarly, bins 612 to 620 keep the respective information for the  $(n+1)^{th}$  DT period and bins 622-630 keep the respective information for the  $(n-1)^{*}$  DT period.

[0054] The multiplexer has a timer that executes a function in DT period intervals. Each DT period has a bin number associated with it. Current bin number refers to the bin number for

current DT period and is the one that keeps all the complexity information used to calculate the rate for current DT period.

[0055] When the first complexity information from an encoder arrives at the multiplexer, it needs to go to a bin. The initial bin is selected according to the following formula:

$$\text{InitialBin} = \text{CurBin} + (\text{RxTime} - \text{CurDtPeriodStartTime} + 2 * \text{MaxJitter}) / \text{DtPeriod},$$

[0056] where CurBin is the bin associated with the DtPeriod in which the complexity message was received, RxTime is the arrival time of complexity message, CurDtPeriodStartTime is the start time of current DtPeriod (The DT period in which the complexity message was received), and MaxJitter is the maximum network communication jitter. The parameter MaxJitter is a value provisioned by a network management system to the statistical multiplexer.

[0057] The number of active encoders will be incremented after a bin is successfully assigned to the first complexity information from an encoder. After the InitialBin is calculated and used, an association between complexity\_index and bin numbers (or DT periods) is created. This association remains in effect as long as the connection between multiplexer and encoder exists.

[0058] A rate message will be created and sent when the last complexity message for that DT period is received. In normal cases this will be before the end of DT period. If the complexity message from one or more encoders is not received until the end of a DT period, a rate message will be created and sent at the end of the DT period. Any complexity message received for that bin after this time is considered late. The main complexity in the message is discarded, but the look-ahead complexities can still be used.

[0059] When calculating the rate for the encoders for which no complexity message was received, the multiplexer will use the nearest look-ahead information if it is available. If a look-ahead complexity is not available, the previous complexity information is used. If the complexity information for an encoder is not received for x consecutive DT periods, the number of active encoders is decremented and mux goes to the startup state for the encoder.

[0060] The arrival time of each complexity message is stored in the assigned bin with the complexity information. When a rate is calculated, the time\_on\_mux parameter is calculated by

subtracting the arrival time from current time. This parameter indicates the amount of time that a complexity message was waiting in the multiplexer to be used in the rate calculation.

[0061] When creating a rate message the multiplexer also calculates the multiplex time for current DT period as follows:

$$\text{mux\_time} = \text{DtPeriodStart} + \text{MuxRoundTripDelay},$$

where MuxRoundTripDelay is the time from the beginning of current DT period to the time that the first TS packet from each encoder for this DT period is removed from the multiplexer's input buffer and processed for multiplexing. In other words, the first video TS packet created for this DT period will have an HRTP (HRTP is an extension of RTP protocol (RFC-3550) and is used to transfer information between encoders and multiplexers) time stamp equal to mux\_time.

[0062] The parameter MuxRoundTripDelay is a provisioned value calculated based on maximum value of all delays (network, FEC, ...) and maximum omega.

[0063] When creating a rate message the multiplexer also calculates the multiplex time for current DT period as follows:

$$\text{mux\_time} = \text{DtPeriodStart} + \text{MuxRoundTripDelay}$$

where MuxRoundTripDelay is the time from the beginning of current DT period to the time that the first TS packet from each encoder for this DT period is removed from the multiplexer's input buffer and processed for multiplexing. In other words, the first video TS packet created for this DT period will have an HRTP time stamp equal to mux\_time.

[0064] The parameter MuxRoundTripDelay is a provisioned value calculated based on maximum value of all delays such as network delay, Forward Error Correction (FEC) for example, and maximum omega, where omega is defined as the time period measured from the moment that the proration layer gets the rate from the rate queue, prorates it to picture bitrate and sends the bitrate to the coding, to the moment that the IP network receives the first TS packet from the pacing. Pacing is the process of delaying the packets in the output queue of the encoder

and sent them exactly at the time specified for each packet (Packet Timestamp). This process makes sure that the packets are sent evenly over time based on the bitrate.

[0065] When a rate message is received at encoder, it will enter a Rate Queue. The size of the Rate Queue depends on the maximum network delay/jitter allowed for the system and other features such as the ability to reorder out-of-order rate messages.

[0066] The received bitrate information is given to the proration layer. The rate information includes the complexity index that indicates which DT period this rate belongs to. The proration layer converts the DT period bitrate and complexity index to picture bitrate and picture index. The picture bitrate is then passed to the coding chip just before it is going to encode the picture with the specified picture index.

[0067] The bitrate information for the DT period is also given to the packetizer so that it will create the TS packet using the specified bitrate during the specified DT period. The HRTP timestamps of the TS packets are calculated based on the mux\_time value received in the rate message and an increment value that is calculated based on current bitrate. The first packet will have an HRTP time stamp equal to mux\_time. The next packets will have a time stamp equal to mux\_time + increment, mux\_time + 2\*increment, ...

[0068] The timestamp calculation around DT period boundaries is slightly different. It needs to account for the partial packets that pass a DT period boundary. To simplify the above explanation, we assumed that the first packet begins exactly at the start of DT period.

[0069] An exemplary timeline for the statistical multiplexer is shown in Figure 7 where the arrowed line 701 represents the timeline. The first action 702 is the time when the coding chip inside the encoder sends picture statistics to a host processor in the encoder. In action 722, the Proration Layer prorates the picture statistics to DtPeriod complexity info and assigns a complexity\_index to the info. The Complexity message is then sent to the statistical multiplexer in block 704 and received by the multiplexer at time corresponding to block 724. At a certain time 706 that may not be synchronized with the encoder time, the multiplexer may start its current DT period and at the end of the current DT period 708, the multiplexer calculates the rate

and sends the rate message to the encoders that is then received by the encoder at block 710 subject to some upstream network delay. The rate information received by the encoder is stored in the rate queue and the proration layer gets the rate from the rate queue at block 712 subject to some rate queue delay. The proration layer then prorates the received rate information to picture bitrate and sends the bitrate to the coding chip inside the encoder. In block 726, packetizer gets the rate from the rate queue and uses it to packetize the picture data. The packets are then sent to the pacing FPGA. Pacing FPGA is the hardware component used to do the pacing process as defined above.

[0070] The present invention is mainly focused on the statistical multiplexing methods and systems with improved performance. The actual video data being transmitted from video encoders to the multiplexer is not shown in the drawings in Figures 1 and 2. For those skilled in the art, it is well known to produce video data to match the allocated bit rate. The IP (IP is a software subsystem inside encoder that is responsible for all Ethernet network communications.) receives the first TS (Transport Stream) packet from the pacing in block 714, and adjusts HRTP timestamp and sends the packet to the multiplexer in block 728. After downlink delay, the TS packets enter the multiplexer input buffer in block 716 and the multiplexer removes the first TS packet from the input buffer to process in block 718. The timeline in Figure 7 has shown the instances starting with the encoder sending statistics, i.e., picture complexity, and ending with the multiplexer processing the compressed video data, i.e., TS packets. During this period, a full cycle of processing is completed, including the encoders generating the complexity values and sending them to the multiplexer, the multiplexer generating bit rates and communicating them to the encoders, encoders generating video packets according to the bit rate allocated and sending the packets to the multiplexer, and the multiplexer receiving and processing the packets.

#### **[0071] Handling network delay changes**

[0072] As noted above, the delay over IP networks has dynamic characteristics. When network traffic is high, longer delays are likely. Conversely, when network traffic is low, delays are likely to be minimal. These periodic delay changes may be rather frequent. In order to ensure proper system operation, a mechanism to handle the delay changes is needed. The method and system to handle the delay changes are described by way of exemplary cases where three

encoders are used. Those skilled in the art should be able to appreciate the present invention and extend to cases with different numbers of encoders and different network environments.

[0073] Assume that the amount of network delay change in worst case is  $n$  DT periods one way. For example, if in the worst case, network delay changes from 10 ms to 120 ms one way,  $n$  would be 4.

[0074] The round-trip delay used for all LAN encoders is:

$$RTD = RTDbest + n,$$

where the RTDbest is the lowest possible round trip value based on encoders in LAN (Local Area Network) mode with minimum queuing on both Encoder and the multiplexer. In current system RTDbest = 9 field times for NTSC. For encoders on the longest possible network delay the round-trip delay is:

$$RTD = RTDbest + 2n.$$

[0075] Encoders send the complexities as soon as they are available. The multiplexer receives complexities, calculates, and sends the rates as soon as the complexities for all encoders are available for each DT period. For the encoders in LAN mode there will be  $n$  rates available in the rate queue. For the encoders with the longest network delay the rate queue will be almost empty and the rates will arrive just in time to be used.

[0076] When an encoder experiences a network delay change of  $m$  DT periods, the fullness of the rate queue for that encoder changes by  $m$ . In the worst case, the fullness goes from  $n$  to 0.

[0077] Notations:

$C(e,c)$ : The complexity value for encoder  $e$ , for DT period specified by complexity index  $c$ .

$C'(e,c)$ : The look-ahead complexity value for encoder  $e$ , for DT period specified by complexity index  $c$ .

$R(e,c)$ : The rate calculated by the video multiplexer for encoder  $e$ , to be used for DT period specified by complexity index  $c$ .

$R'(e,c)$ : The rate calculated by the video multiplexer for encoder  $e$ , to be used for DT period specified by complexity index  $c$ . This is sent by video multiplexer when it does not receive the main complexity in time for the DT period specified by  $c$ . So it uses the Look-Ahead complexity  $C'(e,c)$  for rate calculation.

[0078] In the following example, some assumptions are made about the system:

- a. The biggest change in the network delay is 4 DT periods. ( $n=4$ ,  $RTDb_{es} \leftarrow 1$ ), and
- b. There are encoders 1, 2, and 3. Encoders 1 and 2 are running in LAN mode (0 network delay). Encoder 3 is running in the longest network delay (4 DT Periods).

[0079] It is understood that the above assumptions are used as an example to describe the system operations. By no means are they intended as limitations of the present invention. Those skilled in the art can easily extend the cases with a different number of encoders and different network environment having different network delays among different encoders.

#### **[0080] Exemplary Case 1: Handling network delay increase**

[0081] In this example we assume that there is a network delay change for Encoder 1. The network delay will increase from 0 to 4 DT periods.

[0082] The states of the three encoders before the change in network delay are shown in Figure 8. The multiplexer part 815 is a part of the multiplexer responsible for handling video encoder #1 810. At the current instance, the multiplexer part 815 uses complexity  $C(1,5)$  just received from the video encoder #1 810 to generate bit rate  $R(1,5)$ . The bit rate  $R(1,5)$  is then sent to the video encoder #1 810 through the uplink network 817. Since there is no network delay, the bit rate  $R(1,5)$  is received and placed into the bit rate queue 812 almost instantly. Video encoder #1 810 now stores bit rates  $R(1,2)$ ,  $R(1,3)$ ,  $R(1,4)$  and  $R(1,5)$  in the rate queue 812. The video encoder #1 calculates complexity  $C(1,6)$  based on  $R(1,1)$  and sends it through network 819 having 0 delay. Video encoder #2 820 operates similarly to video encoder #1 810. Video encoder #2 includes a rate queue 822, receives bit rates through uplink network 827, and sends complexity values through downlink network 829. The multiplexer part 825 handles video encoder #2 820.

[0083] The uplink network 837 and downlink network 839 for video encoder #3 830 to communicate with the multiplexer part 835 are subject to 4 DT periods of network delay as shown in Figure 8. At the current time, 4 bit rates ( $R(3,2)$ ,  $R(3,3)$ ,  $R(3,4)$  and  $R(3,5)$ ) and 4

complexity values (C(3,6), C(3,7), C(3,8) and C(3,9)) are still in transit in the networks. The rate buffer 832 is empty.

[0084] Now the network delay for Encoder 1 changes from 0 to 4 DT periods. The states of encoders after this change are shown in Figure 9 at 1 DT period after the states of Figure 8. Unlike the instance of Figure 8, the networks for the video encoder #1 810 are now subject to network delay. As shown in Figure 9, the multiplexer part 815 could not receive the main complexity value C(1,6) on time and has to use the look-ahead complexity value C(1, 6) previously received to calculate the bit rate. Since the bit rate is based on a look-ahead complexity value instead of the main complexity value, the bit rate is designated as R'(1,6). Due to network delay, bit rate R'(1,6) is in the queue of unlink network 917. For video encoder #2 820 and video encoder #3 830, they both function as before.

[0085] The network change for video encoder #1 810 will cause its operations to remain in a transitional stage for a few DT periods. The states associated with video encoder #1 810 during the next 4 DT periods are shown in Figures 10 A-D. From Figure 10A to Figure 10C, the queues for bit rates and complexity values grow from 2 values to full queue. Figure 10D shows the video encoder #1 810 starts to receive delayed bit rate R'(1,6) and to create complexity value based on the R'(1,6).

[0086] At the same time, the video encoder #1 810 notices that the bit rate buffer becomes empty from full and needs to create complexity value having an index further into the future to accommodate the new network delay. So it detects the network delay change and instead of creating the next complexity C(I<sub>5</sub>11), it creates the complexity in future C(1, 15). The RTD for this encoder changes from 5 to 9 DT periods. The states of encoders after this are shown in Figure 11. While the video encoder #1 810 sends the complexity value C(1, 15) having a new complexity index 15, C(1, 15) is queued due to network delay and the multiplexer will not receive it until another 3 DT periods later. Before the timely complexity value is received, the multiplexer will have to continue using the look-ahead complexity values as shown in Figures 12A-12D. Figures 12A-12D show 4 consecutive states associated with the video encoder #1 810. In Figure 12A, the complexity value C(1, 15) moved further down toward the multiplexer from the states corresponding to Figure 11. In the bottom drawing of Figure 12D, the

complexity value  $C(1, 15)$  finally goes through the network delay and is used by the multiplexer to generate bit rate  $R(1, 15)$ . Up to this moment, the multiplexer has been generating bit rates based on look-ahead complexity values.

[0087] It will take 4 more DT periods until Encoder #1 receives the rate  $R(1, 15)$  which is calculated based on a main complexity value. After that, the system state becomes stable and everything works normally. From this point until another new network delay, there is no change in the behavior of Mux or other encoders.

#### **[0088] Exemplary Case 2: Handling network delay decrease**

[0089] When the network delay decreases, some processing will be required for both the encoder side and the multiplexer side to ensure correct operations. Again, an exemplary case is used to illustrate the steps for embodying the present invention. It is understood that the exemplary case is used mainly to illustrate the steps involved in the current invention. By no means is the exemplary case intended as a limitation to the present invention.

[0090] The states associated with the three encoders before the network delay change is shown in Figure 8. Starting with initial state, now assume that there is a network delay change for Encoder 3. Now the network delay for Encoder 3 changes from 4 to 1 DT period. Depending on how the network devices handle this situation, this change may cause reordering of rate and complexity messages. The states of encoders after this change are shown in Figure 13 for the instance at 1 DT period after the network delay change. As shown in Figure 13, the previous bit rates  $R(3,3)$ ,  $R(3,4)$  and  $R(3,5)$  are still queued in the network while the just-sent bit rate  $R(3,6)$  is also in the uplink network queue 1337 during the transition. Similarly, the previously sent complexity values  $C(3,7)$ ,  $C(3,8)$ , and  $C(3,9)$  and the just-sent complexity value  $C(3,10)$  are all in the downlink network queue 1339.

[0091] In the next DT period, encoder 3 receives rates  $R(3,3)$  and  $R(3,6)$ . The rate  $R(3,3)$  is just in time to be used by the encoder for coding the underlying video source.  $R(3,6)$  is too early to use it and it stays in the rate queue 832 as shown in Fig. 14A. Also mux will receive the complexity messages  $C(3,7)$  and  $C(3,10)$ .  $C(3,7)$  will be used for rate calculation.  $C(3,10)$  is too early and it will go to its related bin and wait until the rate calculation time for that period. The

state of Encoder #3 for the next 2 DT periods are shown in Figure 14B and Figure 14C respectively.

[0092] Now the change in the network delay is complete. The video encoder stays in this mode for some time to make sure the network delay is stable. In the interim, it notices an increase in the value of time\_on\_mux received in the rate messages R(3,10) , and later as shown in Figure 15.

[0093] Then, at the next DT period, the encoder sends the complexities later to ensure better video quality. So instead of creating next complexity C(3,16) it will create a better instance of C(3,13) as shown in Figure 16A. This results in a change in the round-trip delay for this encoder from 9 to 6. As noted, at this time the video multiplexer already has the look-ahead version of complexity for C(3,13). When the multiplexer receives a complexity for a bin, it will overwrite the existing values with new values. The states associated with video Encoder #3 830 for the next two DT periods are shown in Figures 16B and 16C respectively. Now, everything continues as normal. The value of time\_on\_mux goes back to normal after the rate R(3,13).

#### **[0094] Handling complexity message problems at the multiplexer**

[0095] If the multiplexer does not receive the complexity message from an encoder by the end of current DT period, it will use the nearest look-ahead complexity information for rate calculations. In the rate message the value of time\_on\_mux is set to 0xFFFF and the bit downstream\_cable\_problem is set in rate\_flags to indicate that the multiplexer did not receive a complexity for this DT period and the calculated rate is an estimation based on look-ahead complexity. An event will also be added to the multiplexer's event log.

[0096] If look-ahead complexity information is not available for the encoder, the multiplexer will use previous complexity to calculate the rate and sets the time\_on\_mux to 0xFFFFD.

[0097] If after x DT periods the multiplexer still is not receiving complexity information from the encoder, it will go to startup state for that encoder. This means a nominal bitrate is allocated for that encoder in rate calculation until a communication is established again. The value of x must be more than the maximum number of DT periods it takes for the encoder to detect a

network delay change and start sending complexities earlier. For a maximum round-trip delay of 300 msec, we can use x=20.

[0098] If the complexity messages are received after the end current DT period, the main complexity in the message cannot be used but the look-ahead complexities can still be used. If the complexity messages continue to arrive late the multiplexer keeps using look-ahead (or previous) complexities, until the number of late/lost complexities exceeds x. Please note that it is the responsibility of the encoder to send the complexities earlier so that the multiplexer does not try to fix the problem of late complexity messages.

[0099] If a complexity message is received too early, the video multiplexer will put the information in the next bins. This can happen when there is a network delay change. If the network delay is decreasing, the video multiplexer will probably receive a better complexity for the same bin in future.

#### **[00100] Handling rate message problems at encoder**

[00101] Encoders have a rate queue that stores received rate messages before they are used by the coding chip and the packetizer. If a single rate message is lost and the depth of queue is more than one, the next rate message will fix the problem because it will include the previous rate information. So we can update the rate queue before the rate is needed by the coding.

[00102] If the encoder does not receive the rate message in time for the coding, it will use the look-ahead sum of complexities that was received in the earlier rate messages to calculate a bitrate. If the look-ahead sum of complexities is not available, the encoder uses the previous sum of complexities to calculate an estimated bitrate. In each bitrate message, the encoder always receives the global information (including sum of bitrates, sum of complexities ...) for previous and current DT Periods. In normal cases it also receives look ahead global information (Future DT Periods).

[00103] Previous sum of complexities in this sentence refers to the value of sum of complexities received in the previous rate message. This bitrate will be given to the coding chip.

[00104] If the bitrate is received after the estimated bitrate was send to the coding, but before the packetizer needs the bitrate, the real bitrate received from mux will be used by the

packetizer. The VBV correction will then make up for the difference between the bitrates used by the coding chip and the packetizer.

[00105] When a rate message is lost, the bit upstream\_cable\_problem in the complexity\_flags parameter is set in the next complexity message sent to the multiplexer. If the rate message is not received in time for a second consecutive time, the encoder will use the nominal bitrate for both coding and packetizer and will generate an alarm indicating the upstream connection was lost. The encoder keeps using the nominal rate in CBR mode until it starts receiving rate message again.

[00106] If a rate message is received too early, it just stays in the rate queue. The rate queue is an ordered queue; if the rate messages are received out of order, they will be reordered as they enter the queue.

#### **[00107] Handling large network Jitters**

[00108] As explained earlier, the InitialBin assigned to the first complexity message received from an encoder depends on the maximum network jitter .

$$\text{InitialBin} = \text{CurBin} + (\text{RxTime} - \text{CurDtPeriodStartTime} + 2*\text{MaxJitter})/\text{DtPeriod}$$

[00109] As network jitter increases, the InitialBin will be farther in future compared to CurBin. This works as a complexity queue for the multiplexer and compensates for the big changes in the arrival time of complexities. For example, if maximum one way network jitter is equal to one DtPeriod, the maximum difference between the arrival time of 2 complexity messages is 2 DtPeriods. In this case the InitialBin assigned for the first complexity info will be (CurBin + 2).

#### **[00110] Time Synchronization**

[00111] The encoders and multiplexers share a common 27 MHz clock for synchronization of all participating devices in the statistical video multiplexing system. There are two ways time is distributed to the encoders from the multiplexer, the rate message and the STC (System Time Clock) pool message. The actual mechanism is based on the arrival time of

the message over IP, measured with the encoder's local 27MHz mux clock (not locked to the video source) and a PLL filter algorithm that measures differences in these two clocks over time.

[001 12] One subtle point above is that the clock locking mechanism relies on the timestamp of the STC pool or rate message to be sent with low latency and high accuracy from the multiplexer HW. The video encoders may use the timestamp of the rate messages to recover the clock, which puts a requirement on the system that rate messages for video encoders must be sent with accurate timestamps (not early). Another requirement for the video encoders is that the rate message size is limited to 188 bytes including the MPEG2 transport header. Some video encoders can receive both messages, so their dependency is only on the STC pool message.

[001 13] It is another goal of the present invention to detect network delay changes so as to enable the required management for bit rate and complexity value buffers. Accordingly, a new Phase Locked Loop (PLL) algorithm is described here. The new algorithm is capable of cancelling the effects of network jitter significantly and locking to the master frequency faster. This algorithm is based on averaging the network delay over time and then using the growth seen in the network delays on the encoder side to estimate the difference between the encoder's frequency and that of the master clock (In this case multiplexer's clock).

[001 14] This algorithm uses different stages to lock faster. At initial stages we need to find the direction of changes as fast as possible. The accuracy of the PLL drift value is not of critical importance here. As time passes the differences grow enough to estimate the value of PLL drift more accurately. Initial simulations indicate that this algorithm reaches the master frequency faster with less overshoots.

[001 15] The relationship between values of the encoder's multiplexing clock (y) and multiplexer's clock (x) at the time  $j^{\text{th}}$  PLL message is sent is given by the following equation:

$$y_j = m \cdot X_j + h$$

where:

$$m = f_s/f_m$$

$f_s$  : The encoder's multiplexing clock frequency  
 $f_m$  : The multiplexer's clock frequency

[001 16] The value of the encoder's mux clock when the message is received at encoder is:

$$r_J = y_J + N + j_J$$

where  $N$  is the upstream network delay and  $j_j$  is the  $j^{\text{th}}$  network jitter value. The network delay seen by the encoder is:

$$r_i - x_i = y_i + N + j_i - X_i = m \cdot X_i + h + N + j_i - x_i = (m-l) \cdot x_i + h + N + j_i$$

[001 17] The average of last  $K+l$  network delays is:

$$a_i = \frac{\sum_{j=i-K}^i r_j - X_j}{K+l} = \frac{\sum_{j=i-K}^i [(m-l) \cdot x_j + h + N + j_j]}{K+l} = \frac{(K+l)(h+N) + (m-l) \cdot \sum_{j=i-K}^i X_j + \sum_{j=i-K}^i j_j}{K+l}$$

[001 18] By replacing:

$$x_j = x_0 + j \cdot T$$

where  $T$  is the period used by multiplexer to send PLL messages and assuming:

$$\sum_{j=i-K}^i j_j \sim 0$$

[001 19] we will have:

$$a_i = (m-l)(X_0 + i \cdot T + K \cdot T/2) + N + h$$

[00120] The difference between the  $i^{\text{th}}$  and  $j^{\text{th}}$  average is:

$$\begin{aligned} a_i - a_j &= (m-l) \cdot T \cdot (i - j) \\ m &= 1 + (a_i - a_j) / [T \cdot (i - j)] = 1 + (a_i - a_j) / (x_1 - x_j) \\ f_s / f_m &= (X_1 - x_j + a_i - a_j) / (x_1 - X_j) \end{aligned}$$

[00121] The frequency of the encoder's PLL is given by:

$$f_p = f_s + (d/2^{40}) \cdot f_s = f_s \cdot [1 + (d/2^{40})]$$

[00122] where  $d$  is the value in the Drift register.

$$f_s/f_p = 1/[1 + (d/2^{40})]$$

[00123] by setting  $f_p = f_m$  we will have:

$$1/[1 + (d/2^{40})] = (X_1 - X_j + a_1 - a_j)Z(X_I - X_j)$$

[00124] Solving for d:

$$d = - [(a_i - a_j) \cdot 2^{40}] / (X_1 - X_j + a_1 - a_j)$$

[00125] As we can see this equation is independent of network delay and (almost) network jitter.

[00126] At startup the encoder simply listens to the PLL messages from mux and calculates the average of K+1 network delays. After having K+1 messages, we initialize the PLL value with:  $x_i + a_i$ . Where  $x_i$  is the value of the mux clock in the  $i^{\text{th}}$  received message and  $a_i$  is the average of last K+1 network delays at that time.

[00127] To calculate the Drift register value, the encoder calculates the average of the last K+1 network delays at two different times i and j. The accuracy of the calculated Drift register value improves as the difference between i and j grows. At startup, this difference is small in order to start moving to the right direction as soon as possible. As time passes, the difference between i and j is increased to get a better estimation of the difference between the frequencies and therefore a better value for the Drift register. With higher network jitter values, the simulated PLL software shows that averaging the drift register values can result in more stable PLL frequency.

[00128] After running this algorithm for a few hours, we will have the average of values for the drift register. At this time we can add the drift register value to a data base. This data base is a lookup table of drift registers and mux's Mac addresses. The next time the PPL starts, the encoder can look up the initial drift value from this database. The encoder keeps updating the database periodically as long as the network delay is stable.

[00129] A change in the network delay can be detected immediately by comparing the delay for each message to the calculated average network delays. When a change in the network delay is detected, this algorithm stops updating the drift value, and restarts calculation of its

average network delays. Therefore the PLL continues with current drift value until we have a stable network delay.

[00130] The detected change in the network delay is also reported to the video multiplexer controller on the encoder. The video multiplexer controller uses this information to decide if it should send the complexities earlier or later. In this algorithm the PLL does not try to compensate for the extra phase difference between encoder's PLL and mux's clock by slewing the frequency.

## CLAIMS

1. A method of video multiplexing for a multiplexing system having a video multiplexer and a plurality of video encoders, the method comprising:
  - communicating a bit rate for a time period from the video multiplexer to each of the plurality of video encoders;
  - receiving the bit rate by each of the plurality of video encoders using a first buffer;
  - determining a complexity index corresponding to a future time period according to a status of the first buffer by each of the plurality of video encoders;
  - calculating a main complexity value and at least one look-ahead complexity value corresponding to the complexity index according to the status of the first buffer by each of the plurality of video encoders;
  - communicating the main complexity value and the at least one look-ahead complexity value from each of the plurality of video encoders to the video multiplexer;
  - receiving the main complexity value and the at least one look-ahead complexity value by the video multiplexer using a second buffer; and
  - determining a bit rate for a next time period according to a status of the second buffer.
2. The method of claim 1, wherein the bit rate for the time period is prorated to a picture bit rate for a picture period.
3. The method of claim 2, wherein the picture period is a field period.
4. The method of claim 2, wherein the picture period is a frame period.
5. The method of claim 1, wherein the main complexity value and the at least one look-ahead complexity value are prorated from one or more picture complexity values.
6. The method of claim 5, wherein the picture complexity value is measured for a field period.
7. The method of claim 5, wherein the picture complexity value is measured for a frame period.

8. The method of claim 1, wherein the determining a bit rate for the next time period includes data associated with a nearest look ahead complexity value if no main complexity value is received for the time period.
9. The method of claim 8, wherein the determining a bit rate for the next time period includes data associated with a previous main complexity value if no look ahead complexity value is available.
10. The method of claim 9, wherein the video multiplexer enters into a start up state if the main complexity value and the at least one look-ahead complexity value are not received more than a number of times exceeding a threshold.
11. The method of claim 1, wherein the first buffer has a size equal to a maximum network delay change.
12. The method of claim 11, wherein a rate message from the video multiplexer to each of the plurality video encoders is included to manage the first buffer.
13. The method of claim 12, wherein fullness of the first buffer is determined according to data including a current network delay change and the maximum network delay change.
14. The method of claim 11, wherein the complexity index includes data associated with the time period and a round-trip network delay.
15. The method of claim 12, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a look-ahead sum of complexities in the rate message if the bit rate for the time period is not available.
16. The method of claim 15, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated

with a previous look-ahead sum of complexities if the look-ahead sum of complexities is not available.

17. The method of claim 15, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a nominal bit rate if the rate message is not received in time for a second consecutive time.
18. The method of claim 12, wherein the rate message stays in the first buffer if the rate message is received too early.
19. A method of video multiplexing for a video multiplexer, the method comprising:
  - communicating a bit rate for a time period from the video multiplexer to each of a plurality of video encoders;
  - receiving a main complexity value and at least one look-ahead complexity value corresponding to a future time period from each of the plurality of video encoders using a buffer; and
  - determining a bit rate for a next first time period according to a status of the buffer.
20. The method of claim 19, wherein the determining a bit rate for the next time period includes data associated with a nearest look ahead complexity value if no main complexity value is received for the time period.
21. The method of claim 20, wherein the determining a bit rate for the next time period includes data associated with a previous main complexity value if no look ahead complexity value is available.
22. The method of claim 21, wherein the video multiplexer enters into a start up state if the main complexity value and the at least one look-ahead complexity value are not received more than a number of times exceeding a threshold.
23. A method of video multiplexing for a plurality of video encoders, the method comprising:

receiving from a video multiplexer a bit rate for a time period by each of the plurality of video encoders using a first buffer;

determining a complexity index corresponding to a future time period according to a status of the first buffer by each of the plurality of video encoders;

calculating a main complexity value and at least one look-ahead complexity value corresponding to the complexity index according to the status of the first buffer by each of the plurality of video encoders; and

communicating the main complexity value and the at least one look-ahead complexity value from each of the plurality of video encoders to the video multiplexer.

24. The method of claim 23, wherein the bit rate for the time period is prorated to a picture bit rate for a picture period.

25. The method of claim 24, wherein the picture period is a field period.

26. The method of claim 24, wherein the picture period is a frame period.

27. The method of claim 23, wherein the main complexity value and the at least one look-ahead complexity value are prorated from one or more picture complexity values.

28. The method of claim 26, wherein the picture complexity value is measured for a field period.

29. The method of claim 26, wherein the picture complexity value is measured for a frame period.

30. The method of claim 23, wherein the first buffer has a size equal to a maximum network delay change.

31. The method of claim 30, wherein a rate message from the video multiplexer to each of the plurality video encoders is included to manage the first buffer.

32. The method of claim 31, wherein fullness of the first buffer is determined according to data including a current network delay change and the maximum network delay change.
33. The method of claim 30, wherein the complexity index is associated with the time period and a round-trip network delay.
34. The method of claim 31, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a look-ahead sum of complexities in the rate message if the bit rate for the time period is not available.
35. The method of claim 34, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a previous look-ahead sum of complexities if the look-ahead sum of complexities is not available.
36. The method of claim 34, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a nominal bit rate if the rate message is not received in time for a second consecutive time.
37. The method of claim 31, wherein the rate message stays in the first buffer if the rate message is received too early.
38. A system for video multiplexing comprising:
  - a video multiplexer having
    - a first interface module,
    - a first buffer, and
    - a first processor; and
  - a plurality of video encoders, wherein each of the plurality of video encoders having
    - a second interface module,
    - a second buffer,
    - a second processor, and

a third processor, wherein

the first interface module is configured to communicate a bit rate for a time period to the second interface module,

the second interface module is configured to receive the bit rate using the second buffer,

the second processor is configured to determine a complexity index corresponding to a future time period according to a status of the second buffer,

the third processor is configured to calculate a main complexity value and at least one look-ahead complexity value corresponding to the complexity index according to the status of the second buffer,

the second interface module is further configured to communicate the main complexity value and the at least one look-ahead complexity value to the first interface module,

the first interface module is further configured to receive the main complexity value and the at least one look-ahead complexity value, and

the first processor is configured to determine a bit rate for a next time period according to a status of the first buffer.

39. The system of claim 38, wherein the bit rate for the time period is prorated to a picture bit rate for a picture period.

40. The system of claim 39, wherein the picture period is a field period.

41. The system of claim 39, wherein the picture period is a frame period.

42. The system of claim 38, wherein the main complexity value and the at least one look-ahead complexity value are prorated from one or more picture complexity values.

43. The system of claim 42, wherein the picture complexity value is measured for a field period.

44. The system of claim 42, wherein the picture complexity value is measured for a frame period.

45. The system of claim 38, wherein the determining a bit rate for the next time period includes data associated with a nearest look ahead complexity value if no main complexity value is received for the time period.
46. The system of claim 45, wherein the determining a bit rate for the next time period includes data associated with a previous main complexity value if no look ahead complexity value is available.
47. The system of claim 46, wherein the video multiplexer enters into a start up state if the main complexity value and the at least one look-ahead complexity value are not received more than a number of times exceeding a threshold.
48. The system of claim 38, wherein the second buffer has a size equal to a maximum network delay change.
49. The system of claim 48, wherein a rate message from the video multiplexer to each of the plurality video encoders is included to manage the second buffer.
50. The system of claim 49, wherein fullness of the second buffer is determined according to data including a current network delay change and the maximum network delay change.
51. The system of claim 48, wherein the complexity index includes data associated with the time period and a round-trip network delay.
52. The system of claim 49, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a look-ahead sum of complexities in the rate message if the bit rate for the time period is not available.
53. The system of claim 52, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated

with a previous look-ahead sum of complexities if the look-ahead sum of complexities is not available.

54. The system of claim 53, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a nominal bit rate if the rate message is not received in time for a second consecutive time.

55. The system of claim 49, wherein the rate message stays in the second buffer if the rate message is received too early.

56. A video multiplexer comprising:

an interface module configured to communicate a bit rate for a time period to each of a plurality of video encoders and to receive a main complexity value and at least one look-ahead complexity value for a future time period from each of the plurality of video encoders;

a buffer configured to store status value data; and

a processor configured to determine a bit rate for a next time period according to a status value of the buffer.

57. The system of claim 56, wherein the determining a bit rate for the next time period includes data associated with a nearest look ahead complexity value if no main complexity value is received for the time period.

58. The system of claim 57, wherein the determining a bit rate for the next time period includes data associated with a previous main complexity value if no look ahead complexity value is available.

59. The system of claim 58, wherein the video multiplexer enters into a start up state if the main complexity value and the at least one look-ahead complexity value are not received more than a number of times exceeding a threshold.

60. A video encoder for a video multiplexing system comprising:

a buffer;

an interface module configured to receive a bit rate for a time period from a video multiplexer using the buffer, and further configured to communicate the main complexity value and the at least one look-ahead complexity value to the video multiplexer<sup>^</sup> first processor configured to determine a complexity index corresponding to a future time period according to a status of the buffer; and

a second processor configured to calculate a main complexity value and at least one look-ahead complexity value corresponding to the complexity index according to the status of the buffer.

61. The system of claim 60, wherein the bit rate for the time period is prorated to a picture bit rate for a picture period.

62. The system of claim 61, wherein the picture period is a field period.

63. The system of claim 61, wherein the picture period is a frame period.

64. The system of claim 60, wherein the main complexity value and the at least one look-ahead complexity value are prorated from one or more picture complexity values.

65. The system of claim 64, wherein the picture complexity value is measured for a field period.

66. The system of claim 64, wherein the picture complexity value is measured for a frame period.

67. The system of claim 66, wherein the second buffer has a size equal to a maximum network delay change.

68. The system of claim 67, wherein a rate message from the video multiplexer to each of the plurality video encoders is included to manage the second buffer.

69. The system of claim 68, wherein fullness of the second buffer is determined according to data including a current network delay change and the maximum network delay change.
70. The system of claim 67, wherein the complexity index includes data associated with the time period and a round-trip network delay.
71. The system of claim 68, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a look-ahead sum of complexities in the rate message if the bit rate for the time period is not available.
72. The system of claim 71, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a previous look-ahead sum of complexities if the look-ahead sum of complexities is not available.
73. The system of claim 53, wherein the calculating the main complexity value and the at least one look-ahead complexity value corresponding to the complexity index includes data associated with a nominal bit rate if the rate message is not received in time for a second consecutive time.
74. The system of claim 71, wherein the rate message stays in the second buffer if the rate message is received too early.

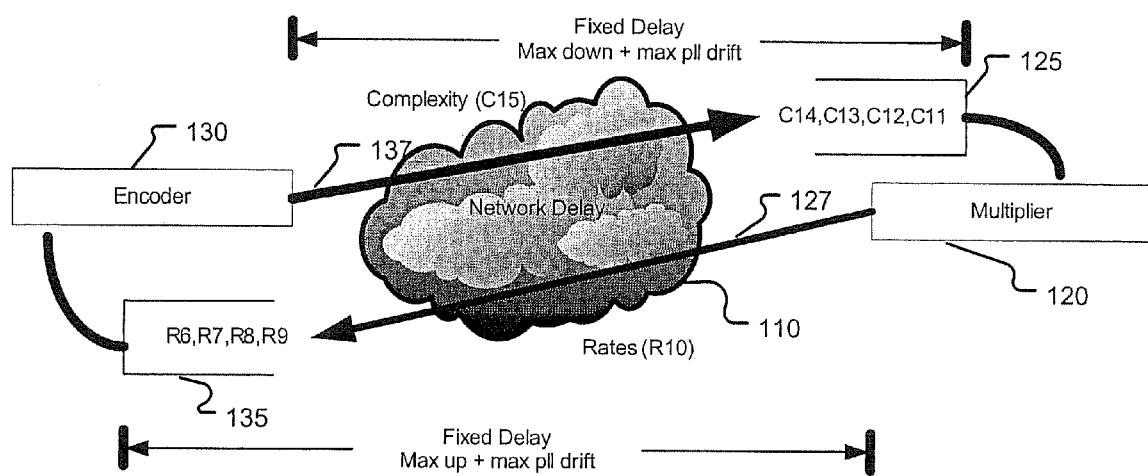


Figure 1

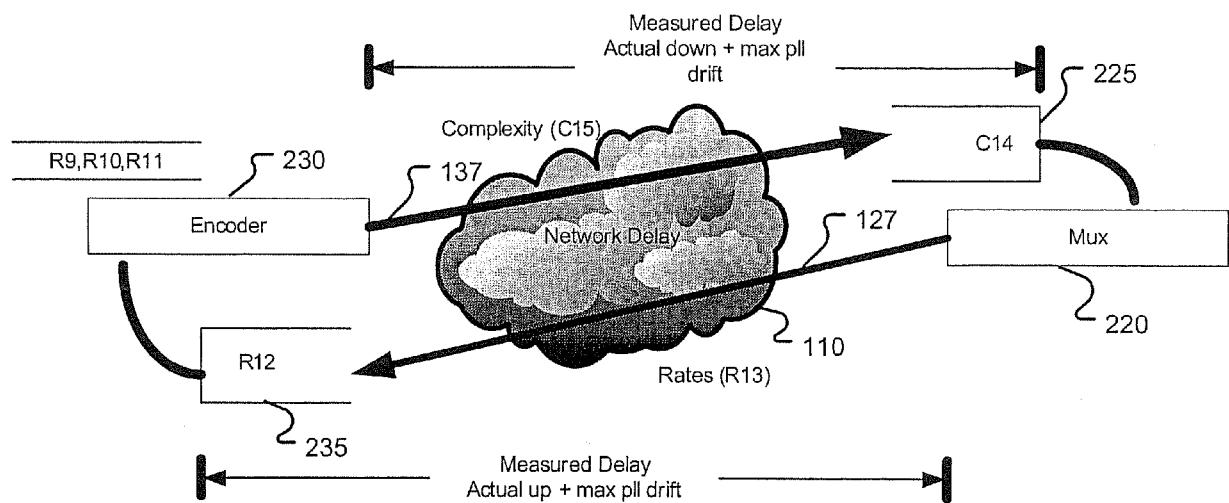


Figure 2

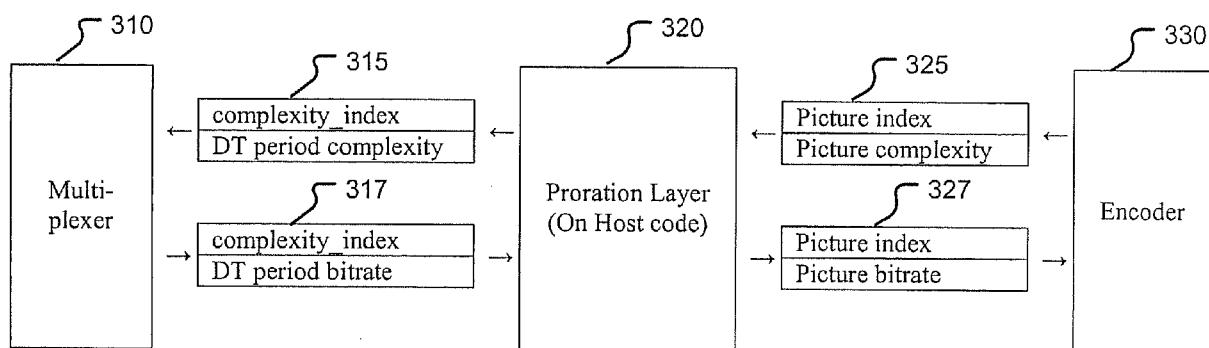


Figure 3

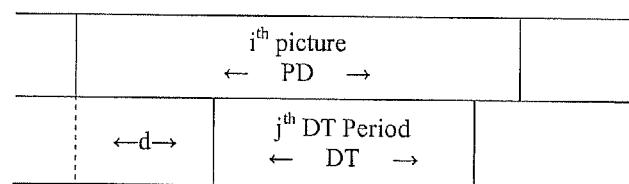


Figure 4A

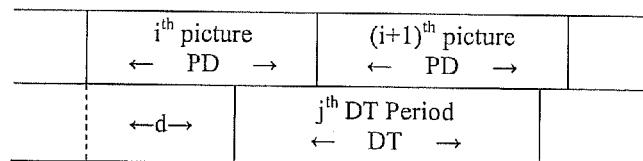


Figure 4B

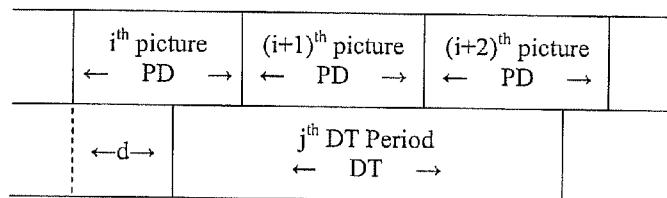


Figure 4C

	↔p↔	$i^{\text{th}}$ picture ↔ PD ↔	
	$j^{\text{th}}$ DT Period ↔ DT ↔		

Figure 5A

	↔p↔	$i^{\text{th}}$ picture ↔ PD ↔	
	$j^{\text{th}}$ DT Period ↔ DT ↔	$(j+1)^{\text{th}}$ DT Period ↔ DT ↔	

Figure 5B

	↔p↔	$i^{\text{th}}$ picture ↔ PD ↔	
	$j^{\text{th}}$ DT Period ↔ DT ↔	$(j+1)^{\text{th}}$ DT Period ↔ DT ↔	$(j+2)^{\text{th}}$ DT Period ↔ DT ↔

Figure 5C

DT Periods	Queue 0 Main complexity information	Queue 1 1 <sup>st</sup> look-ahead complexity information	Queue 2 2 <sup>nd</sup> look-ahead complexity information	Queue 3 3 <sup>rd</sup> look-ahead complexity information	Queue 4 4 <sup>th</sup> look-ahead complexity information
n-1	622 Previous Bin →	624	626	628	630
n (Current DTperiod)	n*DtPeriod = DlPeriodStart → 602 CxInfo 1, CxInfo 2, ...	604 CxInfo 1 (LA1), CxInfo 2 (LA1), ...	606 CxInfo 1 (LA2), CxInfo 2 (LA2), ...	608 CxInfo 1 (LA3), CxInfo 2 (LA3), ...	610 CxInfo 1 (LA4), CxInfo 2 (LA4), ...
n+1	(n+1)*DlPeriod → 612 Next Bin →	614	616	618	620
	(n+2)*DlPeriod →				

Figure 6

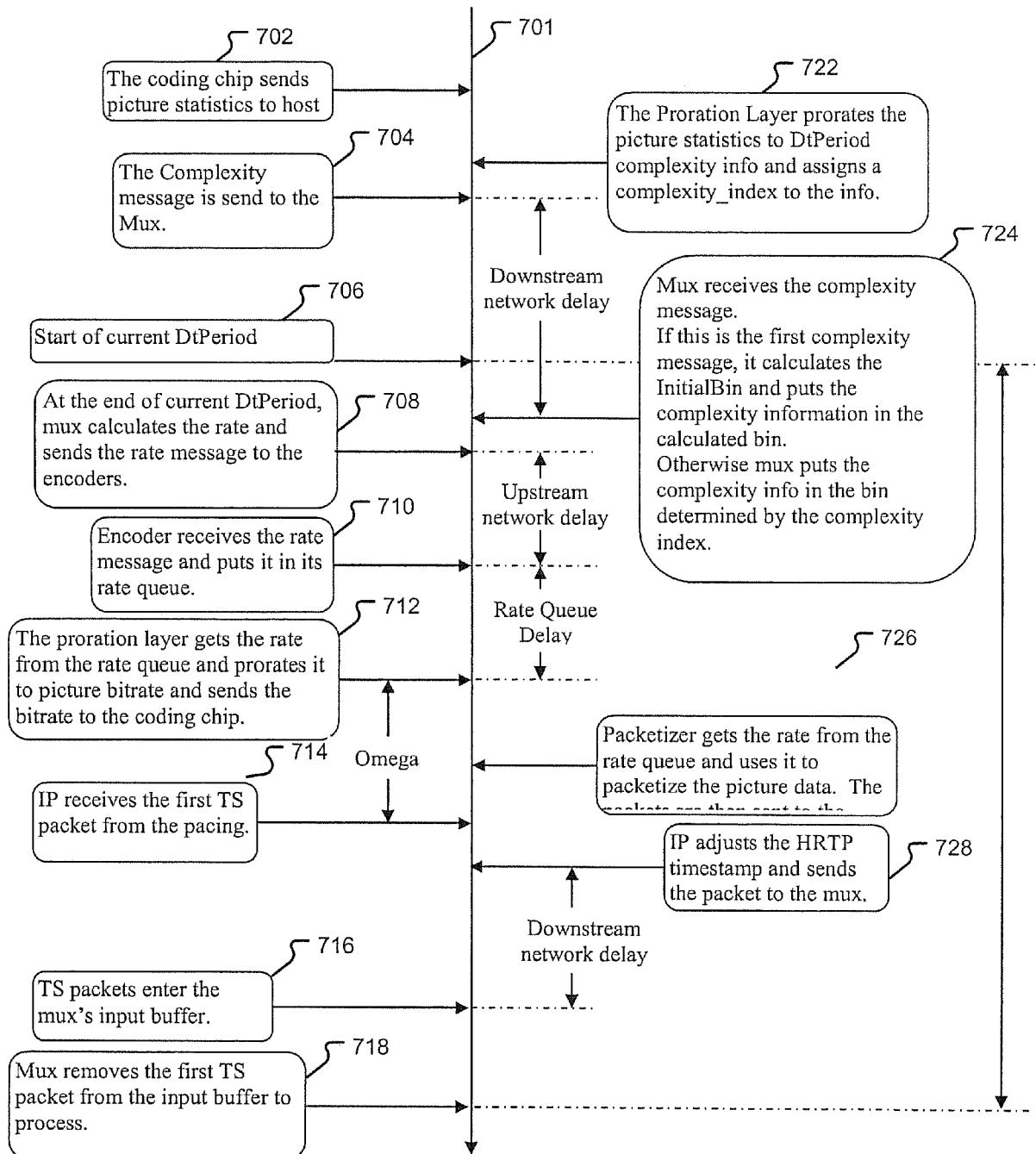


Figure 7

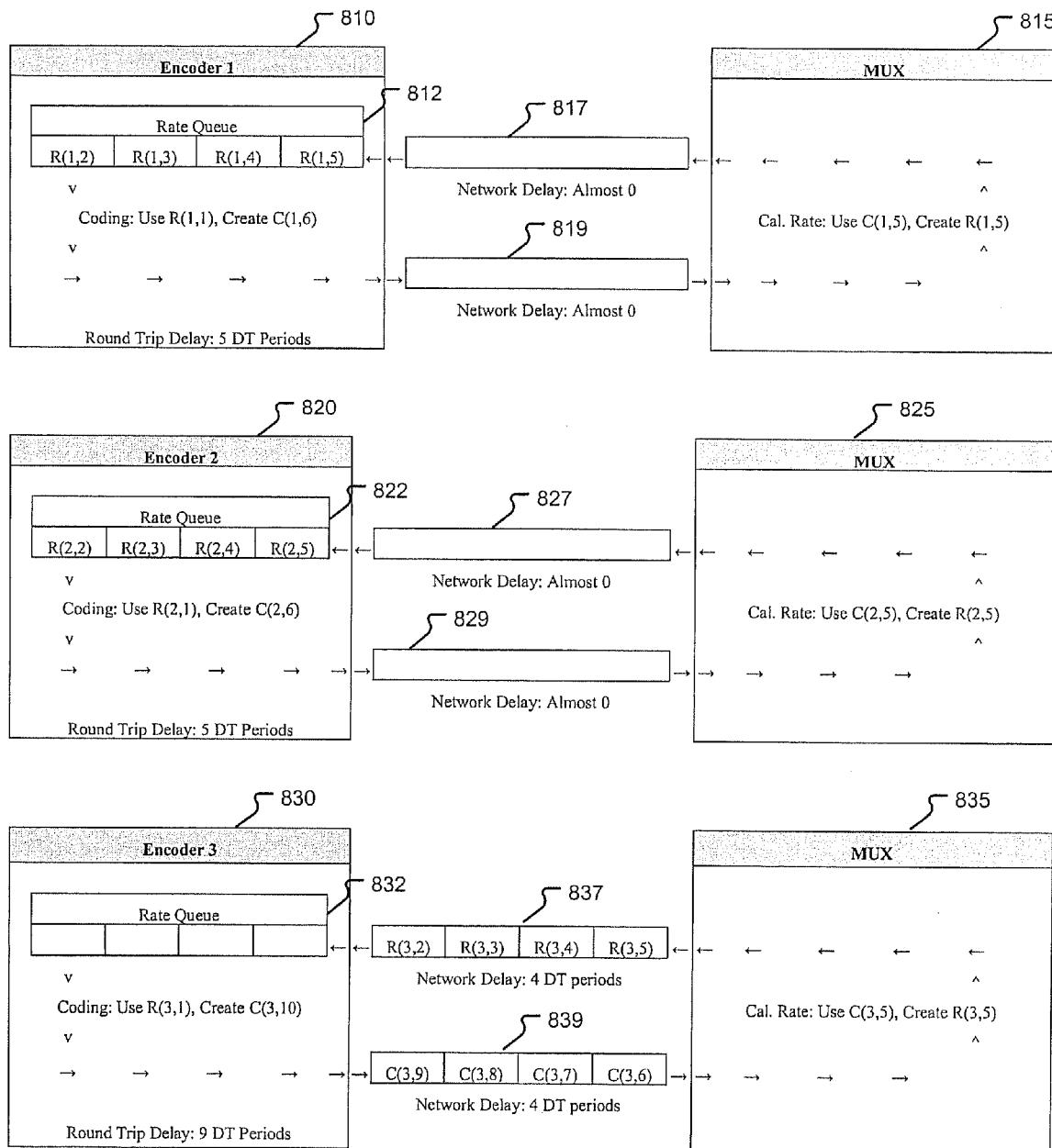


Figure 8

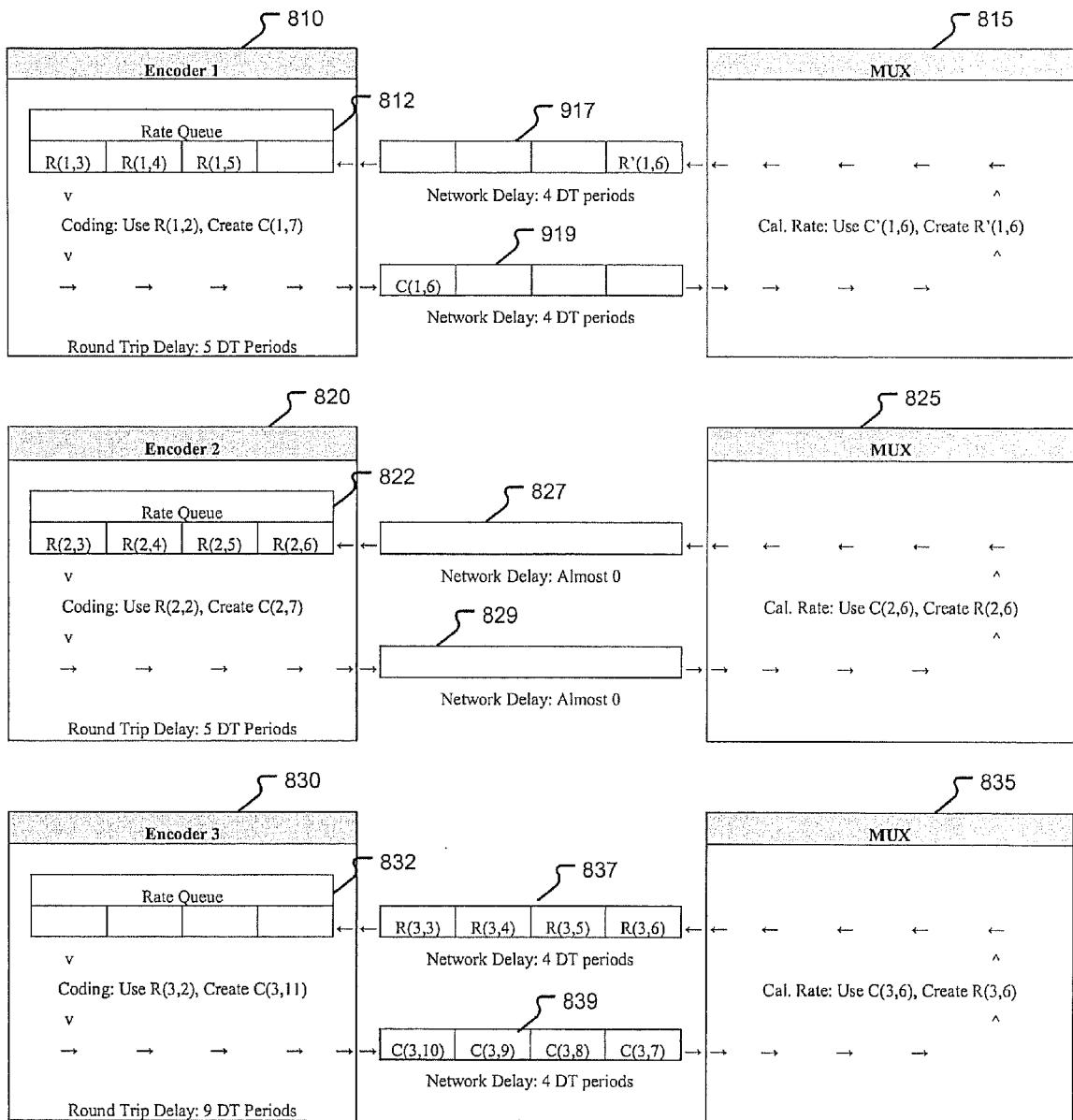


Figure 9

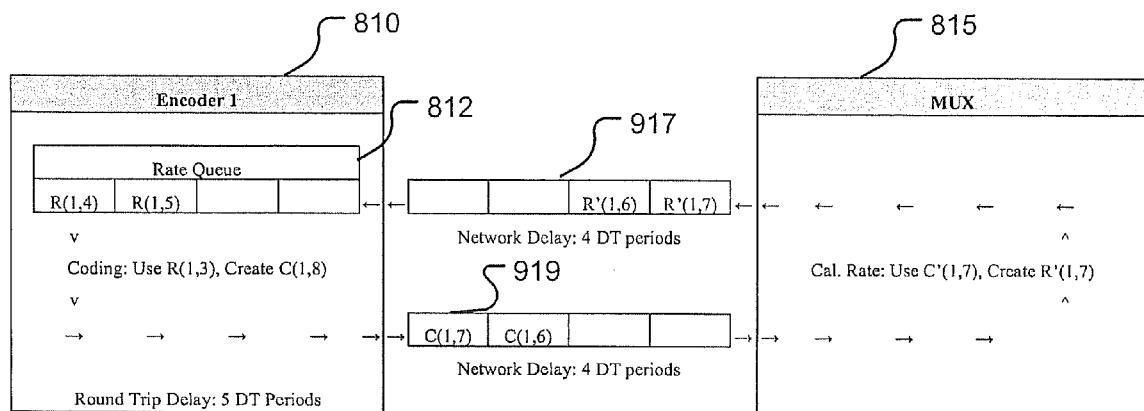


Figure 10A

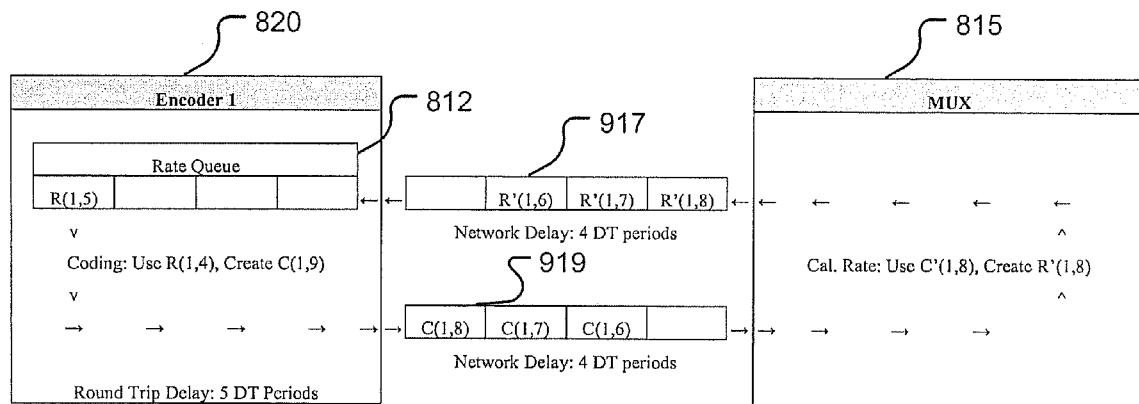


Figure 10B

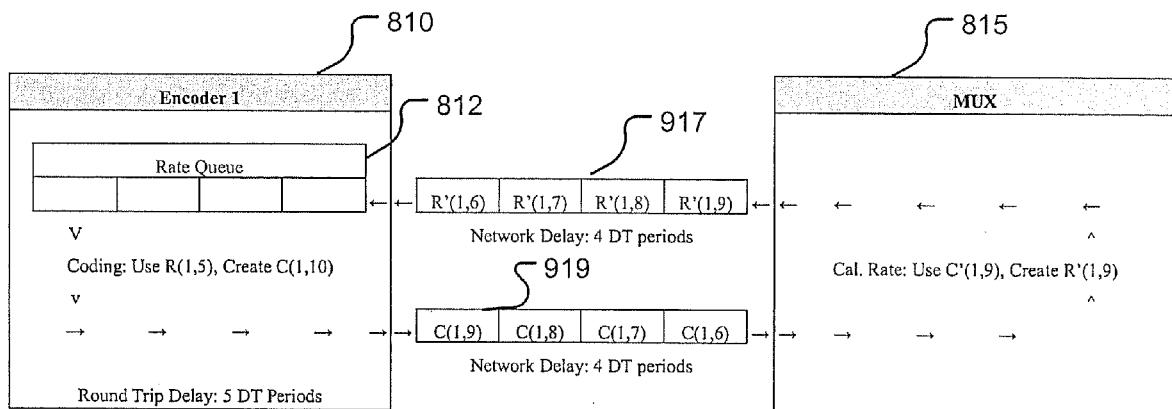


Figure 10C

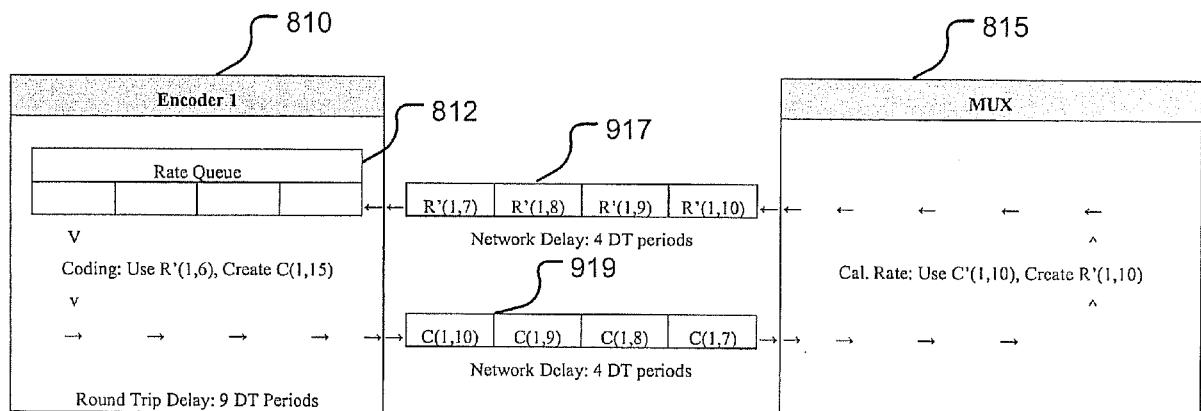


Figure 10D

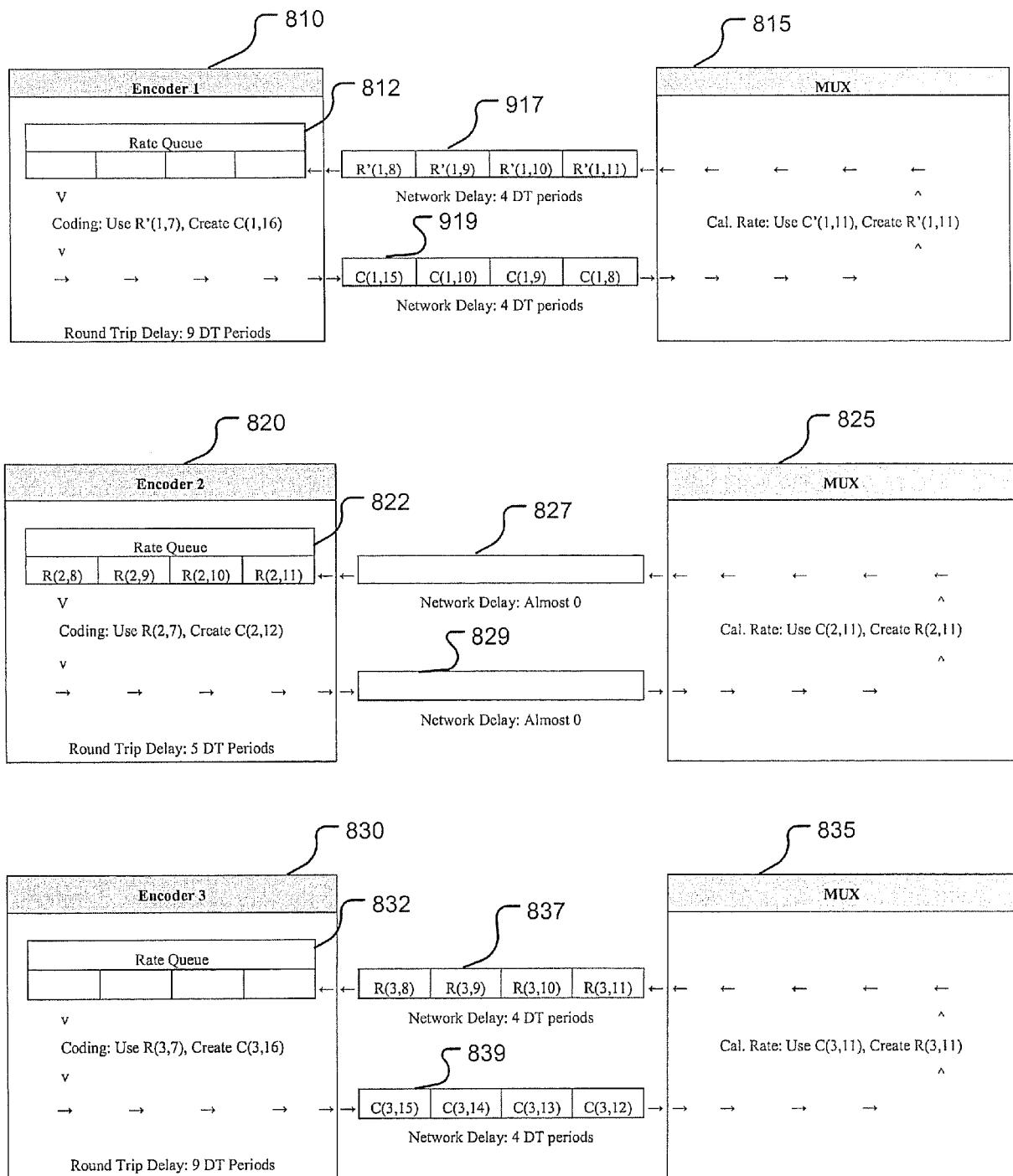


Figure 11

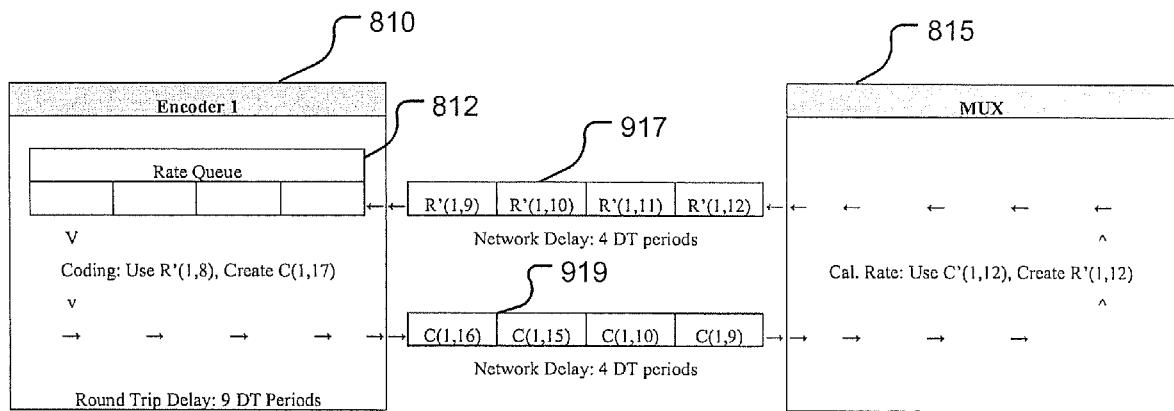


Figure 12A

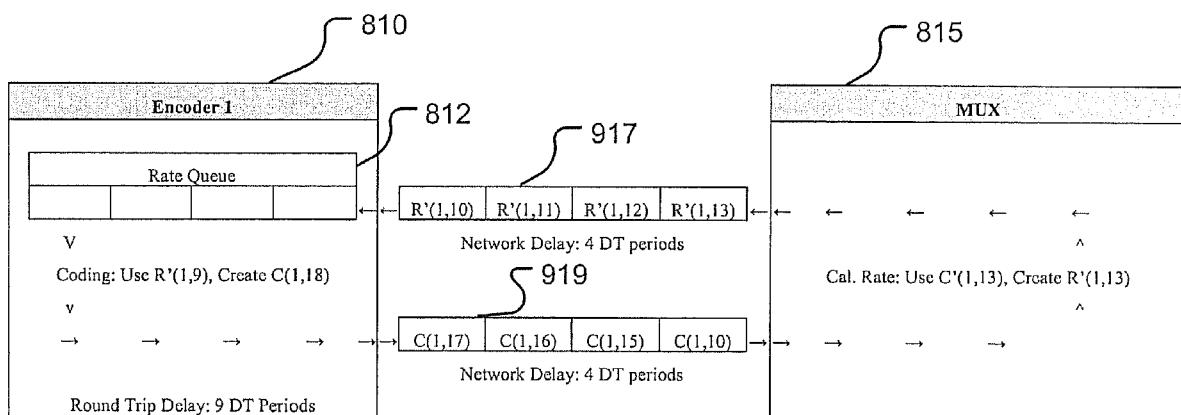


Figure 12B

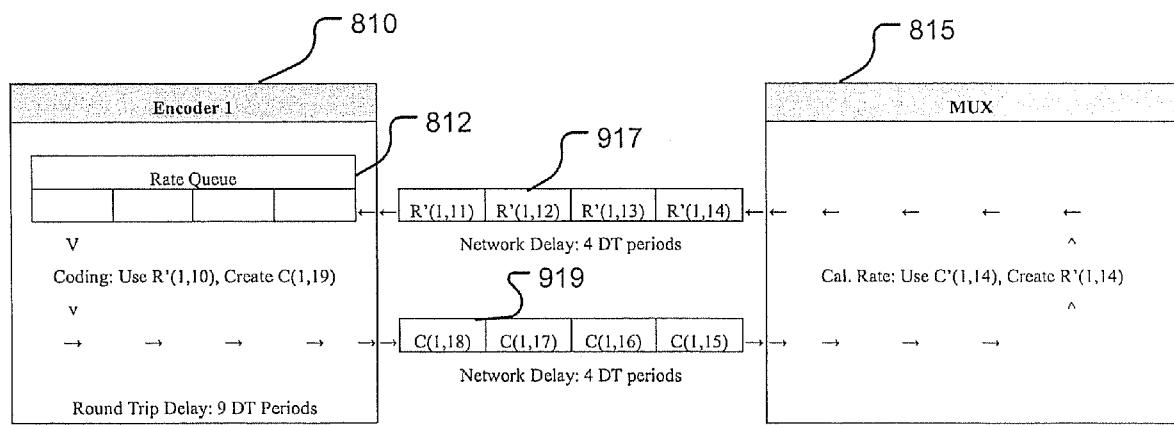


Figure 12C

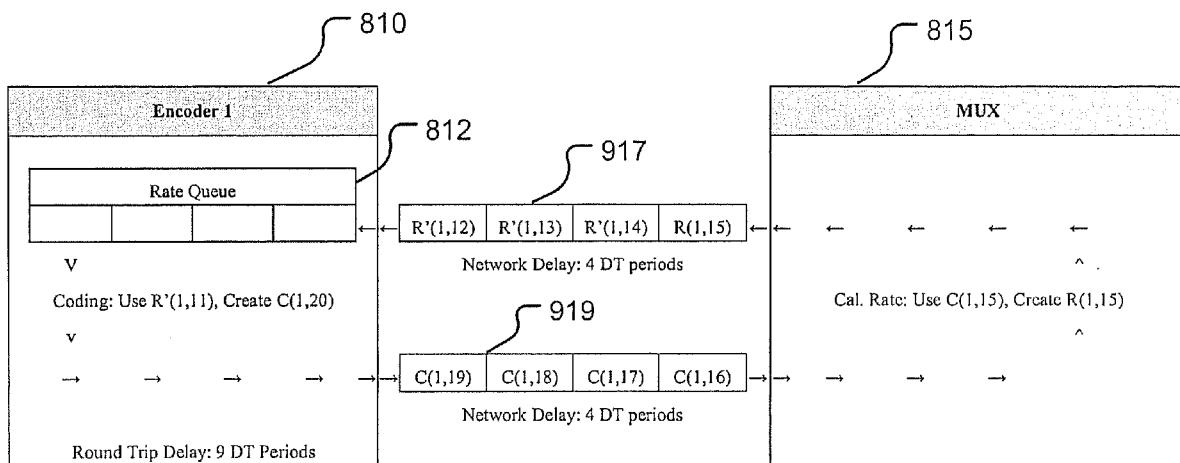


Figure 12D

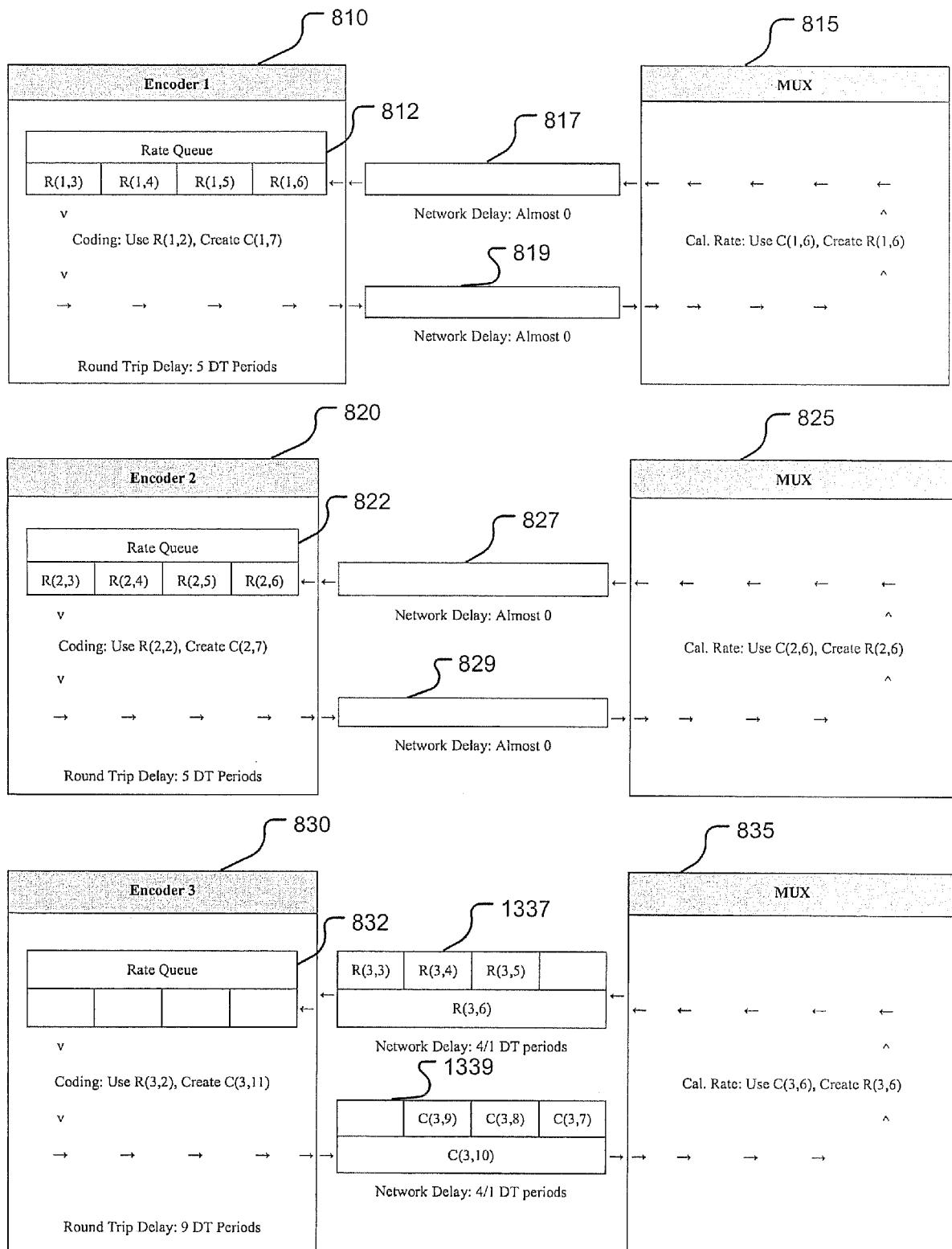


Figure 13

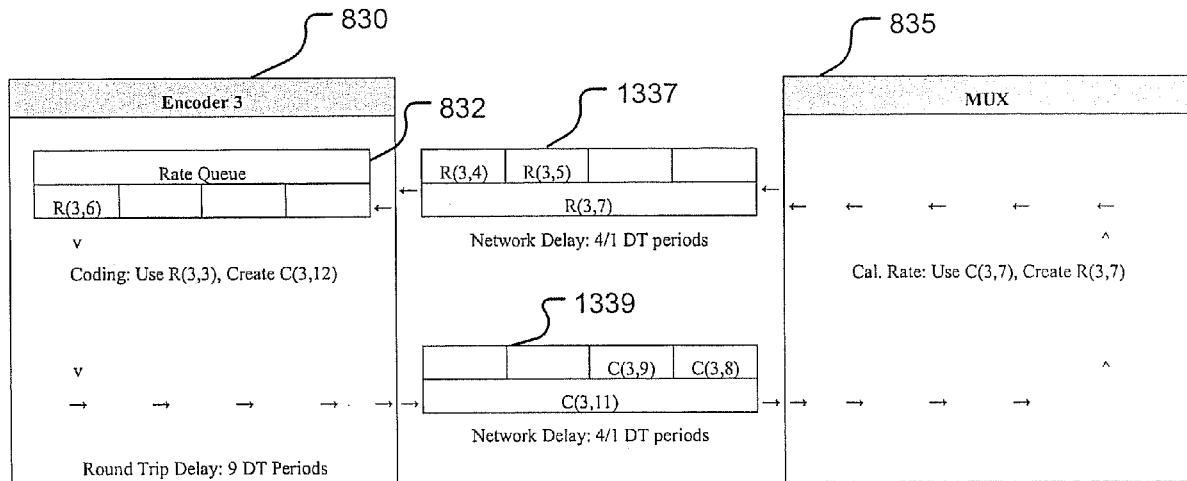


Figure 14A

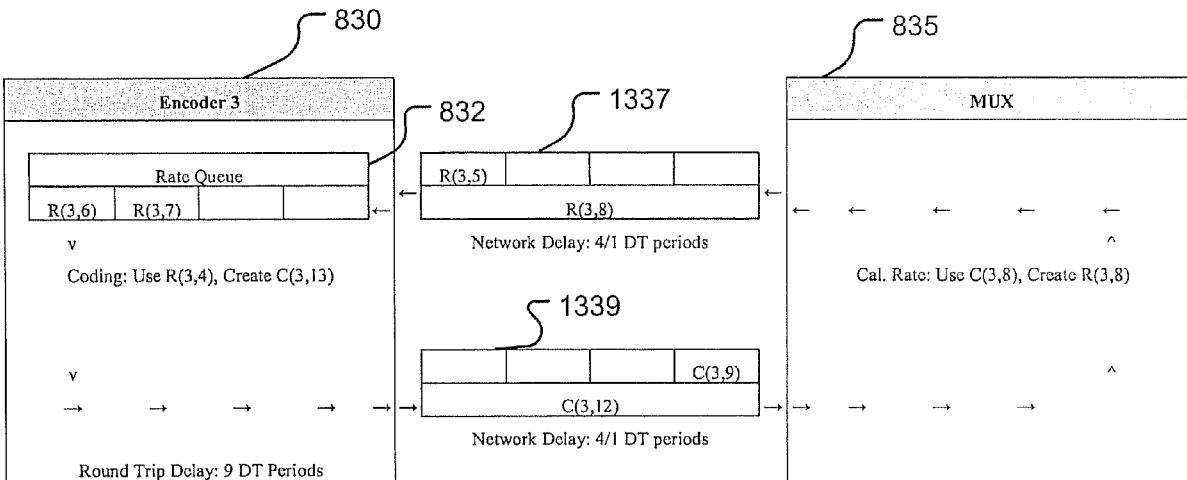


Figure 14B

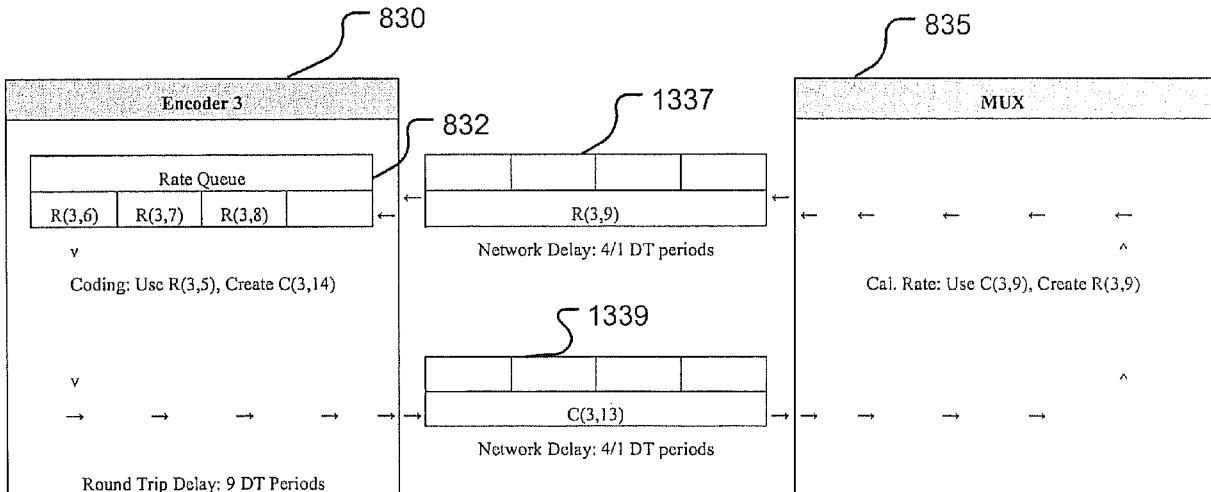


Figure 14C

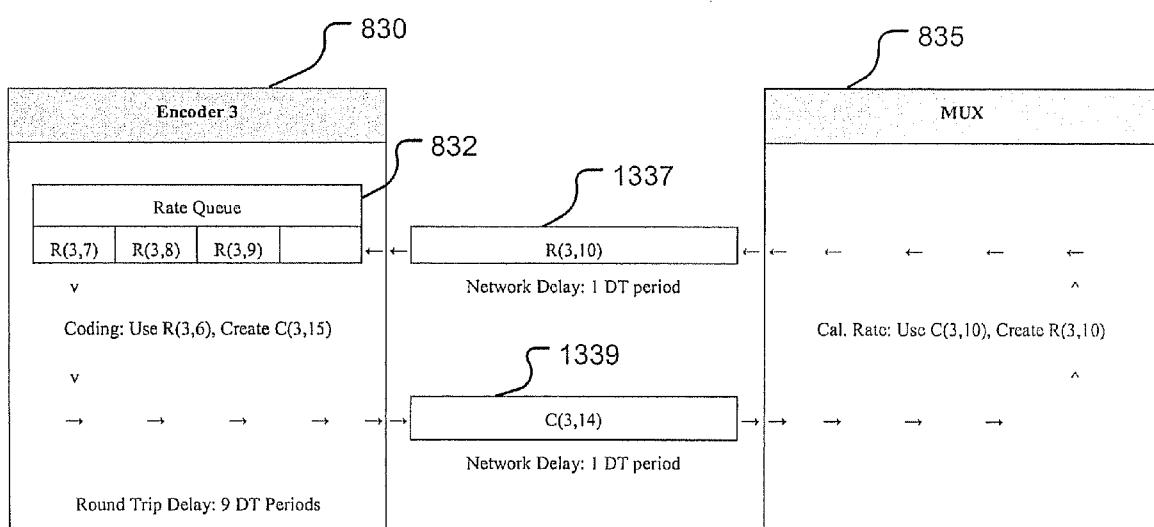


Figure 15

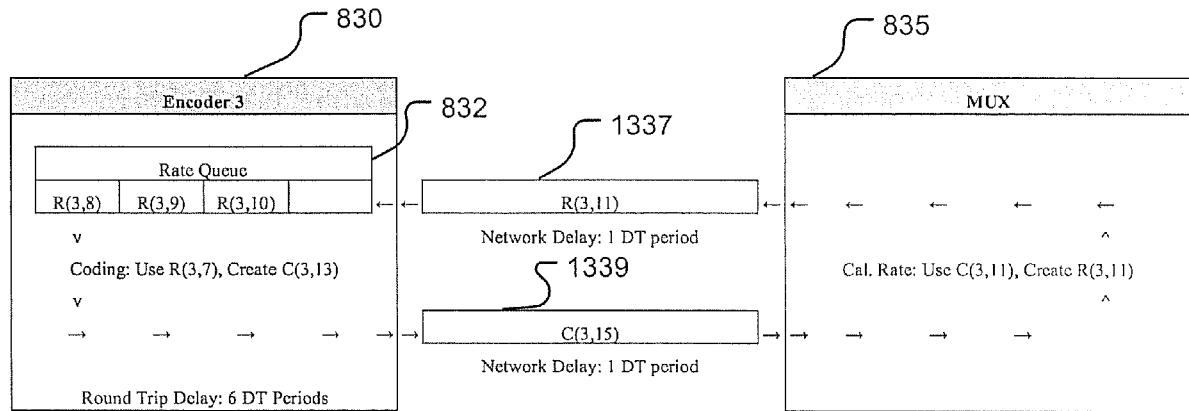


Figure 16A

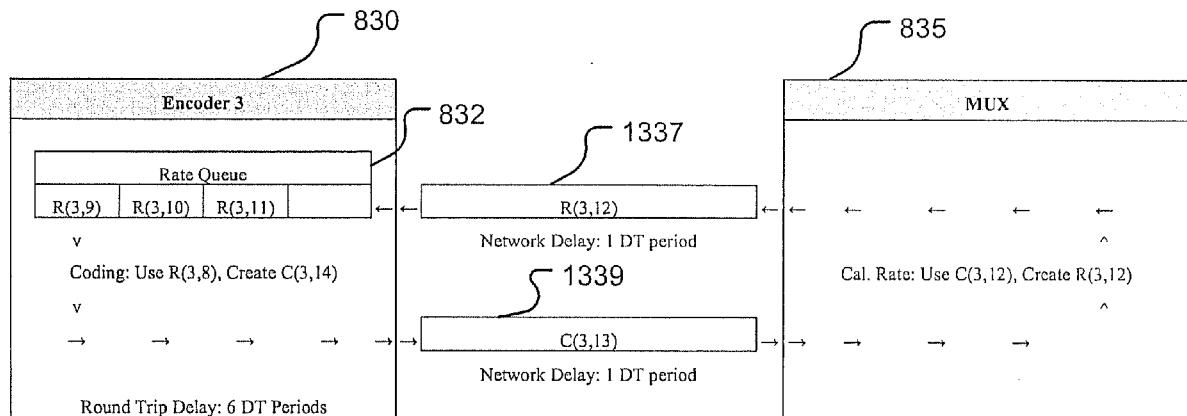


Figure 16B

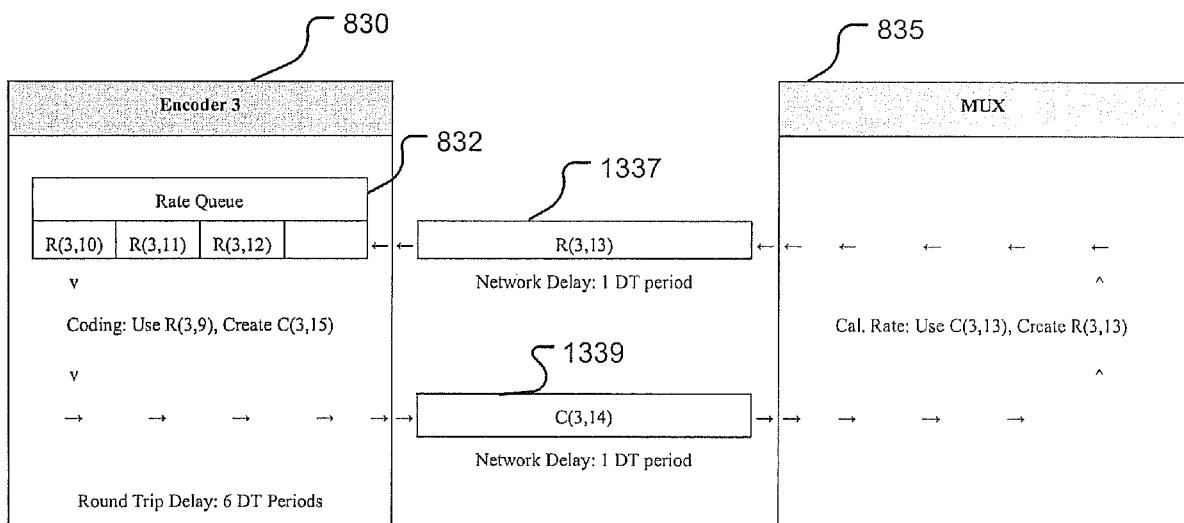


Figure 16C

**INTERNATIONAL SEARCH REPORT**

International application No

PCT/US2010/036727

**A CLASSIFICATION OF SUBJECT MATTER**

IPC(8) - H04J 3/16 (2010.01)

USPC - 370/468

According to International Patent Classification (IPC) or to both national classification and IPC

**B FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H04J 3/16, 3/22, H04N 1/41, 7/12 (2010.01)

USPC - 348/387 1, 390 1, 370/465, 468, 375/240 01, 240 12, 382/236, 298

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent

**C DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X	US 7,418,007 B1 (LIU et al) 26 August 2008 (26.08.2008) entire document	1-74
A	US 6,094,457 A (LINZER et al) 25 July 2000 (25.07.2000) entire document	1-74
A	US 5,861,919 A (PERKINS et al) 19 January 1999 (19.01.1999) entire document	1-74
A	US 6,674,796 B1 (HASKEL et al) 06 January 2004 (06.01.2004) entire document	1-74

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- "&" document member of the same patent family

Date of the actual completion of the international search

20 August 2010

Date of mailing of the international search report

**07 SEP 2010**

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