United States Patent

[11] **3,617,901**

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[73] Assignee **U.S. Philips Corporation**
New York, N.Y.
[32] Priority **Aug. 15, 1967**
[33] **Netherlands**
[31] **6711170**

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[54] **METHOD OF PRODUCING TONES OF AN EQUALLY TEMPERED SCALE**
11 Claims, 15 Drawing Figs.

[52] **U.S. Cl.** **328/17,** 84/1.01, 328/39, 328/105
[51] **Int. Cl.** **H03b 19/00**
[50] **Field of Search** 328/17, 39, 105; 84/1.23, 1.01, 1.19; 307/225, 271

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Primary Examiner—Stanley T. Krawczewicz
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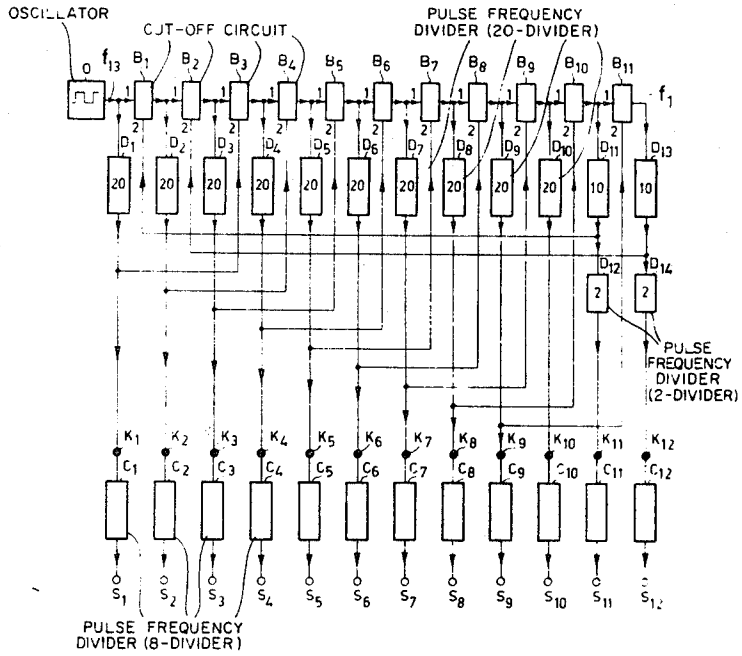
ABSTRACT: A single oscillator connected to a series of pulse dividers and cutoff circuits generates the twelve tones of a musical scale. Each cutoff circuit removes a single cycle from a first input signal in response to each cycle of a second input signal.



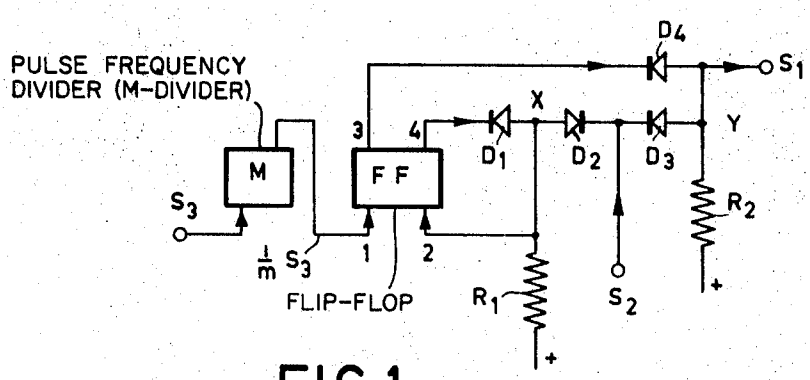


FIG.1

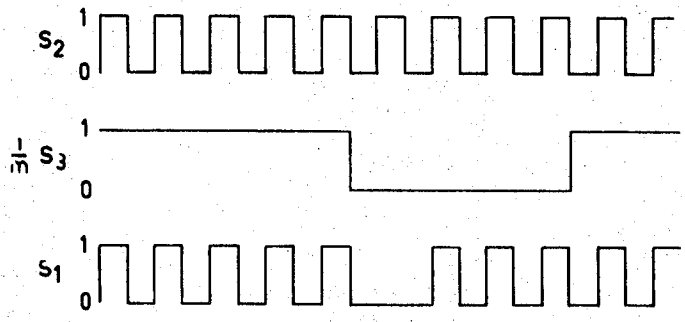


FIG.2

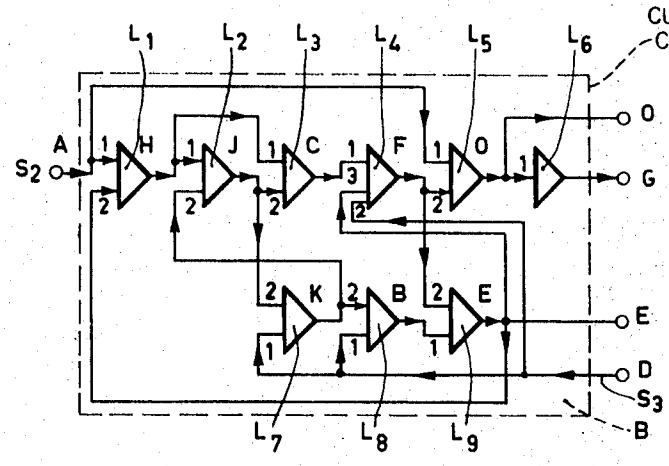


FIG.3

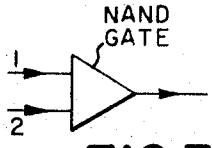


FIG.3a

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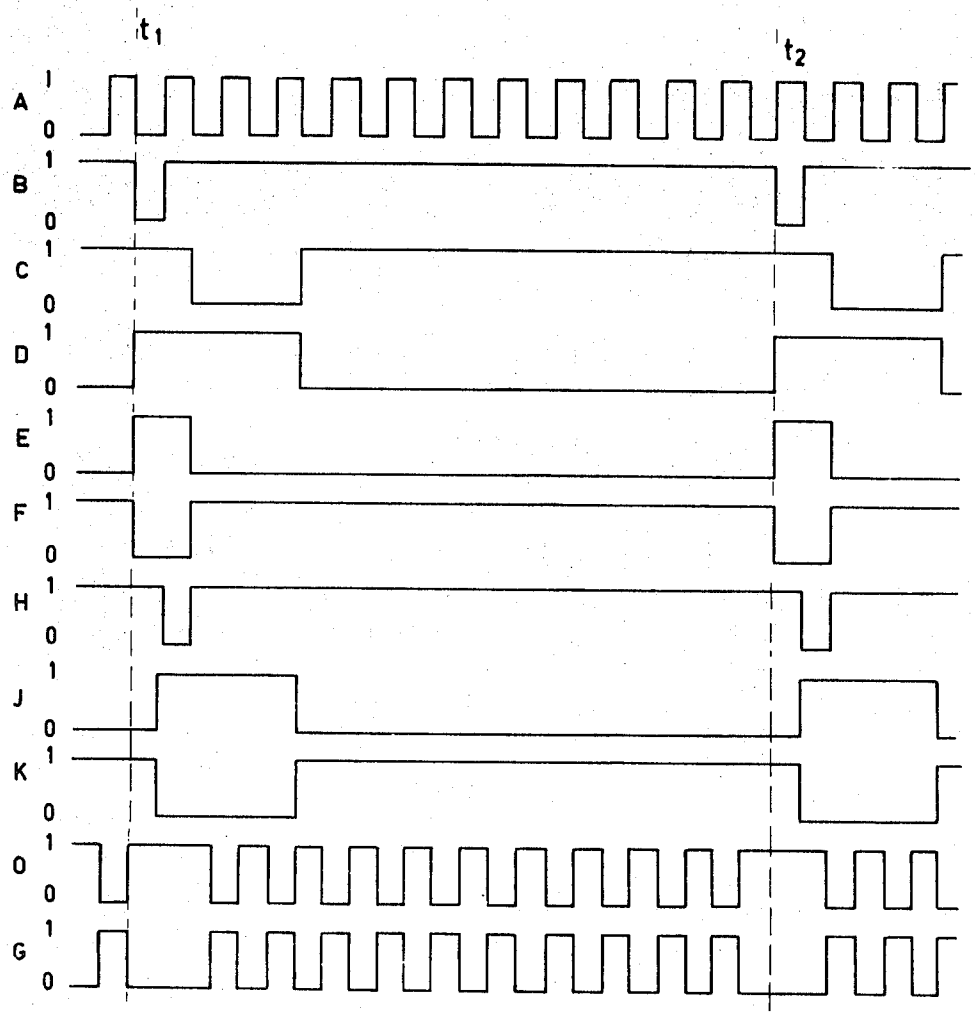

FIG. 4

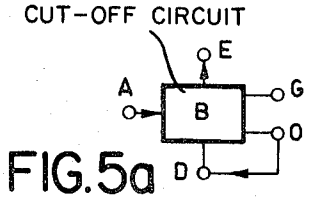

FIG. 5a

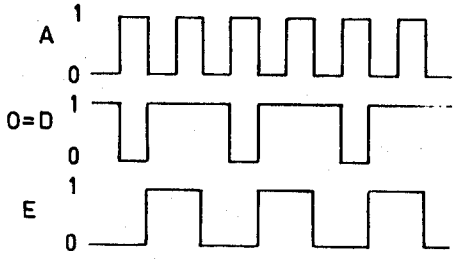

FIG. 5b

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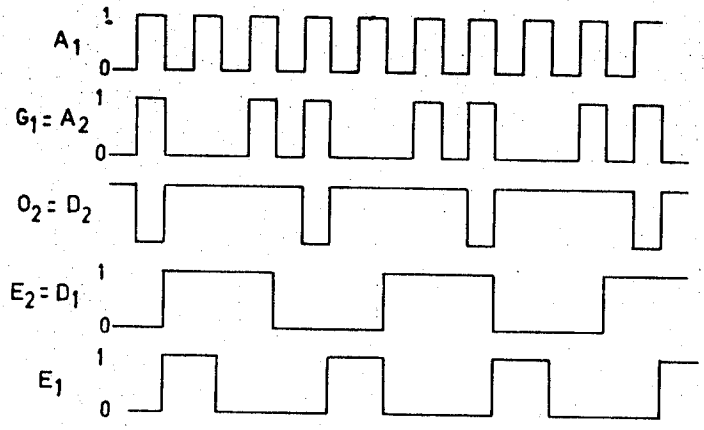

FIG. 6b

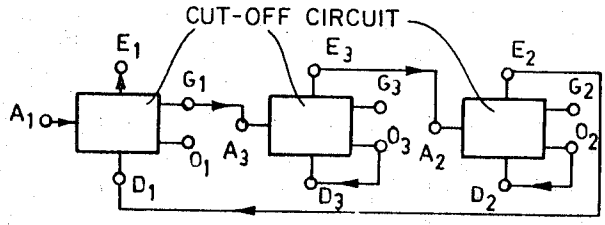

FIG. 7a

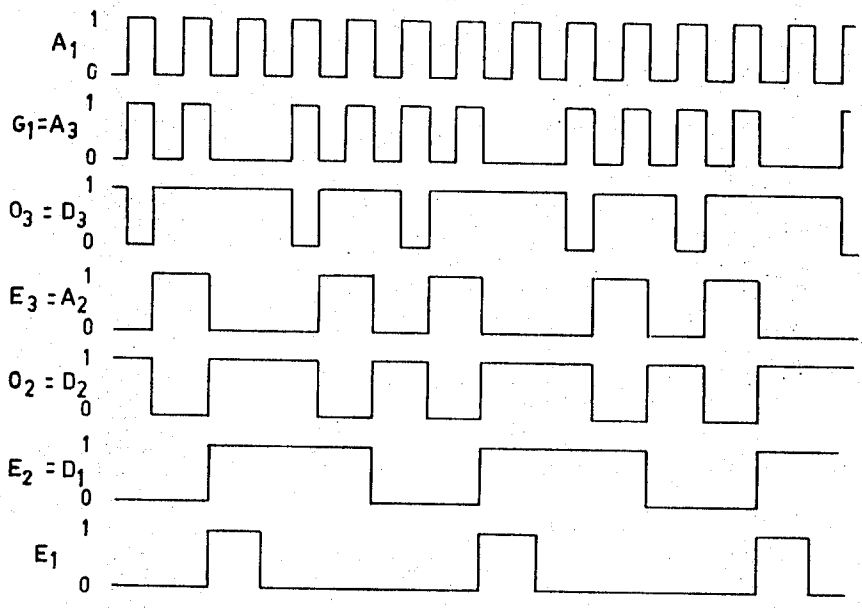

FIG. 7b

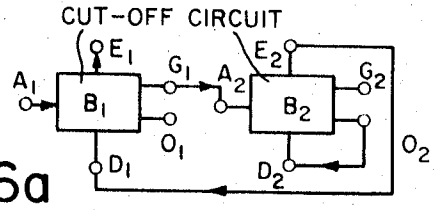

FIG. 6a

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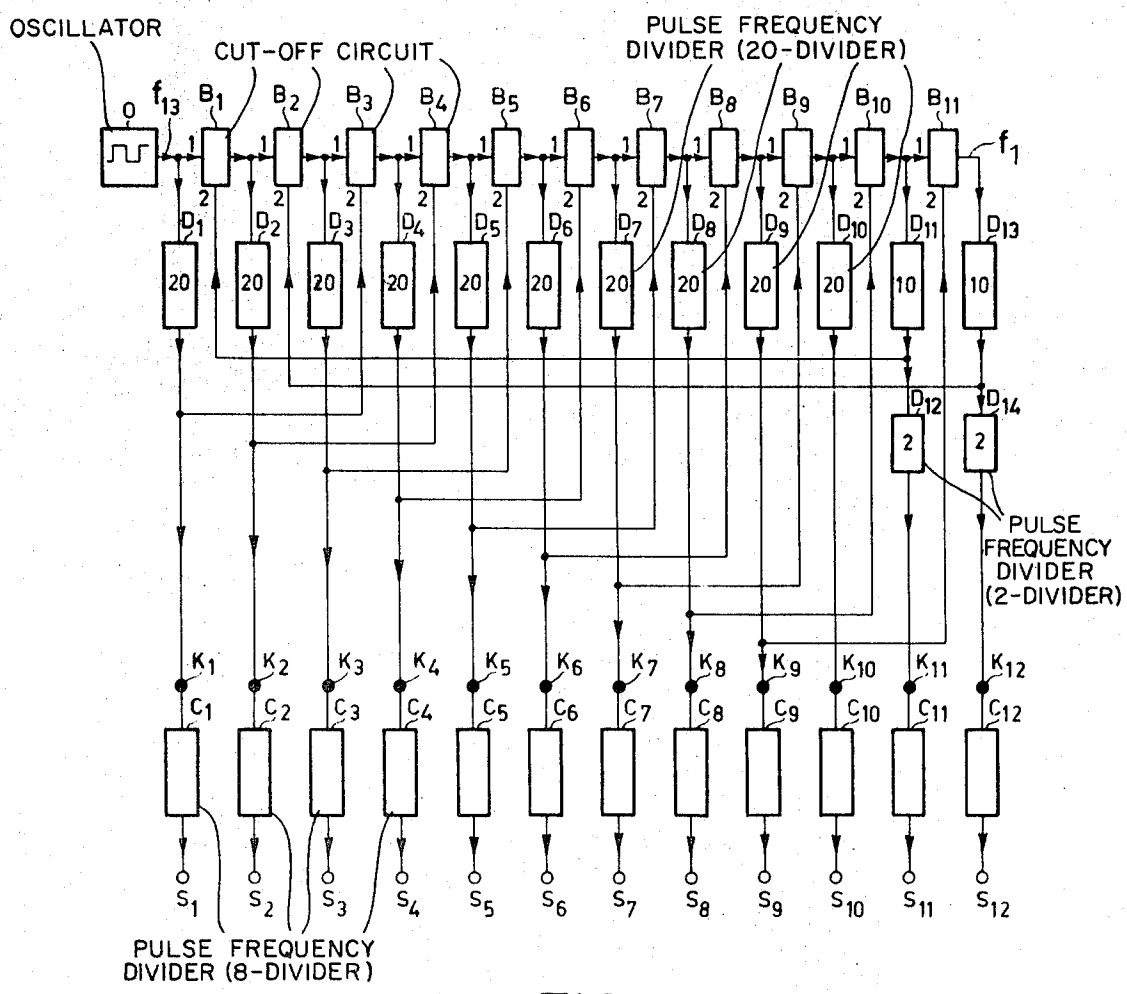

FIG. 8

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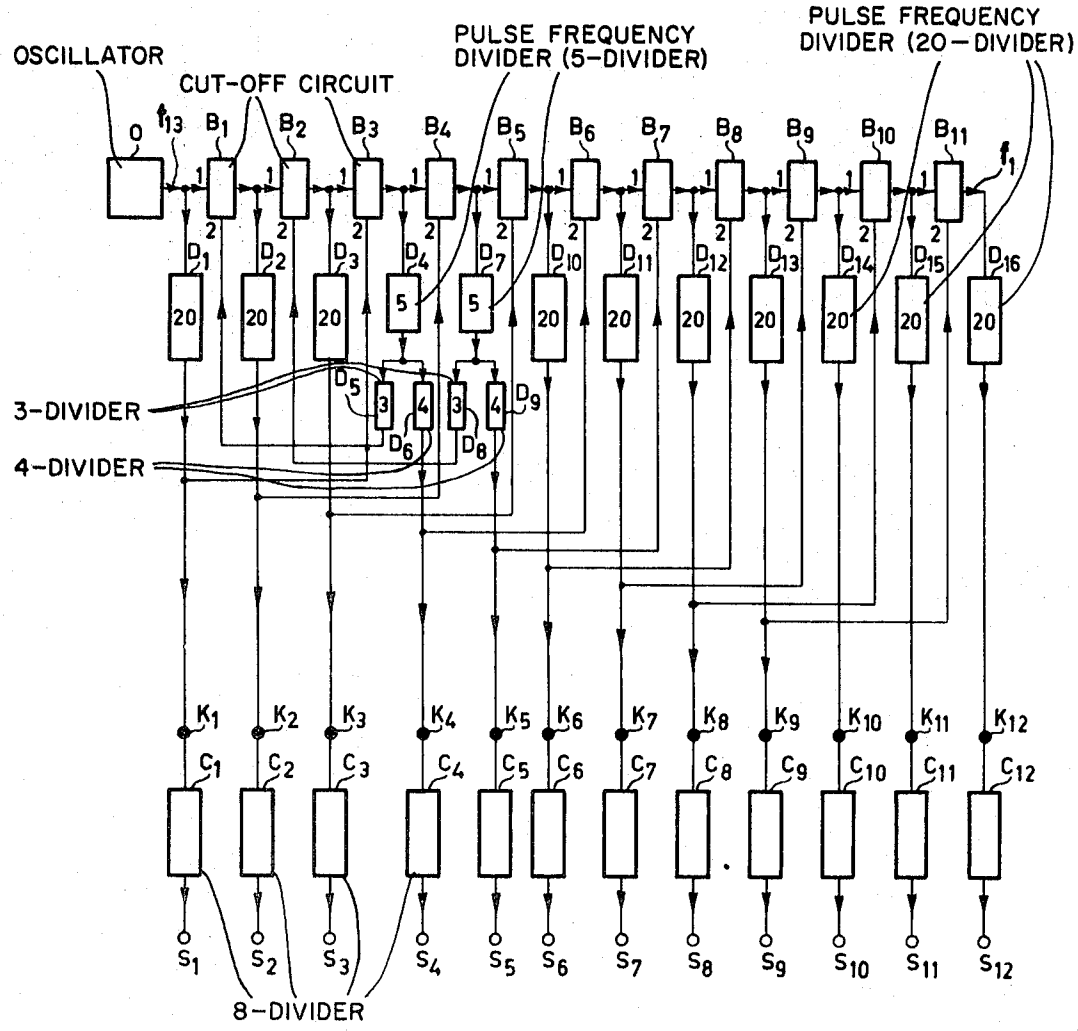

FIG. 9

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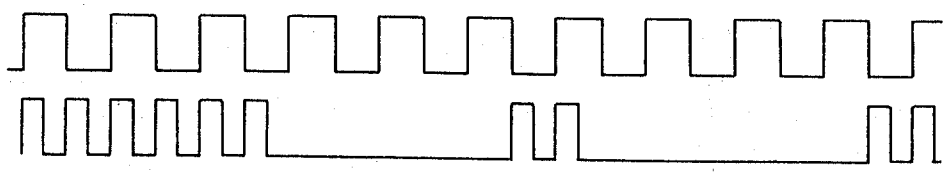

FIG. 10

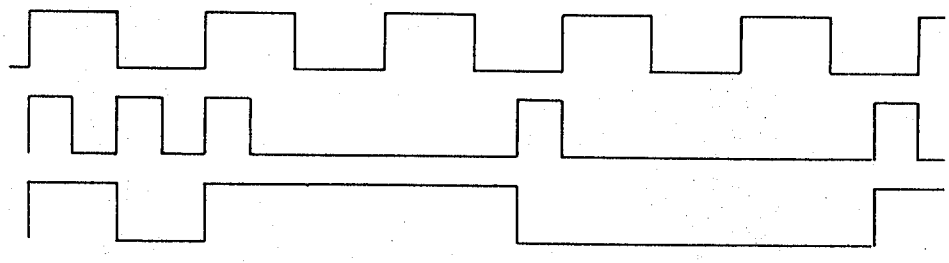

FIG. 11

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METHOD OF PRODUCING TONES OF AN EQUALLY TEMPERED SCALE

The invention relates to a method of producing tones of a substantially equally tempered scale by an electronic musical instrument.

In a known method a number of independent oscillators equal to the number of tones per octave is used, each oscillator being tuned to a different pitch, while the tones of the next lower or further lower octaves are derived from the 12 tones by means of divide-by-2 circuits (2-dividers.)

Obviously when one or more of these oscillators are detuned all derived tones are also detuned so that the instrument gets false.

In the method according to the invention this disadvantage is avoided by having at least one signal determine the position of the scale, while each of the further tones of the octave is derived from the difference frequency of a second tone and the $1/m^{th}$ part of the frequency of a third tone, wherein m is an integral.

By a suitable choice of the number m the frequencies of the further tones of the octave are fixed with respect to the frequencies of the independent oscillators so that the relative frequency ratios which determine the correct tuning of the instrument remain more constant.

If, for example, in the system of 31 tones per octave with intervals between two successive tones equal to $\sqrt[31]{2}$ the number m is chosen to be equal to 37, $f_{10}-f_9=1/74f_{32}=1/37f_1=0.0270270$. This value deviates only by 1.3×10^{15} from the correct value of 0.0270405, which deviation is not perceived by the ear. The frequency of f_1 is standardized at 1.0.

In accordance with the nature of the scale and/or the circuit arrangement employed it may be advantageous to choose m so as not to be equal to for all tones. For example, for the tones of an octave corresponding to the natural tuning m may be chosen to be equal to 5, 4, 3 and 2 so that the following relations are found:

$c_2=c_2$
$b_1=c_2-1/5d_1$
$a_1=c_2-1/4f_1$
$g_1=c_2-1/4c_2$
$f_1=c_2-1/2f_1$
$e_1=c_2-1/3g_1$
$d_1=g_1-1/3g_1$

In a variant of the method according to the invention, particularly for producing tones of a substantially equally tempered 12-tone scale the derived tones are obtained each time from two other tones according to the relation: $f_{n13}=f_{n12}-1/20$ $f_n=f_{n12}-1/10f_{n112}$, wherein n is the ordinal number of the tone in scale.

While an equally tempered 12-tone scale the ratio between the frequencies of adjacent tones is equal to $\sqrt[12]{2}$. If the lowest of the frequencies is designated by f_1 and if it is standardized at 1, the other frequencies of the tones of the chromatic scale based thereon are:

$f_1=1.000\,000$
$f_2=1.059\,463$
$f_3=1.122\,462$
$f_4=1.189\,207$
$f_5=1.259\,921$
$f_6=1.334\,840$
$f_7=1.414\,214$
$f_8=1.498\,307$
$f_9=1.587\,401$
$f_{10}=1.681\,793$
$f_{11}=1.781\,797$ $f_{12}=1.781\,749$
$f_{13}=2.000\,000$

Herein f_{13} is the octave of f_1.

A further consideration of the values of the frequencies shows that the frequency difference between f_{11} and f_{10} is substantially equal to 1/10th of the frequency of the fundamental tone f_1 or to 1/20th of the frequency of the octave tone f_{13}. Since the frequencies form a geometrical progression a corresponding relation applies to all further successive frequencies of the scale.

In accordance with the above-mentioned relation the following set of equations is obtained:

$f_{13}=f_{13}$ (master oscillator)
$f_{12}=f_{13}-1/10f_3$
$f_{11}=f_{12}-1/10f_2$
$f_{10}=f_{11}-1/10f_1=f_{11}-1/20f_{13}$
$f_9=f_{10}-1/20f_{12}$
$f_8=f_9-1/20f_{11}$
$f_7=f_8-1/20f_{10}$
$f_6=f_7-1/20f_9$
$f_5=f_6-1/20f_8$
$f_4=f_5-1/20f_7$
$f_3=f_4-1/20f_6$ $f_2=f_3-1/20\,f_5$

The solution of this set provides the following values of the frequencies with the deviations in 1/1.000.000 between the frequencies by using the approximation relation and the ideal frequencies:

f_2=1,059 460–3,1
f_3=1,122 455–6,2
f_2=1,059 460–3,1
f_3=1,122 455–6,2
f_4=1,189 196–9,3
f_5=1,259 905–12,4
f_6=1,334 819–15,5
f_7=1,414 187–18,4
f_8=1,498 275–21,3
$f_9$1,587 366–22,4
f_{10}=1,681 753–23,5
f_{11}=1,781 809+6,2
f_{12}=1,887 754+3,1

The maximum deviation appears between f_{11} and f_{10}, but even this deviation is less than 30×10^{15}.

In a further variant of the method according to the invention for producing a substantially equally tempered 12-tone scale the derived tones are obtained each time from two other tones in accordance with the relation:

$f_{n13}=f_{n12}-1/15f_{n15}=f_{n12}-1/30f_{n+7}$

f_{n15} is the quint on f_{n112} or the quarter below f_n, which intervals in the tempered tuning are substantially natural. Thus $1/15f_{n15}$ is substantially equal to $0.1f_{n112}$ or $1/20f_n$. The deviation from the ideal frequencies is then slightly greater than in the preceding case but the result is still quite acceptable.

With nonsinusoidal signals, for example, pulsatory signals, the term frequency is understood to mean the pulse repetition frequency which may be considered to be the number of pulses per second. This is no longer a strictly regular sequence of pulses. Whether this sequence of pulses is perceived subjectively as an acceptable tone depends upon the extent of variation of the pulse interval. If the frequency f is replaced by the number of pulses N for a given period of time the preceding formulas obtain like before, when f is replaced by N.

It is now possible in a variant of the method according to the invention to obtain the difference signal by cutting off such a number of periods in a cutoff circuit from any pulse sequence of the second signal as corresponds to $1/n$ part of the number of periods of the third signal in the same period of time. A cutoff circuit is therefore defined as a circuit wherein one cycle of a first input signal will be removed in response to each cycle of a lower frequency signal.

On the basis of the relation $N_{n13}=N_{n12}-1/20N_n$ the sequence N_{n12} is applied to a first input of the cutoff circuit and the pulse sequence N_n via a 20-divider to a second input. At the N_{n13} output appears the sequence of pulses N_{n12} until the pulse sequence N_n has reached a multiple of 20, at which instant the cutoff circuit takes care that one pulse of the N_{n12} sequence is not passed to the N_{n13} output.

In one embodiment of a device for carrying out the method according to the invention the cutoff circuit is formed by a first input terminal to which the second signal is applied and which leads to a first input of a first AND-gate, a second input of which is connected to a first output of a bistable flip-flop, a first input of which leads to a second input terminal, which

leads to an output of an *m*-divider, to the input of which is applied the third signal, while a second output of the flip-flop is connected to a first input of a second AND-gate, to a second input of which is also applied the second signal, the output being connected to a second input of the flip-flop.

In a further embodiment of such a device the cutoff circuit is formed solely by logical circuits comprising a number of inputs and one output, at which a voltage may appear at two levels, the voltage occurring at the first level when at least one of the voltages at the inputs has a first value and the voltage occurring at the second level when the voltages at the inputs have solely a second value, while the second signal is applied via a first input terminal to a first input of a first logical circuit, the output of which is connected to a first input of a second logical circuit and of a third logical circuit, the output of the second logical circuit leading to a second input of the third logical circuit, the output of which is connected to a first input of a fourth logical circuit, the output of which leads to a second input of a fifth logical circuit, to a first input of which is also applied the second signal, while the output is connected to a first output terminal and to an input of a sixth logical circuit, the output of which leads to a second output terminal and a second input terminal leads to a second input of the fourth logical circuit and to a first input of a seventh and of an eighth logical circuit, a second input of the seventh logical circuit being connected to the output of the second logical circuit and the output of the seventh logical circuit leads to the second input of the second and of the eighth logical circuits, while the output of the eighth logical circuit is connected to a first input of a ninth logical circuit, a second input of which leads to the output of the fourth logical circuit and the output to a third input of the fourth logical circuit, to a second input of the first logical circuit and to a third output terminal.

The advantage is that this circuitry can be readily constructed in the form of an integrated circuit and that in a further embodiment of the invention these circuits may serve to form the dividing circuits, so that a whole generator can be composed of identical parts.

In accordance with a further feature of the device for producing a substantially equally tempered 12-tone scale a master oscillator is connected to a first input of a first cutoff circuit and through a first 20-divider (divide-by-20 circuit) to a second input of a third cutoff circuit and a first output terminal, the output of the first cutoff circuit being connected to a first input of a second cutoff circuit and through a second 20-divider to a second input of a fourth cutoff circuit and a second output terminal, the output of the second cutoff circuit leading to a first input of the third cutoff circuit and through a third 20-divider to a second input of a fifth cutoff circuit and to a third output terminal, the output being connected to a first input of the fourth cutoff circuit and through a fourth 20-divider to a second input of a sixth cutoff circuit and to a fourth output terminal, the output of the fourth cutoff circuit being connected to a first input of the fifth cutoff circuit and through a fifth 20-divider to a second input of a seventh cutoff circuit and to a fifth output terminal, the output of the fifth cutoff circuit leading to a first input of the sixth cutoff circuit and through a sixth 20-divider to a second input of an eighth cutoff circuit and to a sixth output terminal, the output of the sixth cutoff circuit being connected to a first input of the seventh cutoff circuit and through a seventh 20-divider to a second input of a ninth cutoff circuit and to a seventh output terminal, the output of the seventh cutoff circuit leading to a first input of the eighth cutoff circuit and via an eighth 20-divider to a second input of the tenth cutoff circuit and to an eighth output terminal, the output being connected to a first input of the ninth cutoff circuit and through a ninth 20-divider to a second input of an eleventh cutoff circuit and to a ninth output terminal, the output of the ninth cutoff circuit leading to a first input of the tenth cutoff circuit and through a tenth 20-divider to a tenth output terminal, the output of the tenth cutoff circuit being connected to a first input of the eleventh cutoff circuit and through a first 10-divider on the one hand to a second input of the first cutoff circuit and on the other hand through a first 2-divider to an eleventh output terminal, while the output of the eleventh cutoff circuit is connected through a second 10-divider on the one hand to a second input of the second cutoff circuit and on the other hand through a second 2-divider to a twelfth output terminal.

In each cutoff circuit a pulse is cutoff and the resultant signal is applied to the next cutoff circuit, in which again pulses are cutoff from the resultant pulse sequence. The result consists of 12 pulse sequences in which the ratios between the mean numbers correspond to the frequency ratios in accordance with the tempered tuning, the pulse distribution with the lower tones exhibiting an increasing irregularity, since the pulses thereof have passed through a progressive number of cutoff circuits. The signal f_1, which is in fact not obtained in this way since it is the octave of f_{13}, then comprises a number of pulses equal to half the number of f_{13}. In the ideal case it is to be expected that after each pulse one pulse is omitted. In reality the situation is approximately as follows: six pulses, five pulses cutoff, two pulses, six pulses omitted and so on. This irregularity makes a very disagreeable impression on the ear. By applying the signal to dividing circuits these irregularities are drastically reduced.

Owing to the effect of capacitances and resistances the circuits involve a delay time. The delay times are added in the consecutive circuits and when a given value is exceeded too few pulses will be omitted so that the height of the pulse frequency is restricted.

This results in that it is not possible to divide by a sufficiently high number for obtaining an acceptable quality of the tones of the highest octave of the keyboard. The influence of the delay time is at a maximum between the outputs of the 10-dividers and the input signals of the cutoff circuits controlled thereby. In accordance with a further embodiment of a device for producing a substantially equally tempered 12-tone scale this influence can be reduced by connecting a master oscillator to a first input of a first cutoff circuit and through a first 20-divider to a second input of a third cutoff circuit and to a first output terminal, the output of the first cutoff circuit being connected to a first input of a second cutoff circuit and through a second 20-divider to a second input of a fourth cutoff circuit and to a second output terminal, the output of the second cutoff circuit leading to a first input of the third cutoff circuit and through a third 20-divider to a second input of a fifth cutoff circuit and to a third output terminal, the output of the third cutoff circuit being connected to a first input of the fourth cutoff circuit and to a first 5-divider, which is connected on the one hand to a first 3-divider, the output of which leads to a second input of the first cutoff circuit and on the other hand to a first 4-divider, the output of which leads to a second input of a sixth cutoff circuit and to a fourth output terminal, the output of the fourth cutoff circuit being connected to a first input of the fifth cutoff circuit and to a second 5-divider, which is connected on the one hand through a second 3-divider to a second input of the second cutoff circuit and on the other hand through a second 4-divider to a second input of a seventh cutoff circuit and to a fifth output terminal, the output of the fifth cutoff circuit being connected to a first input of a sixth cutoff circuit and through a fourth 20-divider to a second input of an eighth cutoff circuit and to a sixth output terminal, the output of the sixth cutoff circuit being connected to a first input of a seventh cutoff circuit and through a fifth 20-divider to a second input of a ninth cutoff circuit and to a seventh output terminal, the output of the seventh cutoff circuit leading to a first input of the eighth cutoff circuit and through a sixth 20-divider to a second input of a tenth cutoff circuit and to an eighth output terminal, the output of the eighth cutoff circuit being connected to a first input of a ninth cutoff circuit and through a seventh 20-divider to a second input of an eleventh cutoff circuit and to a ninth output terminal, while the output of the ninth cutoff circuit leads to a first input of the tenth cutoff circuit and through an eighth 20-divider to a tenth output terminal, the output of the tenth cu-

toff circuit being connected to a first input of the eleventh cutoff circuit and through a ninth 20-divider to an eleventh output terminal, the output of the eleventh cutoff circuit being connected through a tenth 20-divider to a twelfth output terminal.

The aforesaid irregular distribution of the pulses, which makes a very disagreeable impression on the ear, may be strongly reduced by applying the signal to divide-by-2 circuits so that, when the outputs of the 20-dividers are employed and when in accordance with a further feature of the device according to the invention the output terminals are each connected to a *m*-divider in which *m* is at least 4, while the output signals are the tones of the highest desired octave, said irregularities are reduced to an acceptable level. Since the frequencies of the tones of the octave are unambiguously determined by the frequency of the master oscillator, it is advantageous in accordance with a further feature of the device embodying the invention, to render the master oscillator continuously and/or stepwise detunable. Thus the pitch of the oscillators may be adapted to other instruments and/or it may be transposed. The continuous detuning permits, in addition, of obtaining special effects, for example, for imitating a Hawaiian guitar. The lower octave tones are derived from the tones of the highest octave by means of divide-by-2 circuits.

This will be explained more fully with reference to the following Figures.

FIG. 1 shows a cutoff circuit comprising two AND-gates and a flip-flop.

FIG. 2 illustrates the voltages at various points of this circuitry.

FIG. 3 shows a cutoff circuitry comprising logical circuits and

FIG. 4 illustrates the voltages at various points of this circuitry and

FIG. 5*a* shows the cutoff circuits of FIG. 3 and 2-dividers and

FIG. 5*b* illustrates the associated voltages.

FIG. 6*a* shows the same circuits as 3-dividers and

FIG. 6*b* illustrates the associated voltages.

FIG. 7*a* shows the circuits as 5-dividers and

FIG. 7*b* illustrates the associated voltages.

FIG. 8 shows a complete oscillator comprising 10- and 20-dividers and

FIG. 9 shows an oscillator comprising 15- and 20-dividers.

FIG. 10 illustrates the ideal pulse distribution and the distribution obtained by the circuit arrangement.

FIG. 11 illustrates the improvement of the pulse distribution after the passage through 2-dividers.

Referring to FIG. 1, the terminal S_2 receives the second signal. The terminal S_2 is connected to a first input of a first AND-gate comprising the diodes D_3, D_4 and the resistor R_2. The second input of this AND-gate is connected to a first output 3 of a bistable flip-flop FF. The first input 1 of the flip-flop FF leads to the output of an *m*-divider M, such as that shown in FIG. 6*a* and described hereinafter to the input of which is applied the third signal S_3. A second output 4 of the flip-flop FF is connected to a first input of a second AND-gate comprising the diodes D_1, D_2 and the resistor R_1, to the second input of which is also applied the second signal S_2, whereas the output of this second AND-gate is connected to a second input 2 of the flip-flop FF. The *m*-divider is in this constructed so that its output voltage varies when the input pulse changes over from the voltage level 1 to the voltage level 0. In the normal state the pulses of the signal S_2 are passed through the first AND-gate, since the output 3 of the flip-flop FF is 1 so that the voltage at point *y* varies in the same way. Since the voltage at the output 4 of the flip-flop FF is 0, the point *x* also remains 0 independently of the signal S_2.

It will be assumed that the output of the *m*-divider M that is to say the input 1 of the flip-flop FF changes over from 0 to 1; at the instant when the pulse sequence S_2 is 0, the flip-flop FF changes over. Point 4 becomes 1 and point 3 becomes 0 so that the diode D_4 is conducting and D_2 is cutoff. At the next pulse of the sequence S_2 point *y* remains 0 so that this pulse is not allowed to pass. Point *x*, on the contrary, follows the voltage of the input pulses so that at the end of the next pulse of S_2 *x* changes over from 0 to 1, which voltage variation is transferred to the input 2 of the flip-flop FF, which is thus changed over to its initial state, in which point 3 is 1 and point 4 is 0 so that the next pulses are again passed through the first AND-gate to the point *y*. After a given time the output of the *m*-divider M changes over from 0 to 1, but this does not affect the state of the flip-flop FF, since it responds only to the trailing edge of the pulses. This is illustrated in detail in FIG. 2.

FIG. 3 shows a cutoff circuit comprising conventional solely logical NAND gate circuits having a number of inputs and one output, to which a voltage may appear at two levels 0 and 1, the voltage at the first level 0 appearing on the output terminals when the voltages at the inputs all have a value 1, whereas a voltage appears on the output terminal at the second level 1 when one of the voltages at the inputs has a second value 0. The second signal S_2 is applied through a first input terminal A to a first input 1 of a first logical circuit L_1. The output H of circuit L_1 is connected to a first input 1 of a second and of a third logical circuit L_2 and L_3 respectively. The output J of the second logical circuit L_2 leads to a second input 2 of the third logical circuit L_3, the output C of which is connected to a first input of a fourth logical circuit L_4. The output F of the circuit L_4 leads to a second input 2 of a fifth logical circuit L_5, to a first input 1 of which is also applied the second signal S_2. The output of circuit L_5 is connected to a first output terminal 0 and to an input 1 of a sixth logical circuit L_6, the output of which leads to a second output terminal G, while a second input terminal D, to which is applied the third signal S_3, leads to a second input of the fourth logical circuit L_4 and to a first input 1 of a seventh and of an eighth logical circuit L_7 and L_8 respectively. A second input 2 of the seventh logical circuit L_7 is connected to the output J of the second logical circuit L_2. The output K of the seventh logical circuit L_7 leads to the second input of the second and of the eighth logical circuit L_2 and L_8 respectively. The output B of the eighth logical circuit L_8 is connected to a first input 1 of a ninth logical circuit L_9, a second input 2 of which leads to the output F of the fourth logical circuit L_4. The output of the ninth logical circuit L_9 leads to a third input 3 of the fourth logical circuit L_4 and to a second input of the first logical circuit and to a third output terminal E.

The truth table associated with this circuitry is as follows:

A	B	C	D	E	F	H	J	K	O	G	
A	1	1	0	0	1	1	0	1	A	A	(A may be 0 or 1).
1	1	1	1	1	0	0	1	0	1	0	(The third signal S_3 becomes 1).
0	1	0	1	0	1	1	1	0	1	0	(A new pusle of S_2 arrives).
1	1	0	1	0	1	1	1	0	0	1	(Pulse of S_2 terminates).
0	1	1	0	0	1	1	0	1	1	0	(A new pulse of S_2 arrives).
and so on											
1	1	1	0	0	1	1	0	1	0	1	(Pulse of S_2 terminates and the third signal S_3 is 0). (The next pulse of S_2 arrives).
and so on											

The waveforms of the voltages at the various outputs are illustrated in FIG. 4, It appears that the occurrence of a pulse S_3 of any length at the input terminal D cuts off the next-following pulse of the signal S_2 at the input terminal A, whereas the further pulses are allowed to pass.

In FIG. 4 two cases are illustrated, that is to say, the case in which at the instant t_1 the voltage at the input A just becomes 0 and a second case in which at the instant t_2 the voltage at the input A just becomes 1. It is apparent that in both cases the first positive-going pulse at the input A is cutoff.

FIG. 5*a* illustrates how a cutoff circuit of FIG. 3 may be arranged as a divide-by-2 circuit (2-divider) by connecting the output 0 to the input D of the third signal and by deriving the signal from the output E. By applying the signal E to an input A of a second cutoff circuit and by deriving the voltage from the output E of this circuit, a divider with a division ratio of 4

is obtained. FIG. 6*a* illustrates how two cutoff circuits of FIG. 3 may be used to obtain a divider with a division ratio of 3 by connecting the output G_1 of a first cutoff circuit B_1 to the input A_2 of a cutoff circuit B_2. The output 0_2 of circuit B_2 is connected to the input D_2, which the signal of the output E_2 is applied to the input D_1 of the first cutoff circuit B_1. The signal of the output E_1 is divided by 3 is obtained at the output E_2 output. The voltages appearing at various points of this circuitry are illustrated in the associated graphs of FIG. 6*b*. By including a third cutoff circuit B_3, connected as a 2-divider, between the output G_1 of the first cutoff circuit B_1 and the input A_2 of the second cutoff circuit, a divider with a division ratio of .5 is obtained as is shown in FIG. 7*a*, the graphs of FIG. 7*b* illustrating the voltages at various points of this arrangement. These cutoff circuits permit of manufacturing a complete oscillator for an electronic musical instrument including all dividers by means of only one type of element.

Such an oscillator is shown in FIG. 8; it is capable of producing the tones of a substantially equally tempered 12-tone scale by means of a master oscillator, 11 cutoff circuits such as the devices shown in FIG. 1 or FIG. 3, 10 divide-by-20 circuits and two divide-by-10 circuits. The 10-divider may be made by connecting a 5-divider as shown in FIG. 7*a* and a 2-divider as shown in FIG. 5*a* in series. Obviously connecting an additional divide-by-2 circuit to the series circuit would result in a divide-by-20 circuits. The signal of the master oscillator 0 is applied to a first input 1 of a first cutoff circuit B_1 and through a first 20-divider D_1 to a second input 2 of a third cutoff circuit B_3 and to a first output terminal K_1. The output of the first cutoff circuit B_1 is connected to a first input 1 of a second cutoff circuit B_2 and through a second 20-divider D_2 to a second input 2 of a fourth cutoff circuit B_4 and to a second output terminal K_2. The output of the second cutoff circuit B_2 is connected to a first input 1 of a third cutoff circuit B_3 and through a third 20-divider D_3 to a second input 2 of a fifth cutoff circuit B_5 and to a third output terminal K_3. The output of circuit B_3 is also connected to a first input 1 of the fourth cutoff circuit B_4 and via a fourth 20-divider D_4 to a second input 2 of a sixth cutoff circuit B_6 and to a fourth output terminal K_4. The output of the fourth cutoff circuit B_4 is connected to a first input 1 of the fifth cutoff circuit B_5 and via a fifth 20-divider D_5 to a second input 2 of a seventh cutoff circuit B_7 and to a fifth output terminal K_5. The output of the fifth cutoff circuit B_5 leads to a first input 1 of a sixth cutoff circuit B_6 and via a sixth 20-divider D_6 to a second input 2 of an eighth cutoff circuit B_8 and to a sixth output terminal K_6. The output of the sixth cutoff circuit B_6 is connected to a first input 1 of a seventh cutoff circuit B_7 and via a seventh 20-divider D_7 to a second input 2 of a ninth cutoff circuit B_9 and to a seventh output terminal K_7. The output of the seventh cutoff circuit B_7 leads to a first input 1 of the eighth cutoff circuit B_8 and via an eighth 20-divider D_8 to a second input 2 of the tenth cutoff circuit B_{10} and to an eighth output terminal K_8. The output of the eighth cutoff event B_8 is connected to a first input 1 of the ninth cutoff circuit B_9 and via a ninth 20-divider D_9 to a second input 2 of an eleventh cutoff circuit B_{11} and to a ninth output terminal K_9. The output of the ninth cutoff circuit B_9 leads to a first input of the tenth cutoff circuit B_{10} and through a tenth 20-divider D_{10} to a tenth output terminal K_{10}. The output of the tenth cutoff circuit B_{10} is connected to a first input 1 of the eleventh cutoff circuit B_{11} and via a first 10-divider D_{11} on the one hand to a second input 2 of the first cutoff circuit B_1 and on the other hand via a first 2-divider D_{12} to an eleventh output terminal K_{11}. The output of the eleventh cutoff circuit is connected via a second 10-divider D_{13} on the one hand to a second input 2 of the second cutoff circuit B_2 and on the other hand via a second 2-divider D_{14} to a twelfth output terminal K_{12}. Pulse frequency divider C_1 through C_{12} are described hereinabove.

Owing to the effect of capacitances and resistances the pulses are passed through the elements with a given delay. The delay times are added in the consecutive circuits and when a given value is exceeded too many pulses may be skipped.

The influence of the delay time is at a maximum between the outputs of the 10-dividers D_{11} and D_{13} and the input signals of the cutoff circuits B_1 and B_2 respectively controlled thereby. The result is that it is not possible to divide by a sufficiently high number to obtain the highest tone of the keyboard.

In the device shown in FIG. 9 for producing a substantially equally tempered 12-tone scale the influence of the delay time may be reduced by deriving the third signal, in those cases in which a signal of the 10-divider D_{11} or D_{13} is fed back to the first and to the second cutoff circuits B_1 and B_2 respectively such as the devices shown in FIGS. 1 or 3, from the outputs of the two further cutoff circuits whose frequency is divided by 15, instead of being derived from said 10-dividers. The accuracy of the resultant frequency is lower, it is true, but it is certainly sufficient for the purpose aimed at. In the arrangement of FIG. 9 a master oscillator 0 is connected to a first input 1 of a first cutoff circuit B_1 and through a first 20-divider D_1 to a second input 2 of a third cutoff circuit B_3 and to a first output terminal K_1. The output of the first cutoff circuit B_1 is connected to a first input 1 of a second cutoff circuit B_2 and through a second 20-divider D_2 to a second input 2 of a fourth cutoff circuit B_4 and to a second output terminal K_2. The output of the second cutoff circuit B_2 leads to a first input 1 of the third cutoff circuit B_3 and via a third 20-divider D_3 to a second input 2 of a fifth cutoff circuit B_5 and to a third output terminal K_3. The output of the third cutoff circuit B_3 is connected to a first input 1 of the fourth cutoff circuit B_4 and to a first 5-divider D_4, which is connected on the one hand to a first 3-divider D_5 whose output leads to a second input 2 of the first cutoff circuit B_1 and on the other hand to a first 4-divider D_6. The output of divider D_6 leads to a second input 2 of a sixth cutoff circuit B_6 and to a fourth output terminal K_4. The output of the fourth cutoff circuit B_4 is connected to a first input 1 of the fifth cutoff circuit B_5 and to a second 5-divider D_7, which is connected on the one hand via a second 3-divider D_8 to a second input 2 of the second cutoff circuit B_2 and on the other hand via a second 4-divider D_9 to a second input 2 of a seventh cutoff circuit B_7 and to a fifth output terminal K_5. The output of the fifth cutoff circuit B_5 is connected to a first input 1 of the sixth cutoff circuit B_6 and via a fourth 20-divider D_{10} to a second input 2 of an eighth cutoff circuit B_8 and to a sixth output terminal K_6. The output of the sixth cutoff circuit B_6 is connected to a first input 1 of the seventh cutoff circuit B_7 and via a fifth 20-divider D_{11} to a second input 2 of a ninth cutoff circuit B_9 and to a seventh output terminal K_7. The output of the seventh cutoff circuit B_7 leads to a first input 1 of the eighth cutoff circuit B_8 and through a sixth 20-divider D_{12} to a second input 2 of a tenth cutoff circuit B_{10} and to an eighth output terminal K_8. The output of the eighth cutoff circuit B_8 is connected to a first input 1 of the ninth cutoff circuit B_9 and via a seventh 20-divider D_{13} to a second input 2 of an eleventh cutoff circuit B_{11} and to a ninth output terminal K_9. The output of the ninth cutoff circuit B_9 leads to a first input 1 of the tenth cutoff circuit B_{10} and via an eighth 20-divider D_{14} to a tenth output terminal K_{10}. The output of the tenth cutoff circuit B_{10} is connected to a first input 1 of the eleventh cutoff circuit B_{11} and via a ninth 20-divider D_{15} to an eleventh output terminal K_{11}. The output of the eleventh cutoff circuit B_{11} is connected through a tenth 20-divider D_{16} to a twelfth output terminal K_{12}.

In each cutoff circuit pulses are cutoff and the resultant signal is applied to the next-following cutoff circuit, in which arbitrary other pulses are cut off from the resultant pulse sequences. The result consists of 12 pulse sequences in which the ratios between the average numbers correspond to the frequency ratios in accordance with the tempered tuning, the pulse distribution in the lower tones exhibiting a progressive irregularity, since the pulses thereof have passed through an even higher number of cutoff circuits. If, for example, the signal f_1 is produced in this way, which is not done in reality since it is the octave of f_{13}, the number of pulses is on an average equal to half the number of pulses of f_{13}. In the ideal

case it could be expected that after each pulse one pulse is omitted. In reality the situation may be as follows: six pulses, five pulses cutoff, two pulses, six pulses omitted and so on. This is illustrated in FIG. 10 which also illustrates the ideal pulse sequence. This irregularity makes a very unpleasant impression on the ear. By applying the signal to divide-by-2 circuits, these irregularities are strongly reduced, as will be apparent from FIG. 11, which illustrates the two signals of FIG. 10 after having passed through such a 2-divider. The voids in the pulse sequence of FIG. 10, amounting to 11 and 13 pulse widths respectively, are reduced here to six an seven pulse widths respectively. A further division by 2 reduces this number to 3.5 and 4 respectively, as is indicated also in FIG. 11.

In FIGS. 8 and 9 C_1 to C_{12} designate these additional dividers, the output voltages being derived from terminals S_1 and S_{12}. In this case the dividers C_1 and C_{12} and 8-dividers which may be derived by series connecting three 2-dividers as shown in FIG. 5*a* so that the frequency of the master oscillator—it being assumed that the tone C_5 of a frequency of 4,186 c.p.s. has also to be produced—is equal to $8\times20\times4{,}186=\pm670$ k.c.p./s. To the terminals S_1 to S_{12} are connected the additional 2-dividers to obtain the lower octave tones.

The master oscillator is in this case continuously and stepwise tunable. By choosing each step of detuning equal to half a tone, transposition is possible in a simple manner. The continuous detuning permits of adapting accurately the pitch of the whole instrument to that of other instruments, with which it should be played. It is furthermore possible to obtain special effects, for example, those of a Hawaiian guitar by having detuning performed over a given range at each depression of a key.

What is claimed is:

1. A method of producing a preselected tone of a musical scale, comprising generating a first frequency of the scale, generating a second frequency in the same scale, dividing the first frequency by an integral divisor, and subtracting the results of the division from the second generated frequency, whereby the result of the subtraction is the preselected tone.

2. A method as claimed in claim 1; wherein the step of generating the second frequency comprises the steps of generating a fourth frequency of the same scale, generating a fifth frequency of the same scale, dividing the fourth frequency by a second integral divisor, and subtracting the result of the division by the second integral divisor from the fifth frequency; and wherein the steps of generating the fourth, fifth and every other frequency of the scale with the exception of the first frequency comprise the steps of dividing a frequency of the scale other than the frequency to be generated by an *N*th integral factor, and subtracting the result of the division by the *N*th integral factor from an additional frequency different from the frequency to be generated and different from the frequency divided by the *N*th integral factor.

3. A method as claimed in claim 2, wherein the frequencies are generated in accordance with the relation

$$f_{n13}=f_{n12}-(1/20)f_n=f_{n12}-(1/10)f_{n112},$$

where *n* is the ordinal number of the tone in the scale.

4. A method as claimed in claim 11, wherein the frequency are generated in accordance with the relation

$$f_{n13}=f_{n12}-(1/15)f_{n15}=f_{n12}-(1/30)f_{n+7}$$

5. Apparatus for producing a predetermined tone of a musical scale from a first and a second different additional tones of that scale, comprising means for dividing the frequency of the first tone by an integer, a bistable multivibrator having first and second input terminals and switchable to a first stable state in response to the trailing edge of an input pulse in the first terminal and switchable to a second stable state in response to the trailing edge of a pulse on the second input terminal, means for connecting the output of the divider to the first input terminal of the bistable multivibrator, whereby pulses from the divider trigger the multivibrator to the first stable state, a first AND gate means connected to the second input terminal of the multivibrator and to the second tone of the scale for triggering the multivibrator into the second stable state in response to the concurrence of a pulse of the second tone and the first stable state of the multivibrator, and a second AND gate means for providing output pulses from the apparatus in response to the concurrence of pulses of the second tone and the second stable state of the multivibrator.

6. Apparatus for producing a predetermined tone of a musical scale from a first and second different tones NAND gate the same scale, comprising a first group of six NAND gate stages, a second group of three additional NAND gate stages, means for connecting an output of each of the first group of NAND gate stages of the first group to an input terminal of the next succeeding stage, means for connecting an output of each of the second group of NAND gates to an input of the next succeeding stage of the second group, means for connecting the first tone to inputs of the first and fifth NAND gates of the first group, means for connecting an output of the first NAND gate of the first group to an input of the third NAND gate of the first group, means for cross-coupling the second NAND gate of the first group with the first NAND gate of the second group, means for cross-coupling the fourth NAND gate of the first group with the third NAND gate of the second group, means for connecting the second tone of the scale to an input of the fourth NAND gate of the first group and to inputs of the first and second NAND gates of the second group, the outputs from the fifth and sixth NAND gates comprising mutually reciprocal outputs of the apparatus.

7. A device for producing a substantially equally tempered 12-tone scale, comprising an oscillator, a series of 11 cutoff circuit means each having first and second input terminals and an output terminal for removing a cycle of a signal applied to the first input terminal of the cutoff circuit in response to each cycle of a different signal applied to the second input terminal of the cutoff circuit and for providing the thus-altered signal on the output terminal of the cutoff circuit, 10 20-dividers each providing one output pulse in response to each 20 input pulses, two 10-dividers each providing one output pulse in response to each 10 input pulses, two 2-dividers each providing a single output pulse in response to each two input pulses, means for connecting the output terminal of each of the first 10 cutoff circuits to the first input terminal of the next sequential cutoff circuit in the series, means for connecting the oscillator to the first terminal of the first cutoff circuit and through the first 20-divider to the second input terminal of the third cutoff circuit of the series, means for connecting the output terminal of the first cutoff circuit to the second input terminal of the fourth cutoff circuit through the second 20-divider, means for connecting the output terminal of the second cutoff circuit to the second input terminal of the second cutoff circuit through the third 20-divider, means for connecting the output of the third cutoff circuit to the second input terminal of the sixth cutoff circuit through the fourth 20-divider, means for connecting the output of the fourth cutoff circuit to the second input terminal of the seventh cutoff circuit through the fifth 20-divider, means for connecting the output of the fifth cutoff circuit to the second input terminal of the eighth cutoff circuit through the sixth 20-divider, means for connecting the output of the sixth cutoff circuit to the second input terminal of the ninth cutoff circuit through the seventh 20-divider, means for connecting an output of the seventh cutoff circuit to the second input terminal of the tenth cutoff circuit through the eighth 20-divider, means for connecting an output of the eighth cutoff circuit to the second input terminal of the eleventh cutoff circuit through the ninth 20-divider, means for connecting the output of the ninth cutoff circuit to the input of the tenth 20-divider, means for connecting the output of the tenth cutoff circuit to the second input terminal of the first cutoff circuit through the first 10-divider, means for connecting the output of the eleventh cutoff circuit to the second input of the second cutoff circuit through the second 10-divider, means for connecting the output of each 20-divider to a separate output terminal of the tone-producing device, means for connecting the output of the 10-divider to an output ter-

minal of the tone-producing device through the first 2-divider, and means for connecting the second 10-divider to a further output terminal of the tone-producing device through the second 2-divider.

8. A device as claimed in claim 7, wherein each cutoff circuit comprises a first series of six NAND gates, a second series of three NAND gate, means for connecting an output of each of the first five NAND gates in the first series to an input of the next succeeding NAND gate in the first series, means for connecting an output of the first and second NAND gates in the second series to the next succeeding NAND gate in the second series, means for connecting the output of the first NAND gate of the first series to an input of the third NAND gate in the first series, means for connecting the first input terminal of the cutoff circuit to inputs of the first and fifth NAND gates of the first series, means for cross-coupling the second NAND gate of the first series with the first NAND gate of the second series, means for cross-coupling the fourth NAND gate of the first series with the third NAND gate of the second series, means for connecting an output of the third NAND gate of the second series to an input of the first NAND gate of the first series, means for connecting the second input terminal of the cutoff circuit to an input of the fourth NAND gate of the first series and to inputs of the first and second NAND gates of the second series, and means for connecting the output terminal of the cutoff circuit to the output of the sixth NAND gate in the first series.

9. Apparatus as claimed in claim 8, wherein each of the 2-dividers comprises a cutoff circuit wherein the input of the divider comprises the first input terminal of the cutoff circuit, wherein the output of the divider comprises the output of the third NAND gate in the second series, and wherein the output of the fifth NAND gate in the first series is connected to the second input terminal of the cutoff circuit.

10. Apparatus for producing a substantially equal tempered 12-tone scale, comprising a series of 11 cutoff circuit means each having a first and second input terminals and an output terminal for removing a cycle of a signal applied to the first input terminal of the cutoff circuit in response to each cycle of a different signal applied to the second input terminal of the cutoff circuit and for providing the thus altered signal on the output terminal of the cutoff circuit, a series of 10 20-dividers for providing an output pulse in response to each 20 input pulses applied to the 20-divider, two 5-dividers for providing an output pulse in response to each five input pulses applied to the 5-divider, two 4-dividers for providing a single pulse in response to each four input pulses applied to the 4-divider, two 3-divider for providing a single output pulse in response to each three input pulses applied to the 3-divider, an oscillator connected to the first input terminal of the first cutoff circuit, means for connecting the output of each of the first 10 cutoff circuits to an input of the next succeeding cutoff circuit, means for connecting the output of the oscillator to the second input terminal of the third cutoff circuit through the first 20-divider, means for connecting the output of the first cutoff circuit to the second input of the fourth cutoff circuit through the second 20-divider, means for connecting the output of the second cutoff circuit to the second input of the fifth cutoff circuit through the third 20-divider, means for connecting the output of the third cutoff circuit to an input of the first 5-divider, means for connecting the output of the first 5-divider to the second input of the first cutoff circuit through the first 3-divider and to the second input terminal of the sixth cutoff circuit through the first 4-divider, means for connecting the output of the fourth cutoff circuit to an input of the second 5-divider, means for connecting the output of the second 5-divider to the second input terminal of the second cutoff circuit through the second 3-divider and to the second input terminal of the seventh cutoff circuit through the second 4-divider, means for connecting the output of the fifth cutoff circuit to the second input terminal of the eighth cutoff circuit through the fourth 20-divider, means for connecting the output of the sixth cutoff circuit to the second input terminal of the ninth cutoff circuit through the fifth 20-divider, means for connecting the output of the seventh cutoff circuit to the second input terminal of the tenth cutoff circuit through the sixth 20--divider, means for connecting the output of the eighth cutoff circuit to the second input terminal of the eleventh cutoff circuit through the seventh 20-divider, means for connecting the output of the ninth cutoff circuit to the input of the eighth 20-divider, means for connecting the output of the tenth cutoff circuit to the input of the ninth 20-divider, means for connecting the output of the eleventh cutoff circuit to the input of the tenth 20-divider, means for connecting each output of the 20-divider to separate output terminals of the tone-producing apparatus, and means for connecting the output of the 4-divider to additional output terminals of the tone-generating apparatus.

11. Apparatus as claimed in claim 10, wherein each cutoff circuit comprises a first series of six NAND gates, a second series of three NAND gates, means for connecting an output of each of the first five NAND gates in the first series to an input of the next succeeding NAND gate in the first series, means for connecting an output of the first and second NAND gates in the second series to the next succeeding NAND gate in the second series, means for connecting the output of the first NAND gate of the first series to an input of the third NAND gate in the first series, means for connecting the first input terminal of the cutoff circuit to inputs of the first and fifth NAND gates of the first series, means for cross-coupling the second NAND gate of the first series with the first NAND gate of the second series, means for cross-coupling the fourth NAND gate of the first series with the third NAND gate of the second series, means for connecting an output of the third NAND gate of the second series to an input of the first NAND gate of the first series, means for connecting the second input terminal to the cutoff circuit to an input of the fourth NAND gate of the first series and to inputs of the first and second NAND gates of the second series, and means for connecting the output terminal of the cutoff circuit to the output of the sixth NAND gate in the first series.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,617,901 Dated November 2, 1971

Inventor(s) NICO VALENTINUS FRANSSEN

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 1, line 28, "10^{15}" should be --10^{-5}--;

Col. 1, line 42, "$e_1=c_2-1/3g_1$" should be --$e_1=c_2-1/2g_1$--;

Col. 1, lines 47 and 48, $f_{n13}=f_{n12}-1/20f_n=f_{n12}-1/10f_{n112}$" should be --$f_{n-3}=f_{n-2}-1/20f_n=f_{n-2}-1/10f_{n-12}$--;

Col. 1, line 65, "f_{12}=1.781 749" should be --f_{12}=1.887 749--;

Col. 2, line 18, "f_2=1,059 460-3.1" should be --f_2=1.059 460-3.1--;

Col 2, line 19, "f_3=1,122 455-6,2" should be --f_3=1.122 455-6.2--;

Col. 2, line 20, "f_2=1,059 460-3,1" should be --f_2=1.059 460-3.1--;

Col. 2, line 21, "f_3=1,122 455-6,2" should be --f_3=1.122 455-6.2--;

Col. 2, line 22, "f_4=1,189 196-9,3" should be --f_4=1.189 196-9.3--;

Col. 2, line 23, "f_5=1,259 905-12,4" should be --f_5=1.259 905-12.4-;

Col. 2, line 24, "f_6=1,334 819-15,5" should be -f_6=1.334 819-15.5--;

Col. 2, line 25, "f_7=1,414 187-18,4" should be --f_7=1.414 187-18.4-;

Col. 2, line 26, "f_8=1,498 275-21,3" should be --f_8=1.498 275-21.3-;

Col. 2, line 27, "$f_9$1,587 366-22,4" should be --f_9=1.587 366-22.4--;

Col. 2, line 28, "f_{10}=1,681 753-23,5" should be--f_{10}=1.681 753-23.5;

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 2, line 29, "f_{11}=1,781 809+6,2" should be --f_{11}=1.781 809+6.2-

Col. 2, line 30, "f_{12}=1,887 754+3,1" should be -f_{12}=1.887 754+3.1--

Col. 2, line 32, "$30x10^{15}$" should be --$30x10^{-5}$--;

Col. 2, line 37, "$f_{n13}=f_{n12}-1/15f_{n15}=f_{n12}-1/30f_{n+7}$" should be --$f_{n-3}=f_{n-2}-1/15f_{n-5}=f_{n-2}-1/30f_{n+7}$--;

Col. 2, line 38, "f_{n15}" should be --f_{n-5}--;

"f_{n112}" should be --f_{n-12}--;

Col. 2, line 40, "$1/15f_{n15}$" should be --$1/15f_{n-5}$--;

"$0.1f_{n112}$" should be --$0.1f_{n-12}$--;

Col. 2, line 56, "1/n" should be --1/m--;

Col. 2, line 61, "$N_{n13}=N_{n12}-1/20N_n$" should be --$N_{n-3}=N_{n-2}-1/20N_n$--;

Col. 2, line 62, "N_{n12}" should be --N_{n-2}--;

Col. 2, line 63, "N_{n13}" should be --N_{n-3}--;

Col. 2, line 64, "N_{n12}" should be --N_{n-2}--;

Col. 2, line 66, "N_{n12}" should be --N_{n-2}--;

Col. 2, line 67, "N_{n13}" should be --N_{n-3}--;

Col. 6, line 12, cancel "conventional";

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,617,901 Dated November 2, 1971

Inventor(s) NICO VALENTINUS FRANSSEN

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 6, line 13, after "logical" insert --conventional--;

Col. 7, line 7, cancel "out-";

Col. 7, line 8, cancel "put";

Col. 7, line 12, cancel ".5" and insert --5--;

Col. 9, line 11, "an" should be --and--;

Col. 9, line 17 "and" first occurence should be --to--;

Col. 9, line 17, "and" 2nd occurence should be --to--;

Col. 9, line 17, "and" 3rd occurence should be --are--;

IN THE CLAIMS

Claim 3, line 3, "$f_{n13}=f_{n12}-(1/20)\,fn=f_{n12}-(1/10)\,f_{n112}$ should be --$f_{n-3}=f_{n-2}-(1/20)\,f_n=f_{n-2}-(1/10)\,f_{n-12}$--;

Claim 4, line 1, "11" should be --2--;

Claim 4, line 3, "$f_{n13}=f_{n12}-(1/15)\,f_{n15}=f_{n12}-(1/30)\,fn+7$ should be --$f_{n-3}=f_{n-2}-(1/15)\,f_{n-5}=f_{n-2}-(1/30)\,f_{n+7}$ --;

Claim 6, line 2, "NAND gate" should be --of--;

Claim 7, line 22, "second" 2nd occurence should be --fifth--.

Signed and sealed this 9th day of May 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents