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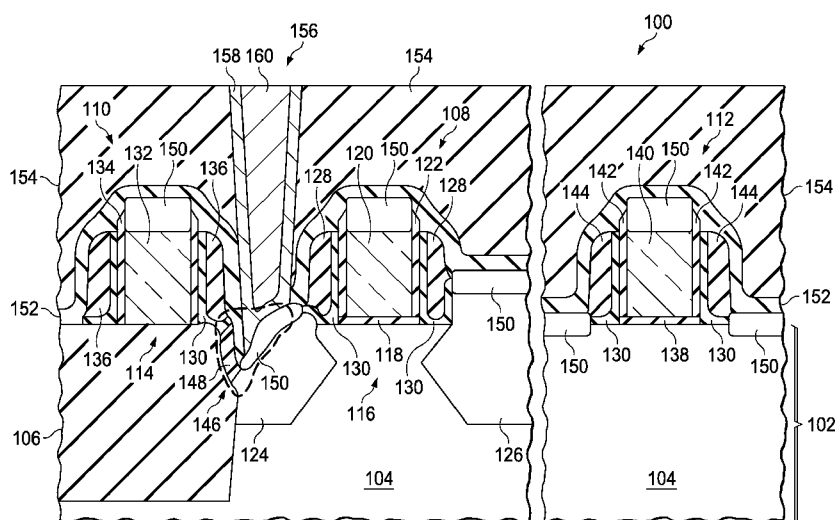
(54) **Title:** FORMING SILICIDE AND CONTACT AT EMBEDDED EPITAXIAL FACET

FIG. 1

(57) **Abstract:** In described examples, an integrated circuit (100) is formed with an MOS transistor (108) abutting field oxide (106) and a gate structure (110) on the field oxide (106) adjacent to the MOS transistor (108). A gap (146) between an epitaxial source/drain (124) and the field oxide (106) is formed with a silicon dioxide-based gap filler (148) in the gap (146). Metal silicide (150) is formed on the exposed epitaxial source/drain region (124). A CESL (152) is formed over the integrated circuit (100), and a PMD layer (154) is formed over the CESL (152). A contact (156) is formed through the PMD layer (154) and CESL (152) to make an electrical connection to the metal silicide (150) on the epitaxial source/drain region (124).

**Declarations under Rule 4.17:**

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- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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## FORMING SILICIDE AND CONTACT AT EMBEDDED EPITAXIAL FACET

## BACKGROUND

[0001] This relates in general to integrated circuits, and in particular to epitaxial regions of MOS transistors in integrated circuits.

[0002] An integrated circuit may include a metal oxide semiconductor (MOS) transistor with epitaxial source/drain regions. For example, a p-channel metal oxide semiconductor (PMOS) transistor may have silicon-germanium epitaxial source/drain regions. An n-channel metal oxide semiconductor (NMOS) transistor may have phosphorus-doped silicon epitaxial source/drain regions. An instance of the epitaxial source/drain regions may abut field oxide formed by a shallow trench isolation (STI) process. The epitaxial source/drain region may have a highly angled surface facet and a cavity between the epitaxial material and the dielectric material of the field oxide.

[0003] A gate structure may be located on the field oxide adjacent to the epitaxial source/drain region so that dielectric spacer material on a lateral surface of the gate structure may extend into the cavity and down to the epitaxial material, reducing an area for metal silicide on the epitaxial source/drain region. A contact disposed on the epitaxial source/drain region may undesirably provide a high resistance connection to the MOS transistor due to the reduced silicide area and possibly in combination with alignment tolerance of the contact to the source/drain region.

## SUMMARY

[0004] In described examples, an integrated circuit containing an MOS transistor abutting field oxide and a gate structure on the field oxide adjacent to a source/drain region of the MOS transistor is formed by forming a patterned epitaxy hard mask layer over the MOS transistor and the gate structure on the field oxide, which exposes the source/drain between the field oxide and a gate structure of the MOS transistor. Semiconductor material is epitaxially formed in the source/drain regions, so that an epitaxial source/drain region of the MOS transistor abutting the field oxide may have a highly angled surface facet and a gap may exist between the epitaxial semiconductor material and the dielectric material of the field oxide. A silicon dioxide-based gap filler is formed in the gap between the epitaxial semiconductor material and the dielectric

material of the field oxide. Source/drain spacers are subsequently formed adjacent to lateral surfaces of the MOS gate structure and the gate structure on the field oxide. Metal silicide is formed on the exposed epitaxial semiconductor material. A conformal contact etch stop liner is formed over the MOS transistor and the gate structure on the field oxide. A contact is formed to the metal silicide on the epitaxial source/drain region abutting the field oxide.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is a cross-section of an example integrated circuit containing a gap filler.

[0006] FIG. 2A through FIG. 2H are cross-sections of the integrated circuit of FIG. 1, depicted in successive stages of fabrication.

[0007] FIG. 3A through FIG. 3G are cross-sections of another example integrated circuit depicted in successive stages of fabrication.

#### DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] An integrated circuit containing an MOS transistor abutting field oxide and a gate structure on the field oxide adjacent to a source/drain region of the MOS transistor is formed by forming a patterned epitaxy hard mask layer over the MOS transistor and the gate structure on the field oxide, which exposes the source/drain between the field oxide and a gate structure of the MOS transistor. Semiconductor material is epitaxially formed in the source/drain regions, so that an epitaxial source/drain region of the MOS transistor abutting the field oxide may have a highly angled surface facet and a gap may exist between the epitaxial semiconductor material and the dielectric material of the field oxide. A silicon dioxide-based gap filler is formed in the gap between the epitaxial semiconductor material and the dielectric material of the field oxide.

[0009] In one example fabrication process sequence, a conformal layer of silicon dioxide-based dielectric material is formed over the integrated circuit, extending into the gap between the epitaxial semiconductor material and the field oxide. Subsequently an isotropic etchback process removes the silicon dioxide-based dielectric material from over the MOS transistor and the gate structure on the field oxide, leaving the gap filler. Source/drain spacers which are predominantly non-silicon dioxide are formed adjacent to the gate structure of the MOS transistor and the gate structure on the field oxide which advantageously leave at least one half of the epitaxial source/drain region of the MOS transistor abutting the field oxide exposed.

[0010] In another example fabrication process sequence, a silicon dioxide-based first sublayer of source/drain spacers is conformally formed over the integrated circuit, extending into the gap

between the epitaxial semiconductor material and the field oxide. Subsequently an anisotropic etchback process removes the first sublayer from top surfaces of the MOS transistor and the gate structure on the field oxide, leaving first source/drain spacers adjacent to the gate structure of the MOS transistor and the gate structure on the field oxide. The first spacer on the gate structure on the field oxide extends into the gap between the epitaxial semiconductor material and the field oxide, providing the gap filler. A silicon nitride-based second sublayer of the source/drain spacers is conformally formed over the integrated circuit. An anisotropic etchback removes the second sublayer to leave silicon nitride-based second spacers. At least one third of the epitaxial source/drain region of the MOS transistor abutting the field oxide is exposed.

**[0011]** Following formation of the gap filler, such as by either of the example fabrication process sequences described above, metal silicide is formed on the exposed epitaxial source/drain region. A conformal contact etch stop layer (CESL) is formed over the integrated circuit and a pre-metal dielectric (PMD) layer is formed over the CESL. A contact is formed through the PMD layer and CESL to make an electrical connection to the metal silicide on the epitaxial source/drain region.

**[0012]** FIG. 1 is a cross-section of an example integrated circuit containing a gap filler. The integrated circuit 100 is formed in and on a substrate 102 which includes semiconductor material 104 such as single crystal silicon extending to a top surface of the substrate 102. Field oxide 106 is formed in the substrate 102, for example using a STI process.

**[0013]** The integrated circuit 100 includes a first MOS transistor 108 having a first polarity adjacent to the field oxide 106, a gate structure 110 on the field oxide 106 adjacent to the first MOS transistor 108, and a second MOS transistor 112 having a second, opposite, polarity. A top surface 114 of the field oxide 106 is coplanar within 20 nanometers with a top surface 116 of the semiconductor material 104 under the first MOS transistor 108.

**[0014]** The first MOS transistor 108 includes a gate dielectric layer 118 at the top surface of the semiconductor material 104. The gate dielectric layer 118 may include silicon dioxide formed by thermal oxidation of the semiconductor material 104. The gate dielectric layer 118 may include deposited dielectric materials with high dielectric constants such as hafnium oxide, zirconium oxide and/or tantalum oxide. The first MOS transistor 108 includes a gate 120 over the gate dielectric layer 118. The gate 120 may include polycrystalline silicon, commonly referred to as polysilicon. The first MOS transistor 108 may include gate offset spacers 122 on

lateral surfaces of the gate 120. The gate offset spacers 122 may include one or more layers of thermal oxide, deposited silicon dioxide and/or deposited silicon nitride. The first MOS transistor 108 includes a first epitaxial source/drain region 124 in the substrate 102 between the gate 120 and the field oxide 106, such that the first epitaxial source/drain region 124 abuts the field oxide 106. The first MOS transistor 108 also includes a second epitaxial source/drain region 126 in the substrate 102 adjacent to the gate 120 opposite from the first epitaxial source/drain region 124. The first MOS transistor 108 includes source/drain spacers 128 laterally adjacent to the gate 120 and abutting the gate offset spacers 122 if present. The source/drain spacers 128 include one or more layers of silicon nitride and/or silicon oxynitride or other non-silicon dioxide dielectric material. The first MOS transistor 108 may include an optional spacer liner 130 of silicon dioxide-based dielectric material under the source/drain spacers 128. The spacer liner 130 may be 3 nanometers to 10 nanometers thick.

**[0015]** The gate structure 110 may possibly have a gate dielectric layer of the same material as the gate dielectric layer 118 if the gate dielectric layer 118 is a deposited dielectric layer which is concurrently deposited on the semiconductor material 104 and the field oxide 106. If the gate dielectric layer 118 is, on the other hand, a thermally grown oxide layer which does not form on the field oxide 106, the gate structure 110 may be free of a gate dielectric layer, as depicted in FIG. 1. The gate structure 110 includes a gate 132 over the field oxide 106 and over the gate dielectric layer of the gate structure 110, if present. In the instant example, the gate 132 does not overlap an edge of the field oxide 106 adjacent to the first MOS transistor 108. The gate 132 may have the same composition and structure as the gate 120 of the first MOS transistor 108. The gate structure 110 may include gate offset spacers 134 on lateral surfaces of the gate 132 if the first MOS transistor 108 includes the gate offset spacers 122. The gate offset spacers 134 may have a similar composition and structure as the gate offset spacers 122 of the first MOS transistor 108. The gate structure 110 includes source/drain spacers 136 laterally adjacent to the gate 132 and abutting the gate offset spacers 134 if present. The source/drain spacers 136 have the same structure and composition as the source/drain spacers 128 of the first MOS transistor 108. The gate structure 110 may include the spacer liner 130 if present in the first MOS transistor 108.

**[0016]** The second MOS transistor 112 includes a gate dielectric layer 138 at the top surface of the semiconductor material 104. The gate dielectric layer 138 may possibly have the same

composition and structure as the gate dielectric layer 118 of the first MOS transistor 108. The second MOS transistor 112 includes a gate 140 over the gate dielectric layer 138. The gate 140 may possibly have a similar composition and structure as the gate 120 of the first MOS transistor 108. The second MOS transistor 112 may include gate offset spacers 142 on lateral surfaces of the gate 140. The gate offset spacers 142 may include one or more layers of thermal oxide, deposited silicon dioxide and/or deposited silicon nitride, and may possibly have a similar structure and composition as the gate offset spacers 122 of the first MOS transistor 108. The second MOS transistor 112 includes source/drain spacers 144 laterally adjacent to the gate 140 and abutting the gate offset spacers 142 if present. The source/drain spacers 144 may possibly have the same structure and composition as the source/drain spacers 128 of the first MOS transistor 108. The second MOS transistor 112 may include the spacer liner 130 if present in the first MOS transistor 108.

[0017] The first epitaxial source/drain region 124 has an angled facet facing the field oxide 106 and so is laterally separated from the field oxide 106 at the top surface 114 of the field oxide 106, forming a gap 146 between the first epitaxial source/drain region 124 and the field oxide 106 which extends at least 20 nanometers down from the top surface 114. A silicon dioxide-based gap filler 148 is disposed in the gap 146 abutting the field oxide 106 and extending down to and contacting the first epitaxial source/drain region 124 at a bottom of the gap 146. In the instant example, the gap filler 148 extends up to the source/drain spacers 136 of the gate structure 110, touching the spacer liner 130 if present, or touching the source/drain spacers 136 if the spacer liner 130 is not present.

[0018] Metal silicide 150 is disposed on the first epitaxial source/drain region 124 and on the second epitaxial source/drain region 126. Additional metal silicide 150 may be disposed on source/drain regions of the second MOS transistor 112, on the gate 120 of the first MOS transistor 108, on the gate 132 of the gate structure 110 and on the gate 140 of the second MOS transistor 112. The metal silicide 150 on the first epitaxial source/drain region 124 extends into the gap 146 on the angled facet and covers at least one half of the first epitaxial source/drain region 124. The metal silicide 150 may include, for example, nickel silicide.

[0019] A CESL 152 is disposed over the first MOS transistor 108, the gate structure 110 and the second MOS transistor 112. The CESL 152 is predominantly non-silicon dioxide-based dielectric material such as silicon nitride, 10 nanometers to 30 nanometers thick. A PMD layer

154 is disposed over the CESL 152. The PMD layer 154 may be silicon dioxide-based dielectric material such as boron phosphorus silicate glass (BPSG). The PMD layer 154 may be planarized as depicted in FIG. 1, and may be, for example, 50 nanometers to 150 nanometers thick over the first MOS transistor 108, the gate structure 110 and the second MOS transistor 112.

**[0020]** A contact 156 is disposed through the PMD layer 154 and the CESL 152 to make direct connection with the metal silicide 150 on the first epitaxial source/drain region 124. The contact 156 may include a metal liner 158 of titanium and titanium nitride, and a fill metal 160 of tungsten. The gap filler 148 may prevent the gap 146 from being filled with the source/drain spacers 136 and the CESL 152, thus advantageously allowing the metal silicide 150 to occupy a larger fraction of the angled facet of the first epitaxial source/drain region 124 and provide a lower resistance connection between the contact 156 and the first epitaxial source/drain region 124.

**[0021]** In one version of the instant example, the first MOS transistor 108 may be a PMOS transistor 108, and the first epitaxial source/drain region 124 and the second epitaxial source/drain region 126 may be silicon-germanium, and the second MOS transistor 112 may be an NMOS transistor 112. In an alternate version, the first MOS transistor 108 may be an NMOS transistor 108, and the first epitaxial source/drain region 124 and the second epitaxial source/drain region 126 may be phosphorus doped silicon, and the second MOS transistor 112 may be a PMOS transistor 112.

**[0022]** FIG. 2A through FIG. 2H are cross-sections of the integrated circuit of FIG. 1, depicted in successive stages of fabrication. Referring to FIG. 2A, the integrated circuit 100 has completed formation of epitaxial source/drain regions for transistors having the first polarity. The first MOS transistor 108 has the gate dielectric layer 118, the gate 120, the gate offset spacers 122 and the first epitaxial source/drain region 124 and the second epitaxial source/drain region 126 in place. The gate structure 110 has the gate 132 and the gate offset spacers 134 in place. The second MOS transistor 112 has the gate dielectric layer 138, the gate 140 and the gate offset spacers 142 in place.

**[0023]** Gate hard mask material 162 may be disposed over the gates 120, 132 and 142 from a gate etch operation. An epitaxy hard mask 164 is adjacent to lateral surfaces of the gate 120 of the first MOS transistor 108, adjacent to lateral surfaces of the gate 132 of the gate structure 110 and covers the second MOS transistor 112. The epitaxy hard mask 164 may include, for



example, silicon nitride 15 nanometers to 25 nanometers thick. The epitaxy hard mask 164 was used to define lateral extents of the first epitaxial source/drain region 124 and the second epitaxial source/drain region 126. The gap 146 between the first epitaxial source/drain region 124 and the field oxide 106 is substantially free of material.

**[0024]** Referring to FIG. 2B, a gap fill layer 166 of silicon dioxide-based dielectric material is formed over an existing top surface of the integrated circuit 100, extending into and substantially filling the gap 146. The gap fill layer 166 may include, for example, 15 nanometers to 25 nanometers of silicon dioxide formed by a plasma enhanced chemical vapor deposition (PECVD) process using tetraethyl orthosilicate, also known as tetraethoxysilane or TEOS. The thickness of the gap fill layer 166 is high enough to substantially fill the gap 146 and is low enough to avoid completely filling between the gate 120 of the first MOS transistor 108 and the gate 132 of the gate structure 110.

**[0025]** Referring to FIG. 2C, the gap fill layer 166 of FIG. 2B is removed from over the first MOS transistor 108, the gate structure 110 and the second MOS transistor 112 to leave gap filler 148 substantially filling the gap 146. The gap fill layer 166 may be removed, for example, using an isotropic plasma etch which is selective to the epitaxy hard mask 164, or possibly using a timed wet etch in an aqueous solution of dilute hydrofluoric acid.

**[0026]** Referring to FIG. 2D, the epitaxy hard mask 164 of FIG. 2C is removed, leaving the gap filler 148 substantially filling the gap 146. The epitaxy hard mask 164 may be removed, for example, using an isotropic plasma etch which is selective to silicon dioxide. The gate hard mask material 162 of FIG. 2C, if present, is also removed, possibly concurrently with the epitaxy hard mask 164, or possibly in a separate etch step. If the gate hard mask material 162 included amorphous carbon, it may be removed by ashing.

**[0027]** Referring to FIG. 2E, the optional spacer liner 130 may possibly be formed over an existing top surface of the integrated circuit 100. The spacer liner 168 may be formed, for example, by a PECVD process using TEOS.

**[0028]** A conformal layer of spacer material 168 is formed over the existing top surface of the integrated circuit 100, on the spacer liner 130 if present. The layer of spacer material 168 is predominantly non-silicon dioxide material such as silicon nitride and/or silicon oxynitride. The layer of spacer material 168 may be formed by a PECVD process using bis (tertiary-butylamino) silane (BTBAS), a PECVD process using a combination of BTBAS and TEOS, or a PECVD

process using dichlorosilane and ammonia. The layer of spacer material 168 may be, for example, 15 nanometers to 30 nanometers thick.

**[0029]** Referring to FIG. 2F, an anisotropic reactive ion etch (RIE) process removes the layer of spacer material 168 of FIG. 2E from over the gap filler 148 and the first epitaxial source/drain region 124 and the second epitaxial source/drain region 126, and from over tops of the gates 120, 132 and 140, to form the source/drain spacers 128 laterally adjacent to the gate 120 of the first MOS transistor 108, the source/drain spacers 136 laterally adjacent to the gate 132 of the gate structure 110, and the source/drain spacers 144 laterally adjacent to the gate 140 of the second MOS transistor 112. The RIE process leaves the gap filler 148 substantially intact.

**[0030]** Referring to FIG. 2G, a silicon dioxide etch removes the spacer liner 130 which is exposed by the source/drain spacers 128, 136 and 144, and removes a portion of the gap filler 148 so as to expose at least a half of the first epitaxial source/drain region 124. The silicon dioxide etch may include an RIE process or may include a timed etch in an aqueous solution of dilute hydrofluoric acid. After the silicon dioxide etch is completed, the gap filler 148 abuts the field oxide 106 and extends down to and contacts the first epitaxial source/drain region 124 at a bottom of the gap 146, and extends up to the spacer liner 130.

**[0031]** Referring to FIG. 2H, the metal silicide 150 is formed on exposed semiconductor material, including the first epitaxial source/drain region 124 and the second epitaxial source/drain region 126, and possibly the source/drain regions of the second MOS transistor 112. The metal silicide 150 may also be formed over the gates 120, 132 and 140. The metal silicide 150 on the first epitaxial source/drain region 124 extends into the gap 146 on the angled facet and covers at least one half of the first epitaxial source/drain region 124. The metal silicide 150 may be formed, for example, by depositing a layer of metal, such as nickel or cobalt, on a top surface of the integrated circuit 100, heating the integrated circuit 100 to react a portion of the metal with the exposed semiconductor material, and selectively removing unreacted metal by exposing the integrated circuit 100 to wet etchants including a mixture of an acid and hydrogen peroxide.

**[0032]** Following formation of the metal silicide 150, the CESL 152, PMD layer 154 and contact 156 are formed to provide the structure of FIG. 1. The CESL 152 may be formed, for example, by a PECVD process using dichlorosilane and ammonia. The PMD layer 154 may be formed, for example, by a PECVD process using silane, diborane, phosphine and nitrous oxide,

or a high aspect ratio process (HARP) using silane, diborane, phosphine and ozone.

[0033] The contact 156 may be formed by etching a contact hole through the PMD layer 154 and CESL 152 to expose the metal silicide 150. The metal liner 158 of titanium and titanium nitride may be formed by a sputter process and an atomic layer deposition (ALD) process respectively. The fill metal 160 of tungsten may be formed by a metal organic chemical vapor deposition (MOCVD) process. The fill metal 160 and the metal liner 158 may be removed from a top surface of the PMD layer 154 by etchback or chemical mechanical polish (CMP) processes.

[0034] FIG. 3A through FIG. 3G are cross-sections of another example integrated circuit depicted in successive stages of fabrication. Referring to FIG. 3A, the integrated circuit 300 is formed in and on a substrate 302 which includes semiconductor material 304 such as single crystal silicon extending to a top surface of the substrate 302. Field oxide 306 is formed in the substrate 302. The integrated circuit 300 includes a first MOS transistor 308 having a first polarity adjacent to the field oxide 306, a gate structure 310 on the field oxide 306 adjacent to the first MOS transistor 308, and a second MOS transistor 312 having a second, opposite, polarity. A top surface 314 of the field oxide 306 is coplanar within 20 nanometers with a top surface 316 of the semiconductor material 304 under the first MOS transistor 308. The integrated circuit 300 has completed formation of epitaxial source/drain regions for transistors having the first polarity. An epitaxy hard mask and any gate hard mask material have been removed.

[0035] The first MOS transistor 308 includes a gate dielectric layer 318 at the top surface of the semiconductor material 304. The gate dielectric layer 318 may include silicon dioxide formed by thermal oxidation of the semiconductor material 304, or may include deposited dielectric materials with high dielectric constants. The first MOS transistor 308 includes a gate 320, possibly polysilicon, over the gate dielectric layer 318. Gate offset spacers 322 may be disposed on lateral surfaces of the gate 320. The first MOS transistor 308 includes a first epitaxial source/drain region 324 in the substrate 302 between the gate 320 and the field oxide 306, such that the first epitaxial source/drain region 324 abuts the field oxide 306, and a second epitaxial source/drain region 326 in the substrate 302 adjacent to the gate 320 opposite from the first epitaxial source/drain region 324. The first epitaxial source/drain region 324 has an angled facet facing the field oxide 306 and so is laterally separated from the field oxide 306 at the top surface 314 of the field oxide 306, forming a gap 346 between the first epitaxial source/drain region 324 and the field oxide 306 which extends at least 20 nanometers down from the top

surface 314.

[0036] The gate structure 310 may possibly have a gate dielectric layer of the same material as the gate dielectric layer 318 as explained in reference to FIG. 1. The gate structure 310 includes a gate 332 over the field oxide 306; in the instant example, the gate 332 does not overlap an edge of the field oxide 306 adjacent to the first MOS transistor 308. The gate 332 may have the same composition and structure as the gate 320 of the first MOS transistor 308. Gate offset spacers 334 may be disposed on lateral surfaces of the gate 332.

[0037] The second MOS transistor 312 includes a gate dielectric layer 338 at the top surface of the semiconductor material 304, possibly having the same composition and structure as the gate dielectric layer 318 of the first MOS transistor 308. The second MOS transistor 312 includes a gate 340 over the gate dielectric layer 338, possibly with a similar composition and structure as the gate 320 of the first MOS transistor 308. Gate offset spacers 342 may be disposed on lateral surfaces of the gate 340. The gate offset spacers 342 may possibly have a similar structure and composition as the gate offset spacers 322 of the first MOS transistor 308.

[0038] A silicon dioxide-based spacer layer 370 of subsequently formed source/drain spacers is conformally formed over an existing top surface of the integrated circuit 300, extending into, and substantially filling, the gap 346. The spacer layer 370 may include, for example, 15 nanometers to 30 nanometers of silicon dioxide formed by a PECVD process using TEOS. The thickness of the spacer layer 370 is high enough to substantially fill the gap 346 and is low enough to avoid completely filling between the gates 320 and 332.

[0039] Referring to FIG. 3B, an anisotropic RIE process removes the spacer layer 370 of FIG. 3A from over a portion of the first epitaxial source/drain region 324 and from over the second epitaxial source/drain region 326, and from over tops of the gates 320, 332 and 340, to form source/drain spacers 328 laterally adjacent to the gate 320 of the first MOS transistor 308, source/drain spacers 336 laterally adjacent to the gate 332 of the gate structure 310, and source/drain spacers 344 laterally adjacent to the gate 340 of the second MOS transistor 312. The RIE process is performed so that the source/drain spacer 328 extends into the gap 346, abutting the field oxide 306 and extending down to and contacting the first epitaxial source/drain region 324 at a bottom of the gap 346, thus providing a gap filler 348.

[0040] Referring to FIG. 3C, a non-silicon dioxide-based sacrificial layer 372 is conformally formed over an existing top surface of the integrated circuit 300. The sacrificial layer 372 may

be, for example, 10 nanometers to 30 nanometers thick, and may be formed by a PECVD process using BTBAS, a PECVD process using a combination of BTBAS and TEOS, or a PECVD process using dichlorosilane and ammonia.

[0041] Referring to FIG. 3D, an anisotropic RIE process removes the sacrificial layer 372 of FIG. 3C from over a portion of the first epitaxial source/drain region 324 and a portion of the second epitaxial source/drain region 326, and from over tops of the gates 320, 332 and 340, to form sacrificial spacers 374 on the source/drain spacers 328 of the first MOS transistor 308, sacrificial spacers 376 on the source/drain spacers 328 of the gate structure 310, and sacrificial spacers 378 on the source/drain spacers 328 of the second MOS transistor 312. Forming the source/drain spacers 336 on the gate structure 310 so as to extend into the gap 346, providing the gap filler 348, may reduce a thickness of the sacrificial spacers 376 over the first epitaxial source/drain region 324, thereby exposing sufficient area for subsequent formation of metal silicide.

[0042] Referring to FIG. 3E, metal silicide 350 is formed on exposed semiconductor material, including the first epitaxial source/drain region 324 and the second epitaxial source/drain region 326, and possibly the source/drain regions of the second MOS transistor 312. The metal silicide 350 may also be formed over the gates 320, 332 and 340. The metal silicide 350 on the first epitaxial source/drain region 324 extends into the gap 346 on the angled facet and covers at least one third of the first epitaxial source/drain region 324. The metal silicide 350 may be formed, for example, as described in reference to FIG. 2H.

[0043] Referring to FIG. 3F, the sacrificial spacers 374, 376 and 378 of FIG. 3E are removed, for example using an isotropic plasma etch which is selective to the silicon-dioxide-based dielectric material of the source/drain spacers 328, 336 and 344. The gap filler 348 is substantially intact after the sacrificial spacers 374, 376 and 378 are removed.

[0044] Referring to FIG. 3G, a first sublayer 380 of a CESL 352 is formed over an existing top surface of the integrated circuit 300. The first sublayer 380 includes 2 nanometers to 10 nanometers of silicon dioxide-based dielectric material, formed by a PECVD process. A second sublayer 382 of the CESL 352 is formed on the first sublayer 380. The second sublayer 382 is predominantly non-silicon dioxide-based dielectric material such as silicon nitride, 10 nanometers to 30 nanometers thick, formed by a PECVD process. A PMD layer 354 is formed over the CESL 352, for example as described in reference to FIG. 1 and FIG. 2H. A contact 356

is formed through the PMD layer 354 and CESL 352 to make direct connection with the metal silicide 350 on the first epitaxial source/drain region 324. The contact 356 may be formed as described in reference to FIG. 2H.

**[0045]** Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

## CLAIMS

What is claimed is:

1. An integrated circuit, comprising:
  - a substrate including semiconductor material extending to a top surface of the substrate;
  - field oxide disposed in the substrate;
  - a first metal oxide semiconductor (MOS) transistor of a first polarity, including:
    - a gate dielectric layer at the top surface of the semiconductor material;
    - a gate over the gate dielectric layer of the first MOS transistor;
    - a first epitaxial source/drain region in the substrate between the gate of the first MOS transistor and the field oxide, abutting the field oxide, having an angled facet facing the field oxide such that the first epitaxial source/drain region is laterally separated from the field oxide at the top surface of the field oxide by a gap which extends at least 20 nanometers down from the top surface of the field oxide;
    - a second epitaxial source/drain region in the substrate adjacent to the gate of the first MOS transistor, opposite from the first epitaxial source/drain region; and
    - source/drain spacers laterally adjacent to the gate of the first MOS transistor;
  - a gate structure over the field oxide, including:
    - a gate over the field oxide, such that the gate of the gate structure does not overlap an edge of the field oxide; and
    - source/drain spacers laterally adjacent to the gate of the gate structure;
  - a gap filler of silicon dioxide-based dielectric material in the gap, abutting the field oxide and extending down to and contacting the first epitaxial source/drain region at a bottom of the gap;
  - metal silicide on the angled facet of the first epitaxial source/drain region; and
  - a contact on the metal silicide on the angled facet of the first epitaxial source/drain region.
2. The integrated circuit of claim 1, wherein a top surface of the field oxide is coplanar within 20 nanometers of the top surface of the substrate under the gate dielectric layer.
3. The integrated circuit of claim 1, wherein the source/drain spacers of the gate structure are predominantly non-silicon dioxide dielectric material, and the metal silicide covers at least one half of the first epitaxial source/drain region.

4. The integrated circuit of claim 3, further comprising a spacer liner of silicon dioxide-based dielectric material under the source/drain spacers of the first MOS transistor and the source/drain spacers of the gate structure.
5. The integrated circuit of claim 1, wherein the source/drain spacers of the gate structure are predominantly silicon dioxide-based dielectric material, the gap filler is a portion of the source/drain spacers of the gate structure, and the metal silicide covers at least one third of the first epitaxial source/drain region.
6. The integrated circuit of claim 1, wherein the metal silicide is predominantly nickel silicide.
7. The integrated circuit of claim 1, further comprising a second MOS transistor of a second, opposite, polarity.
8. The integrated circuit of claim 1, wherein: the first MOS transistor is a p-channel metal oxide semiconductor (PMOS) transistor; and the first epitaxial source/drain region and the second epitaxial source/drain region include silicon-germanium.
9. The integrated circuit of claim 1, wherein: the first MOS transistor is an n-channel metal oxide semiconductor (NMOS) transistor; and the first epitaxial source/drain region and the second epitaxial source/drain region include phosphorus doped silicon.
10. A method of forming an integrated circuit, comprising:
  - providing a substrate including semiconductor material extending to a top surface of the substrate;
  - forming field oxide in the substrate;
  - forming a first epitaxial source/drain region of a first MOS transistor in the substrate between a gate of the first MOS transistor and the field oxide so that the first epitaxial source/drain region has an angled facet facing the field oxide and abuts the field oxide, and such that the first epitaxial source/drain region is laterally separated from the field oxide at the top surface of the field oxide by a gap which extends at least 20 nanometers down from the top surface of the field oxide, and concurrently forming a second epitaxial source/drain region of the first MOS transistor in the substrate adjacent to the gate of the first MOS transistor and opposite from the first epitaxial source/drain region, the first MOS transistor being of a first polarity;
  - forming a layer of silicon dioxide-based dielectric material over the first MOS transistor and a gate structure located over the field oxide adjacent to the first epitaxial source/drain region,



wherein a gate of the gate structure does not overlap an edge of the field oxide, the layer of silicon dioxide-based dielectric material extending into the gap;

removing a portion of the layer of silicon dioxide-based dielectric material from over the first epitaxial source/drain region, leaving a portion of the layer of silicon dioxide-based dielectric in the gap to form a gap filler abutting the field oxide and extending down to and contacting the first epitaxial source/drain region at a bottom of the gap;

forming metal silicide on the angled facet of the first epitaxial source/drain region; and

forming a contact on the metal silicide on the angled facet of the first epitaxial source/drain region.

11. The method of claim 10, wherein a top surface of the field oxide is coplanar within 20 nanometers of the top surface of the substrate under a gate dielectric layer of the first MOS transistor.

12. The method of claim 10, further comprising:

forming a conformal layer of spacer material over the first MOS transistor, the gate structure and the gap filler, the conformal layer of spacer material being predominantly non-silicon dioxide material; and

removing the conformal layer of spacer material from over the gap filler and the first epitaxial source/drain region and the second epitaxial source/drain region and from over tops of the gates of the first MOS transistor and the gate structure, to form source/drain spacers laterally adjacent to the gate of the first MOS transistor and source/drain spacers laterally adjacent to the gate of the gate structure, so that the metal silicide covers at least one half of the first epitaxial source/drain region.

13. The method of claim 12, wherein the conformal layer of spacer material is predominantly silicon nitride.

14. The method of claim 12, further comprising:

forming a spacer liner of silicon dioxide-based dielectric material over the first MOS transistor, the gate structure and the gap filler, prior to forming the conformal layer of spacer material; and

removing the spacer line which is exposed by the source/drain spacers laterally adjacent to the gate of the first MOS transistor and the source/drain spacers laterally adjacent to the gate of the gate structure, after removing the conformal layer of spacer material.

15. The method of claim 10, wherein: the layer of silicon dioxide-based dielectric material is a spacer layer; and removing the portion of the layer of silicon dioxide-based dielectric material is performed by an anisotropic etch process leaving source/drain spacers laterally adjacent to the gate of the first MOS transistor and source/drain spacers laterally adjacent to the gate of the gate structure, so that the gap filler is a portion of the source/drain spacers laterally adjacent to the gate of the gate structure, and so that the metal silicide covers at least one third of the first epitaxial source/drain region.

16. The method of claim 15, further comprising:

forming a non-silicon dioxide-based sacrificial layer over the first MOS transistor, the gate structure, the gap filler, the source/drain spacers laterally adjacent to the gate of the first MOS transistor and the source/drain spacers laterally adjacent to the gate of the gate structure;

removing the non-silicon dioxide-based sacrificial layer by an anisotropic etch process from over a portion of the first epitaxial source/drain region and a portion of the second epitaxial source/drain region, and from over tops of the gates of the first MOS transistor and the gate structure, to form sacrificial spacers on the source/drain spacers of the first MOS transistor and sacrificial spacers on the source/drain spacers of the gate structure, before forming the metal silicide; and

removing the sacrificial spacers on the source/drain spacers of the first MOS transistor and sacrificial spacers on the source/drain spacers of the gate structure, after forming the metal silicide.

17. The method of claim 10, wherein the integrated circuit includes a second MOS transistor of a second, opposite, polarity.

18. The method of claim 10, wherein: the first MOS transistor is a PMOS transistor; and the first epitaxial source/drain region and the second epitaxial source/drain region include silicon-germanium.

19. The method of claim 10, wherein: the first MOS transistor is an NMOS transistor; and the first epitaxial source/drain region and the second epitaxial source/drain region include phosphorus doped silicon.

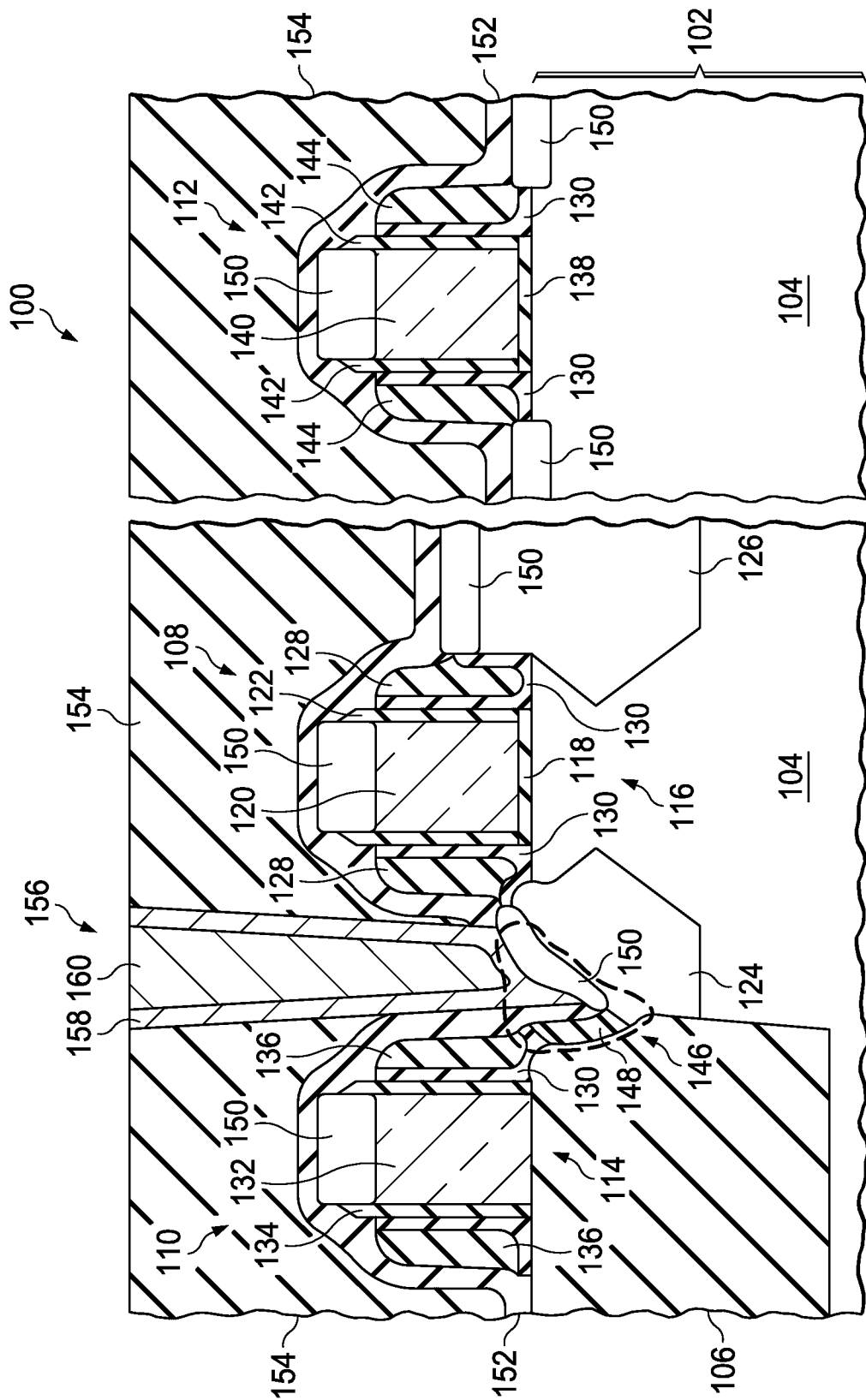


FIG. 1

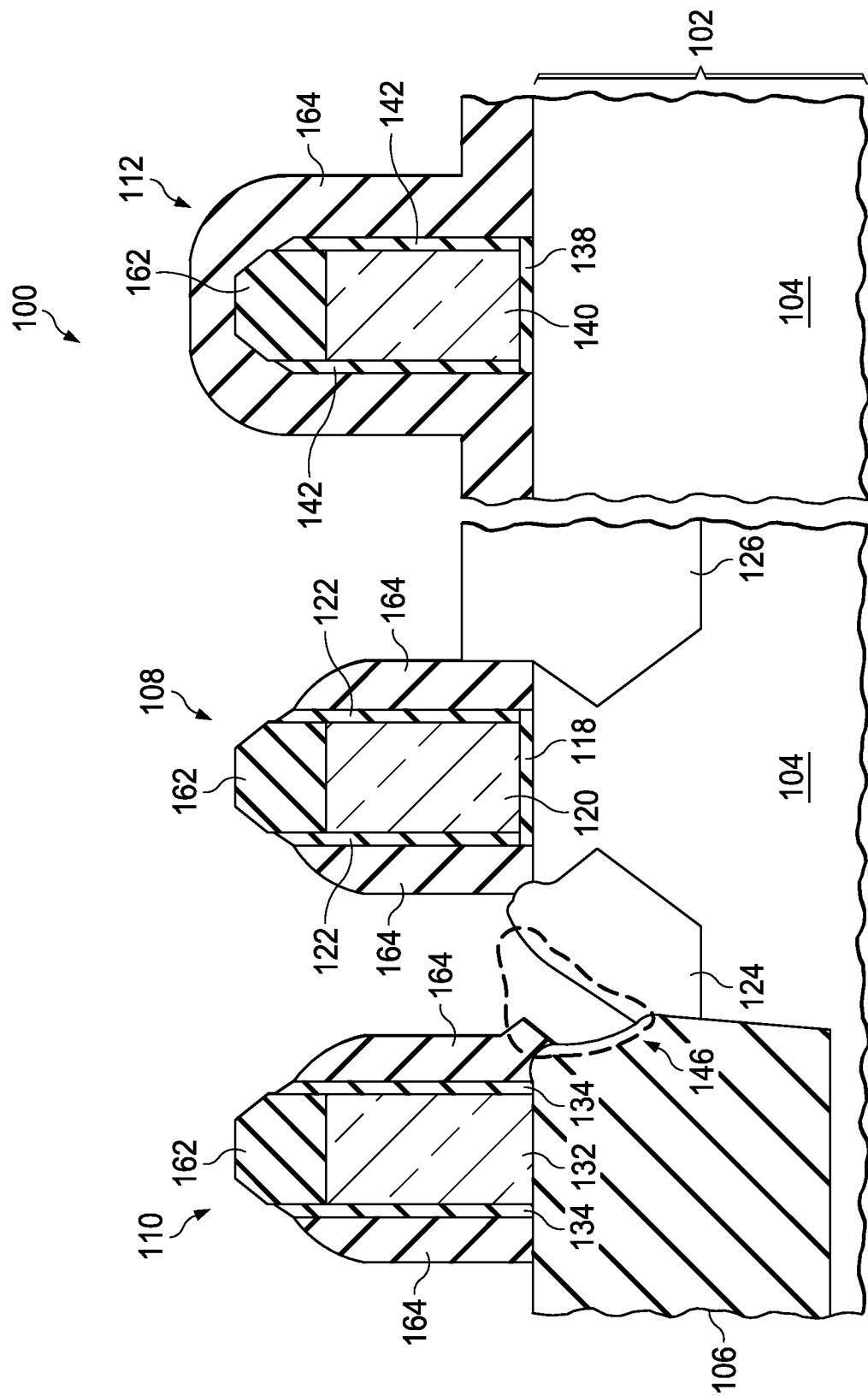


FIG. 2A

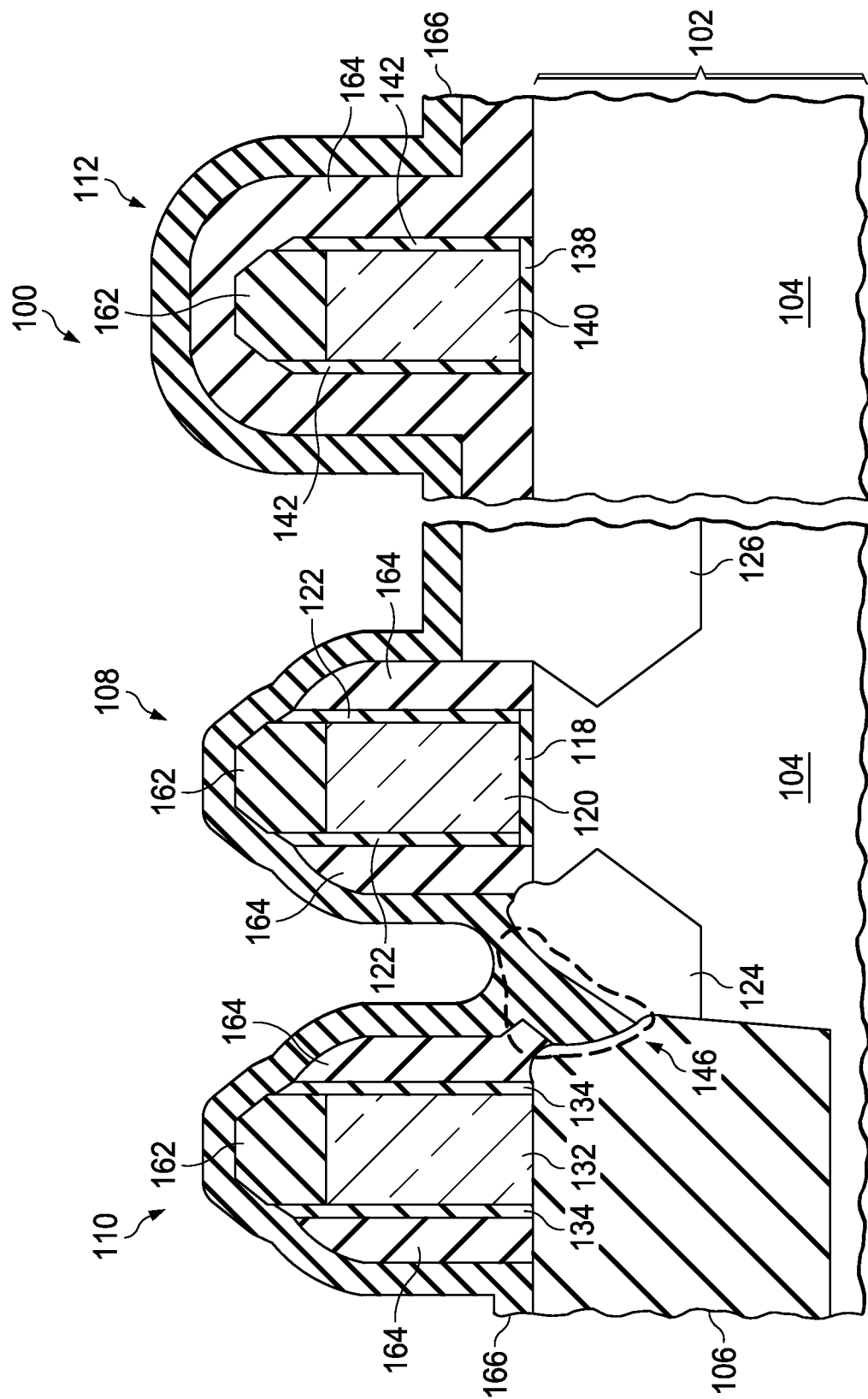


FIG. 2B

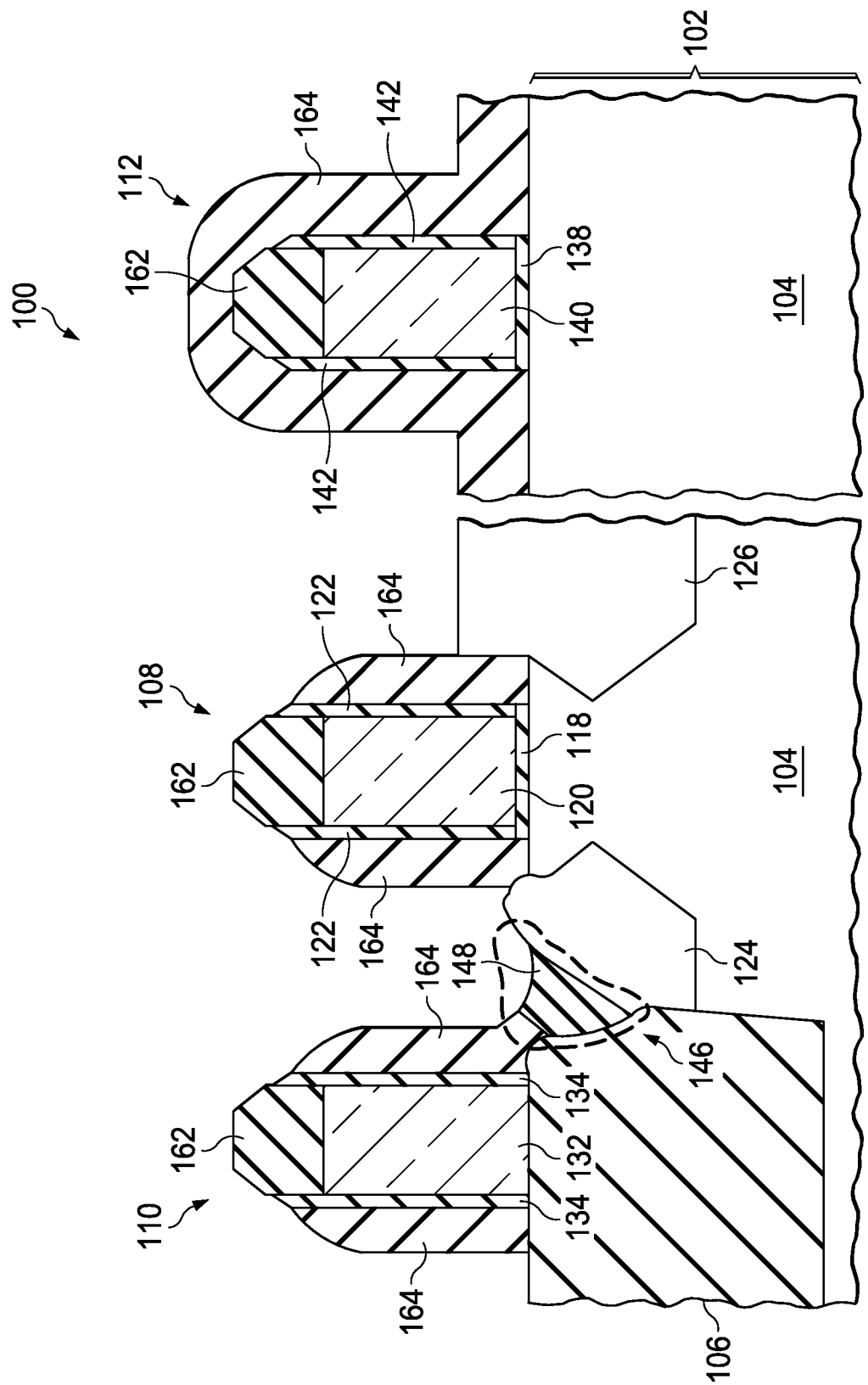


FIG. 2C

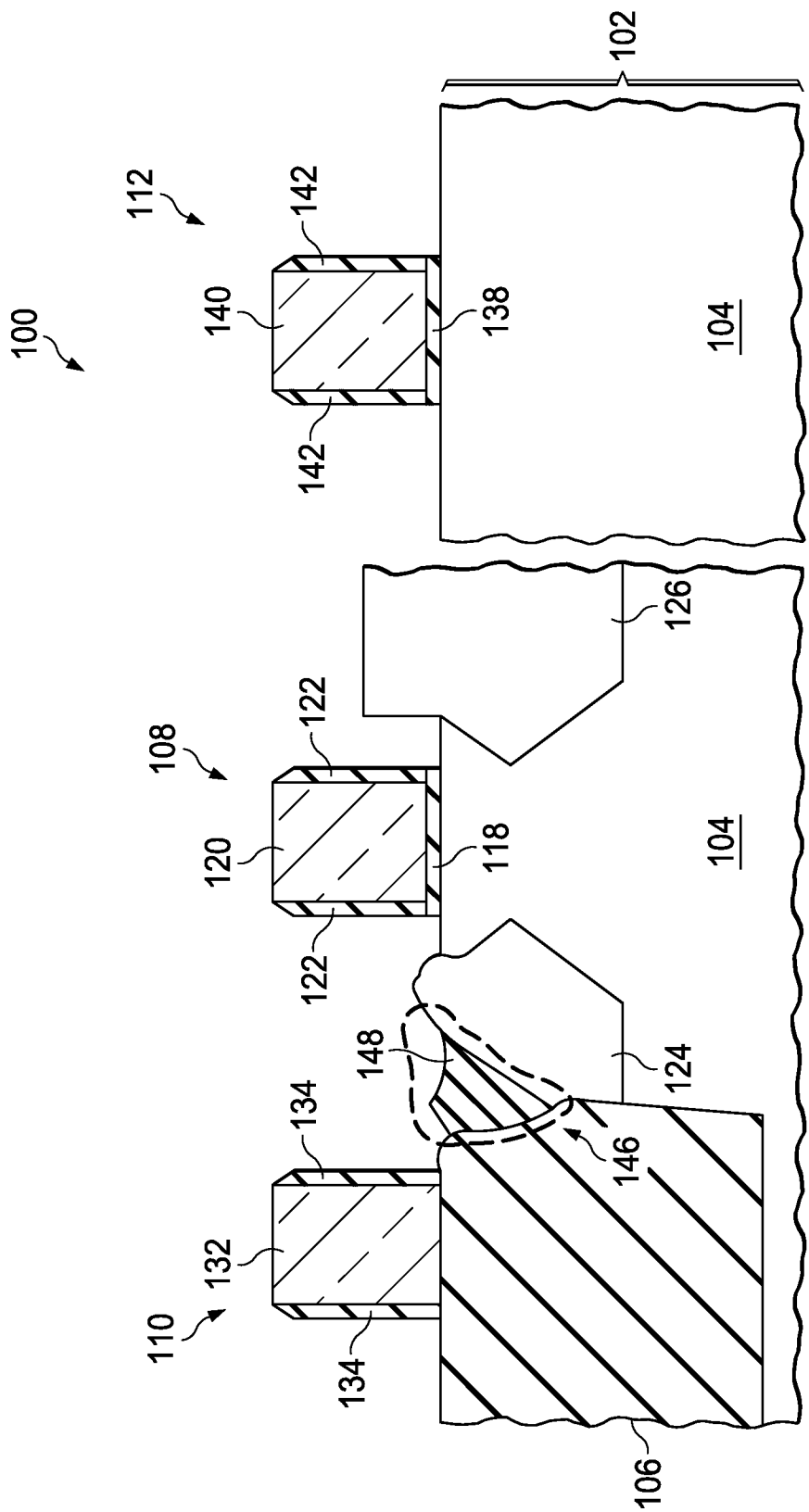


FIG. 2D

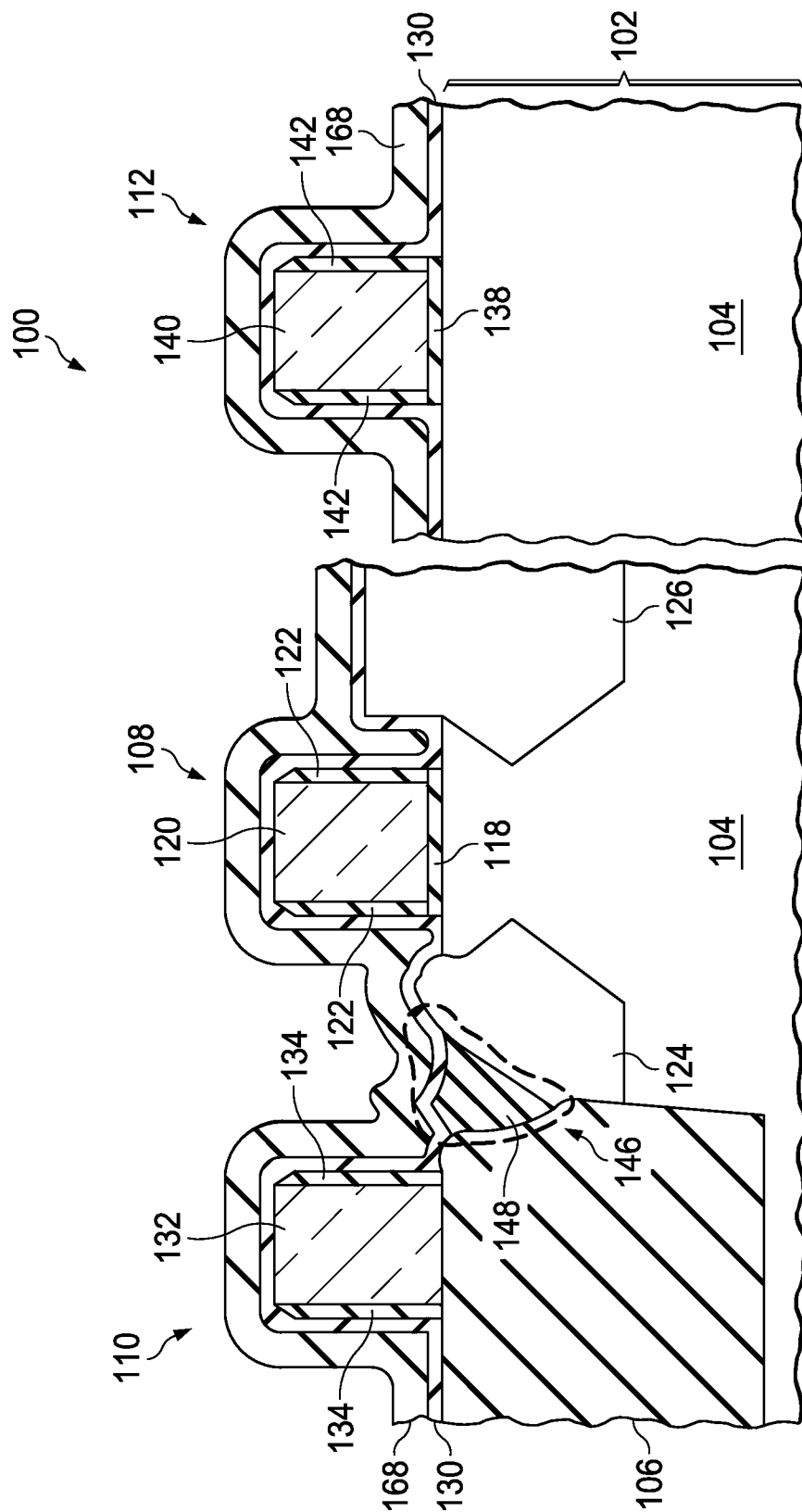


FIG. 2E



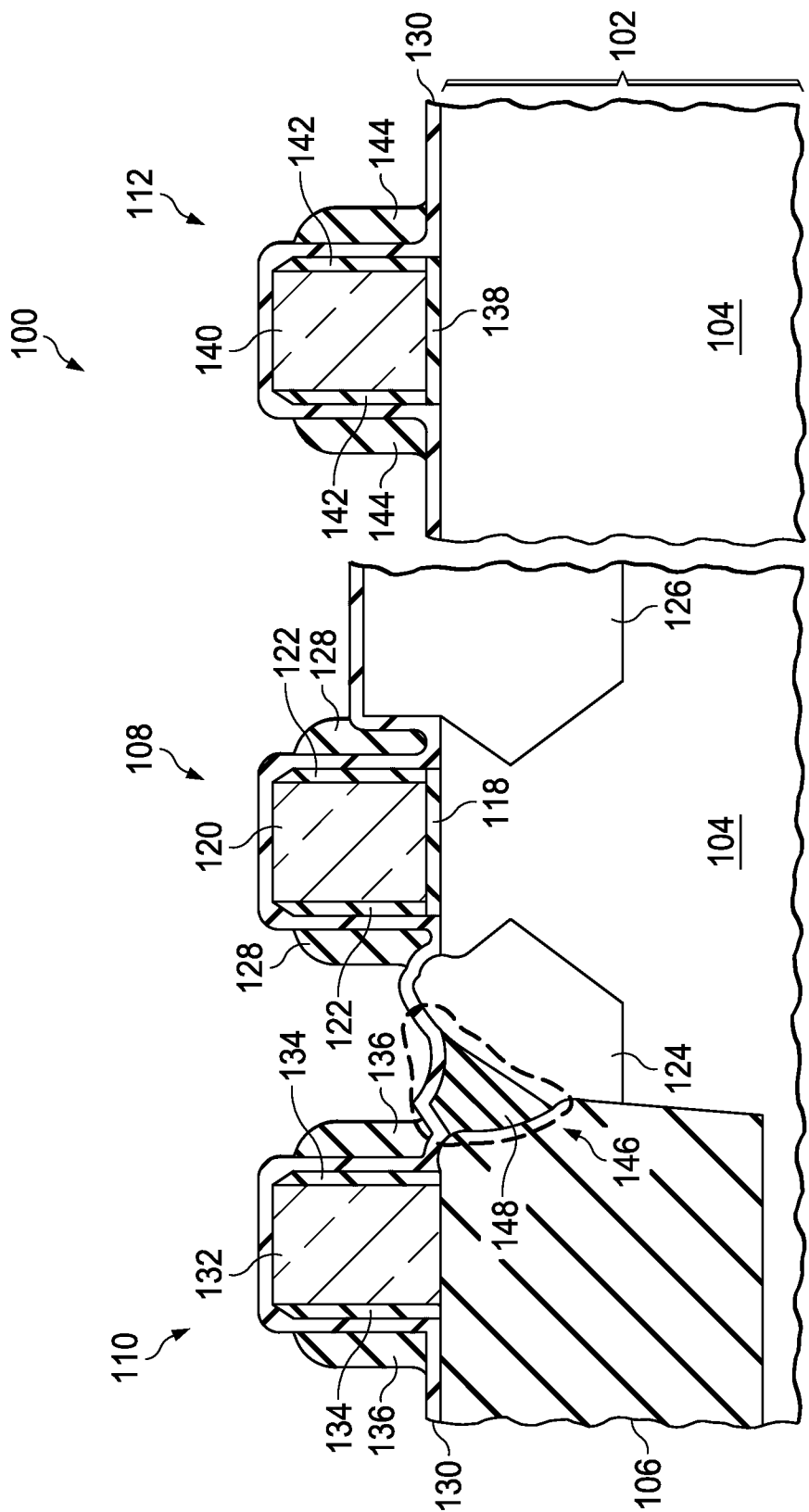


FIG. 2F

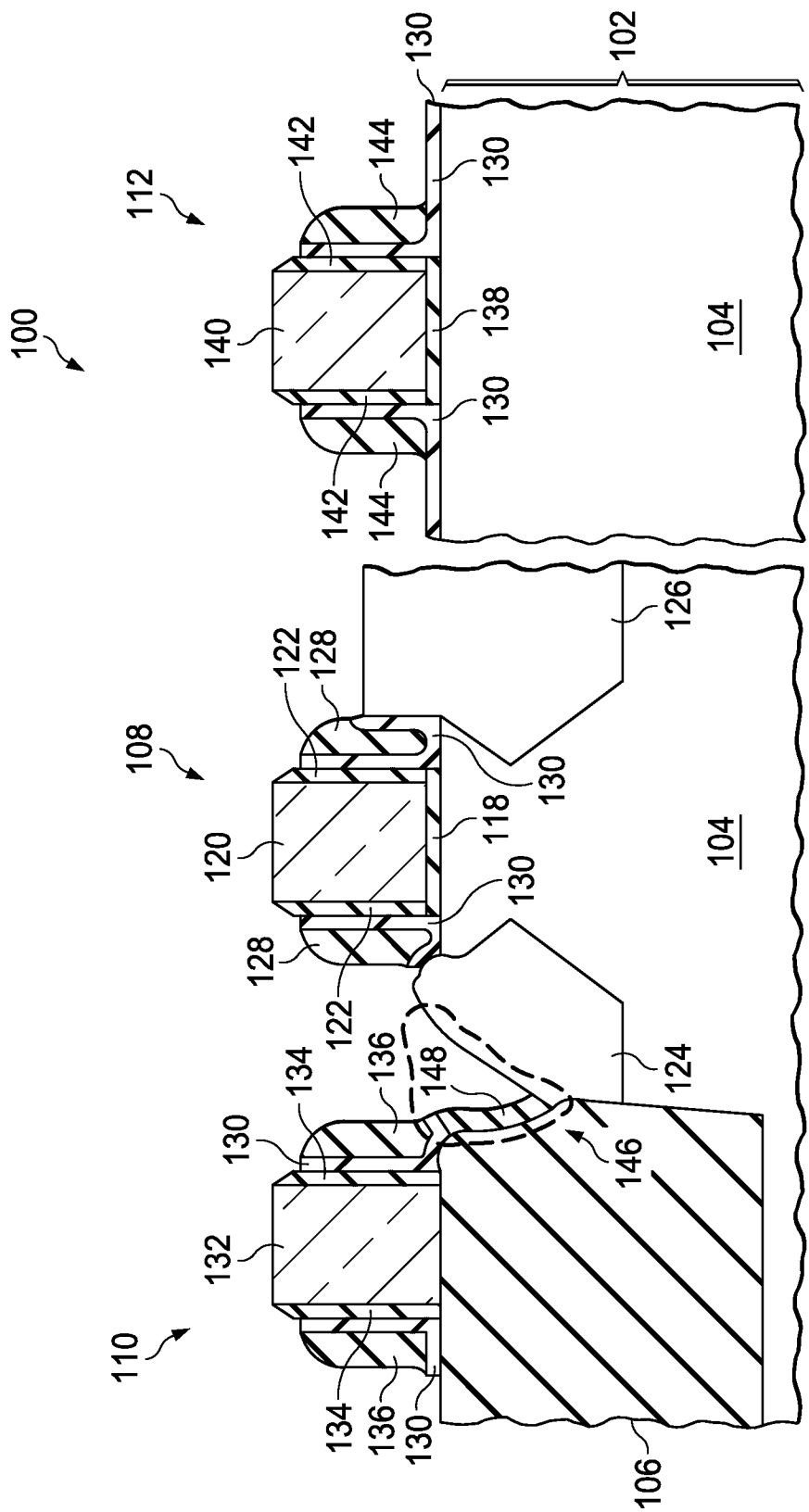


FIG. 2G

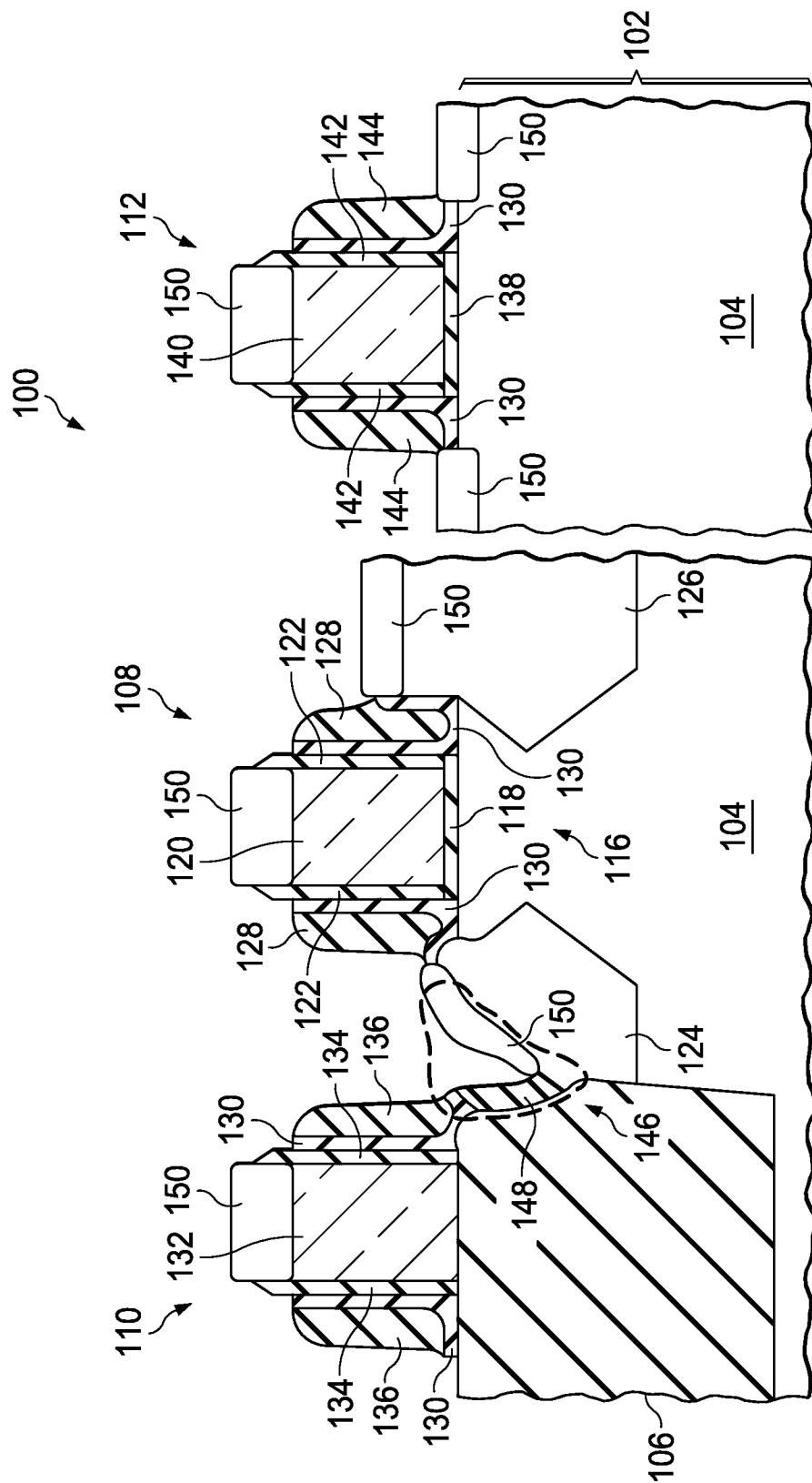


FIG. 2H

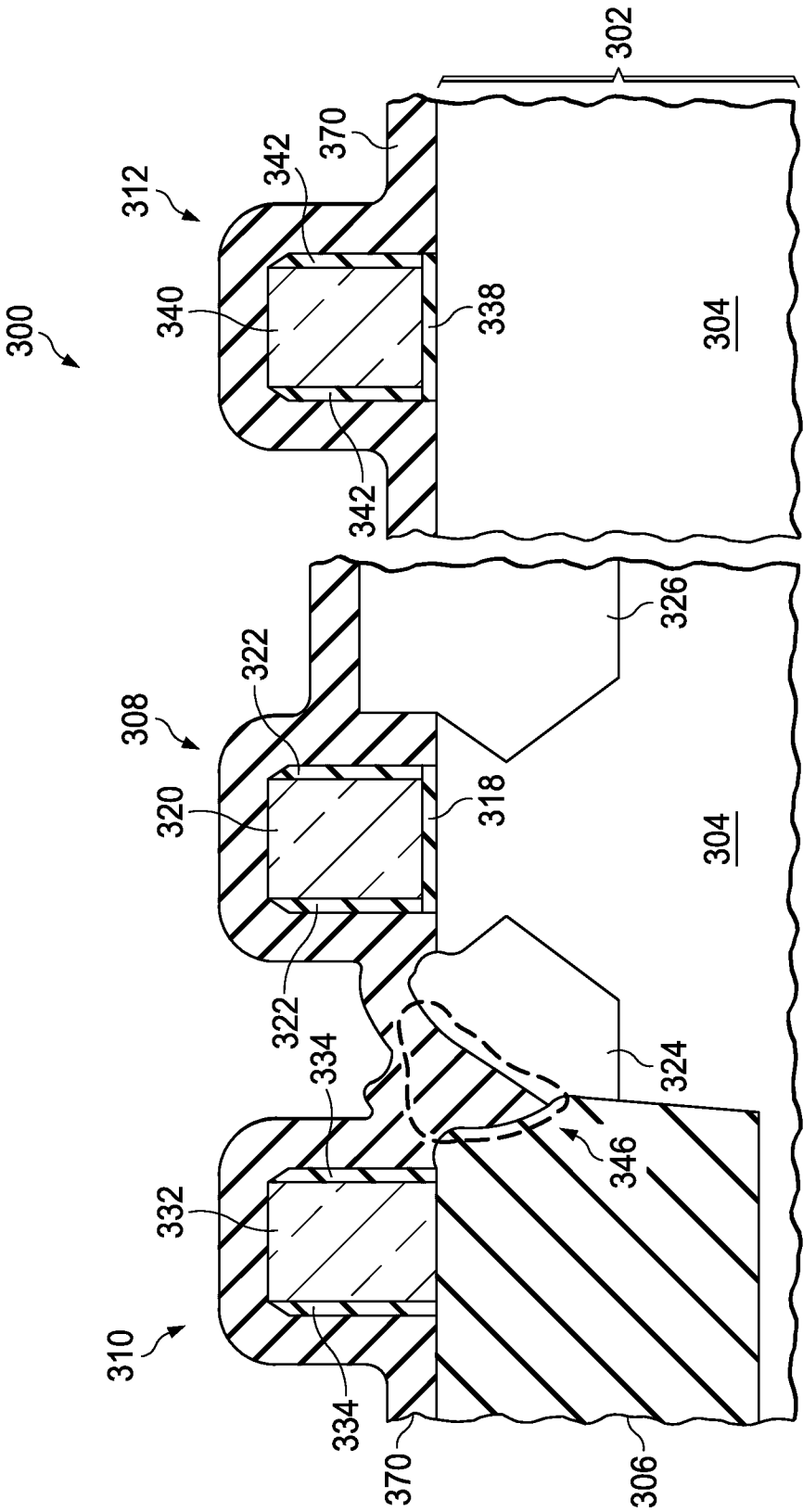


FIG. 3A

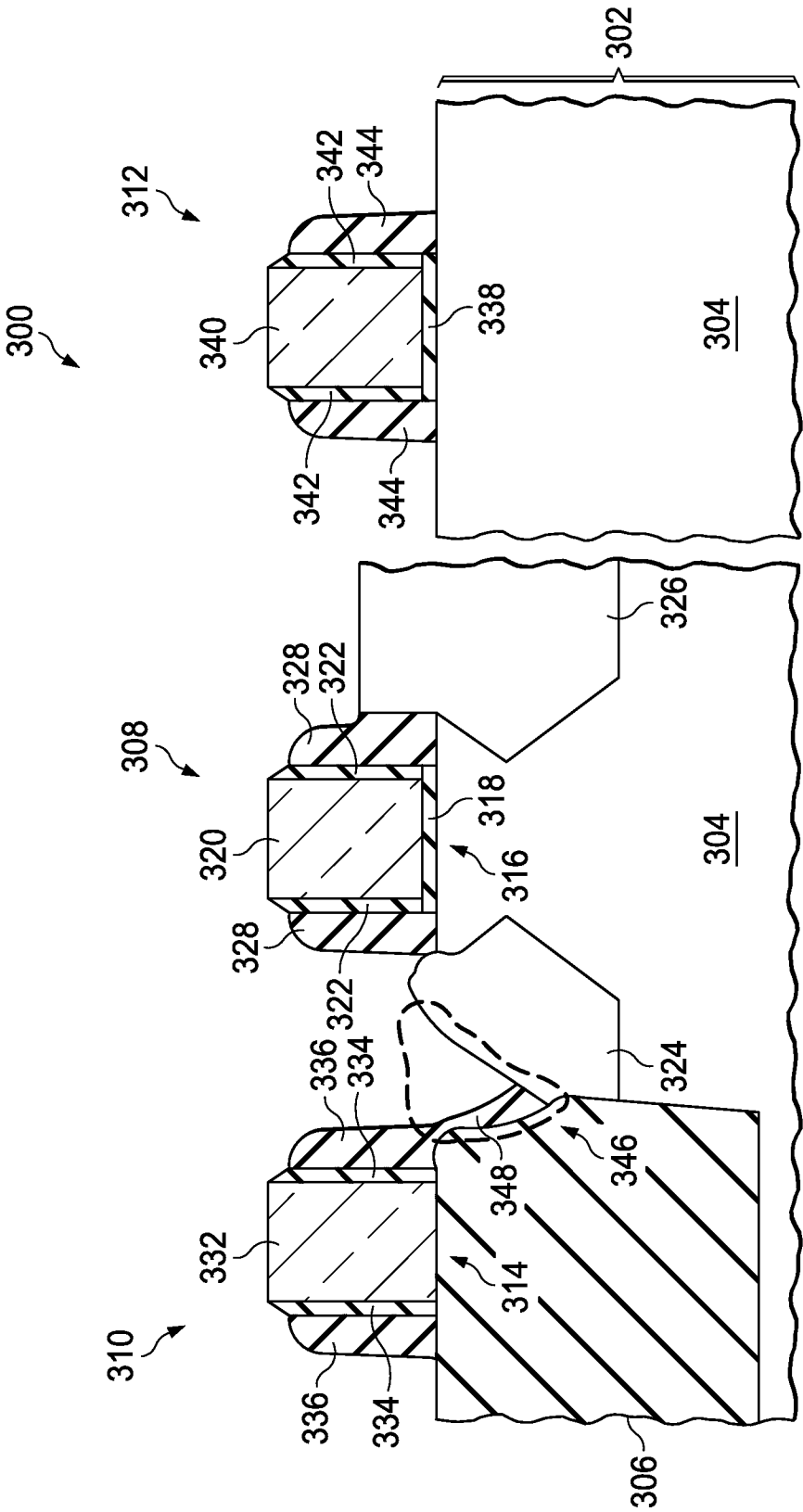


FIG. 3B

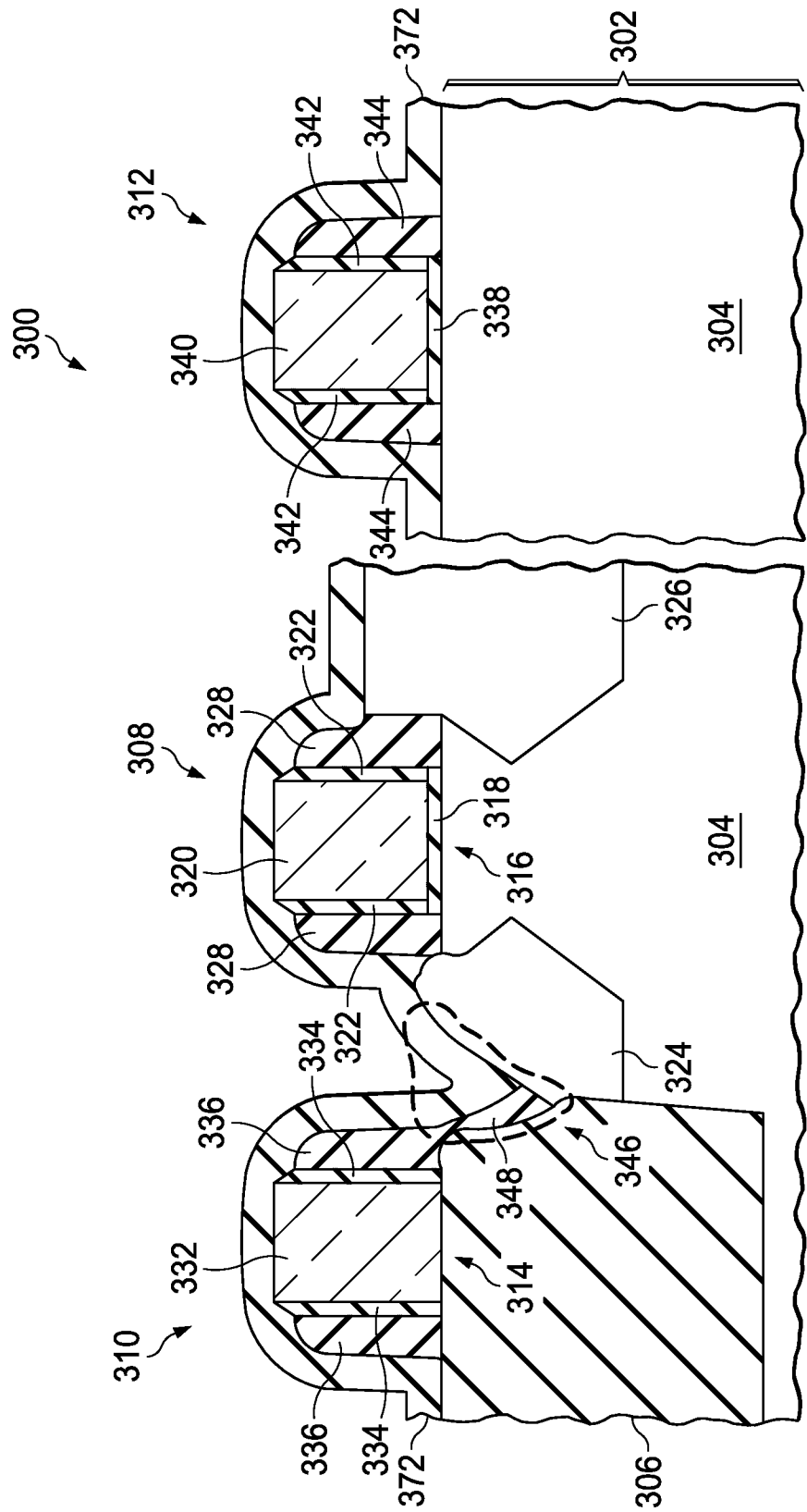


FIG. 3C

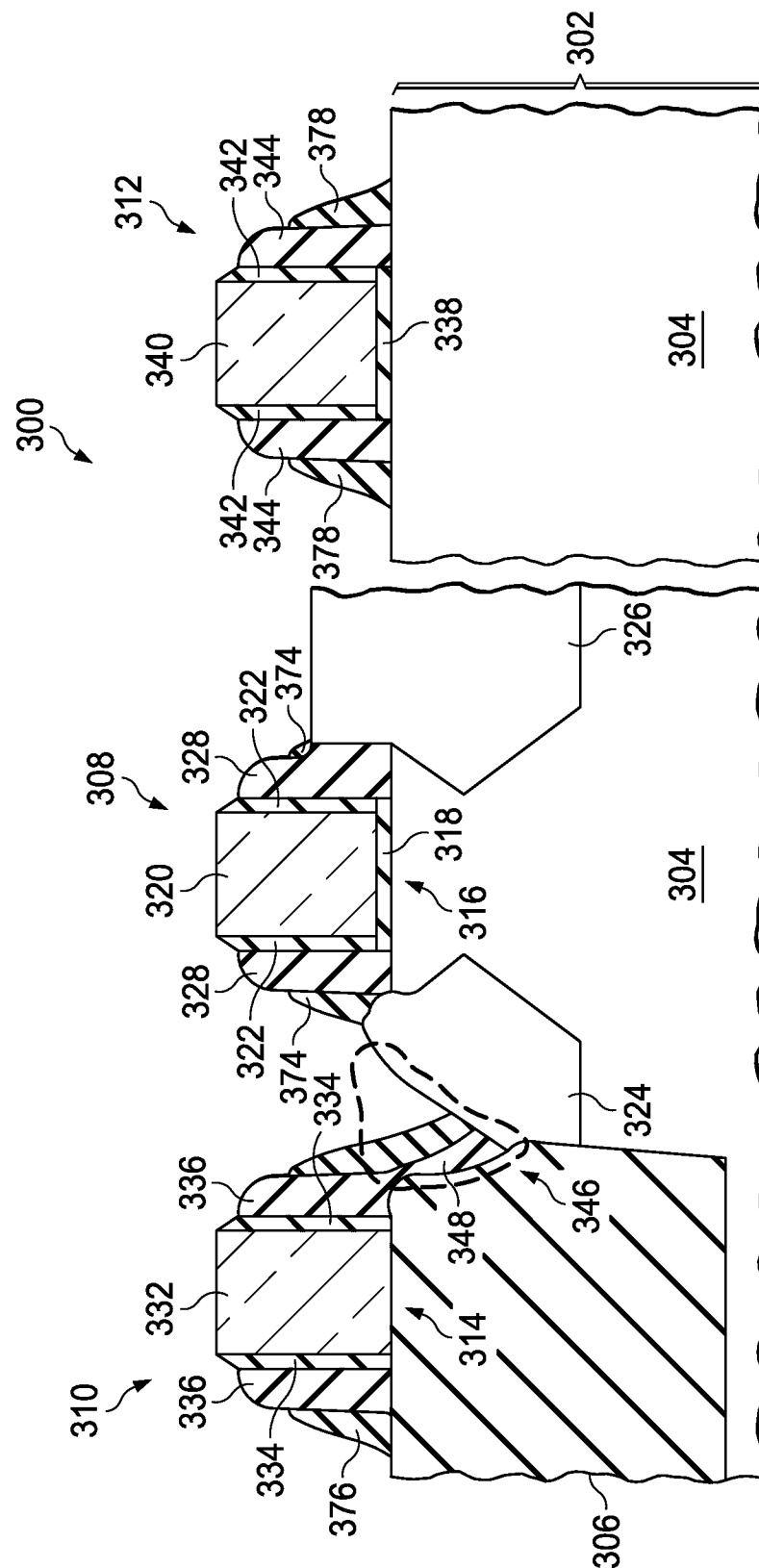


FIG. 3D

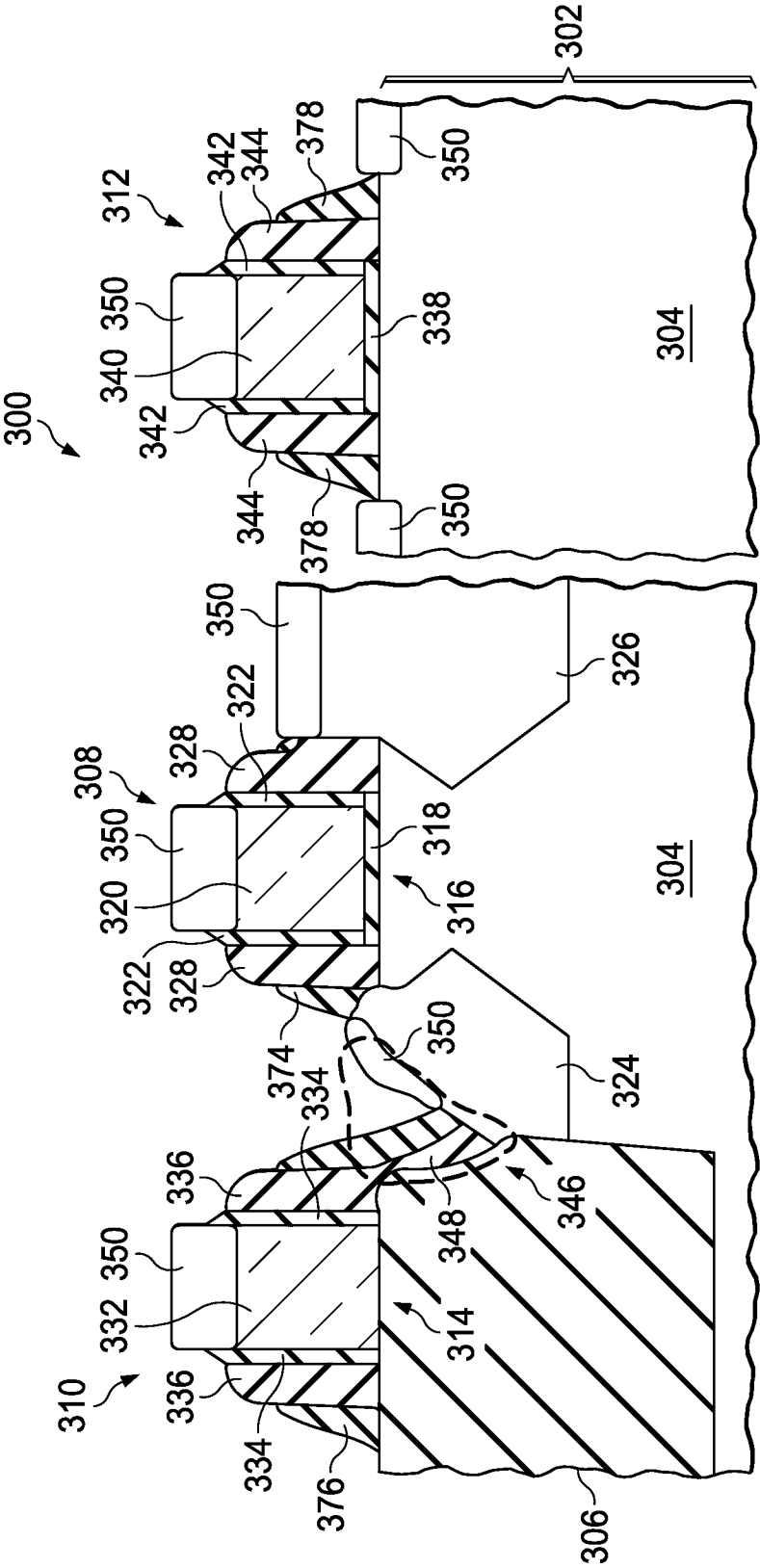


FIG. 3E



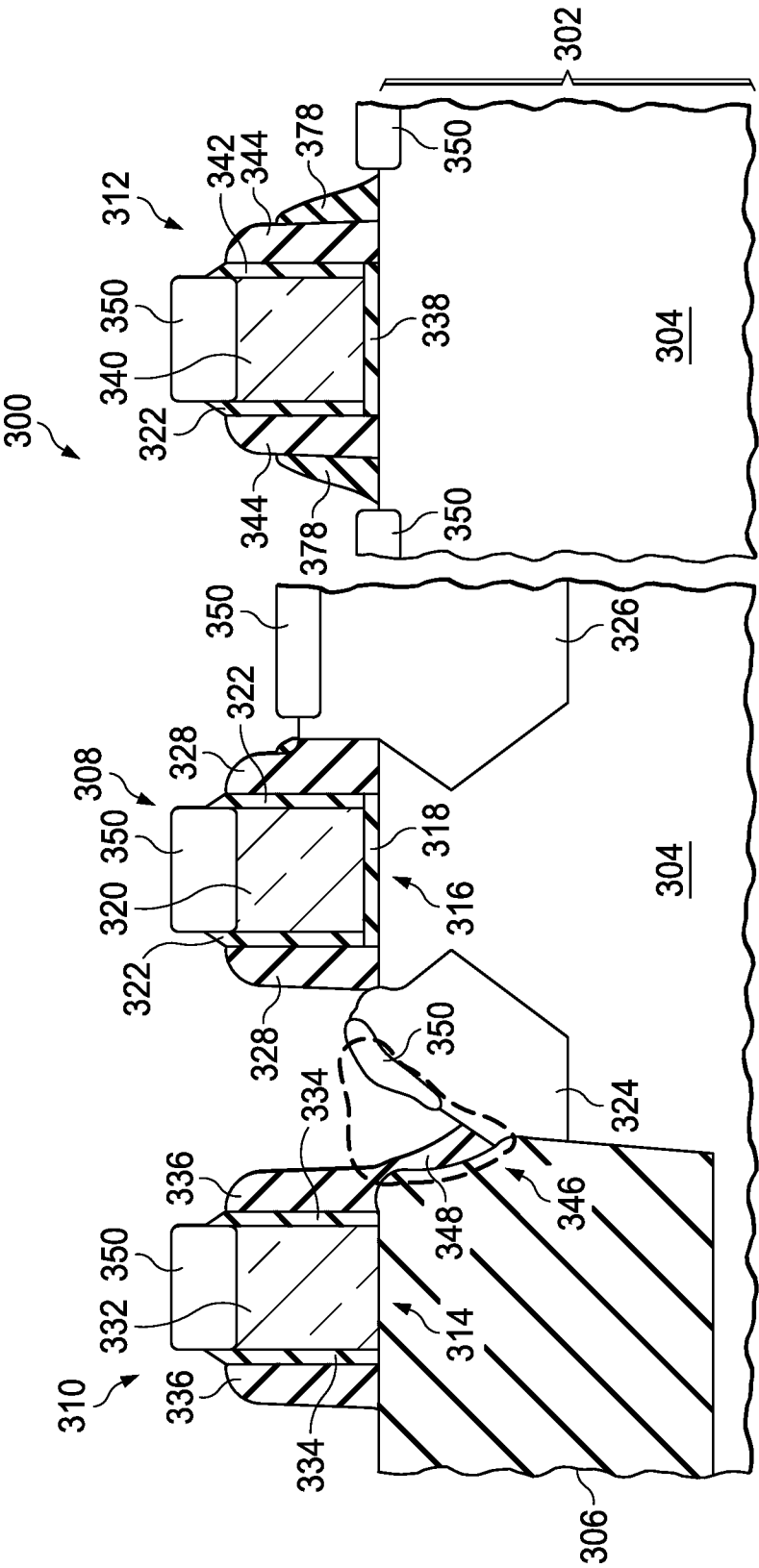
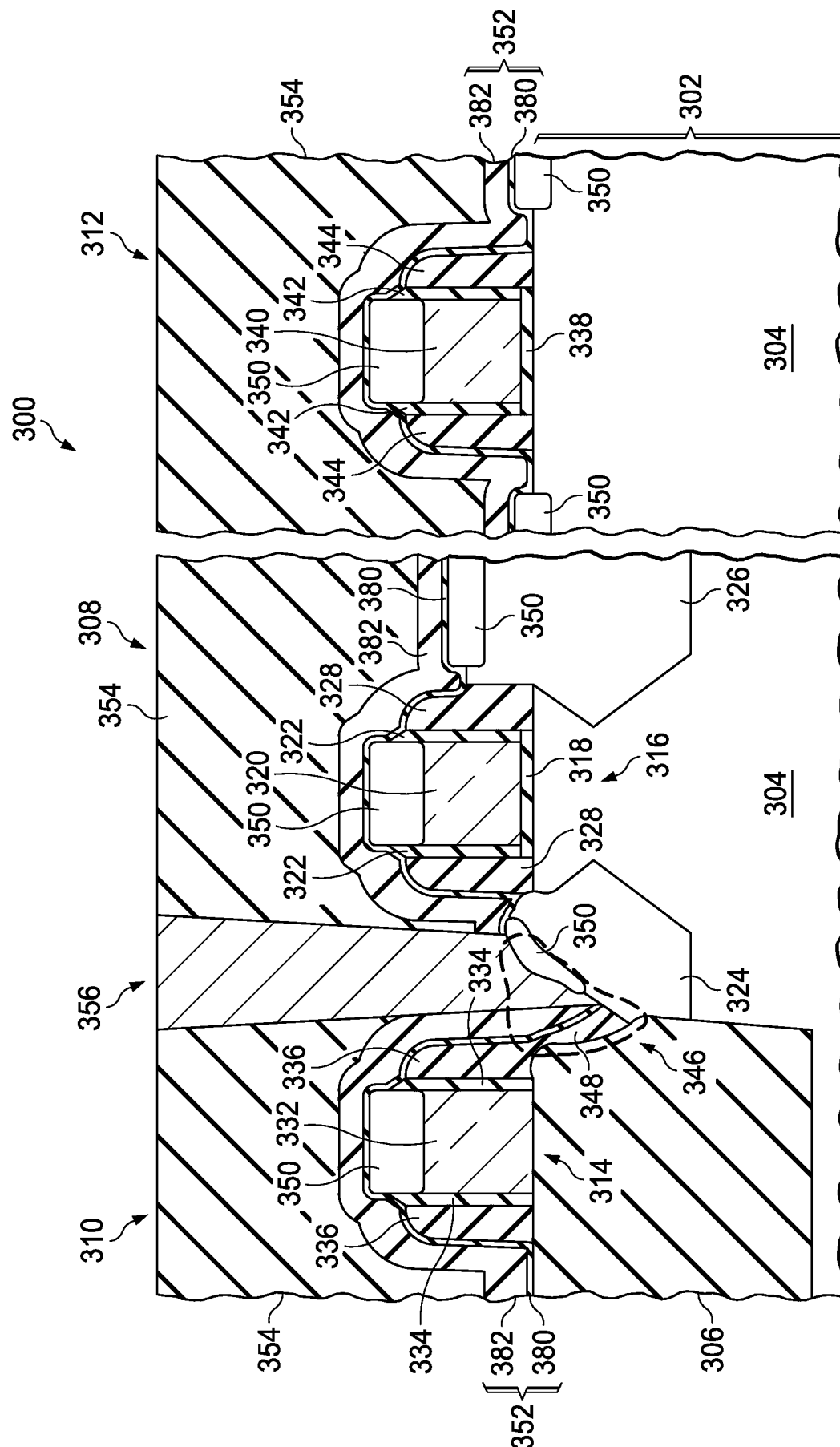


FIG. 3F



**FIG. 3G**

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/070111

## A. CLASSIFICATION OF SUBJECT MATTER

*H01L 27/088 (2006.01)**H01L 21/336 (2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/334-21/338, 27/08-27/095

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7342273 B2 (MICRON TECHNOLOGY, INC.) 11.03.2008	1-19
A	US 6358801 B1 (MICRON TECHNOLOGY, INC.) 19.03.2002	1-19
A	US 5571733 A (MICRON TECHNOLOGY, INC.) 05.11.1996	1-19

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Further documents are listed in the continuation of Box C.

☐

See patent family annex.

\* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier document but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&amp;” document member of the same patent family

Date of the actual completion of the international search

18 March 2015 (18.03.2015)

Date of mailing of the international search report

02 April 2015 (02.04.2015)

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