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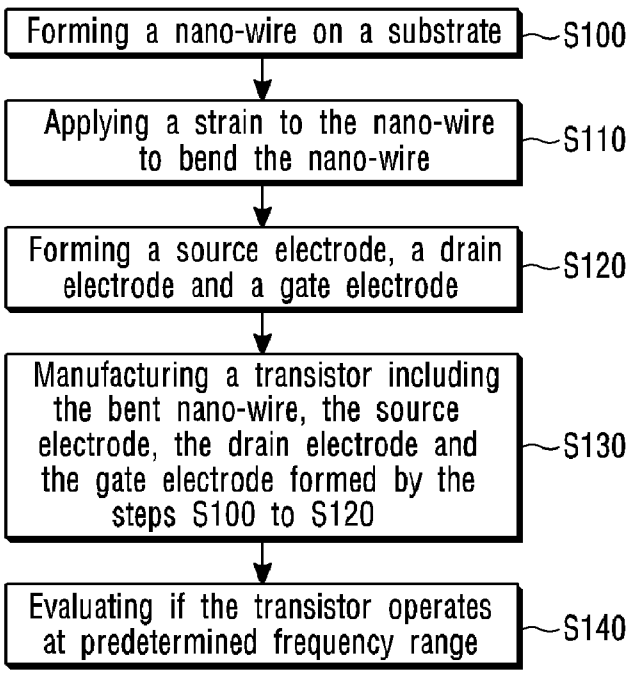
[Continued on next page]

(54) Title: METHOD FOR ENHANCING PERFORMANCE OF PLASMA-WAVE TRANSISTOR



(57) Abstract: The method for enhancing the performance of a transistor may be provided that includes forming a nano-wire on a substrate, applying strain to the nano-wire to bend the nano-wire, forming a source electrode, a drain electrode and a gate electrode, and manufacturing a transistor including the bent nano-wire formed by the applying of the strain, and source electrode, drain electrode and gate electrode formed by the forming of the electrodes. Through the above configuration, a silicon device that operates in a terahertz band can be more easily manufactured, and it is possible to evaluate whether or not the silicon device operates as a plasma-wave transistor.

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Description

Title of Invention: METHOD FOR ENHANCING PERFORMANCE OF PLASMA-WAVE TRANSISTOR

Technical Field

[1] The present invention relates to a method for enhancing the performance of a plasma-wave transistor (PWT) for the applications of the plasma-wave transistor, and more particularly, to a method for evaluating the performance of a plasma-wave transistor, which amplifies plasma-wave emission through the increase of the electron mobility of a nano-wire, thereby determining whether or not the plasma-wave transistor operates in a terahertz (THz) band.

Background Art

[2] A terahertz frequency range refers to a frequency ranging from 10^{11}Hz to 10^{13}Hz (from 0.1THz to 10THz). A terahertz wave is an electromagnetic wave resource corresponding to a frequency band between a millimeter wave obtained by using a conventional semiconductor transistor and a far-infrared radiation electromagnetic wave obtained by using semiconductor laser. Since a reliable optical or electronic device has not been developed, less research has been devoted to the terahertz band in comparison with an electromagnetic wave in another wavelength band.

[3] Up to the present time, it has been believed that a silicon electron moves with vibration at a frequency of gigahertz and cannot moves with vibration at a frequency higher than gigahertz. Due to such a limitation of a silicon semiconductor, current electronic products can use only a frequency up to the gigahertz range. In order to overcome the limitation of the silicon device, a compound semiconductor is now being developed. However, the compound semiconductor requires a very high cost and is not able to use the existing cutting-edge silicon manufacturing process.

Disclosure of Invention

Technical Problem

[4] Embodiments are intended to overcome the above disadvantages and other disadvantages not described above. The present inventive concept provides a method for enhancing the performance of a plasma-wave transistor, which applies the existing silicon manufacturing process at it is and more easily manufactures a silicon device operating in a terahertz band, so that it is possible to evaluate whether or not the silicon device operates as the plasma-wave transistor.

Solution to Problem

[5] One embodiment is a method for enhancing the performance of a transistor comprising: forming a nano-wire on a substrate, applying strain to the nano-wire to

bend the nano-wire, forming a source electrode, a drain electrode and a gate electrode, manufacturing a transistor including the bent nano-wire formed by the applying of the strain, and source electrode, drain electrode and gate electrode formed by the forming of the electrodes.

[6] The method may further include evaluating whether or not the transistor operates in a predetermined band.

[7] The forming the electrodes may form a grating gate having two gate electrodes.

[8] The applying the strain may bend the nano-wire by forming a natural oxide layer.

[9] The transistor may be a plasma-wave transistor.

[10] The predetermined band may range from 10^{11}Hz to 10^{13}Hz (from 0.1THz to 10THz.)

[11] The nano-wire may be made of at least any one selected from the group consisting of Si, Ge, Sn, Se, Te, B, C, B-Si, Si-C, Si-Ge, Si-Sn, Ge-Sn, SiC, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SeTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, $(Cu,Ag)(Al,Ga,In,Tl,Fe)(S,Se,Te)_2$, Si_3N_4, Ge_3N_4, Al_2O_3, $(Al,Ga,In)_2$, $(S,Se,Te)_3$ and Al_2CO.

[12] The length of the gate electrode may be greater than 20 nm.

Advantageous Effects of Invention

[13] Through a method for enhancing the performance of a plasma-wave transistor according to various embodiments of the present invention, a silicon device may be more easily manufactured which operates in a terahertz band. Also, it is possible to evaluate whether or not the silicon device operates as the plasma-wave transistor.

Brief Description of Drawings

[14] FIG. 1 illustrates a view for comparing a field effect transistor (FET) with a plasma-wave transistor (PWT).

[15] FIG. 2 illustrates a flowchart showing a method for enhancing the performance of the transistor in accordance with an embodiment of the present invention.

[16] FIG. 3 illustrates a configuration of the transistor manufactured by the method according to the embodiment of the present invention.

[17] FIG. 4 illustrates an enlarged view of a nano-wire which is an element of the transistor manufactured by the method according to the embodiment of the present invention.

[18] FIG. 5 illustrates a graph of electron mobility variation according to a temperature.

[19] FIG. 6 illustrates a graph for evaluating the performance of the plasma-wave transistor.

Best Mode for Carrying out the Invention

[20] Hereafter, embodiments of the present invention will be described in greater detail with reference to the accompanying drawings.

[21] FIG. 1 is a view for comparing a field effect transistor (FET) with a plasma-wave transistor (PWT).

[22] The field-effect transistor (FET) controls current by using an electric field, and, as shown in (a) of FIG. 1, includes three electrodes; a source electrode, a drain electrode and a gate electrode.

[23] Briefly describing the operation principle of the field-effect transistor, a channel is formed on a doped silicon substrate by applying a voltage higher than a threshold voltage to a gate electrode, and electrons or holes are allowed to flow through the formed channel by using the voltage difference between the source electrode and the drain electrode.

[24] In general, according to the theory of the field-effect transistor, it is described that channel electrons move individually with being scattered by lattices or ions while they are moving from the source electrode to the drain electrode.

[25] However, when the density of the channel electrons exceeds a certain level, the electrons move, as shown in (b) of FIG. 1, in a collective way. That is, a collective spatio-temporal variation of the electron density occurs in a certain boundary condition. It is called a plasma-wave which has a velocity 10 to 100 times faster than the local electron drift velocity. The local electron drift velocity refers to an average velocity of the local electron while passing through the channel.

[26] The plasma-wave transistor using the principle above has a velocity about 10 to 100 times faster than the velocity of the conventional field-effect transistor. Therefore, a frequency band for the transistor may be extended to a terahertz band.

[27] An existing technique for enhancing the velocity of a silicon device and an existing technology for enhancing the performance of an ultra high frequency depend on how fast the electron that forms the channel moves.

[28] The terahertz band having a lot of advantages, such as the coexistence of straightness of a light wave (light) and transmittance of an electric wave, harmlessness to a human body due to the low energy, etc., can be variously applied to an ultra-high speed/ high-capacity communication in an ultra high frequency band, etc., on the basis of an imaging technique, a spectroscopic technique, or the like.

[29] The electron mobility of the silicon device is about 250cm^2/Vs at a room temperature (approximately 25℃ or 298.15K). To achieve terahertz emission by using such a degree of the electron mobility, the length of the gate electrode should be extremely shortened.

[30] The electron mobility is a measure of how easily electrons drift. Through the electron mobility, it can be understood how much the local electron drift velocity is increased in proportion to an electric field.

[31] The method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention achieves the terahertz emission even though the length of the gate electrode is relatively large, thereby making it easier to evaluate whether the transistor operates in the terahertz band.

[32] In order to achieve the terahertz emission with the electron mobility of a common silicon device, the length of the gate electrode should be as short as about 5 nm. However, with the current silicon integration technology, it is difficult to perform the patterning to form the gate electrode with a length of about 5 nm. In addition, it is not easy to prevent a short channel effect.

[33] Specifically, the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention increases the electron mobility by applying strain to a nano-wire and bending it. That is, it is possible to bend the nano-wire by applying a physical or chemical force to the nano-wire, resulting in the increase of the electron mobility as described below.

[34] One embodiment to bend the nano-wire is to grow a natural oxide layer on the nano-wire. When the natural oxide layer is grown on the nano-wire, the electron mobility is increased to about 1000㎠/Vs at a room temperature due to the applied strain. When the electron mobility is increased by employing the above principle, the terahertz emission can be achieved even though the length of the gate electrode is greater than 20nm.

[35] In other words, the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention increases the electron mobility by using the strain at the time of fabricating the natural oxide layer on the nano-wire and manufactures the transistor that includes the gate electrode with an enough length to be patterned by the current patterning technology, so that the evaluation of the performance of the plasma-wave transistor can be easily made.

[36] FIG. 2 illustrates a flowchart showing the method for enhancing the performance of the transistor in accordance with the embodiment of the present invention. First, the nano-wire is formed on a substrate (S100). Next, the nano-wire is bent by applying the strain to the nano-wire(S110). An oxide layer process may be representatively taken as an example of the method for applying the strain to the nano-wire. However, the nano-wire may be bent by another method.

[37] Next, the source electrode and the drain electrode are formed at both ends of the nano-wire before the gate electrode is formed (S120). Subsequently, a transistor having the bent nano-wire channel is manufactured by adding a general transistor manu-

facturing process with the inclusion of S100 to S120 (S130). In other words, the transistor is manufactured which includes the nano-wire, the source electrode, the drain electrode and the gate electrode which have been formed through the steps of S100 to S120.

[38] Lastly, it is to evaluate whether or not the transistor manufactured in the step S130 operates in a predetermined band (S140). The evaluation the step S140 will be described in more detail with reference to FIG. 6.

[39] It is enough as long as the manufacturing step S130 in the method for enhancing the performance of the transistor according to the embodiment of the present invention includes the steps from S100 to S120. The steps from S100 to S120 are not necessarily performed in sequence. That is, the order of S100 to S120 may be changed, or an extra common transistor manufacturing process may be added between each of the steps.

[40] In the meantime, while FIG. 2 includes the step S140 of evaluating the transistor, it will be apparent to those skilled in the art that the performance of the transistor can be enhanced only by up to the step S130.

[41] FIG. 3 illustrates a configuration of the transistor manufactured by the method according to the embodiment of the present invention. FIG. 4 illustrates an enlarged view of the nano-wire which is an element of the transistor manufactured by the method according to the embodiment of the present invention.

[42] As illustrated in FIG. 3, the transistor manufactured by the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention includes a substrate 10, a drain electrode 20, a source electrode 30, a nano-wire 40 and a gate electrode 50. Herein, the gate electrode 50 is illustrated as a grating gate electrode having a first gate electrode 52 and a second gate electrode 54.

[43] As described above with reference to FIG. 2, the transistor that is used in the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention has the nano-wire channel bent by the steps; forming the nano-wire 40 on the substrate 10 and applying the strain to the nano-wire 40. Subsequently, each of the electrodes 20, 30 and 50 is formed.

[44] Particularly, the gate electrode 50, as shown in FIG. 3, may be the grating gate electrode including the two gate electrodes 52 and 54. By adopting a structure in which the grating gate electrode 50 surrounds the nano-wire 40, the field-effect transistor can be more integrated. However, the gate electrode 50 is not necessarily implemented by the grating gate electrode.

[45] The measurement of the plasma wave emission by using the gate electrode employs a principle in which, when the plasma wave excited in the channel is transmitted as a mirror image wave to the gate electrode and dipoles are generated, an electromagnetic wave is radiated in the air in the form of free radiation, and then the electric power of

the radiated electromagnetic wave is measured.

[46] In particular, since the electromagnetic wave radiated from the gate electrode is added and amplified by using the grating gate electrode having the two electrodes , the plasma-wave emission can be measured more easily. In this embodiment, the gate electrode 50 has the two electrodes 52 and 54. However, it can be considered that the gate electrode 50 includes more than two electrodes.

[47] The grating gate electrode 50 is formed to surround the bent nano-wire 40. The first gate electrode 52 and second gate electrode 54 constituting the grating gate electrode 50 include a longitudinal base and a plurality of protrusions which protrude perpendicularly to the base. The protrusion of the first gate electrode 52 and the protrusion of the second gate electrode 54 are spaced from each other at a predetermined distance so as not to contact each other and are inserted opposite to each other. However, the shape of the grating gate electrode 50 illustrated in FIG. 3 is no more than one embodiment, and the grating gate electrode 50 may have a shape different from the shape shown in FIG. 3.

[48] Meanwhile, the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention may further include forming an insulation spacer.

[49] Meanwhile, the nano-wire 40 may be made of any one selected from the group consisting of Si, Ge, Sn, Se, Te, B, C, B-Si, Si-C, Si-Ge, Si-Sn, Ge-Sn, SiC, BN/BP/BAs, AlN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SeTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, $(Cu,Ag)(Al,Ga,In,Tl,Fe)(S,Se,Te)_2$, Si_3N_4, Ge_3N_4, Al_2O_3, $(Al,Ga,In)_2$, $(S,Se,Te)_3$ and Al_2CO.

[50] FIG. 5 illustrates a graph of electron mobility variation according to a temperature.

[51] The electron mobility of the silicon device is about 250㎠/Vs at a room temperature (approximately 25℃ or 298.15K.) As described above, to achieve the terahertz emission by using the electron mobility of about 250㎠/Vs, the length of the gate electrode should be as short as about 5nm. However, there is a technical limitation in patterning for forming of the electrode or preventing the short channel effect, etc.

[52] However, with the increase of the electron mobility of the silicon device, the length of the gate electrode can be relatively longer, so that it becomes easier to manufacture the gate electrode.

[53] In case of manufacturing the silicon device with the nano-wire bent by applying the strain, the silicon device has a high electron mobility represented by two lines (a line (d) and a line (f)) in the top part of FIG. 5. Herein, "L" means the length of the nano-

wire, and "W" means the diameter of the nano-wire. As shown in FIG. 5, it can be found that the mobility is increased to about 1000㎠/Vs at a room temperature by using the bent nano-wire channel.

[54] Also, referring to FIG. 5, it can be seen that the effect of applying the strain is increased with the decrease of the diameter of the nano-wire.

[55] The transistor manufactured by the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention includes the bent nano-wire channel, so that the transistor has a higher electron mobility at a room temperature.

[56] Further, since the nano-wire channel of the transistor manufactured by the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention has a higher electron mobility, the length of the gate electrode can be implemented within a technical scope of the current technology.

[57] FIG. 6 illustrates a graph for evaluating the performance of the plasma-wave transistor.

[58] In the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention, as shown in FIG. 6, the local electron drift velocity is plotted on the x-axis, the plasma wave velocity is plotted on the y-axis and the channel length is plotted on the z-axis.

[59] In addition, the method for enhancing the performance of the plasma-wave transistor according to the embodiment of the present invention generates a design window including a relational expression between the x-axis, y-axis and z-axis, and measures whether or not the manufactured transistor operates as a terahertz emitter in accordance with the change of a performance parameter value of the manufactured transistor.

[60] Herein, it is desirable that the design window 3-dimensionally represents the change of emission boundary according to the channel mobility and channel length at the same time, and thus, decides the range of the channel length ensuring a function as a terahertz emitter, the range of the plasma wave velocity and the range of the electron drift velocity.

[61] Specifically, the emission boundary of the design window changes according to the channel mobility and channel length, and the design window may be generated by the performance parameter corresponding to the point of the emission boundary acquired by a user's input. That is, prior to the real plasma-wave transistor process and experiment, a parameter suitable for the channel mobility or channel length, which should be confirmed experimentally and obtained later, is assumed, and then the calculated momentum relaxation time and the calculated injection velocity are input to the relational expression between the x-axis, y-axis and z-axis, so that the design window can be generated.

[62] Subsequently, according to the embodiment of the present invention, the performance of the plasma-wave transistor that operates as a terahertz emitter can be evaluated by checking the plasma-wave velocity and the electron drift velocity in the design window.

[63] Also, the movement of the plasma-wave is divided into upstream and downstream movements. The design window may be designed to include a physical condition satisfying the mathematical formula "(plasma-wave velocity - electron drift velocity) x momentum relaxation time > channel length" which uses a property that the emission of the terahertz emitter is caused by the multiple reflection.

[64] According to the embodiment of the present invention, the electron mobility can be increased to 1000㎠/Vs by using the nano-wire bent by the strain. As a result, the length of the gate electrode can be increased to the range that enables the terahertz emission, so that it becomes easier to evaluate whether or not the terahertz emission occurs.

[65] To avoid making the subject matter of the present invention unclear, the specific method and process of evaluating the performance of the transistor have been described in a brief summary. It will be apparent to those skilled in the art that the evaluation of the performance of the plasma-wave transistor can be made by using the performance evaluating method disclosed by other various types (published patent document, thesis, etc).

[66] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. It can be understood by those skilled in the art that the embodiments may be changed and modified in various ways without departing from the essential features of the embodiments. Also, the scope of the right specified by the matters described in the claims of the present specification includes all the various modifications and applications.

[67]

[68]

Claims

[Claim 1] A method for enhancing the performance of a transistor, the method comprising:
forming a nano-wire on a substrate;
applying strain to the nano-wire to bend the nano-wire;
forming a source electrode, a drain electrode and a gate electrode; and
manufacturing a transistor including the bent nano-wire formed by the applying of the strain, and source electrode, drain electrode and gate electrode formed by the forming of the electrodes.

[Claim 2] The method of claim 1, further comprising evaluating whether or not the transistor operates in a predetermined band.

[Claim 3] The method of claim 1, wherein the forming the electrodes forms a grating gate electrode having two gate electrodes.

[Claim 4] The method of claim 1, wherein the applying the strain on the nano-wire bends the nano-wire by forming a natural oxide layer.

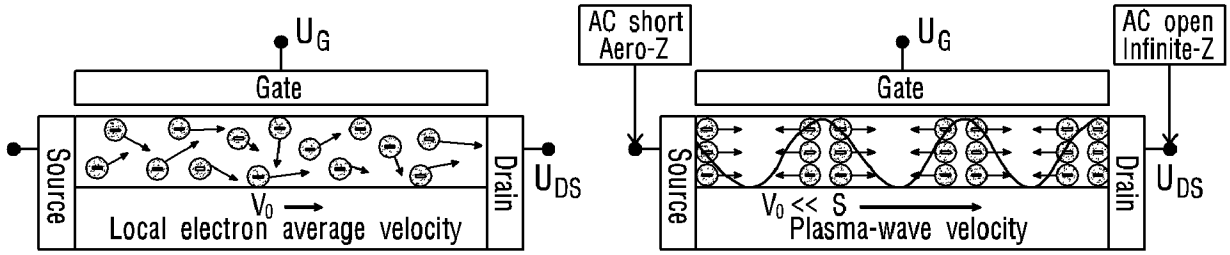
[Claim 5] The method of claim 1, wherein the transistor is a plasma-wave transistor.

[Claim 6] The method of claim 2, wherein the predetermined band ranges from 10^{11}Hz to 10^{13}Hz (from 0.1THz to 10THz.)

[Claim 7] The method of claim 1, wherein the nano-wire is made of at least any one selected from the group consisting of Si, Ge, Sn, Se, Te, B, C, B-Si, Si-C, Si-Ge, Si-Sn, Ge-Sn, SiC, BN/BP/BAs, AIN/AlP/AlAs/AlSb, GaN/GaP/GaAs/GaSb, InN/InP/InAs/InSb, ZnO/ZnS/ZnSe/ZnTe, CdS/CdSe/CdTe, HgS/HgSe/HgTe, BeS/BeSe/BeTe/MgS/MgSe, GeS, GeSe, GeTe, SnS, SnSe, SeTe, PbO, PbS, PbSe, PbTe, CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, $(Cu,Ag)(Al,Ga,In,Tl,Fe)(S,Se,Te)_2$, Si_3N_4, Ge_3N_4, Al_2O_3, $(Al,Ga,In)_2$, $(S,Se,Te)_3$ and Al_2CO.

[Claim 8] The method of claim 1, wherein the length of the gate electrode is greater than 20nm.

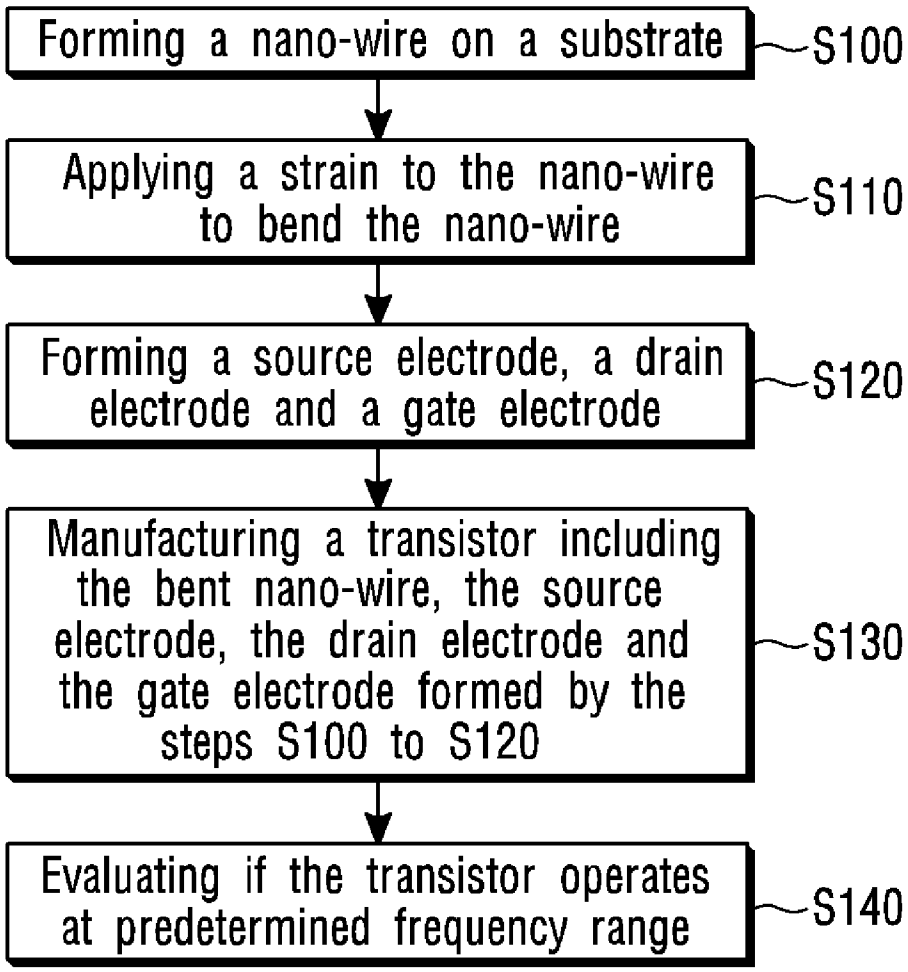
[Fig. 1]



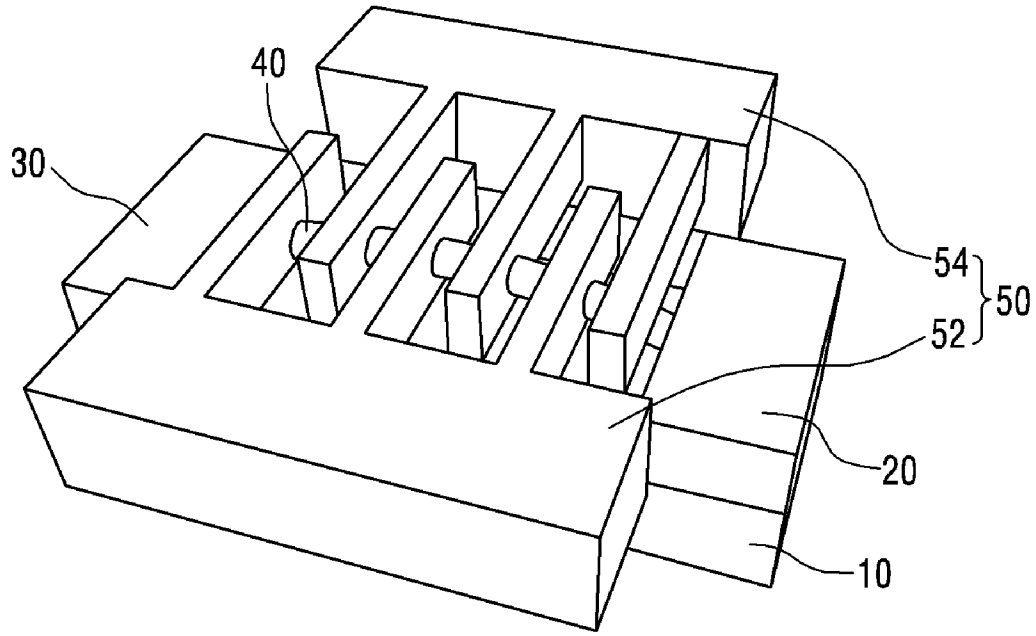
Field-Effect Transistor (FET)
(a)

Plasma-Wave Transistor (PWT)
(b)

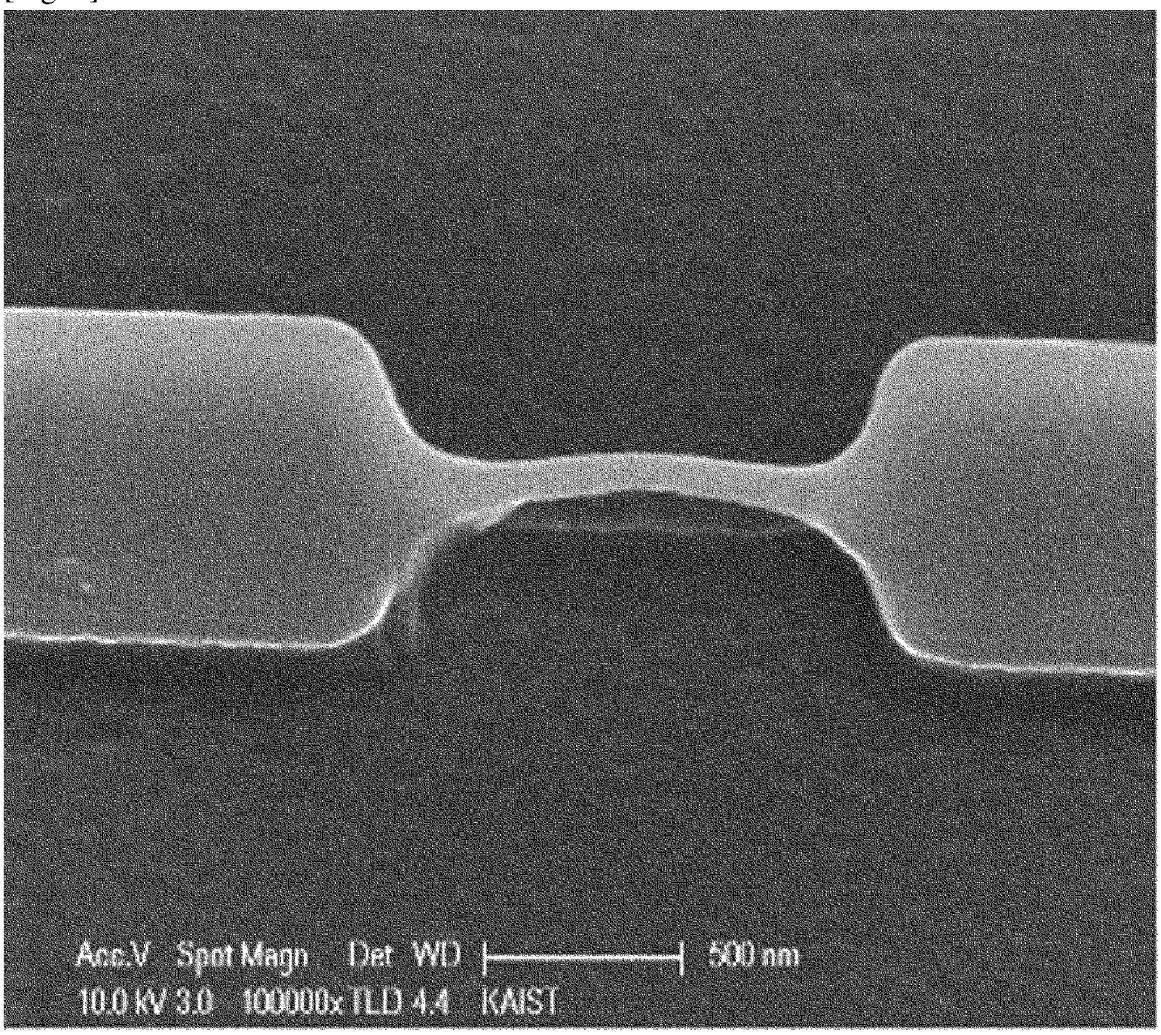
[Fig. 2]



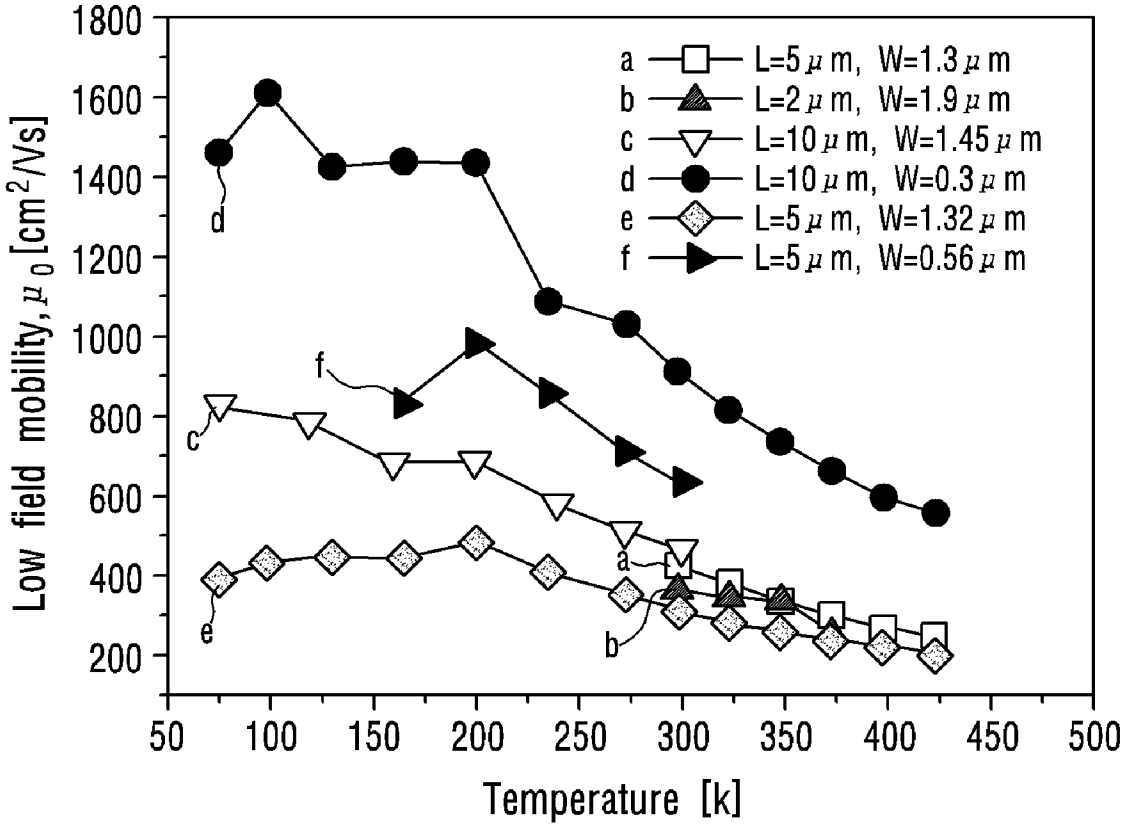
[Fig. 3]


40
30
54
50
52
20
10

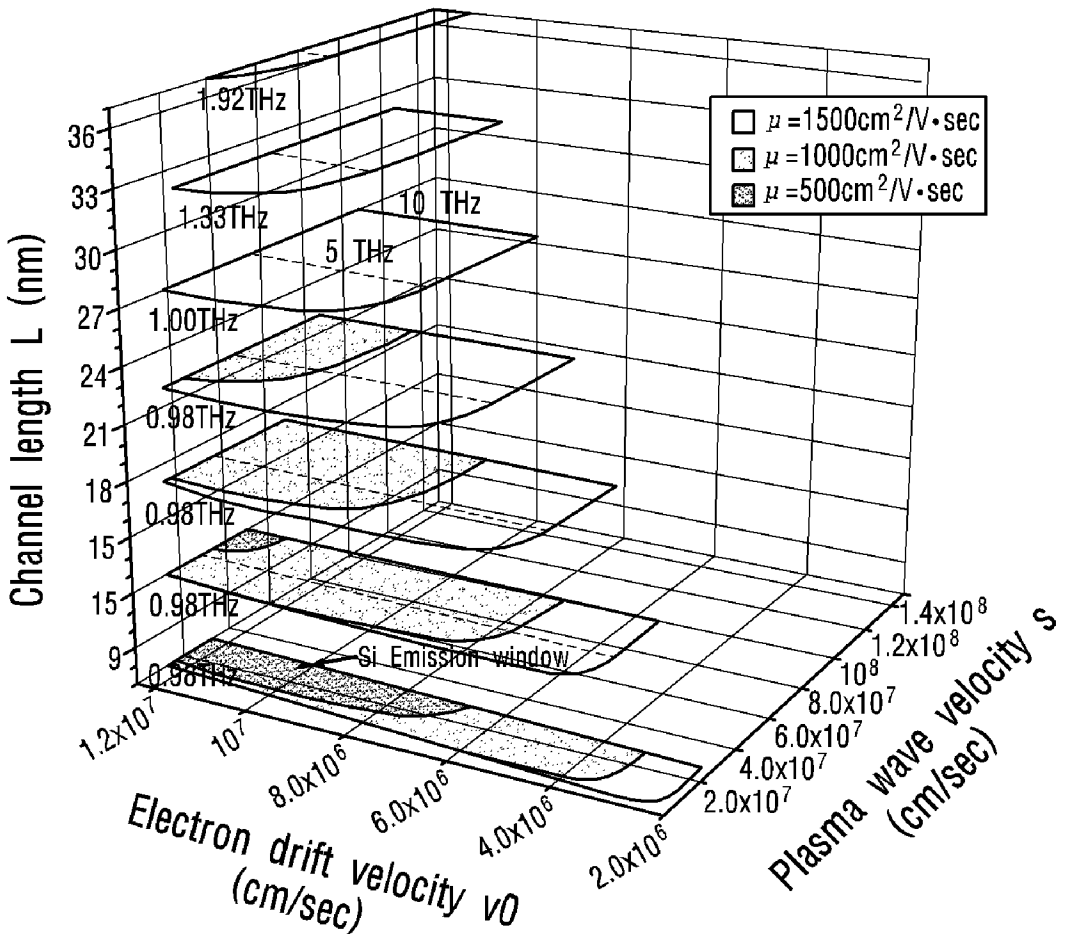
[Fig. 4]


Acc.V Spot Magn Det WD 500 nm
10.0 kV 3.0 100000x TLD 4.4 KAIST

[Fig. 5]


Low field mobility, μ_0 [cm^2/Vs]
Temperature [k]
a L=5μm, W=1.3μm
b L=2μm, W=1.9μm
c L=10μm, W=1.45μm
d L=10μm, W=0.3μm
e L=5μm, W=1.32μm
f L=5μm, W=0.56μm

[Fig. 6]


Channel length L (nm)
Electron drift velocity v0 (cm/sec)
Plasma wave velocity s (cm/sec)
μ=1500cm^2/V·sec
μ=1000cm^2/V·sec
μ=500cm^2/V·sec
1.92THz
1.33THz
1.00THz
0.98THz
0.98THz
0.98THz
0.98THz
10 THz
5 THz
Si Emission window

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2015/001821

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 21/28; H01L 29/78; H01L 29/786; H01L 29/06; H01L 21/335; H01L 29/775

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: transistor, nano-wire, terahertz, strain, plasma-wave

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	K.E. MOSELUND et al. "The High-Mobility Bended n-Channel Silicon Nanowire Transistor", IEEE Transactions on electron devices, Vol. 57, No. 4, pp. 866-876, 17 February 2010, DOI: 10.1109/TED.2010.2040939 See abstract, page 866-873, and figure 1.	1-8
A	CN 102683205 A (SHANGHAI HUALI MICROELECTRONICS CORPORATION) 19 September 2012 See abstract, paragraphs [0025]-[0046], claims 1-5 and figures 1-8.	1-8
A	US 2014-0225184 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 14 August 2014 See paragraph [0024], claim 1 and figure 1M.	1-8
A	JP 2008-258622 A (SHARP CORP.) 23 October 2008 See paragraphs [0004]-[0045], claim 1 and figures 1-3.	1-8
A	JP 2014-131044 A (RENESAS ELECTRONICS CORP.) 10 July 2014 See paragraphs [0014]-[0016], claim 1 and figures 4, 5.	1-8

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 November 2015 (27.11.2015)	**27 November 2015 (27.11.2015)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2015/001821

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN102683205 A	19/09/2012	None	
US 2014-0225184 A1	14/08/2014	KR 10-1423429 B1	24/07/2014
JP 2008-258622 A	23/10/2008	JP 5117906 B2	16/01/2013
		US 2008-0248642 A1	09/10/2008
		US 7935599 B2	03/05/2011
JP 2014-131044 A	10/07/2014	CN 103915484 A	09/07/2014
		US 2014-0183452 A1	03/07/2014