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WO 99/65012 A2 **US 5903246 A**
US 4528480 A

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(54) Abstract Title
Display device using TFT's

(57) A multi-pixel display device, each pixel containing an organic electroluminescent element LEP and substantially rectangular shaped circuit areas, some of which include thin film transistors (TFT's). The circuit areas include two input pair circuit areas 22 abutting each other and two current mirror circuit areas 24 abutting each other. Each of the input pair circuit areas 22 also abuts a current mirror circuit area 24. This arrangement of circuit areas overcomes the problem of the spatial variation of TFT characteristics without the need for compensating circuits. Additionally, this arrangement of circuit areas can reduce to a minimum the p-type and n-type doping areas required in each pixel.

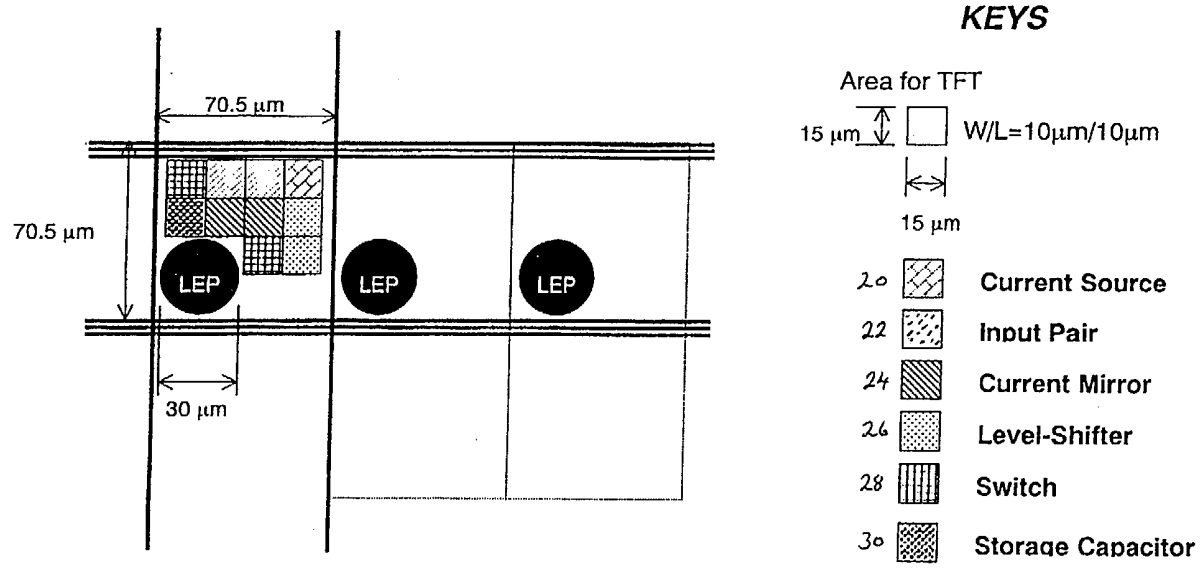


Figure 3

GB 2 367 414 A

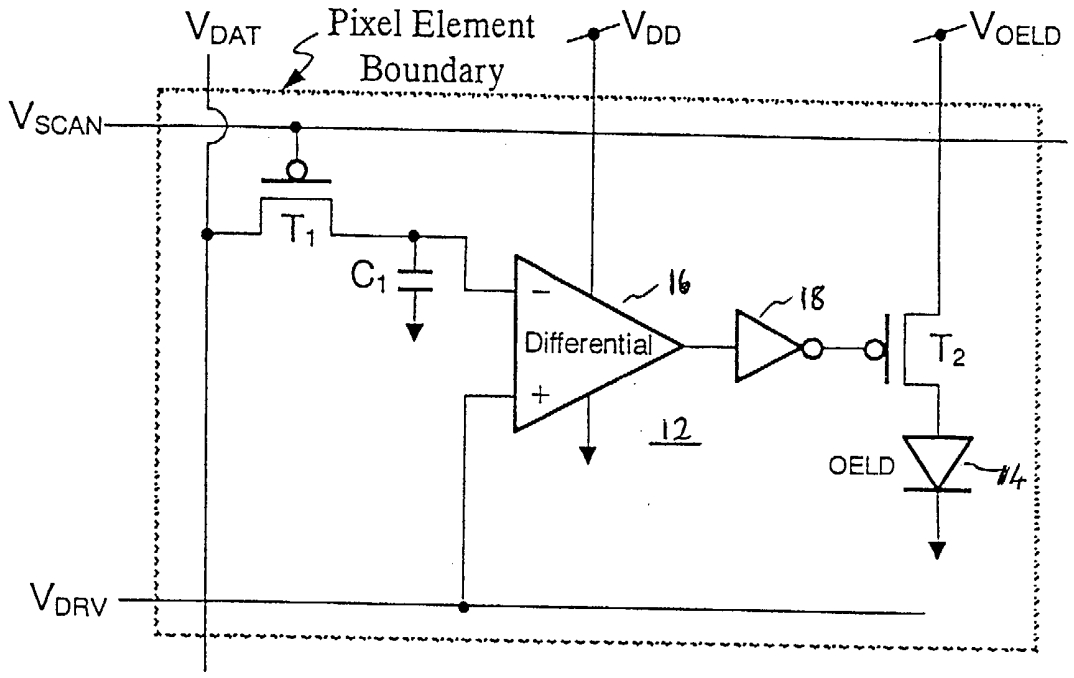


Figure 1

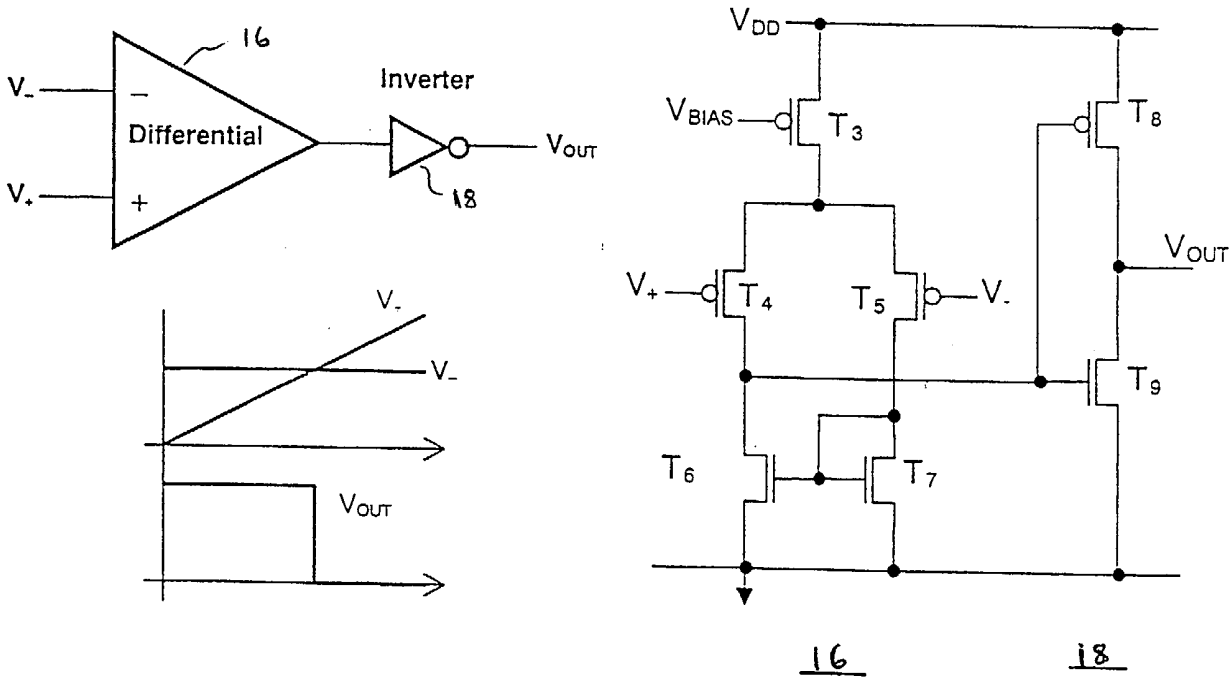
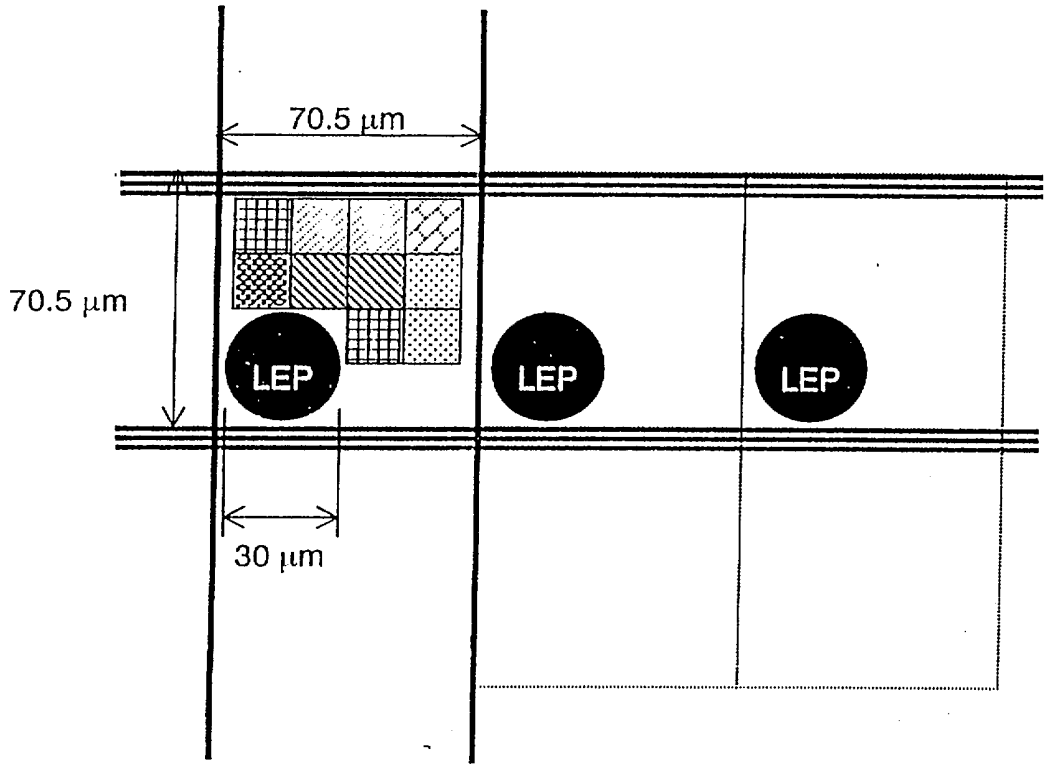


Figure 2


70.5 μm
70.5 μm
LEP
LEP
LEP
30 μm

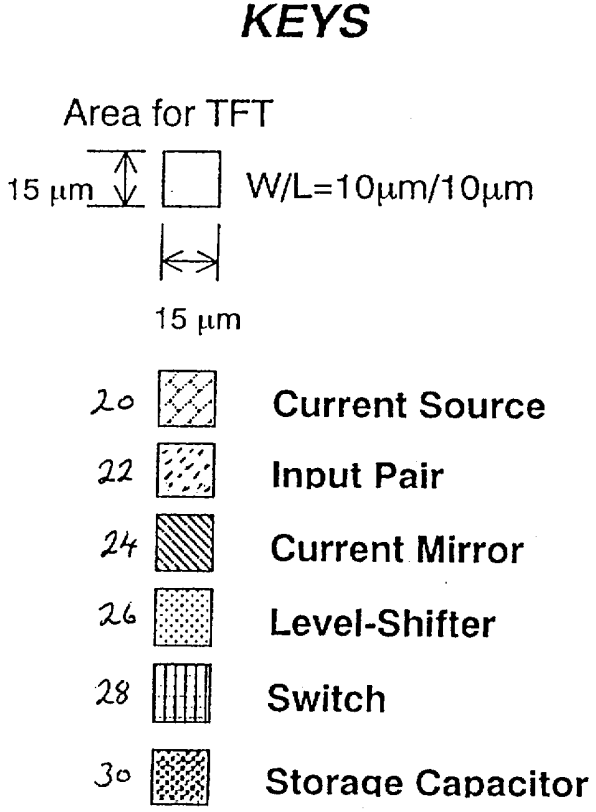

KEYS
Area for TFT
15 μm
W/L=10μm/10μm
15 μm
20
Current Source
22
Input Pair
24
Current Mirror
26
Level-Shifter
28
Switch
30
Storage Capacitor

Figure 3

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Display Device

The present invention relates to a display device, particularly a display device comprising a plurality of pixels with each pixel containing a light emitting element and a plurality of circuit components.

There is a desire to fabricate a display device of the aforementioned type using a large number of thin film transistors (hereinafter referred to as TFTs) on a single substrate. However, devices comprising a large number of TFTs on a single substrate suffer from the problem of relatively large spatial variation of the transistor characteristics. The problem can be sufficiently severe to result in some analog circuits simply failing to operate to their designed standard. Although it might be possible, in at least some devices, to overcome this problem by introducing compensation circuits; such a solution increases the component count, increases the required substrate area and increases operating power consumption. Further, for example, there is currently no known design of such compensation circuits available for use with CMOS transistors.

It is an object of the present invention to provide a display device which can be implemented using TFTs, which avoids the use of compensation circuits and which reliably performs to it's design standard.

According to the present invention there is provided a display device comprising a plurality of pixels, each pixel containing a light emitting element and a plurality of substantially rectangular shaped circuit areas at least some of which include thin film transistors, the circuit areas comprising two current mirror circuit areas and two input pair circuit areas; the two current mirror circuit areas abutting each other so as to have a side of their rectangular areas in common, the two input pair circuit areas abutting each other so as to have a side of their rectangular areas in common, with both of the input pair circuit areas abutting a respective one of the current mirror circuit areas so as each to have a side of their rectangular areas in common.

The above described arrangement of circuit areas has been shown to overcome the spatial variation of characteristics problem while avoiding the use of compensating circuits. Additionally, the described arrangement of circuit areas can reduce to a minimum the p-type and n-type doping area required within each pixel.

Embodiments of the present invention will now be described in more detail, by way of further example only and with reference to the accompanying drawings in which:-

Figure 1 is a circuit diagram of pixel level circuitry to which the present invention can be applied;

Figure 2 contains a circuit and waveform diagram for the comparator included in the circuitry shown in figure 1; and

Figure 3 illustrates the detailed arrangement of the circuit components within each pixel according to an embodiment of the present invention.

Co-pending patent application (Agent's Ref: GBP13234A) describes an organic electroluminescent active matrix display device comprising a driver circuit which modulates the duty cycle of the on-state of a pixel during a frame period so as to provide gray scaling. The display provides pulse width modulation of the on-period of a pixel and the integrating function of the human eye perceives this as modulation of the intensity of the emitted light. Modulation of the on-period is in stark contrast to the conventional control of brightness to provide gray scaling in such devices, ie control of the instantaneous amplitude of the current supplied. Figure 1 is a circuit diagram of the pixel level circuitry disclosed in the co-pending application.

Figure 1 is a circuit diagram of an individual pixel 10 within an active matrix OELD display panel. The circuit is implemented using polysilicon TFT components and comprises an MOS-input comparator 12 and two pass-gates, T_1 and T_2. Comparator 12 comprises a long tail differential pair 16 and an inverter 18. The use of pass-gates avoids so-called "feed-through", i.e. coupling with other circuit voltages. The inverting input (+) of the comparator 12 is connected to a waveform source V_{DRV}. The non-inverting input (-) is connected to a storage capacitor C_1 and a pass-gate T_1. The pass-gate T_1 is controlled by a waveform V_{SCAN}. The output of the comparator is connected to a pass-gate T_2. Pass-gate T_2 controls the current flowing in to the organic light emitting element 14. By applying a time varying signal to V_{DRV}, the light emitting element 14 is switched on for a period depending on the value of the data voltage V_{DAT} which is applied to the other side of pass-gate T_1 compared to the capacitor C_1 and the comparator 12.

In a line-at-a-time driving scheme, V_{SCAN} sets the state of the pass-gate T_1 of the pixel elements on the same row. When pass-gate T_1 is closed, the data voltage V_{DAT} is

transferred to the inverting input of the comparator 12 and to the capacitor C_1. Then, when pass-gate T_1 is opened the data voltage is memorised by capacitor C_1. The waveform V_{DRV} is then initiated. When the voltage, V_+, at the inverting input of the comparator 12 is less than the voltage, V-, at the non-inverting input thereof, the comparator outputs a LO signal which puts the light emitting element 14 in to the on-state. When the voltage, V_+, at the inverting input of the comparator 12 is greater than the voltage, V-, at the non-inverting input thereof, the comparator outputs a HI signal which puts the light emitting element 14 in to the off-state. As a result the data voltage stored by the capacitor C_1 modulates the duration for which the light emitting element 14 remains in the on-state during a frame period.

The frame period might typically be 20mS and with the response time of the light emitting element 14 being of the order of nano-seconds, the speed of the polysilicon TFTs and any stray capacitance become the limiting factors in operation of the driving scheme. That is, exceptionally effective switching can be obtained.

In the circuit illustrated in figure 1, a common operating voltage V_{OELD} is used for all OELD pixels of the same type. The voltage V_{OELD} is set externally and is independent of the supply voltage V_{DD} of the driving circuit. This significantly increases the flexibility of controlling the bias conditions for the OELDs.

A description will now be given of the detailed considerations which apply to the practical implementation of the comparator 12 used in the circuit of figure 1.

Since a separate comparator is provided for each pixel, the circuit area and power consumption of the comparator should be kept as low as possible. Further, in order to achieve a high number of gray scales, the comparator must be able to distinguish a small difference in input voltages. For example, if it is desired to implement 256 gray scales with a voltage swing of 0V to 5V then clearly something of the order of $\Delta V = 19.5mV$ is appropriate. Thus switching must be very fast but, from the previous discussion, it is well within the ability of the described circuit.

A detailed circuit diagram of one implementation of the comparator 12 of figure 1 is illustrated in figure 2. The circuit of figure 2 comprises two stages: a CMOS differential amplifier 16, and a CMOS inverter 18. The CMOS inverter 18 turns the pass-gate T_2 fully

on or fully off very quickly. For level shifting purposes the power supply of the inverter stage 18 can be different from that of the differential stage 16.

The differential stage 16 comprises the drain-source series connection circuit of transistors T_3, T_4 and T_6 connected between the V_{DD} rail and ground, together with the similarly connected circuit of transistors T_3, T_5 and T_7, wherein transistors T_5 and T_7 are connected in parallel with transistors T_4 and T_6. The respective gates of transistors T_4 and T_5 provide the two input terminals (+), (-) of the comparator 12, whereas the gate of transistor T_3 receives a bias voltage V_{BIAS}. The output stage 18 comprises two transistors, T_8 and T_9, which are source-drain series connected between the V_{DD} rail and ground. The output V_{OUT} of the comparator is taken from the connection between the transistors T_8 and T_9 and the gates thereof receive there input from the junction between transistors T_4 and T_6.

The circuit illustrated in figure 2 uses seven TFTs. Using a respective TFT for T_1 and T_2 brings the total per pixel to nine. As illustrated; TFTs T_1, T_2, T_3, T_4, T_5 and T_8 are p-type and TFTs T_6, T_7 and T_9 are n-type. All of these TFTs, as well as the storage capacitor, the OELD and all of the connection leads must be accommodated in the area of one pixel. Typically the pixel area might be 70.5μm^2 and the OELD (denoted by "LEP" in figure 3) might be assigned a circular area of 30μm^2 diameter.

As illustrated in figure 3, the circuit components are assigned to rectangular areas of 15μm by 15μm. This compares with an achievable TFT size (W/L) of 10μm/10μm. Generally, it is preferred that the area of each circuit area is substantially equal to one quarter of the area of the light emitting element. The layout of the ten rectangular circuit areas is illustrated in figure 3. They comprise: one current source area 20, two input pair areas 22, two current mirror areas 24, two level shifter areas 26, two switch areas 28 and a storage capacitor area 30.

The present invention resides, in part, in the determination of the device components which are most critically sensitive to variation of transistor characteristic. It has been determined that the most critically sensitive components are the input pair (22) and the current mirror pair (24). The input pair consists of transistors T_4 and T_5 and the current mirror pair consists of transistors T_6 and T_7. The present invention resides, in part, in arranging the two current mirror circuit areas 24 to abut each other so as to have a side of their rectangular areas in common, in arranging the two input pair circuit areas 22 to abut

each other so as to have a side of their rectangular areas in common, and in arranging for both input pair circuit areas to abut a respective one of the current mirror circuit areas each to have a side of their rectangular areas in common. That is, the four circuit areas form a square one half of which is occupied by the two input pair transistors and the other half of which is occupied by the two current mirror transistors.

Preferably, the two current mirror circuit areas abut each other so as to have a side of their rectangular areas in common, the two input pair circuit areas abut each other so as to have a side of their rectangular areas in common, the two level shifter circuit areas abut each other so as to have a side of their rectangular areas in common, both input pair circuit areas abutting a respective one of the current mirror circuit areas, and one current mirror circuit area abutting a level shifter circuit area so as to have a side of their rectangular areas in common. Preferably, the current source circuit area abuts one of the input pair circuit areas so as to have a side of their rectangular areas in common. Preferably, the current source circuit area abuts one of the level shifter circuit areas so as to have a side of their rectangular areas in common. Preferably, the capacitor circuit area abuts one of the current mirror circuit areas so as to have a side of their rectangular areas in common. Preferably, one switch circuit area abuts one of the input pair circuit areas so as to have a side of their rectangular areas in common. Preferably, the said one switch circuit area abuts the capacitor circuit area so as to have a side of their rectangular areas in common. Preferably, the second switch circuit area abuts one of the current mirror circuit areas so as to have a side of their rectangular areas in common. Preferably, the second switch circuit area abuts one of the level shifter circuit areas so as to have a side of their rectangular areas in common. These preferences, which are illustrated in figure 3, result in the p-type and n-type doping area within the pixel being kept to a minimum.

Adjacent pixels might be arranged to have light emitting elements having different wavelength outputs. Thus, the three, elements denoted LEP in figure 3 might for example have respective outputs in the red, green, and blue regions of the spectrum. A colour display can thus be achieved.

CLAIMS

1. A display device comprising a plurality of pixels, each pixel containing a light emitting element and a plurality of substantially rectangular shaped circuit areas at least some of which include thin film transistors, the circuit areas comprising two current mirror circuit areas and two input pair circuit areas; the two current mirror circuit areas abutting each other so as to have a side of their rectangular areas in common, the two input pair circuit areas abutting each other so as to have a side of their rectangular areas in common, with both of the input pair circuit areas abutting a respective one of the current mirror circuit areas so as each to have a side of their rectangular areas in common.

2. A display device as claimed in claim 1, wherein the circuit areas further comprise two level shifter circuit areas.

3. A display device as claimed in claim 2, wherein the two level shifter circuit areas abut each other so as to have a side of their rectangular areas in common, and one current mirror circuit area abutting a level shifter circuit area so as to have a side of their rectangular areas in common.

4. A display device as claimed in claim 1, wherein the circuit areas further comprise a current source circuit area.

5. A display device as claimed in claim 3, wherein the current source circuit area abuts one of the input pair circuit areas so as to have a side of their rectangular areas in common.

6. A display device as claimed in claim 2 and claim 4, wherein the current source circuit area abuts one of the level shifter circuit areas so as to have a side of their rectangular areas in common.

7. A display device as claimed in claim 1, wherein the circuit areas further comprise a switch circuit area.

8. A display device as claimed in claim 7, wherein the switch circuit area abuts one of the input pair circuit areas so as to have a side of their rectangular areas in common.

9. A display device as claimed in claim 7, wherein the switch circuit area abuts the capacitor circuit area so as to have a side of their rectangular areas in common.

10. A display device as claimed in claim 1, wherein the circuit areas further comprise a capacitor circuit area.

11. A display device as claimed in claim 10, wherein the capacitor circuit area abuts one of the current mirror circuit areas so as to have a side of their rectangular areas in common.

12. A display device as claimed in claim 7, wherein the circuit areas comprise a second switch circuit area.

13. A display device as claimed in claim 12, wherein the second switch circuit area abuts one of the current mirror circuit areas so as to have a side of their rectangular areas in common.

14. A display device as claimed in claim 2 and claim 12, wherein the second switch circuit area abuts one of the level shifter circuit areas so as to have a side of their rectangular areas in common.

15. A display device as claimed in any preceding claim, wherein the circuit areas are all of substantially the same size.

16. A display device as claimed in any preceding claim, wherein each pixel is of substantially rectangular shape and each light emitting element is located in one corner of the respective pixel.

17. A display device as claimed in any preceding claim, wherein the area of each circuit area is substantially equal to one quarter of the area of the light emitting element.

18. A display device as claimed in any of claims 1 to 16, wherein the area of each circuit area is substantially equal to $1/\pi$ of the area of the light emitting element.

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Application No: GB 0023789.1 9 **Examiner:** Richard Pannett
Claims searched: 1-18 **Date of search:** 3 April 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): G5C (CHBH CHE)

Int Cl (Ed.7): G09G 3/06, 3/12, 3/20, 3/30, 3/32

Other: Online: WPI, EPODOC, PAJ, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	WO 99/65012	(KNAPP) For example, page 4, lines 4-28	1
Y	US 5903246	(DINGWALL) For example, column 2, lines 10-26 and claim 1.	1
Y	US 4528480	(UNAGAMI) For example, column 5, lines 40-59 and column 9, lines 10-25.	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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