The present invention relates to an apparatus and a method for sigma–delta modulation with a reduced periodic noise (idle noise) in a sigma–delta modulator. The reduction is achieved by means of addition of two different Dither signals (217, 218) to the sigma–delta modulator. A first Dither signal (218) is constituted by a particular bit pattern of a certain period while a second Dither signal (217) is constituted by a pseudo–random signal of a certain other period.
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APPARATUS AND METHOD FOR THE REDUCTION OF PERIODIC NOISE IN A SIGMA-DELTA MODULATOR

TECHNICAL FIELD

The present invention relates to a method of sigma-delta modulation with reduced periodic noise.

DESCRIPTION OF RELATED ART

In most audio devices, for example, mobile telephones or CD-players in which an analogue/digital or digital/analogue conversion is carried out, often a sigma-delta modulator is used in the analogue/digital or digital/analogue converter.

A sigma-delta modulator according to prior art comprises a number of integrators, a number of amplifiers and a quantifier. These are arranged in a way characteristic to the sigma-delta modulator. The configuration of a sigma/delta modulator is described below.

In a sigma-delta modulator there arises, when its input signal is low, constant, or changes slowly, a so-called periodic noise, or idle tones. Even if the periodic noise has a relatively low amplitude it is fully audible to the human ear. This noise must therefore be reduced to a non-audible level.

In EP 0 709 969 A2, a sigma-delta modulator reducing periodic noise by means of a Dither signal is disclosed. The Dither signal is a random signal, for example, a pseudo-noise code (PN-code). This Dither signal may be added in one or more places in the sigma-delta modulator. Depending on where the addition of the Dither signal in the sigma-delta modulator is carried out, the signal is filtered by a particular filter before the addition.
A preferred length of the PN-code is that the period of the PN-code is much longer than the period of the lowest frequency to be treated by the sigma-delta modulator. The PN-code should be at least 21 bits long. The rectified AC-power of the Dither signal is dependent on the order of the sigma-delta modulator.

One disadvantage of this solution is that depending on where it is chosen to add the Dither signal, one or more filters will be needed.

Another common solution for reducing the periodic noise in the sigma-delta modulator is adding the Dither signal in one of the integrators. The Dither signal is added without filtering.

This solution also has the disadvantage that the performance of the sigma-delta modulator is deteriorated.

A deterioration of the signal/noise ratio in the sigma-delta modulator implies that the complexity of the sigma-delta modulator must be increased. This means that a larger number of integrators must be used in the sigma-delta modulation to maintain the desired level of performance.

If the sigma-delta modulator is comprised in a D/A-converter, there is another solution to the deterioration of the signal/noise ratio. It is then possible to increase the over-sampling rate in an interpolation filter in the D/A-converter or increase the complexity of a low-pass filter arranged at the output of the signal-delta modulator.

The three solutions mentioned above, however, lead to an increased power consumption and an increased complexity of the sigma/delta modulator, which is not desirable for radio communication devices, such as mobile telephones.
SUMMARY OF THE INVENTION

The present invention attacks the problem of reducing periodic noise (idle tones) in a sigma-delta modulator.

Another problem attacked by the present invention is to maintain, when reducing the periodic noise, the signal/noise ratio for output signals from the sigma-delta modulator without increasing the complexity of the sigma-delta modulator.

Yet another problem attacked by the present invention is, when reducing the periodic noise when the inventive apparatus and the inventive method for sigma-delta modulation are comprised in a D/A-converter, to maintain the signal/noise ratio for output signals from the D/A-converter without increasing the complexity of the D/A-converter.

One object of the present invention is therefore to provide an apparatus and a method for sigma-delta modulation with reduced periodic noise in the modulated output signal.

Another object is to obtain, when reducing the periodic noise, a good signal/noise ratio for the output signal of the sigma-delta modulator without increasing the complexity of the sigma-delta modulator performing the modulation procedure.

The above-mentioned problems are solved according the present invention by adding two different signals to the sigma-delta modulator. The first signal has a relatively short period. Said first signal is added to one of the most significant bits of the sigma-delta modulator. The second signal has, compared to said first signal, a long period. The second signal is added to the least significant bit of one of the integrators comprised in the sigma-delta modulator.
One advantage of the inventive apparatus and the inventive method is that the reduction of periodic noise is carried out without causing a deterioration of the signal/noise ratio of the output signal from the sigma-delta modulator.

Another advantage of the present invention is that, since the complexity can be kept down when reducing the periodic noise, a sigma-delta modulator consuming relatively little power is obtained.

The invention will now be described in more detail by means of preferred embodiments and with reference to the appended drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a D/A-converter comprising a sigma-delta modulator.

Figure 2 is a block diagram of a sigma-delta modulator representing one embodiment of an inventive apparatus and an inventive method.

Figure 3 is a block diagram of a sigma-delta modulator representing another embodiment of the inventive apparatus and the inventive method.

Figure 4 is a block diagram of a sigma-delta modulator representing yet another embodiment of the inventive apparatus and the inventive method.

Figure 5 is a block diagram of a sigma-delta modulator representing yet another embodiment of the inventive apparatus and the inventive method.
DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 is a block diagram of a D/A-converter 100 according to prior art. The D/A-converter 100 comprises a time-discrete interpolation filter 102 arranged to receive a time-discrete signal 101 comprising a number of N bits. If, for example, the D/A-converter 100 is arranged in a GSM-mobile telephone, the time-discrete signal 101 is a digital 13-bit signal. The time-discrete interpolation filter 102 increases the sampling rate of the received time-discrete signal 101 so that a new time-discrete signal 103 having a higher sampling rate is obtained. This increase of the sampling rate is carried out to obtain a better signal/noise ratio in the analogue output signals 108 received from the D/A-converter 100. The ratio between the higher sampling rate and the lower sampling rate is here called Over-Sampling Ratio (OSR). The new time-discrete signal 103 is fed to a sigma-delta modulator 104. The sigma-delta modulator 104, comprising a number of integrators and a quantifier, is arranged to generate an output signal 106. The output signal 106 can assume a previously determined number of amplitude levels. Said output signal 106 is often a 1-bit signal with only two different levels. In such a case, a conversion has been carried out from a value represented by N bits to a number of samples that can assume two different amplitude values. The time-discrete signal 106 is fed to a low-pass filter 107, arranged to even out the time-discrete 1-bit signal 106 between different amplitude values, in order to obtain the analogue signal 108 in this way.

A/D-converters function principally in the opposite way to that described above. One difference is that the D/A-converter 100 is implemented mainly with digital hardware 105, whereas the A/D-converter is implemented mainly with analogue components.

Figure 2 is a block diagram of a sigma-delta modulator representing an embodiment of an inventive apparatus and an inventive method. The sigma-delta modulator 104 is arranged to receive the time-discrete signal 103 occurring at an input 206 of said
sigma-delta modulator, and to generate the output signal 106 as an output 207 of the sigma-delta modulator. The output signal 106 is dependent on the time-discrete signal 103. The sigma-delta modulator 104 comprises two integrators 200,201, a quantifier 202, three adders 203, 204, 205, a first Dither generator 216 intended to generate a first Dither signal 218 and a second Dither generator 215 intended to generate a second Dither signal 217.

In the first Dither generator 216, which may be, for example, a memory or a shift register, the first Dither signal 218 is stored. The first Dither signal 218 is a 1-bit sequence of a previously defined amplitude and having a relatively short period. The relatively short period implies that the first Dither signal 218 does not comprise any frequency components in a frequency range intended for the D/A-converter 100. In, for example, audio devices intended for the human ear, this frequency range corresponds to the frequencies that may be perceived by the human ear, i.e. in a frequency range substantially equal to 0-20 kHz. How to select the amplitude and the period of the second Dither signal will be explained below.

From the second Dither generator 215, which may be, for example, a maximum-length shift register, the second Dither signal 217 is generated with a long period, a low amplitude and with statistic properties similar to those of white noise. How to select the length and the amplitude will be described below. The second Dither signal 217 is a 1-bit sequence which, when generated with a maximum length shift register of the length 22 and a period longer than 4 seconds, obtains statistic properties similar to those of white noise. The period of 4 seconds should here be seen as a relatively long period. This Dither signal is primarily intended to avoid the sigma-delta modulator generating an output signal having tones in the frequency range intended for the sigma-delta modulator, depending on the first Dither signal 218.

The adder 203 is arranged to add the time-discrete signal 103 to the output signal 106, which is fed back by means of a feedback connection 208 through a multiplier
219, whereby a first sum signal 209 is obtained. A multiplication factor k for the multiplier 219 is selected in a manner known in the art. If k is selected as k<0, a subtraction of said output signal from said time-discrete signal 103 is performed. Said first sum signal 209 is integrated in the integrator 200, whereby a first integrated signal 210 is obtained. The adder 204 is arranged to add said first integrated signal 210 to the output signal 106, which is fed back, through a multiplier 220, in the same way as described above. A first partial sum is obtained in this addition. The adder 204 is arranged to add the first Dither signal 218 to one of the most significant bits of the first partial sum. The additions performed in the adder can, of course, be performed in the opposite order. Thereby a second sum signal 211 is obtained. The second sum signal 211 is integrated in the integrator 201, whereby a second integrated signal 212 is obtained. The adder 205 is arranged to add the second integrated sum signal to the output signal 106, which is fed back to a multiplier 221, and to the second Dither signal 218, whereby a third sum signal 214 is obtained. The second Dither signal 218 is added to one of the least significant bits. The third sum signal occurs as an input 213 of the quantifier 202 arranged to generate the output signal 106. The output signal 106 is a signal that can assume two levels.

The output signal 106 is fed back through the three multipliers 219,220,221 with a respective multiplication factor k,l,m. The multiplication factors k,l,m may be determined in different ways. Generally, however, an analysis of transfer functions for the noise and the signal must be carried out. How to determine said multiplication coefficients is previously known by those skilled in the art.

The first Dither signal 218 is a 1-bit signal having a previously determined spectral property. The first Dither signal should not, for a predetermined sampling frequency $f_s$ of the received signal 101 and a determined OSR (OverSampling Ratio), comprise frequency components in a range $f_B$ intended for the D/A-converter 100, which may be, for example, the base band range of a mobile telephone. The length of the first Dither signal 218, to fulfil the above, should preferably be shorter than
the period of the highest frequency $f_{BH}$ of the frequency range intended for the D/A-converter. This is achieved if the second Dither signal 217 is selected with a bit sequence shorter than $\frac{1}{f_{BH}} \times f_s \times OSR$ bits. The human ear can perceive tones up to 20 kHz, which gives the highest frequency of D/A converters arranged, for example, in mobile telephones. Using, for example, the sampling rate $f_s=8000$Hz and OSR=64, the requirement that the first Dither signal 218 comprise no frequency components within the frequency range audible to man is fulfilled if the first Dither signal is selected shorter than 26 bits. This is achieved by substituting the above mentioned values in the above mentioned equation: $\frac{1}{20000} \times 8000 \times 64 \approx 26$ bits.

The amplitude of the first Dither signal is preferably selected as 4-32 times lower than the amplitude of the feedback output signal. The selection of the amplitude of the first Dither signal is dependent on the structure of the sigma-delta modulator and the bit to which the first Dither signal is added. The amplitude of the first Dither signal may be simulated after the structure of the sigma-delta modulator has been determined.

The second Dither signal 217 is a bit sequence having statistic properties corresponding to those of white noise. This may be, for example a Pseudo Noise (PN) code generated by a maximum-length shift register. The period of this Dither signal should be long, preferably a few seconds. If, for example, a period of 4 seconds is desired when the sampling rate $f_s$ is equal to 8000 Hz and OSR is equal to 64, the bit sequence, the period, should be longer than 2048000 bits ($4 \times 8000 \times 64 = 2048000$). This sequence is obtained using a maximum-length shift register of the length 22, which gives a period of $(2^{22} - 1) = 4194303$. How to design a maximum-length shift register of a certain length is well known to the person skilled in the art.

The amplitude of the first Dither signal is determined by connecting the Dither generator 216 with a controllable amplitude to an adder in the sigma-delta modulator.
The amplitude is increased until no periodic noise is found in the output signal 108. This may be checked in several ways, for example by connecting a spectrum analyzer registering the frequency components of the signals, for registering the output signal 108.

In this embodiment the first Dither signal 218 as well may be connected to the adder 205 and the second Dither signal 217 may be connected to the adders 203, 204. The same result as above will be obtained.

Figure 3 is a block diagram of a sigma-delta modulator representing a second embodiment of the inventive apparatus and the inventive method. The difference between the embodiment described in connection with Figure 2 and the one shown in Figure 3 is that the embodiment shown in Figure 3 comprises an additional integrator 300, and is therefore referred to as a 3rd order sigma-delta modulator, an adder 302 and an amplifier 301.

The input signal 103 is added to the output signal 106, amplified in the amplifier 301, in the adder 302, whereby a sum signal is obtained. This sum signal is integrated in the integrator 300 generating an integrated signal 303. Instead of the input signal 103 described in connection with Figure 2, the adder 203 thereby obtains the input signal 303. In all other respects the sigma-delta modulator functions as described above in connection with Figure 2.

The Dither signal 217 and the Dither signal 218 used in the two embodiments described above, of course, are not exactly the same signal, but have been adjusted according to that described above.

In this embodiment the first Dither signal 218 as well may be connected to one of the adders 203, 205 and the second Dither signal 217 may be connected to one of the adders 203, 204, 302. The same result as above will be obtained.
Figure 4 is a block diagram of a sigma-delta modulator representing another embodiment of the inventive apparatus and the inventive method. The difference between this embodiment and the one described in connection with Figure 2 is that the Dither generators 216, 215 have changed places. A first Dither signal 417 generated by one of the Dither generators 215 is added to the first integrated signal 210 and the output signal 106 fed back through the amplifier 220, in the adder 204, in the same way as described in connection with Figure 2 for the Dither signal 217, whereby a second sum signal 411 is obtained. The sum signal 411 is integrated in the integrator 201, whereby a second integrated signal 412 is obtained. A second Dither signal 418 is added to the second integrated signal 412 and to the output signal 106, fed back through the amplifier 221, whereby a third sum signal 414 is obtained. Said addition is carried out in the same way as described in connection with Figure 2 for the Dither signal 218. The output signal 106 is obtained at the output 106 in the same way as described above, by quantification 202 of the third sum signal 414.

Figure 5 is a block diagram of yet another embodiment of the inventive sigma-delta modulator. The difference between the one described in connection with Figure 3 is that the Dither generators 216, 215 have changed places. The first Dither signal 417 generated by the Dither generator 215 is added to the first integrated signal 210 and to the output signal 106 fed back through the amplifier 220, in the adder 204, in the same way as described in connection with Figure 3 for the Dither signal 217, whereby a second sum signal 511 is obtained. The sum signal 511 is integrated in the integrator 201, whereby a second integrated signal 512 is obtained. The second Dither signal 418 is added to the second integrated signal 512 and to the output signal 106, fed back through the amplifier 221, whereby a third sum signal 514 is obtained. Said addition is carried out in the same way as described in connection with Figure 3 for the Dither signal 218. The output signal 106 is obtained at the output
106 in the same way as described above, by quantification 202 of the third sum signal 414.

The invention is of course not limited to the ones described above and shown in the drawings, but may be modified within the scope of the claims.
Claims

1. A method of sigma-delta modulation, said method being carried out with a reduction of periodic noise, comprising the following steps:
   a) at least a first integration (200) of a signal (209, Fig. 2) corresponding to an input signal (103) added to an output signal (106) multiplied by a predetermined factor k, whereby a first integrated signal (210) is obtained;
   b) at least a second integration (201) of said first integrated signal (210) added to a first signal (218), whereby a second integrated signal (212) is obtained;
   c) quantification (202) of said second integrated signal (212) added to a second signal (217), whereby said output signal (106) is obtained, characterized in
      that the first signal (218) is constituted by a particular bitmap of a certain period;
      and
   that the second signal (217) is constituted by a pseudo-random signal of a certain period.

2. A method according to claim 1, characterized in
   that the first signal (218) is constituted by a one-bit time discrete sequence of a certain determined period, which is short relative to the period of said second signal (217); and
   that the second signal (217) is constituted by a one-bit time discrete sequence of a certain determined period.

3. A method according to claim 2, wherein said input signal (103) and said first integrated signal (210) are constituted by an N-bit time discrete signal, characterized in
   that the first signal (218) is added to a previously determined bit in said first integrated signal (210); and
that the second signal (217) is added to a least significant bit in the second integrated signal (212); and
that said output signal (106) is constituted by a one-bit time discrete signal.

4. A method according to any one of the claims 2 and 3, characterized in
that the period of the first signal (218) is such that its frequency components lie outside a frequency range of the sigma-delta modulator; and
that the period of the second signal (217) is so long that the sequence repeats itself with a frequency not audible to man.

5. A method according to claim 4 wherein the frequency range of the sigma-delta modulator is audible to man, characterized in that the period of the first signal (218) repeats itself with a frequency not audible to man.

6. A method according to any one of the preceding claims, characterized in
that the second integration (201) is preceded by an addition of said output signal (106) multiplied by a predetermined factor \( l \); and
that the quantification (202) is preceded by an addition of said output signal (106) multiplied by a predetermined factor \( m \).

7. A method of sigma-delta modulation, said method being carried out with a reduction of periodic noise, comprising the following steps:
a) at least a first integration (200) of a signal (209, Fig. 4) corresponding to an input signal (103) added to an output signal (106) multiplied by a predetermined factor \( k \), whereby a first integrated signal (210) is obtained;
b) at least a second integration (201) of said first integrated signal (210) added to a first signal (417), whereby a second integrated signal (412) is obtained;
c) quantification (202) of said second integrated signal (412) added to a second signal (418), whereby said output signal (106) is obtained,
characterized in
that the first signal (417) is constituted by a pseudo-random signal of a certain period; and
that the second signal (418) is constituted by a particular bitmap of a certain period.

8. A method according to claim 7, characterized in
that the first signal (417) is constituted by a one-bit time discrete sequence of a certain determined period; and
that the second signal (418) is constituted by a one-bit time discrete sequence of a certain determined period, which is short relative to the period of said first signal.

9. A method according to claim 8, wherein said input signal (103) and said first integrated signal (210) are constituted by an N-bit time discrete signal, characterized in
that the first signal (417) is added to a least significant bit in the second integrated signal (212); and
that the second signal (418) is added to a previously determined bit in said first integrated signal (210); and
that said output signal (106) is constituted by a one-bit time discrete signal.

10. A method according to any one of the claims 8 and 9, characterized in
that the period of the first signal (417) is so long that the sequence repeats itself with a frequency not audible to man; and
that the period of the second signal (418) is such that its frequency components lie outside a frequency range of the sigma-delta modulator.

11. A method according to claim 10 wherein the frequency range of the sigma-delta modulator is audible to man, characterized in that the period of the first signal (418) repeats itself with a frequency not audible to man.
12. A method according to any one of the preceding claims, characterized in that the second integration (201) is preceded by an addition of said output signal (106) multiplied by a predetermined factor l; and that the quantification (202) is preceded by an addition of said output signal (106) multiplied by a predetermined factor m.

13. An apparatus for sigma-delta modulation, said sigma-delta modulation being carried out with a reduction of periodic noise, said apparatus comprising

a) at least one first integrator (200) arranged for the integration of a signal (209, Fig. 2), corresponding to an input signal (103) added to an output signal (106) multiplied by a previously determined factor k, whereby a first integrated signal (210) is obtained;

b) at least one second integrator (201) arranged for the integration of said first integrated signal (210) added to a first signal (218), whereby a second integrated signal (212) is obtained;

c) a quantifier (202) arranged for the quantification of said second integrated signal (212) added to a second signal (217), whereby said output signal (106) is obtained,

characterized in that a first Dither generator (216) is arranged to generate the first signal (218) constituted by a particular bitmap of a certain period; and that a second Dither generator (215) is arranged to generate the second signal (217) constituted by a pseudo-random signal of a certain period.

14. An apparatus according to claim 13, characterized in that the first Dither generator (216) is constituted by a memory means; and that the second Dither generator (215) is constituted by a maximum length shift register.
15. An apparatus according to claim 13, characterized in that the first Dither generator (216) is constituted by a shift register; and that the second Dither generator (215) is constituted by a maximum length shift register.

16. An apparatus according to any one of the claims 13-15, characterized in that a first adder (204) is arranged to add said output signal (106) multiplied by a previously determined factor \( l \) to the first integrated signal (210) and that a second adder (205) is arranged to add said output signal (106) multiplied by a previously determined factor \( m \) to the second integrated signal (212).

17. An apparatus for sigma-delta demodulation, said sigma-delta demodulation being carried out with a reduction of periodic noise, said apparatus comprising

a) at least one first integrator (200) arranged for the integration of a signal (209, Fig. 4), corresponding to an input signal (103) added to an output signal (106) multiplied by a previously determined factor \( k \), whereby a first integrated signal (210) is obtained;

b) at least one second integrator (201) arranged for the integration of said first integrated signal (210) added to a first signal (417), whereby a second integrated signal (412) is obtained;

c) a quantifier (202) arranged for the quantification of said second integrated signal (412) added to a second signal (418), whereby said output signal (106) is obtained,

characterized in that a first Dither generator (215) is arranged to generate the first signal (417) constituted by a pseudo-random signal of a certain period; and that a second Dither generator (216) is arranged to generate the second signal (418) constituted by a particular bitmap of a certain period.

18. An apparatus according to claim 17, characterized in
that the first Dither generator (215) is constituted by a maximum length shift register; and
that the second Dither generator (216) is constituted by a memory means.

19. An apparatus according to claim 17, characterized in
that the first Dither generator (215) is constituted by a maximum length shift register; and
that the second Dither generator (216) is constituted by a shift register.

20. An apparatus according to any one of the claims 17-19, characterized in
that a first adder (204) is arranged to add said output signal (106), multiplied by
a previously determined factor l, to the first integrated signal (210); and
that a second adder (205) is arranged to add said output signal (106), multiplied by
a previously determined factor m, to the second integrated signal (212).

21. A method of digital/analogue conversion of an N bit time discrete signal (101) to
an analogue signal (108) corresponding to said time discrete signal (101) and with a
reduced periodic noise, said method comprising the following steps:
interpolation filtering (102) of the N bit time discrete signal (101) with a particular
sampling rate, whereby a time discrete signal (103) of a certain higher sampling rate
is obtained;
sigma-delta modulation (104) of the time-discrete signal (103) with said higher
sampling rate, whereby an output signal (106) having a certain number of amplitude
levels is obtained; and
low-pass filtering (107) of said output signal (106), whereby the analogue signal
(108) corresponding to the N-bit time discrete signal (101) is obtained,
characterized in that the sigma-delta modulation is carried out according to the
method of claim 1.
22. A method of digital/analogue conversion of an N bit time discrete signal (101) to an analogue signal (108) corresponding to said time discrete signal (101) and with a reduced periodic noise, said method comprising the following steps: interpolation filtering (102) of the N bit time discrete signal (101) with a particular sampling rate, whereby a time discrete signal (103) of a certain higher sampling rate is obtained; sigma-delta modulation (104) of the time-discrete signal (103) with said higher sampling rate, whereby an output signal (106) having a certain number of amplitude levels is obtained; and

low-pass filtering (107) of said output signal (106), whereby the analogue signal (108) corresponding to the N-bit time discrete signal (101) is obtained, characterized in that the sigma-delta modulation is carried out according to the method of claim 7.

23. An apparatus for the digital/analogue conversion of an N-bit time discrete signal (101) to an analogue signal (108) corresponding to said time discrete signal (101) with reduced periodic noise, said apparatus comprising: means for interpolation filtering (102) of the N-bit time discrete signal (101) with a certain sampling rate, whereby a time discrete signal (103) of a certain higher sampling rate is obtained; means for the sigma-delta modulation (104) of the time discrete signal (103) with said higher sampling rate, whereby an output signal (106) having a certain number of amplitude levels is obtained; means for the low-pass filtering (107) of said output signal (106), whereby the analogue signal (108) corresponding to the N-bit time discrete signal (101) is obtained, characterized in that said means for the sigma-delta modulation is constituted by an apparatus according to claim 13.
24. An apparatus for the digital/analogue conversion of an N-bit time discrete signal (101) to an analogue signal (108) corresponding to said time discrete signal (101) with reduced periodic noise, said apparatus comprising:

means for interpolation filtering (102) of the N-bit time discrete signal (101) with a certain sampling rate, whereby a time discrete signal (103) of a certain higher sampling rate is obtained;

means for the sigma-delta modulation (104) of the time discrete signal (103) with said higher sampling rate, whereby an output signal (106) having a certain number of amplitude levels is obtained;

means for the low-pass filtering (107) of said output signal (106), whereby the analogue signal (108) corresponding to the N-bit time discrete signal (101) is obtained, characterized in that said means for the sigma-delta modulation is constituted by an apparatus according to claim 17.