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(71) Applicant *(for all designated States except US)*: **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, New York 14650-2201 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **XU, Weize** [CN/US]; 155 Crandon Way, Rochester, New York 14618 (US).

(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, New York 14650-2201 (US).

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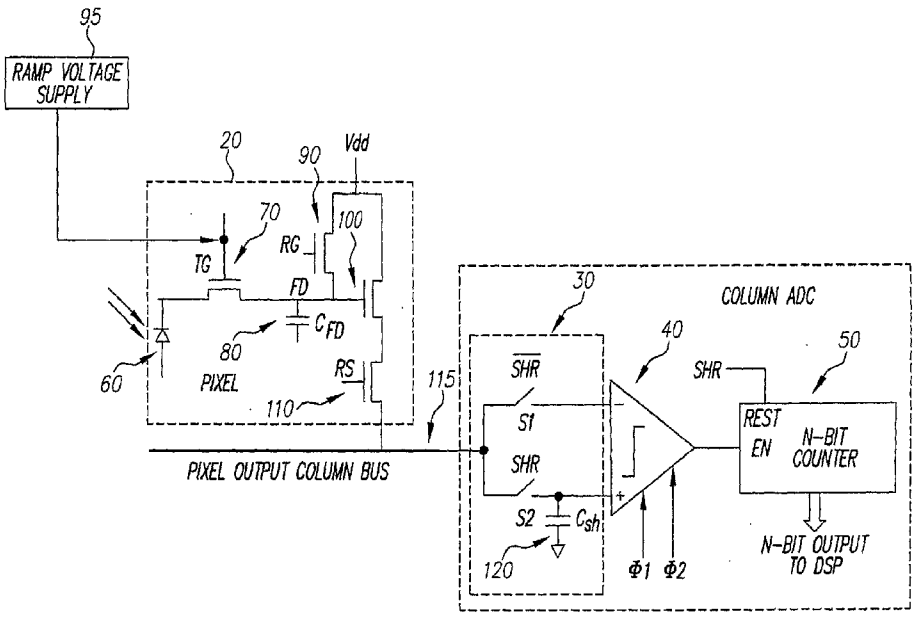
(54) **Title:** A/D CONVERTER USING RAMPED TRANSFER GATE CLOCKS



(57) **Abstract:** An image sensor includes a photosensitive region that accumulates charge corresponding to received incident light; a transfer gate for transferring charge from the photosensitive region; a voltage supply having an increasing voltage over time; a floating diffusion for receiving the charge from the photosensitive region and converting the charge to a voltage; an amplifier for receiving and amplifying a signal from the floating diffusion; a comparator for comparing a voltage from the amplifier to a reference voltage; and a counter for counting clock cycles between initiation of the increasing voltage until a signal is received from the comparator indicating charge transfer from the photosensitive region to the floating diffusion; wherein a digital signal is generated that represents an unfilled capacity of the photosensitive region.

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A/D CONVERTER USING RAMPED TRANSFER GATE CLOCKS

FIELD OF THE INVENTION

The invention relates generally to the field of image sensors, and more particularly, to such CMOS image sensors in which the image signal is converted into a digital signal immediately after output from the pixel array.

BACKGROUND OF THE INVENTION

Presently known CMOS image sensors all have the same or substantially the same structures. They typically include the photosensitive devices, like a photodiode or photogate, in the pixel array to convert the optical signal to charge; a floating diffusion capacitor for converting the charge to a voltage; and a pixel amplifier buffering the floating diffusion capacitance from the large output bus capacitance and sending the electrical signal out of the pixel array. The pixel output signals are stored by a sample/hold circuit array followed by an analog signal processing chain and an analog-to-digital converter.

The drawbacks for this present CMOS image sensor is the high noise, low speed and high power. These problems can be addressed by moving the analog-to-digital conversion to earlier stages and then processing the signal in the digital domain. One such prior art for processing in digital domain in an earlier stage is disclosed in IEEE Journal of Solid-State Circuits, Vol. 36, No. 12, December 2001 (page 2049). This prior art includes a ramped voltage applied to a comparator independently of the pixel. This independence can cause pixel-to-pixel non-uniformities at the output.

Consequently, a need exists for addressing the high noise, low speed and high power of the image sensors having the latter stage analog-to-digital conversion circuits and the pixel-to-pixel non-uniformities of the image sensors having earlier stage analog-to-digital conversion circuits. This pixel-to-pixel non-uniformities is addressed in the present invention in which the transfer gate

adjacent the photodiode is ramped, and the reference voltage is from the pixel reset.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, the invention resides in an image sensor comprising (a) a photosensitive region that accumulates charge corresponding to received incident light; (b) a transfer gate for transferring charge from the photosensitive region; (c) a voltage supply having a ramped voltage over time; (d) a floating diffusion for receiving the charge from the photosensitive region and converting the charge to a voltage; (e) an amplifier for receiving and amplifying a signal from the floating diffusion; (f) a comparator for comparing a voltage from the amplifier to a reference voltage; and (g) a counter for counting clock cycles between initiation of the increasing voltage until a signal is received from the comparator indicating charge transfer from the photosensitive region to the floating diffusion.

The above and other objects of the present invention will become more apparent when taken in conjunction with the following description and drawings wherein identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

Advantageous Effect Of The Invention

The present invention has the advantage of high-speed processing, lower power dissipation and low noise. It further eliminates the effects of non-linearity and threshold variations in the pixel amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of the image sensor of the present invention;

Fig. 2 is a schematic diagram of Fig. 1;

Fig. 3 is a timing diagram for Fig 2;

Fig. 4a illustrates the image sensor of the present invention in schematic form;

Fig. 4b illustrates a cross section of the present invention;

Fig. 4c illustrates a well potential diagram for Fig. 4b for clearly illustrating the concept of the present invention; and

Fig. 5 is a digital camera of the present invention for illustrating a typical commercial embodiment for the image sensor of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 1, there is shown a image sensor 10 of the present invention having a plurality of pixels 20 and a plurality of sample and hold circuits 30 for receiving and storing the signals from the plurality of pixels 20 in a predetermined manner. A plurality of comparators 40 are respectively connected to the output of each sample and hold circuit 30, and a plurality of counters 50 are respectively connected to the plurality of comparators 40.

For clarity of understanding, it is noted that the above-described apparatus of the present invention limits the analog circuit usage (for the purpose of noise reduction) and maximally utilizes the advantages of digital circuits. It is also noted that Fig. 2 illustrates only one pixel and its associated circuitry of the present invention for illustrating a representative pixel of the plurality of pixels of the present invention for clarity of understanding. It is understood that the present invention includes a plurality of such pixels; for example, the pixel array 20 as shown in Fig. 1. Referring to Fig. 2, the pixel 20 is composed of a photosensitive region or photodiode 60 that accumulates charge in response to incident light. A transfer gate 70 receives a ramped voltage over time (preferably an increasing voltage over time) from a voltage supply 95 which causes transfer of charge from the photodiode 60 to a charge-to-voltage conversion region or floating diffusion 80, which converts charge to a voltage signal. The increasing voltage is supplied by a voltage supply 95 which is preferably on-chip but outside the pixel array 20. The voltage supply 95 may optionally be located off-chip in an alternative embodiment. A reset transistor 90 sets a reference voltage for both the floating

diffusion 80 and the sample and hold circuit 30, which (in the case of the sample and hold circuit 30) will be subsequently used by the comparator 40, as will be described in detail hereinbelow. An amplifier or amplifier transistor 100 receives and amplifies the signal from the floating diffusion 80. A row select transistor 110 selects the particular row of pixels for output to the sample and hold circuit 30.

Fig. 3 includes the preferred timing for Fig. 2 and includes common timing signal acronyms for the timing signal to be applied to a component referred to in Fig. 2 - RS, TG, RG and SHR. Referring now to Figs. 2 and 3, an image is captured by the plurality of photodiodes 60 during integration, and after integration, a row of pixels in the pixel array is selected for readout by applying a "high" to the gate of row select transistor 110. A pulse voltage is then applied to the gate of the reset transistor 90 to clear charge from the floating diffusion (FD) capacitor 80 and to then reset the floating diffusion 80 to the reference voltage. The voltage at FD 80 is amplified by the amplifier 100 and sent out to the column bus. With the reference signal at the output node 115, clock SHR goes from "low" to "high" to close switch S2 and open switch S1. The reference voltage is sampled onto the capacitor (Csh) 120. The SHR clock also resets the counter 50. Following the SHR pulse, a ramped or an increasing voltage over time is applied onto the transfer gate 70 to create a potential underneath the transfer gate 70 for transferring the signal from the photodiode 60 to the floating diffusion 80. Then SHR changes from high to low, switch S1 closes and S2 opens which puts the comparator 40 in the comparing state, and the counter 50 starts counting clock cycles until the comparator 40 signals the counter 50 to terminate counting. The comparator 50 compares the pixel output voltage to the sampled reset voltage in each column.

When the ramped TG voltage generates a sufficient potential underneath the TG gate 70, charge accumulated in photodiode 60 begins to flow from photodiode 60 to floating diffusion 80. It is noted that the present invention uses the floating diffusion 80 to sense the "beginning" or "initiation" of charge transfer from the photodiode 60, as opposed to sensing the "entire" charge on the photodiode as in the prior art. Returning to the present invention discussion, a

voltage change is created at the floating diffusion 80 upon initiation of charge transfer, and the voltage change is sent out through the pixel amplifier 100 to the column comparator 40. This voltage change triggers the comparator 40 to change output states. The "enable" input of the counter 50 senses the change in output from the comparator 40 and then stops counting. The content of the column counter 50 is the raw pixel digital output.

A digital calibration function is included in the A/D conversion operation by sampling incident light in darkness which is stored in memory (on or off-chip). This calibration signal will be subtracted from the digital signal representing the captured image. The pixel noise and pixel amplifier offset are removed or greatly reduced.

Referring to Figs. 4a-4c, it is noted for clarity that the prior art detects the number of electrons. In contrast, the image sensor of the present invention detects the electrical charge potential of the photodiode, or in other words, it detects the depth of the unfilled potential well of the photodiode. With the presence of the light on the photodiode 60 in the pixel array 20, electrical charges are generated and accumulated in an electrical potential well 121 in the photodiode 60. There is a transfer gate 70 in the pixel in between the photodiode 60 and a floating diffusion 80, which floating diffusion 80 is used to convert the charge to voltage. The voltage applied on the gate of the transfer gate 70 controls the potential underneath the gate and creates a conductive channel when the voltage is higher the threshold voltage of the transfer gate 70. The potential well 121 of the photodiode 60 and the floating diffusion area 80 are connected by this created channel of the transfer gate 70. With the increase of this gate voltage, the electrical potential underneath the gate is lowered. When the potential underneath the transfer gate 70 is equal to the electrical potential of the well 121 of the photodiode 60, charge accumulated in the photodiode 60 starts to move from photodiode 60 to the diffusion area 80 through the transfer gate 70. The move of charge from photodiode 60 to the floating diffusion 80 will generate a voltage signal at the floating diffusion area 80 which is then sent to the input of the pixel amplifier 100. The circuit in the column sample-and-hold array 30 compares the

voltage signal at the pixel amplifier output 115 to a previously generated reference voltage when the transfer gate voltage is applied. The move of the electrons from photodiode 60 to the floating diffusion 80 will trigger the comparator 40 in the sample-and-hold circuit 30 to change its output state. This change of comparator 40 output state stops the counter 50 and a digital code is generated at the counter 50 output. This digital code or the digital signal represents the image signal created by the pixel.

Referring to Fig. 5, there is shown a digital camera 125 in which the image sensor 10 of the present invention is disposed for illustrating a preferred commercial embodiment of the present invention.

PARTS LIST

10	image sensor
20	plurality of pixels
30	sample and hold circuits
40	comparators
50	counters
60	photodiode
70	transfer gate
80	floating diffusion
90	reset transistor
95	voltage supply
100	amplifier transistor
110	row select transistor
115	output node or pixel amplifier output
120	capacitor (Csh)
121	electrical potential well
125	digital camera

CLAIMS:

1. An image sensor comprising:

(a) a photosensitive region that accumulates charge corresponding to received incident light;

(b) a transfer gate for transferring all or a portion of the charge from the photosensitive region;

(c) a voltage supply having a ramped voltage over time that is applied to the transfer gate;

(d) a floating diffusion for receiving all or a portion of the charge from the photosensitive region and converting the charge to a voltage;

(e) an amplifier for receiving and amplifying a signal from the floating diffusion;

(f) a comparator for comparing a voltage from the amplifier to a reference voltage; and

(g) a counter for counting clock cycles between initiation of the increasing voltage until a signal is received from the comparator which indicates initiation of charge transfer from the photosensitive region to the floating diffusion.

2. The image sensor as in claim 1, wherein the ramped voltage is an increasing voltage over time.

3. The image sensor as in claim 1 further comprising a reset transistor for generating the reference voltage.

4. The image sensor as in claim 1 further comprising a capacitor electrically connected to the comparator for holding the reference voltage.

5. The image sensor as in claim 1, wherein the photosensitive region is a photodiode.

6. The image sensor as in claim 1 further comprising a row select transistor electrically connected to the amplifier for enabling readout.

7. An imaging device comprising:

(a) a photosensitive region that accumulates charge corresponding to received incident light;

(b) a transfer gate for transferring all or a portion of the charge from the photosensitive region;

(c) a voltage supply having a ramped voltage over time that is applied to the transfer gate;

(d) a floating diffusion for receiving all or a portion of the charge from the photosensitive region and converting the charge to a voltage;

(e) an amplifier for receiving and amplifying a signal from the floating diffusion;

(f) a comparator for comparing a voltage from the amplifier to a reference voltage; and

(g) a counter for counting clock cycles between initiation of the increasing voltage until a signal is received from the comparator which indicates initiation of charge transfer from the photosensitive region to the floating diffusion.

8. The imaging device as in claim 7, wherein the ramped voltage is an increasing voltage over time.

9. The imaging device as in claim 7 further comprising a reset transistor for generating the reference voltage.

10. The imaging device as in claim 7 further comprising a capacitor electrically connected to the comparator for holding the reference voltage.

11. The imaging device as in claim 7, wherein the photosensitive region is a photodiode.

12. The imaging device as in claim 7 further comprising a row select transistor electrically connected to the amplifier for enabling readout.

13. An image sensor comprising:

(a) a photosensitive region having a capacity in which charge accumulates that corresponds to received incident light;

(b) a transfer gate for transferring all or a portion of the charge from the photosensitive region;

(c) a voltage supply having a ramped voltage over time that is applied to the transfer gate;

(d) a charge collection portion for receiving all or a portion of the charge from the photosensitive region and converting the charge to a voltage; and

(e) a circuit which indicates initiation of charge transfer from the photosensitive region to the charge collection portion.

14. The image sensor as in claim 13, wherein the ramped voltage is an increasing voltage over time.

15. The image sensor as in claim 13, wherein the charge collection region is a floating diffusion.

16. The image sensor as in claim 13, wherein the photosensitive region is a photodiode.

17. The image sensor as in claim 16, wherein the charge collection region is a floating diffusion.

18. An imaging device comprising:

(a) a photosensitive region having a capacity in which charge accumulates which corresponds to received incident light;

(b) a transfer gate for transferring all or a portion of the charge from the photosensitive region;

(c) a voltage supply having a ramped voltage over time that is applied to the transfer gate;

(d) a charge collection portion for receiving all or a portion of the charge from the photosensitive region and converting the charge to a voltage; and

(e) a circuit which indicates initiation of charge transfer from the photosensitive region to the charge collection portion.

19. The imaging device as in claim 18, wherein the ramped voltage is an increasing voltage over time.

20. The imaging device as in claim 18, wherein the charge collection region is a floating diffusion.

21. The imaging device as in claim 18, wherein the photosensitive region is a photodiode.

22. The imaging device as in claim 21, wherein the charge collection region is a floating diffusion.

23. A method of operating an image sensor, the method comprising the steps of:

(a) accumulating charge corresponding to received incident light by a photosensitive region having a capacity;

(b) transferring all or a portion of the charge from the photosensitive region by a transfer gate;

(c) applying a ramped voltage over time to the transfer gate;

(d) receiving all or a portion of the charge from the photosensitive region and converting the charge to a voltage by a charge collection portion; and

(e) indicating initiation of charge transfer from the photosensitive region to the charge collection portion.

24. The method as in claim 23 further comprising the step of providing an increasing voltage over time as the ramped voltage.

25. The method as in claim 23 further comprising the step of providing the charge collection region as a floating diffusion.

26. The method as in claim 23 further comprising the step of providing the photosensitive region as a photodiode.

27. The method as in claim 26 further comprising the step of providing the charge collection region as a floating diffusion.

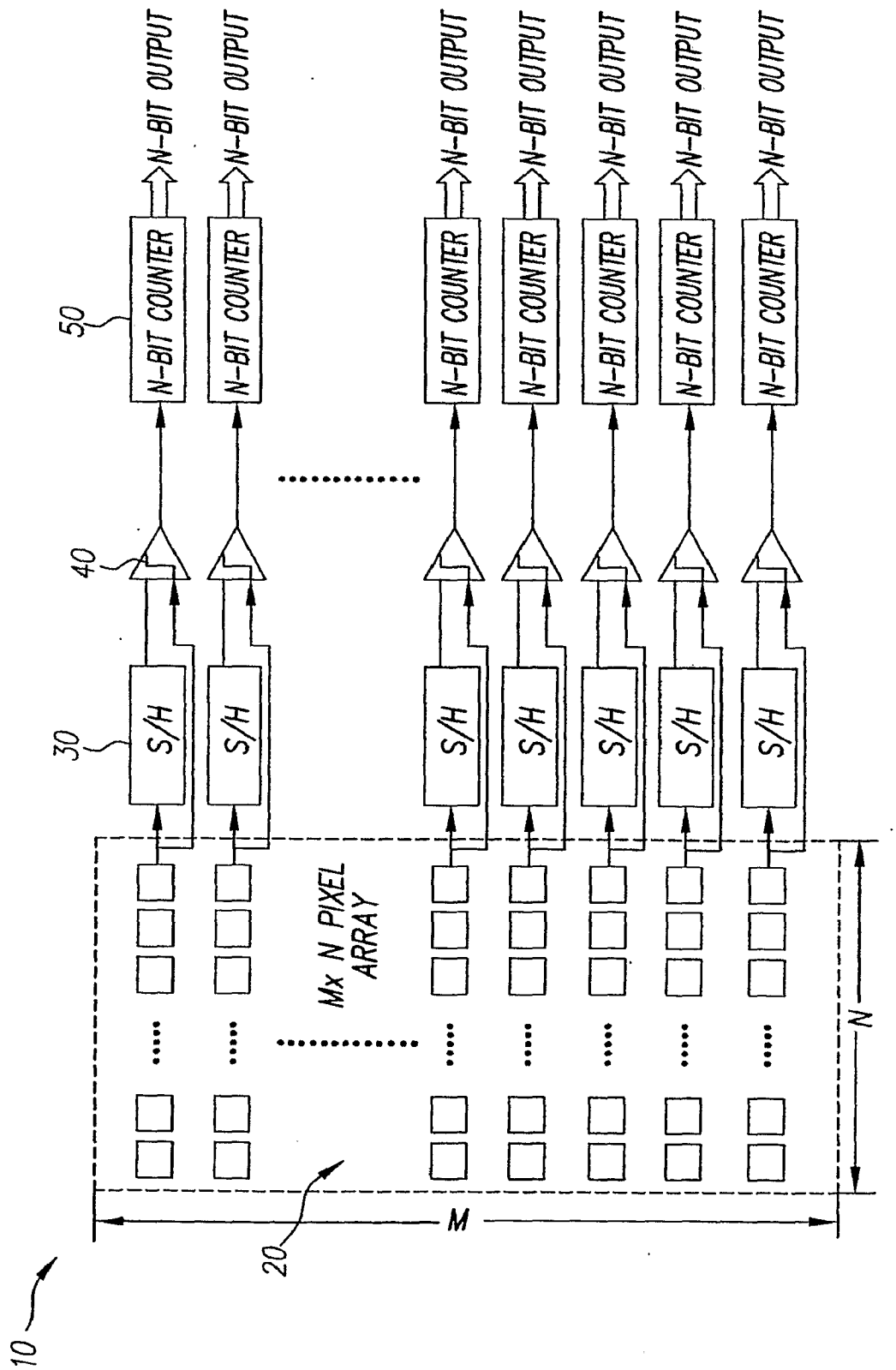

FIG. 1

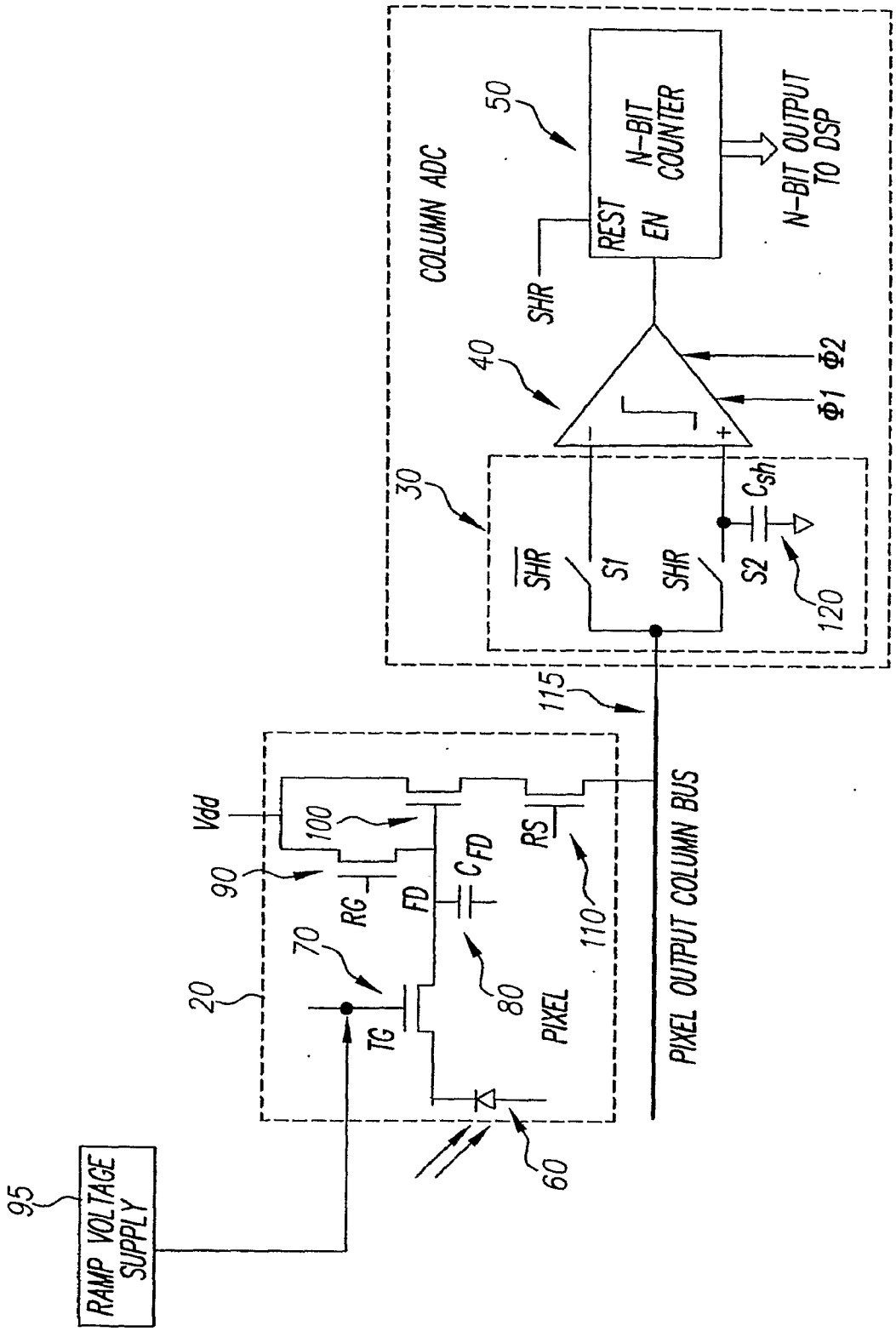
COLUMN ADC
50
N-BIT COUNTER
REST
EN
N-BIT OUTPUT TO DSP
SHR
40
Φ2
Φ1
30
C_{sh}
$\overline{SHR}$
S1
SHR
S2
120
115
PIXEL OUTPUT COLUMN BUS
Vdd
100
90
RG
FD
C_{FD}
RS
110
70
20
TG
80
PIXEL
60
95
RAMP VOLTAGE SUPPLY

FIG. 2

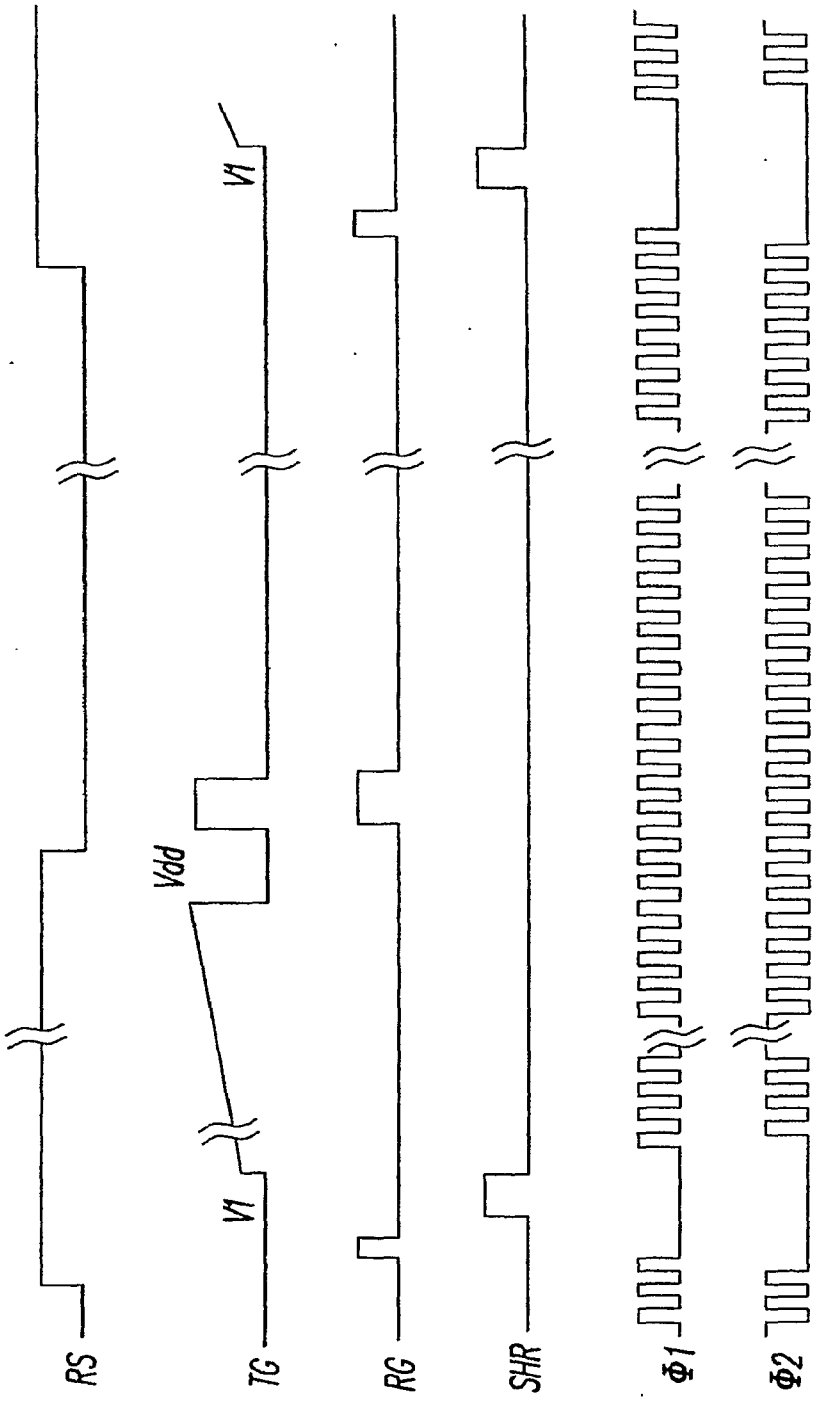

FIG. 3

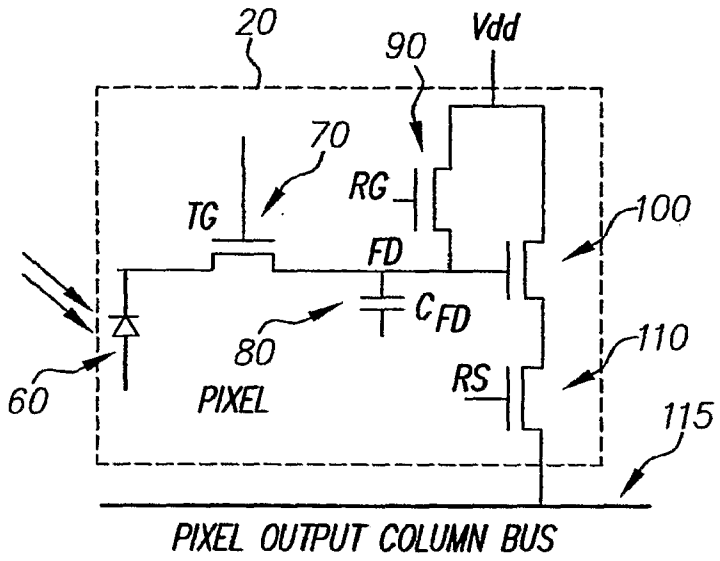
20
90
Vdd
70
RG
TG
100
FD
C_{FD}
80
110
60
PIXEL
RS
115
PIXEL OUTPUT COLUMN BUS

FIG. 4a

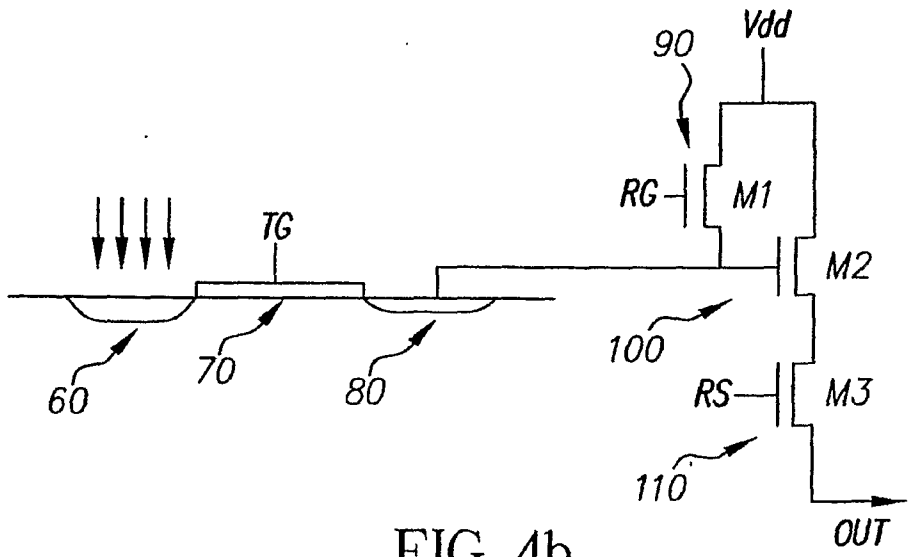
90
Vdd
RG
M1
TG
M2
100
60
70
80
RS
M3
110
OUT

FIG. 4b

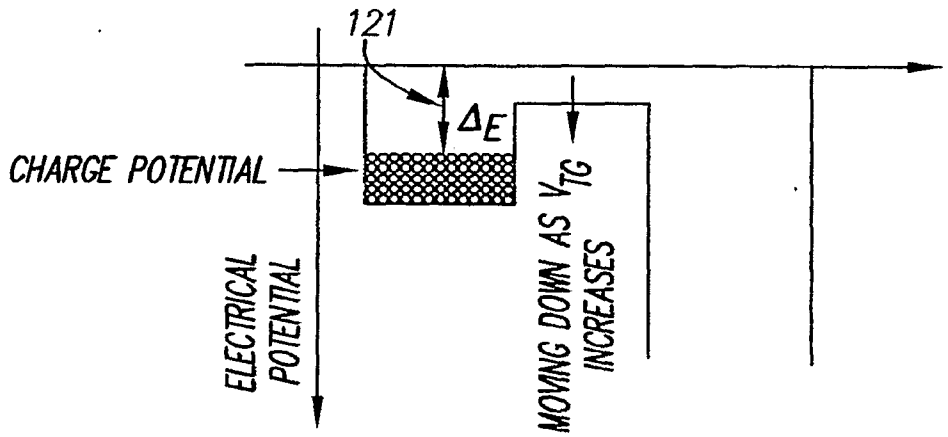
121
Δ_E
CHARGE POTENTIAL
ELECTRICAL POTENTIAL
MOVING DOWN AS V_{TG} INCREASES

FIG. 4c

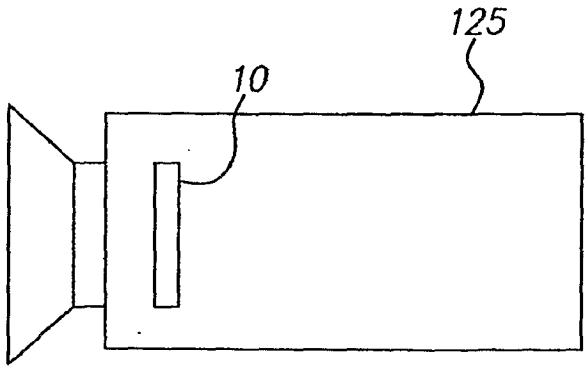
125
10

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/003332

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/083421 A1 (BEREZIN VLADIMIR [US] ET AL) 21 April 2005 (2005-04-21) paragraphs [0028], [0031]; figure 5	13-27
A	WO 2005/120046 A (COUNCIL CENT LAB RES COUNCILS [GB]; CROOKS JAMIE [GB]; TOWRIE MIKE [GB) 15 December 2005 (2005-12-15) page 2, line 26 - page 3, line 8; figure 2	1,7
A	US 2003/058360 A1 (LIU XINQIAO [US] ET AL) 27 March 2003 (2003-03-27) paragraph [0091]; figures 1,4	1,7
A	US 2002/067417 A1 (TAN CHARLES M C [US] ET AL) 6 June 2002 (2002-06-06) paragraph [0024]; figures 1,2	1,7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
22 June 2007	04/07/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bequet, Thierry

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/003332

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005083421 A1	21-04-2005	NONE	
WO 2005120046 A	15-12-2005	EP 1762088 A2	14-03-2007
US 2003058360 A1	27-03-2003	NONE	
US 2002067417 A1	06-06-2002	NONE	