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(71) Applicant: **THE REGENTS OF THE UNIVERSITY OF CALIFORNIA** [US/US]; 1111 Franklin St., Twelfth Floor, Oakland, CA 94607-5200 (US).

(72) Inventors: **MISHRA, Umesh**; 2040 Creekside Road, Montecito, CA 93108 (US). **KELLER, Stacia**; 1335 San Antonio Creek Road, Santa Barbara, CA 93111 (US). **AHMADI, Elaheh**; 7910 18th Avenue, Apt. 104, Hyattsville, MD 20783 (US). **GUPTA, Chirag**; 460 Whitman Street, Apt. 76, Goleta, CA 93117 (US). **TSUKADA, Yusuke**; Umezono 2-15-5, Yokota-Bild. 4, Tsukuba, Ibaraki 305-0045 (JP).

(74) Agent: **SERAPIGLIA, Gerard, B.** et al.; Gates & Cooper LLP, 6060 Center Drive, Suite 830, Los Angeles, CA 90045 (US).

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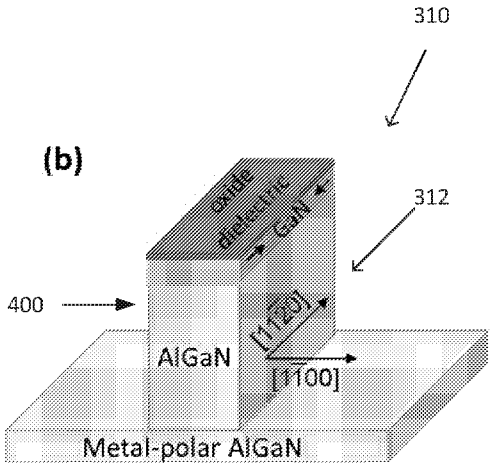

Fig. 3

(57) Abstract: Strain is used to enhance the properties of p- and n- materials so as to improve the performance of III-N electronic and optoelectronic devices. In one example, transistor devices include a channel aligned along uniaxially strained or relaxed directions of the III-nitride material in the channel. Strain is introduced using buffer layers or source and drain regions of different composition.

WO 2020/149922 A2

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III-N BASED MATERIAL STRUCTURES, METHODS, DEVICES AND CIRCUIT MODULES BASED ON STRAIN MANAGEMENT

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit under 35 U.S.C. Section 119(e) of the following co-pending and commonly-assigned application:

U.S. Provisional Application Serial No. 62/756,999, filed on November 7, 2018, by Umesh Mishra, Stacia Keller, Elaheh Ahmadi, Chirag Gupta, and Yusuke Tsukada, entitled "III-N BASED MATERIAL STRUCTURES, METHODS, DEVICES AND CIRCUIT MODULES BASED ON STRAIN MANAGEMENT," attorneys' docket number G&C 30794.0655USP2 (UC 2017-99F);

which application is incorporated by reference herein.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

This invention was made with Government support under Grant Nos. N00014-16-1-2933, N00014-17-1-2106 and N00014-16-1-2250 from the Office of Naval Research, awarded by the U.S. Office of Naval Research. The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to III-N based material structures, methods, devices and circuit modules based on strain management.

2. Description of the Related Art.

(Note: This application references a number of different publications as indicated throughout the specification by one or more reference numbers in brackets, e.g., [x]. A list of these different publications ordered according to these reference

numbers can be found below in the section entitled "References." Each of these publications is incorporated by reference herein.)

SUMMARY OF THE INVENTION

Previous group-III-Nitride photonic devices are based on biaxial strained heterostructures. Their performance is often limited by the low hole conductivity in group-III Nitride materials, which is associated in part with the high relative hole mass in the nitrides, resulting in a very low hole mobility. This invention describes how strain can be incorporated into photonic nitride heterostructures, resulting in an upward movement of the light hole band and formation of holes with a relative mass less than electrons, as derived from previous band structure calculations. The availability of the light holes results in significant performance improvements in photonic devices. For example, the invention enables the improvement of the performance of optoelectronic devices, in particular lasers and LEDs, where it leads to a significant reduction in the threshold carrier density.

In another embodiment, this invention utilizes strain to enhance the properties of p-channel and n-channel materials and implements the benefits of these materials. The invention enables the improvement of the performance of p-type and n-type III-N electronic devices.

Example devices include, but are not limited to, the following.

1. A device (e.g., electronic or optoelectronic), comprising:

III-nitride material strained along a first direction and at least partially relaxed along a direction perpendicular to the first direction.

2. The device of example 1, wherein the III-nitride is on or above porous III-nitride, and patterned into ridge or fin structures, wherein the porous III-nitride allows relaxation or partial relaxation of the fin structure perpendicular to the fin or the short axis while the fin material remains strained or relaxes less in the direction along the fin or the long direction resulting in uniaxial strain in the fin structure.

3. The device of example 2, wherein the porous III-nitride includes etched pores.

4. The device of example 2 or example 3, wherein the porous III-nitride comprises gallium nitride.

5. The device of example 1, wherein the device is a field effect transistor (FET), including:

a stripe comprising the III-nitride material, wherein:

the III-nitride material is strained along the first direction comprising a long axis of the stripe and at least partially relaxed along the second direction comprising a direction (short axis) perpendicular to the long axis ;

the III-nitride material includes a channel layer;

a source contact comprising first metal on the stripe making ohmic contact to the channel;

a drain contact comprising second metal on the stripe making ohmic contact to the channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of current along a direction of the long axis or short axis through the channel and between the source contact and the drain contact.

6. The device of example 5, wherein:

the channel comprises gallium and/or indium and/or aluminum (and/or boron)

the III-nitride material comprises the channel layer on a layer including gallium and/or aluminum and/or indium and/or boron,

a thickness of the layer comprising gallium and/or aluminum, and/or indium is more than 50% of a thickness of the stripe,

an composition is selected so as to obtain a desired strain in the channel along the long axis.

7. The device of example 5, wherein:

the III-nitride material further includes a source region and a drain region,

the source region is in physical contact with the channel layer between the source contact and the channel layer,

the drain region is in physical contact with the channel layer between the drain contact and the channel layer, and

the source region and the drain region have a lattice constant different than a lattice constant of channel so as to induce the strain in the channel layer along the long axis.

8. The device of example 7, wherein the source region and the drain region comprise gallium and/or aluminum, and/or indium (e.g., InGaN channel case on GaN).

9. The device of any of the examples 5-8, wherein:

the current between the source contact and the drain contact is along the long axis that is a crystallographic a- or m-direction of the III-nitride,

the short axis direction perpendicular to the long axis is a crystallographic m- or a- direction of the III-nitride, respectively.

the top surface of the stripe has a polar (0001) or (000-1) orientation, and

the channel has a lattice constant larger than the underlying III-nitride material.

10. The device of any of the examples 5-8, wherein:

the current between the source contact and the drain contact is along the short axis that is a crystallographic a- or m-direction of the III-nitride,

the long axis direction perpendicular to the short axis is a crystallographic a- or m-direction of the III-nitride,

the top surface of the stripe has a polar (0001) or (000-1) orientation, and

the channel has a lattice constant smaller than the underlying III-nitride material.

11. The device of any of the examples 5-8, wherein:

the current between the source contact and the drain contact is along the short axis that is a crystallographic m-direction of the III-nitride,

the long axis direction perpendicular to the short axis is a crystallographic c-direction of the III-nitride, and

the top surface of the stripe has a nonpolar a- or m-plane orientation.

12. The device of any of the examples 5-9, wherein the FET comprises a p-type FET conducting the current comprising holes and the strain along the long axis is uniaxial compressive strain.

13. A device comprising a CMOS device of any of the examples 5-12 wherein the FET comprises a p-type FET, the CMOS device further including:

the stripe including a second n-type FET including a second source contact to the III-nitride material, a second drain contact to the III-nitride material, and a second gate contact on the stripe between the second source contact and the second drain contact;

the III-nitride material comprises a second n-type channel layer between the second source contact and the second drain contact; and

insulator between the n-type FET and the p-type FET.

14. The CMOS device of example 13, wherein the second channel layer is strained along the long axis between the second source contact and the second drain contact.

15. The devices of any of the examples 5-9 or 13-14, wherein the strain along the long axis is uniaxial compressive strain and the long axis is along a direction of lowest hole effective mass.

16. A device, comprising:

a bipolar heterojunction transistor (BJT), including:

a stripe comprising first n-type material, wherein the n-type is strained along a long axis of the stripe;

an emitter contact on a top surface of the stripe;

p-type material between the first n-type material and second n-type material, wherein the p-type material is on a bottom surface of the stripe opposite the emitter contact;

a base contact to the p-type material;

a collector contact to the second n-type material; wherein a direction of electron flow in an active mode of the BJT is between the emitter and the collector.

17. The device of example 16, wherein the strain along the long axis is uniaxial tensile strain.

18. The device of any of the examples 16-17, further comprising the base contact on a side of the stripe parallel to the long axis.

19. The device of any of the examples 16-18, further comprising a plurality of the BJTs attached to the stripe and further including an additional base contact on top of the stripe between the BJTs.

20. The device of any of the examples 16-19, wherein the n-type material and the p-type material comprise III-nitride material.

21. A field effect transistor (FET), comprising:

a stripe including III-nitride material, wherein:

the III-nitride material includes an n-type channel layer strained along a long axis of the stripe and at least partially relaxed along a direction perpendicular to the long axis;

the III-nitride material includes an n-type channel layer which is more strained/less relaxed along a long axis of the stripe and less strained/ more relaxed along a direction perpendicular to the long axis; and

the n-type channel layer comprises gallium and/or aluminum, and/or indium;

a source contact comprising first metal on the stripe making ohmic contact to the n-type channel;

a drain contact comprising second metal on the stripe making ohmic contact to the n-type channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of electron current along the direction perpendicular to the long axis through the n-type channel layer and between the source contact and the drain contact.

22. The FET of example 21, wherein the III-nitride material includes a layer comprising aluminum and gallium and indium between the n-type channel and the source contact, the drain contact, and the gate contact.

23. The FET of examples 21 or 22, wherein a top surface of the stripe on which the source contact and drain contact are formed is an N-polar surface, so that the n-type channel layer has an N-polar orientation.

24. The FET of example 23, wherein the current flows through a 2DEG induced from a back-barrier comprising the layer of gallium and/or aluminum, and/or indium, so contact to the 2DEG is formed over an entire contact area and not merely at an edge of the ohmic regions contacting the n-type channel layer.

25. The device or FET of any of the preceding examples, wherein the stripe length is at least 2 times longer than the stripe width.

26. An optoelectronic device, comprising:

a stripe comprising III-nitride material, wherein:

the III-nitride material is strained along a long axis of the stripe and at least partially relaxed along a direction perpendicular to the long axis or the short axis; and

the III-nitride material includes:

an active region;

a III-nitride n-type layer; and

a III-nitride p-type layer, wherein the active region is between the n-type layer and the p-type layer.

27. The device of example 26, wherein the active region includes InGaN, the p-type region includes n-type GaN, and the p-type layer comprises p-type GaN.

28. The device of example 26 or 27, further comprising:

a pixel including the stripe;

material grown on either side of the stripe so as to create compressive strain in the layers in the stripe, resulting in light hole formation in the enclosed layers and additional improved hole transport occurring along the stripe direction.

29. The device of example 28, wherein the material grown on either side of the stripe comprises InGaN.

30. The device of examples 26-29, wherein the device has an N-polar orientation.

31. The device of examples 26-30, wherein the device comprises a light emitting diode, a laser diode, a solar cell, or a photodiode.

32. A device, comprising:

III-nitride material is strained along a long axis of the stripe and at least partially relaxed along a direction perpendicular to the long axis or the short axis;

the III-nitride material includes a channel layer;

a source contact comprising first metal on the stripe making ohmic contact to the channel;

a drain contact comprising second metal on the stripe making ohmic contact to the channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of current along a direction of the long axis or short axis through the channel and between the source contact and the drain contact.

33. The device of examples 1-2, wherein the device is a transistor, a light emitting diode, a laser diode, a solar cell or a photodiode, and the III-nitride material includes the device's active region.

34. The device of example 33, wherein the active region includes InGaN.

35. The device of examples 33 or 34, wherein the device is biased and contacted so as to take advantage of lower effective hole mass along the first direction.

36. The device of example 35, wherein the device comprises a field effect transistor including a channel, wherein the source and drain are along the first

direction so that current flows along the first direction between the source and the drain.

37. The device of example 36, wherein the III-nitride material is relaxed over a distance of at least one micron in the second direction.

38. A device, comprising:

III-nitride material which is at least partially biaxially relaxed.

39. The device of example 1 or 38, wherein the III-nitride is on a porous III-nitride, and patterned into features, wherein the porous III-nitride allows relaxation or partial biaxial relaxation of the structure.

40. The device of example 2 or 39, wherein the porous III-nitride includes etched pores.

41. The device of example 2, 3 or 39 or 40, wherein the porous III-nitride comprises gallium nitride.

42. A device comprising III-nitride or gallium nitride, wherein the III-nitride or the gallium nitride is biaxially strained such that the biaxial strain results in the split-off band as the topmost valence band (above the light hole and the heavy hole in the valence band) resulting in increased hole mobility in a vertical direction.

43. A device, comprising a channel region, wherein the channel region may or may not be on a sidewall, wherein the AlGaN or InGaN is re-grown on an a- or m-plane or semi-polar sidewall of a GaN feature, resulting in enhanced hole mobility in the vertical direction.

44. A device of example 42 and 43, wherein the gallium nitride in example 42 comprises the drift region of the device and example 43 comprises the channel region of the device.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

Fig. 1. Schematic valence-band structures of wurtzite GaN (a) without a strain, (b) with a biaxial strain, and (c) with a uniaxial strain. Here, the effect of the weak spin-orbit coupling is neglected. In the case of significant biaxial strain the split off band energies can be substantially affected. (d) Directions of the strains in the *c* plane. From [1].

Fig. 2. Reciprocal space maps recorded around the asymmetric (1124) reflection for (a) the nanopillar array fabricated from a 8 period MQW wafer with 9.2 nm-thick GaN barriers and 2.7 nm-thick In0.25Ga0.75 N wells, (a) the nanostripe array fabricated from the same wafer with an angle of 90° between the stripes and the X-ray scattering plane. The RSM (b) was taken from the same nanostripe array around the asymmetric (10-15) reflection with the X-ray scattering plane parallel to the stripes (rlu: reciprocal lattice units), from [2]. (c) TEM image of nanostripe array, From reference [3]. (d) Angular resolved PL spectra recorded from nanostripe arrays fabricated from 5 period MQW fins, from reference [2].

Fig. 3. (a) Schematic of the proposed D-mode device structure, (b) fin design for fins along the [11-20] direction, for example. Conversely, the fins can also be fabricated along the orthogonal [1-100] direction. The GaN {(In,Ga)N} channel on (Al,Ga)N {GaN} is under compression along the fin and light hole current flow occurs along the fin (case: a (channel) > a(base of fin), and (c) final device layout.

Fig. 3 (d) Left: schematic of device structure for case that in plane lattice constant *a* (channel= material C) > *a*(base of fin= material A), where a is lattice constant. Conversely, the fins can also be fabricated along the orthogonal [1-100] direction. Light hole current flow occurs perpendicular to the fin. Right: final device layout.

Fig. 3e illustrates a device according to another example.

Fig. 3f. Example structures using porous GaN to aid the relaxation or partial relaxation of material B perpendicular to the fin direction to achieve uniaxial strain. Parallel to the fin along the long axis of the fin material B remains strained to material A or relaxes less compared to the direction perpendicular to the long axis of the fin. Thereby material B can be composed of multiple layers. Using porous GaN, the fin dimensions can be in the micrometer range. a is lattice constant.

Fig. 4. Schematic showing a p-FET fabricated along the direction of low effective mass holes. The anisotropy in hole effective mass is induced by uniaxial strain existed along the fin.

Fig. 5. Schematic of p-FET and n-FET implemented on the same substrate, both along the fin direction.

Fig. 6. p-FET and n-FET structures showing use of stressor and p+ regrowth to induce uniaxial compression to the p-channel.

Fig. 7. Schematic of a BJT/HBT using uniaxial tensile strain to enhance base characteristics, showing the fin in the direction parallel to the direction of the uniaxial tensile strain. Base contacts are formed in the direction perpendicular to the fin

Fig. 8. Schematic of BJT/HBT using uniaxial compressive strain to enhance base characteristics.

Fig.. 9. Output power vs Frequency.

Fig. 10. W-Band output power density of various GaN device technologies over time. Traditional AlGaN/GaN HEMTs have saturated around 2 W/mm while N-polar GaN has recently demonstrated 7.94 W/mm.

Fig. 11. Device Cross-section schematic of the N-polar GaN Deep Recess MISHEMT structure. Key properties of the device structure are highlighted.

Fig. 12. Calculated conduction band effective mass for strained and bulk (strain-free) InGaAs as a function of InAs mole fraction X of In.

Fig. 13. Electron mobility in $In_{0.2}Ga_{0.8}N$ film sandwiched between two GaN layers. InGaN-2 and InGaN-1 are electron mobility calculated assuming $m^* = 0.04$

and m* = 0.07 for InN, respectively. From Z. Yarar et al, Journal of ELECTRONIC MATERIALS, Vol. 36, No. 10, 2007

Fig. 14. Bandgap of InGaN versus In composition. From E. Sakalauskas et al., Phys. Stat. Sol. B 249 (2012) 485.

Fig. 15. Schematic of the proposed structure.

Fig. 16. Left: Schematic of stripe patterned InGaN/GaN MQW, right: reciprocal space map of stripe patterned MQW sample taken around the asymmetric $(11\bar{2}4)$ reflection with x-ray scattering plane perpendicular to the stripe direction showing relaxation of the MQW.

Fig 17: Illustration of variation in contact resistance for finite-length contacts, using best reported values for GaN HEMTs [HRL], [Sansaptak]. Includes 0.026 Ω-mm n+ to 2DEG interfacial contact resistance for Ga-polar [HRL].

Fig. 18. Cross-sectional schematic of strained InGaN layer on GaN

Fig. 19. Post growth reciprocal space map for fully strained InGaN layer sample. The alignment of GaN peak (above) and InGaN peak (below) shows the fully strained state of the InGaN layer.

Fig. 20. Hole conductivity as a function of temperature for planar biaxially strained InGaN layer. The increase in R_{SH} can be attributed to the freezing of holes in the bulk InGaN layer with reduced temperatures. The presence of 2-DHG at the InGaN/GaN interface results in the observance of reasonable sheet resistance values at 80K.

Fig. 21. (Left) Uniaxially strained layers (fins) demonstrated lower R_{SH} (~25-50% lower) compared to planar biaxially strained layers at the room temperature. (Right) However, the difference in the R_{SH} was almost negligible at 80 K. These results indicate that at the InGaN/GaN interface strain-relaxation was not achieved. These results demonstrate the use of strain engineering (*for the first time*) to improve the transport properties of holes by changing the valence band-ordering in III-Nitrides.

Fig. 22-30. Implementations using nonpolar/semipolar orientations. Illustrations are for a-plane material, as example. Similar structures can be fabricated using m-plane material, exchanging the [11-20] and [1-100] axis.

Fig. 22 plots valence band structure under strained conditions of a-plane bulk In0.2Ga0.8N.

Fig. 23 is a cross sectional schematic of a transistor device on a-plane according to a first example.

Fig. 24 is a cross sectional schematic of a transistor device on a-plane according to a second example.

Fig. 25A is a cross sectional schematic of a transistor device on a-plane according to a third example.

Fig. 25B is a cross sectional schematic of a transistor device on a-plane according to a fourth example.

Fig. 26 is a cross sectional schematic of a transistor device on a-plane according to a fifth example.

Fig. 27 is a cross sectional schematic of a device on 0001 or 000-1 GaN.

Fig. 28 is a Transmission Electron Microscope (TEM) image of a device and schematic of a device.

Fig. 29 is a schematic of a transistor device.

Fig. 30 illustrates cross-sectional schematics of transistor structures.

Fig. 31A, 31B, and 31C illustrate devices on semi-insulating GaN, wherein Fig. 31C illustrates a device according to another example on m-plane GaN.

Fig. 32. Example structures with biaxial tensile strain in material B to allow light hole transport in the vertical direction, as the a-lattice constant of relaxed material A is larger than that of relaxed material B. A porous group III-nitride layer, e.g. porous GaN can be used to aid the fabrication of layer A larger a-lattice constant compared to layer B, where material A could be InGaN and material B could be GaN. a is lattice constant.

Fig. 33 illustrates an optoelectronic device.

Fig. 34 illustrates an optoelectronic device including a pixel.

Fig. 35 illustrates an optoelectronic device according to another example.

Fig. 36 is a flowchart illustrating a method of making a device.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Technical Description

III-N based structures are widely used for photonic and electronic devices. The state-of-the-art devices are based on either lattice-matched or biaxially strained wurtzite III-N materials. Such materials use in-plane electron and hole material properties that are substantially similar to bulk wurtzite materials. This present disclosure describes structures and methods on a class of materials wherein either the electron or the hole or both materials properties are modified through the appropriate implementation of strain to modify electronic and photonic device performance and enable a new class of circuit embodiments.

PART I: Electronic Devices

P-type channel devices are limited by the transport properties of the p channel. This is dominantly dependent on the effective mass of the holes; the lower the effective mass the higher the hole mobility. In one example, we describe a structure for and method to make high performance p-MOSFETs in GaN. The method and structure is designed using first principles band structure calculations of the anisotropy of the effective mass of holes in the GaN system, as shown in Fig. 1a [1].

The valence band of unstrained GaN exhibits degeneracy of the light hole and heavy hole bands resulting in a large average hole effective mass and therefore a low hole mobility. The situation remains largely unchanged on application of biaxial strain as shown in Fig. 1b. However, as shown in Fig. 1c and 1d, under the application of uniaxial compressive strain in the y direction, the energy of the light hole band energy rises and there is a marked anisotropy, with a very light hole effective mass available in the k_y direction. The preferred orientation of the pFET channel is in the y-direction. Conversely the uniaxial strain can be applied in the x direction and a very light hole effective mass will be available in the k_x direction and the preferred orientation of the pFET channel will be the x direction. This enables, in one embodiment, the source drain spacing required to hold voltage in a power pFET to exist in the direction of the low hole effective mass. In another embodiment, the source drain spacing could be such that the FET is self-aligned as in conventional digital MOSFETs. The range of effective masses in GaN and AlN are shown in table I. The light hole effective mass, m_{lh}, is predicted to be in the range $0.14m_o$, which is even lower than the electron effective mass. Either a strained fin technology or strained stressor and source drain regrowths, when applicable, can be used to implement uniaxial strain as is described in the following sections. The application of uniaxial strain to get high performance p-FETs is an exciting pathway of developing complementary GaN technology.

In addition, vertical light hole effective mass to enhance vertical hole transport (perpendicular to the c plane as an example) can be accessed by using biaxial strain in the target material. As an example, tensile strain in a III-N target material can be generated by growing a material with a smaller lattice constant on a larger lattice constant substrate (for example AlGaN on GaN or GaN on InGaN). The templates can also be generated using commercially available materials employing porous GaN as a compliant layer

Table I. Electron and hole effective masses (m_0) and crystal-field and spin-orbit splitting energies (mryd) of bulk wurtzite GaN and AlN. m_e, m_{hh} , m_{lh} , and m_{ch} denote electron, heavy-hole, light-hole, and crystal-field split-off hole effective masses, respectively. The superscripts II and ⊥, stand for the k_z direction and the k_x direction, respectively. D_{cr} and D_{so} represent crystal-field and spin-orbit splitting energies, respectively. From ref. [5]

	$m_e^{\parallel}$	$m_e^{\perp}$	$m_{hh}^{\parallel}$	$m_{lh}^{\parallel}$	$m_{ch}^{\parallel}$	$m_{hh}^{\perp}$	$m_{lh}^{\perp}$	$m_{ch}^{\perp}$	Δ_{cr}	Δ_{so}
GaN	0.20	0.18	1.76	1.76	0.16	1.61	0.14	1.04	5.3	1.2
AlN	0.33	0.25	3.53	3.53	0.25	10.42	0.24	3.81	−4.3	1.5

A. Example methods to generate uniaxial strain

1. First Example Method

The present disclosure demonstrates uniaxially strained quantum wells by using strain relaxation in fin geometries as seen for an InGaN/GaN Multi Quantum Well (MQW) fin in Fig. 2 [2, 3, 4]. While the MQW fin partially relaxes in the direction perpendicular to the stripe, it is fully strained parallel to the stripe direction. The etched stripe arrays were of high crystalline quality and exhibited intense photoluminescence as illustrated in Fig. 2d.

When the fin structures are composed in part of a porous group-III nitride material, such as porous GaN, for example, or are placed on top of a porous group-III nitride material, relaxation or partial relaxation can be achieved over larger dimensions easing the fabrication process of the fin based devices.

This is the preferred approach to create strained GaN channels for the proposed p-MOSFETs with the ability to hold substantial voltage (greater than 2V) between source/gate and drain. To generate the necessary compressive strain in the GaN channel along the stripe direction, the bulk of the stripes may be composed of $Al_xGa_{1-x}N$, and the amount of strain can be tailored by the specific Al mole fraction x.

The epitaxial layer structures can be grown by MOCVD or MBE or any other technique suitable to deposit III-N materials. The preferred embodiment shown here is based on the metal-polar orientation of the III-N system. The device shown is one in which a substantial voltage (>2V) is held in the source drain direction when the

device is in the off-state. On the AlGaN base layers GaN channel, p-GaN:Mg and oxide dielectric layers can be deposited for a metal -polar device design (Fig. 3a). For ease of presentation the structure shown is a depletion mode device and represents the voltage bearing section of the p-FET. The oxide dielectric layers help to reduce gate leakage and thereby enhance the device breakdown performance. A normally-off gate module is achieved by etching the doped region under the gate and applying the MOS gate structure. The dielectrics can be deposited by any suitable technique including, but not limited to, using an MOCVD oxide growth process for the deposition of Al_2O_3 and Al_xSi_yO (and Si_3N_4) dielectric materials [5,6].

2. Second Method

The second method is to use either strained source-drain contact regions or stressor films or both to induce the strain in the desired region. This is best applied to the self-aligned structures described in the device structures below and also simplified by the use of materials that include porous GaN in the material stack.

3. Porous III-Nitride example

Fig. 3F illustrates example structures using porous GaN to aid the relaxation or partial relaxation of material B perpendicular to the fin direction to achieve uniaxial strain. Parallel to the fin along the long axis of the fin material B remains strained to material A or relaxes less compared to the direction perpendicular to the long axis of the fin. Thereby material B can be composed of multiple layers. Using porous GaN, the fin dimensions can be in the micrometer range.

4. Example Electronic Device structures

Fig. 3b shows and example wherein the Channel comprising GaN has a lattice constant larger than the base material (e.g., AlGaN) so that the channel is under compressive strain. In another example, the structure is a uniaxial fin structure as shown in Fig. 3c where the direction of transport is in the $[1\bar{1}20]$ or *a*-direction and

the direction of relaxation is in the $[1\bar{1}00]$ or *m*-direction (for example). This is for uniaxial compressive strain generated by GaN channels grown on AlGaN buffer layers for the embodiment shown.

Similarly, in the bulk of the stripe can be composed of GaN and the channel of InGaN, or any nitride material where the in-plane lattice constant of the bulk of the stripe is smaller than the in-plane lattice constant of the channel material. Thereby for epitaxial layers grown in the c or –c-directions, the stripes can run parallel to the [11-20] or [1-100] direction for light hole current flow to occur along the corresponding stripe direction in which the channel material is still compressively strained.

The channel is in general made of III-N materials which may be of uniform composition, graded or stepped composition, or any combination thereof. The buffer layers can also be of uniform composition, graded or stepped composition, or any combination thereof. The source drain spacing can be in the direction of low effective mass holes and the number of fins can be scaled to enhance device current requirements. The device structure shown has spacing between the gate and the drain to hold significant voltage.

Similarly, light holes form in fins composed of a group-III nitride material C which under relaxed conditions has an in-plane lattice constant smaller than the base material A. In this case, if the fins propagate along the [11-20] direction the light hole current flows perpendicular to the fins in the [1-100] directions. Here materials A and C could be, for example, GaN and (Al,Ga)N, respectively.

In one example, the light holes form in fins made from group-III nitride materials B grown on a base layer A in the c or (0001) or –c or (000-1) direction, when the relaxed in-plane lattice constant *a* of the base material A is smaller than that of the relaxed material B which is a constituent of the fins as illustrated in Fig. 3d. In the fin structure , material B is strained to material A along the fins, but B relaxes perpendicular to the fin. Thereby the fin propagation direction is [1-100] with a light hole current flow in devices, for example p-FETs, along the [1-100] direction of the fin. Here materials A and B could be GaN and InGaN, respectively. Alternately

materials A and B could be AlN or AlGaN and GaN, respectively, with p-FET structure examples.

A self-aligned p-FET structure such as shown in Fig. 4 can also be similarly fabricated. If the dimensions of the scaled gate are small (200nm) the p-type source and drain regions may incorporate strained materials which can further modify the strain in the channel. In one embodiment the structure can be such that all the compressive strain in the channel can be exerted by the source and drain regions. In this instance the need to form a fin to create the uniaxial is ameliorated and the buffer design can be altered.

The impact of the stressor can be enhanced by placing the channel material on a porous group –III nitride material such as porous GaN, taking advantage of the reduced stiffness of porous materials. Similarly, incorporating porous group-III nitride material allows stressing the material over larger dimensions, eliminating the need for employing submicron structures.

5. Complementary integrated circuits (CMOS) using III-N materials

CMOS architectures are by far the dominant architecture in Si today. CMOS in GaN has not been attractive because of the limitations of the p-MOSFET in GaN. Using the light hole channels as described herein will enable a high-performance GaN p-MOSFET. This will allow CMOS architectures where both the n-type and p-type devices are collocated on the same substrate. One embodiment is shown in Fig. 5. The n-FET and p-FET devices can be both oriented in the same direction on the fin as shown in this figure. This is because although the hole effective mass is reduced in the fin direction (as explained earlier in Fig. 4), the electron effective mass remains substantially the same and hence the n-FET performance will be similar to the conventional GaN n-FETs. In Fig. 6 the devices can be co-located on a wafer where the strain is applied only to the p-channel device using stressors generated either with source drain materials or by dielectric stressors or both. The impact of the stressor can again be enhanced by incorporating porous GaN into the structure.

6. Bipolar transistors:

Uniaxial tensile strain in the x direction causes the hole effective mass to reduce in the y-direction as in ref [1]. Similarly, tensile strain in the y direction results in a lowering of the effective mass for hole transport in the x-direction (e.g. light hole transport occurs in the direction orthogonal to the direction of the uniaxial tensile strain). Using this principle, we propose a device shown in Fig. 7, wherein the base contacts are in the short direction of the fin when the base is placed under uniaxial tensile strain. The base current flows in a direction perpendicular to the fin. In this case, the III-N buffer layer on which the active materials are grown could be of a larger lattice constant such as InGaN or another material to induce tensile strain on the overlying materials.

Uniaxial compressive strain can also be employed to enhance III-N-based bipolar transistors as shown in Fig. 8. In this embodiment, a grid like structure is used with a two-level metal scheme. Level 1 metal interconnects the emitter layers and level 2 metal interconnects the base layers. The collector metal here is assumed at the back of the wafer, otherwise a third level interconnect (level 3) can be used to interconnect the collector regions. The base current is in the direction of the fin. In this case, the III-N buffer layer on which the active materials will be grown could be of a smaller lattice constant such as AlGaN or another material to induce tensile strain on the overlying materials.

B. Enhanced relaxation of materials and device structures based on the same

1. Introduction

The intrinsic material properties of GaN, with its combination of large critical electric field and high electron mobility, provide an ideal platform to fabricate devices for high power millimeter-wave power amplifiers. As shown in Fig. 9, traditional Ga-polar AlGaN/GaN devices have demonstrated superior power performance over a

wide frequency range when compared to alternative device technologies. However, when examining reported device performance in W-band over the past decade, one observes that the power density of traditional GaN HEMTs has been saturated at 2 W/mm (Fig. 10) with power-added efficiencies (PAE) limited to about 25%. To break this barrier a technology had to be developed that simultaneously provided high current, high breakdown voltage and low dispersion without paying the penalty of reduced gain caused by the capacitance of field plates; a very high price to pay at mm-waves. The deep recessed N-polar AlGaN/GaN structure grown on miscut SiC shown in Fig. 11 succeeded because of it provided low channel resistance and low dispersion because of the GaN cap and a high gate breakdown because of the reverse polarization field of the AlGaN under the gate. This has resulted in a power density of 7.94 W/mm at 94 GHz with a PAE of 26.9%. .

2. Example

The present disclosure describes how to increase the electron velocity in the channel by using ***relaxed InGaN as the channel material*** which provides a reduced electron effective mass, critical in reducing electron scattering and enhancing electron velocity. Relaxation of the InGaN channel is required since a fully strained InGaN channel does not provide an effective mass commensurate with the In mole fraction because the lattice constant and hence the Brillouin Zone and conduction band curvature of the InGaN is more akin to GaN, as previously observed for strained and relaxed InGaAs (Fig. 12) [7]. The 2DEG mobility in an $In_{0.2}Ga_{0.8}N$ channel, as shown in Fig. 13 has been as predicted to be more than 5000 cm^2/Vs as calculated by Yarar et al [11]. This composition is attractive as the bandgap of InGaN is still around 2.5ev (Fig. 14) which enables high frequency operation with high voltage operation along with high current . At one limit of composition electron mobility values as high as 3570 cm^2/Vs were measured for InN films with an electron carrier density of 1.5×10^{17} cm^{-3} compared to values around 600 cm^2/Vs for GaN films with similar carrier densities [8]. We achieve the InGaN relaxation in a unique manner by

using Fin geometries of nominal 200 nm width which allow an N-polar InGaN layer or GaN/InGaN/GaN stack to relax to their average lattice constant after patterning. The proposed structure is shown in Fig. 15 using the N-polar orientation of the III-N material as the preferred orientation. By relaxing the InGaN in the direction of electron transport, the electron effective mass is determined by the relaxed lattice constant. We have shown the effectiveness of patterning to relax Ga-polar nano-stripes of InGaN/GaN multi quantum well structures using X-ray analysis (Fig. 16) [9-10]. This technique is applicable to all materials (beyond III-N materials) in all polarities and crystal planes.

In contrast to a FinFET, the channel in this device the electron transport direction is perpendicular to the fin direction. For small fin dimensions ohmic contacts with sub-micron length are required. For these contacts an extremely low specific contact resistivity (ρ_C) is needed. In the preferred embodiment using N-polar III-N orientation, record values of GaN HEMT contact resistance (R_C) of 27 Ω-μm, corresponding to ρ_C of 2.3 Ω-μm^2, have already been demonstrated in a full N-polar GaN HEMT process. It utilized a regrown structure with the GaN channel graded to $In_{0.63}Ga_{0.37}N$ capped with InN. The InN has been shown to exhibit surface electron accumulation of ~10^{13} cm^{-2} density, ideal for low resistivity contacts to metal. The graded InGaN was used to minimize the barrier due to conduction band discontinuity between the channel and InN. For N-polar this graded region also creates a positive polarization charge which then gives rise to a 3-dimensional electron gas (3DEG), which reduces the barrier at the InN/$In_{0.63}Ga_{0.37}N$ interface and reduces sheet resistance of the contact layer. The second unique benefit of the N-polar orientation is that the HEMT's 2DEG is induced from the back-barrier, so contact to the 2DEG is formed over the entire contact area, and not merely at the edge of the ohmic region (Fig. 17). Appropriate contact materials will simultaneously reduce contact resistance and preferably enhance the relaxation of the channel. While the uniaxial strain conditions described in the examples hold for epitaxial layer structure grown in the

(0001) or c-direction as well as in the (000-1) or –c-direction, other strain conditions can be used in devices grown in non-c-plane directions.

3. Circuit Modules:

Exemplary n channel and p-channel devices can be implemented in digital CMOS architectures, analog circuits such as push-pull amplifiers, wideband amplifiers and mixed signal architectures.

4. Results

In our work, *for the first time*, we experimentally demonstrate the improvement in hole conductivity under the application of uniaxial compressive strain in c-plane III-Nitrides. We obtained approximately 25-50% lower sheet resistance (R_{SH}) extracted from TLM measurements at room temperature (295 K) with uniaxially strained InGaN layers compared to planar biaxially strained InGaN layers.

Fully strained (as observed from reciprocal space map) 300nm thick, Mg (3 x 10^{19} cm^{-3}) doped $In_{0.1}Ga_{0.9}N$ layers were grown on bulk GaN substrates (Fig.-1 and Fig.-2). The R_{SH} of planar biaxially fully strained InGaN layer increased from 16 kΩ/□ (at 295 K) to 36 kΩ/□ (at 80 K) at low temperature (Fig. 19). The increase in R_{SH} can be attributed to the freezing of holes at low temperature in the bulk p-InGaN layer, however, the presence of 2-DHG at the InGaN/GaN interface results in reasonable R_{SH} at 80 K (~36 kΩ/□).

Fin structures were fabricated with fin-widths ranging from 100nm to 500nm to obtain uniaxial compressive strain in the longitudinal direction as the fin relaxes in the transverse direction. Uniaxially strained layers (fins) demonstrated lower R_{SH} (~25-50% lower) compared to planar biaxially strained layers at the room temperature (Fig. 22). However, the difference in the R_{SH} was almost negligible with lower temperature (80 K). These results indicate that at the InGaN/GaN interface, strain-relaxation was not achieved in the transverse direction.

These results demonstrate the use of strain engineering (*for the first time*) to improve the transport properties of holes by changing the valence band-ordering in III-Nitrides.

C. Non-polar/Semi-polar Examples

Unisotropic strain also exists in planar layer structure grown in the non-polar a- and m- directions and semi-polar directions of the nitride wurtzite crystal, leading to a splitting of the valence bands into heavy hole and light hole bands. For example, in optoelectronic devices based on m-plane InGaN/GaN heterostructures, this leads to polarized light emission. In these the heavy hole band moves in the highest energy position among the valence bands. However, when a group-III nitride material B with a larger lattice constant than the base material A is grown strained on top of material A in the *a*- or [11-20]] direction, on *a*-plane substrates, for example, the light hole band moves again in the highest position among the valence bands and allows light hole current flow in the [1-100] direction (Fig.22). Conversely, when material B with a larger lattice constant than the base material A is grown in the [1-100] or m-direction on m-plane substrate, the light hole band moves in the highest position along the [11-20] direction. Materials A and B can, for example, again be GaN and InGaN, respectively, or AlN or AlGaN and GaN, respectively.

Utilizing planar a-plane GaN or AlN substrates, planar p-FETs are fabricated with source and drain contacts aligned in such a way that the current flows along [1-100]. Examples for planar *a*- or m-plane InGaN/GaN and GaN/(Al,Ga)N p-FETs are illustrated in Figs. 23 and 24.

Thereby in one example, a p-type Mg doped $In_xGa_{1-x}N$ layer will be deposited on a *a*-plane GaN substrate which can be of any conductivity, but preferentially semi-insulating.

Gate, source and drain p-type contacts are then fabricated in the preferred direction for MESFETs. To improve the contact formation a p++-InGaN layer can be implemented for contact formation, and re-grown p-type InGaN contacts can be used

as illustrated in Fig. 25. Thereby the In composition in the re-grown contacts and/or in the p++ InGaN contact layer can be higher than in the InGaN p-channel layer. In addition a dielectric such as aluminum oxide or silicon aluminum oxide can be utilized under the gate.

Instead of a single p-type Mg doped $In_xGa_{1-x}N$ layer thin Mg doped and undoped $In_xGa_{1-x}N$ layers can be alternated. Thereby the Mg doped $In_xGa_{1-x}N$ layers can be of lower In composition x compared to the undoped $In_yGa_{1-y}N$ layers, and the number of doped and undoped layers can vary (Fig. 26)

The $In_xGa_{1-x}N$ and $In_yGa_{1-y}N$ layers can be arranged in such a way, that one or more a two dimensional hole gas channels form.

The doped layers can be formed through delta doping.

The *a*- or m-InGaN/GaN p-FET can be integrated with n-FETs, for example via selective area deposition.

Instead of the planar *a*- or m-plane p-FET structures, the p-FETs can be grown on the *a*-plane or (11-20) sidewalls (or m-plane or (1-100) sidewalls) of fins or ridge structures fabricated on (0001) or (000-1) GaN base layers. *C*-plane GaN is available in much larger diameters and the fin or ridge structures also allow the integration of p-FETs with n- FETs. In this case the above discussed planar *a*-plane heterostructures are deposited on the *a*-plane sidewalls of fins along the [11-20] direction as shown in Fig. 27.

Using p-InGaN/GaN structures as example, the InGaN can be forced to grow on the a-plane sidewalls by masking the (0001) or (000-1) surface areas prior to InGaN deposition. In the case of (000-1) fins, the growth rate in the a-direction is naturally higher compared to the one the (000-1) plane, similar to the observations for the growth on the m-plane sidewalls as illustrated in Fig. 28. Thereby prior to the InGaN or p-InGaN layers a GaN or other suitable interlayer can be deposited. P-FETs can then be fabricated by wrapping the fins with the source, drain, and gate contacts as illustrated in Fig. 29. Alternately, contacts can be made to each side of the fins or ridges individually.

In addition, the properties of compressively strained materials on the *a*-plane orientation can be taken advantage of, for example, for the above discussed strained fin structures. Here an improved device performance is expected when the p-contacts are made of p-InGaN:Mg at the end of the fin structures, where the fins propagate along the [1-100] or *m*-direction and p-InGaN contacts are grown on the (11-20) sidewalls of the fins. (Fig. 30) For all applications, all directions can be rotated by 90 degrees.

The planar p-FETs and the p-FET fins can be integrated with planar n-FETs or fin n-FETs for CMOS architectures, which are by far the dominant architecture in Si today. CMOS in GaN has not been attractive because of the limitations of the p-MOSFET in GaN. Using the light hole channels as described herein enables a high-performance GaN p-MOSFET. This allows CMOS architectures where both the n-type and p-type devices are collocated on the same substrate.

The epitaxial layer structures can be grown by MOCVD or MBE or any other technique suitable to deposit III-N or (B,Al,Ga,In)N materials. The device shown is one in which a substantial voltage (>2V) is held in the source drain direction when the device is in the off-state. For ease of presentation the structures shown in Figs.5 to 8 are a depletion mode devices and represent the voltage bearing section of the p-FET. The oxide dielectric layers help to reduce gate leakage and thereby enhance the device breakdown performance. A normally-off gate module is achieved by etching the doped region under the gate and applying the MOS gate structure, for example, as illustrated in Fig. 13. The dielectric material can be deposited by any suitable technique including but not limited to using an MOCVD oxide growth process for the deposition of Al_2O_3 and Al_xSi_yO (and Si_3N_4) dielectric materials. Thereby any dielectric material can be used, which can be deposited using any suitable technique.

For all applications, regrown InGaN:Mg or GaN:Mg/InGaN:Mg contacts may be used to minimize the contact resistance.

In all described cases the preferred orientation of the pFET channel is in the direction in which the very light hole effective mass available This enables, in one embodiment, the source drain spacing required to hold voltage in a power pFET to exist in the direction of the low hole effective mass. In another embodiment, the source drain spacing could be such that the FET is self-aligned as in conventional digital MOSFETs. The range of effective masses in GaN and AlN are shown in table I. The light hole effective mass, m_{lh}, is predicted to be in the range $0.14m_o$, which is even lower than the electron effective mass. We can use either a strained planar technology or strained fin structures, or strained heterostructures grown on the sidewalls of fins or ridges, or use these advantages for source drain regrowths, when applicable. The application of anisotropic in-plane strain to get high performance p-FETs is an exciting pathway of developing complementary GaN technology.

D. Examples for light hole creation using biaxial tensile strain

In addition to uniaxial strain, light holes transport can be achieved under biaxial tensile strain in the a-m-plane of the hexagonal lattice when the hole transport occurs perpendicular to the plane of the biaxial strain, along the c-axis. Biaxial tensile strain is created in heterostructures where a layer composed of material B is placed on material A, where the a-lattice constant of material B is larger than that of material A. Example structures are GaN placed on top of InGaN or AlGaN placed on top of GaN (Fig. 32).

Thereby a porous group-III nitride material, e.g. porous GaN, can aid in the fabrication of relaxed (B,Al,Ga,In)N material, for example InGaN.

In a further layout the channel region which may or may not be on a sidewall, the AlGaN or InGaN is re-grown on the a- or m-plane or semi-polar sidewall of a GaN feature resulting in enhanced hole mobility in the vertical direction.

Advantages and Improvements

Illustrated herein are high performance complementary solution to power management using GaN based materials. One key to the complementary solution is to make high performance p-MOSFETs in GaN. We will use the pathway shown by first principles band structure calculations of the anisotropy of the effective mass of holes in the GaN system as shown in Fig. 1. The valence band of unstrained GaN exhibits degeneracy of the light hole and heavy hole bands resulting in a large average hole effective mass and therefore a low hole mobility (predicted to be ~100cm2V-1s-1 and measured to be less than 30 cm2V-1s-1 in MOSFETs). Besides the metal polar device structures, complementary N-polar structures will be evaluated as well.

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PART II: Impact of strain on enhancing the performance of III-nitride photonic devices such as lasers and light emitting diodes

III-N based structures are widely used for photonic and electronic devices. The state-of-the-art devices are based on either lattice-matched or biaxially strained wurtzite 111-N materials. Such materials use in plane electron and hole material properties that are substantially similar to bulk wurtzite materials. This patent teaches structures and methods on a class of materials wherein either the electron or the hole or both materials properties are modified through the implementation of strain to modify electronic and photonic device performance and enable a new class of circuit embodiments.

A critical parameter limiting the performance of today's nitride based optoelectronic devices, in particular lasers, is the low hole concentration and low hole mobility in p-type III-nitride layers,[caused by the high electronic hole mass and resulting low hole mobility. In this section, we describe structure(s) for and method(s) to make high performance optoelectronic devices in GaN. In one or more embodiments, we use the pathway revealed by first principles band structure calculations of the anisotropy of the effective mass of holes in the GaN system as discussed herein. The valence band of

unstrained GaN exhibits degeneracy of the light hole and heavy hole bands resulting in a large average hole effective mass and therefore a low hole mobility. The situation remains largely unchanged on application of biaxial strain. However, as shown in Figs. 1e and 1d, under the application of uniaxial compressive strain in the y direction, the energy of the light hole band energy rises and there is a marked anisotropy, with a very light hole effective mass available in the ky direction. To take advantage of the light hole mass the preferred orientation of for hole conduction is in the y-direction.

Example Photonic Device Structures

Fig. 33 illustrates a structure wherein light holes can reduce the threshold current in lasers and increase the modulation speed of both group III nitride lasers and LEDs.

In this first approach the dimensions of the laser stripe geometry are tuned in such a way that the geometry allows relaxation of the p-GaN layer perpendicular to the stripe direction while maintaining its strained nature in the parallel direction so that light holes will form in the p-GaN layers. While the schematic shows an edge emitting laser, the invention can also be applied to LEDs and VCELs.

In a second approach either strained regrown III-nitrides or stressor films or both are used to induce the strain in the desired region. This second approach is illustrated for an individual pixel in a pixelated LED structure in Fig. 34. The regrown InGaN sides create compressive strain in the GaN layers perpendicular to the stripe, resulting in light hole formation in the enclosed layers and additional improved hole transport occurring along the stripe direction. To prevent escape of carriers into the InGaN side regions, a thin barrier layer can be grown prior to the deposition of the InGaN side regions (not shown in the Fig. 34).

In an alternate layout the stripe direction can be rotated by 90 degrees as illustrated in Fig. 35. Here uniaxial tension perpendicular to stripe is induced by regrown p-AlGaN, generating light holes in all enclosed layers.

This method can be used for all photonic group-III nitride photonic devices. While the uniaxial strain conditions described in the examples hold for epitaxial layer structure grown in the (0001) or c-direction as well as in the (000-1) or -c-direction, other strain conditions can be used in devices grown in non-c-plane directions

Part III: Process Steps

Fig. 36 is a flowchart illustrating a method of making a device.

Block 3600 represents providing a substrate.

Block 3602 represents depositing or forming a device on the substrate or layer, the device including III-nitride material strained along a first direction and at least partially relaxed along a direction perpendicular to the first direction. In one or more examples, the III-nitride is on or above a substrate or layer comprising porous III-nitride, and the forming comprises patterning the III-nitride into ridge or fin structures, wherein the porous III-nitride allows relaxation or partial relaxation of the fin structure perpendicular to the fin or the short axis while the fin material remains strained or relaxes less in the direction along the fin or the long direction resulting in uniaxial strain in the fin structure.

Block 3604 represents the end result, a device. Examples include, but are not limited to, the following.

1. A device 300 (referring to Fig. 3e and Fig. 3f), comprising:

III-nitride material (layer B) strained along a first direction 302 and at least partially relaxed along a second direction 304 perpendicular to the first direction.

2. The device of example 1, wherein the III-nitride is on or above porous III-nitride (layer A) wherein the porous III-nitride and/or the III-nitride is patterned into ridge or fin structures 306, wherein the porous III-nitride allows relaxation or partial relaxation of the fin structure perpendicular to the fin or the short axis 304 while the fin material remains strained or relaxes less in the direction 302 along the fin or the long direction 302 resulting in uniaxial strain in the fin structure (see Fig. 3f).

3. The device of example 2, wherein the porous III-nitride includes etched pores.

4. The device of example 2 or example 3, wherein the porous III-nitride comprises gallium nitride.

5. The device of example 1, wherein the device is a field effect transistor (FET), e.g., as illustrated in Fig. 3(a) or Fig. 3(c) including:

a stripe 310 comprising the III-nitride material 312, wherein:

the III-nitride material 312 is strained along the first direction comprising a long axis of the stripe and at least partially relaxed along the second direction comprising a direction (short axis) perpendicular to the long axis ;

the III-nitride material includes a channel layer;

a source contact (S) comprising first metal on the stripe making ohmic contact to the channel;

a drain contact (D) comprising second metal on the stripe making ohmic contact to the channel;

a gate contact (G) on the stripe between the source contact and the drain contact, the gate contact controlling flow of current along a direction of the long axis or short axis through the channel and between the source contact and the drain contact.

6. The device of example 5, wherein:

the channel comprises gallium and/or indium and/or aluminum (and/or boron)

the III-nitride material comprises the channel layer on a layer including gallium and/or aluminum and/or indium and/or boron,

a thickness of the layer comprising gallium and/or aluminum, and/or indium is more than 50% of a thickness of the stripe,

an composition is selected so as to obtain a desired strain in the channel along the long axis.

7. The device of example 5, e.g., as illustrated in Fig. 5 or Fig. 6 wherein:

the III-nitride material further includes a source region (p+ in Fig. 5) and a drain region (p+ in Fig. 5),

the source region is in physical contact with the channel layer between the source contact and the channel layer,

the drain region is in physical contact with the channel layer between the drain contact and the channel layer, and

the source region and the drain region have a lattice constant different than a lattice constant of channel so as to induce the strain in the channel layer along the long axis.

8. The device of example 7, wherein the source region and the drain region comprise gallium and/or aluminum, and/or indium (e.g., InGaN channel case on GaN).

9. The device of any of the examples 5-8, wherein:

the current between the source contact and the drain contact is along the long axis that is a crystallographic a- or m-direction of the III-nitride,

the short axis direction perpendicular to the long axis is a crystallographic m- or a- direction of the III-nitride, respectively.

the top surface of the stripe has a polar (0001) or (000-1) orientation, and

the channel has a lattice constant larger than the underlying III-nitride material.

10. The device of any of the examples 5-8, wherein:

the current between the source contact and the drain contact is along the short axis that is a crystallographic a- or m-direction of the III-nitride,

the long axis direction perpendicular to the short axis is a crystallographic a- or m-direction of the III-nitride,

the top surface of the stripe has a polar (0001) or (000-1) orientation, and

the channel has a lattice constant smaller than the underlying III-nitride material.

11. The device of any of the examples 5-8, wherein:

the current between the source contact and the drain contact is along the short axis that is a crystallographic m-direction of the III-nitride,

the long axis direction perpendicular to the short axis is a crystallographic c-direction of the III-nitride, and

the top surface of the stripe has a nonpolar a- or m-plane orientation.

12. The device of any of the examples 5-9, wherein the FET comprises a p-type FET conducting the current comprising holes and the strain along the long axis is uniaxial compressive strain.

13. A device comprising a CMOS device (e.g., as illustrated in Fig. 5) of any of the examples 5-12 wherein the FET comprises a p-type FET, the CMOS device further including:

the stripe including a second n-type FET including a second source contact (S) to the III-nitride material, a second drain contact (D) to the III-nitride material, and a second gate contact on the stripe between the second source contact and the second drain contact;

the III-nitride material comprises a second n-type channel layer between the second source contact and the second drain contact; and

insulator between the n-type FET and the p-type FET.

14. The CMOS device of example 13, wherein the second channel layer is strained along the long axis between the second source contact and the second drain contact.

15. The devices of any of the examples 5-9 or 13-14, wherein the strain along the long axis is uniaxial compressive strain and the long axis is along a direction of lowest hole effective mass.

16. A device, comprising (e.g., as illustrated in Fig. 7):

a bipolar heterojunction transistor (BJT), including:

a stripe 310 comprising first n-type material 700 (n), wherein the n-type is strained along a long axis of the stripe;

an emitter contact (E) on a top surface of the stripe;

p-type material 702 between the first n-type material and second n-type material 704 (n), wherein the p-type material is on a bottom surface of the stripe opposite the emitter contact;

a base contact (B) to the p-type material;

a collector contact (C) to the second n-type material; wherein a direction of electron flow in an active mode of the BJT is between the emitter and the collector.

17. The device of example 16, wherein the strain along the long axis is uniaxial tensile strain.

18. The device of any of the examples 16-17, further comprising the base contact on a side of the stripe parallel to the long axis, as illustrated in Fig. 7.

19. The device of any of the examples 16-18, further comprising a plurality of the BJTs attached to the stripe and further including an additional base contact on top of the stripe between the BJTs, as illustrated in Fig. 8A.

20. The device of any of the examples 16-19, wherein the n-type material and the p-type material comprise III-nitride material.

21. A field effect transistor (FET), comprising:

a stripe 310 including III-nitride material 312, wherein:

the III-nitride material includes an n-type channel layer strained along a long axis 302 of the stripe and at least partially relaxed along a direction 304 perpendicular to the long axis;

the III-nitride material includes an n-type channel layer (400, see Fig. 4 and Fig. 3) which is more strained/less relaxed along a long axis of the stripe and less strained/ more relaxed along a direction perpendicular to the long axis; and

the n-type channel layer comprises gallium and/or aluminum, and/or indium;

a source contact (S) comprising first metal on the stripe making ohmic contact to the n-type channel;

a drain contact (D) comprising second metal on the stripe making ohmic contact to the n-type channel;

a gate contact (G) on the stripe between the source contact and the drain contact, the gate contact controlling flow of electron current along the direction perpendicular to the long axis through the n-type channel layer and between the source contact and the drain contact.

22. The FET of example 21, wherein the III-nitride material includes a layer comprising aluminum and gallium and indium between the n-type channel and the source contact, the drain contact, and the gate contact.

23. The FET of examples 21 or 22, wherein a top surface of the stripe on which the source contact and drain contact are formed is an N-polar surface, so that the n-type channel layer has an N-polar orientation.

24. The FET of example 23, wherein the current flows through a two dimensional electron gas (2DEG) or two dimensional hole gas induced from a back-barrier comprising the layer of gallium and/or aluminum, and/or indium, so contact to the 2DEG or hole gas is formed over an entire contact area and not merely at an edge of the ohmic regions contacting the n-type channel layer.

25. The device or FET of any of the preceding examples, wherein the stripe length is at least 2 times longer than the stripe width.

26. An optoelectronic device, comprising (e.g., as illustrated in Fig. 33):

a stripe 3300 comprising III-nitride material 3302, wherein:

the III-nitride material is strained along a long axis 3304 of the stripe and at least partially relaxed along a second direction 3306 perpendicular to the long axis or the short axis; and

the III-nitride material includes:

an active region 3308;

a III-nitride n-type layer 3310; and

a III-nitride p-type layer 3312, wherein the active region is between the n-type layer and the p-type layer. The active region may emit light in response

to holes injected from the p-type region and electrons injected from the n-type region recombining in the active region.

27. The device of example 26, wherein the active region includes InGaN, the p-type region includes n-type GaN, and the p-type layer comprises p-type GaN.

28. The device of example 26 or 27, further comprising (e.g., as illustrated in Fig. 34):

a pixel 3500 including the stripe;

material 3502 grown on either side of the stripe so as to create compressive strain in the layers in the stripe, resulting in light hole formation in the enclosed layers and additional improved hole transport occurring along the stripe direction.

29. The device of example 28, wherein the material grown on either side of the stripe comprises InGaN or III-nitride.

30. The device of examples 26-29, wherein the device has an N-polar orientation.

31. The device of examples 26-30, wherein the device comprises a light emitting diode, a laser diode, a solar cell, or a photodiode.

32. A device, comprising:

III-nitride material 312 is strained along a long axis 302 (or short axis) of the stripe 310 and at least partially relaxed along a direction 304 perpendicular to the long axis (or the short axis);

the III-nitride material includes a channel layer;

a source contact comprising first metal on the stripe making ohmic contact to the channel;

a drain contact comprising second metal on the stripe making ohmic contact to the channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of current along a direction of the long axis or short axis through the channel and between the source contact and the drain contact.

33. The device of examples 1-2, wherein the device is a transistor, a light emitting diode, a laser diode, a solar cell or a photodiode, and the III-nitride material includes the device's active region.

34. The device of example 33, wherein the active region includes InGaN.

35. The device of examples 33 or 34, wherein the device is biased and contacted so as to take advantage of lower effective hole mass along the first direction.

36. The device of example 35, wherein the device comprises a field effect transistor including a channel, wherein the source and drain are along the first direction so that current flows along the first direction between the source and the drain.

37. The device of example 36, wherein the III-nitride material is relaxed over a distance of at least one micron in the second direction.

38. A device, comprising:

III-nitride material which is at least partially biaxially relaxed (e.g., along the first direction 302 and the second direction 304).

39. The device of example 1 or 38, wherein the III-nitride is on a porous III-nitride, and patterned into features 306, wherein the porous III-nitride allows relaxation or partial biaxial relaxation of the structure.

40. The device of example 2 or 39, wherein the porous III-nitride includes etched pores.

41. The device of example 2, 3 or 39 or 40, wherein the porous III-nitride comprises gallium nitride.

42. The FET of any of the preceding examples, wherein the stripe has a width in a range of 100-20 000 nanometers and the source contact and drain contact have a width less than the device width.

43. The stripe and channel materials can be composed of any (B,Al,Ga,In)(N) and any (B,Al,Ga,In)(N, As,P) alloy, as long as the geometry and the lattice constant conditions are met.

44. For high power, plus useful gain at 220 GHz and 340 GHz, the HEMTs must exhibit fmax of 500 GHz and 800 GHz respectively. For high fmax , we must first increase fτ. Increasing the electron velocity in the channel brings a double benefit, decreasing the transit time and, through increased transconductance, reducing the C parasitic/ gm charging time. Increasing the electron velocity in the channel by using relaxed InGaN as the channel material which provides a reduced electron effective mass, critical in reducing electron scattering and enhancing electron velocity.

45. In one example, the device comprises a high-power nitrogen-polar AIGaN/InGaN mm-Wave Power HEMTs. Adding InGaN channels to this technology, the upper cutoff frequencies can be extended to as high as 800GHz, and provide output power exceeding 1 W/mm at 220 and 340GHz. The InGaN channel must be relaxed; growth directly on GaN would introduce strain. Similar to strain-induced changes in mobility in InGaAs, strain in InGaAs would increase the electron effective mass and thus decrease the electron mobility and channel injection velocity. An $In_{0.2}Ga_{0.8}N$ channel should have a high >5000 cm2/V-s 2DEG mobility, enabling high , plus a 2.5eV bandgap, enabling high-voltage, high-power operation. Indeed , 3570 cm2/Vs mobility has been measured for InN, nearly 6: 1 larger that than that observed in GaN at similar carrier densities. As described herein, relaxed InGaN layers can be formed in an unique manner, e.g., growing material in 200nm width fin. In the direction of the cross-section of the fin, the N-polar GaN/InGaN/AlGaN stack relaxes after patterning to that of InGaN. The electron effective mass in the transport direction, determined by the relaxed lattice constant, will then be low. Using X-ray analysis, we have demonstrated that of nano-stripe patterning relaxes the strain in InGaN /GaN multi quantum wells; in this example, the technique is applied to N-polar GaN/InGaN /AlGaN HEMTs.

46. With an InGaN channel the electron velocity will be ~$1 . 3 \bullet 1 0^{7}$ cm/s, increasing fmax to 500GHz. In one or more further examples, improved targets may be reached with a shorter gate length and a slightly higher relaxed indium

composition. Other example enhancements extending fmax to its targets include reduced gate length for reduced intrinsic delay and thinned channels to maintain aspect ratio and voltage gain. Together, these methods may, in some examples, double f_τ to ~240 GHz. Source, drain, and gate parasitic resistances will be reduced by improved contact resistivity, increased channel conductivity, shorter access regions, and reduced gate finger length. Together, these can deliver fmax beyond 800 GHz.

47. In one or more examples, to adequately relax the strain, the fins must be narrow. To fit, in one or more examples the Ohmic contacts must be at most 100 nm long, which then demands extremely low specific contact resistivity. N-polar GaN HEMTs have shown 2.3 Ohm-μm^2 ρ, a record low for GaN . In one or more examples, to further reduce the contact resistivity, the N+ contact regrowths may be graded from $In_{0.2}Ga_{0.8}N$ to $In_{0.63}Ga_{0.37}N$ or even to InN, and may be doped at ~ 10^{20} cm^{-3}, the high doping assisted in part by strong 3D polarization doping from the rapid compositional gradient.

48. A transistor operating at terahertz modulation frequencies comprising a transistor of any of the preceding embodiments.

49. A power amplifier or cellular network including the transistor of any of the preceding embodiments.

50. A device comprising III-nitride material having a low hole effective mass in the vertical direction via biaxial strain (here the split off band is the one with the low effective mass). See e.g., Fig. 32.

51. (a) A device where the GaN is biaxially strained such that it results in the split-off band as the topmost valence band (above the light hole and the heavy hole in the valence band) resulting in increased hole mobility in the vertical direction.

52. (b) A device wherein the channel region which may or may not be on a sidewall, the AlGaN or InGaN is re-grown on the a- or m-plane or semi-polar sidewall of a GaN feature resulting in enhanced hole mobility in the vertical direction.

53. (c) A device that combines the above examples 51 and 52, with example 51a) referring to the drift region of the device and example 52 b) referring to the channel region of the device.

Nomenclature

GaN and its ternary and quaternary compounds incorporating aluminum and indium (AlGaN, InGaN, AlInGaN) are commonly referred to using the terms (Al,Ga,In)N, III-nitride, III-N, Group III-nitride, nitride, Group III-N, $Al_{(1-x-y)}In_yGa_xN$ where $0 < x < 1$ and $0 < y < 1$, or AlInGaN, as used herein. All these terms are intended to be equivalent and broadly construed to include respective nitrides of the single species, Al, Ga, and In, as well as binary, ternary and quaternary compositions of such Group III metal species. Accordingly, these terms comprehend the compounds AlN, GaN, and InN, as well as the ternary compounds AlGaN, GaInN, and AlInN, and the quaternary compound AlGaInN, as species included in such nomenclature. When two or more of the (Ga, Al, In) component species are present, all possible compositions, including stoichiometric proportions as well as "off-stoichiometric" proportions (with respect to the relative mole fractions present of each of the (Ga, Al, In) component species that are present in the composition), can be employed within the broad scope of the invention. Accordingly, it will be appreciated that the discussion of the invention hereinafter in primary reference to GaN materials is applicable to the formation of various other (Al, Ga, In)N material species. Further, (Al,Ga,In)N materials within the scope of the invention may further include minor quantities of dopants and/or other impurity or inclusional materials. Boron (B) may also be included.

One approach to eliminating the spontaneous and piezoelectric polarization effects in GaN or III-nitride based optoelectronic devices is to grow the III-nitride devices on nonpolar planes of the crystal. Such planes contain equal numbers of Ga (or group III atoms) and N atoms and are charge-neutral. Furthermore, subsequent nonpolar layers are equivalent to one another so the bulk crystal will not be polarized

along the growth direction. Two such families of symmetry-equivalent nonpolar planes in GaN are the {11-20} family, known collectively as a-planes, and the {1-100} family, known collectively as m-planes. Thus, nonpolar III-nitride is grown along a direction perpendicular to the (0001) c-axis of the III-nitride crystal.

Another approach to reducing polarization effects in (Ga,Al,In,B)N devices is to grow the devices on semi-polar planes of the crystal. The term "semi-polar plane" (also referred to as "semipolar plane") can be used to refer to any plane that cannot be classified as c-plane, a-plane, or m-plane. In crystallographic terms, a semi-polar plane may include any plane that has at least two nonzero h, i, or k Miller indices and a nonzero l Miller index.

Some commonly observed examples of semi-polar planes include the (11-22), (10-11), and (10-13) planes. Other examples of semi-polar planes in the wurtzite crystal structure include, but are not limited to, (10-12), (20-21), and (10-14). The nitride crystal's polarization vector lies neither within such planes or normal to such planes, but rather lies at some angle inclined relative to the plane's surface normal. For example, the (10-11) and (10-13) planes are at 62.98° and 32.06° to the c-plane, respectively.

References for PART A

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Part IV: Example Applications and Systems using embodiments described herein.

Modern computing systems based on Von Neumann architecture relies on a clear distinction between logic and memory and processes information by executing a sequence of precise atomic instructions with periodic uploads to the memory. As we enter the age of machine learning, big data analytics and secure cloud computing, the heavy data traffic between the processing units and memory becomes a fundamental bottleneck of high performance computing.

The mega trends of cloud computing, big data and IoT are driving an insatiable need for unlimited bandwidth and enhanced security for wireless communication systems, requiring disruptive innovations in frequency-agile and adaptive-bandwidth analog technologies. Extensive research expertise in in-situ control and tuning of extra-ordinary electrical, mechanical and magnetic response in synthetic heterostructures can be used to create reconfigurable and adaptive analog circuits that are capable of operating at multiple frequencies and bandwidths.

Extremely large-scale heterogeneous integration of memory, logic and analog devices in future electronic systems warrant radical packaging solutions to address the growing challenges in power delivery, signal integrity, thermal management and electromagnetic/RF interferences. Innovations in materials can be leveraged for logic, memory and analog devices and seek

new packaging paradigm to provide superior power-performance-reliability-cost in smaller volume, with higher security through smart shielding, with efficient power management by fine-grain integration of passives, and enhanced communication bandwidth by package level implementation of waveguides.

RF and mixed-signal technologies for frequency-agile systems targeting smaller volume, higher energy- efficiency, fine-grain reconfiguration, hardware security and CMOS compatibility through heterogeneous integration of functional materials such as MIT and ferroelectric phase transition materials, complementary ultra-wide band gap (UWBG) power transistors and magneto- electric multi-ferroics into analog devices (Fig. 4). The six tasks in this theme are described below:

High efficiency DC-DC converters: 48 to 1V point-of-load (PoL), system-in- package, DC-DC converters for data center applications, targeting >100MHz operation, ~200W output power, >90% peak (>70% light-load) efficiency. Breakthroughs in complementary GaN FETs and control and circuit design techniques (3.1) will lead to significant energy and cost savings in power routing. Polarization-induced p-channel FETs in AlN/GaN heterostructures can be used as a step towards complementary GaN logic.

Part V: Example THz Systems including embodiments described herein

0.1-1THz converged wireless systems may enable revolutionary capabilities in communications and perception with far-reaching implications for industry and national security. The tiny wavelengths enable vast numbers of elements to be packed into physically small antenna arrays, which in turn allows the vast available bandwidth to be reused many times by using narrow, tightly focused beams. These physical characteristics to build highly agile

systems with immense communications capacity, and an unparalleled combination of resolution and robustness.

Embodiments (e.g., transistors) described herein can be used cellular infrastructure using hubs with massive spatial multiplexing, providing 1-100Gb/s to the end user, and, with 100-1000 simultaneous independently-modulated beams, aggregate hubs capacities in the 10's of T b/s. Cellular infrastructure may include a mix of optical links and Tb/s-capacity point-point massive MIMO links. These mobile links will support cm-precision localization, supplementing GPS, and will use imaging techniques to locate communications partners. This intelligent immersive infrastructure may support low-latency virtual reality (VR), augmented reality (AR), and seamless telepresence.

Embodiments described herein (e.g., transistors) can be used in transportation, supporting autonomous vehicles and intelligent highways. Wideband inter-car links may communicate data and measure vehicle locations to cm- precision; anticipating and manage interactions, and avoid collisions . Unparalleled high- resolution imaging, compact enough to fit on a car, may let drivers see through extreme fog and rain as well as our eyes can on a clear day, while low-cost, lightweight "whisper radios" will replace wire harnesses in vehicles.

Embodiments described herein may be used in the air, providing a framework for rich situational awareness, navigation and mapping using networks of drones. Revolutionary new capabilities in individual sensors include THz 4K-video resolution imaging radar or synthetic aperture radar (SAR) may be small enough to fit on a drone or UAV, allowing these to fly in smoke/dust to detect, identify, and engage threats, even in darkness or when blinded by weather or sunlight.

Embodiments described herein may be used in RF/wireless/THz, analog and digital IC, and, for increased range and reduced DC power.

In one or more examples, we refer to 0.1-ITHz as "THz". 30-300GHz is mm-wave and 0.3-3THz sub-mm-wave.

Many aspects have direct applicability to 5G and future standards, including > 100GHz , with orders of magnitude higher data rates and spectral efficiency. The move to the mm-wave and THz bands is an attractive option for obtaining truly transformative gains in wireless systems.

Embodiments described herein can be used for mm-wave/THz ICs and arrays for communication and imaging. Exemplary modules contain arrays of antennas and the RF (THz) signal channels . The modules may operate with RF carriers in the 1O0's of GHz, with arrays of 100- 1000 elements, and with 1-100GHz symbol modulation rates, where each module will transmit or receive 100-1000 independent beams simultaneously. The baseband signal processing, with a careful balance of analog and digital stages, may spatially demultiplex (separate) hundreds of high-rate signals, and will do so while consuming only moderate DC power. Multipath propagation will cause inter symbol interference in these high-rate streams, which will be corrected by analog and digital equalizers or nulled by adaptive beamformers.

Application-specific THz transistors may be key to extending performance. Advanced GaN and InP transistors may increase the output power and improve the efficiency while reducing the receiver noise and increasing the upper frequency range of these THz systems . These component-level improvements may result in reduced system power, increased system range and bit rate for carrier frequencies where silicon solutions remain feasible, but will also enable higher-frequency systems for increased capacity and - in the context of imaging - resolution.

Embodiments described herein can be the foundation of a new generation of Tb/s capacity mobile and residential wireless communications, compact yet high-resolution imaging systems for cars and UAVs, and systems merging communications, sensing and imaging.

These terabit-capacity wireless networks and high-resolution imaging systems exploit the 900GHz of bandwidth between 0.1- 1 THz - spectrum that has been made newly accessible by rapid increases in transistor cutoff frequencies in the last decade. Yet, increasing the carrier frequency not only brings more channel capacity into play, but also changes the character of propagation, bringing radically new opportunities along with significant technical difficulties.

The difficulties include high attenuation and easily-blocked beams. Of course, the high frequencies also bring considerable opportunities. In one or more examples, an antenna array designed for broad angular steering may have ~ λ/2 element spacing. Because the wavelengths are small (0.3-3mm), even a large array will occupy little space: a 1000-element, 140GHz array occupies less than 2 square inches. Such arrays have high gain, recovering signal strength, though the radiation pattern is now narrow, hence beams must be steered to find and track moving communication partners. With the right electronics and control algorithms, such arrays can form, aim, and track multiple beams, with each beam using the same spectrum while carrying independent modulation, and with a massive number of beams. An antenna array can resolve the directions of incoming signals; it is thus, of course, also an imaging system. With an array of diameter D, the angular resolution is ~ λ/ D , so very sharp, TV-like imaging is feasible, even from a very small imager. Yet, in a simple imaging array, the number of image pixels is the number of receiver channels; an HDTV-like 1920 x1080 pixel imager would need a staggering $2 \bullet 1\ 0^{6}$ RF channels.

Large, 100-to 10,000-element THz phased-array transmitters and receivers, constructed in silicon VLSI, may be very small, fitting easily on platforms from large to tiny: planes, cars, unmanned aerial vehicles (UAVs), drones, and even handsets. The large arrays compensate for the high THz propagation losses, allowing ~250-500m range. High- capacity radio

transceivers, carrying 100-1000 channels, and high-resolution imaging systems, can both be made very small. The functions of imaging and communication can be merged, using imaging techniques to determine directions of incoming signals when establishing communication links, and using, as with GPS, signal time-of-flight in communications networks so that radios on mobile platforms can determine precisely where they are.

THz wireless systems need application-specific THz transistors. High-speed transistors, based on advanced semiconductor materials described herein, may enable systems operating above 250GHz. Even at lower frequencies, from 100-250GHz, MOSFET noise figures are relatively high, and MOSFET transistor output power and efficiency are low. Custom high-power and low-noise transistors may greatly improve the transmission range and reduce the DC power consumption in systems below 200GHz. As antenna element spacings are typically $\lambda/2$, there is little IC area available to fit the power amplifier, so high power density is also important.

Hardware, such as the mm-wave/THz ICs and Arrays for Communication and Imaging include sophisticated THz RF- IC architectures supporting the targeted systems. In one or more examples, these silicon ICs must operate at signal frequencies up to 220 GHz, with ICs in the custom semiconductor technologies up/down- converting to 340, 650, or 1080GHz as appropriate. The transmitter and receiver ICs may be arrays, e.g., containing -100-1000 elements, the symbol rates may be be 1-100GHz, and, whether on transmit or receive, and the ICs may process up to 100 or even 1000 simultaneous beams. In one or more examples, the front- end RF-IC design thus requires high carrier frequencies, wide bandwidths, high dynamic range, and very many channels.

Transceiver RF sections and its baseband may use Terabit baseband signal processing ICs. In one or more examples, the baseband sections of the massive MIMO receivers must process and separate 100-1000 channels of 1-

100Gbs/s data. If the MIMO beam separation is 100% digital, then the ADCs must have high sample rates and high resolution (note that despite the large number of antennas - which would reduce the ADC resolution requirements- there is also a large number of beams), and the subsequent digital processing may have many bits of resolution, high clock rates, and many parallel channels .

Example Application-Specific THz Transistors

Embodiments described herein may be used to exploit 100GHz-1THz carrier frequencies for high-capacity communications and for high-resolution imaging.

Given the high propagation losses noted above, even with arrays of considerable size, THz links can be constrained to very short transmission range. Though we will increase range greatly by increasing the number of array elements and array RF channels, at some point array size becomes limited by the cost of these increasingly complex ICs and by the power consumed in managing so many RF channels. Thus, application-specific THz transistors using embodiments described herein may comprise high- power GaN- and InP- based power transistors for increased transmitter power and improved efficiency, and InP-based low-noise transistors for improved receiver sensitivity, both increasing range and both reducing DC power consumption. Further, for increased capacity and improved resolution, communications links and imaging systems having carrier frequencies above 250GHz may be used. Although in fundamental mode operation transistors can provide gain close to their cutoff frequencies, or, in harmonic mode operation, even several times this, in both cases receiver sensitivity and transmitter power and efficiency are very low. For amplifiers with low noise, high output power, or high efficiency, the transistor cutoff frequencies must be 3:1 to 4:1 times the signal frequency. Embodiments described herein may

be used in infrastructure and consumer hardware (e.g., GaN and InP transistors with bandwidth sufficient for efficient low-noise, high-power, efficient operation at 340, 650, and 1080GHz).

Examples include advanced III-V (e.g., Gallium Nitride and Indium Phosphide) high-frequency transistors. THz systems may use transistors, at strategic points in the signal chain, to extend communications range and reduce power consumption. As with today's cell phones, future THz systems may use CMOS VLSI for the baseband and the RF signal chain, but, where performance demands it, also in high-performance transistors in the RF front-ends, specifically in the power amplifiers and low-noise amplifiers.

CMOS VLSI offers high integration scales and low die cost. Though the raw device-level cutoff frequencies are c.a. 300-400 GHz in leading technologies, once wiring stack losses are considered, useful amplifier gain can be obtained up to - 220GHz. High-frequency performance is best in 45-32-22nm technologies; in nodes beyond this, the transistors start to approach the physical limits of scaling, and the RF bandwidth degrades. Further, above 100 GHz, even though there is sufficient available gain, these transistors have high noise figures, provide only limited RF output power, and generate signal power at only low DC-RF efficiency . Radios using these transistors in the power- and low-noise amplifiers will have very limited transmission range; at least, unless the transceivers use very large phased arrays for high aperture gains.

Example systems at 140, 220, 340, 650, and 1080GHz may be used. At 140 and 220GHz, we will explore the trade-offs in system complexity, cost, and power consumption between smaller arrays using high-efficiency III-V power- and low-noise amplifiers and larger arrays using CMOS PAs and LNAs. At 340 GHz and higher, III-V transistors, with their wider bandwidths , must also translate 220GHz signals, generated by CMOS, to the higher transmission frequency.

Higher-power amplifiers directly increase system range. Efficient power amplifiers reduce power consumption. This is particularly important, as power amplifier efficiency might otherwise be only 5-10%. Lower-noise amplifiers also directly increase system range. Importantly, a less noisy low-noise amplifier saves much DC power; if we improve the receiver noise figure by 3dB, then the transmitter need radiate only one-half the RF power.

Advanced mm-Wave/THz devices, extending the capabilities of 0.1-1THz systems may be implemented using embodiments described herein, including advanced field-effect-transistors with very low noise figure, and transistors with high output power and high efficiency. The benefit is increased system range and greatly reduced DC power. The GaN transistors, offer very high output powers; the applications for these include arrays, but extend beyond them to high-power single- source systems such as synthetic aperture radar and jammers. The InP transistors offer - 3:l smaller power densities at a given frequency, but offer - 3: 1 greater useful frequency range. The cutoff frequencies of these GaN and InP transistors will be high, enabling operation , with low noise, high power, and high efficiency , at 340, 650, and 1080GHz.

Advanced, high-performance mm-wave/THz devices can be developed, including N-polar GaN HEMTs, adding InGaN channels in a strain-relaxed pedestal structure to push bandwidth to 800 GHz, and supporting high-power amplifiers to 220 and perhaps 340GHz.

In one or more examples, reducing the effective mass of InGaN on GaN through strain relaxation and thereby increasing frequency performance of InGaN on GaN, opens a pathway to enhancing electron transport properties in InGaN channels through strain relaxation enabling THz performance at high efficiency.

GaN HEMTs are now considered the preferred power device for RF power for commercial to military applications. The trade-off between

dispersion, gate breakdown, and field-plate capacitance limiting gain in Ga-polar HEMTs to date has been broken using N-polar GaN based HEMTs. Deep recessed N-polar HEMTs have produced power density three times larger than Ga-polar HEMTS at 94GHz; with power added efficiency (PAE) greater than 25% at 8W/ mm. This is because of the ability to simultaneously maximize charge in the channel, eliminate/reduce field plates dimensions, enabling high gain while maintaining breakdown because of the reverse polarization of the AlGaN under that gate (compared to Ga-polar structures). The clear remaining hard problem that has emerged is the limited velocity of electrons in the GaN channel and the ability to maintain high gain at bias conditions amenable to high efficiency operation. In one approach, N-polar HEMTs are made using relaxed lnGaN channels using both MBE and MOCVD. The variation of electron effective mass with In composition may also be determined. Relaxed InGaN channels may achieve lower effective mass by using fin geometries for the transistors. We have shown relaxation using fin geometries in InGaN/GaN superlattices. The degree of relaxation with fin dimension may be established via X-ray reciprocal space maps (RSMs). Processes to fabricate fin HEMTs to exploit the effective mass in the relaxed dimension may be optimized.

Table 5 – Summary of Thrust C challenges and approaches

Critical Challenges	Solutions	Demonstration Vehicles
Efficient, high-power-density PAs	N-polar InGaN HEMTs	MIMO grand challenge testbed at 140, 220, 340 GHz
	AlN/GaN/AlN HEMTs	
Cost-effective GaN	AlN/GaN/AlN HEMTs on silicon	MIMO grand challenge testbed at 140 GHz
Removing heat in high-power PAs	diamond thermal management for GaN	MIMO grand challenge testbed at 140 GHz
Ultra-efficient 140GHz , 220GHz PAs	THz InP HBTs	MIMO grand challenge tested at 140-1080GHz. 340GHz frequency-scanned imaging demonstration.
340-1080GHz transmitter front-ends		
Low noise for energy-efficient 140GHz , 220GHz links	THz InAs/InP MOS-HEMTs	MIMO grand challenge tested at 140-1080GHz. 340GHz frequency-scanned imaging demonstration
340-1080GHz receiver front-ends		
Low cost LNAs and PAs	THz InP MOS-HEMTs and HBTs on silicon	MIMO grand challenge testbed at 140, 220, 340 GHz
High-power sources for near-THz imaging	Monolithically integrated GaN THz signal sources by harmonic generation	Focal-plane imaging grand challenge sent test (source)

Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS

1. A device, comprising:

III-nitride material strained along a first direction and at least partially relaxed along a direction perpendicular to the first direction.

2. The device of claim 1, wherein the III-nitride is on or above porous III-nitride, and patterned into ridge or fin structures, wherein the porous III-nitride allows relaxation or partial relaxation of the fin structure perpendicular to the fin or the short axis while the fin material remains strained or relaxes less in the direction along the fin or the long direction resulting in uniaxial strain in the fin structure.

3. The device of claim 2, wherein the porous III-nitride includes etched pores.

4. The device of claim 2 or claim 3, wherein the porous III-nitride comprises gallium nitride.

5. The device of claim 1, wherein the device is a field effect transistor (FET), including:

a stripe comprising the III-nitride material, wherein:

the III-nitride material is strained along the first direction comprising a long axis of the stripe and at least partially relaxed along the second direction comprising a direction (short axis) perpendicular to the long axis ;

the III-nitride material includes a channel layer;

a source contact comprising first metal on the stripe making ohmic contact to the channel;

a drain contact comprising second metal on the stripe making ohmic contact to the channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of current along a direction of the long axis or short axis through the channel and between the source contact and the drain contact.

6. The device of claim 5, wherein:

the channel comprises gallium and/or indium and/or aluminum (and/or boron)

the III-nitride material comprises the channel layer on a layer including gallium and/or aluminum and/or indium and/or boron,

a thickness of the layer comprising gallium and/or aluminum, and/or indium is more than 50% of a thickness of the stripe,

an composition is selected so as to obtain a desired strain in the channel along the long axis.

7. The device of claim 5, wherein:

the III-nitride material further includes a source region and a drain region,

the source region is in physical contact with the channel layer between the source contact and the channel layer,

the drain region is in physical contact with the channel layer between the drain contact and the channel layer, and

the source region and the drain region have a lattice constant different than a lattice constant of channel so as to induce the strain in the channel layer along the long axis.

8. The device of claim 7, wherein the source region and the drain region comprise gallium and/or aluminum, and/or indium (e.g., InGaN channel case on GaN).

9. The device of any of the claims 5-8, wherein:

the current between the source contact and the drain contact is along the long axis that is a crystallographic a- or m-direction of the III-nitride,

the short axis direction perpendicular to the long axis is a crystallographic m- or a- direction of the III-nitride, respectively.

the top surface of the stripe has a polar (0001) or (000-1) orientation, and

the channel has a lattice constant larger than the underlying III-nitride material.

10. The device of any of the claims 5-8, wherein:

the current between the source contact and the drain contact is along the short axis that is a crystallographic a- or m-direction of the III-nitride,

the long axis direction perpendicular to the short axis is a crystallographic a- or m-direction of the III-nitride,

the top surface of the stripe has a polar (0001) or (000-1) orientation, and

the channel has a lattice constant smaller than the underlying III-nitride material.

11. The device of any of the claims 5-8, wherein:

the current between the source contact and the drain contact is along the short axis that is a crystallographic m-direction of the III-nitride,

the long axis direction perpendicular to the short axis is a crystallographic c-direction of the III-nitride, and

the top surface of the stripe has a nonpolar a- or m-plane orientation.

.

12. The device of any of the claims 5-9, wherein the FET comprises a p-type FET conducting the current comprising holes and the strain along the long axis is uniaxial compressive strain.

13. A device comprising a CMOS device of any of the claims 5-12 wherein the FET comprises a p-type FET, the CMOS device further including:

the stripe including a second n-type FET including a second source contact to the III-nitride material, a second drain contact to the III-nitride material, and a second gate contact on the stripe between the second source contact and the second drain contact;

the III-nitride material comprises a second n-type channel layer between the second source contact and the second drain contact; and

insulator between the n-type FET and the p-type FET.

14. The CMOS device of claim 13, wherein the second channel layer is strained along the long axis between the second source contact and the second drain contact.

15. The devices of any of the claims 5-9 or 13-14, wherein the strain along the long axis is uniaxial compressive strain and the long axis is along a direction of lowest hole effective mass.

16. A device, comprising:

a bipolar heterojunction transistor (BJT), including:

a stripe comprising first n-type material, wherein the n-type is strained along a long axis of the stripe;

an emitter contact on a top surface of the stripe;

p-type material between the first n-type material and second n-type material, wherein the p-type material is on a bottom surface of the stripe opposite the emitter contact;

a base contact to the p-type material;

a collector contact to the second n-type material; wherein a direction of electron flow in an active mode of the BJT is between the emitter and the collector.

17. The device of claim 16, wherein the strain along the long axis is uniaxial tensile strain.

18. The device of any of the claims 16-17, further comprising the base contact on a side of the stripe parallel to the long axis.

19. The device of any of the claims 16-18, further comprising a plurality of the BJTs attached to the stripe and further including an additional base contact on top of the stripe between the BJTs.

20. The device of any of the claims 16-19, wherein the n-type material and the p-type material comprise III-nitride material.

21. A field effect transistor (FET), comprising:

a stripe including III-nitride material, wherein:

the III-nitride material includes an n-type channel layer strained along a long axis of the stripe and at least partially relaxed along a direction perpendicular to the long axis;

the III-nitride material includes an n-type channel layer which is more strained/less relaxed along a long axis of the stripe and less strained/ more relaxed along a direction perpendicular to the long axis; and

the n-type channel layer comprises gallium and/or aluminum, and/or indium;

a source contact comprising first metal on the stripe making ohmic contact to the n-type channel;

a drain contact comprising second metal on the stripe making ohmic contact to the n-type channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of electron current along the direction perpendicular to the long axis through the n-type channel layer and between the source contact and the drain contact.

22. The FET of claim 21, wherein the III-nitride material includes a layer comprising aluminum and gallium and indium between the n-type channel and the source contact, the drain contact, and the gate contact.

23. The FET of claims 21 or 22, wherein a top surface of the stripe on which the source contact and drain contact are formed is an N-polar surface, so that the n-type channel layer has an N-polar orientation.

24. The FET of claim 23, wherein the current flows through a 2DEG induced from a back-barrier comprising the layer of gallium and/or aluminum, and/or indium, so contact to the 2DEG is formed over an entire contact area and not merely at an edge of the ohmic regions contacting the n-type channel layer.

.

25. The device or FET of any of the preceding claims, wherein the stripe length is at least 2 times longer than the stripe width.

26. An optoelectronic device, comprising:

a stripe comprising III-nitride material, wherein:

the III-nitride material is strained along a long axis of the stripe and at least partially relaxed along a direction perpendicular to the long axis or the short axis; and

the III-nitride material includes:

an active region;

a III-nitride n-type layer; and

a III-nitride p-type layer, wherein the active region is between the n-type layer and the p-type layer.

27. The device of claim 26, wherein the active region includes InGaN, the p-type region includes n-type GaN, and the p-type layer comprises p-type GaN.

28. The device of claim 26 or 27, further comprising:

a pixel including the stripe;

material grown on either side of the stripe so as to create compressive strain in the layers in the stripe, resulting in light hole formation in the enclosed layers and additional improved hole transport occurring along the stripe direction.

29. The device of claim 28, wherein the material grown on either side of the stripe comprises InGaN.

30. The device of claims 26-29, wherein the device has an N-polar orientation.

31. The device of claims 26-30, wherein the device comprises a light emitting diode, a laser diode, a solar cell, or a photodiode.

32. A device, comprising:

III-nitride material is strained along a long axis of the stripe and at least partially relaxed along a direction perpendicular to the long axis or the short axis;

the III-nitride material includes a channel layer;

a source contact comprising first metal on the stripe making ohmic contact to the channel;

a drain contact comprising second metal on the stripe making ohmic contact to the channel;

a gate contact on the stripe between the source contact and the drain contact, the gate contact controlling flow of current along a direction of the long axis or short axis through the channel and between the source contact and the drain contact.

33. The device of claims 1-2, wherein the device is a transistor, a light emitting diode, a laser diode, a solar cell or a photodiode, and the III-nitride material includes the device's active region.

34. The device of claim 33, wherein the active region includes InGaN.

35. The device of claims 33 or 34, wherein the device is biased and contacted so as to take advantage of lower effective hole mass along the first direction.

36. The device of claim 35, wherein the device comprises a field effect transistor including a channel, wherein the source and drain are along the first direction so that current flows along the first direction between the source and the drain.

37. The device of claim 36, wherein the III-nitride material is relaxed over a distance of at least one micron in the second direction.

38. A device, comprising:

III-nitride material which is at least partially biaxially relaxed.

39. The device of claim 1 or 38, wherein the III-nitride is on a porous III-nitride, and patterned into features, wherein the porous III-nitride allows relaxation or partial biaxial relaxation of the structure.

40. The device of claim 2 or 39, wherein the porous III-nitride includes etched pores.

41. The device of claim 2, 3 or 39 or 40, wherein the porous III-nitride comprises gallium nitride.

42. A device comprising III-nitride or gallium nitride, wherein the III-nitride or the gallium nitride is biaxially strained such that the biaxial strain results in the split-off band as the topmost valence band (above the light hole and the heavy hole in the valence band) resulting in increased hole mobility in a vertical direction.

43. A device, comprising a channel region, wherein the channel region may or may not be on a sidewall, wherein the AlGaN or InGaN is re-grown on an a- or m-plane or semi-polar sidewall of a GaN feature, resulting in enhanced hole mobility in the vertical direction.

44. A device of claim 42 and 43, wherein the gallium nitride in claim 42 comprises the drift region of the device and claim 43 comprises the channel region of the device.

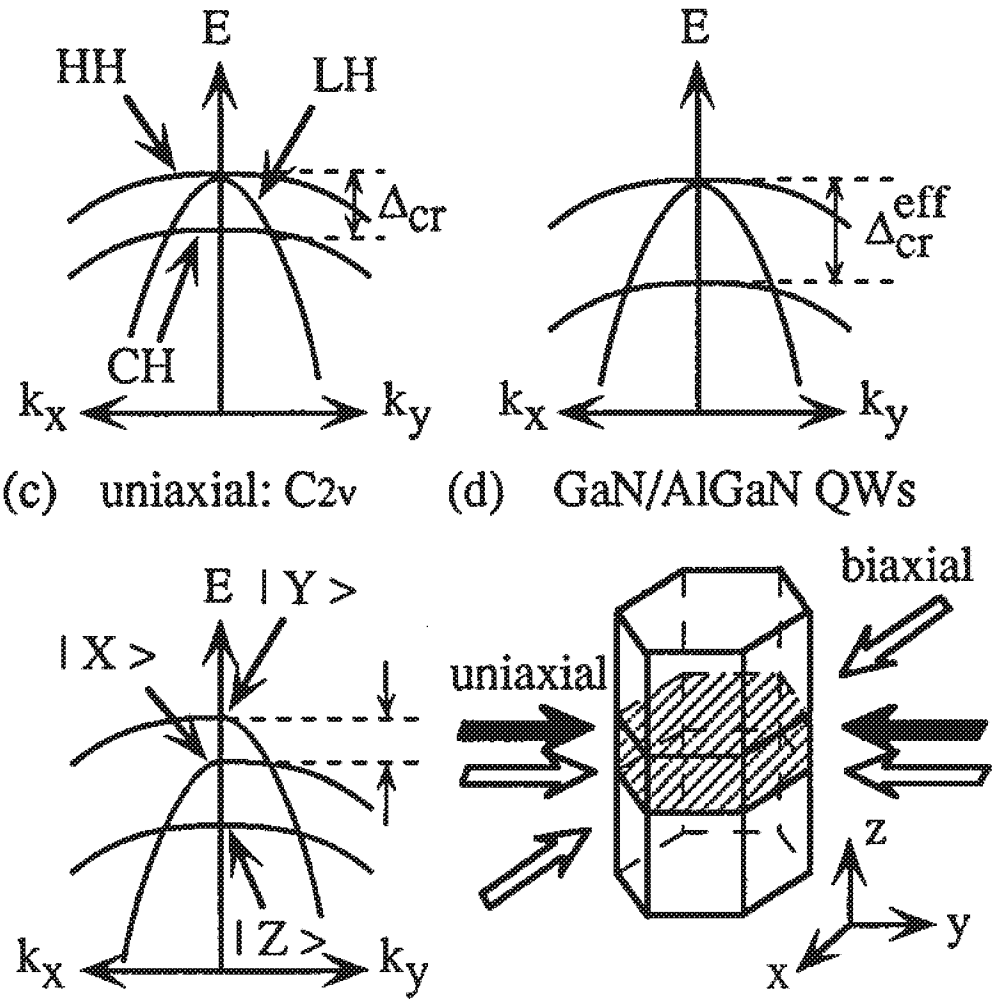

E
HH
LH
Δ_{cr}
CH
k_x
k_y
(c) uniaxial: C2v
E
Δ_{cr}^{eff}
k_x
k_y
(d) GaN/AlGaN QWs
E | Y >
| X >
| Z >
k_x
k_y
uniaxial
biaxial
z
y
x

Fig. 1

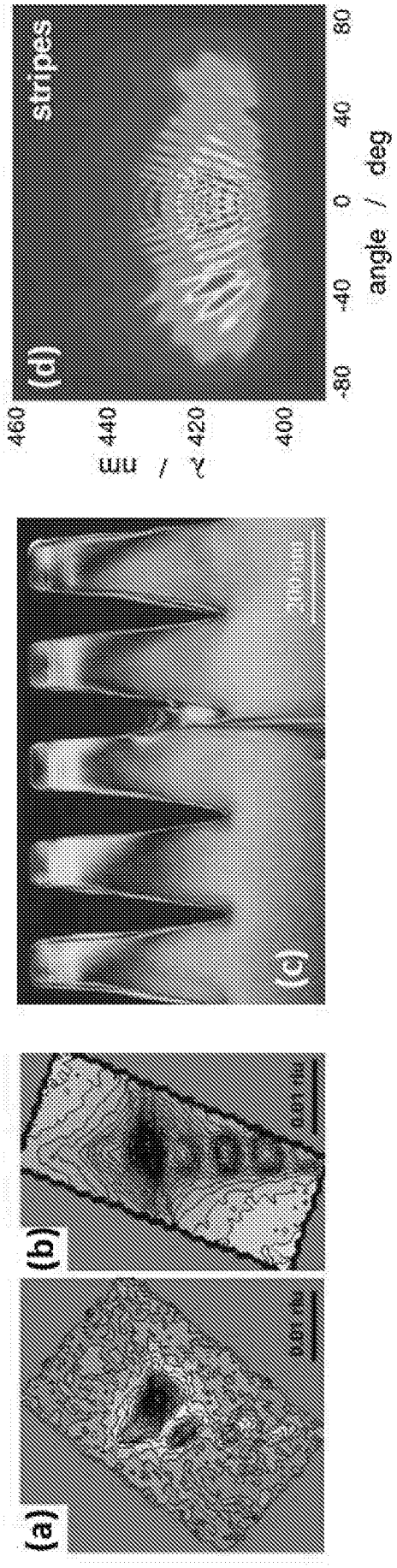


Fig. 2

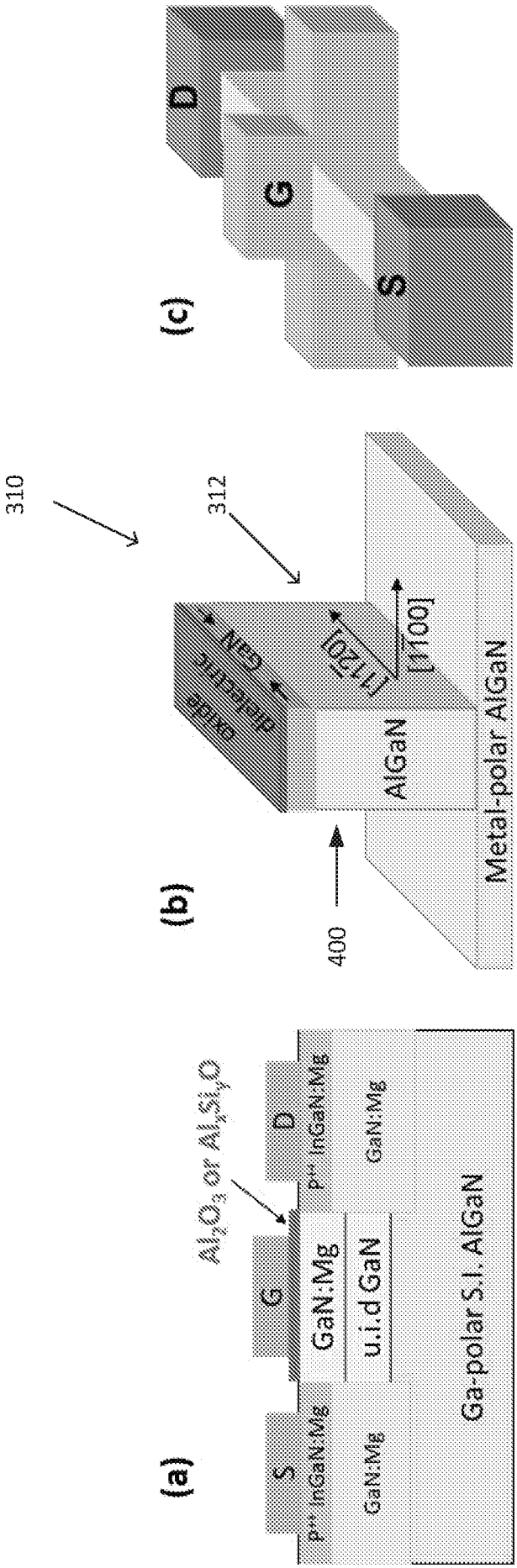

(a)
S
G
D
P++ InGaN:Mg
GaN:Mg
u.i.d GaN
GaN:Mg
P++ InGaN:Mg
Ga-polar S.I. AlGaN
Al_2O_3 or Al_xSi_yO
(b)
310
312
400
Metal-polar AlGaN
AlGaN
[1100]
[0001]
Oxide
Deplete GaN
(c)
S
G
D

Fig. 3

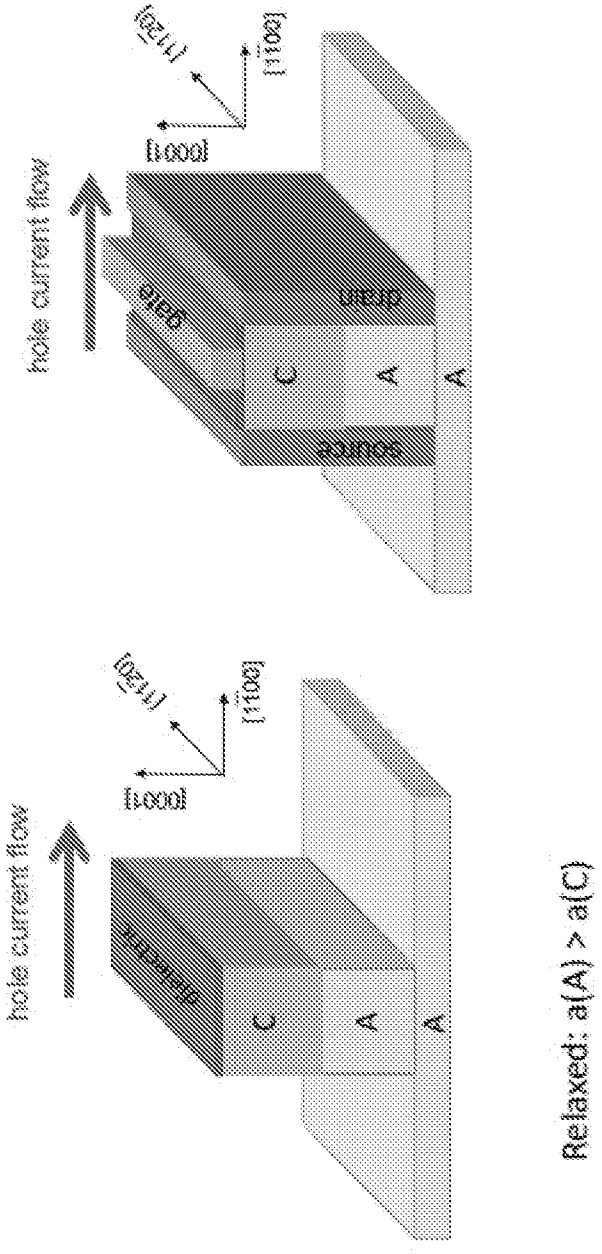
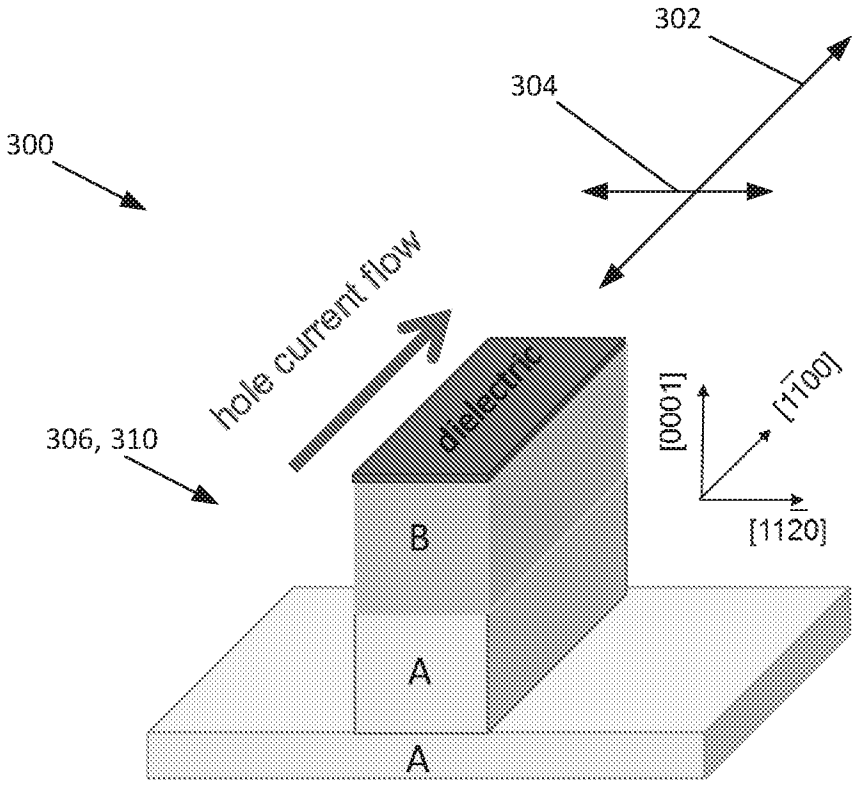

[0001]
[11$\bar{2}$0]
[$\bar{1}$100]
hole current flow
gate
drain
C
A
A
source
[0001]
[11$\bar{2}$0]
[$\bar{1}$100]
hole current flow
source
C
A
A
Relaxed: a(A) > a(C)

Fig. 3d



relaxed: a(A) < a(B)

Fig. 3e

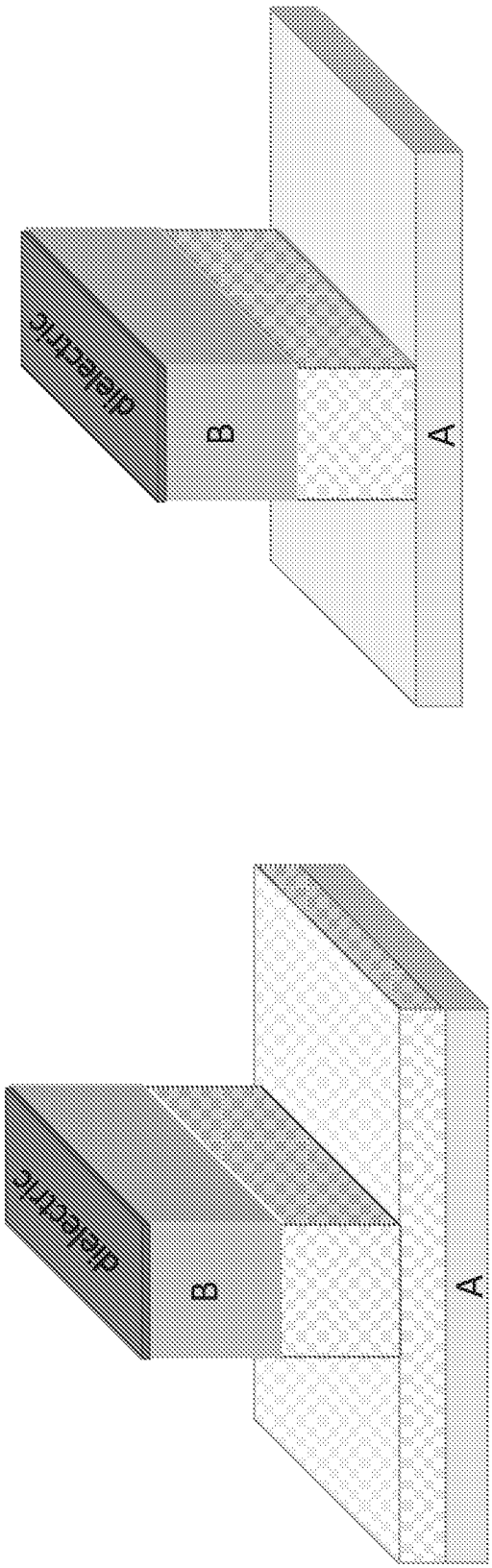


Fig. 3f

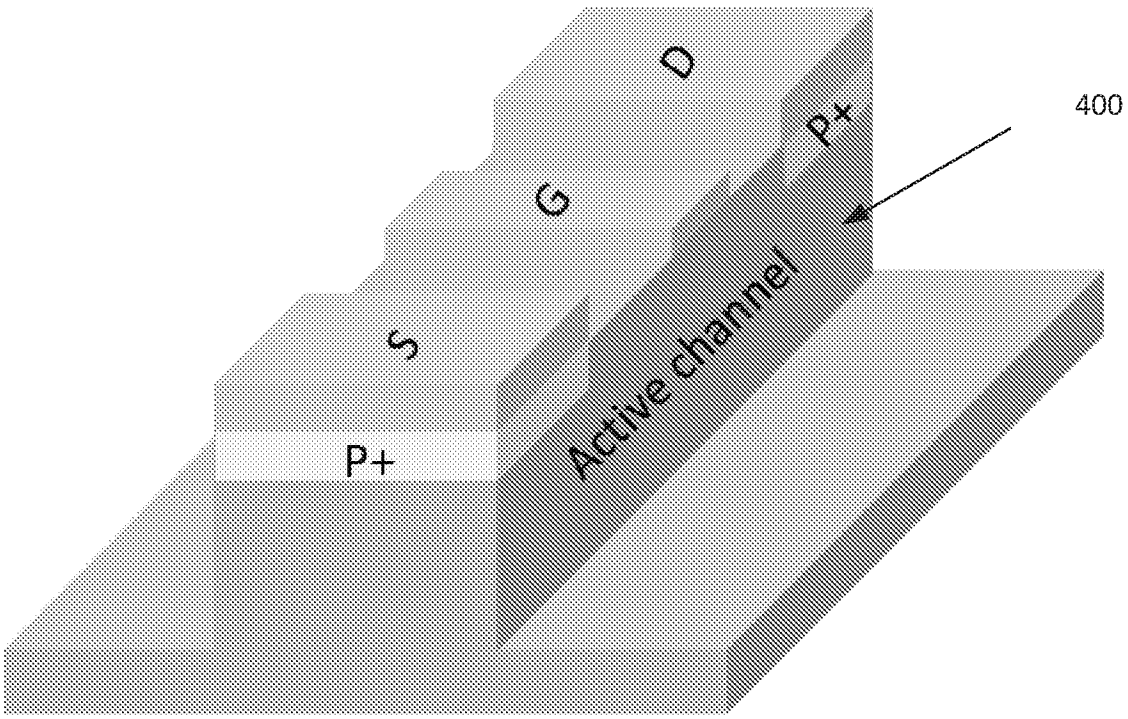


Fig. 4

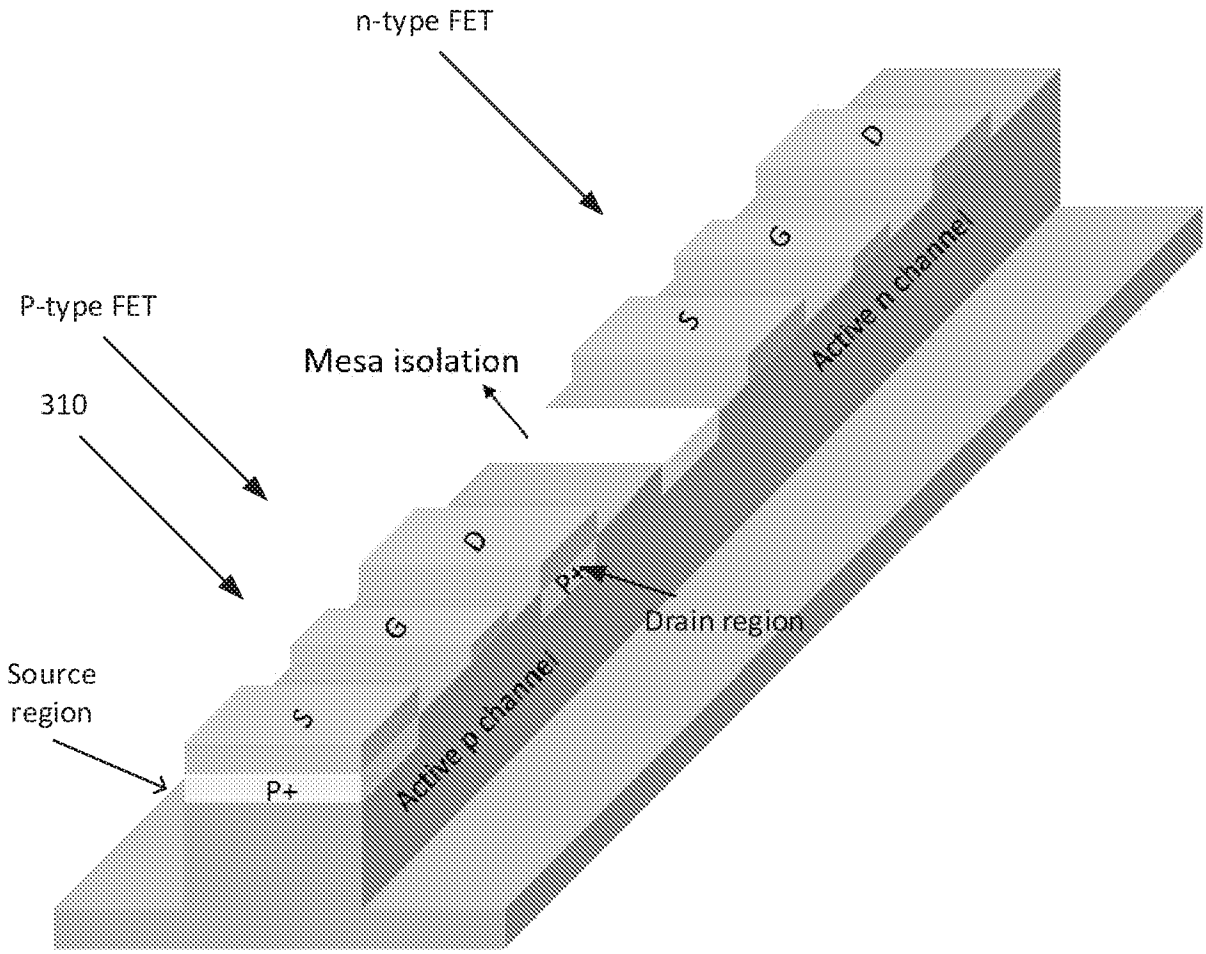

n-type FET
P-type FET
310
Mesa isolation
Source region
S
G
D
Active n channel
P+
Drain region
S
G
D
P+
Active p channel

Fig. 5

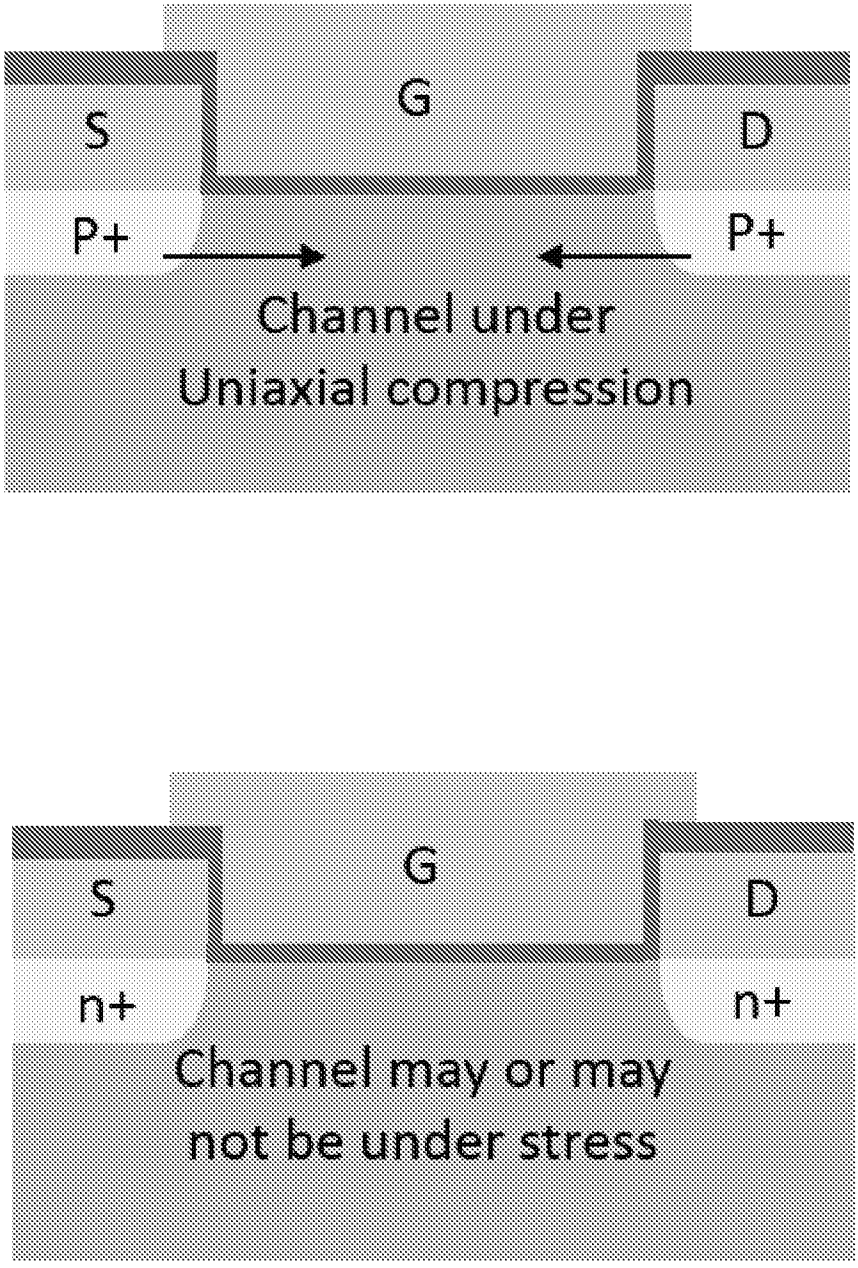

G
S
D
P+
P+
Channel under
Uniaxial compression
G
S
D
n+
n+
Channel may or may
not be under stress

Fig. 6

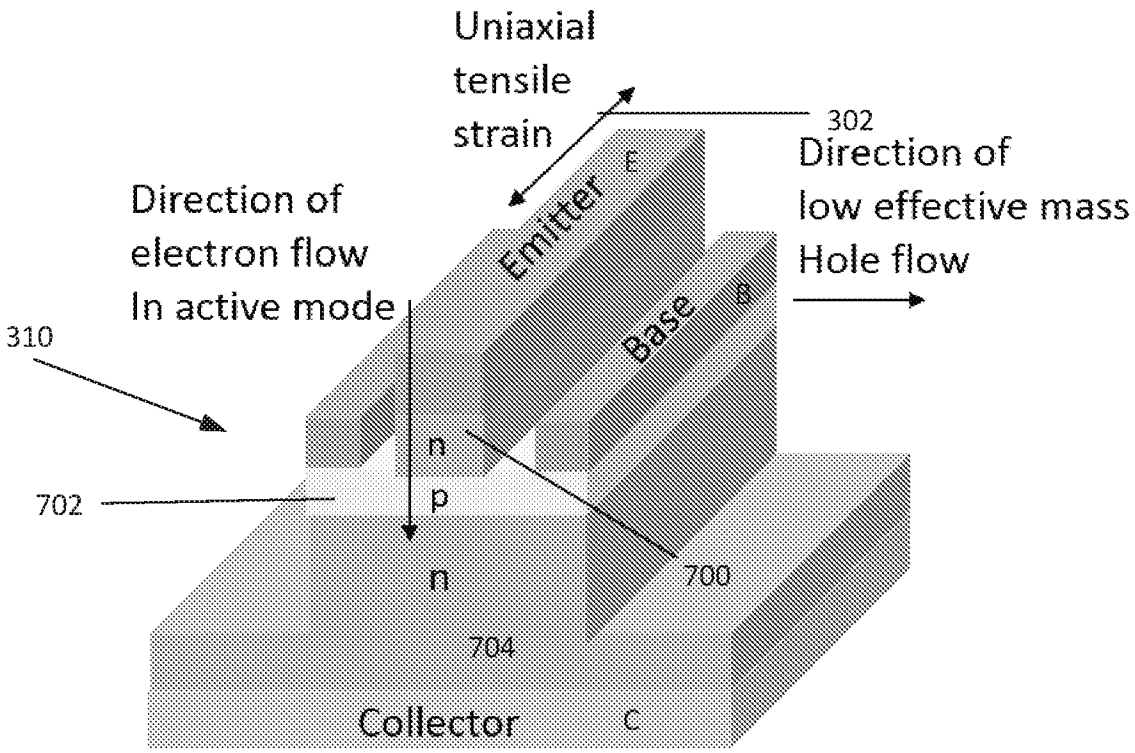

Uniaxial
tensile
strain
302
Direction of
low effective mass
Hole flow
Direction of
electron flow
In active mode
310
Emitter
E
Base
B
n
p
n
702
700
704
Collector
C

Fig. 7

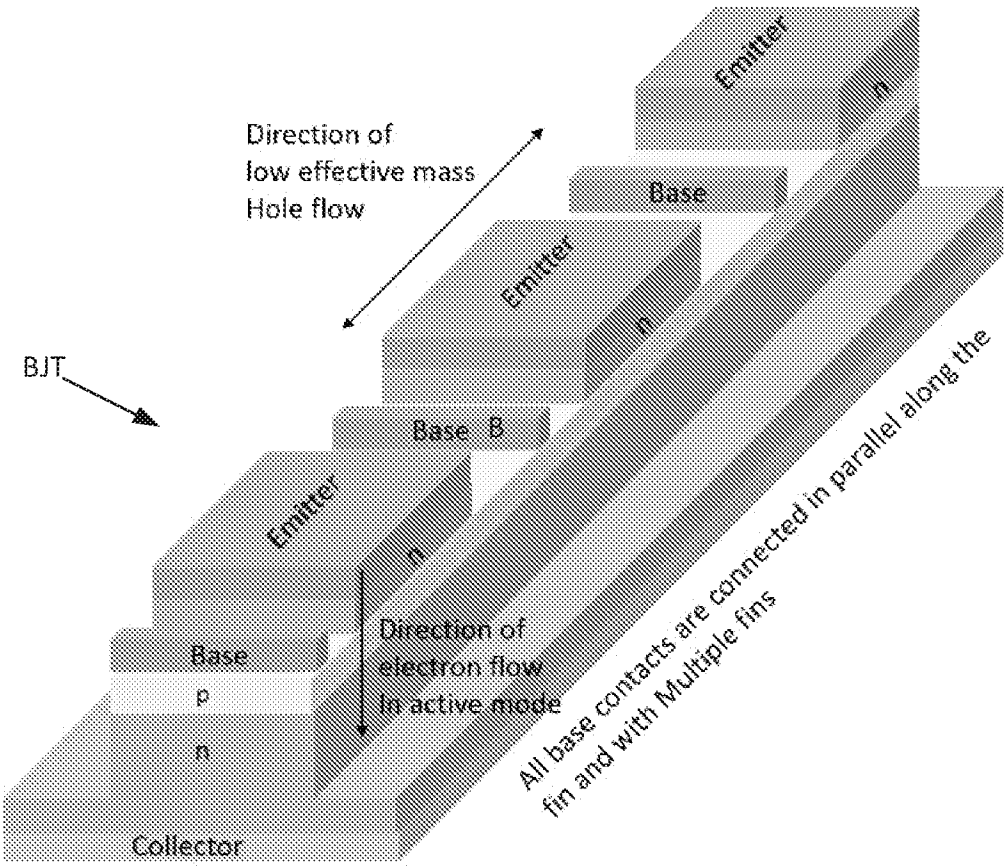

Direction of
low effective mass
Hole flow
BJT
Emitter
n
Base
Emitter
n
Base B
Emitter
n
Direction of
electron flow
In active mode
Base
p
n
Collector
All base contacts are connected in parallel along the
fin and with Multiple fins

Fig. 8A

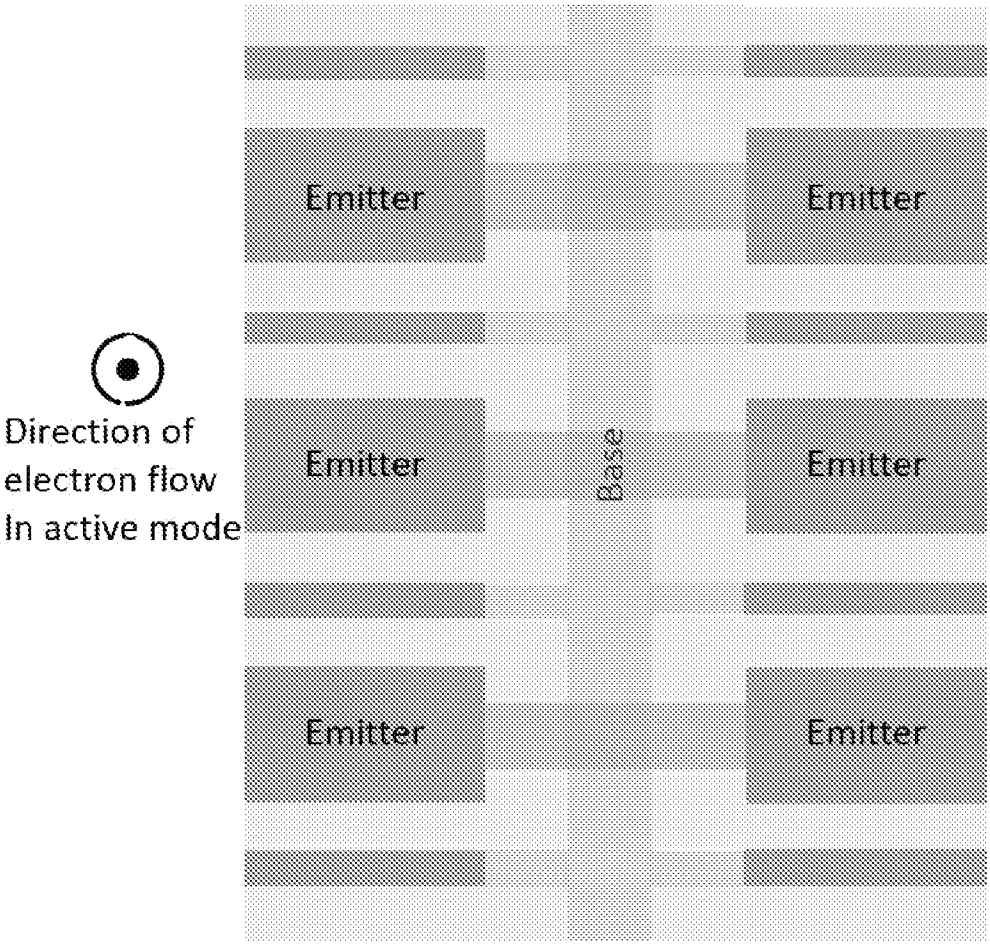

Emitter
Emitter
Direction of
electron flow
In active mode
Emitter
Base
Emitter
Emitter
Emitter
Low capacitance interconnects
are on dielectric

Fig. 8B

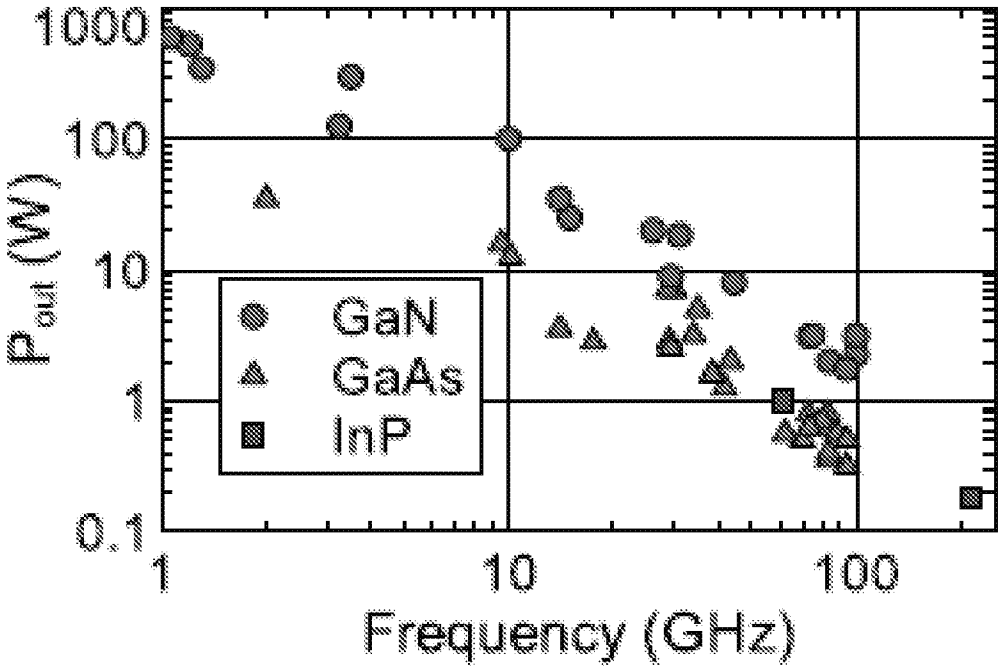


Fig. 9

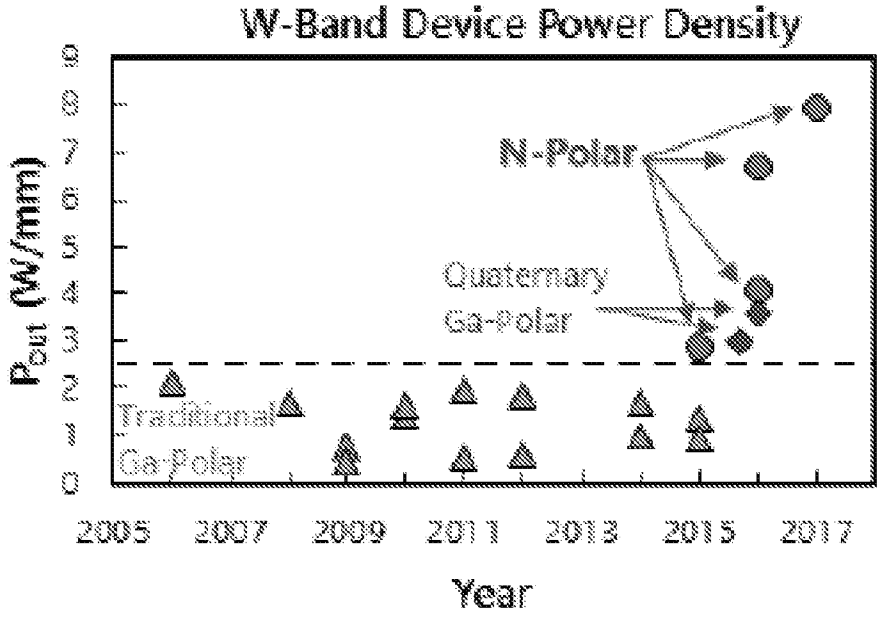

W-Band Device Power Density
P_{out} (W/mm)
N-Polar
Quaternary
Ga-Polar
Traditional
Ga-Polar
2005
2007
2009
2011
2013
2015
2017
Year

Fig. 10

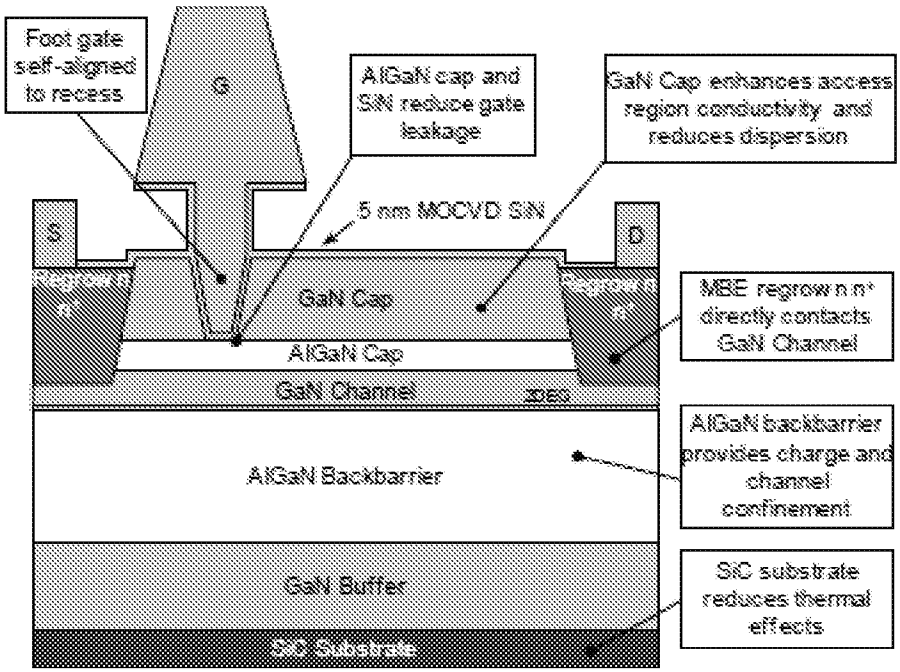

Foot gate self-aligned to recess
G
AlGaN cap and SiN reduce gate leakage
GaN Cap enhances access region conductivity and reduces dispersion
5 nm MOCVD SiN
S
D
GaN Cap
AlGaN Cap
GaN Channel
MBE regrown n+ directly contacts GaN Channel
AlGaN Backbarrier
AlGaN backbarrier provides charge and channel confinement
GaN Buffer
SiC substrate reduces thermal effects
SiC Substrate

Fig. 11

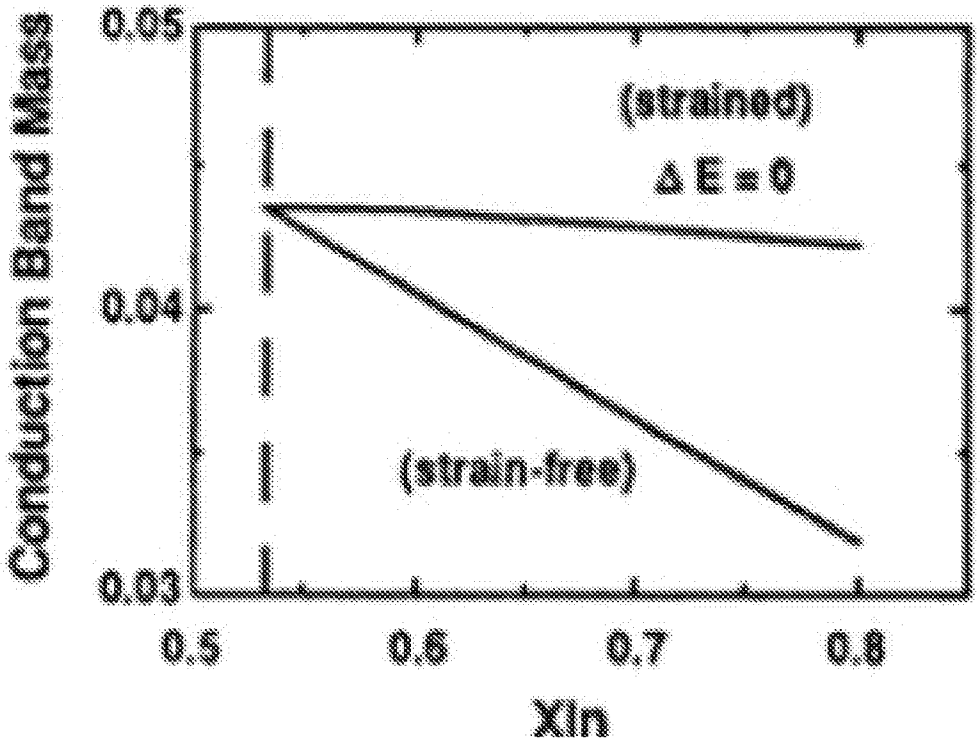

Conduction Band Mass
0.05
0.04
0.03
(strained)
Δ E = 0
(strain-free)
0.5
0.6
0.7
0.8
Xin

Fig. 12

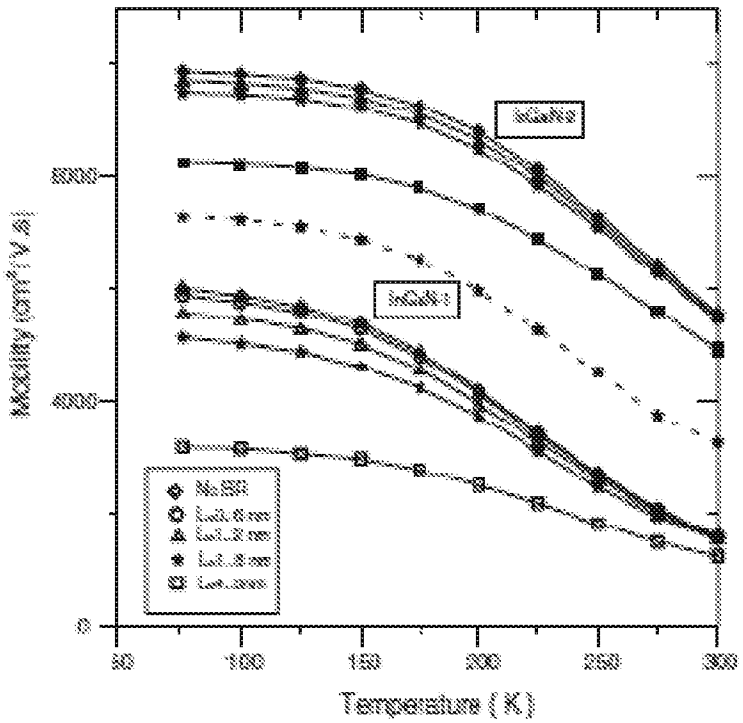

Mobility (cm² / V-s)
8000
4000
0
50
100
150
200
250
300
Temperature (K)

Fig. 13

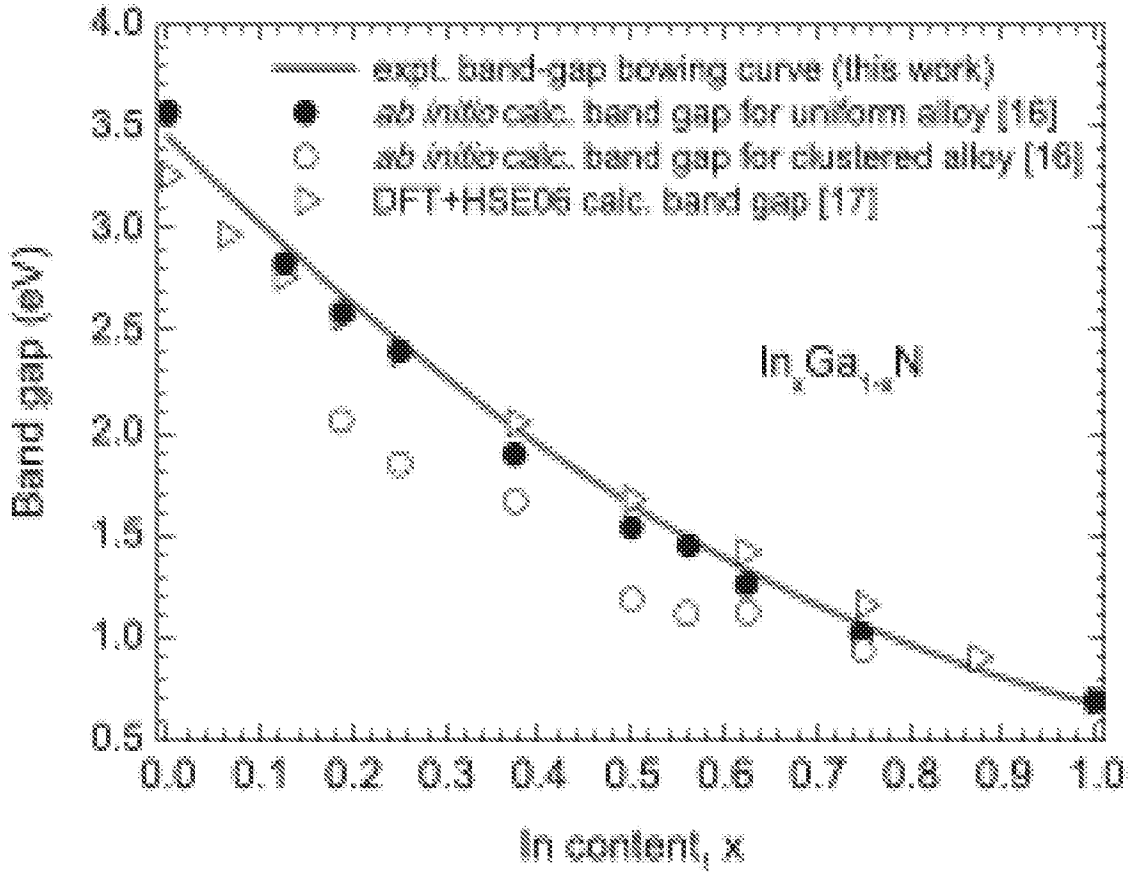

expt. band-gap bowing curve (this work)
ab initio calc. band gap for uniform alloy [16]
ab initio calc. band gap for clustered alloy [16]
DFT+HSE06 calc. band gap [17]
InxGa1-xN
Band gap (eV)
In content, x
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0

Fig. 14

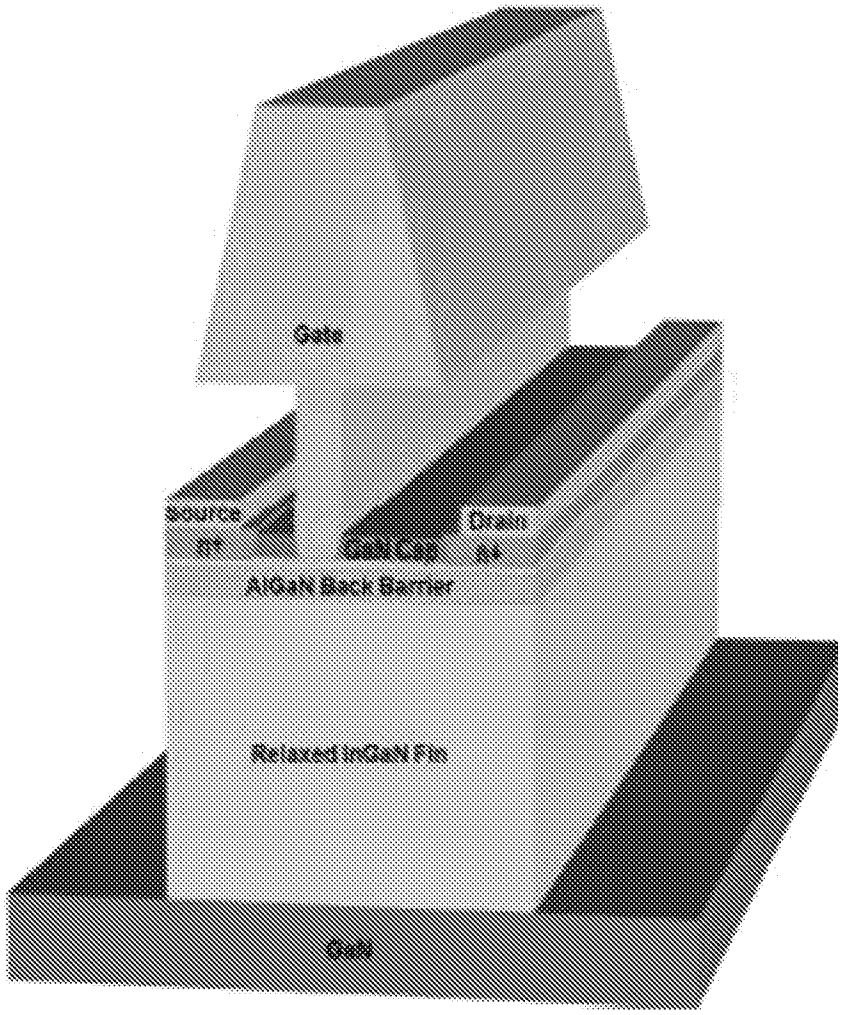

Gate
Source
n+
Drain
n+
AlGaN Back Barrier
Relaxed InGaN Fin
GaN

Fig. 15

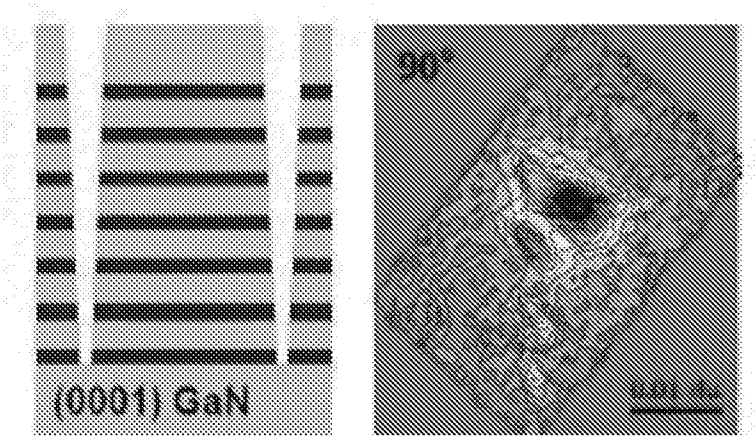


Fig. 16

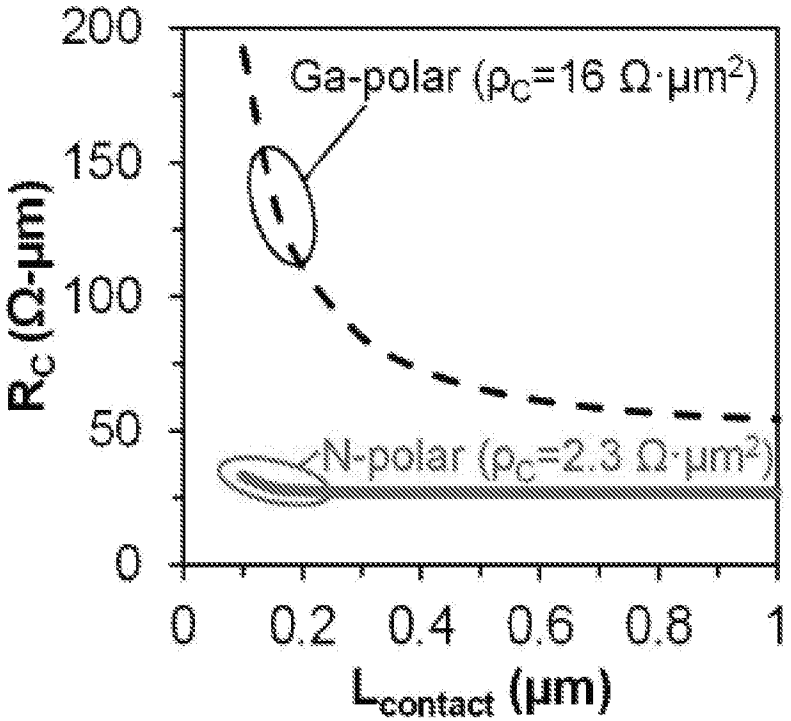

200
150
100
50
0
R_C (Ω-μm)
Ga-polar (ρ_C=16 Ω·μm^2)
N-polar (ρ_C=2.3 Ω·μm^2)
0
0.2
0.4
0.6
0.8
1
$L_{contact}$ (μm)

Fig. 17

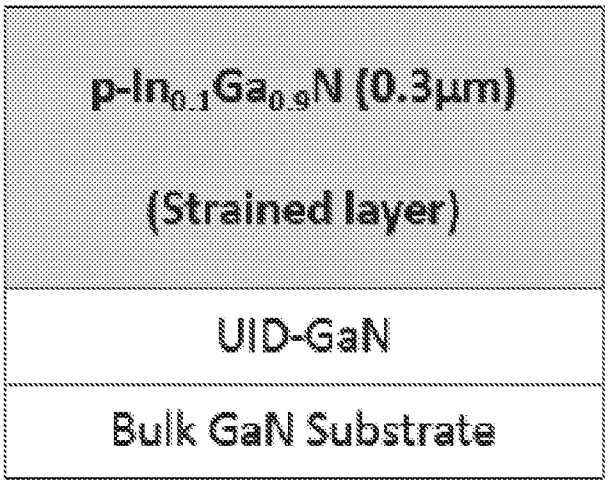


Fig. 18

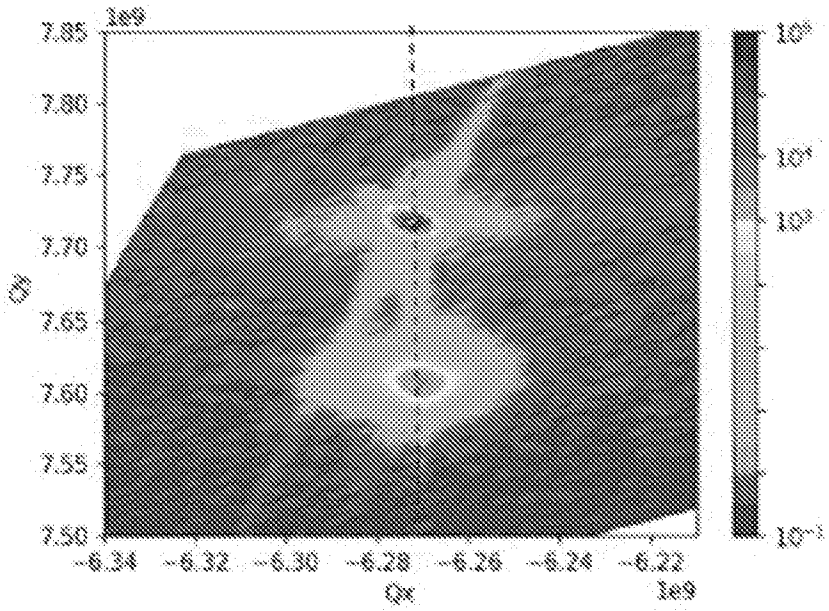

1e9
7.85
7.80
7.75
7.70
7.65
7.60
7.55
7.50
Qy
−6.34
−6.32
−6.30
−6.28
−6.26
−6.24
−6.22
Qx
1e9

Fig. 19

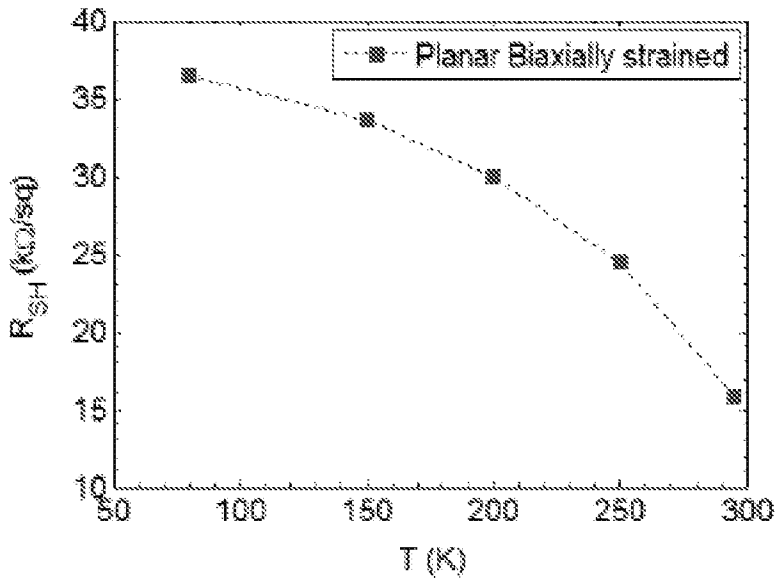

Planar Biaxially strained
R_{SH} (kΩ/sq)
T (K)
40
35
30
25
20
15
10
50
100
150
200
250
300

Fig. 20

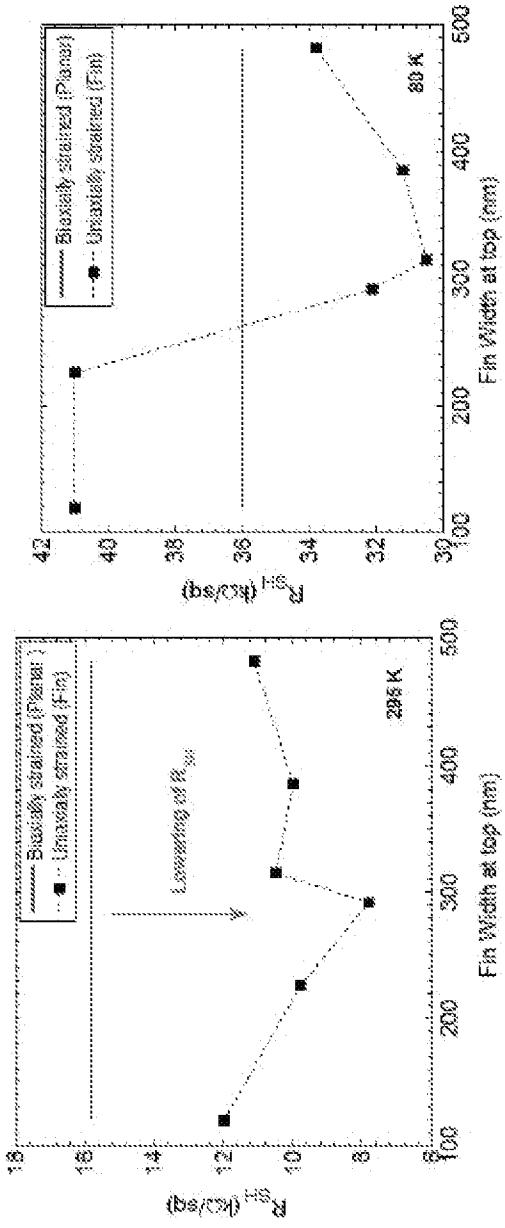
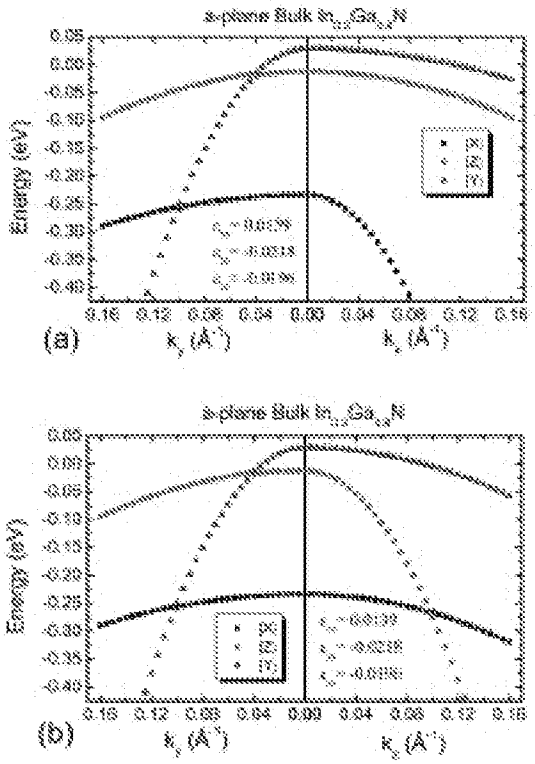

Biaxially strained (Planar)
Uniaxially strained (Fin)
80 K
296 K
Lowering of R_{SH}
R_{SH} (kΩ/sq)
Fin Width at top (nm)

Fig. 21

J. Appl. Phys. 106, 023106 (2009)



(Color online) The valence band structure under strained condition of a-plane bulk $In_{0.3}Ga_{0.7}N$ material along (a) the k_z direction and the k_y direction and (b) along the k_y direction and the k_z direction.

Fig. 22

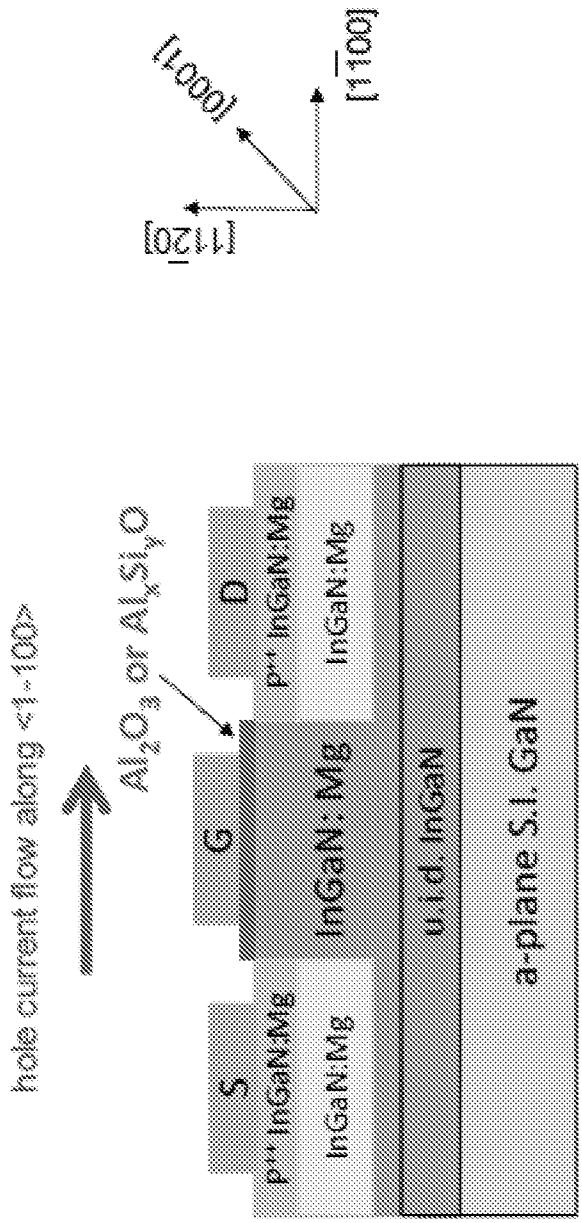

[0001]
[11$\bar{2}$0]
[1$\bar{1}$00]
hole current flow along <1-100>
Al_2O_3 or Al_xSi_yO
S
G
D
p^{++} InGaN:Mg
InGaN:Mg
InGaN: Mg
u.i.d. InGaN
a-plane S.I. GaN

Fig. 23

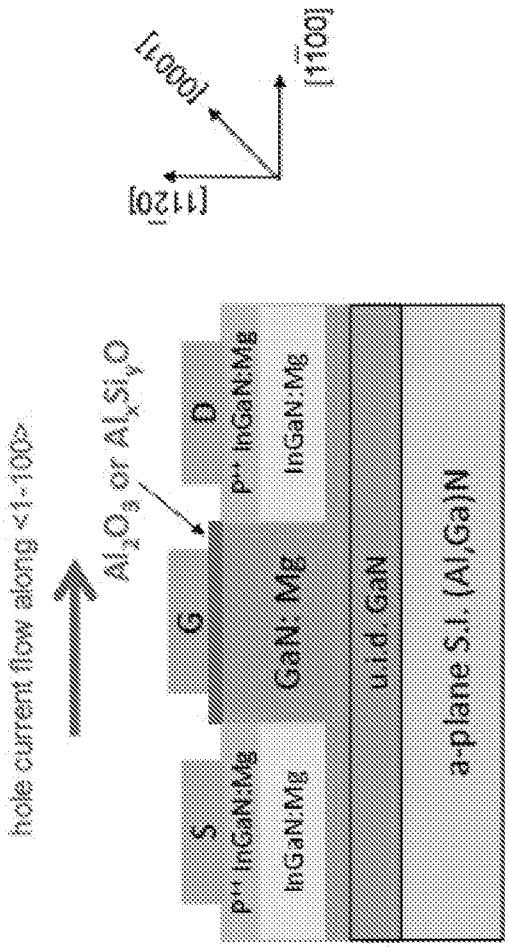

[0001]
[1120]
[01$\bar{1}$0]
hole current flow along <1-100>
Al_2O_3 or Al_xSi_yO
S
G
D
P++ InGaN:Mg
InGaN:Mg
GaN: Mg
u.i.d. GaN
a-plane S.I. (Al,Ga)N

Fig. 24

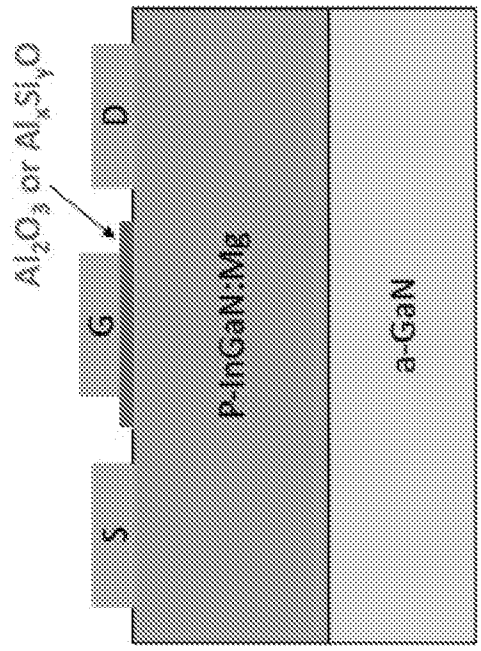


Fig. 25A

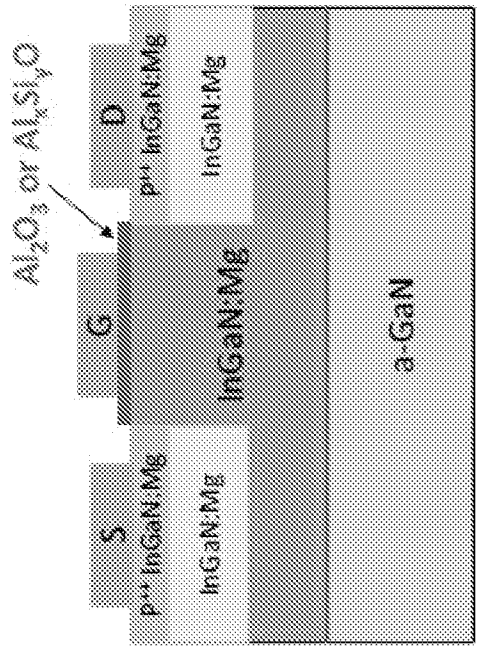


Fig. 25B

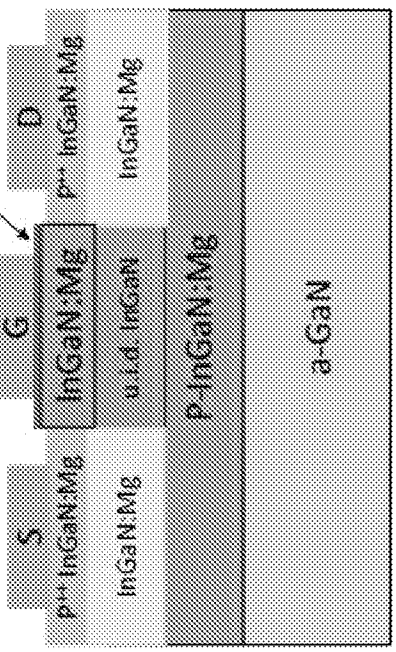


Fig. 26

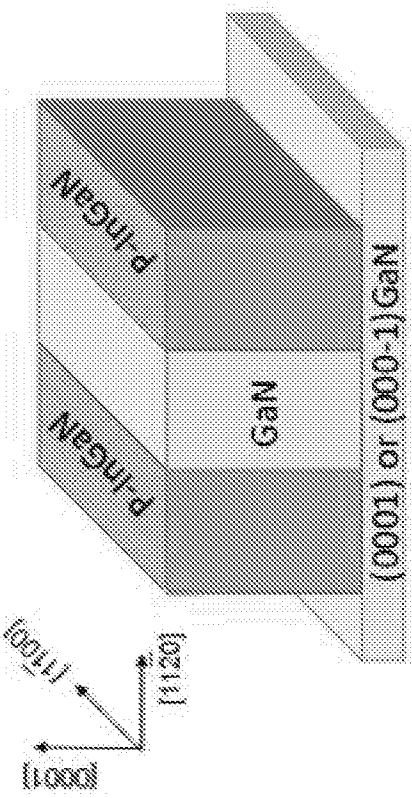


Fig. 27

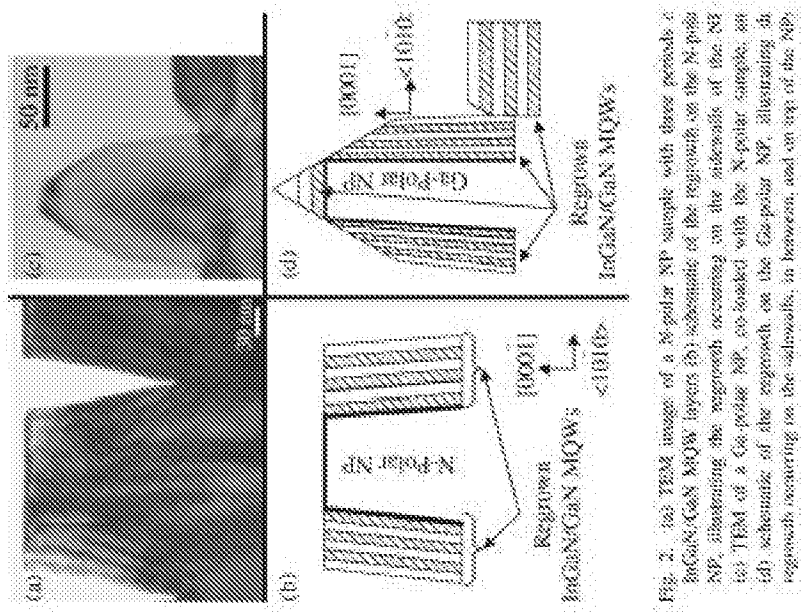
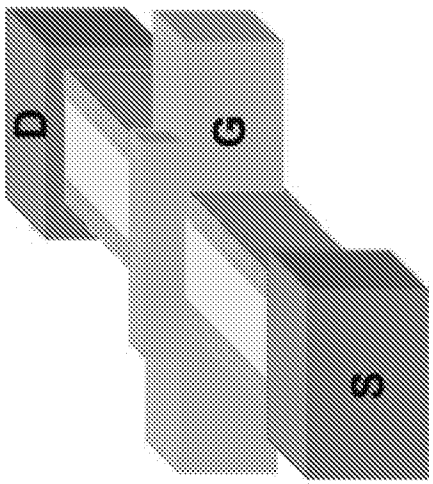


Fig. 2. (a) TEM image of a N-polar NP sample with three periods of InGaN/GaN MQW layers (b) schematic of the regrowth on the N-polar NP, illustrating the regrowth occurring on the sidewalls of the NP (c) TEM of a Ga-polar NP, co-loaded with the N-polar sample, and (d) schematic of the regrowth on the Ga-polar NP, illustrating the regrowth occurring on the sidewalls, in between, and on top of the NP

Fig. 28

Fig. 29



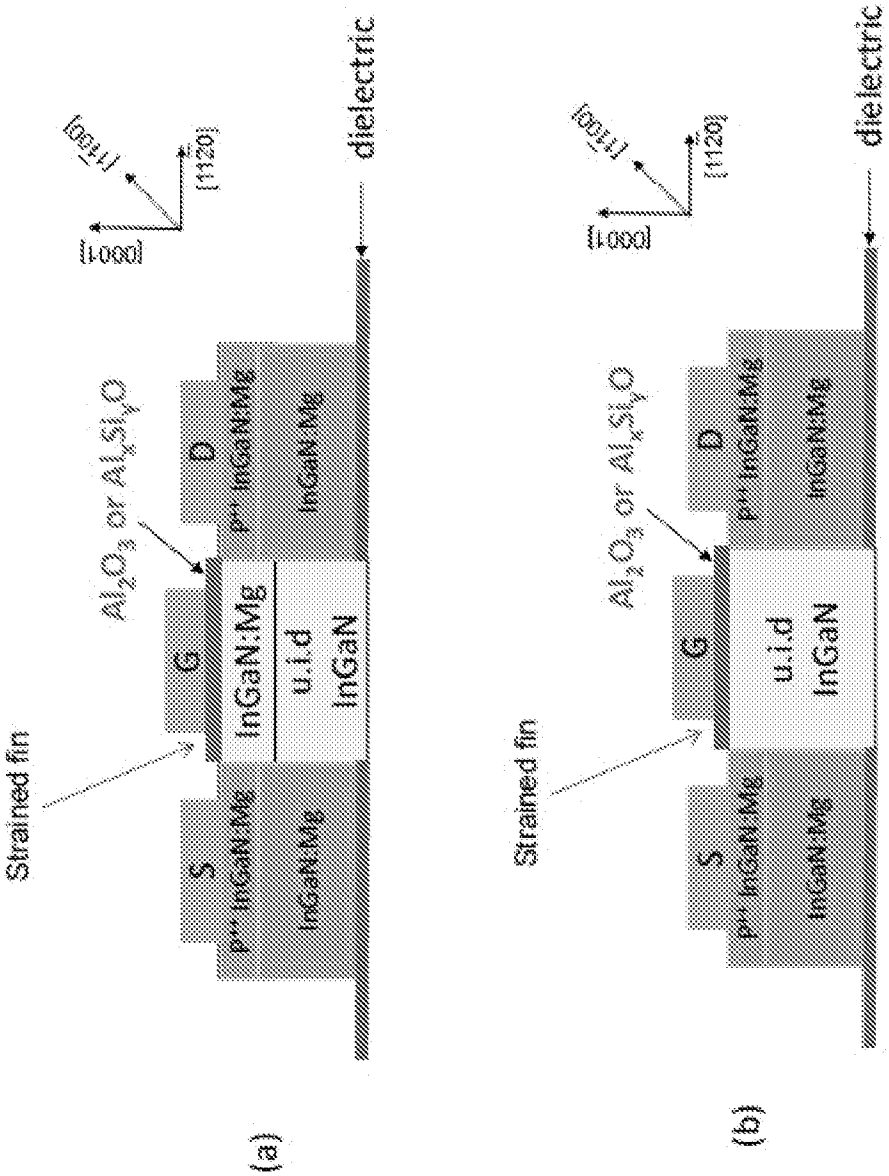
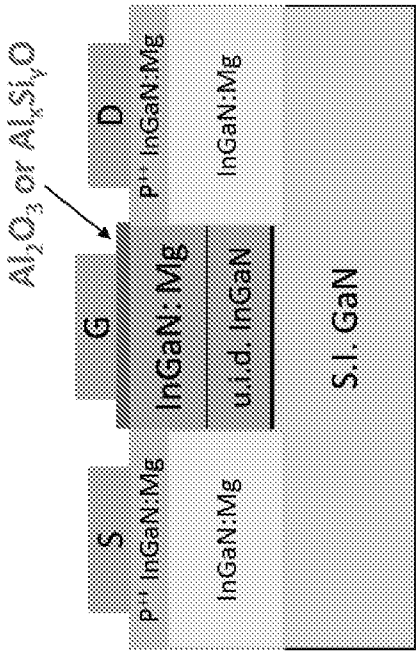
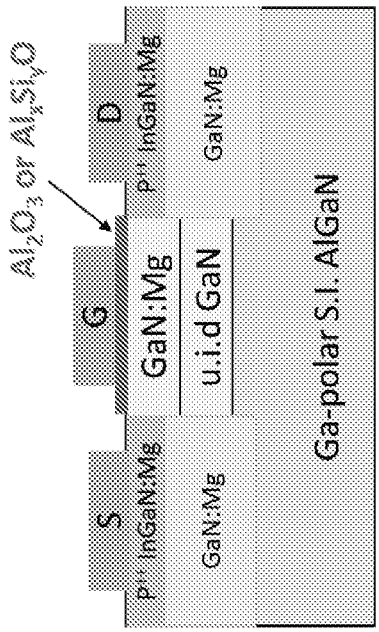

Strained fin
S
P++ InGaN:Mg
InGaN:Mg
G
Al_2O_3 or Al_xSi_yO
InGaN:Mg
u.i.d
InGaN
D
P++ InGaN:Mg
InGaN:Mg
dielectric
[0001]
[1120]
[1-100]
(a)
Strained fin
S
P++ InGaN:Mg
InGaN:Mg
G
Al_2O_3 or Al_xSi_yO
u.i.d
InGaN
D
P++ InGaN:Mg
InGaN:Mg
dielectric
[0001]
[1120]
[1-100]
(b)

Fig. 30


Al_2O_3 or Al_xSi_yO
S
G
D
P++ InGaN:Mg
InGaN:Mg
InGaN:Mg
u.i.d. InGaN
S.I. GaN

(b)


Al_2O_3 or Al_xSi_yO
S
G
D
P++ InGaN:Mg
GaN:Mg
GaN:Mg
u.i.d GaN
GaN:Mg
Ga-polar S.I. AlGaN

(a)

Fig. 31

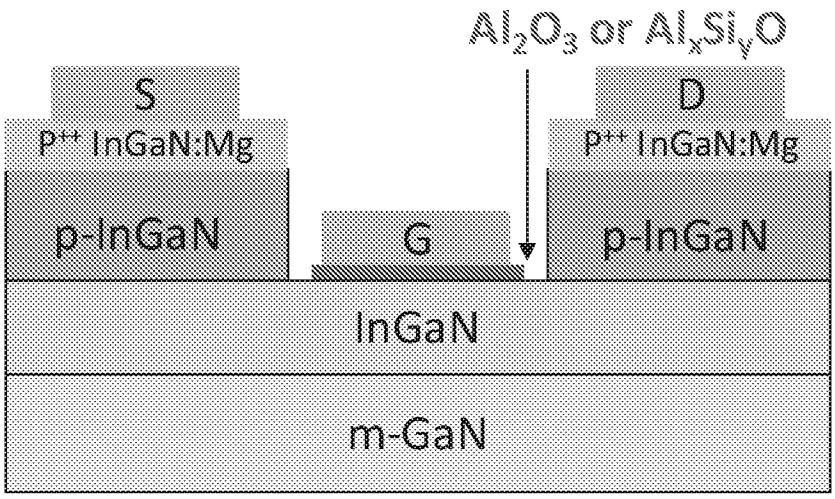
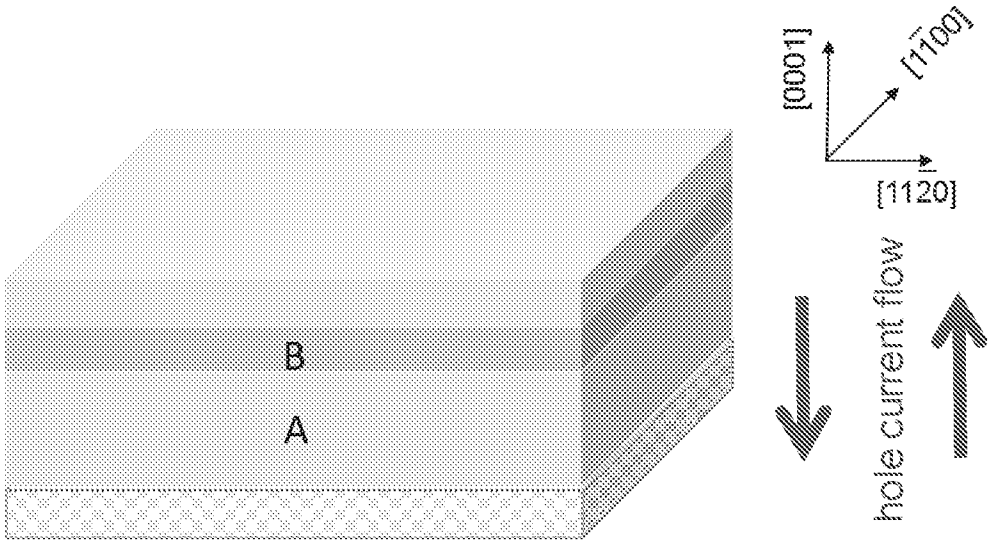

Al_2O_3 or Al_xSi_yO
S
D
P++ InGaN:Mg
P++ InGaN:Mg
p-InGaN
G
p-InGaN
InGaN
m-GaN

Fig. 31C



relaxed: a(A) > a(B), e.g. A=(In,Ga)N, B=GaN

Fig. 32

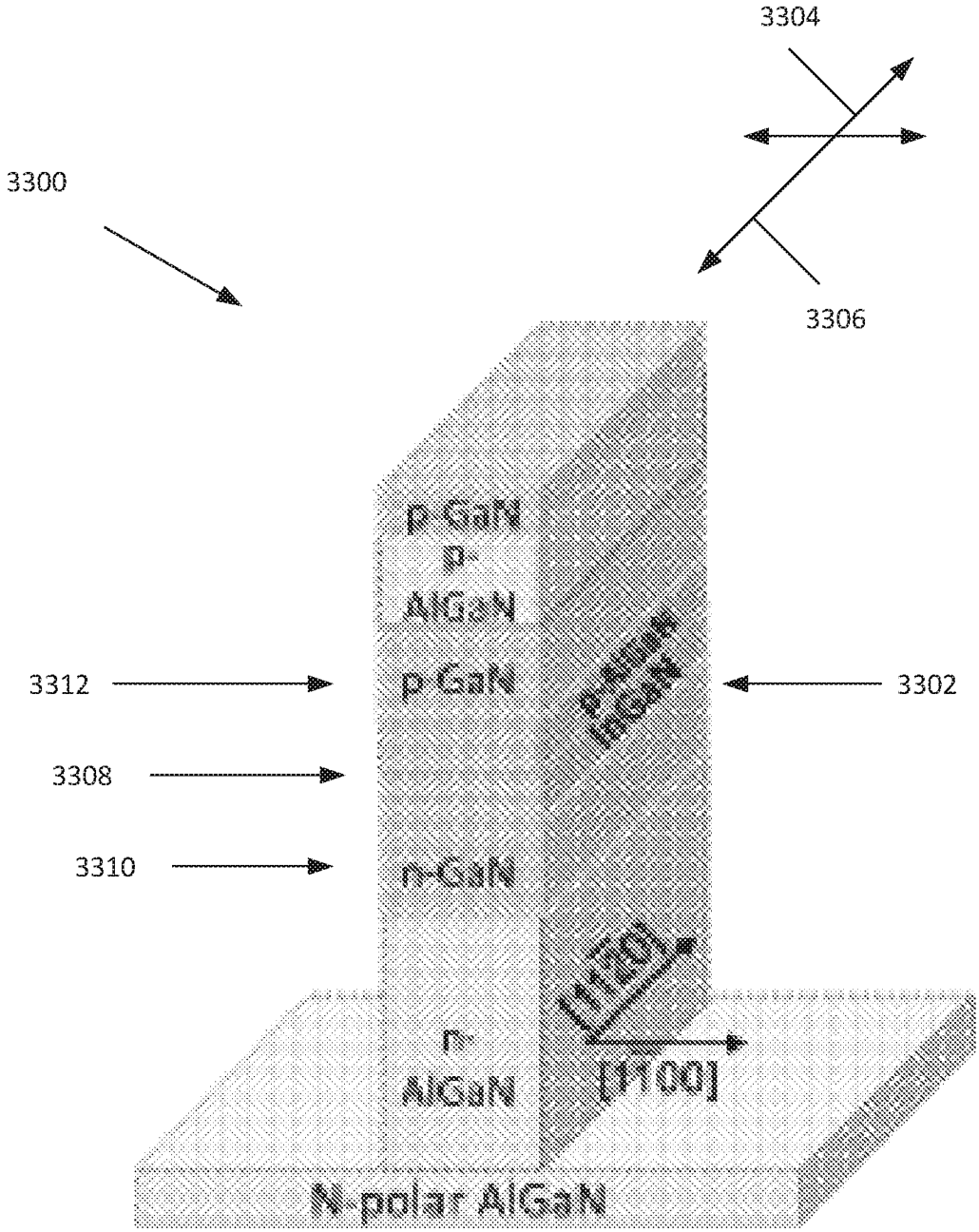

3304
3300
3306
p-GaN
p-
AlGaN
3312
p-GaN
3302
3308
3310
n-GaN
n-
AlGaN
[1100]
N-polar AlGaN

Fig. 33

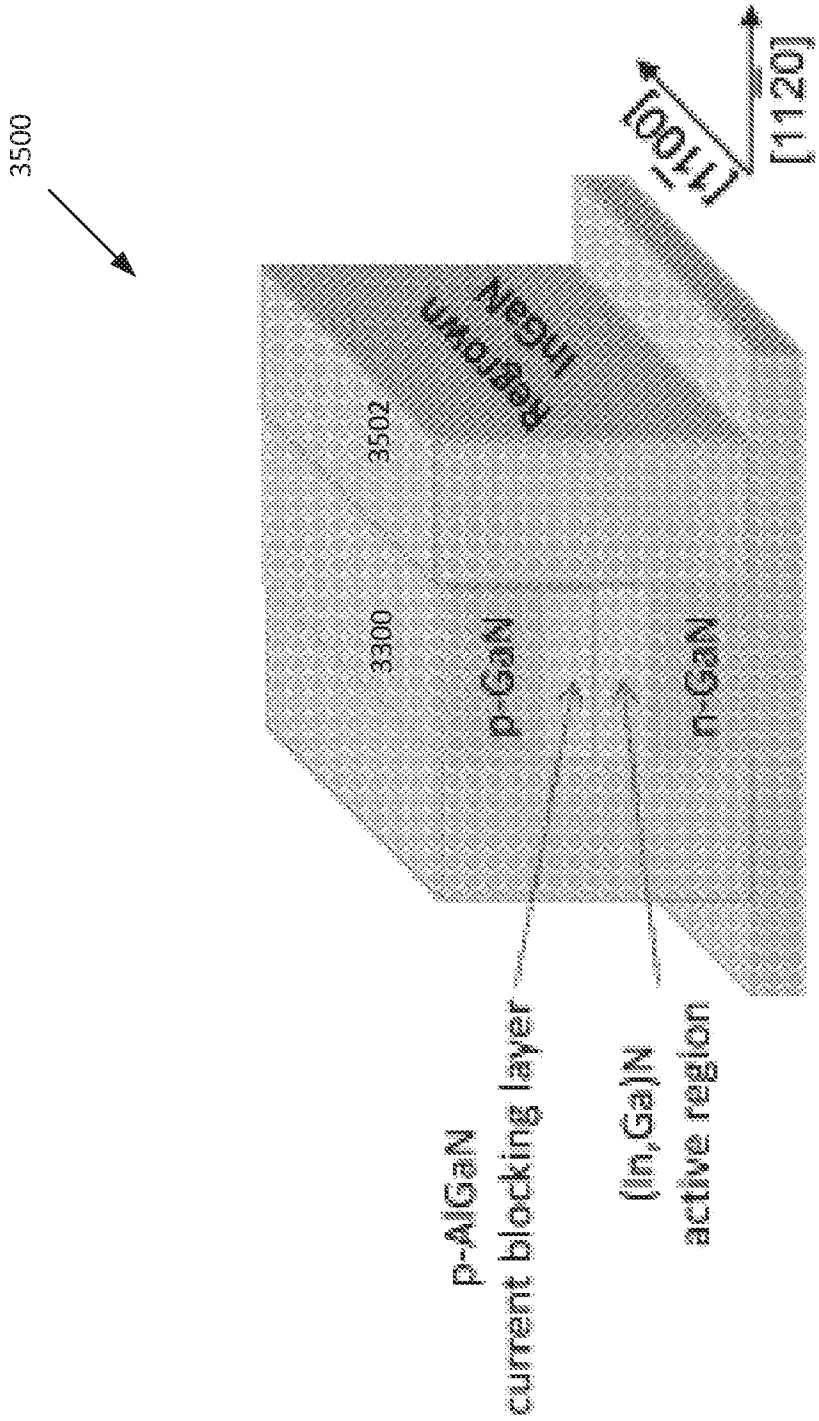

3500
[1120]
[1-100]
Mesa
3502
3300
p-GaN
n-GaN
p-AlGaN
current blocking layer
(In,Ga)N
active region

Fig. 34

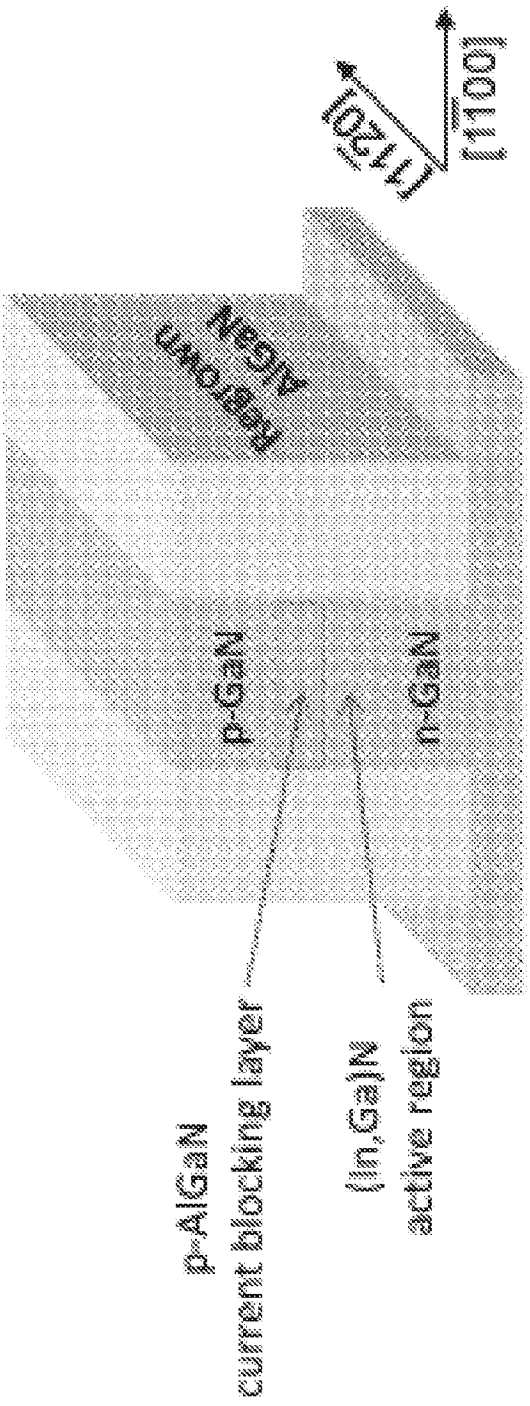

[1101]
[10$\bar{1}$4]
Recessed window
p-GaN
n-GaN
p-AlGaN
current blocking layer
(In,Ga)N
active region

Fig. 35

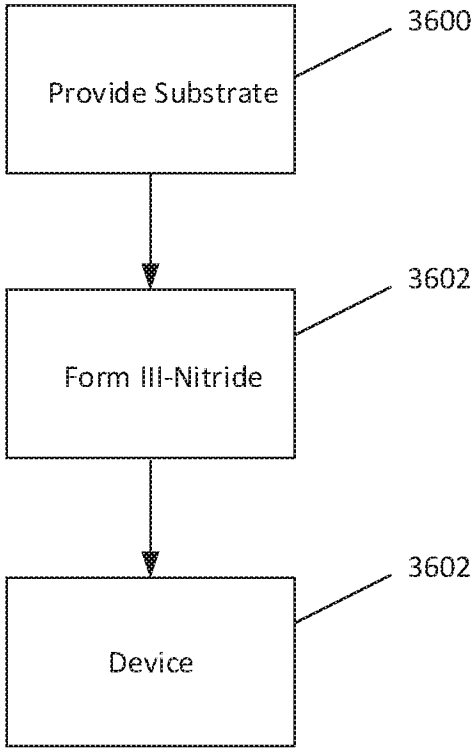


Fig. 36