(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 December 2018 (20.12.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/232267 A1

(51) International Patent Classification:
H01H 85/12 (2006.01) *H01H 85/04* (2006.01)
H01H 85/00 (2006.01) *H02B 1/18* (2006.01)
H01H 85/02 (2006.01)

(21) International Application Number:
PCT/US2018/037794

(22) International Filing Date:
15 June 2018 (15.06.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/625,191 16 June 2017 (16.06.2017) US

(71) Applicant: **LITTELFUSE, INC.** [US/US]; 8755 West Higgins Road, Suite 500, Chicago, Illinois 60631 (US).

(72) Inventors: **PINEDA, Martin**; 285 Mortimer Avenue, Fremont, California 94536 (US). **BHATAWADEKAR, Kedar**; 450 Harvard Avenue, Apt. 1Q, Santa Clara, California 95051 (US). **YU, Dong**; 2081 Dome Place, Fremont, California 94539 (US).

(74) Agent: **DAISAK, Daniel N.** et al.; 101 Carnegie Center, Suite 106, Princeton, New Jersey 08540 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: ELECTRICAL CIRCUIT PROTECTION DEVICE WITH HIGH RESISTIVE BYPASS MATERIAL

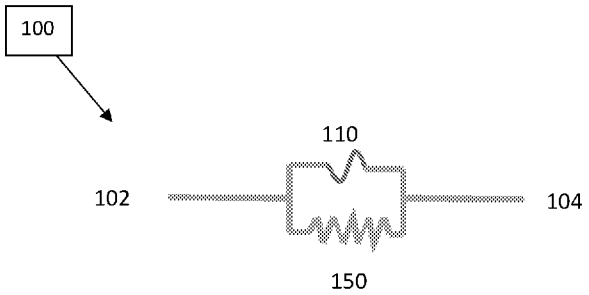


FIG. 1

(57) Abstract: A fuse suitable for arc quenching is disclosed. The fuse incorporates a high-resistive material or element placed in parallel relationship with the fusible element to mitigate, minimize and/or prevent arcing during an overcurrent condition. By incorporating a high-resistive material or element in parallel with a fusible element an alternate or second path for current flow during an overcurrent condition is provided. As such, during normal operating conditions, current travels through the fusible element. However, during an overcurrent condition, the resistance through the fusible element increases. Once the resistance through the fusible element is greater than the resistance through the high-resistive material or element, the current will bypass the fusible element and travel through the high-resistive material or element. In this manner, arcing through the fusible element during the overcurrent condition can be prevented or minimized.

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ELECTRICAL CIRCUIT PROTECTION DEVICE WITH HIGH RESISTIVE BYPASS MATERIAL

Cross References to Related Applications

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 15/625,191, filed June 16, 2017, which is incorporated by reference herein in its entirety.

FIELD OF THE DISCLOSURE

[0002] The disclosure relates generally to the field of fuses (e.g., electrical circuit protection devices) for protection against overcurrent conditions and more particularly to a fuse, such as, for example, a surface-mountable electrical circuit protective device having a high resistive material in parallel with a fusible element.

BACKGROUND OF THE DISCLOSURE

[0003] Fuses, which are commonly used as electrical circuit protection devices, provide electrical connections between sources of electrical power and circuit components that are to be protected. Upon the occurrence of a specified fault condition in a circuit, such as an overcurrent condition, a fusible element can melt, or otherwise separate, to interrupt current flow in the circuit path. Protected portions of the circuit are thereby electrically isolated and damage to such portions may be prevented or at least mitigated.

[0004] One known issue with existing fuses is that the current may arc across the fusible element during a clearing time, which may result in additional damage to the downstream circuit components. In addition, such arcing prevents fuses from obtaining significantly higher safety ratings.

[0005] Thus, a need exists for an improved fuse that prevents or minimizes arcing. It is with respect to these and other considerations that the present improvements have been needed.

SUMMARY

[0006] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended as an aid in determining the scope of the claimed subject matter.

[0007] Various embodiments are generally directed to a fuse that utilizes both a fusible element and a high-resistive material disposed in layers of a chip fuse.

[0008] In accordance with the present disclosure, a fuse is disclosed that includes a fusible element having a first electrical resistance, and a high-resistive material having a second electrical resistance where the high-resistive material is in a parallel relationship with the fusible element. During a normal operating condition, the first electrical resistance is less than the second electrical resistance such that current flows through the fusible element. During an overcurrent condition, the first electrical resistance is greater than the second electrical resistance such that current flows through the high-resistive material. As mentioned, the fuse may be in the form of a chip fuse having a plurality of non-conductive layers wherein the fusible element is disposed between adjacent layers of the plurality of non-conductive layers and the high-resistive material is also disposed between adjacent layers of the plurality of non-conductive layers such that at least one of the plurality of non-conductive layers is disposed between the fusible element and the

high-resistive material. A substrate upon which the fusible element, high-resistive material and plurality of non-conductive layers are disposed is also included in the chip fuse configuration.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] By way of example, specific embodiments of the disclosed device will now be described, with reference to the accompanying drawings, in which:

[0010] **FIG. 1** is a schematic illustration of an exemplary embodiment of a fuse according to the present disclosure;

[0011] **FIG. 2** is a side view illustrating an exemplary embodiment of a chip fuse according to the present disclosure;

[0012] **FIG. 3** is an exploded perspective view of the chip fuse shown in **FIG. 2**;

[0013] **FIG. 4** is a side view illustrating an alternate, exemplary embodiment of a chip fuse according to the present disclosure;

[0014] **FIG. 5** is an exploded perspective view of the chip fuse shown in **FIG. 4**;

[0015] **FIG. 6** is a perspective view illustrating an alternate, exemplary embodiment of a fuse according to the present disclosure; and

[0016] **FIG. 7** is a flow diagram of a method for manufacturing a chip fuse, all arranged in accordance with at least some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0017] The present disclosure will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments are shown. This disclosure, however, may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, like numbers refer to like elements throughout.

[0018] Referring to **FIG. 1**, according to one aspect of the present disclosure, a fuse or an electrical circuit protection device (collectively referred to herein as a fuse without the intent to limit) 100 is disclosed. As shown, the fuse 100 may include an input 102, an output 104, a fusible element 110, and a high-resistive element or material 150 (collectively referred to herein as a high-resistive material without the intent to limit). In use, the fuse 100 includes a high-resistive material 150 placed in a parallel relation relationship with a fusible element 110 to mitigate, minimize and/or prevent arcing during an overcurrent condition. That is, by placing a high-resistive material 150 in parallel with a fusible element 110, an arc quenching system is created wherein the electrical current is provided with an alternate, second path to flow during an overcurrent condition (e.g., during a fuse opening event) thus facilitating an arc-less operation as the electrical circuit is being de-energized. In one embodiment, the high-resistive material 150 may be as high as 200kΩ at room temperature. Alternatively, the high-resistive material 150 may have values in the range of, for example, 0.2kΩ - 200 kΩ and is dependent on the particular application.

[0019] As previously mentioned, during an overcurrent condition, the fusible element 110 may be exposed to higher currents including currents exceeding normal operating ranges. As such, the fusible element 110 may melt, or otherwise separate, to interrupt current flow in the circuit path to thereby electrically isolate and protect downstream portions of the circuit. However, during the clearing time, the current may arc across the melted or separated fusible element 110. Generally, the clearing time refers to the total amount of open time of the fuse, or the time from the occurrence of an electrical overstress (EOS) to the time the fuse prevents current flow. The clearing time may include the total amount of time for the fusible element to melt and/or separate, plus the amount of time arcing occurs. The arc continues until the gap created by the fusible element melting or separating is large enough to prevent the arc.

[0020] As will be appreciated by one of ordinary skill in the art, in a DC circuit, current travels through the path of least resistance. As such, during normal operating conditions, current travels through the fusible element 110 with the high-resistive material 150 having no affect. This is because, during normal operating conditions, the fusible element 110 has a first electrical resistance that is less than a second electrical resistance of the high-resistive material 150. However, during an overcurrent condition, the resistance through the fusible element 110 increases. Once the resistance through the fusible element 110 is greater than the resistance through the high-resistive material 150 (e.g., once the second electrical resistance of the high-resistive material is less than the first electrical resistance of the fusible element), the current will bypass the fusible element 110 and travel through the high-resistive material 150. In this manner, by properly selecting

and designing the high-resistive material 150, arcing through the fusible element 110 during an overcurrent condition can be prevented or minimized.

[0021] As will be described in greater detail below, the fuse 100 including the fusible element 110 and the high-resistive material 150 may be incorporated into a single housing, body or enclosure. Alternatively, the fusible element 110 and the high-resistive material 150 may be separate and distinct from one another. In any event, the fusible element 110 and the high-resistive material 150 may be arranged in a parallel relationship with each other so that in a first, normal operating condition, current flows through the fusible element 110, while in a second, overcurrent condition, current bypasses the fusible element 110 and travels through the high-resistive material 150.

[0022] In addition, as will be described in greater detail below, the present invention will be described and illustrated in conjunction with a chip fuse, also known as a thin-film fuse, a surface-mount fuse, or SMD fuses. Chip fuses are often used to provide protection to components on a printed circuit board (not shown). It should be appreciated however that any fuse arranged and configured to provide electrical protection between sources of electrical power and circuit components that are to be protected may be used.

[0023] Referring to **FIGS. 2** and **3**, an illustrative, exemplary embodiment of a fuse 200 according to the present invention is illustrated. As shown, the fuse 200 is in the form of a chip fuse and includes a fusible element 210 disposed between non-conductive layers of material 220 (shown as first and second non-conductive layers 220a, 220b). Upon the occurrence of a specified fault condition in a circuit, such as an overcurrent condition, the fusible element 210 can melt, or otherwise separate, to interrupt current flow in the circuit

path (e.g., between the input and output) in order to electrically isolate and protect downstream portions of the circuit.

[0024] The fuse 200 may also include first and second conductive terminals 230, 232. The first and second conductive terminals 230, 232 may be connected to each end of the fusible element 210 to provide a means of connecting the fuse 200 within the circuit. That is, the fusible element 210 may extend horizontally across the non-conductive layers of material 220 to contact each of the first and second conductive terminals 230, 232. The fusible element 210 contacts the first and second conductive terminals 230, 232 to form an electrical connection through the fuse 200. In use, the first and second conductive terminals 230, 232 connect the fuse 200 to the print circuit board.

[0025] The fusible element 210 may be any material having desirable electrically conductive properties. For example, the fusible element 210 may be any now known or hereafter developed conductive material such as nickel, copper, tin, silver, or an alloy or mixture comprising nickel, copper, silver, gold, or tin. The fusible element 210 may be formed of one or more layers of electrically conductive material. The fusible element 210 may be selected to have a desired diameter, width, and configuration to provide a predetermined response to current and voltage. Alternatively, the fusible element 210 may be a deposited film or other suitable material having predetermined characteristics. In some examples, the fusible element 210 may have a thickness between 0.02 and 5 mils.

[0026] The non-conductive layers 220 may be any material having desirable electrically non-conductive properties. For example, the non-conductive layers 220 may be any now known or hereafter developed non-conductive material such as ceramic (e.g.,

alumina), a ceramic-glass compound, a low temperature co-fired ceramic (LTCC) material, combination of such materials, etc. The non-conductive layers 220 may be formed of one or more layers of electrically non-conductive material. In some examples, the non-conductive layers 220 may have a thickness between 0.5 and 20 mils.

[0027] The first and second conductive terminals 230, 232 may be any material having desirable electrically conductive properties. For example, the first and second conductive terminals 230, 232 may be any now known or hereafter developed conductive material such as silver, copper, tin, nickel, or any combination of such materials.

[0028] The fuse 200 may also include a high-resistive material 250. The high-resistive material 250 may be disposed between non-conductive layers of material 220. For example, the high-resistive material 250 may be disposed between the second non-conductive layer of material 220b and a third non-conductive layer of material 220c.

[0029] Alternatively, as shown, the fuse 100 may also include a substrate 240. In use, the substrate 240 may be a non-conductive layer of material 220. As such, the substrate 240 may take the place of one of the non-conductive layers of material 220 (e.g., shown as the third non-conductive layer of material 220c). In this manner, as shown, the high-resistive material 250 may be disposed between the second layer of non-conductive material 220b and the layer of substrate 240.

[0030] In use, the substrate 240 provides support to the fuse 200 and ensures that when the fusible element 210 melts in response to a fault condition, the fuse 200 does not rupture as rupturing of the fuse 200 can cause damage to the components to be protected as well as adjacent components on the printed circuit board. The substrate 240 may be any

rigid substrate now known or hereafter developed. For example, the substrate 240 may be an Alumina substrate, FR4, etc. The substrate 240 may be printed with identifying information that can be visible to consumers. As shown, the substrate 240 may be located at the bottom of the fuse 200. However, it should be appreciated that the substrate 240 may be vertically located anywhere within the fuse 200.

[0031] In use, the high-resistive material 250 provides greater resistance to current flow than the fusible element 210. In this manner, during normal operating conditions, the high-resistive material 250 sits dormant (i.e., the high-resistive material 250 does not affect or alter current flow through the fuse 200). That is, as will be appreciated by of ordinary skill in the art, in an electrical DC circuit, current takes the path of least resistance. The fusible element 210 may have a first electrical resistance while the high-resistive material 250 may have a second electrical resistance, which is greater than the first electrical resistance through the fusible element 210. As such, during normal operating conditions, the current flows through the fusible element 210. During an over-current situation, however, as the fusible element 210 melts and/or separates, the resistance through the fusible element 210 increases. Once the resistance through the fusible element 210 exceeds the resistance through the high-resistive material 250, the current travels through the high-resistive material 250 thereby preventing or minimizing arcing across the fusible element 210.

[0032] The high-resistive material 250 may be any now known or hereafter developed material including, but not limited to, Polymeric Thermo confident polymer, think film resistor, wire wound resistors, etc.

[0033] Referring to **FIGS. 4** and **5**, an alternate illustrative, exemplary embodiment of a fuse 300 according to the present invention is illustrated. The fuse 300 illustrated in **FIGS. 4** and **5** is substantially similar to the fuse 200 illustrated in **FIGS. 2** and **3**. As such, some of the disclosure is hereby omitted for the sake of brevity.

[0034] As shown, the fuse 300 is in the form of a chip fuse and includes a fusible element 310 disposed between non-conductive layers of material 320 (shown as first and second non-conductive layers 320a, 320b). Upon the occurrence of a specified fault condition in the circuit, such as an overcurrent condition, the fusible element 310 can melt, or otherwise separate, to interrupt current flow in the circuit path (e.g., between the input and output) in order to electrically isolate and protect downstream portions of the circuit.

[0035] The fuse 300 may also include first and second conductive terminals 330, 332. The first and second conductive terminals 330, 332 may be connected to each end of the fusible element 310 to provide a means of connecting the fuse 300 within the circuit. That is, the fusible element 310 may extend horizontally across the non-conductive layers of material 320 to contact each of the first and second conductive terminals 330, 332. The fusible element 310 contacts the first and second conductive terminals 330, 332 to form an electrical connection through the fuse 300. In use, the first and second conductive terminals 330, 332 connect the fuse 300 to the print circuit board.

[0036] The fuse 300 may also include a high-resistive material 350. The high-resistive material 350 may be disposed between non-conductive layers of material 320. Alternatively, as shown, the fuse 300 may also include a substrate 340. In use, the substrate 340 may be a non-conductive layer of material 320. As such, the substrate 340 may take

the place of one of the non-conductive layer of material 320. In this manner, as shown, the high-resistive material 350 may be disposed between the layer of substrate 340 and a third layer of non-conductive material 320c.

[0037] Thus, as shown, the primary difference between fuse 200 (shown and described in connection with **FIGS. 2** and **3**) and fuse 300 (shown and described in connection with **FIGS. 4** and **5**) is the location of the layer of substrate. In connection with fuse 300, the layer of substrate 340 is located more in the middle of the fuse 300 as compared to fuse 200 where the layer of substrate 240 was located at the bottom of the fuse 200. In addition, by locating the layer of substrate 340 more in the middle, above the layer of high-resistive material 350, the fuse 300 includes an additional layer of non-conductive material 320c.

[0038] In use, the substrate 340 provides support to the fuse 300 and ensures that when the fusible element 310 melts in response to a fault condition, the fuse 300 does not rupture as rupturing of the fuse 300 can cause damage to the components to be protected as well as adjacent components on the printed circuit board. The substrate 340 may be printed with identifying information that can be visible to consumers.

[0039] In use, the high-resistive material 350 provides greater resistance to current flow than the fusible element 310. In this manner, during normal operating conditions, the high-resistive material 350 sits dormant (i.e., the high-resistive material 350 does not affect or alter current flow through the fuse 300). That is, as will be appreciated by of ordinary skill in the art, in an electrical DC circuit, current takes the path of least resistance. The fusible element 310 may have a first electrical resistance while the high-

resistive material 350 may have a second electrical resistance, which is greater than the first electrical resistance through the fusible element 310. As such, during normal operating conditions, the current flows through the fusible element 310. During an over-current situation, however, as the fusible element 310 melts and/or separates, the resistance through the fusible element 310 increases. Once the resistance through the fusible element 310 exceeds the resistance through the high-resistive material 350, the current travels through the high-resistive material 350 thereby preventing or minimizing arcing across the fusible element 310.

[0040] It is to be appreciated, that the number and arrangement of layers depicted in **FIGS. 2-5** is done to facilitate understanding and is not intended to be limiting. More specifically, for example, various embodiments may include more or less nonconductive layers 220, 320 than depicted. Furthermore, as will be appreciated, it may not be possible to distinguish between the non-conductive layers 220, 320 in the manufactured device.

[0041] Referring to **FIG. 6**, a perspective view of an alternate illustrative, exemplary embodiment of a fuse 400 according to the present invention is illustrated. The fuse 400 illustrated in **FIG. 6** is substantially similar to fuse 200 (**FIGS. 2** and **3**) and fuse 300 (**FIGS. 4** and **5**). As such, some of the disclosure is hereby omitted for the sake of brevity.

[0042] As shown however, the primary difference between fuse 400 (shown and described in connection with **FIG. 6**) and fuses 200, 300 (shown and described in connection with **FIGS. 2-5**) is that fuse 400 is no longer in the form of a chip fuse. As shown, for example, the fusible element 410 may be in the form of a standard glass fuse,

although other fuses are contemplated. In use, the glass fuse 410 may be coupled to a fuse holder 450. That is, a fuse holder 450 may be provided. The fuse holder 450 including a body portion 452 and contacts 454, 456. In use, the contacts 454, 456 may couple and engage the ends of the glass fuse 410 as would be readily appreciated by one of ordinary skill in the art. In accordance with the principles of the present disclosure, the body portion 452 of the fuse holder 450 may be manufactured from a high-resistive material so that, in use, upon the occurrence of a specified fault condition in the circuit, such as an overcurrent condition, the fusible element (e.g., glass fuse) 410 can melt, or otherwise separate, to interrupt current flow in the circuit path (e.g., between the input and output) in order to electrically isolate and protect downstream portions of the circuit. However, by forming the body portion 452 of the fuse holder 450 from a high-resistive material, during an over-current situation, as the fusible element (e.g., glass fuse) 410 melts and/or separates, the resistance through the fusible element (e.g., glass fuse) 410 increases. Once the resistance through the fusible element (e.g., glass fuse) 410 exceeds the resistance through the body portion 452 of the fuse holder 450 made from the high-resistive material, the current travels through the high-resistive fuse holder 450 thereby preventing or minimizing arcing across the fusible element (e.g., glass fuse) 410.

[0043] Thus, in accordance with the principles of the present disclosure, the fusible element (e.g., glass fuse) 410 may have a first electrical resistance while the body portion 452 of the fuse holder 450 manufactured from a high-resistive material may have a second electrical resistance, which is greater than the first electrical resistance through the fusible element (e.g., glass fuse) 410. In normal operating condition, the high-resistive fuse holder 450 provides greater resistance to current flow than the fusible element (e.g., glass fuse)

410. Thus, during normal operating conditions, the high-resistive fuse holder 450 sits dormant (i.e., the high-resistive fuse holder 450 does not affect or alter current flow through the fuse 400). But, during an overcurrent situation, as the fusible element (e.g., glass fuse) 410 melts and/or separates, the resistance through the fusible element (e.g., glass fuse) 410 surpasses the resistance through the high-resistive fuse holder 450 so that the current travels through the high-resistive fuse holder 450 thereby preventing or minimizing arcing across the fusible element (e.g., glass fuse) 410.

[0044] **FIG. 7** is a flow diagram of a method 500 for manufacturing a fuse according to some embodiments of the present disclosure. The method 500 may begin at block 510. At block 510, a fusible element may be placed on a layer of a non-conductive material. For example, the fusible element 210 may be placed on non-conductive layer 220b.

[0045] Continuing to block 520, one or more non-conductive layers may be stacked onto the first non-conductive layer and the fusible element thus sandwiching the fusible element between non-conductive layers. For example, non-conductive layer 220a may be stacked onto fusible element 210 and non-conductive layer 220b.

[0046] Continuing to block 530, a high-resistive material may be stacked onto a non-conductive layer. Alternatively, if the chip fuse is going to include a substrate, the high-resistive material may be stacked onto the substrate. For example, a layer of high-resistive material 250 may be stacked onto a layer of non-conductive material 220c, for example, substrate 240.

[0047] Continuing to block 540, the layers of non-conductive material and fusible element may be stacked onto the high-resistive material thus sandwiching the layer of high-resistive material between layers of non-conductive material. For example, non-conductive layer 220b may be stacked onto the layer of high-resistive material 250.

[0048] Continuing to block 550, first and second fuse terminals may be formed on the fuse. For example, the first and second conductive terminals 230, 232 may be formed on the fuse 200. In some examples, the materials may be formed by dipping and/or plating the ends of the fuse.

[0049] It is to be appreciated, that the number and arrangement of layers described in connection with **FIG. 7** is done to facilitate understanding and is not intended to be limiting. For example, the chip fuse may include more or less layers. In addition, and/or alternatively, the chip fuse may be manufactured in different steps. As an example, a layer of non-conductive material or a layer of substrate may be placed first. Next, a layer of high-resistive material may be stacked onto the layer of non-conductive material or the layer of substrate. A layer of non-conductive material may then be stacked on the high-resistive material followed by stacking the fusible element and then another layer of non-conductive material.

[0050] The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Thus, such other embodiments and modifications are in the tended to fall within the scope of the

present disclosure. Furthermore, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Thus, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

CLAIMS

1. A fuse comprising:

a fusible element having a first electrical resistance; and

a high-resistive material having a second electrical resistance, the high-resistive material being in a parallel relationship with the fusible element;

wherein during a normal operating condition the first electrical resistance is less than the second electrical resistance such that current flows through the fusible element; and

wherein during an overcurrent condition the first electrical resistance is greater than the second electrical resistance such that current flows through the high-resistive material.

2. The fuse of claim 1, wherein the fuse is in the form of a chip fuse having a plurality of non-conductive layers wherein the fusible element is disposed between adjacent layers of the plurality of non-conductive layers and the high-resistive material is disposed between adjacent layers of the plurality of non-conductive layers.

3. The fuse of claim 2, wherein one of the plurality of non-conductive layers comprises a substrate upon which the fusible element, high-resistive material and plurality of non-conductive layers are disposed.

4. The fuse of claim 3, wherein the substrate is FR4.

5. The fuse of claim 1, further comprising a first conductive terminal at a first end of the chip fuse and a second conductive terminal disposed at a second end of the chip

fuse, the first and second conductive terminals electrically connected to the fusible element and the high-resistive material.

6. The fuse of claim 1, wherein the fuse further comprises first, second and third layers of non-conductive material, the fusible element being disposed between the first and second layers of non-conductive material, the high-resistive material being disposed between the second and third layers of non-conductive material.

7. The fuse of claim 6, wherein the third layer of non-conductive material comprises a substrate for supporting the fuse.

8. The fuse of claim 1, wherein the fuse further comprises first, second, third and fourth layers of non-conductive material, the fusible element being disposed between the first and second layers of non-conductive material, the high-resistive material being disposed between the third and fourth layers of non-conductive material.

9. The fuse of claim 8, wherein the third layer of non-conductive material comprises a substrate upon which the fusible element, high-resistive material and non-conductive material are disposed.

10. The fuse of claim 1, further comprising a fuse holder including a body portion and contacts, the fusible element being in the form of a glass fuse, the body portion comprising the high-resistive material.

11. The fuse of claim 1, wherein the second resistance of the high-resistive material is up to approximately 200kohms at room temperature.

12. A fuse comprising:

a plurality of non-conductive layers;

a fusible element having a first electrical resistance, the fusible element being disposed between adjacent non-conductive layers of the plurality of non-conductive layers; and

a high-resistive material having a second electrical resistance, the high-resistive material being disposed between adjacent non-conductive layers of the plurality of non-conductive layers, the high-resistive material being in a parallel relationship with the fusible element, wherein during a normal operating condition the first electrical resistance is less than the second electrical resistance such that current flows through the fusible element, and wherein during an overcurrent condition the first electrical resistance is greater than the second electrical resistance such that current flows through the high-resistive material.

13. The fuse of claim 12, further comprising first and second conductive terminals, the first and second conductive terminals being electrically connected to the fusible element and the high resistive material.

14. The fuse of claim 12, further comprising a substrate upon which the fusible element, high-resistive material and plurality of non-conductive layers are disposed.

15. The fuse of claim 12, wherein the plurality of non-conductive layers includes first, second and third layers of non-conductive material, the fusible element being disposed between the first and second layers of non-conductive material, the high-resistive material being disposed between the second and third layers of non-conductive material.

16. The fuse of claim 12, wherein the plurality of non-conductive layers includes first, second, third and fourth layers of non-conductive material, the fusible element being disposed between the first and second layers of non-conductive material, the high-resistive material being disposed between the third and fourth layers of non-conductive material.

17. The fuse of claim 16, wherein the third layer of non-conductive material comprises a rigid substrate for supporting the fuse.

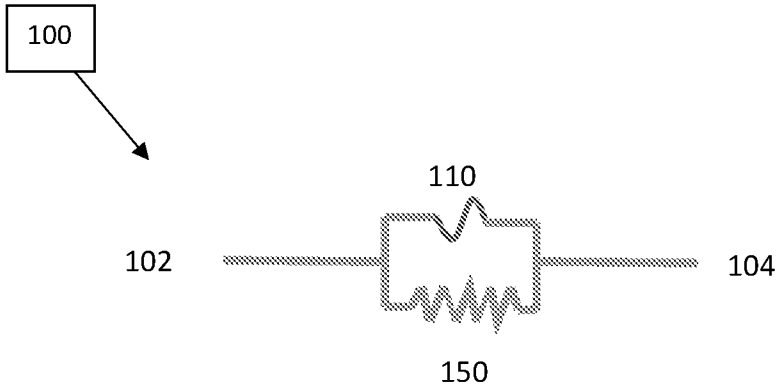


FIG. 1

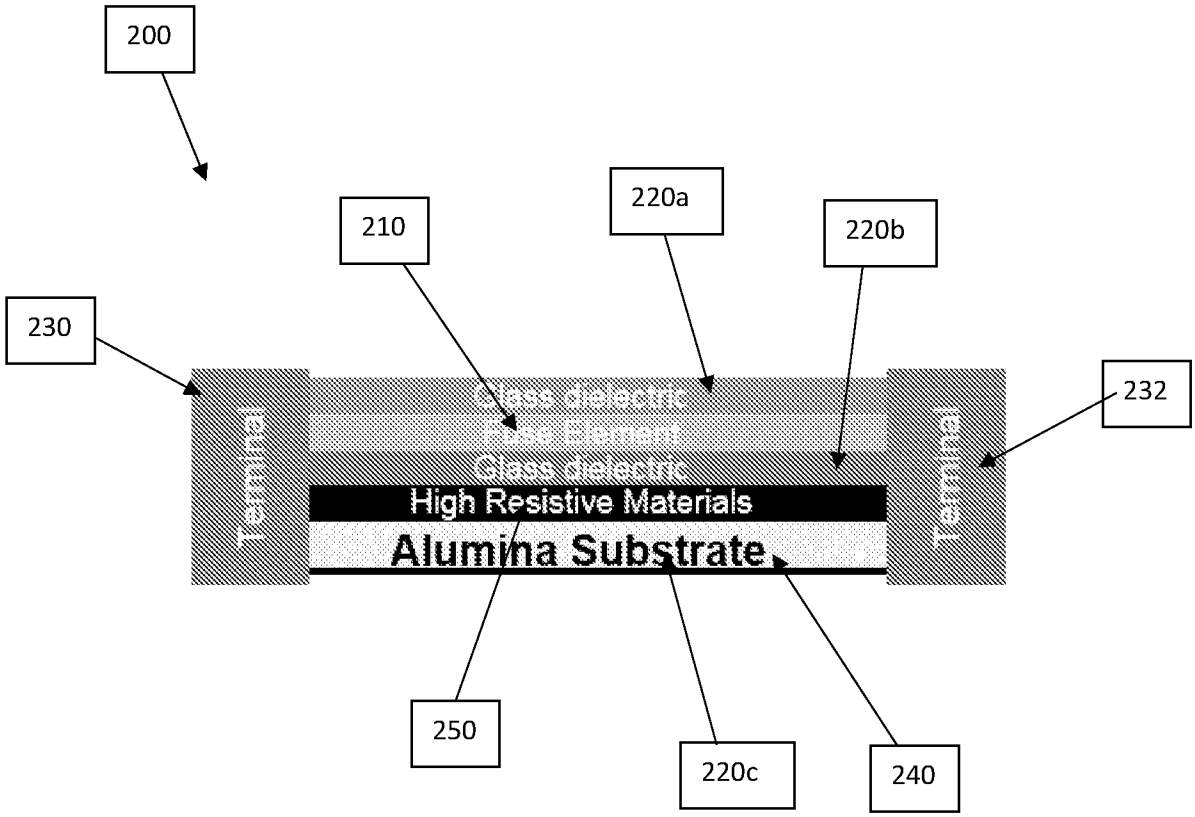

200
210
220a
220b
230
232
Glass dielectric
Heat Element
Glass dielectric
High Resistive Materials
Alumina Substrate
Terminal
Terminal
250
220c
240

FIG. 2

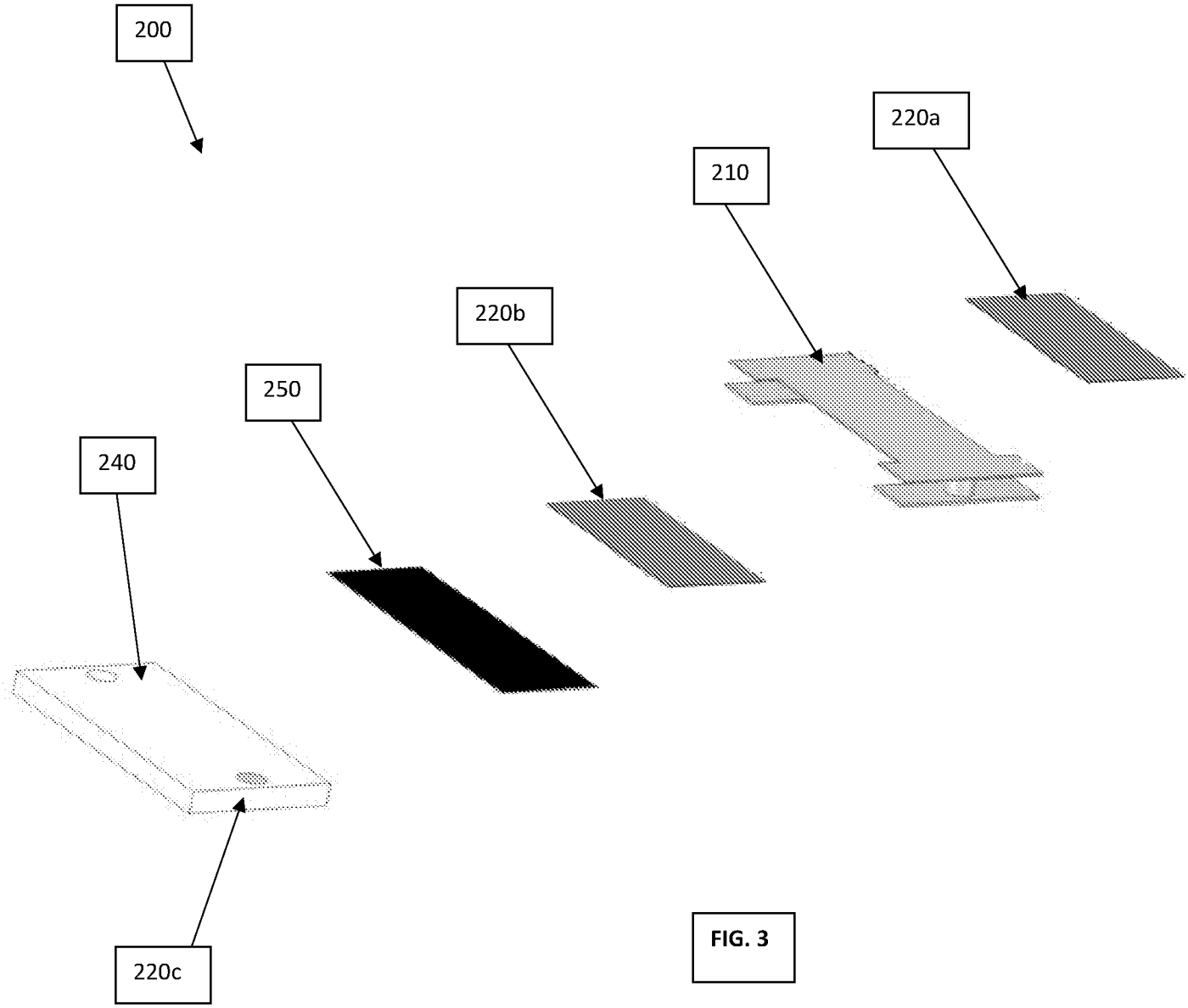


FIG. 3

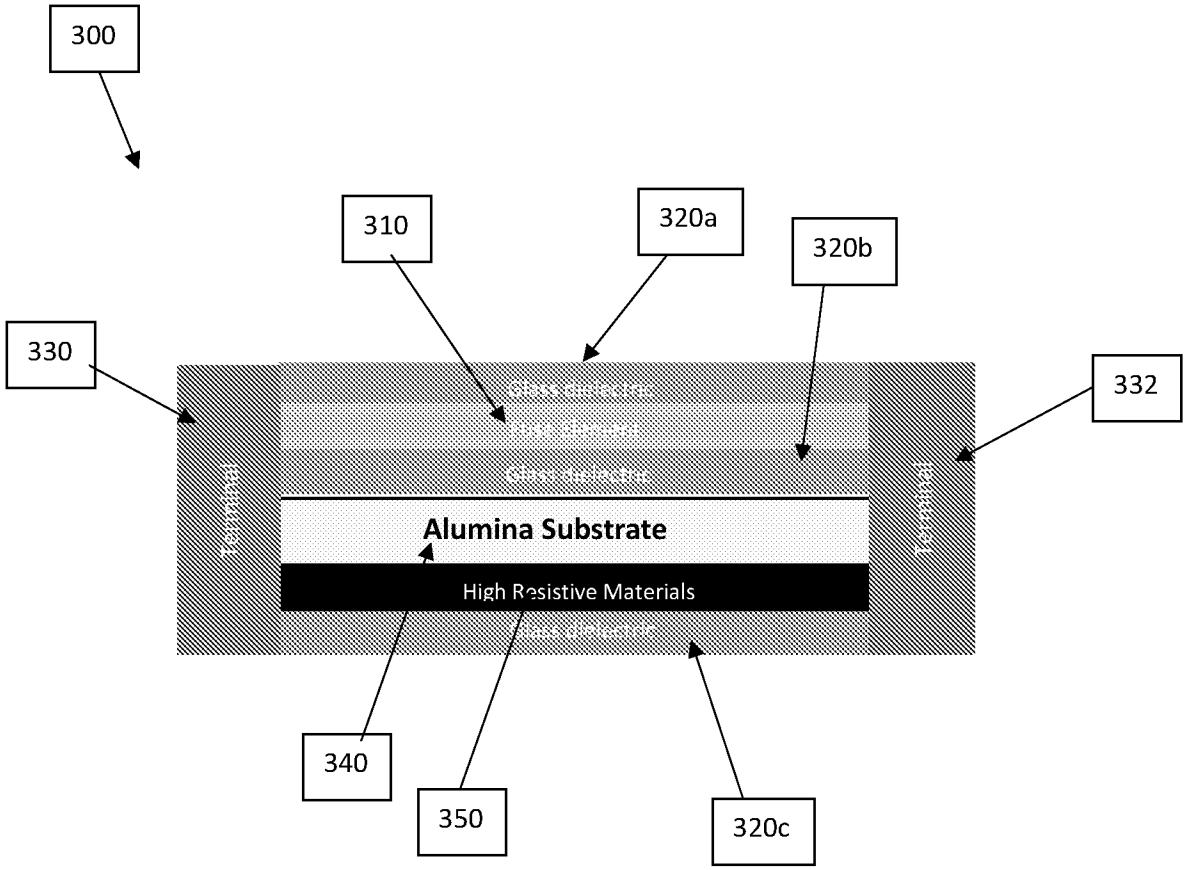

300
310
320a
320b
330
332
Alumina Substrate
High Resistive Materials
340
350
320c

FIG. 4

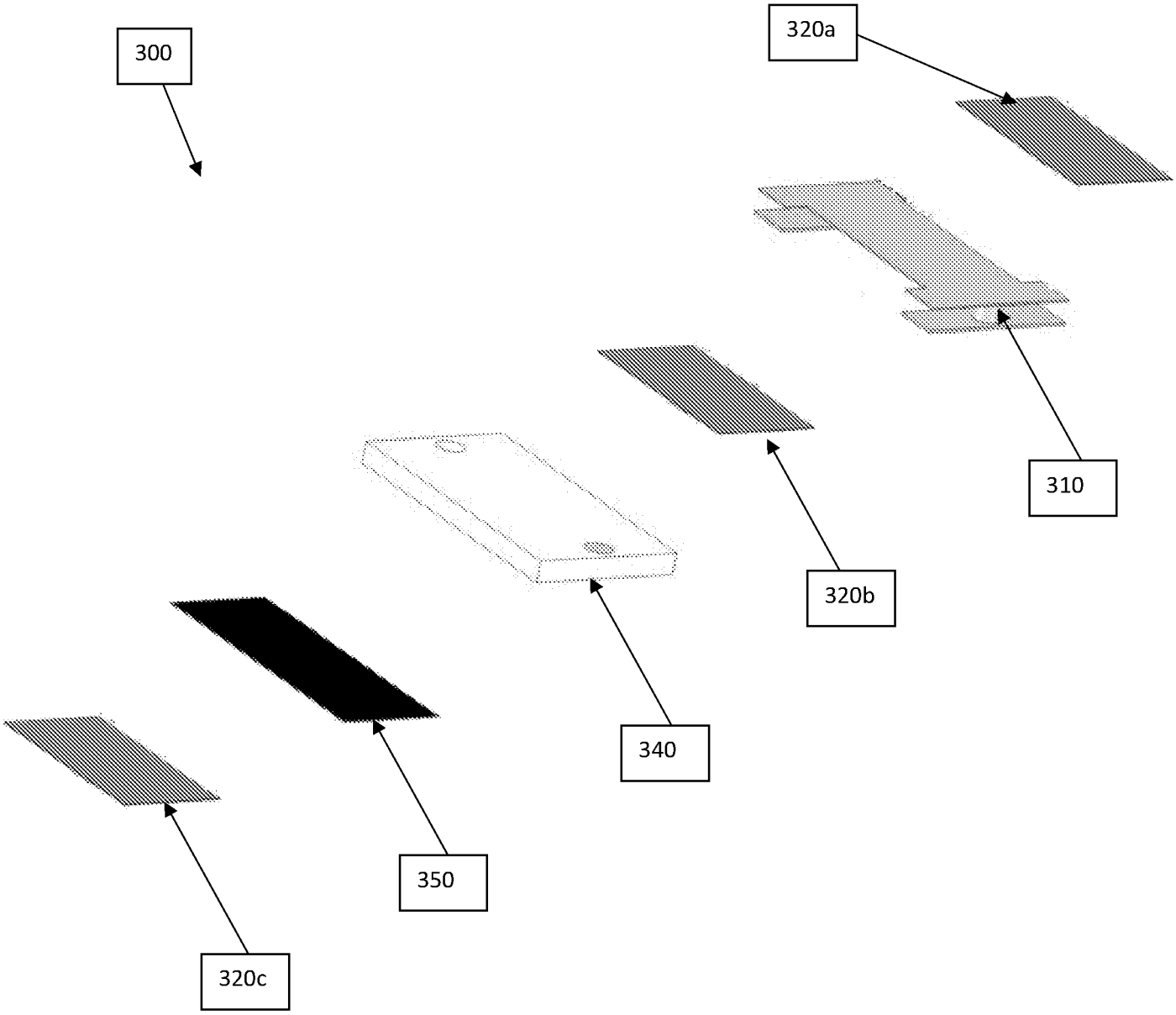


FIG. 5

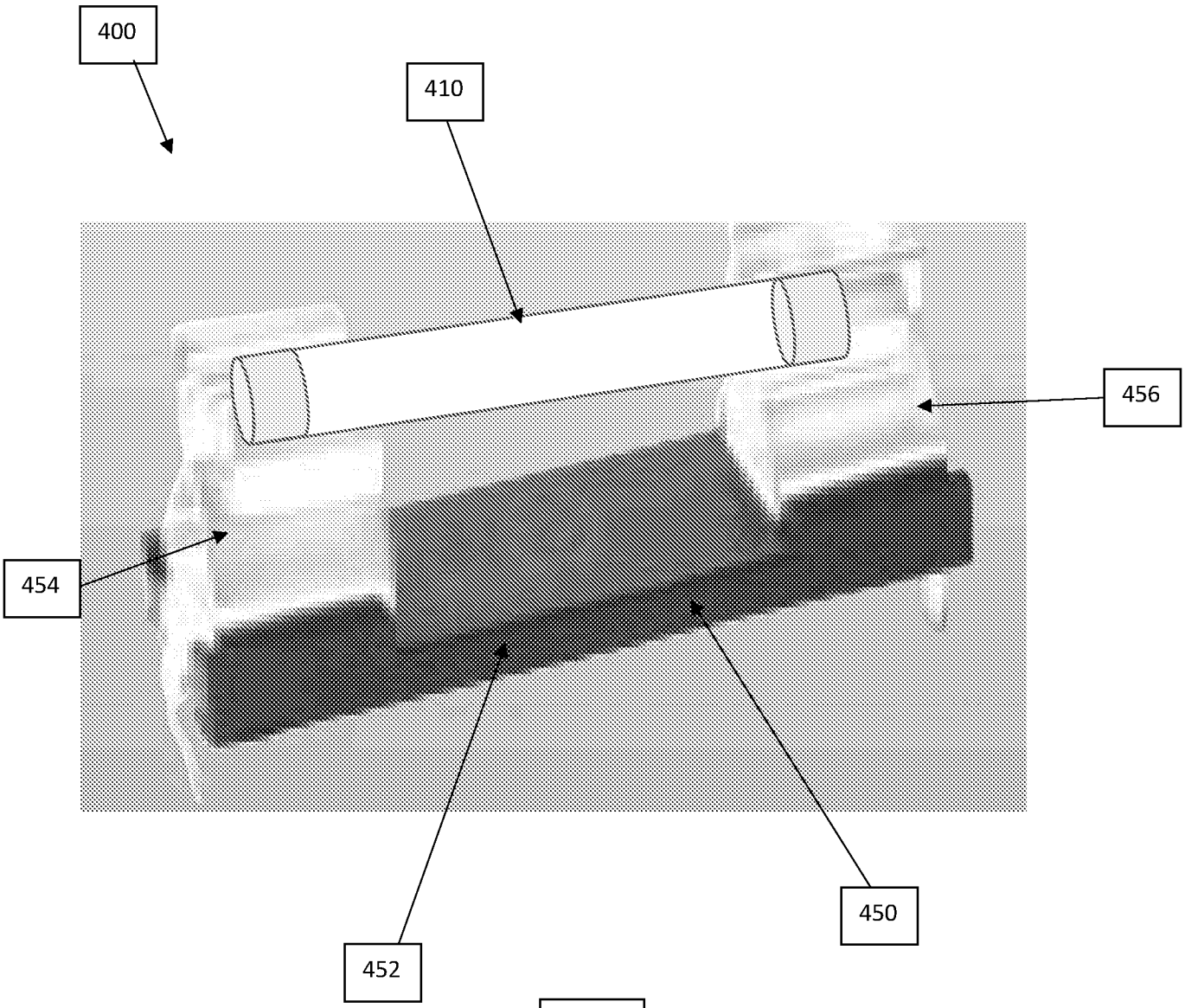


FIG. 6

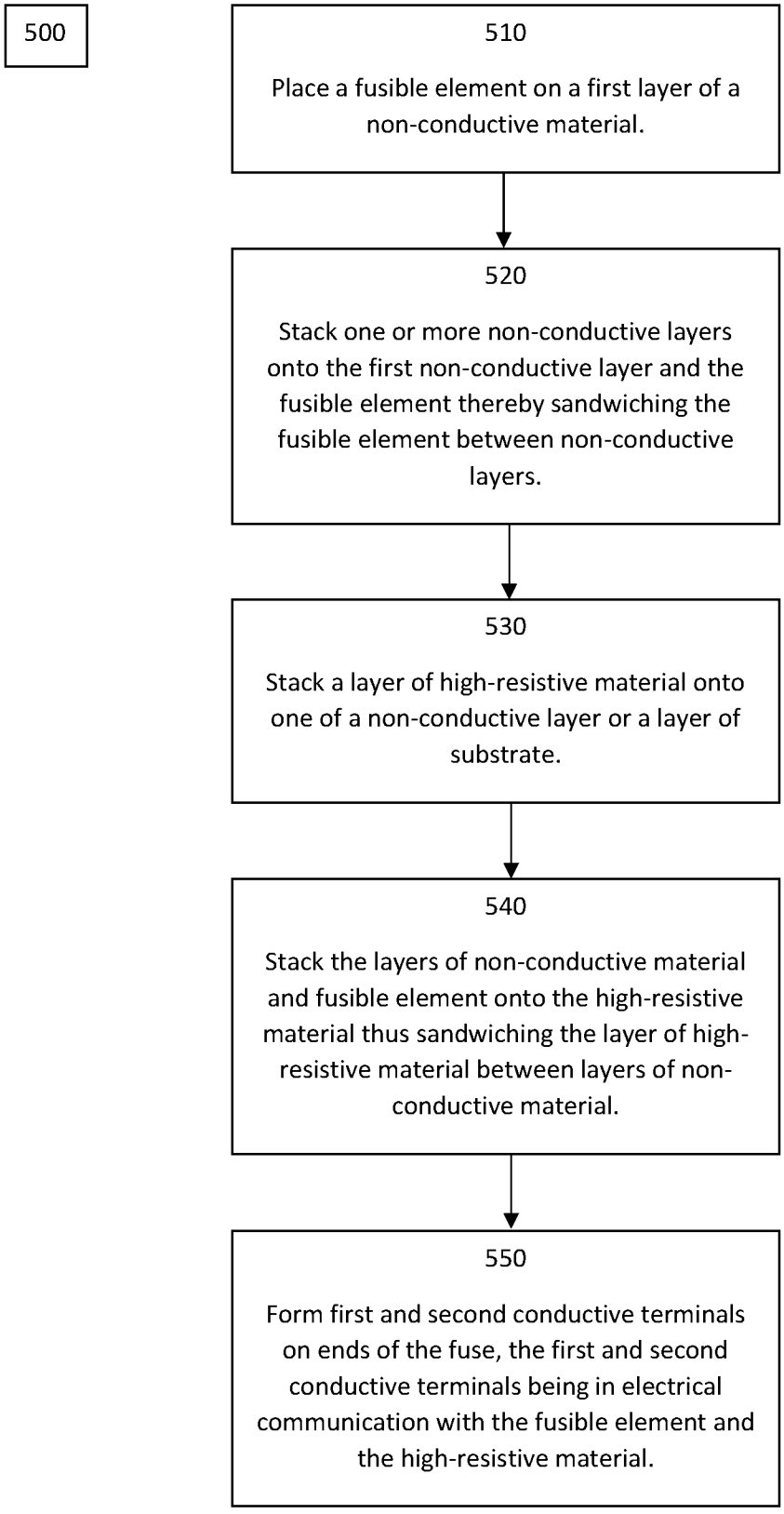

500
510
Place a fusible element on a first layer of a non-conductive material.
520
Stack one or more non-conductive layers onto the first non-conductive layer and the fusible element thereby sandwiching the fusible element between non-conductive layers.
530
Stack a layer of high-resistive material onto one of a non-conductive layer or a layer of substrate.
540
Stack the layers of non-conductive material and fusible element onto the high-resistive material thus sandwiching the layer of high-resistive material between layers of non-conductive material.
550
Form first and second conductive terminals on ends of the fuse, the first and second conductive terminals being in electrical communication with the fusible element and the high-resistive material.

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/037794

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01H 85/12; H01H 85/00; H01H 85/02; H01H 85/04; H02B 1/18 (2018.01)
CPC - H01H 85/12; H01H 85/00; H01H 85/02; H01H 85/04; H02B 1/18 (2018.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 337/297; 29/623; 174/250 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/0096448 A1 (WORTBERG) 28 April 2011 (28.04.2011) entire document	1-17
Y	US 2009/0261451 A1 (WHITNEY) 22 October 2009 (22.10.2009) entire document	1-17
Y	US 2008/0191832 A1 (TSAI) 14 August 2008 (14.08.2008) entire document	2-5, 10
A	US 2006/0214259 A1 (SPAUNHORST) 28 September 2006 (28.09.2006) entire document	1-17
A	US 2006/0022300 A1 (WU et al) 02 February 2006 (02.02.2006) entire document	1-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2018	17 SEP 2018

Name and mailing address of the ISA/US	Authorized officer
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774