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(71) Applicant *(for all designated States except US)*: **IGNIS INNOVATION INC.** [CA/CA]; 22 Frederick St., Suite 1020, Kitchener, ON N2H 6M6 (CA).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **NATHAN, Arokia** [CA/GB]; 189 Huntingdon Road, Cambridge CB3 0DL (GB). **CHAJI, G. Reza** [CA/CA]; 463 Kelso Drive, Waterloo, ON N2V 2S3 (CA). **ALEXANDER, Stefan** [CA/CA]; 601 East Bridge Blvd., Waterloo, ON N2K 4C1 (CA).

(74) Agent: **HARRIS, John, D.**; Gowling Lafleur Henderson LLP, 160 Elgin Street, Suite 2600, Ottawa, Ontario K1P 1C3 (CA).

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(54) **Title**: SYSTEM AND DRIVING METHOD FOR LIGHT EMITTING DEVICE DISPLAY

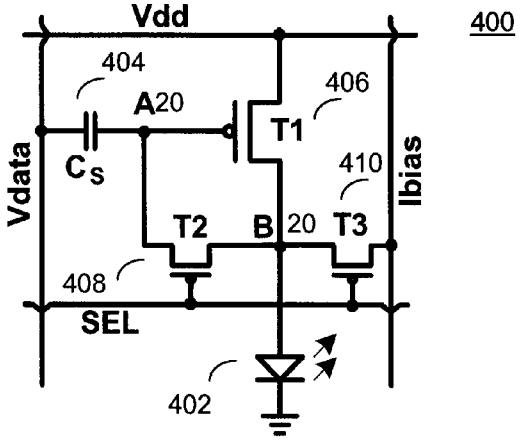

FIG.24

(57) **Abstract**: A light emitting device display, its pixel circuit and its driving technique is provided. The pixel includes a light emitting device and a plurality of transistors. A bias current and programming voltage data are provided to the pixel circuit in accordance with a driving scheme so that the current through the driving transistor to the light emitting device is adjusted.

System and Driving Method for Light Emitting Device Display

FIELD OF INVENTION

[0001] The present invention relates to a light emitting device displays, and more specifically to a driving technique for the light emitting device displays.

BACKGROUND OF THE INVENTION

[0002] Recently active-matrix organic light-emitting diode (AMOLED) displays with amorphous silicon (a-Si), poly-silicon, organic, or other driving backplane technology have become more attractive due to advantages over active matrix liquid crystal displays. An AMOLED display using a-Si backplanes, for example, has the advantages which include low temperature fabrication that broadens the use of different substrates and makes flexible displays feasible, and its low cost fabrication is well-established and yields high resolution displays with a wide viewing angle.

[0003] An AMOLED display includes an array of rows and columns of pixels, each having an organic light-emitting diode (OLED) and backplane electronics arranged in the array of rows and columns. Since the OLED is a current driven device, the pixel circuit of the AMOLED should be capable of providing an accurate and constant drive current.

[0004] One method that has been employed to drive the AMOLED display is programming the AMOLED pixel directly with current. However, the small current required by the OLED, coupled with a large parasitic capacitance, undesirably increases the settling time of the programming of the current-programmed AMOLED display. Furthermore, it is difficult to design an external driver to accurately supply the required current. For example, in CMOS technology, the transistors must work in sub-threshold regime to provide the small current required by the OLEDs, which is not ideal. Therefore, in order to use current-programmed AMOLED pixel circuits, suitable driving schemes are desirable.

[0005] Current scaling is one method that can be used to manage issues associated with the small current required by the OLEDs. In a current mirror pixel circuit, the current passing through the OLED can be scaled by having a smaller drive transistor as

compared to the mirror transistor. However, this method is not applicable for other current-programmed pixel circuits. Also, by resizing the two mirror transistors the effect of mismatch increases.

SUMMARY OF THE INVENTION

[0006] It is an object of the invention to provide a method and system that obviates or mitigates at least one of the disadvantages of existing systems.

[0007] In accordance with an aspect of the present invention there is provided a pixel circuit, which includes a light emitting device, a driving transistor for providing a pixel current to the light emitting device, a storage capacitor provided between a data line for providing programming voltage data and the gate terminal of the driving transistor, a first switch transistor provided between the gate terminal of the driving transistor and the light emitting device, and a second switch transistor provided between the light emitting device and a bias line for providing a bias current to the first terminal of the driving transistor during a programming cycle.

[0008] In accordance with a further aspect of the present invention there is provided a pixel circuit, which includes a light emitting device, a storage capacitor, a driving transistor for providing a pixel current to the light emitting device, a plurality of first switch transistors operated by a first select line, one of the first switch transistors being provided between the storage capacitor and a data line for providing programming voltage data, a plurality of second switch transistors operated by a second select line, one of the second switch transistor being provided between the driving transistor and a bias line for providing a bias current to the first terminal of the driving transistor during a programming cycle; and an emission control circuit for setting the pixel circuit into an emission mode.

[0009] In accordance with a further aspect of the present invention there is provided a display system, which includes a pixel array having a plurality of pixel circuits, a first driver for selecting the pixel circuit, a second driver for providing the programming voltage data, and a current source for operating on the bias line.

[0010] In accordance with a further aspect of the present invention there is provided a a method of driving a pixel circuit, the pixel circuit having a driving transistor for providing a pixel current to a light emitting device, a storage capacitor coupled to a data line, and a switch transistor coupled to the gate terminal of the driving transistor and the storage capacitor. The method includes:at a programming cycle, selecting the pixel circuit, providing a bias current to a connection between the driving transistor and the light emitting device, and providing programming voltage data from the data line to the pixel circuit.

[0011] In accordance with a further aspect of the present invention there is provided a a method of driving a pixel circuit, the pixel circuit having a driving transistor for providing a pixel current to a light emitting device, a switch transistor coupled to a data line, and a storage capacitor coupled to the switch transistor and the driving transistor. The method includes: at a programming cycle, selecting the pixel circuit, providing a bias current to a first terminal of the driving transistor, and providing programming voltage data from the data line to a first terminal of the storage capacitor, the second terminal of the storage capacitor being coupled to the first terminal of the driving transistor, a second terminal of the driving transistor being coupled to the light emitting device; and at a driving cycle, setting an emission mode in the pixel circuit.

[0012] This summary of the invention does not necessarily describe all features of the invention.

[0013] Other aspects and features of the present invention will be readily apparent to those skilled in the art from a review of the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

[0015] Figure 1 is a diagram showing a pixel circuit in accordance with an embodiment of the present invention;

[0016] Figure 2 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 1;

[0017] Figure 3 is a timing diagram showing further exemplary waveforms applied to the pixel circuit of Figure 1;

[0018] Figure 4 is a graph showing a current stability of the pixel circuit of Figure 1;

[0019] Figure 5 is a diagram showing a pixel circuit which has p-type transistors and corresponds to the pixel circuit of Figure 1;

[0020] Figure 6 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 5;

[0021] Figure 7 is a timing diagram showing further exemplary waveforms applied to the pixel circuit of Figure 5;

[0022] Figure 8 is a diagram showing a pixel circuit in accordance with a further embodiment of the present invention;

[0023] Figure 9 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 8;

[0024] Figure 10 is a diagram showing a pixel circuit which has p-type transistors and corresponds to the pixel circuit of Figure 8;

[0025] Figure 11 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 10;

[0026] Figure 12 is a diagram showing a pixel circuit in accordance with an embodiment of the present invention;

[0027] Figure 13 is a timing diagram showing exemplary waveforms applied to the display of Figure 12;

[0028] Figure 14 is a graph showing the settling time of a CBVP pixel circuit for different bias currents;

[0029] Figure 15 is a graph showing I-V characteristic of the CBVP pixel circuit as well as the total error induced in the pixel current;

[0030] Figure 16 is a diagram showing a pixel circuit which has p-type transistors and corresponds to the pixel circuit of Figure 12;

[0031] Figure 17 is a timing diagram showing exemplary waveforms applied to the display of Figure 16;

[0032] Figure 18 is a diagram showing a VBCP pixel circuit in accordance with a further embodiment of the present invention;

[0033] Figure 19 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 18;

[0034] Figure 20 is a diagram showing a VBCP pixel circuit which has p-type transistors and corresponds to the pixel circuit of Figure 18;

[0035] Figure 21 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 20;

[0036] Figure 22 is a diagram showing a driving mechanism for a display array having CBVP pixel circuits;

[0037] Figure 23 is a diagram showing a driving mechanism for a display array having VBCP pixel circuits;

[0038] Figure 24 is a diagram showing a pixel circuit in accordance with a further embodiment of the present invention;

[0039] Figure 25 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 24;

[0040] Figure 26 is a diagram showing a pixel circuit in accordance with a further embodiment of the present invention;

[0041] Figure 27 is a timing diagram showing exemplary waveforms applied to the pixel circuit of Figure 26;

[0042] Figure 28 is a diagram showing a further example of a display system having CBVP pixel circuits;

[0043] Figure 29 is a diagram showing a further example of a display system having CBVP pixel circuits;

[0044] Figure 30 is a photograph showing effect of spatial mismatches on a display using a simple 2-TFT pixel circuit;

[0045] Figure 31 is a photograph showing effect of spatial mismatches on a display using the voltage-programmed circuits; and

[0046] Figure 32 is a photograph showing effect of spatial mismatches on a display using CBVP pixel circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

[0047] Embodiments of the present invention are described using a pixel having an organic light emitting diode (OLED) and a driving thin film transistor (TFT). However, the pixel may include any light emitting device other than OLED, and the pixel may include any driving transistor other than TFT. It is noted that in the description, "pixel circuit" and "pixel" may be used interchangeably.

[0048] A driving technique for pixels, including a current-biased voltage-programmed (CBVP) driving scheme, is now described in detail. The CBVP driving scheme uses voltage to provide for different gray scales (voltage programming), and uses a bias to accelerate the programming and compensate for the time dependent parameters of a pixel, such as a threshold voltage shift and OLED voltage shift.

[0049] Figure 1 illustrates a pixel circuit 200 in accordance with an embodiment of the present invention. The pixel circuit 200 employs the CBVP driving scheme as described below. The pixel circuit 200 of Figure 1 includes an OLED 10, a storage capacitor 12, a driving transistor 14, and switch transistors 16 and 18. Each transistor has a gate terminal, a first terminal and a second terminal. In the description, “first

terminal" ("second terminal") may be, but not limited to, a drain terminal or a source terminal (source terminal or drain terminal).

[0050] The transistors 14, 16 and 18 are n-type TFT transistors. The driving technique applied to the pixel circuit 200 is also applicable to a complementary pixel circuit having p-type transistors as shown in Figure 5.

[0051] The transistors 14, 16 and 18 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), NMOS technology, or CMOS technology (e.g. MOSFET). A plurality of pixel circuits 200 may form an AMOLED display array.

[0052] Two select lines SEL1 and SEL2, a signal line VDATA, a bias line IBIAS, a voltage supply line VDD, and a common ground are provided to the pixel circuit 200. In Figure 1, the common ground is for the OLED top electrode. The common ground is not a part of the pixel circuit, and is formed at the final stage when the OLED 10 is formed.

[0053] The first terminal of the driving transistor 14 is connected to the voltage supply line VDD. The second terminal of the driving transistor 14 is connected to the anode electrode of the OLED 10. The gate terminal of the driving transistor 14 is connected to the signal line VDATA through the switch transistor 16. The storage capacitor 12 is connected between the second and gate terminals of the driving transistor 14.

[0054] The gate terminal of the switch transistor 16 is connected to the first select line SEL1. The first terminal of the switch transistor 16 is connected to the signal line VDATA. The second terminal of the switch transistor 16 is connected to the gate terminal of the driving transistor 14.

[0055] The gate terminal of the switch transistor 18 is connected to the second select line SEL2. The first terminal of transistor 18 is connected to the anode electrode of the OLED 10 and the storage capacitor 12. The second terminal of the switch transistor 18 is connected to the bias line IBIAS. The cathode electrode of the OLED 10 is connected to the common ground.

[0056] The transistors 14 and 16 and the storage capacitor 12 are connected to node A11. The OLED 10, the storage capacitor 12 and the transistors 14 and 18 are connected to B11.

[0057] The operation of the pixel circuit 200 includes a programming phase having a plurality of programming cycles, and a driving phase having one driving cycle. During the programming phase, node B11 is charged to negative of the threshold voltage of the driving transistor 14, and node A11 is charged to a programming voltage VP.

[0058] As a result, the gate-source voltage of the driving transistor 14 is:

$$VGS = VP - (-VT) = VP + VT \qquad (1)$$

where VGS represents the gate-source voltage of the driving transistor 14, and VT represents the threshold voltage of the driving transistor 14. This voltage remains on the capacitor 12 in the driving phase, resulting in the flow of the desired current through the OLED 10 in the driving phase.

[0059] The programming and driving phases of the pixel circuit 200 are described in detail. Figure 2 illustrates one exemplary operation process applied to the pixel circuit 200 of Figure 1. In Figure 2, VnodeB represents the voltage of node B11, and VnodeA represents the voltage of node A11. As shown in Figure 2, the programming phase has two operation cycles X11, X12, and the driving phase has one operation cycle X13.

[0060] The first operation cycle X11: Both select lines SEL1 and SEL2 are high. A bias current IB flows through the bias line IBIAS, and VDATA goes to a bias voltage VB.

[0061] As a result, the voltage of node B11 is:

$$VnodeB = VB - \sqrt{\frac{IB}{\beta}} - VT \qquad (2)$$

where VnodeB represents the voltage of node B11, VT represents the threshold voltage of the driving transistor 14, and β represents the coefficient in current-voltage (I-V) characteristics of the TFT given by $IDS = \beta (VGS - VT)^2$. IDS represents the drain-source current of the driving transistor 14.

[0062] The second operation cycle X12: While SEL2 is low, and SEL1 is high, VDATA goes to a programming voltage VP. Because the capacitance 11 of the OLED 20 is large, the voltage of node B11 generated in the previous cycle stays intact.

[0063] Therefore, the gate-source voltage of the driving transistor 14 can be found as:

$$VGS = VP + \Delta VB + VT \qquad (3)$$

$$\Delta VB = \sqrt{\frac{IB}{\beta}} - VB \qquad (4)$$

[0064] ΔVB is zero when VB is chosen properly based on (4). The gate-source voltage of the driving transistor 14, i.e., VP+VT, is stored in the storage capacitor 12.

[0065] The third operation cycle X13: IBIAS goes to low. SEL1 goes to zero. The voltage stored in the storage capacitor 12 is applied to the gate terminal of the driving transistor 14. The driving transistor 14 is on. The gate-source voltage of the driving transistor 14 develops over the voltage stored in the storage capacitor 12. Thus, the current through the OLED 10 becomes independent of the shifts of the threshold voltage of the driving transistor 14 and OLED characteristics.

[0066] Figure 3 illustrates a further exemplary operation process applied to the pixel circuit 200 of Figure 1. In Figure 3, VnodeB represents the voltage of node B11, and VnodeA represents the voltage of node A11.

[0067] The programming phase has two operation cycles X21, X22, and the driving phase has one operation cycle X23. The first operation cycle X21 is same as the first operation cycle X11 of Figure 2. The third operation cycle X33 is same as the third

operation cycle X 13 of Figure 2. In Figure 3, the select lines SEL1 and SEL2 have the same timing. Thus, SEL1 and SEL2 may be connected to a common select line.

[0068] The second operating cycle X22: SEL1 and SEL2 are high. The switch transistor 18 is on. The bias current IB flowing through IBIAS is zero.

[0069] The gate-source voltage of the driving transistor 14 can be VGS = VP + VT as described above. The gate-source voltage of the driving transistor 14, i.e., VP+VT, is stored in the storage capacitor 12.

[0070] Figure 4 illustrates a simulation result for the pixel circuit 200 of Figure 1 and the waveforms of Figure 2. The result shows that the change in the OLED current due to a 2-volt VT-shift in the driving transistor (e.g. 14 of Figure 1) is almost zero percent for most of the programming voltage. Simulation parameters, such as threshold voltage, show that the shift has a high percentage at low programming voltage.

[0071] Figure 5 illustrates a pixel circuit 202 having p-type transistors. The pixel circuit 202 corresponds to the pixel circuit 200 of Figure 1. The pixel circuit 202 employs the CBVP driving scheme as shown in Figures 6-7. The pixel circuit 202 includes an OLED 20, a storage capacitor 22, a driving transistor 24, and switch transistors 26 and 28. The transistors 24, 26 and 28 are p-type transistors. Each transistor has a gate terminal, a first terminal and a second terminal.

[0072] The transistors 24, 26 and 28 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), PMOS technology, or CMOS technology (e.g. MOSFET). A plurality of pixel circuits 202 may form an AMOLED display array.

[0073] Two select lines SEL1 and SEL2, a signal line VDATA, a bias line IBIAS, a voltage supply line VDD, and a common ground are provided to the pixel circuit 202.

[0074] The transistors 24 and 26 and the storage capacitor 22 are connected to node A12. The cathode electrode of the OLED 20, the storage capacitor 22 and the transistors 24 and 28 are connected to B12. Since the OLED cathode is connected to the other elements of the pixel circuit 202, this ensures integration with any OLED fabrication.

[0075] Figure 6 illustrates one exemplary operation process applied to the pixel circuit 202 of Figure 5. Figure 6 corresponds to Figure 2. Figure 7 illustrates a further exemplary operation process applied to the pixel circuit 202 of Figure 5. Figure 7 corresponds to Figure 3. The CBVP driving schemes of Figures 6-7 use IBIAS and VDATA similar to those of Figures 2-3.

[0076] Figure 8 illustrates a pixel circuit 204 in accordance with an embodiment of the present invention. The pixel circuit 204 employs the CBVP driving scheme as described below. The pixel circuit 204 of Figure 8 includes an OLED 30, storage capacitors 32 and 33, a driving transistor 34, and switch transistors 36, 38 and 40. Each of the transistors 34, 35 and 36 includes a gate terminal, a first terminal and a second terminal. This pixel circuit 204 operates in the same way as that of the pixel circuit 200.

[0077] The transistors 34, 36, 38 and 40 are n-type TFT transistors. The driving technique applied to the pixel circuit 204 is also applicable to a complementary pixel circuit having p-type transistors, as shown in Figure 10.

[0078] The transistors 34, 36, 38 and 40 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), NMOS technology, or CMOS technology (e.g. MOSFET). A plurality of pixel circuits 204 may form an AMOLED display array.

[0079] A select line SEL, a signal line VDATA, a bias line IBIAS, a voltage line VDD, and a common ground are provided to the pixel circuit 204.

[0080] The first terminal of the driving transistor 34 is connected to the cathode electrode of the OLED 30. The second terminal of the driving transistor 34 is connected to the ground. The gate terminal of the driving transistor 34 is connected to its first terminal through the switch transistor 36. The storage capacitors 32 and 33 are in series and connected between the gate of the driving transistor 34 and the ground.

[0081] The gate terminal of the switch transistor 36 is connected to the select line SEL. The first terminal of the switch transistor 36 is connected to the first terminal of the driving transistor 34. The second terminal of the switch transistor 36 is connected to the gate terminal of the driving transistor 34.

[0082] The gate terminal of the switch transistor 38 is connected to the select line SEL. The first terminal of the switch transistor 38 is connected to the signal line VDATA. The second terminal of the switch transistor 38 is connected to the connected terminal of the storage capacitors 32 and 33 (i.e. node C21).

[0083] The gate terminal of the switch transistor 40 is connected to the select line SEL. The first terminal of the switch transistor 40 is connected to the bias line IBIAS. The second terminal of the switch transistor 40 is connected to the cathode terminal of the OLED 30. The anode electrode of the OLED 30 is connected to the VDD.

[0084] The OLED 30, the transistors 34, 36 and 40 are connected at node A21. The storage capacitor 32 and the transistors 34 and 36 are connected at node B21.

[0085] The operation of the pixel circuit 204 includes a programming phase having a plurality of programming cycles, and a driving phase having one driving cycle. During the programming phase, the first storage capacitor 32 is charged to a programming voltage VP plus the threshold voltage of the driving transistor 34, and the second storage capacitor 33 is charged to zero

[0086] As a result, the gate-source voltage of the driving transistor 34 is:

$$VGS = VP + VT \qquad (5)$$

where VGS represents the gate-source voltage of the driving transistor 34, and VT represents the threshold voltage of the driving transistor 34.

[0087] The programming and driving phases of the pixel circuit 204 are described in detail. Figure 9 illustrates one exemplary operation process applied to the pixel circuit 204 of Figure 8. As shown in Figure 9, the programming phase has two operation cycles X31, X32, and the driving phase has one operation cycle X33.

[0088] The first operation cycle X31: The select line SEL is high. A bias current IB flows through the bias line IBIAS, and VDATA goes to a VB-VP where VP is and programming voltage and VB is given by:

$$VB = \sqrt{\frac{IB}{\beta}} \qquad (6)$$

[0089] As a result, the voltage stored in the first capacitor 32 is:

$$VC1 = VP + VT \qquad (7)$$

where VC1 represents the voltage stored in the first storage capacitor 32, VT represents the threshold voltage of the driving transistor 34, β represents the coefficient in current-voltage (I-V) characteristics of the TFT given by $IDS = \beta(VGS - VT)^2$. IDS represents the drain-source current of the driving transistor 34.

[0090] The second operation cycle: While SEL is high, VDATA is zero, and IBIAS goes to zero. Because the capacitance 31 of the OLED 30 and the parasitic capacitance of the bias line IBIAS are large, the voltage of node B21 and the voltage of node A21 generated in the previous cycle stay unchanged.

[0091] Therefore, the gate-source voltage of the driving transistor 34 can be found as:

$$VGS=VP+VT \qquad (8)$$

where VGS represents the gate-source voltage of the driving transistor 34..

[0092] The gate-source voltage of the driving transistor 34 is stored in the storage capacitor 32.

[0093] The third operation cycle X33: IBIAS goes to zero. SEL goes to zero. The voltage of node C21 goes to zero. The voltage stored in the storage capacitor 32 is applied to the gate terminal of the driving transistor 34. The gate-source voltage of the driving transistor 34 develops over the voltage stored in the storage capacitor 32. Considering that the current of driving transistor 34 is mainly defined by its gate-source voltage, the current through the OLED 30 becomes independent of the shifts of the threshold voltage of the driving transistor 34 and OLED characteristics.

[0094] Figure 10 illustrates a pixel circuit 206 having p-type transistors. The pixel circuit 206 corresponds to the pixel circuit 204 of Figure 8. The pixel circuit 206 employs the CBVP driving scheme as shown in Figure 11. The pixel circuit 206 of Figure 10 includes an OLED 50, a storage capacitors 52 and 53, a driving transistor 54, and switch transistors 56, 58 and 60. The transistors 54, 56, 58 and 60 are p-type transistors. Each transistor has a gate terminal, a first terminal and a second terminal.

[0095] The transistors 54, 56, 58 and 60 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), PMOS technology, or CMOS technology (e.g. MOSFET). A plurality of pixel circuits 206 may form an AMOLED display array.

[0096] Two select lines SEL1 and SEL2, a signal line VDATA, a bias line IBIAS, a voltage supply line VDD, and a common ground are provided to the pixel circuit 206. The common ground may be same as that of Figure 1.

[0097] The anode electrode of the OLED 50, the transistors 54, 56 and 60 are connected at node A22. The storage capacitor 52 and the transistors 54 and 56 are connected at node B22. The switch transistor 58, and the storage capacitors 52 and 53 are connected at node C22.

[0098] Figure 11 illustrates one exemplary operation process applied to the pixel circuit 206 of Figure 10. Figure 11 corresponds to Figure 9. As shown in Figure 11, the CBVP driving scheme of Figure 11 uses IBIAS and VDATA similar to those of Figure 9.

[0099] Figure 12 illustrates a display 208 in accordance with an embodiment of the present invention. The display 208 employs the CBVP driving scheme as described below. In Figure 12, elements associated with two rows and one column are shown as example. The display 208 may include more than two rows and more than one column.

[00100] The display 208 includes an OLED 70, storage capacitors 72 and 73, transistors 76, 78, 80, 82 and 84. The transistor 76 is a driving transistor. The transistors 78, 80 and 84 are switch transistors. Each of the transistors 76, 78, 80, 82 and 84 includes a gate terminal, a first terminal and a second terminal.

[00101] The transistors 76, 78, 80, 82 and 84 are n-type TFT transistors. The driving technique applied to the pixel circuit 208 is also applicable to a complementary pixel circuit having p-type transistors, as shown in Figure 16.

[00102] The transistors 76, 78, 80, 82 and 84 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), NMOS technology, or CMOS technology (e.g. MOSFET). The display 208 may form an AMOLED display array. The combination

of the CBVP driving scheme and the display 208 provides a large-area, high-resolution AMOLED display.

[00103] The transistors 76 and 80 and the storage capacitor 72 are connected at node A31. The transistors 82 and 84 and the storage capacitors 72 and 74 are connected at B31.

[00104] Figure 13 illustrates one exemplary operation process applied to the display 208 of Figure 12. In Figure 13, "Programming cycle [n]" represents a programming cycle for the row [n] of the display 208.

[00105] The programming time is shared between two consecutive rows (n and n+1). During the programming cycle of the nth row, SEL[n] is high, and a bias current IB is flowing through the transistors 78 and 80. The voltage at node A31 is self-adjusted to (IB/β)1/2+VT, while the voltage at node B31 is zero, where VT represents the threshold voltage of the driving transistor 76, and β represents the coefficient in current-voltage (I-V) characteristics of the TFT given by IDS = β (VGS – VT)^2, and IDS represents the drain-source current of the driving transistor 76.

[00106] During the programming cycle of the (n+1)th row, VDATA changes to VP-VB. As a result, the voltage at node A31 changes to VP+VT if VB = (IB/β)1/2. Since a constant current is adopted for all the pixels, the IBIAS line consistently has the appropriate voltage so that there is no necessity to pre-charge the line, resulting in shorter programming time and lower power consumption. More importantly, the voltage of node B31 changes from VP-VB to zero at the beginning of the programming cycle of the nth row. Therefore, the voltage at node A31 changes to (IB/β)1/2+VT, and it is already adjusted to its final value, leading to a fast settling time.

[00107] The settling time of the CBVP pixel circuit is depicted in Figure 14 for different bias currents. A small current can be used as IB here, resulting in lower power consumption.

[00108] Figure 15 illustrates I-V characteristic of the CBVP pixel circuit as well as the total error induced in the pixel current due to a 2-V shift in the threshold voltage

of a driving transistor (e.g. 76 of Figure 12). The result indicates the total error of less than 2% in the pixel current. It is noted that IB=4.5 μA.

[00109] Figure 16 illustrates a display 210 having p-type transistors. The display 210 corresponds to the display 208 of Figure 12. The display 210 employs the CBVP driving scheme as shown in Figure 17. In Figure 12, elements associated with two rows and one column are shown as example. The display 210 may include more than two rows and more than one column.

[00110] The display 210 includes an OLED 90, a storage capacitors 92 and 94, and transistors 96, 98, 100, 102 and 104. The transistor 96 is a driving transistor. The transistors 100 and 104 are switch transistors. The transistors 24, 26 and 28 are p-type transistors. Each transistor has a gate terminal, a first terminal and a second terminal.

[00111] The transistors 96, 98, 100, 102 and 104 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), PMOS technology, or CMOS technology (e.g. MOSFET). The display 210 may form an AMOLED display array.

[00112] In Figure 16, the driving transistor 96 is connected between the anode electrode of the OLED 90 and a voltage supply line VDD.

[00113] Figure 17 illustrates one exemplary operation process applied to the display 210 of Figure 16. Figure 17 corresponds to Figure 13. The CBVP driving scheme of Figure 17 uses IBIAS and VDATA similar to those of Figure 13.

[00114] According to the CBVP driving scheme, the overdrive voltage provided to the driving transistor is generated so as to be independent from its threshold voltage and the OLED voltage.

[00115] The shift(s) of the characteristic(s) of a pixel element(s) (e.g. the threshold voltage shift of a driving transistor and the degradation of a light emitting device under prolonged display operation) is compensated for by voltage stored in a storage capacitor and applying it to the gate of the driving transistor. Thus, the pixel circuit can provide a stable current though the light emitting device without any effect of the shifts, which improves the display operating lifetime. Moreover, because of the

circuit simplicity, it ensures higher product yield, lower fabrication cost and higher resolution than conventional pixel circuits.

[00116] Since the settling time of the pixel circuits described above is much smaller than conventional pixel circuits, it is suitable for large-area display such as high definition TV, but it also does not preclude smaller display areas either.

[00117] It is noted that a driver for driving a display array having a CBVP pixel circuit (e.g. 200, 202 or 204) converts the pixel luminance data into voltage.

[00118] A driving technique for pixels, including voltage-biased current-programmed (VBCP) driving scheme is now described in detail. In the VBCP driving scheme, a pixel current is scaled down without resizing mirror transistors. The VBCP driving scheme uses current to provide for different gray scales (current programming), and uses a bias to accelerate the programming and compensate for a time dependent parameter of a pixel, such as a threshold voltage shift. One of the terminals of a driving transistor is connected to a virtual ground VGND. By changing the voltage of the virtual ground, the pixel current is changed. A bias current IB is added to a programming current IP at a driver side, and then the bias current is removed from the programming current inside the pixel circuit by changing the voltage of the virtual ground.

[00119] Figure 18 illustrates a pixel circuit 212 in accordance with a further embodiment of the present invention. The pixel circuit 212 employs the VBCP driving scheme as described below. The pixel circuit 212 of Figure 18 includes an OLED 110, a storage capacitor 111, a switch network 112, and mirror transistors 114 and 116. The mirror transistors 114 and 116 form a current mirror. The transistor 114 is a programming transistor. The transistor 116 is a driving transistor. The switch network 112 includes switch transistors 118 and 120. Each of the transistors 114, 116, 118 and 120 has a gate terminal, a first terminal and a second terminal.

[00120] The transistors 114, 116, 118 and 120 are n-type TFT transistors. The driving technique applied to the pixel circuit 212 is also applicable to a complementary pixel circuit having p-type transistors as shown in Figure 20.

[00121] The transistors 114, 116, 118 and 120 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), NMOS technology, or CMOS technology (e.g. MOSFET). A plurality of pixel circuits 212 may form an AMOLED display array.

[00122] A select line SEL, a signal line IDATA, a virtual grand line VGND, a voltage supply line VDD, and a common ground are provided to the pixel circuit 150.

[00123] The first terminal of the transistor 116 is connected to the cathode electrode of the OLED 110. The second terminal of the transistor 116 is connected to the VGND. The gate terminal of the transistor 114, the gate terminal of the transistor 116, and the storage capacitor 111 are connected to a connection node A41.

[00124] The gate terminals of the switch transistors 118 and 120 are connected to the SEL. The first terminal of the switch transistor 120 is connected to the IDATA. The switch transistors 118 and 120 are connected to the first terminal of the transistor 114. The switch transistor 118 is connected to node A41.

[00125] Figure 19 illustrates an exemplary operation for the pixel circuit 212 of Figure 18. Referring to Figures 18 and 19, current scaling technique applied to the pixel circuit 212 is described in detail. The operation of the pixel circuit 212 has a programming cycle X41, and a driving cycle X42.

[00126] The programming cycle X41: SEL is high. Thus, the switch transistors 118 and 120 are on. The VGND goes to a bias voltage VB. A current (IB+IP) is provided through the IDATA, where IP represents a programming current, and IB represents a bias current. A current equal to (IB+IP) passes through the switch transistors 118 and 120.

[00127] The gate-source voltage of the driving transistor 116 is self-adjusted to:

$$VGS = \sqrt{\frac{IP + IB}{\beta}} + VT \qquad (9)$$

where VT represents the threshold voltage of the driving transistor 116, and β represents the coefficient in current-voltage (I-V) characteristics of the TFT given by

IDS =β(VGS -VT)^2. IDS represents the drain-source current of the driving transistor 116.

[00128] The voltage stored in the storage capacitor 111 is:

$$VCS = \sqrt{\frac{IP + IB}{\beta}} - VB + VT \qquad (10)$$

where VCS represents the voltage stored in the storage capacitor 111.

[00129] Since one terminal of the driving transistor 116 is connected to the VGND, the current flowing through the OLED 110 during the programming time is:

$$Ipixel = IP + IB + \beta \cdot (VB)^2 - 2\sqrt{\beta} \cdot VB \cdot \sqrt{(IP + IB)} \qquad (11)$$

where Ipixel represents the pixel current flowing through the OLED 110.

[00130] If IB >> IP, the pixel current Ipixel can be written as:

$$Ipixel = IP + (IB + \beta \cdot (VB)^2 - 2\sqrt{\beta} \cdot VB \cdot \sqrt{IB}) \qquad (12)$$

[00131] VB is chosen properly as follows:

$$VB = \sqrt{\frac{IB}{\beta}} \qquad (13)$$

[00132] The pixel current Ipixel becomes equal to the programming current IP. Therefore, it avoids unwanted emission during the programming cycle.

[00133] Since resizing is not required, a better matching between two mirror transistors in the current-mirror pixel circuit can be achieved.

[00134] Figure 20 illustrates a pixel circuit 214 having p-type transistors. The pixel circuit 214 corresponds to the pixel circuit 212 of Figure 18. The pixel circuit 214 employs the VBCP driving scheme as shown Figure 21. The pixel circuit 214 includes an OLED 130, a storage capacitor 131, a switch network 132, and mirror transistors 134 and 136. The mirror transistors 134 and 136 form a current mirror. The transistor 134 is a programming transistor. The transistor 136 is a driving transistor. The switch

network 132 includes switch transistors 138 and 140. The transistors 134, 136, 138 and 140 are p-type TFT transistors. Each of the transistors 134, 136, 138 and 140 has a gate terminal, a first terminal and a second terminal.

[00135] The transistors 134, 136, 138 and 140 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFTs), PMOS technology, or CMOS technology (e.g. MOSFET). A plurality of pixel circuits 214 may form an AMOLED display array.

[00136] A select line SEL, a signal line IDATA, a virtual grand line VGND, and a voltage supply line VSS are provided to the pixel circuit 214.

[00137] The transistor 136 is connected between the VGND and the cathode electrode of the OLED 130. The gate terminal of the transistor 134, the gate terminal of the transistor 136, the storage capacitor 131 and the switch network 132 are connected at node A42.

[00138] Figure 21 illustrates an exemplary operation for the pixel circuit 214 of Figure 20. Figure 21 corresponds to Figure 19. The VBCP driving scheme of Figure 21 uses IDATA and VGND similar to those of Figure 19.

[00139] The VBCP technique applied to the pixel circuit 212 and 214 is applicable to current programmed pixel circuits other than current mirror type pixel circuit.

[00140] For example, the VBCP technique is suitable for the use in AMOLED displays. The VBCP technique enhances the settling time of the current-programmed pixel circuits display, e.g. AMOLED displays.

[00141] It is noted that a driver for driving a display array having a VBCP pixel circuit (e.g. 212, 214) converts the pixel luminance data into current.

[00142] Figure 22 illustrates a driving mechanism for a display array 150 having a plurality of CBVP pixel circuits 151 (CBVP1-1, CBVP1-2, CBVP2-1, CBVP2-2). The CBVP pixel circuit 151 is a pixel circuit to which the CBVP driving scheme is applicable. For example, the CBVP pixel circuit 151 may be the pixel circuit shown in

Figure 1, 5, 8, 10, 12 or 16. In Figure 22, four CBVP pixel circuits 151 are shown as example. The display array 150 may have more than four or less than four CBVP pixel circuits 151.

[00143] The display array 150 is an AMOLED display where a plurality of the CBVP pixel circuits 151 are arranged in rows and columns. VDATA1 (or VDATA 2) and IBIAS1 (or IBIAS2) are shared between the common column pixels while SEL1 (or SEL2) is shared between common row pixels in the array structure.

[00144] The SEL1 and SEL2 are driven through an address driver 152. The VDATA1 and VDATA2 are driven through a source driver 154. The IBIAS1 and IBIAS2 are also driven through the source driver 154. A controller and scheduler 156 is provided for controlling and scheduling programming, calibration and other operations for operating the display array, which includes the control and schedule for the CBVP driving scheme as described above.

[00145] Figure 23 illustrates a driving mechanism for a display array 160 having a plurality of VBCP pixel circuits. In Figure 23, the pixel circuit 212 of Figure 18 is shown as an example of the VBCP pixel circuit. However, the display array 160 may include any other pixel circuits to which the VBCP driving scheme described is applicable.

[00146] SEL1 and SEL2 of Figure 23 correspond to SEL of Figure 18. VGND1 and VGAND2 of Figure 23 correspond to VDATA of Figure 18. IDATA1 and IDATA 2 of Figure 23 correspond to IDATA of Figure 18. In Figure 23, four VBCP pixel circuits are shown as example. The display array 160 may have more than four or less than four VBCP pixel circuits.

[00147] The display array 160 is an AMOLED display where a plurality of the VBCP pixel circuits are arranged in rows and columns. IDATA1 (or IDATA2) is shared between the common column pixels while SEL1 (or SEL2) and VGND1 (or VGND2) are shared between common row pixels in the array structure.

[00148] The SEL1, SEL2, VGND1 and VGND2 are driven through an address driver 162. The IDATA1 and IDATA are driven through a source driver 164. A

controller and scheduler 166 is provided for controlling and scheduling programming, calibration and other operations for operating the display array, which includes the control and schedule for the VBCP driving scheme as described above.

[00149] Figure 24 illustrates a pixel circuit 400 in accordance with a further embodiment of the present invention. The pixel circuit 400 of Figure 24 is a 3-TFT current-biased voltage programmed pixel circuit and employs the CBVP driving scheme. The driving scheme improves the display lifetime and yield by compensating for the mismatches.

[00150] The pixel circuit 400 includes an OLED 402, a storage capacitor 404, a driving transistor 406, and switch transistors 408 and 410. Each transistor has a gate terminal, a first terminal and a second terminal. The transistors 406, 408 and 410 are p-type TFT transistors. The driving technique applied to the pixel circuit 400 is also applicable to a complementary pixel circuit having n-type transistors as well understood by one of ordinary skill in the art.

[00151] The transistors 406, 408 and 410 may be implemented using poly silicon, nano/micro (crystalline) silicon, amorphous silicon, CMOS, organic semiconductor, metal organic technologies, or combination thereof. A plurality of pixel circuits 400 may form an active matrix array. The driving scheme applied to the pixel circuit 400 compensates for temporal and spatial non-uniformities in the active matrix display.

[00152] A select line SEL, a signal line Vdata, a bias line Ibias, and a voltage supply line Vdd are connected to the pixel circuit 400. The bias line Ibias provides a bias current (Ibias) that is defined based on display specifications, such as lifetime, power, and device performance and uniformity.

[00153] The first terminal of the driving transistor 406 is connected to the voltage supply line Vdd. The second terminal of the driving transistor 406 is connected to the OLED 402 at node B20. One terminal of the capacitor 404 is connected to the signal line Vdata, and the other terminal of the capacitor 404 is connected to the gate terminal of the driving transistor 406 at node A20.

[00154] The gate terminals of the switch transistors 408 and 410 are connected to the select line SEL. The switch transistor 408 is connected between node A20 and node B20. The switch transistor 410 is connected between the node B20 and the bias line Ibias.

[00155] For the pixel circuit 400, a predetermined fixed current (Ibias) is provided through the transistor 410 to compensate for all spatial and temporal non-uniformities and voltage programming is used to divide the current in different current levels required for different gray scales.

[00156] As shown in Figure 25, the operation of the pixel circuit 400 includes a programming phase X61 and a driving phase X62. Vdata [j] of Figure 25 corresponds to Vdd of Figure 24. Vp[k,j] of Figure 25 (k=1, 2, ..., n) represents the kth programming voltage on Vdata [j] where "j" is the column number.

[00157] Referring to Figures 24 and 25, during the programming cycle X61, SEL is low so that the switch transistors 408 and 410 are on. The bias current Ibias is applied via the bias line Ibias to the pixel circuit 400, and the gate terminal of the driving transistor 406 is self-adjusted to allow all the current passes through source-drain of the driving transistor 406. At this cycle, Vdata has a programming voltage related to the gray scale of the pixel. During the driving cycle X62, the switch transistors 408 and 410 are off, and the current passes through the driving transistor 406 and the OLED 402.

[00158] Figure 26 is a diagram showing a pixel circuit 420 in accordance with a further embodiment of the present invention. The pixel circuit 420 of Figure 26 is a 6-TFT current-biased voltage programmed pixel circuit and employs the CBVP driving scheme, with emission control. This driving scheme improves the display lifetime and yield by compensating for the mismatches.

[00159] The pixel circuit 420 includes an OLED 422, a storage capacitor 424, and transistors 426-436. Each transistor has a gate terminal, a first terminal and a second terminal. The transistors 426-436 are p-type TFT transistors. The driving technique applied to the pixel circuit 420 is also applicable to a complementary pixel circuit having n-type transistors as well understood by one of ordinary skill in the art.

[00160] The transistors 426-436 may be implemented using poly silicon, nano/micro (crystalline) silicon, amorphous silicon, CMOS, organic semiconductor, metal organic technologies, or combination thereof. A plurality of pixel circuits 420 may form an active matrix array. The driving scheme applied to the pixel circuit 420 compensates for temporal and spatial non-uniformities in the active matrix display.

[00161] One select line SEL, a signal line Vdata, a bias line Ibias, a voltage supply line Vdd, a reference voltage line Vref, and an emission signal line EM are connected to the pixel circuit 420. The bias line Ibias provides a bias current (Ibias) that is defined based on display specifications, such as lifetime, power, and device performance and uniformity. The reference voltage line Vref provides a reference voltage (Vref). The reference voltage Vref may be determined based on the bias current Ibias and the display specifications that may include gray scale and/or contrast ratio. The signal line EM provides an emission signal EM that turns on the pixel circuit 420. The pixel circuit 420 goes to emission mode based on the emission signal EM.

[00162] The gate terminal of the transistor 426, one terminal of the transistor 432 and one terminal of the transistor 434 are connected at node A21. One terminal of the capacitor 424, one terminal of the transistor 428 and the other terminal of the transistor 434 are connected at node B21. The other terminal of the capacitor 424, one terminal of the transistor 430, one terminal of the transistor 436, and one terminal of the transistor 426 are connected at node C21. The other terminal of the transistor 430 is connected to the bias line Ibias. The other terminal of the transistor 432 is connected to the reference voltage line Vref. The select line SEL is connected to the gate terminals of the transistors 428, 430 and 432. The select line EM is connected to the gate terminals of the transistors 434, and 436. The transistor 426 is a driving transistor. The transistors 428, 430, 432, 434, and 436 are switching transistors.

[00163] For the pixel circuit 420, a predetermined fixed current (Ibias) is provided through the transistor 430 while the reference voltage Vref is applied to the gate terminal of the transistor 426 through the transistor 432 and a programming voltage VP is applied to the other terminal of the storage capacitor 424 (i.e., node B21) through the transistor 428. Here, the source voltage of the transistor 426 (i.e., voltage of node C21) will be self- adjusted to allow the bias current goes through the transistor 426 and

thus it compensates for all spatial and temporal non-uniformities. Also, voltage programming is used to divide the current in different current levels required for different gray scales.

[00164] As shown in Figure 27, the operation of the pixel circuit 420 includes a programming phase X71 and a driving phase X72.

[00165] Referring to Figures 26 and 27, during the programming cycle X71, SEL is low so that the transistors 428, 430 and 432 are on, a fixed bias current is applied to Ibias line, and the source of the transistor 426 is self-adjusted to allow all the current passes through source-drain of the transistor 426. At this cycle, Vdata has a programming voltage related to the gray scale of the pixel and the capacitor 424 stores the programming voltage and the voltage generated by current for mismatch compensation. During the driving cycle X72, the transistors 428, 430 and 432 are off, while the transistors 434 and 436 are on by the emission signal EM. During this driving cycle X72, the transistor 426 provides current for the OLED 422.

[00166] In Figure 25, the entire display is programmed, then it is light up (goes to emission mode). By contrast, in Figure 27, each row can light up after programming by using the emission line EM.

[00167] In the operations of Figures 25 and 27, the bias line provides a predetermined fixed bias current. However, the bias current Ibias may be adjustable, and the bias current Ibias may be adjusted during the operation of the display.

[00168] Figure 28 illustrates an example of a display system having array structure for implementation of the CBVP driving scheme. The display system 450 of Figure 28 includes a pixel array 452 having a plurality of pixels 454, a gate driver 456, a source driver 458 and a controller 460 for controlling the drivers 456 and 458. The gate driver 456 operates on address (select) lines (e.g., SEL [1], SEL[2], ...). The source driver 458 operates on data lines (e.g., Vdata [1], Vdata [2], ...). The display system 450 includes a calibrated current mirrors block 462 for operating on bias lines (e.g., Ibias [1], Ibias [2]) using a reference current Iref. The block 462 includes a plurality of calibrated current mirrors, each for the corresponding Ibias. The reference

current Iref may be provided to the calibrated current mirrors block 462 through a switch.

[00169] The pixel circuit 454 may be the same as the pixel circuit 400 of Figure 24 or the pixel circuit 420 of Figure 26 where SEL [i] (i=1, 2, ...) corresponds to SEL of Figure 24 or 26, Vdata [j] (j=1, 2, ...) corresponds to Vdata of Figure 24 or 26, and Ibias [j] (j=1, 2, ...) corresponds to Ibias of Figure 24 or 26. When using the pixel circuit 420 of Figure 26 as the pixel circuit 454, a driver at the peripheral of the display, such as the gate driver 456, controls each emission line EM.

[00170] In Figure 28, the current mirrors are calibrated with a reference current source. During the programming cycle of the panel (e.g., X61 of Figure 25, X71 of Figure 27), the calibrated current mirrors (block 462) provide current to the bias line Ibias. These current mirrors can be fabricated at the edge of the panel.

[00171] Figure 29 illustrates another example of a display system having array structure for implementation of the CBVP driving scheme. The display system 470 of Figure 29 includes a pixel array 472 having a plurality of pixels 474, a gate driver 476, a source driver 478 and a controller 480 for controlling the drivers 476 and 478. The gate driver 476 operates on address (select) lines (e.g., SEL[0], SEL [1], SEL[2], ...). The source driver 478 operates on data lines (e.g., Vdata [1], Vdata [2], ...). The display system 470 includes a calibrated current sources block 482 for operating on bias lines (e.g., Ibias [1], Ibias [2]) using Vdata lines. The block 482 includes a plurality of calibrated current sources, each being provided for the Ibias line.

[00172] The pixel circuit 474 may be the same as the pixel circuit 400 of Figure 24 or the pixel circuit 420 of Figure 26 where SEL [i] (i=1, 2, ...) corresponds to SEL of Figure 24 or 26, Vdata [j] (j=1, 2, ...) corresponds to Vdata of Figure 24 or 26, and Ibias [j] (j=1, 2, ...) corresponds to Ibias of Figure 24 or 26. When using the pixel circuit 420 of Figure 26 as the pixel circuit 474, a driver at the peripheral of the display, such as the gate driver 456, controls each emission line EM.

[00173] Each current source 482 includes a voltage to current convertor that converts voltage via Vdata line to current. One of the select lines is used to operate a switch 490 for connecting Vdata line to the current source 482. In this example, address

line SEL [0] operates the switch 490. The current sources 482 are treated as one row of the display (i.e., the 0^{th} row). After the conversion of voltage on Vdata line at the current source 482, Vdata line is used to program the real pixel circuits 474 of the display.

[00174] A voltage related to each of the current sources is extracted at the factory and is stored in a memory (e.g. flash, EPROM, or PROM). This voltage (calibrated voltage) may be different for each current source due to their mismatches. At the beginning of each frame, the current sources 482 are programmed through the source driver 478 using the stored calibrated voltages so that all the current sources 482 provides the same current.

[00175] In Figure 28, the bias current (Ibias) is generated by the current mirror 462 with the reference current Iref. However, the system 450 of Figure 28 may use the current source 482 to generate Ibias. In Figure 29, the bias current (Ibias) is generated by the current converter of the current source 482 with Vdata line. However, the system 470 of Figure 29 may use the current mirror 462 of Figure 28.

[00176] Effect of spatial mismatches on the image quality of panels using different driving scheme is depicted in Figures 30-32. The image of display with conventional 2-TFT pixel circuit is suffering from both threshold voltage mismatches and mobility variations (Figure 30). On the other hand, the voltage programmed pixel circuits without the bias line Ibias may control the effect of threshold voltage mismatches, however, they may suffer from the mobility variations (Figure 31) whereas the current-biased voltage-programmed (CBVP) driving scheme in the embodiments can control the effect of both mobility and threshold voltage variations (Figure 32).

[00177] The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A pixel circuit comprising:

a light emitting device;

a driving transistor for providing a pixel current to the light emitting device, the driving transistor having a gate terminal, a first terminal coupled to the light emitting device, and a second terminal;

a storage capacitor provided between a data line for providing programming voltage data and the gate terminal of the driving transistor;

a first switch transistor provided between the gate terminal of the driving transistor and the first terminal of the driving transistor; and

a second switch transistor provided between the first terminal of the driving transistor and a bias line for providing a bias current to the first terminal of the driving transistor during a programming cycle.

2. A pixel circuit as claimed in claim 1, wherein the gate terminal of the first switch transistor and the gate terminal of the second switch transistor are operated by a single select line.

3. A pixel circuit as claimed in claim 1, wherein the second switch transistor includes a first terminal coupled to the bias line and a second terminal coupled to a connection node between the light emitting device and the driving transistor.

4. A pixel circuit as claimed in claim 1, wherein the programming voltage data includes a plurality of voltage signals for dividing current in different current levels for different gray scales.

5. A pixel circuit as claimed in claim 1, wherein the light emitting device includes an organic light emitting diode.

6. A pixel circuit as claimed in claim 1, wherein at least one of the transistors is a thin film transistor.

7. A pixel circuit as claimed in claim 1, wherein the transistor is implemented using poly silicon, nano/micro (crystalline) silicon, amorphous silicon, CMOS, organic semiconductor, metal organic technologies, or combination thereof.

8. A pixel circuit as claimed in claim 1, wherein the pixel circuit forms an active matrix array.

9. A pixel circuit comprising:

a light emitting device;

a storage capacitor having a first terminal and a second terminal;

a driving transistor for providing a pixel current to the light emitting device, the driving transistor having a gate terminal, a first terminal coupled to the first terminal of the storage capacitor, and a second terminal coupled to the light emitting device;

a first switch transistor operated by a first select line and provided between the second terminal of the storage capacitor and a data line for providing programming voltage data;

a second switch transistor operated by the first select line and provided between the first terminal of the storage capacitor and a bias line for providing a bias current to the first terminal of the driving transistor during a programming cycle; and

an emission control circuit for setting the pixel circuit into an emission mode.

10. A pixel circuit as claimed in claim 9, wherein the emission control circuit comprises:

a third switch transistor coupled between a first potential and the first terminal of the driving transistor;

a fourth switch transistor coupled between the second terminal of the storage capacitor and the gate terminal of the driving transistor; and

a fifth switch transistor coupled between the gate terminal of the driving transistor and a second potential.

11. A pixel circuit as claimed in claim 10, wherein the third and fourth switch transistors are operated by a second select line, and wherein the fifth switch transistor is operated by the first select line.

12. A pixel circuit as claimed in claim 9, wherein the programming voltage data includes a plurality of voltage signals for dividing current in different current levels for different gray scales.

13. A pixel circuit as claimed in claim 9, wherein the light emitting device includes an organic light emitting diode.

14. A pixel circuit as claimed in claim 9, wherein at least one of the transistors is a thin film transistor.

15. A pixel circuit as claimed in claim 9, wherein the transistor is implemented using poly silicon, nano/micro (crystalline) silicon, amorphous silicon, CMOS, organic semiconductor, metal organic technologies, or combination thereof.

16. A pixel circuit as claimed in claim 9, wherein the pixel circuit forms an active matrix array.

17. A display system, comprising:

a pixel array having a plurality of pixel circuits, each defined in claim 1;

a first driver for selecting the pixel circuit;

a second driver for providing the programming voltage data; and

a current source for operating on the bias line.

18. A display system as claimed in claim 17, wherein the current source comprises at least one of:

a calibrated current mirror for operating on the bias line based on a reference current;

a voltage to current convertor for converting voltage to the bias current.

19. A display system as claimed in claim 17, wherein the current source is calibrated via a data stored in a memory.

20. A display system, comprising:

a pixel array having a plurality of pixel circuits, each defined in claim 9;

a first driver for selecting the pixel circuit;

a second driver for providing the programming voltage data; and

a current source for operating on the bias line.

21. A display system as claimed in claim 20, wherein the current source comprises at least one of:

a calibrated current mirror for operating on the bias line based on a reference current;

a voltage to current convertor for converting voltage to the bias current.

22. A display system as claimed in claim 20, wherein the current source is calibrated via a data stored in a memory.

23. A method of driving a pixel circuit, the pixel circuit having a driving transistor for providing a pixel current to a light emitting device, a storage capacitor coupled to a data line, and a switch transistor coupled to the gate terminal of the driving transistor and the storage capacitor, the method comprising:

at a programming cycle, selecting the pixel circuit, providing a bias current to a connection between the driving transistor and the light emitting device, and providing programming voltage data from the data line to the pixel circuit.

24. A method of driving a pixel circuit, the pixel circuit having a driving transistor for providing a pixel current to a light emitting device, a switch transistor coupled to a data line, and a storage capacitor coupled to the switch transistor and the driving transistor, the method comprising:

at a programming cycle, selecting the pixel circuit, providing a bias current to a first terminal of the driving transistor, and providing programming voltage data from the data line to a first terminal of the storage capacitor, the second terminal of the storage capacitor being coupled to the first terminal of the driving transistor, a second terminal of the driving transistor being coupled to the light emitting device; and

at a driving cycle, setting an emission mode in the pixel circuit.

25. A pixel circuit as claimed in claim 1, wherein the bias current is a predetermined fixed current.

26. A pixel circuit as claimed in claim 9, wherein the bias current is a predetermined fixed current.

27. A method as claimed in claim 23, wherein the bias current is a predetermined fixed current.

28. A method as claimed in claim 24, wherein the bias current is a predetermined fixed current.

200

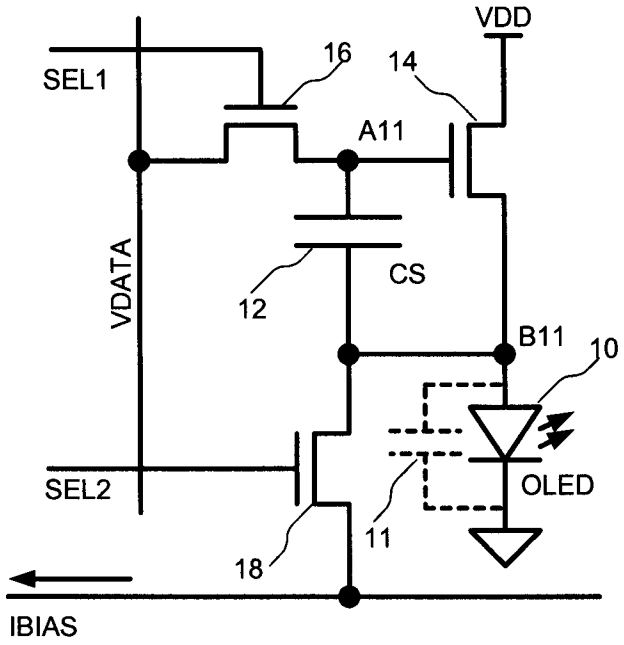

FIG.1

$$V1 = VB - \sqrt{\frac{IB}{\beta}} - VT$$

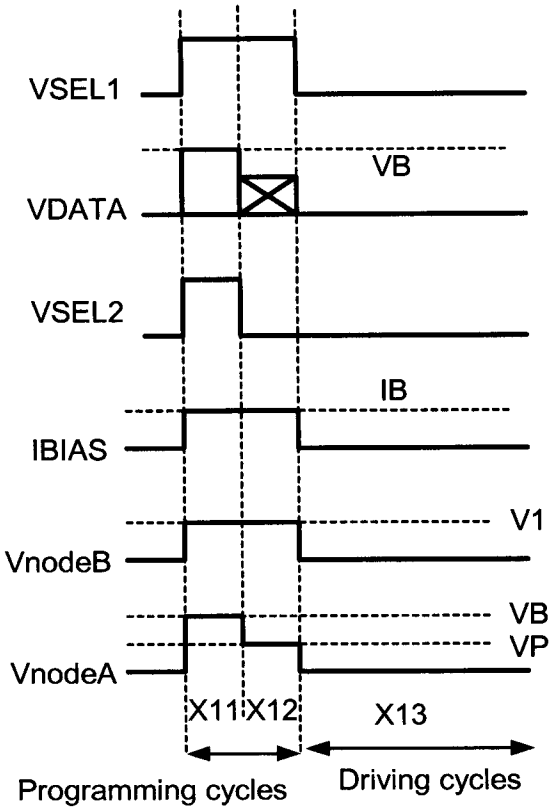

FIG.2

$$V1 = VB - \sqrt{\frac{IB}{\beta}} - VT$$

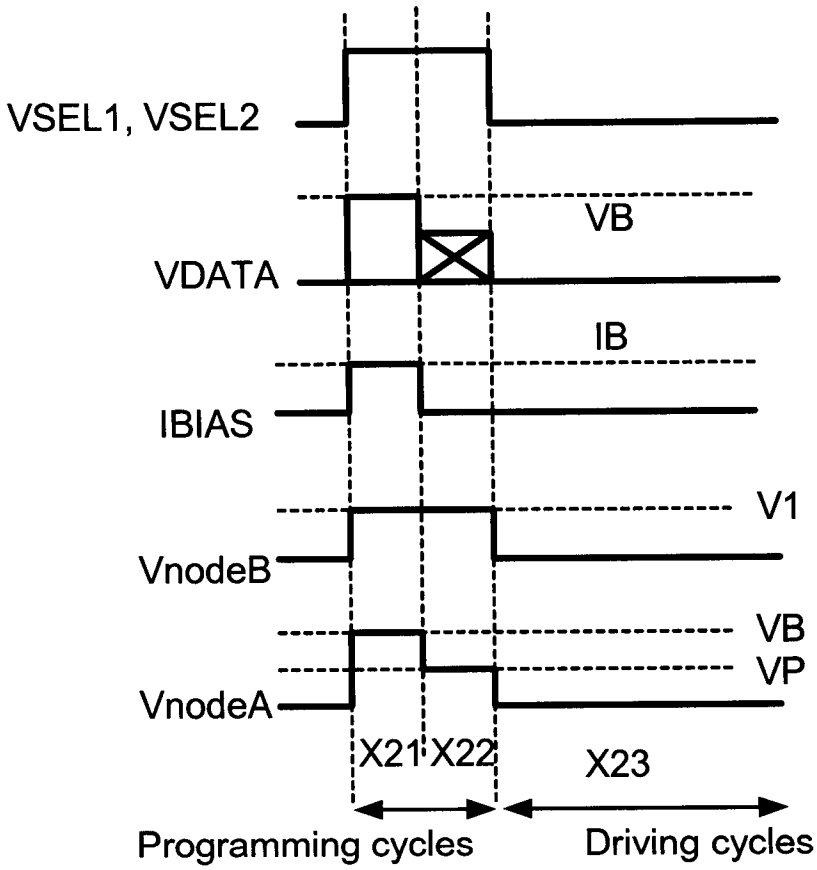

FIG.3

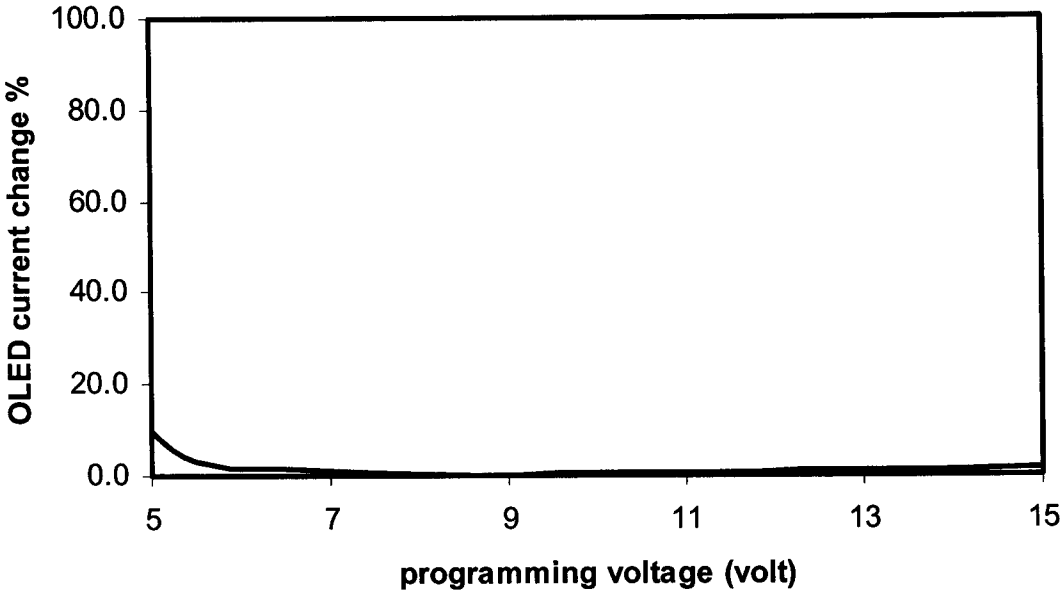
100.0
80.0
60.0
40.0
20.0
0.0
OLED current change %
5
7
9
11
13
15
programming voltage (volt)

FIG. 4

202

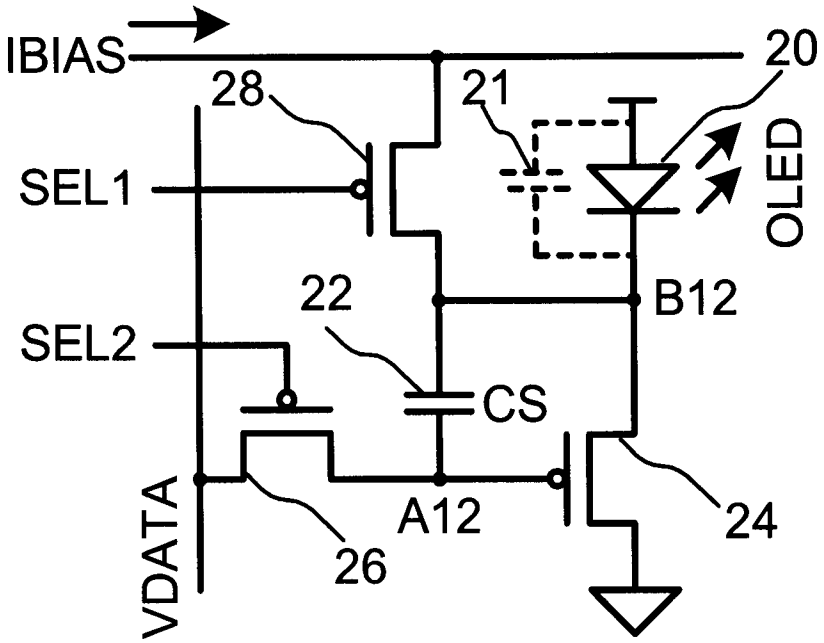

FIG. 5

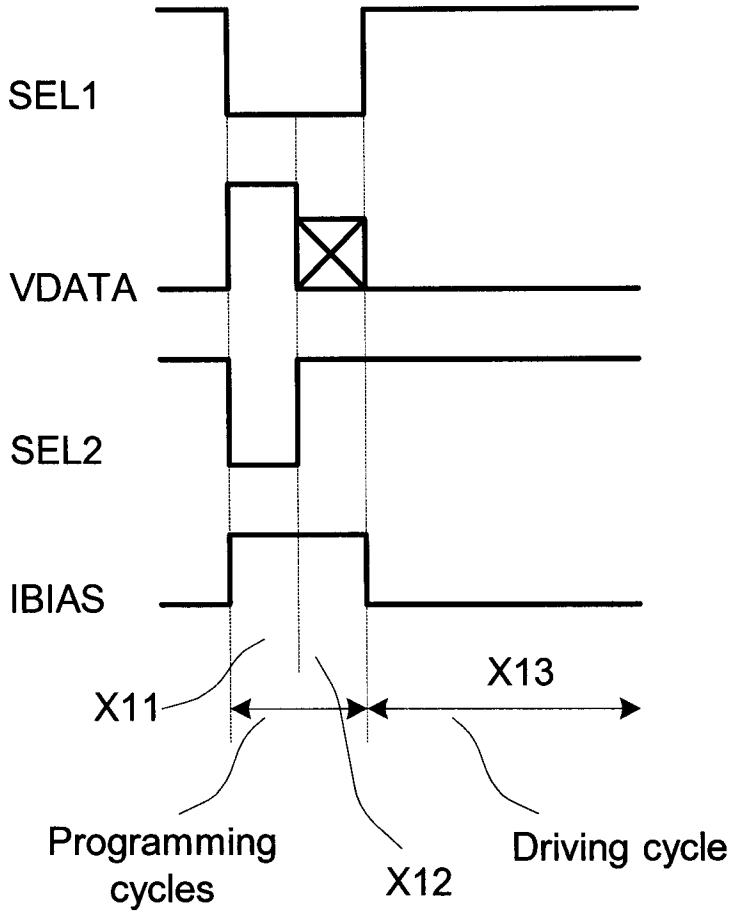
SEL1
VDATA
SEL2
IBIAS
X11
X13
Programming cycles
X12
Driving cycle

FIG. 6

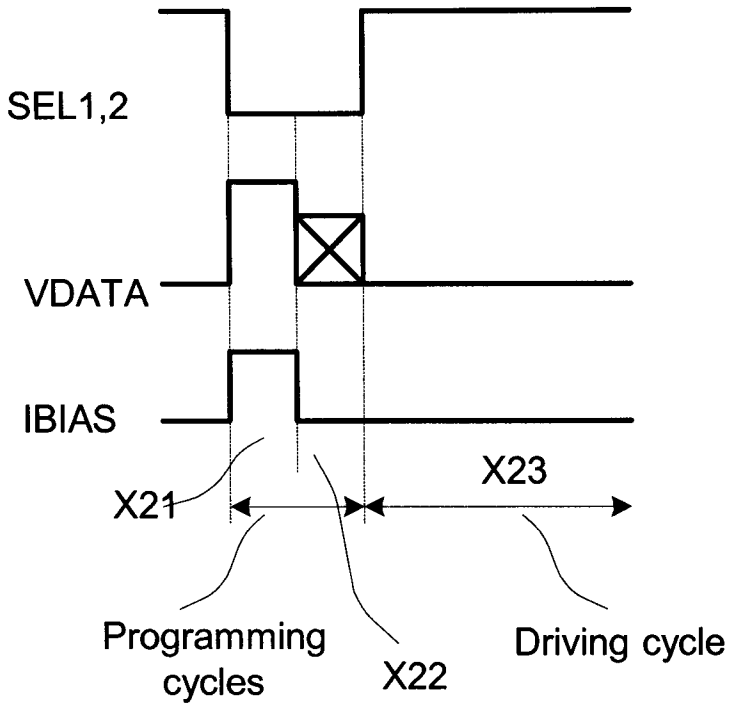
SEL1,2
VDATA
IBIAS
X21
X23
Programming cycles
X22
Driving cycle

FIG. 7

204

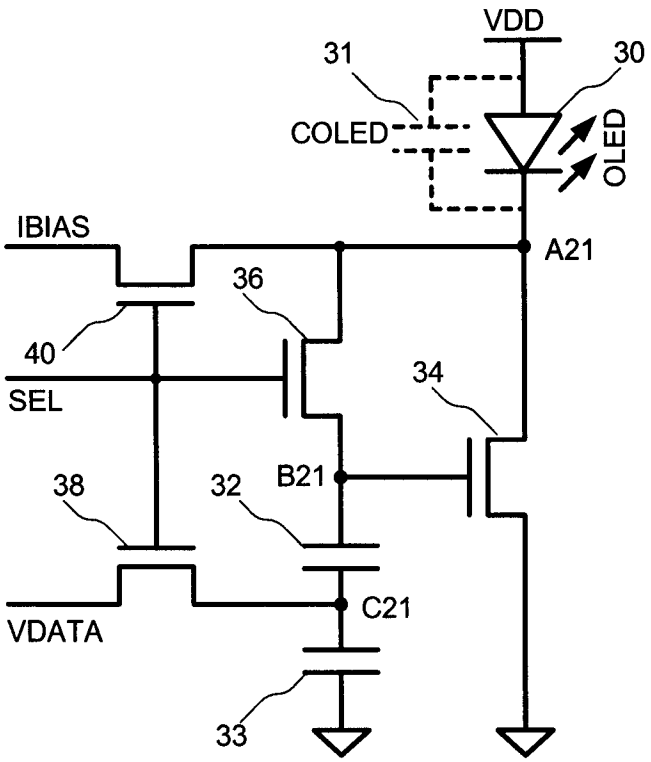
VDD
31
30
COLED
OLED
IBIAS
A21
36
40
34
SEL
38
32
B21
C21
VDATA
33

FIG.8

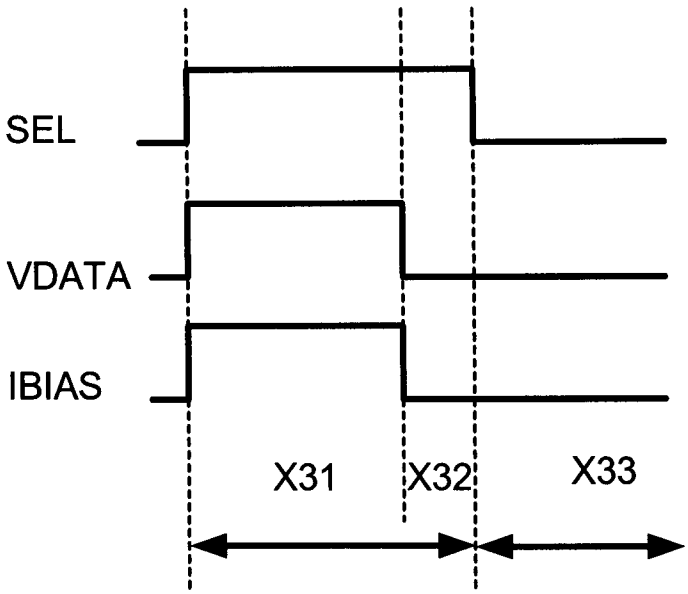

FIG.9

206

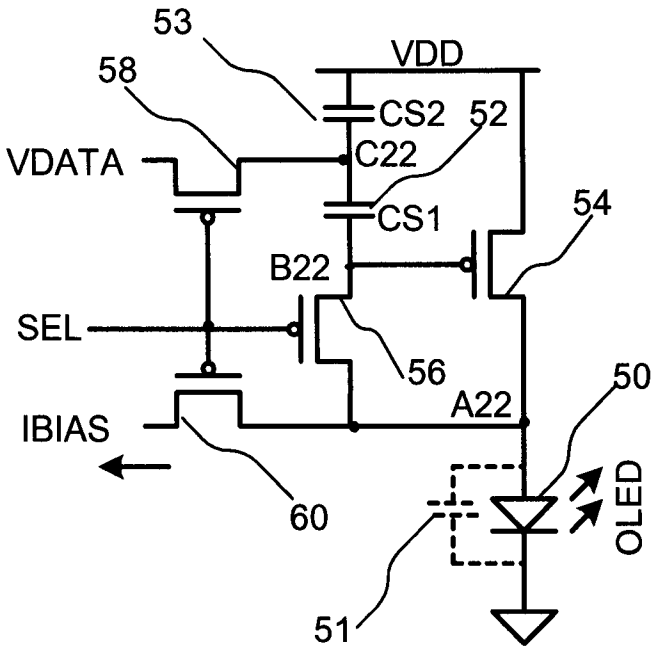
53
VDD
58
CS2
52
VDATA
C22
CS1
54
B22
SEL
56
50
A22
IBIAS
60
OLED
51

FIG.10

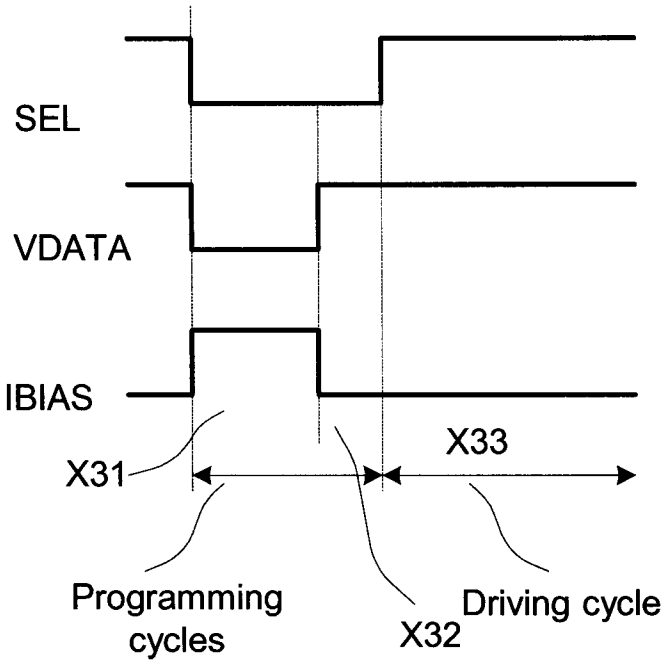
SEL
VDATA
IBIAS
X31
X33
Programming cycles
X32
Driving cycle

FIG.11

208

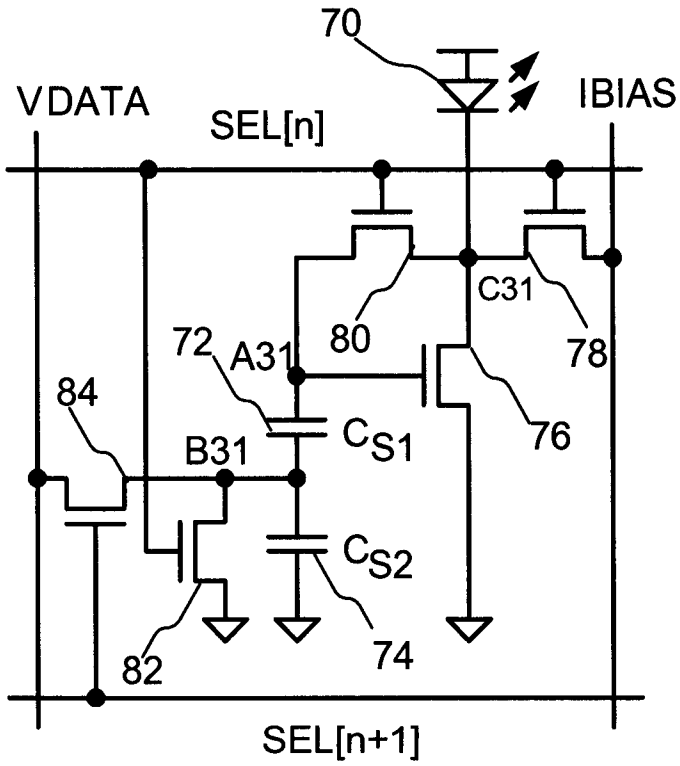
70
VDATA
SEL[n]
IBIAS
C31
72
A31
80
78
84
B31
C_{S1}
76
C_{S2}
82
74
SEL[n+1]

FIG.12

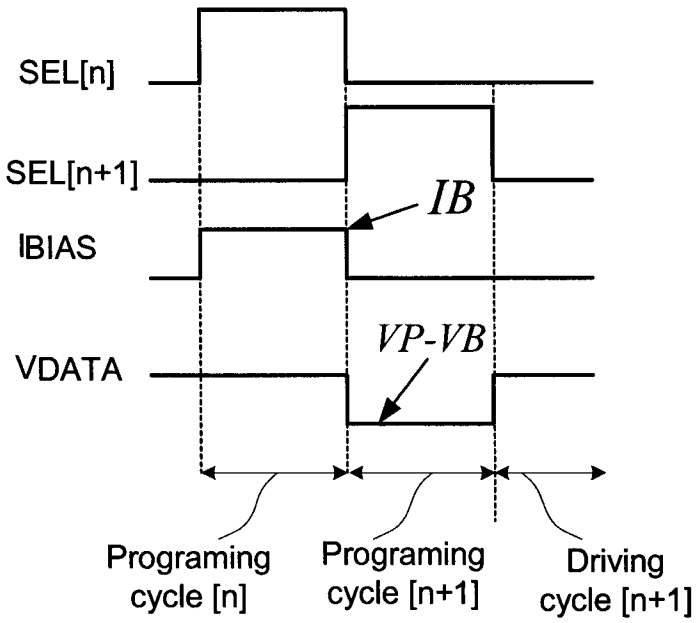
SEL[n]
SEL[n+1]
IBIAS
VDATA
IB
VP-VB
Programing cycle [n]
Programing cycle [n+1]
Driving cycle [n+1]

FIG.13

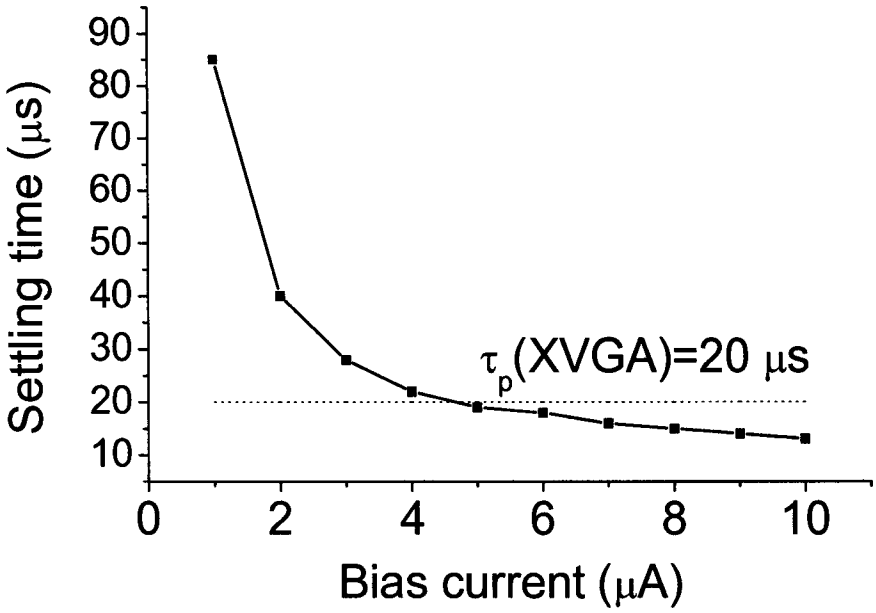
Settling time (μs)
90
80
70
60
50
40
30
20
10
0
2
4
6
8
10
Bias current (μA)
τp(XVGA)=20 μs

FIG.14

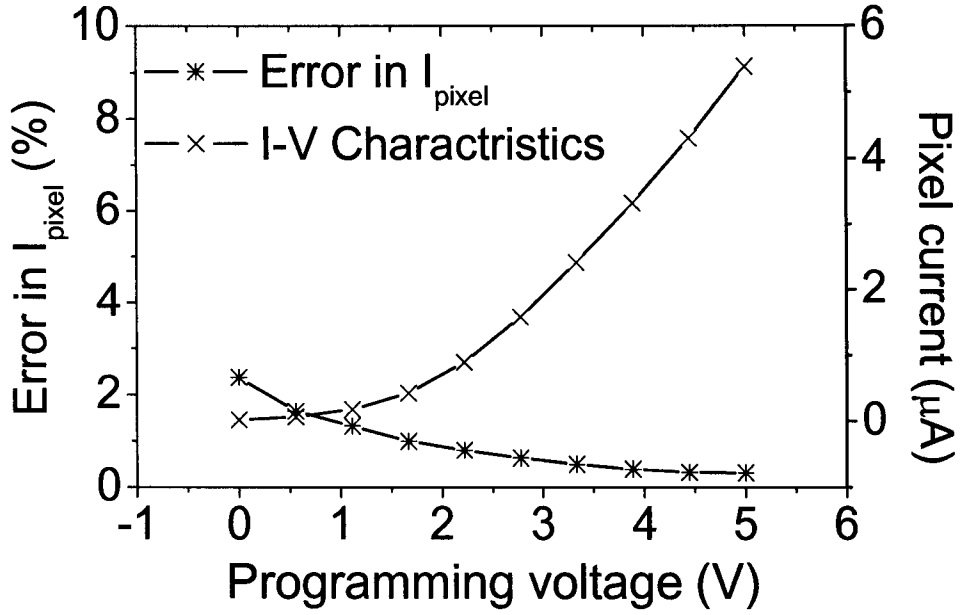
Error in I_{pixel}
I-V Charactristics
Error in I_{pixel} (%)
Pixel current (μA)
Programming voltage (V)
10
8
6
4
2
0
6
4
2
0
-1
0
1
2
3
4
5
6

FIG.15

210

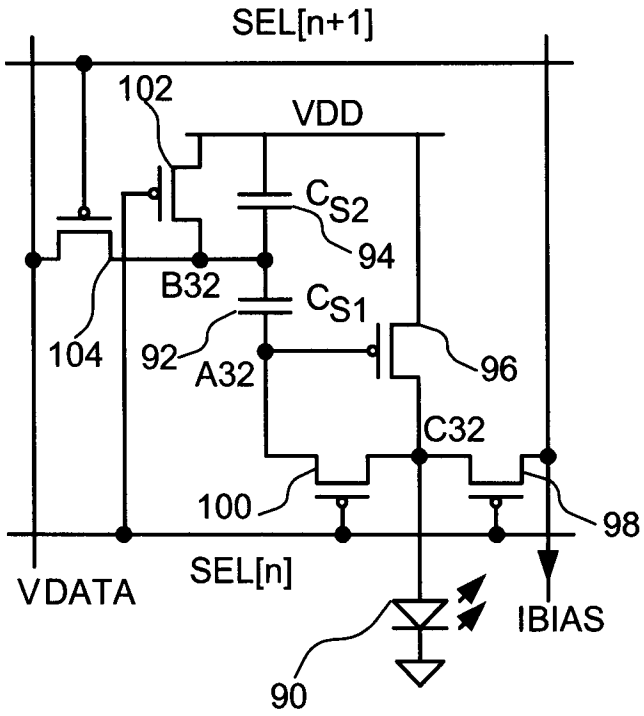
SEL[n+1]
102
VDD
C_{S2}
94
B32
C_{S1}
104
92
A32
96
C32
100
98
VDATA
SEL[n]
IBIAS
90

FIG.16

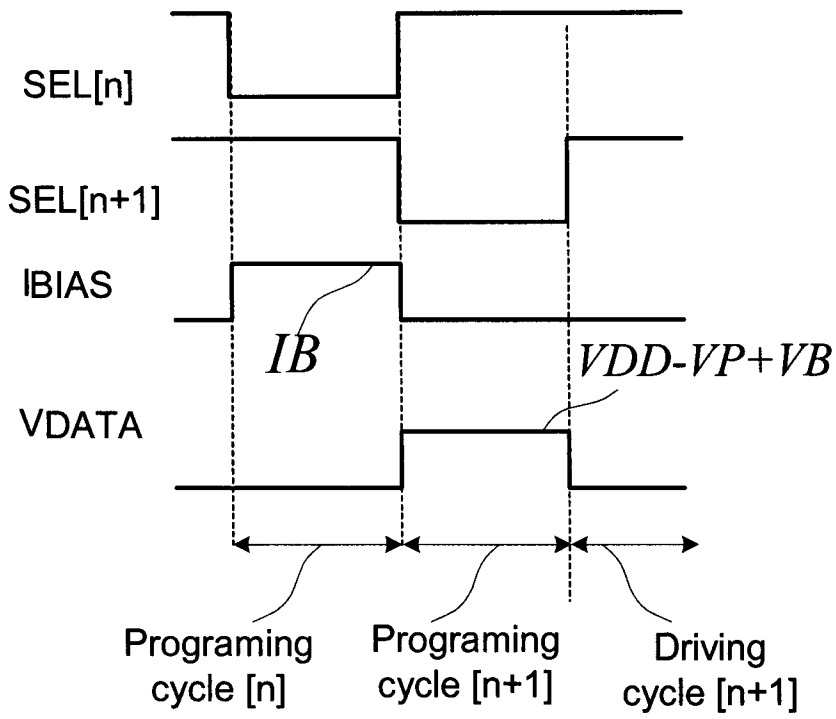
SEL[n]
SEL[n+1]
IBIAS
IB
VDD-VP+VB
VDATA
Programing cycle [n]
Programing cycle [n+1]
Driving cycle [n+1]

FIG.17

212

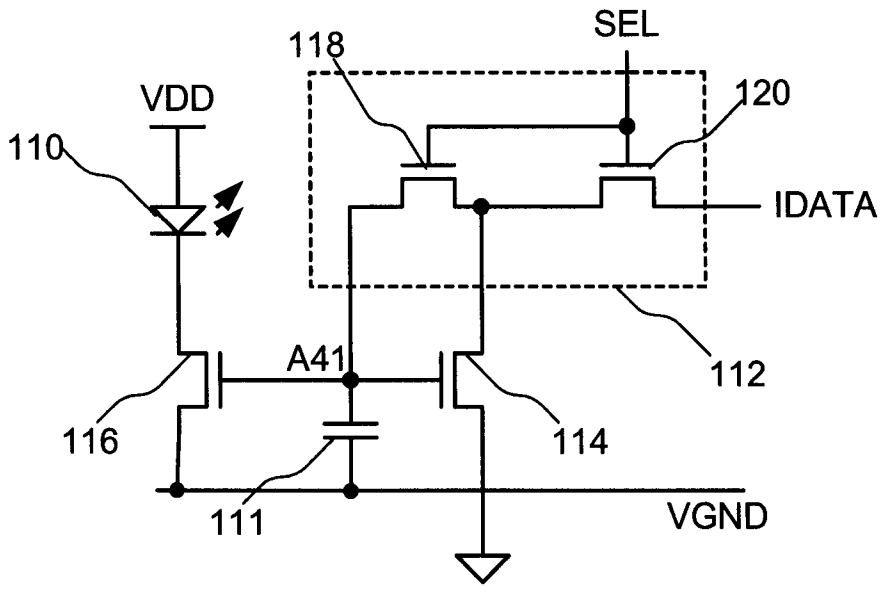

FIG.18

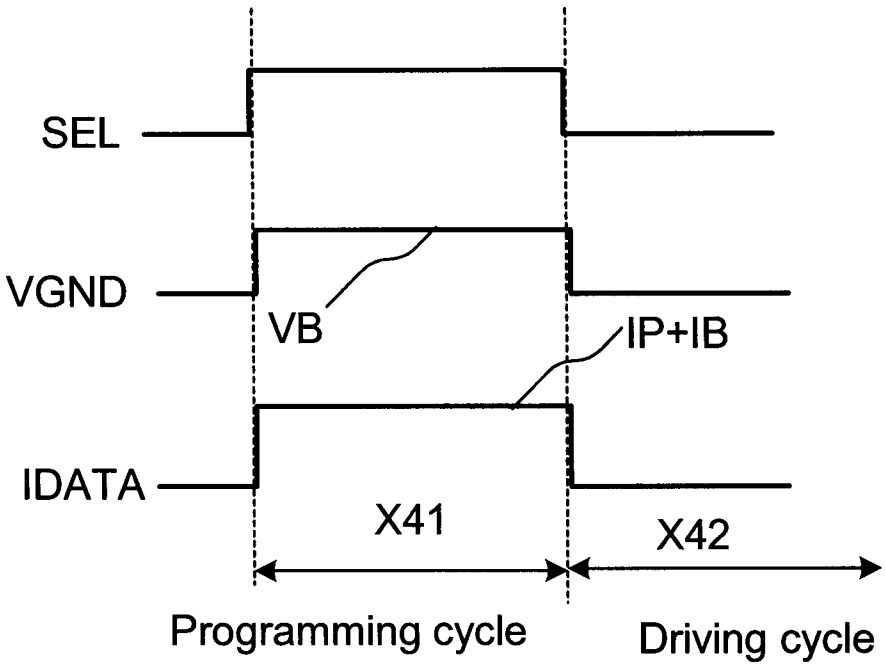
SEL
VGND
VB
IP+IB
IDATA
X41
X42
Programming cycle
Driving cycle

FIG.19

214

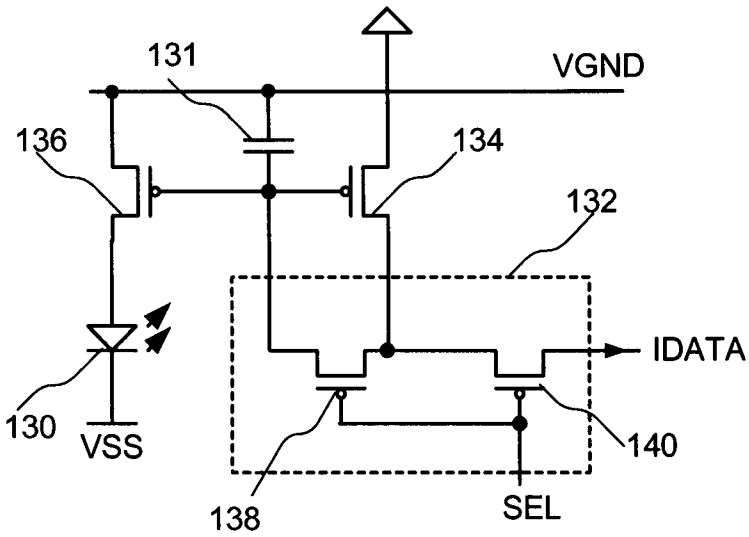

FIG.20

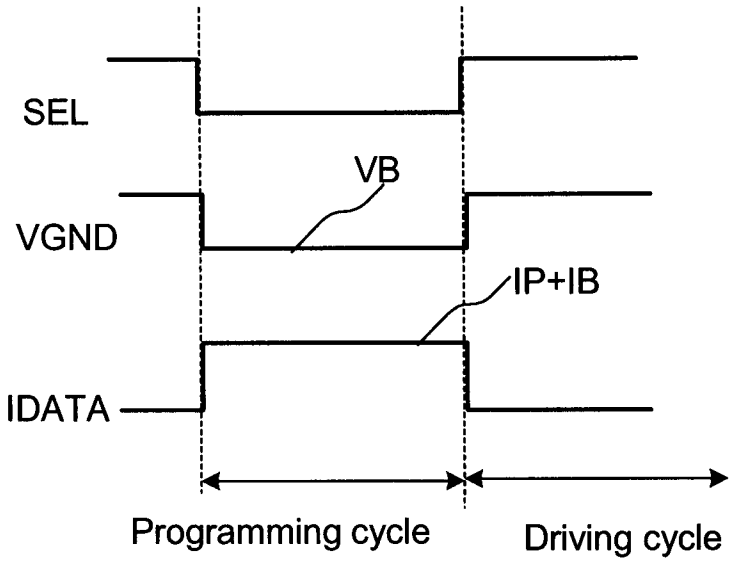

FIG.21

300

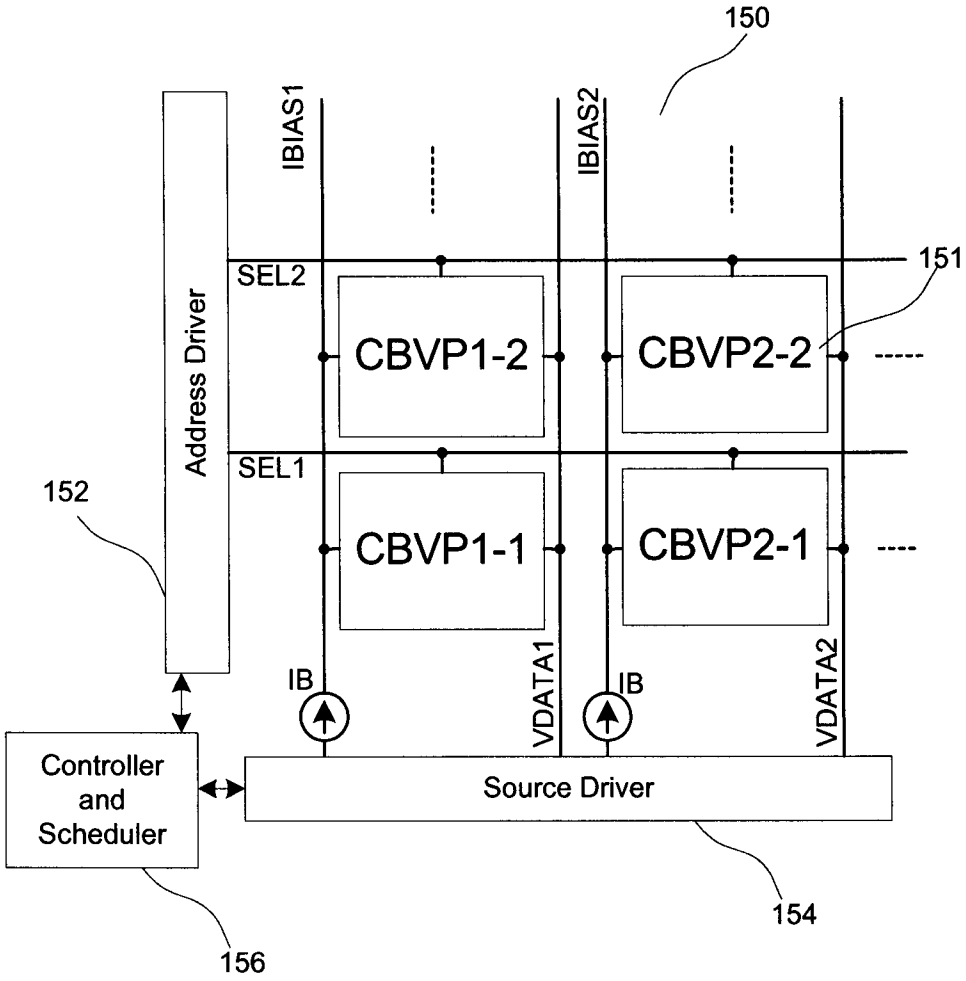
150
IBIAS1
IBIAS2
Address Driver
SEL2
SEL1
CBVP1-2
CBVP2-2
CBVP1-1
CBVP2-1
151
152
IB
IB
VDATA1
VDATA2
Controller and Scheduler
Source Driver
154
156

FIG.22

302

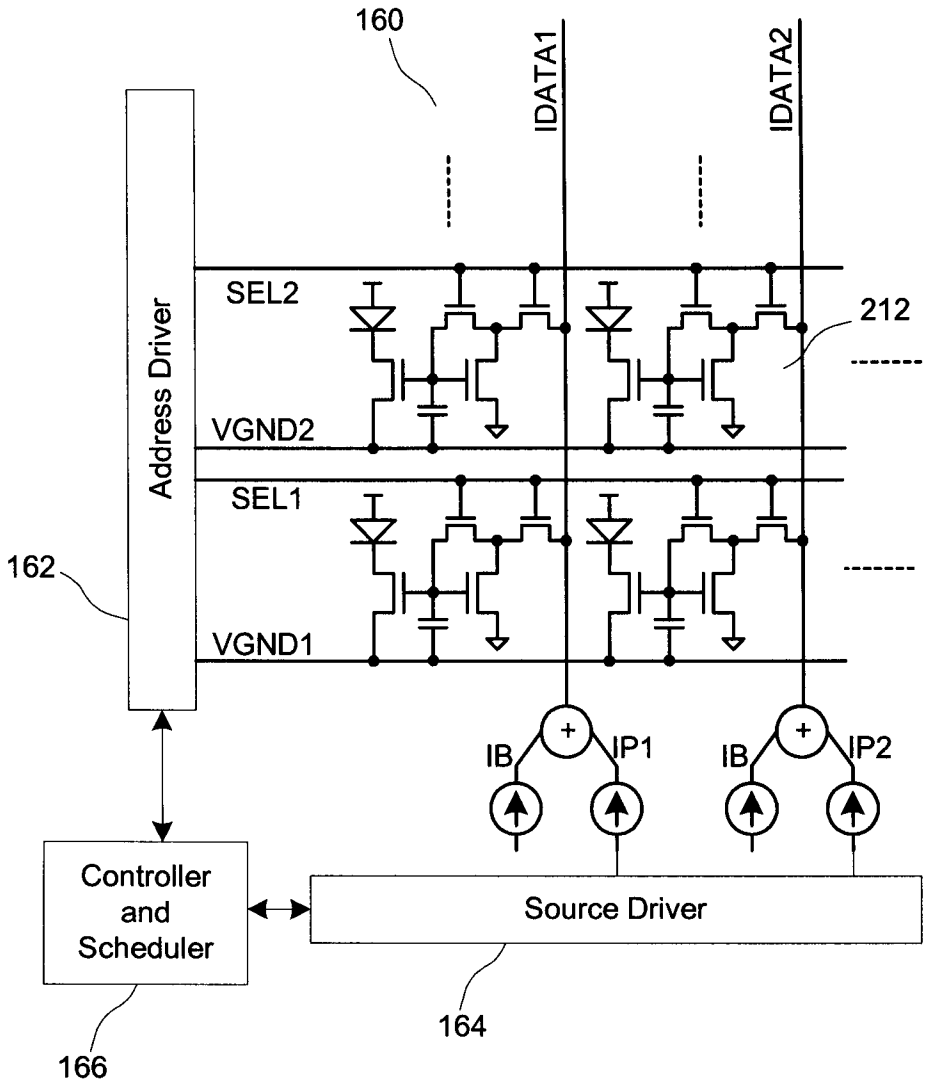
160
IDATA1
IDATA2
Address Driver
SEL2
212
VGND2
SEL1
162
VGND1
IB
IP1
IB
IP2
Controller and Scheduler
Source Driver
166
164

FIG.23

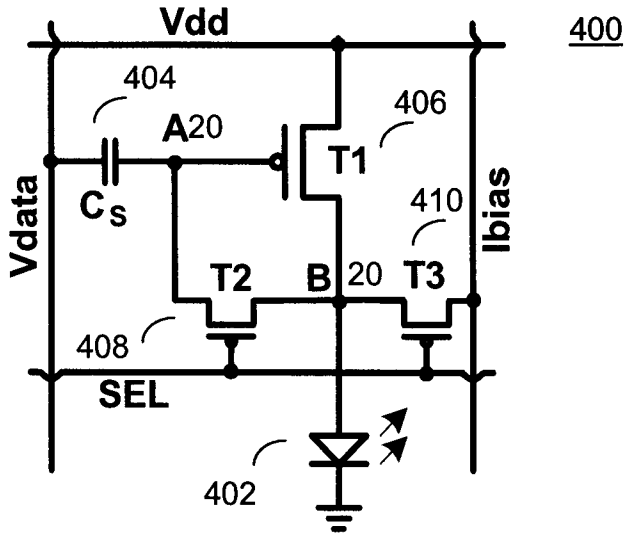
Vdd
400
404
406
A20
T1
Vdata
Cs
410
Ibias
T2
B
20
T3
408
SEL
402

FIG.24

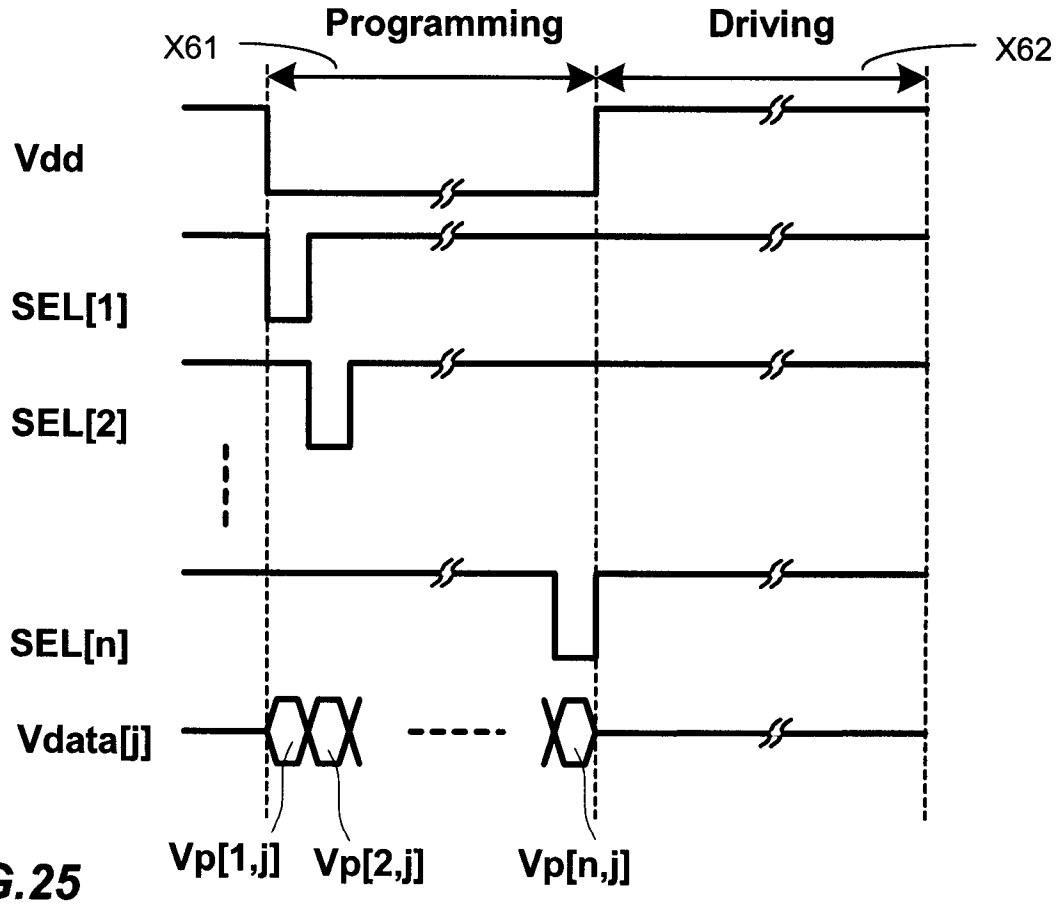
Programming
Driving
X61
X62
Vdd
SEL[1]
SEL[2]
SEL[n]
Vdata[j]
Vp[1,j]
Vp[2,j]
Vp[n,j]

FIG.25

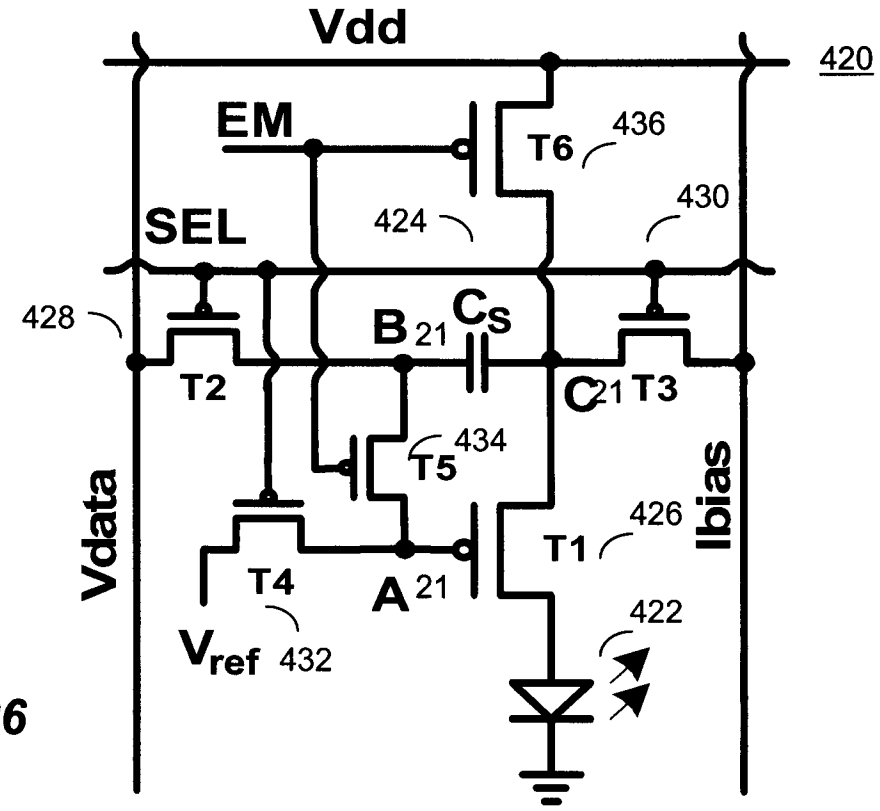
Vdd
420
EM
T6
436
SEL
424
430
428
B 21
Cs
T2
C 21
T3
T5
434
Vdata
Ibias
T1
426
T4
A 21
422
Vref
432

FIG.26

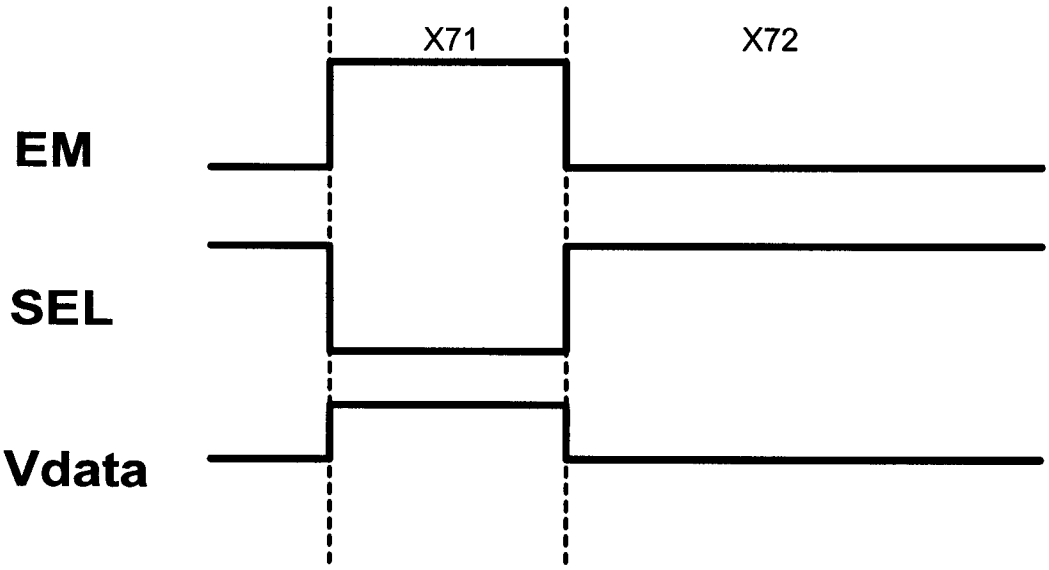
X71
X72
EM
SEL
Vdata

FIG.27

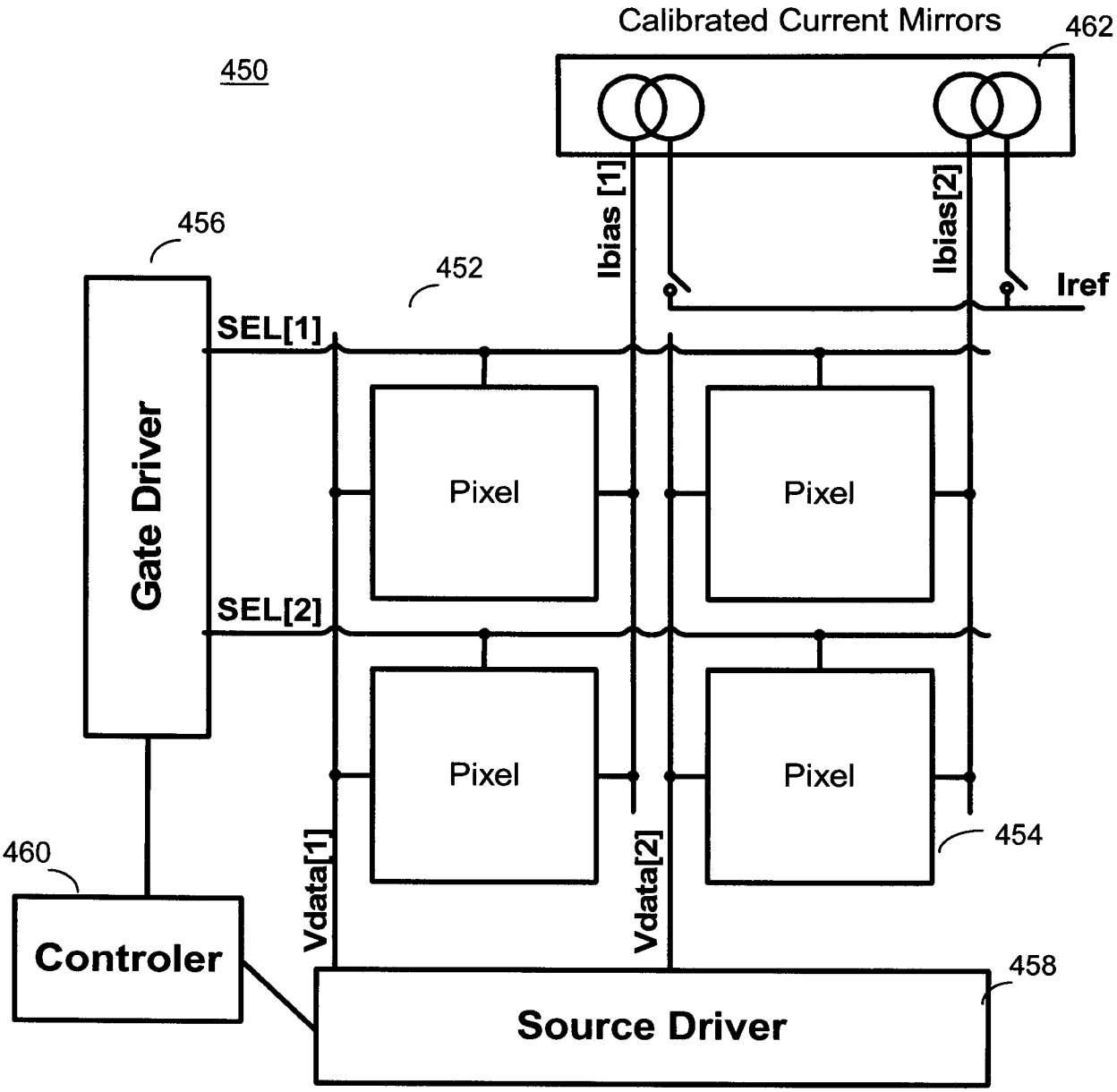

FIG.28 An example of array structure for implementation of CBVP driving scheme.

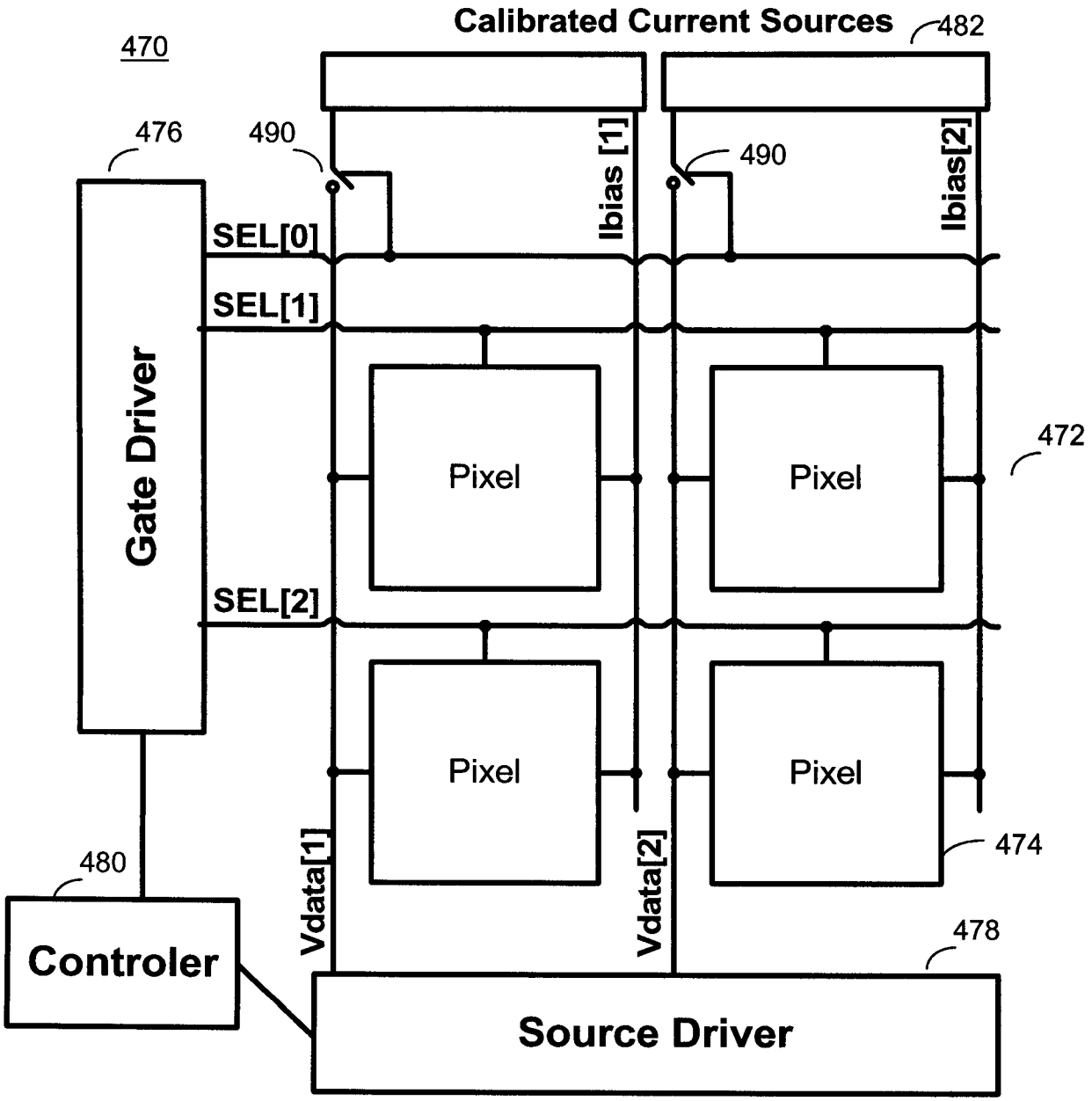

FIG.29 A further example of array structure for implementation of CBVP driving scheme.

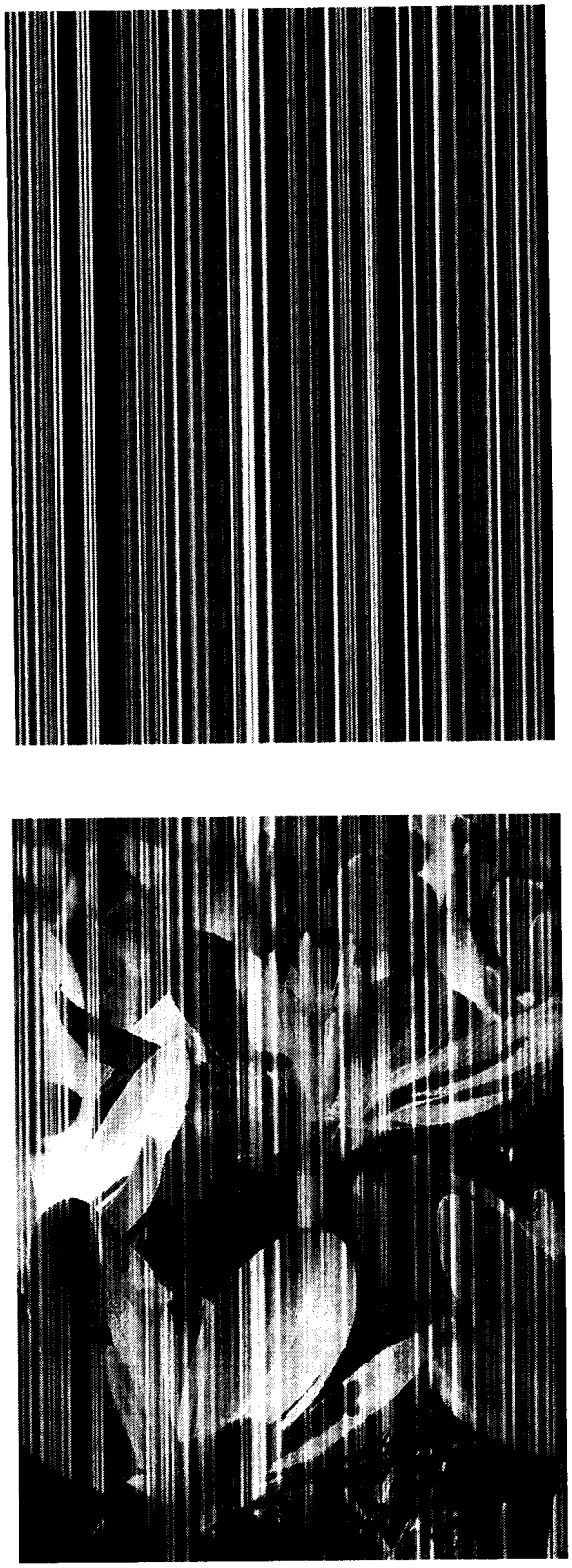

FIG.30

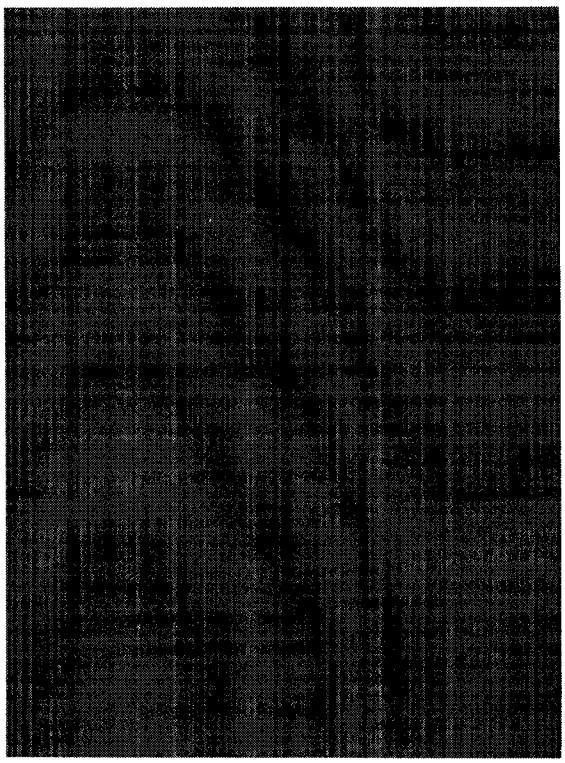

FIG.31

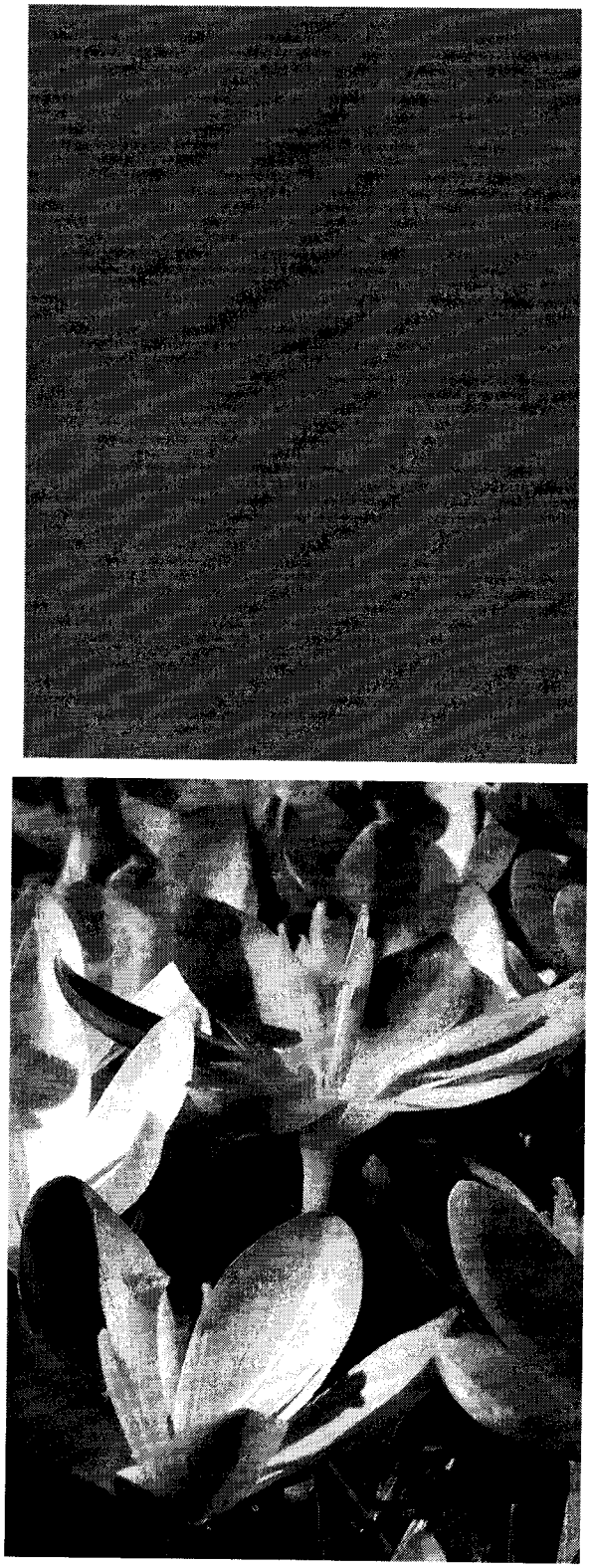

FIG.32

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2009/000502

A. CLASSIFICATION OF SUBJECT MATTER
IPC : ***G09G-3/22*** (2006.01); ***G09G-3/32*** (2006.01); ***H05B-33/08*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: G09G-3/22 (2006.01); G09G-3/32 (2006.01); H05B-33/08 (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of data base, and, where practicable, search terms used) :

Databases : Delphion, West, USPTO, Espacenet, Canadian Patent Database
Keywords : OLED pixel driver; aging compensation; programming voltage; bias current line; compensation mode; pixel degradation; gray scale; current mirror; display latch circuit; display activation/delay; pixel calibration; calibration

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CA 2523841 (CHAJI et al.) 29 July 2006 (29.07.2006), abstract; claims 1, 7, 8, 13, 17-19; figs. 5, 8, 22, 23; paras 0036, 0039, 0106, 0136	1-8, 17, 18, 23
Y		9, 12-16, 19-22, 24
Y	US 0070085801 (PARK et al.) 19 April 2007 (19.04.2007), abstract; claims 10, 13; figs 1, 3	9, 12-16, 20-22, 24
Y	US 6473065 (FAN) 29 October 2002 (29.10.2002), abstract	19, 22
A	CA 2557713 (CHAJI et al.) 26 November 2006 (26.11.2006), The whole document	1-28

[ ] **Further documents are listed in the continuation of Box C.** [X] See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel, or cannot be considered to involve an inventive step, when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 June 2009 (29-06-2009)	8 July 2009 (08-07-2009)
Name and mailing address of the ISA/CA Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No. 001-819-953-2476	Authorized officer Terry Cartile 819- 997-2951

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2009/000502

	Patent Document Cited in the Search Report	Publication Date (dd.mm.yyyy)	Patent Family Members	Publication Date(s) (dd.mm.yyyy)
X	CA 2523841	29.07.2006	WO 06/053424 A1	26.05.2006
			US 20060125408 A1	15.06.2006
			JP 2008521033 T2	19.06.2008
			EP 1825455 A1	29.08.2007
			CN 11111880 A	23.01.2008
Y	US 20070085801	19.04.2007	KR 7042363 A	23.04.2007
			JP 2007114732 A2	10.05.2007
			CN 1953007 A	25.04.2007
Y	US 6473065	29.10.2002	None	
A	CA 2557713	26.11.2006	WO 2007/030927 A1	22.03.2007
			US 20070063932 A1	22.03.2007
			KR 8090382 A	08.10.2008
			JP 2009508168 T2	26.02.2009
			EP 1825455 A1	18.06.2008
			CN 11305409 A	12.11.2008