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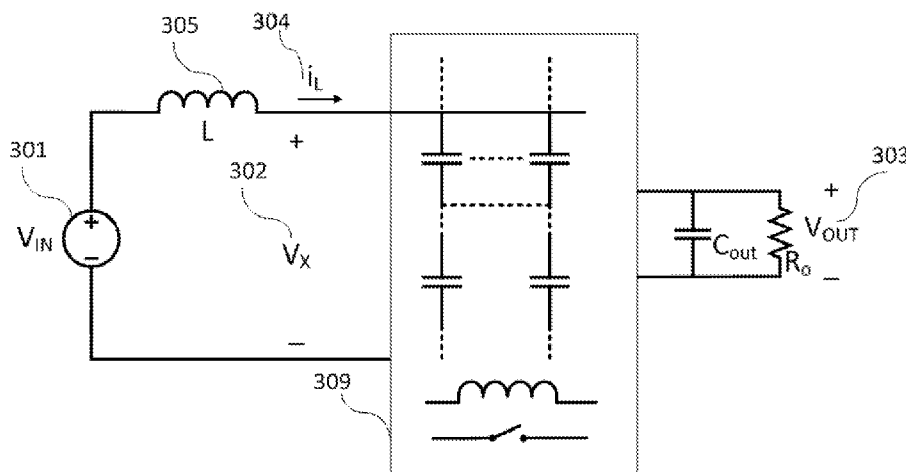


FIG. 3A

(57) Abstract: A hybrid converter achieves high efficiency with an inductor positioned at the lower current path that significantly decreases inductor loss by having the DC component of inductor current reduced. The circuit also features reduced inductance requirement by reducing the voltage swing blocked by the inductor. As a result, it turns to benefit of both efficiency improvement and better integration. Less voltage stress for switches is also an important advantage to switching loss reduction and switching frequency increase which in turns enables passive component size reduction. The circuit in this invention can be realized for both step-down and step-up power conversion as well as bidirectional power flow is available. For simplicity and cost, some of switches can be replaced with passive switches such as diodes which highly simplifies the converter circuit implementation.



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Hybrid Converter with Reduced Inductor Loss

CROSS-REFERENCE TO RELATED APPLICATIONS

[1] This application claims the benefit of United States provisional application no. 62/343,162 entitled “Smart Cable and Methods Thereof” and filed May 31, 2016 and United States provisional application no. 62/455,413 entitled “Hybrid Converter” and filed on February 6, 2017, each of which is hereby incorporated by reference as though fully set forth herein.

Technical Field

[2] This disclosure relates to a hybrid converter that merges advantages of switched inductor-based and capacitor-based converters with fewer semiconductor switches to achieve high efficiency and better integration.

Background

[3] Buck converter topology has been widely adapted in various DC-DC conversion applications due to its simplicity and higher efficiency than linear regulators that steps down input voltage to output voltage by burning out power on a controllable resistor. In fact, a Buck converter is extensively used in personal computer and server applications. From a bus voltage e.g. 12V, a Buck converter supplies power to loads, such as microprocessors. Also, a Buck converter is used in applications for mobile devices to charge Li-ion batteries, at ~3.0 V to 4.5V, from a 5V input.

[4] As shown in FIG. 1A, a Buck converter 100 has a switch 104, a current rectifying diode 105, an inductor 106 and output capacitor 107. In a more popular variation, a Buck converter can have a switch, in place of diode 105, that is operated synchronously with switch 104 and form a half bridge implementation for synchronous rectification in order to achieve better efficiency. However, in some applications that require better integration and efficiency, the conventional Buck converters are not suitable due to two drawbacks. The first drawback is the relatively large voltage swing across the inductor as the switch node voltage V_x 102 swings between zero to

input voltage V_{IN} 101 as shown in FIG. 1B. This large swing of V_X requires an inductor 106 having a larger inductance value to achieve low inductor current ripple. In the same form factor, an increase in inductance leads to increased equivalent series resistance (ESR) of the inductor and thus increased copper loss. As the inductor carries the average output current I_o 109 in the Buck converter, the inductor copper loss is significant because it is proportional to the square of the current expressed as

$$P_{cond} = R_L I_{L_rms}^2 \quad (1)$$

where R_L and I_{L_rms} are the equivalent series resistance of the inductor and the root mean square (RMS) value of the inductor current I_L 108. The second drawback of a Buck converter is that switch Q 104 and diode D 105 need to block the input voltage V_{IN} 101. This imposes the need for high breakdown voltage devices, which leads to either higher switch on-resistance or parasitic capacitance given the same form factor. This contributes to efficiency decrease of the switching regulator.

[5] These two drawbacks of the conventional Buck converter 100 are effectively addressed by a three level Buck converter 200, such as illustrated in FIG. 2A. By reducing the voltage swing at V_X 204 to half of the input voltage V_{IN} 201 and the interleaving effect that makes the effective switching frequency for inductor double, the reliance on inductance is significantly reduced. As a result, the three level Buck converter can enjoy improved efficiency and better integration as pointed out in an article titled “A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS,” published in IEEE Journal of Solid-State Circuits (JSSC) in January 2012, by Wonyoung Kim et al. In addition, by dividing the input voltage V_{IN} 201 into half of input voltage using two capacitors C_1 202 and C_2 203, the voltage sustained by switches Q_1 209 and Q_2 210 and diodes D_1 211 and D_2 212 is half of that of conventional Buck converter, which is beneficial to alleviating switching loss of semiconductor devices because the loss is expressed as

$$P_{switch} = \frac{1}{2} C_{DS} V_{DS}^2$$

where C_{DS} and V_{DS} are equivalent drain-source capacitance and the voltage applied to semiconductors during their off times. Therefore, a three level Buck converter can achieve better

efficiency and shows better potential for integration.

[6] The three level Buck converter 200 reduces inductor voltage swing and semiconductor voltage stress. However, it has several demerits. One of the major loss factor of Buck converter is the loss associated with inductor. Even though the three level Buck converter can help to alleviate the inductor loss by reducing the required inductance resulting in less copper loss with decreased ESR, it still undesirably has to carry the full output current and the related loss. Second, the minimum number of active switches required to operate the circuit is two, twice that of a conventional Buck converter, as the three level Buck converter needs one additional active switch to ensure the charge balance between C_1 202 and C_2 203. This is also discussed in the article titled “Fundamental considerations of three-level dc–dc converters: Topologies, analyses, and control,” published in the IEEE Transactions on Circuits and Systems I in December 2008, by Xinbo Ruan et al.

[7] To overcome the limitations of switched inductor-based converters, switched capacitor (SC) converters can be introduced. The SC converters show easier integration due to lack of magnetic components. The SC converters operate with high efficiency when the output voltage is predetermined fraction of input voltage i.e. $1/2$, $1/3$, and $2/3$. However, as the voltage conversion ratio changes, the efficiency of SC converters decreases. This fact is also discussed and clearly demonstrated in the article titled “Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters,” published in the IEEE Journal of Solid-State Circuits in September 2011, by Hanh-Phuc Le et al.

[8] To overcome the drawback of SC converters and Buck converters, hybrid converters that cascade the two kinds of converters have been proposed. Using the hybrid structure, the output voltage can be tightly regulated with reasonable efficiency. However, the increase of number of components, specifically the number of switches, makes the converter circuitry more complex. Also, sometimes the efficiency degradation due to the multiple stage power processing is not desirable.

[9] FIG 2C shows a circuit design described in US patent no. 9,143,032 B2 issued September 22, 2015 and entitled “Apparatus, systems, and methods for providing a hybrid power regulator”

to Hanh-Phuc Le et al., which is incorporated by reference herein. The circuit employs a flying switched inductor regulator 111 at a front end that enables significantly reducing the voltage swing v_x 119. With the flying switched inductor regulator, a position of the inductor 115 at the input side of the circuit leads to significantly reduced inductor loss and better integration. However, the additional switches 113 and 114 that are put in series in the main power flow from the inductor to the following step-down regulator increases not only the circuit complexity but also switch conduction loss.

[10] Besides, regarding the step-up power conversion, same discussion above is still valid as the boost converter has the same structure with Buck only except the opposite positions of source and load. As the inductor of boost converter is equally forced to carry high current, the input current in case of step up, the same demerit of boost type converters still exists.

SUMMARY

[11] A hybrid converter having its inductor at a low current side of the converter — at the input side in the case of a step-down converter and at the output side in the case of a step-up converter — that can achieve load regulation with improved efficiency is provided. The other side of the converter can be handled by a network with a reduced or minimum number of switches and capacitors.

Brief Description of the Drawings

[12] FIGS. 1A and 1B illustrate an example Buck converter and its operation waveforms, respectively.

[13] FIGS. 2A and 2B illustrate an example three-level Buck converter and its operation waveforms, respectively.

[14] FIG. 2C illustrates an example flying switched inductor regulator hybrid converter circuit.

[15] FIG. 3A shows a schematic drawing of an example of a hybrid converter circuit

arrangement of a step-down converter, according to one or more embodiments shown and described herein.

[16] FIG. 3B shows a schematic drawing of another example of a hybrid converter circuit arrangement of a step-up converter, according to one or more embodiments shown and described herein.

[17] FIG. 3C shows a schematic drawing of yet another example hybrid converter circuit arrangement of a bidirectional converter circuit, according to one or more embodiments shown and described herein.

[18] FIG. 3D shows a schematic drawing of another example hybrid converter circuit implementation with ladder structure, according to one or more embodiments shown and described herein.

[19] FIG. 4 illustrates example operation waveforms of a hybrid converter circuit, according to one or more embodiments shown and described herein.

[20] FIG. 5A and 5B illustrate example equivalent circuits of a hybrid converter circuit during on/off time, according to one or more embodiments shown and described herein.

[21] FIG. 6 illustrates a graph of an example voltage conversion ratio as a function of a duty cycle, according to one or more embodiments shown and described herein.

[22] FIG. 7 illustrates a graph of an example inductor ripple reduction of a hybrid converter circuit compared to a Buck converter, according to one or more embodiments shown and described herein.

[23] FIG. 8 illustrates a schematic drawing of an example hybrid converter circuit arranged as a step-up converter, according to one or more embodiments shown and described herein.

[24] FIG. 9 illustrates a schematic diagram of an example hybrid converter circuit arrangement for a bidirectional power flow, according to one or more embodiments shown and described herein.

[25] FIG. 10 illustrates schematic drawing of an example hybrid converter circuit implementation using three capacitors and five switches using ladder structure, according to one or more embodiments shown and described herein.

[26] FIG. 11 illustrates a schematic drawing of an example hybrid converter circuit implementation using a cable parasitic inductance, according to one or more embodiments shown and described herein.

[27] FIG. 12 illustrates a schematic drawing of an example hybrid converter circuit implementation for multiple loads, according to one or more embodiments shown and described herein.

[28] FIG. 13A illustrates a schematic drawing of an example hybrid converter circuit implementation with a series-parallel structure, according to one or more embodiments shown and described herein.

[29] FIG. 13B illustrates a schematic drawing of an example hybrid converter circuit implementation with a Fibonacci structure, according to one or more embodiments shown and described herein.

[30] FIG. 13C illustrates a schematic drawing of an example hybrid converter circuit implementation with a doubler structure, according to one or more embodiments shown and described herein.

[31] FIG. 14 illustrates a schematic diagram of another example embodiment of a hybrid converter circuit that uses two or more multiple switched capacitor network modules, according to one or more embodiments shown and described herein.

[32] FIG. 15A illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for AC-DC power conversion, according to one or more embodiments shown and described herein.

[33] FIG. 15B illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for AC-DC power conversion, according to one or more embodiments shown and described herein.

[34] FIG. 15C illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for AC-DC power conversion, according to one or more embodiments shown and described herein.

[35] FIG. 16 illustrates a schematic diagram of another example embodiment of a hybrid

converter circuit for DC-AC power conversion, according to one or more embodiments shown and described herein.

[36] FIG. 17A illustrates a schematic diagram of another example embodiment of a hybrid converter circuit implementation for AC-DC power conversion using three switched capacitor networks arranged in series with a full-bridge switch leg, according to one or more embodiments shown and described herein.

[37] FIG. 17B illustrates a graph showing an example switching node voltage of the example hybrid converter circuit shown in FIG. 17A, according to one or more embodiments shown and described herein.

[38] FIG. 18A illustrates a schematic diagram of another example embodiment of a hybrid converter circuit implementation for AC-DC power conversion, according to one or more embodiments shown and described herein.

[39] FIG. 18B illustrates a graph showing an example switching node voltage of the example hybrid converter circuit shown in FIG. 18A, according to one or more embodiments shown and described herein.

Detailed Description

[40] In the following description, numerous specific details are set forth regarding the systems and methods of the disclosed subject matter and the environment in which such systems and methods may operate, etc., in order to provide a thorough understanding of the disclosed subject matter. It will be apparent to one skilled in the art, however, that the disclosed subject matter may be practiced without such specific details, and that certain features, which are well known in the art, are not described in detail in order to avoid complication of the disclosed subject matter. In addition, it will be understood that the examples provided below are exemplary, and that it is contemplated that there are other systems and methods that are within the scope of the disclosed subject matter.

[41] In various embodiments, a hybrid converter having its inductor at a its low current side of the converter — at the input side in the case of a step-down converter and at the output side in

the case of a step-up converter — that can achieve load regulation with improved efficiency is provided. The other side of the converter can be handled by a network with a reduced or minimum number of switches and capacitors.

[42] FIG. 3A, for example, shows a conceptual circuit schematic representation of an example embodiment of a hybrid converter configured for step-down conversion. In this particular embodiment, for example, an inductor L 305 is connected to an input of the converter circuit right after an input voltage source 301. A switched multiple capacitor network 309 follows the inductor L 305. In this embodiment, the inductor L 305 is directly connected to one or a plural number of capacitors of the switched multiple capacitor network 309. The switched multiple capacitor network 309 can include one or more switches to achieve desired operation of the switched capacitor network 309 and some of the switch(es) can be realized by diodes for simplicity of control. In some cases, one or a plural number of inductors L 305 can be used to enhance the circuit operation. The switched multiple capacitor network is also connected to an output stage. In this embodiment, the output stage includes a filtering capacitor C_{out} disposed across an output voltage V_{OUT} 303.

[43] Although FIG. 3A shows an example embodiment of a step-down converter, a hybrid converter design similar to that shown in FIG. 3A can also be used for step-up power conversion and bidirectional power flow as shown in FIG. 3B and FIG. 3C, respectively. In the example step-up hybrid converter embodiment shown in FIG. 3B, for example, the inductor L 305 is connected to an output stage of the converter circuit after a switched multiple capacitor network 309, which is in turn coupled to an input voltage source 301. As described with reference to FIG. 3A, the inductor L 305 can be directly connected to one or a plural number of capacitors of the switched multiple capacitor network 309. The switched multiple capacitor network 309 can include one or more switches to achieve desired operation of the switched capacitor network 309 and some of the switch(es) can be realized by diodes for simplicity of control. In some cases, one or a plural number of inductors L 305 can be used to enhance the circuit operation. Again, in this embodiment, the output stage includes a filtering capacitor C_{out} disposed across an output voltage V_{OUT} 303.

[44] In FIG. 3C, yet another embodiment of a hybrid converter design includes bidirectional

power-flow operations. In this embodiment, the hybrid converter circuit is configured in a similar manner as the converter shown in FIG. 3A, except that V_{OUT} 303 and V_{IN} 301 may switch their function from a load to a power source and vice versa, dependent on external connections of the power source and load and on the operation of the network 309.

[45] In some realizations of the circuits shown in FIGS. 3A through 3C, the inductor 305 can also be positioned between negative side of a source and a switched multiple capacitor network 309. In this case, V_{IN} 301 is directly connected to one or a plural number of capacitors of the switched multiple capacitor network 309 that leads same benefit of switch number reduction. Also, in some realizations, the inductor 305 can be implemented by a plurality of inductors and one or more inductors can be put either on the positive terminal side or the negative terminal side of source.

[46] A switched multiple capacitor network 309, such as the ones shown in FIGS. 3A-3C, can be constructed in some embodiments by one or more switched capacitor circuits to switch the switching node voltage v_x 302. Common switched capacitor circuits such as ladder, series-parallel, doubler, Fibonacci, or Dickson or any other type of switched capacitor circuit can be used to construct a switched multiple capacitor network 309. As the structure and operation of the multiple switched capacitor circuit changes, the fundamental characteristic such as input-to-output voltage conversion ratio M may also change.

[47] The circuit 309 can also include one or more additional inductors to provide additional soft-charging operation for the multiple switched capacitor circuits to improve overall efficiency.

[48] Another example embodiment of a hybrid converter circuit includes a step-down converter, such as illustrated in FIG. 3D. In the example embodiment shown in FIG. 3D, for example, a ladder switched capacitor circuit may be used to construct a functional block of a multiple switched capacitor circuit 309. In this embodiment, for example, the circuit employs an inductor L 305 at its input side coupled between an input voltage source V_{IN} 301 and the multiple switched capacitor circuit 309. Two series connections of capacitors and switches are provided in the multiple switched capacitor circuit 309. The first series connection 306 includes multiple capacitors, C_{a-1} , C_{a-2} , C_{a-3} , $\dots$, C_{a-n} , and a switch Q_1 in series. A first end of the series connection 306 is connected to the inductor L 305 and a second end of the series connection (at the switch

Q₁) is connected to a negative terminal of the voltage source V_{IN} 301. A second series connection including a switch Q_2 and capacitors, C_{b-1} , C_{b-2} , C_{b-3} , ... C_{b-n-1} , 307 is also connected to the same inductor L 305 and the voltage source 301 as illustrated in FIG. 3D. Between the two series connections, 306 and 307, a switch network 308 is located to complete this particular embodiment of the multiple switched capacitor circuit construction. In this particular embodiment, the switches Q_3 to Q_{2n+1} in the switch network 308 are configured to provide a continuous half bridge structure referring to each capacitor as shown in FIG. 3D. Switches Q_2 and Q_3 make a half bridge structure referring to C_{a-1} with its midpoint connected to C_{b-1} and switches Q_3 and Q_4 again make another half bridge for C_{b-1} and this construction continues until it reaches C_{a-n} . The load is connected to C_{out} in FIG. 3D but it can be also connected in parallel with another capacitor or multiple series capacitors in 306 or 307. However, in this embodiment, the load is located referring to the same ground of Q_1 for ease of control and switch drive.

[49] In this particular embodiment, for example, only two switch control signals for all of the semiconductor switches are required for the converter control. The two control signals can be complementary with dead-time when both control signals turn off switches. The first control signal, for example, may be tied to the switches Q_1 , Q_2 , Q_4 , Q_6 , ... and Q_{2n} while the second control signal may be tied to the remainder of the switches, Q_3 , Q_5 , Q_7 , Q_9 , ... and Q_{2n+1} . A duty cycle D, for example, can be used to define the turn-on time of the first control signal as illustrated in FIG. 4, or the second control signal in case of a step-up configuration illustrated in FIG. 8, which will be described in more detail below. The duty cycle D can be used to determine the converter input to output voltage ratio, thus can be used as a control signal to tightly regulate the load.

[50] Compared to the design shown in FIG. 2C published in US patent no. 9,143,032 B2 on Sep. 22, 2015 to Hanh-Phuc Le et al., the circuit a hybrid converter such as shown in FIGS. 3A to 3C requires no dedicated switches 113 and 114 for the flying switched inductor regulator 111 in the circuit shown in FIG. 2C. In the example embodiments shown in FIGS. 3A to 3C, however, an inductor L 305 can be directly connected to a top flying capacitor of a switched capacitor network, allowing the inductor L 305 operation to be synchronized and controlled by the following switched capacitor network 309. As the operations of the two stages (flying

inductor and switched capacitor network) are merged, the number of switches can be reduced or even minimized, leading to lower switching and conduction losses. Control design, including switch drivers and regulation, can also be simpler and more energy efficient.

[51] In some embodiments, for example, following the switch control signals, the switching node voltage V_x 302 can be modulated, thus modulating the inductor current as shown in FIG. 4. In a steady-state operation, all the voltages of the capacitors can ideally be equalized. Two equivalent circuits are illustrated in FIGS. 5A and 5B according to the control signal states. As illustrated in FIG. 4, the inductor charges by $(V_{IN} - NV_{OUT})$ during DTs and discharges by $(V_{IN} - (N+1)V_{OUT})$ during $(1-D)Ts$. An input to output voltage ratio can be derived using the inductor voltage second balance with an assumption that the converter operates in steady state and a small ripple approximation. A general voltage ratio for this circuit can be expressed as

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{1}{(N+1)-D}$$

where M is the input to output voltage conversion ratio ranging from $1/(N+1)$ to $1/N$ and N is the number of capacitors stacked in series connections 306. As illustrated in FIG. 6, a voltage conversion ratio range of this circuit differs according to factor N.

[52] In this example, the converter's efficiency improvement is significant as the inductor L 305 is positioned at the input side of the converter. A conventional step-down converter such as a Buck converter having its inductor 106 at an output side of the converter as shown in FIG. 1A forces the inductor 305 to carry the whole amount of output current, which is higher than the input current because

$$I_O = \frac{1}{M} I_{IN}$$

in a lossless assumption, i.e. 100% efficiency, where I_{IN} is the input current of a converter. On the other hand, the hybrid step-down converter circuit, such as those shown in FIGS. 3A and 3C enables the inductor to carry a fraction of the output current that is the input current I_{IN} . In a step-up conversion configuration shown in FIG. 3B, the hybrid architecture allows the inductor to carry the output current which in this case is a fraction of the in current from V_{IN} 301. As the inductor resistive/copper loss is proportional to the square of the RMS value of the inductor current, the inductor-related loss factor is significantly reduced in these hybrid converter circuits.

In addition, as shown in FIG. 4, the voltage swing at V_X 302 is limited to V_{OUT} that is smaller than that of Buck converter, V_{IN} , and dramatically further decreases as the input to output voltage ratio M decreases. This feature is beneficial to reducing losses of both inductors and semiconductors.

[53] The reliance on high inductance in inductor-based converters can be a detrimental factor as the loss related to inductor, which is dominant in converter total loss, highly depends on inductor current ripple and DC current it carries. If the reliance is reduced, the inductor loss factor decreases because less inductance results in smaller ESR that contributes to efficiency improvement. Therefore, the reliance on the inductance of a converter can be used as an indicator to recognize its effectiveness to address loss of inductors. In contrast, hybrid converters, such as those provided, features less reliance on the inductance as it shows superior inductor DC current and ripple. As mentioned earlier, the DC current is reduced by a factor M as the inductor is positioned at the input side. In addition, the inductor ripple is also highly reduced compared to a standard Buck converter in the same operating condition. The inductor ripple of an example hybrid converter circuit can be derived as

$$\Delta i_{L,Hybrid} = \frac{V_{IN}T_s}{L} \frac{(1-D)D}{(N+1-D)}$$

while the inductor current ripple of Buck converter can be expressed as

$$\Delta i_{L,Buck} = \frac{V_{IN}T_s}{L} (1-D)D .$$

According to the two above equations, the benefit of the hybrid converter circuits provided herein can be confirmed. FIG. 7, for example, illustrates a comparison of inductor current ripples as a function of voltage ratio M in which the figures are normalized by the common factor $\frac{V_{IN}T_s}{L}$ and multiplied by 4 to make the point of maximum ripple of a Buck converter as a reference. It is noted that the current ripple is highly reduced in the example hybrid converter circuits resulting from the reduced voltage swing at V_X .

[54] Regarding the switching loss, the example hybrid converter circuits also have advantages as the voltage stress is reduced to V_{OUT} . And this reduction can help to employ semiconductor switches with better on-resistance and dynamic performance.

[55] As mentioned earlier, the example hybrid converter circuits can also be configured for a step-up conversion by exchanging the locations of voltage source and load as illustrated in FIG. 8. The benefits of the circuit still exists: less inductor DC current, inductor current ripple, and switch voltage stress than conventional boost converter.

[56] The example hybrid converter circuits, such as those shown in FIGS. 3A to 3C, can be also used for bidirectional power flow as shown in FIG. 9.

[57] As a simple example realization of a hybrid converter circuit, a step-down converter 1000 can be constructed with two capacitors and three switches as illustrated in FIG. 10.

[58] For better integration, the dedicated inductor can be replaced with an input or output cable or circuit parasitic inductance as shown in FIG. 11.

[59] As shown in FIG. 12, multiple loads can be attached to some hybrid converter circuit embodiments. Because the same voltage can be achieved from any capacitors in the circuit, any load which requires either the same output voltage level or multiple factors of it can be attached.

[60] Example embodiments of hybrid converter circuits can also control the output 303 by using pulse width modulation (PWM) and/or pulse frequency modulation (PFM) control method. Additional techniques to improve circuit efficiency can also be utilized, such as burst mode control.

[61] The operation principle discussed above was provided with continuous conduction mode (CCM) operation assumed, but discontinuous conduction mode (DCM) or boundary conduction mode (BCM) control can be also used.

[62] Again, the switched capacitor circuit structure 309 is not limited to a specific type of switched capacitor circuit but any type of switched capacitor circuits can be used. FIG. 13A, for example, shows another possible embodiment of a hybrid converter circuit that uses a series-parallel switched capacitor circuit structure 309. Depending on the system requirement, the number of basic cells 1301 can be integer number from 0 to N. As discussed earlier, the inductor L 305 is directly connected to one or a plural number of capacitors in switched capacitor circuit 309. The direct connection to capacitor enables to the circuit to reduce the number of switches and thus reduces conduction loss. While the converter input-to-output voltage

conversion ratio of FIG. 13A is now

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{1}{(N+1)-ND},$$

a benefit that is reduced voltage swing at vx 302 is still valid and effective to reduce the inductor requirement.

[63] FIG. 13B illustrates another possible embodiment of a hybrid converter circuit that uses a Fibonacci switched capacitor structure. Except the change of the conversion ratio, the benefits of direct connection of an inductor to a capacitor of a switched capacitor network and reduced inductance requirement remains.

[64] FIG. 13C illustrates another possible embodiment of a hybrid converter circuit that uses a doubler structure.

[65] FIG. 14 illustrates a schematic diagram of another example embodiment of a hybrid converter circuit that uses two or more multiple switched capacitor network blocks to provide more functionality. Using this series connected structure enables the circuit to effectively operate with V_{IN} 301 and/or V_{OUT} 303 changing.

[66] FIG. 15A illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for AC-DC power conversion. In this particular embodiment, for example, a full-bridge switch leg 1510 can be added between AC source V_{AC} 1501 and inductor 305 to fold the AC input and they can be implemented by passive switches.

[67] FIG. 15B illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for AC-DC power conversion. In this embodiment, the full-bridge switch leg 1510 is now positioned between the inductor 305 and the multiple switched capacitor network 309 to achieve better functionality. Though the full bridge leg is added between inductor 305 and switched capacitor network 309, the benefit of this hybrid converter circuit embodiment still remains as the switches 1511, 1512, 1513 and 1514 are operated at grid frequency most of the time that is relatively very slow compared to the switching frequency of switched mode power converters.

[68] The hybrid converters shown in FIGS. 15A and 15B can be used for a variety of

applications e.g. AC-DC converters for data centers and other grid tied electric device power supply, AC-DC adapters for mobile devices, and microgrid system.

[69] FIG. 15C illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for AC-DC power conversion. In this embodiment, two or more multiple switched capacitor networks 309 are used. By constructing a series connection of switched capacitor networks 309, the possible number of switching node voltages can be increased.

[70] FIG. 16 illustrates a schematic diagram of another example embodiment of a hybrid converter circuit for DC-AC power conversion. In this embodiment, a DC source becomes an input 301 and an AC section becomes an output 1501. The DC source 301 can be any DC source such as solar array, storage devices like battery pack to be interfaced to AC utility. As discussed above, the location of full-bridge switch leg 1510 could be changed for more functionality.

[71] FIG. 17A illustrates a schematic diagram of another example embodiment of a hybrid converter circuit implementation for AC-DC power conversion using three switched capacitor networks 309 in series a full-bridge switch leg 1510. In this embodiment, each switch in the circuit can be synchronized and operated to switch the inductor and provide multiple level of voltages in a manner to reduce the ripple of current i_L 1704 of inductor 305. As shown in FIG. 17B, the switching node voltage 1702 can be switched between nine levels: -400, -300, -200, -100, 0, 100, 200, 300, and 400V while the voltage of switching node 1802 of conventional bridgeless power factor correction boost converter shown in FIG. 18A can be just three: -400, 0, and 400 shown in FIG. 18B. Reducing the voltage swing helps to reduce the size of inductor 305 as well as reduce the voltage stress on switches in switched capacitor network 309 that enable using lower voltage rated transistors for better performance e.g. lower on-state resistance with less parasitic and better dynamic performance.

[72] The example hybrid converter topologies provided can be applied to electronic platforms that utilize DC-to-DC power conversion. Non-limiting examples include televisions (TVs), video projectors, set-top boxes or set-top units, digital video recorders (DVR), computers, netbooks, laptops, and any other audio/visual equipment with computation capabilities. In these applications, the input voltage V_{IN} 301 can come from a battery, or output of a grid-connected AC-to-DC adapter, or another type of power source, while the output voltage V_{OUT} 303 can

supply power to functional circuits, for example, processors, display, and communication. These loading functional circuits can be configured with one or more processors that process instructions and run software that may be stored in memory. The processor also communicates with the memory and interfaces to communicate with other devices. The processor can be any applicable processor such as a system-on-a-chip that combines a CPU, an application processor, and flash memory. The loading circuits at V_{OUT} 303 can also provide a variety of user interfaces such as a keyboard, a touch screen, a trackball, a touch pad, and/or a mouse. The loading circuits at V_{OUT} 303 may also include speakers and a display device in some embodiments. The loading circuits at V_{OUT} 303 can also include a bio-medical electronic device.

[73] Although embodiments of this invention have been described above with a certain degree of particularity, those skilled in the art could make numerous alterations to the disclosed embodiments without departing from the spirit or scope of this invention. All directional references (e.g., upper, lower, upward, downward, left, right, leftward, rightward, top, bottom, above, below, vertical, horizontal, clockwise, and counterclockwise) are only used for identification purposes to aid the reader's understanding of the present invention, and do not create limitations, particularly as to the position, orientation, or use of the invention. Joinder references (e.g., attached, coupled, connected, and the like) are to be construed broadly and may include intermediate members between a connection of elements and relative movement between elements. As such, joinder references do not necessarily infer that two elements are directly connected and in fixed relation to each other. For example, two elements coupled between a pair of terminals are not necessarily coupled directly to the terminals, but there may be one or more other circuit element disposed between the terminal(s) and the elements coupled between those terminals. It is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative only and not limiting. Changes in detail or structure may be made without departing from the spirit of the invention as defined in the appended claims.

CLAIMS

1. A hybrid converter circuit comprising:

a pair of input terminals adapted to be coupled to a circuit input;

a pair of output terminals adapted to be coupled to a circuit output;

an inductor coupled between a first input terminal of the pair of input terminals and a first output terminal of the pair of output terminals; and

a switched multiple capacitor circuit coupled in series with the inductor between the first input terminal and the first output terminal,

wherein the inductor is coupled directly to at least one capacitor in the switched multiple capacitor circuit.
2. The hybrid converter circuit of claim 1 wherein the hybrid converter comprises a step down converter and the inductor is disposed between the input terminal and the switched multiple converter circuit.
3. The hybrid converter circuit of claim 1 wherein the hybrid converter comprises a step up converter and the inductor is disposed between the output terminal and the switched multiple converter circuit.
4. The hybrid converter circuit of claim 1 wherein the hybrid converter comprises a bidirectional converter circuit.
5. The hybrid converter circuit of claim 1 wherein the switched multiple capacitor circuit comprises (i) a first series connection of at least one first capacitor in series with a first switch and the first switch is coupled to a second input terminal of the pair of input terminals and (ii) a second series connection of a second switch and at least one second capacitor, an end of the at least one second capacitor is coupled to the first output terminal of the pair of output terminals.
6. The hybrid converter circuit of claim 5 wherein the first series connection comprises one first capacitor coupled in series with the first switch and the second series connection comprises

the second switch coupled in series with one second capacitor.

7. The hybrid converter circuit of claim 5 wherein the first series connection comprises a plurality of first capacitors coupled in series with the first switch and the second series connection comprises the second switch coupled in series with a plurality of second capacitors.

8. The hybrid converter circuit of claim 5 wherein the first switch comprises at least one of the group comprising: an active switch, an active transistor switch, a passive switch, and a passive diode switch and the second switch comprises at least one of the group comprising: an active switch, an active transistor switch, a passive switch, and a passive diode switch.

9. The hybrid converter circuit of claim 1 wherein a load is coupled in parallel with a capacitor of either the first series connection of the at least one first capacitor and the first switch or the second series connection of the second switch and the at least one second capacitor.

10. The hybrid converter of claim 1 wherein a load is coupled in parallel with two or more capacitors of either said first series connection of the at least one first capacitor and the first switch or the second series connection of the second switch and the at least one second capacitor.

11. The hybrid converter circuit of claim 1 wherein a first load is coupled to the pair of output terminals and a second load is coupled to a second pair of output terminals.

12. The hybrid converter circuit of claim 1 further comprising a second inductor coupled between a second input terminal of the pair of input terminals and the switched multiple capacitor circuit.

13. The hybrid converter circuit of claim 12 wherein the inductor and the second inductor are implemented at least in part via a parasitic inductance of an input cable coupled to the pair of input terminals.

14. The hybrid converter circuit of claim 12 wherein the inductor and the second inductor are implemented at least in part via a parasitic inductance of an input cable coupled to the pair of output terminals.

15. A step down converter driving a load comprising in combination:

a voltage source having a first and second terminal

a first series connection of first multiple capacitors in series and a first switch, said first switch connected to said first terminal of said voltage source;

a second series connection of a second switch and second multiple capacitors in series, end of said second capacitors connected to said first terminal of said voltage source;

an inductor having first and second terminal, said first terminal of said inductor connected to said second terminal of said voltage source; said second terminal connected to said first capacitors of said first series connection of said first capacitors and said first switch; said second terminal of said inductor also connected to said second switch of said second series connection of said second switch and said second capacitors;

third multiple switches having first and second terminal; said first terminal of said each third switch connected to one of the common nodes of said first series connection of said first capacitors and said first switch; said second terminal of said each third switch connected to one of the common nodes of said second series connection of said second switch and said second capacitors; said each third switch positioned between said common nodes connecting either the same order of common nodes of said first series connection of said first capacitors and said first switch and said second series connection of said second switch and said second capacitors or (N)th common node of said first series connection of said first capacitors and said first switch and (N+1)th common node of said second series connection of said second switch and said second capacitors;

a load connected to the last capacitor of said second series connection of said second switch and said second capacitors in parallel.

16. A method of controlling a hybrid converter circuit comprising:

providing a hybrid converter circuit comprising:

a pair of input terminals adapted to be coupled to a circuit input;

a pair of output terminals adapted to be coupled to a circuit output;

an inductor coupled between a first input terminal of the pair of input terminals and a first output terminal of the pair of output terminals; and

a switched multiple capacitor circuit coupled in series with the inductor between the first input terminal and the first output terminal, wherein the inductor is coupled directly to at least one capacitor in the switched multiple capacitor circuit;

controlling at least one switch of the switched multiple capacitor network to switch the inductor voltage and generate an output voltage at the pair of output terminals.

17. The method of claim 16 wherein the at least one switch is controlled to apply a first voltage level and a second voltage level across the inductor.

18. The method of claim 16 wherein the at least one switch is controlled by a duty cycle.

19. The method of claim 18 further comprising modulating the duty cycle to control the output voltage.

20. The method of claim 18 further comprising changing a switching frequency to control the output voltage.

21. The method of claim 18 further comprising modulating the duty cycle and changing a switching frequency to control the output voltage.

22. The method of claim 16 wherein the at least one switch comprises a first switch and a second switch.

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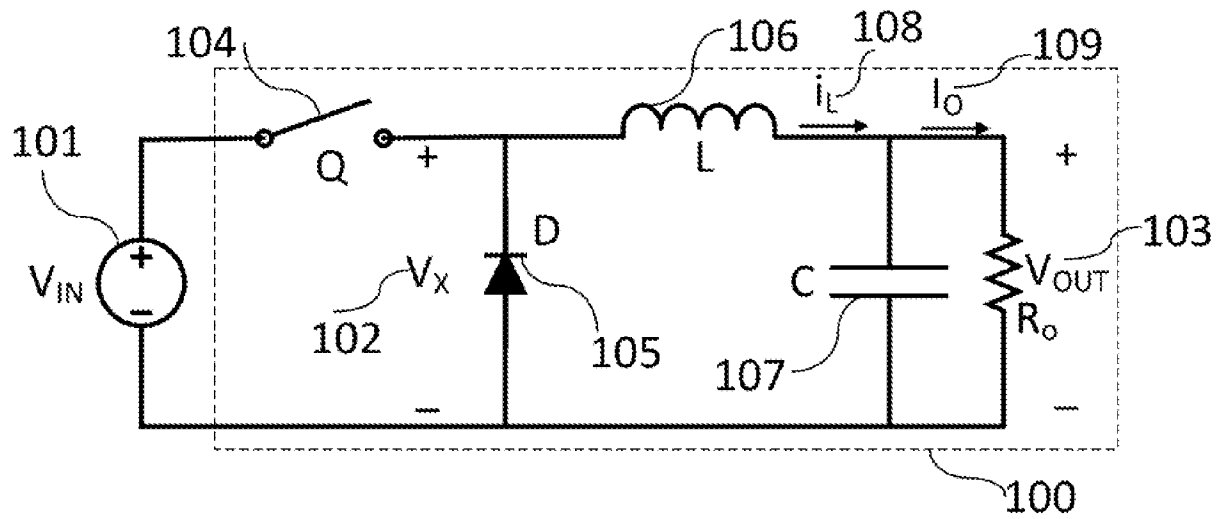


FIG. 1A

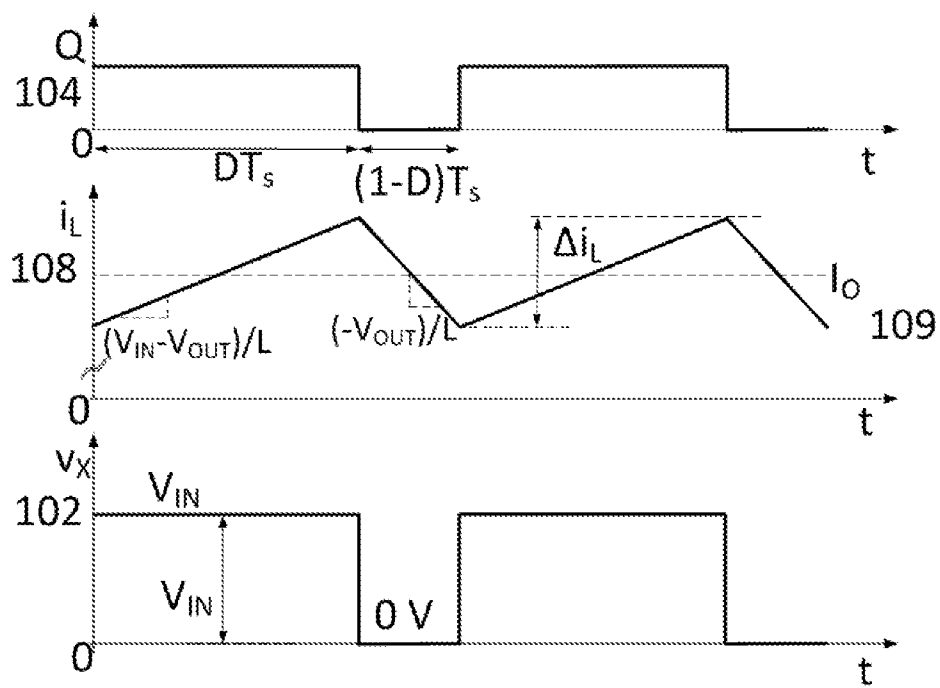


FIG. 1B

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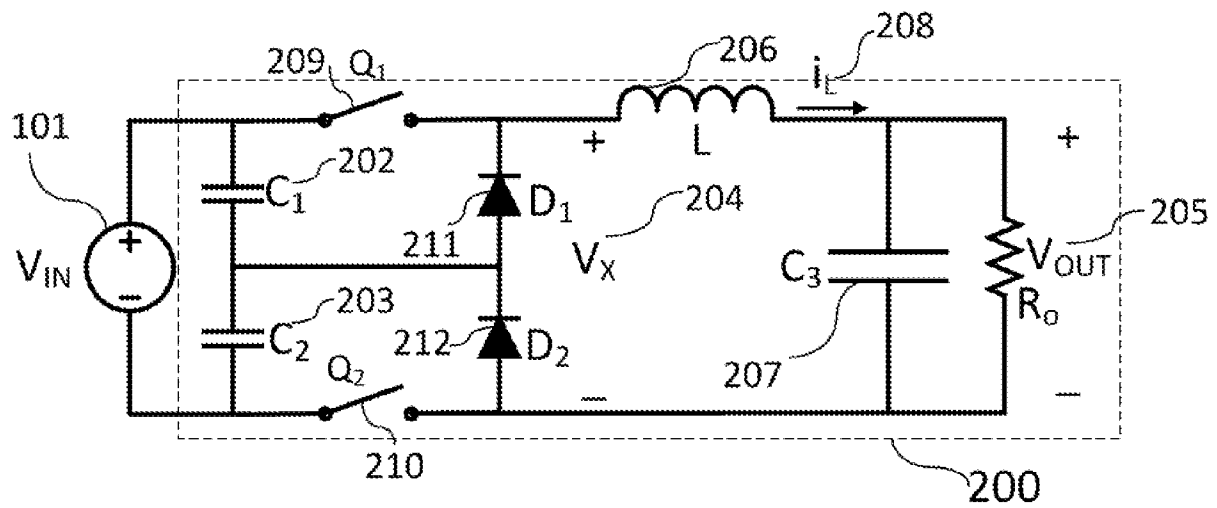


FIG. 2A

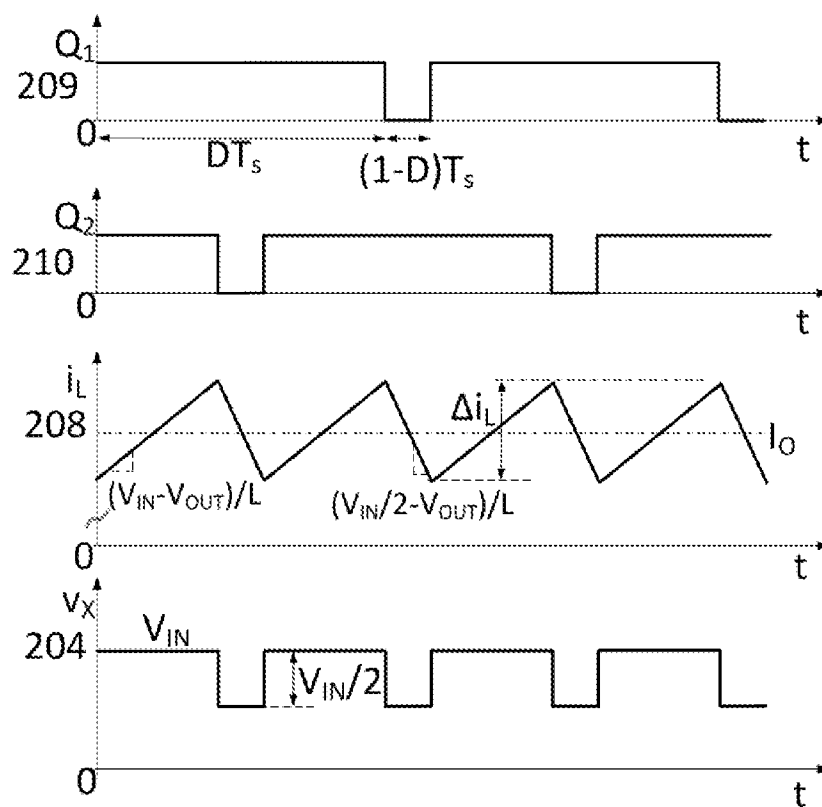


FIG. 2B

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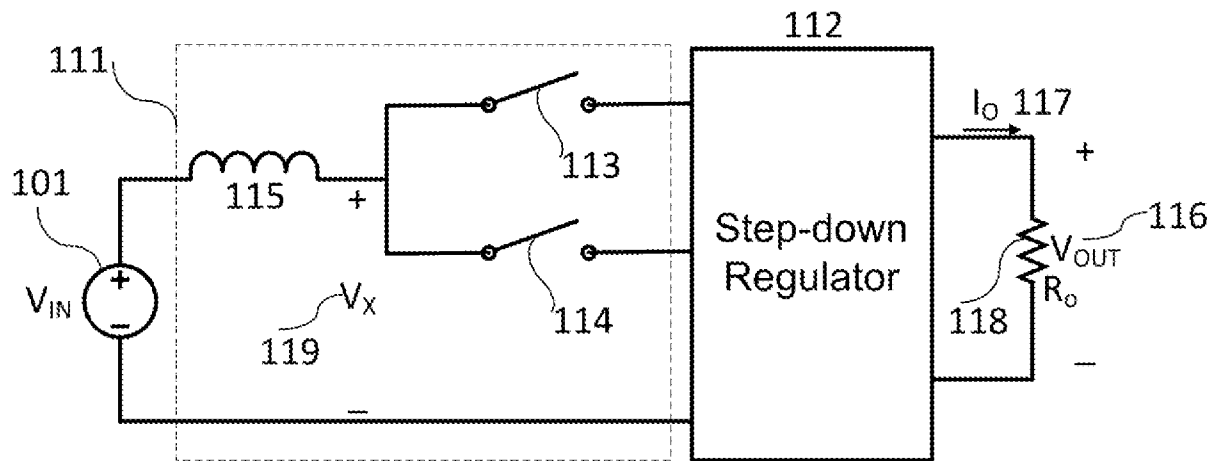


FIG. 2C

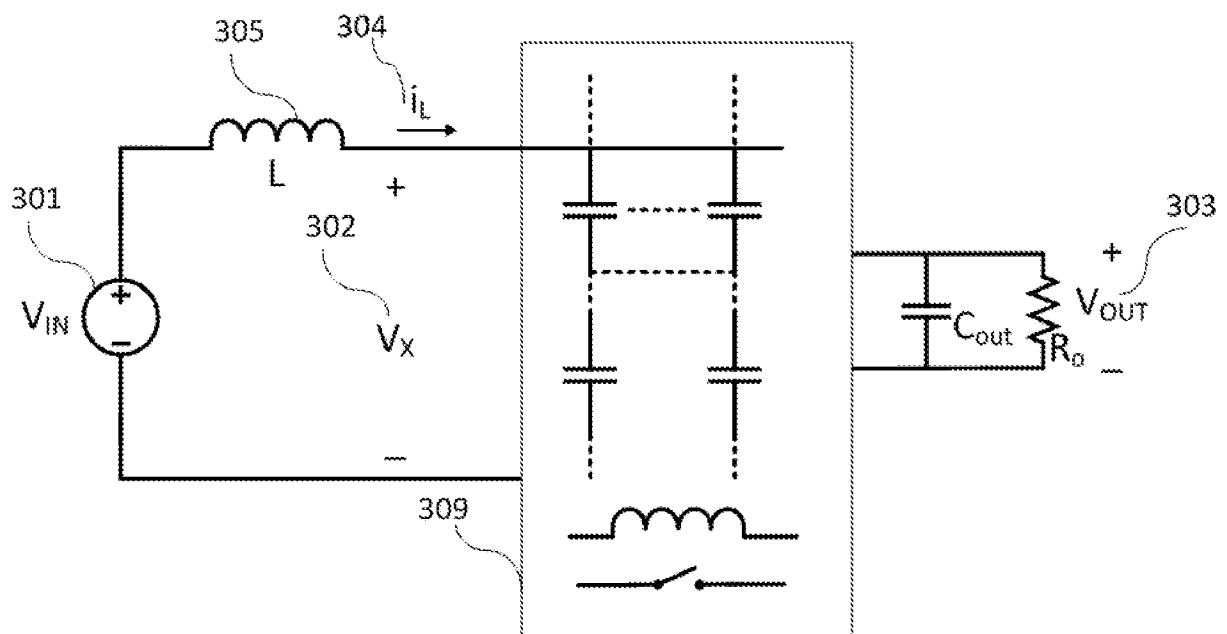


FIG. 3A

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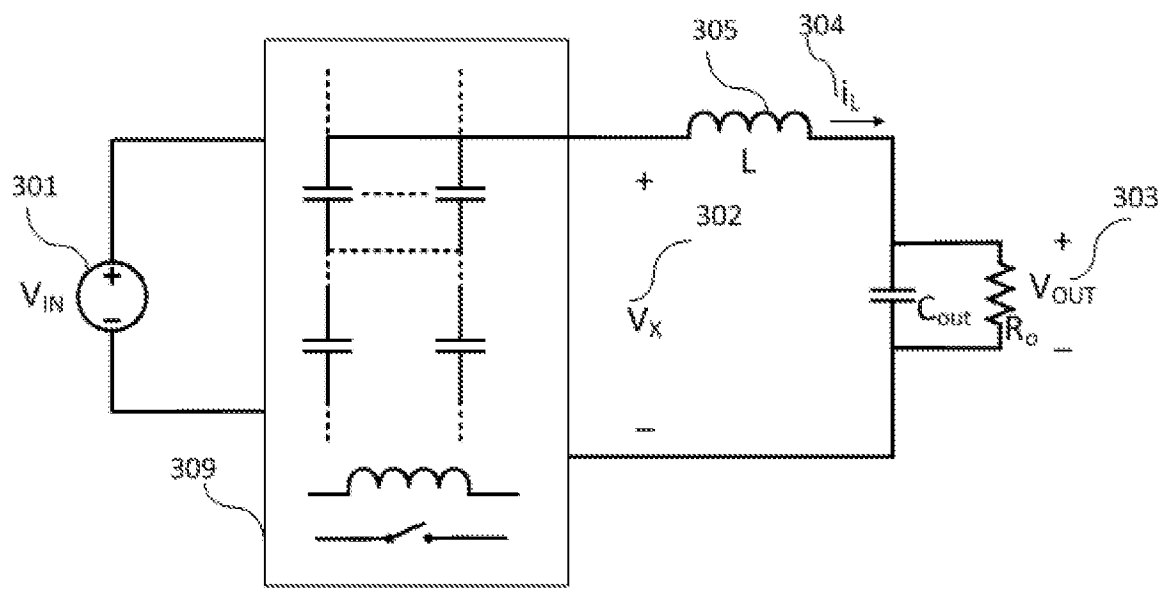


FIG 3B

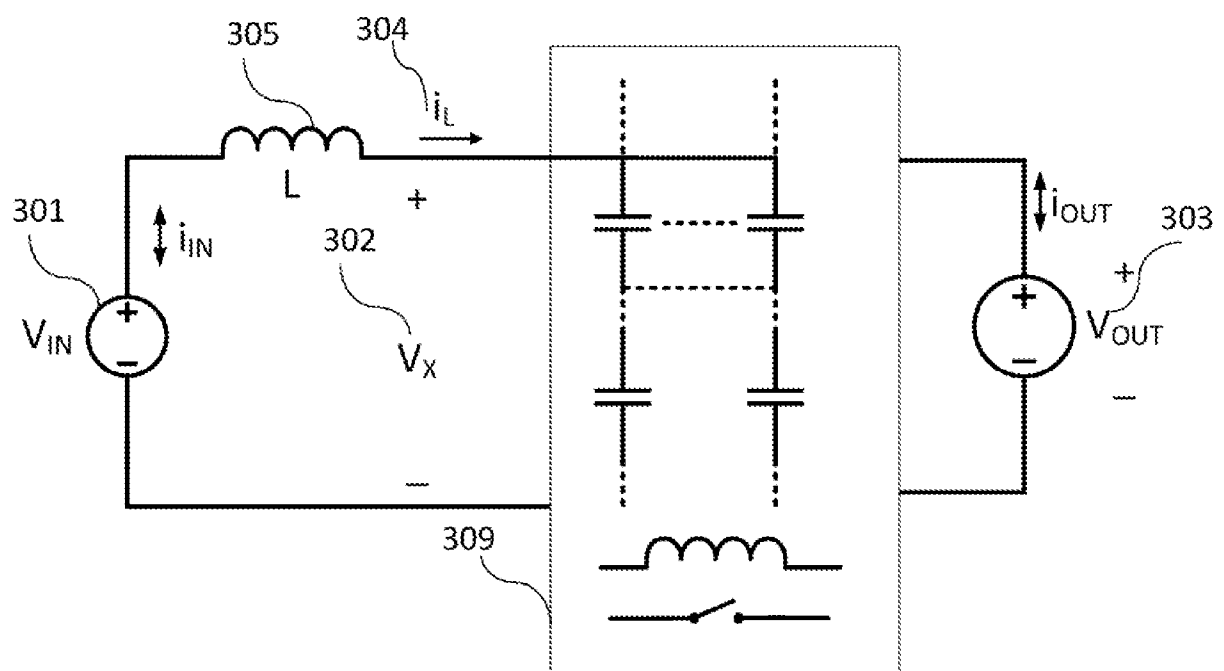


FIG 3C

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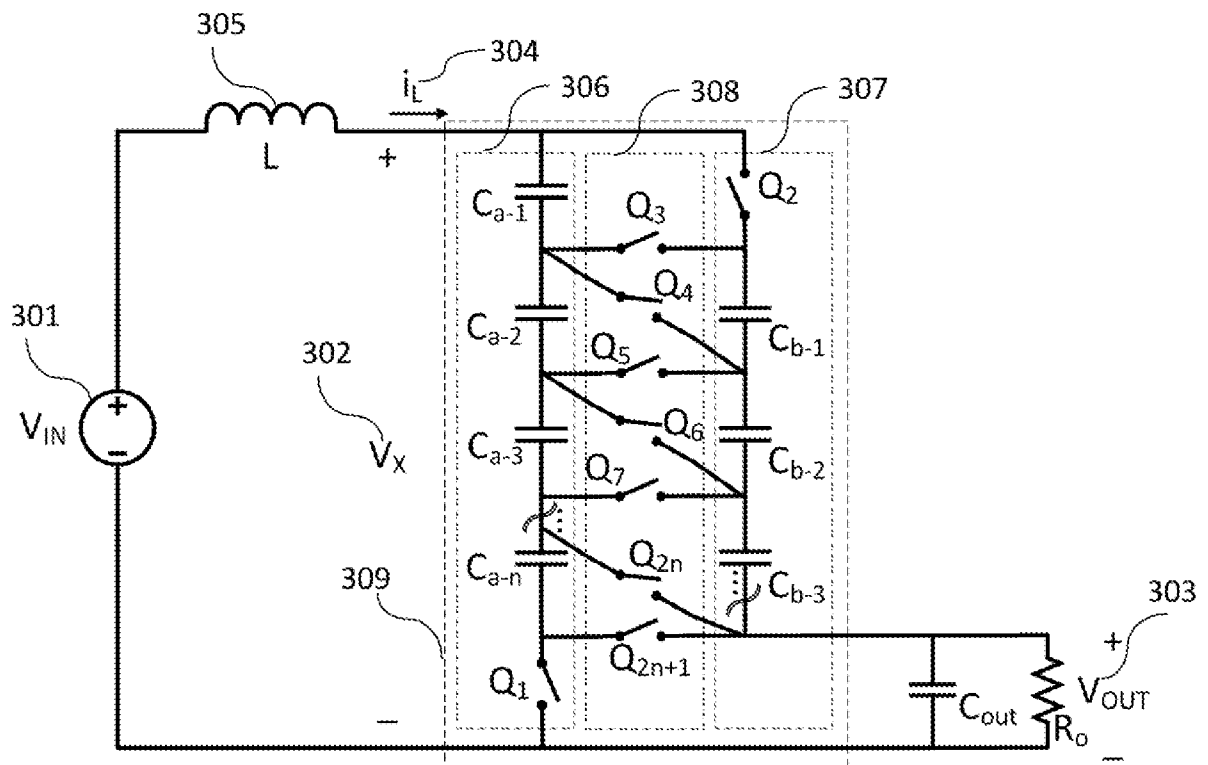


FIG. 3D

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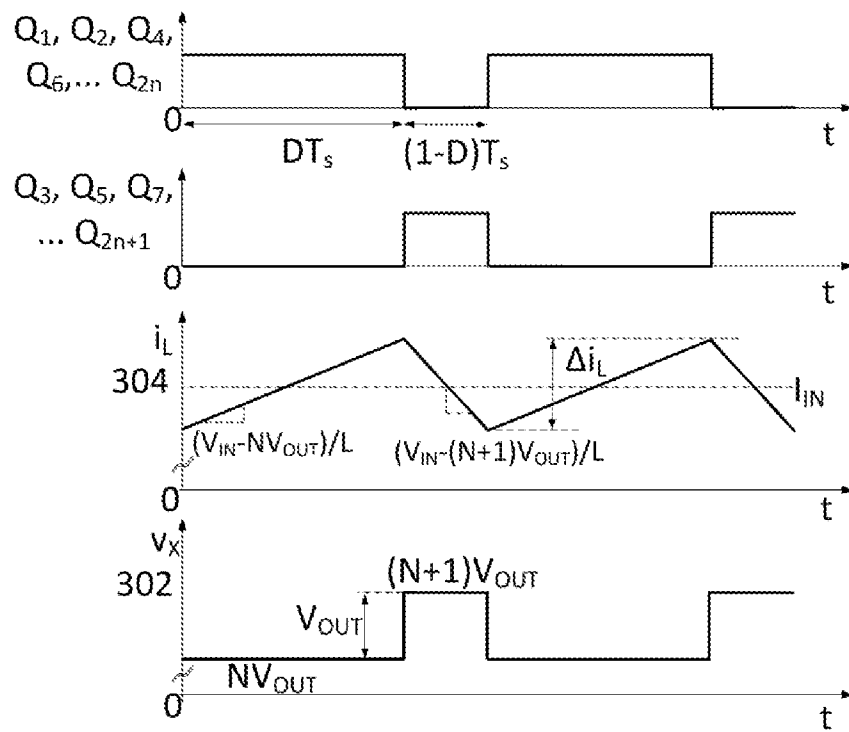


FIG. 4

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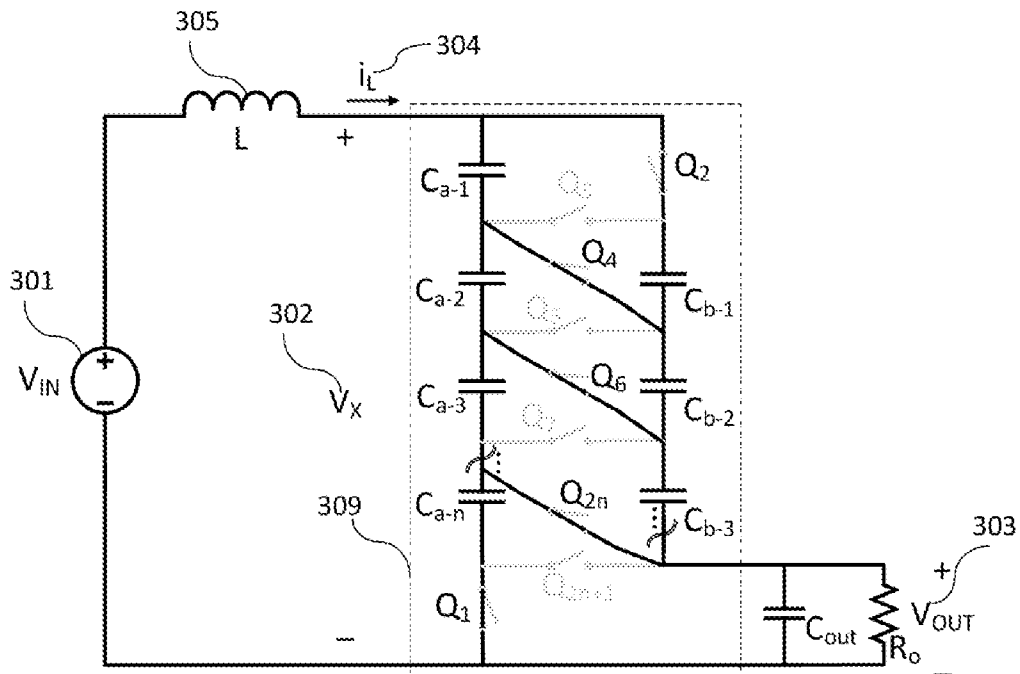


FIG. 5A

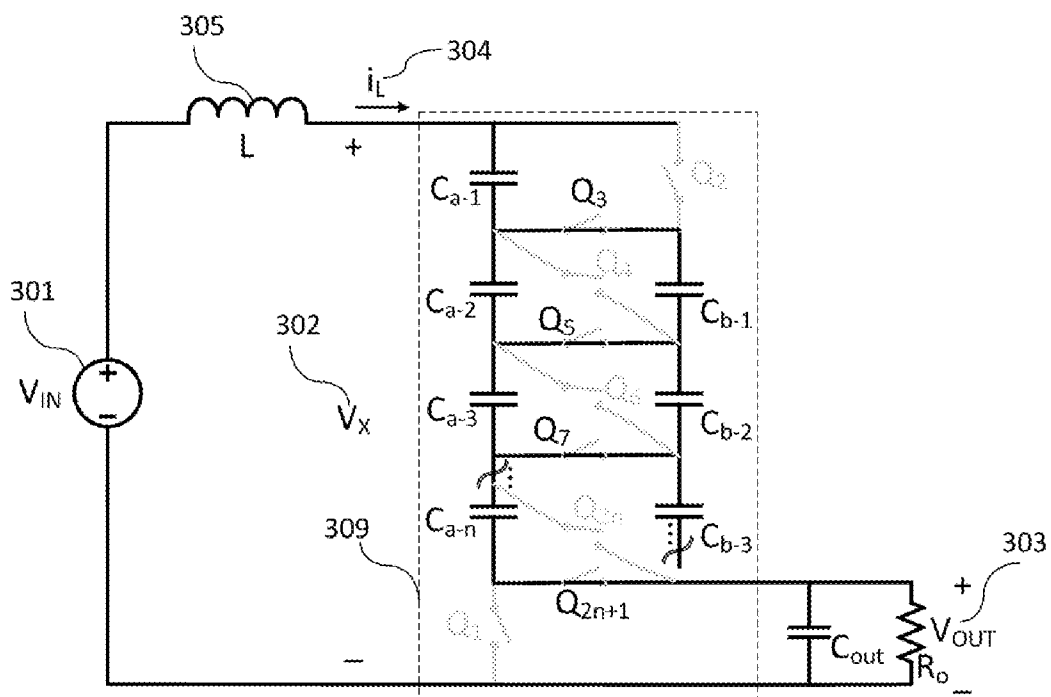


FIG. 5B

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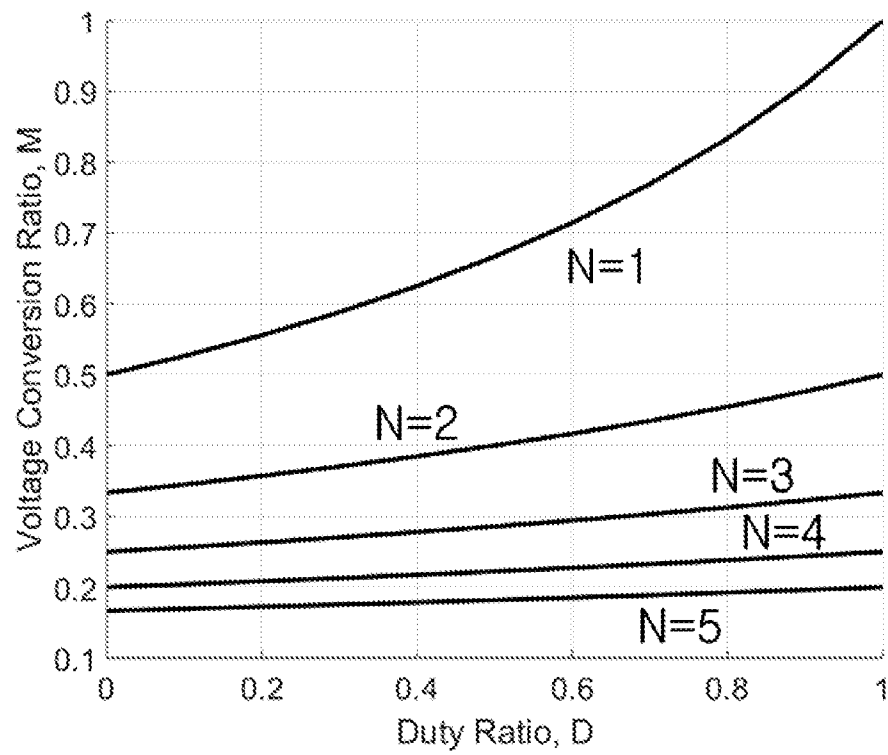


FIG. 6

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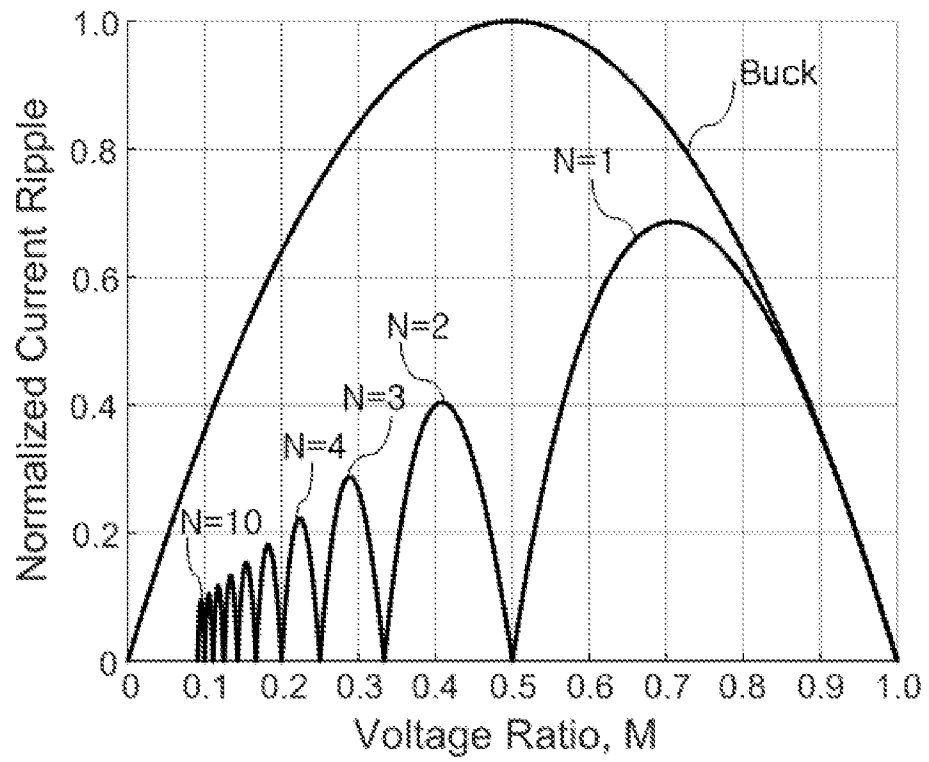


FIG. 7

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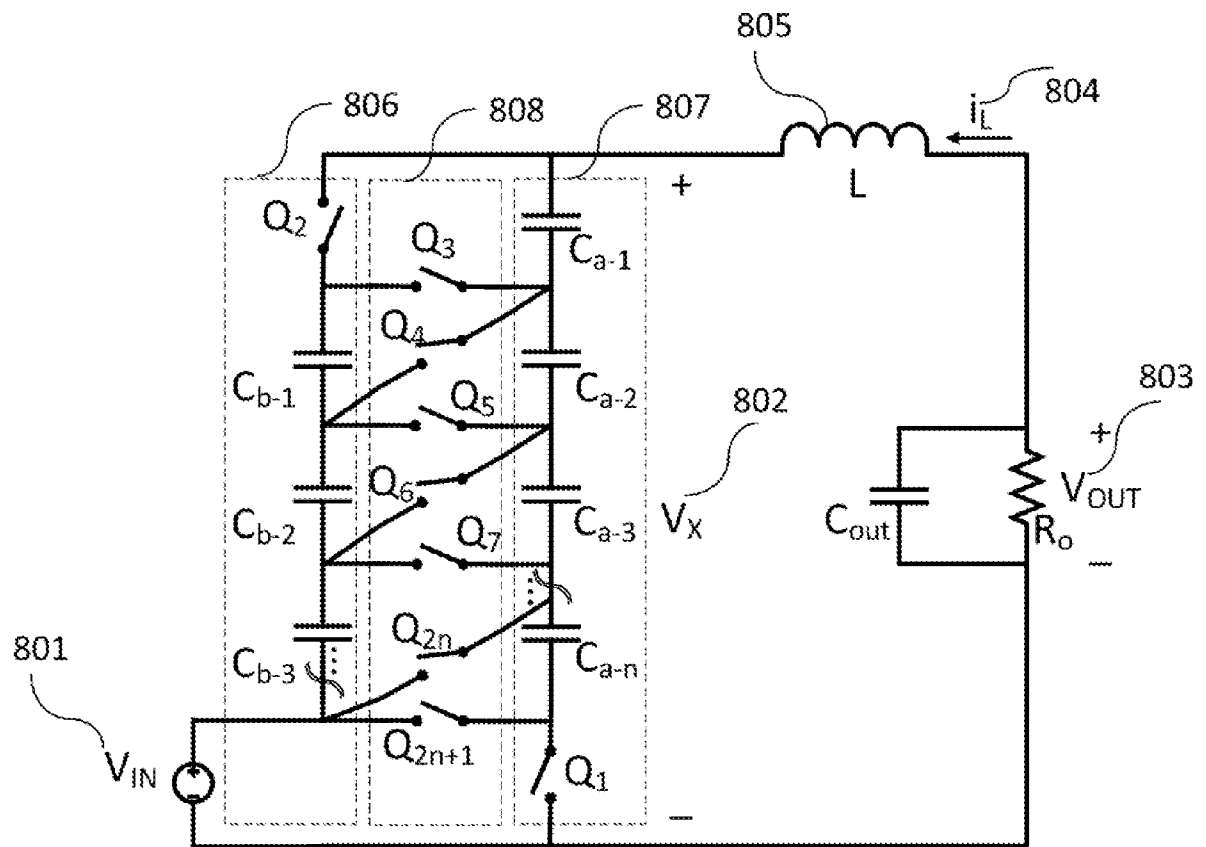


FIG. 8

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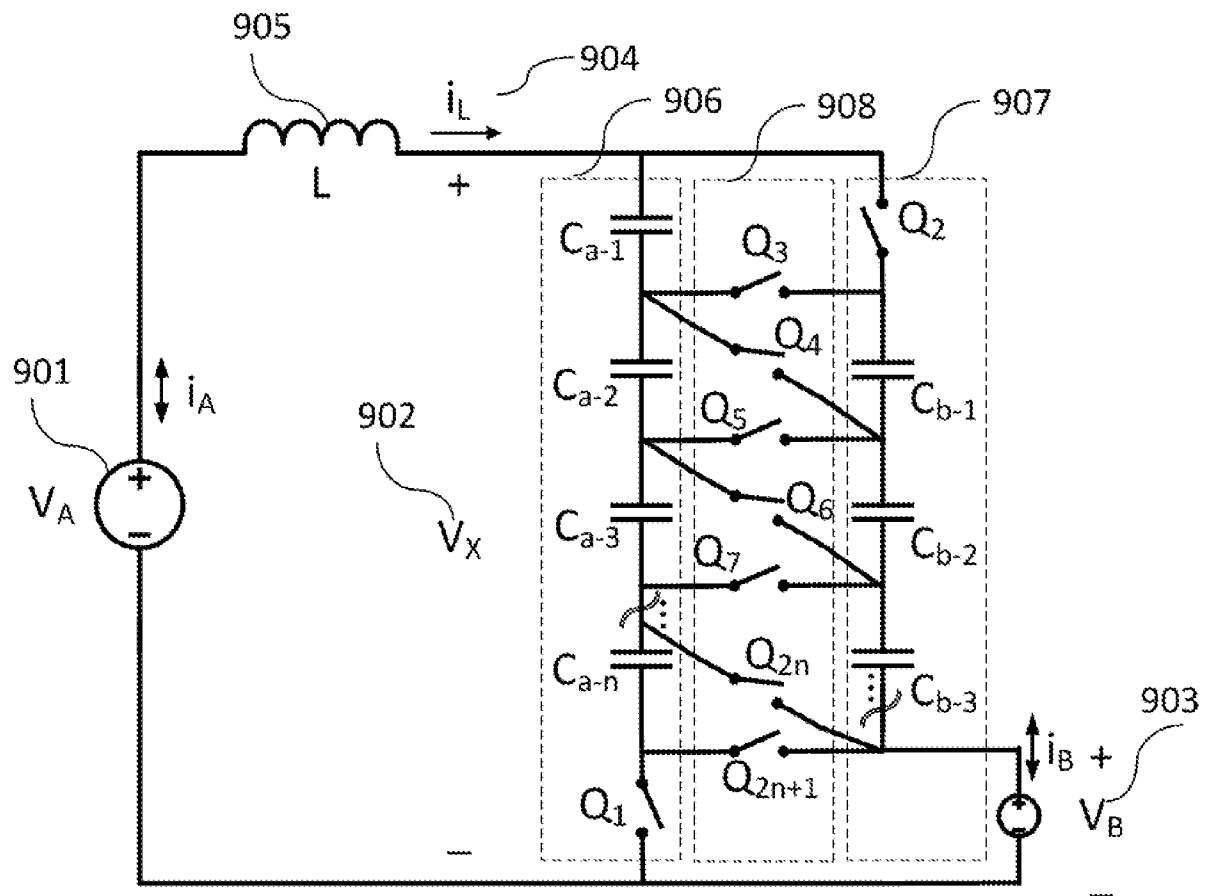


FIG. 9

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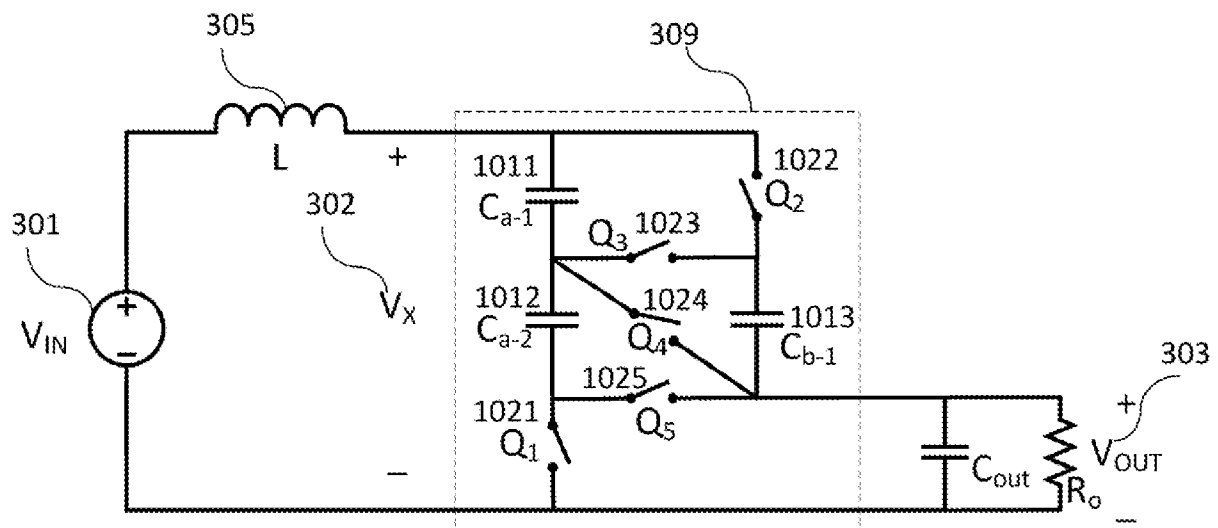


FIG. 10

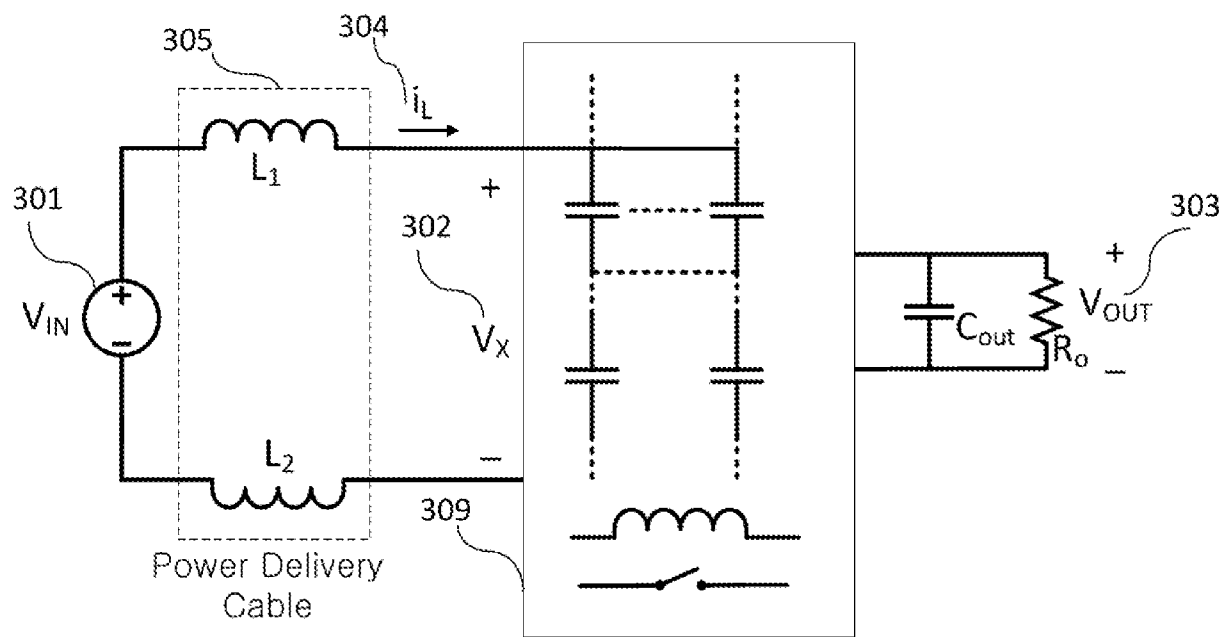


FIG. 11

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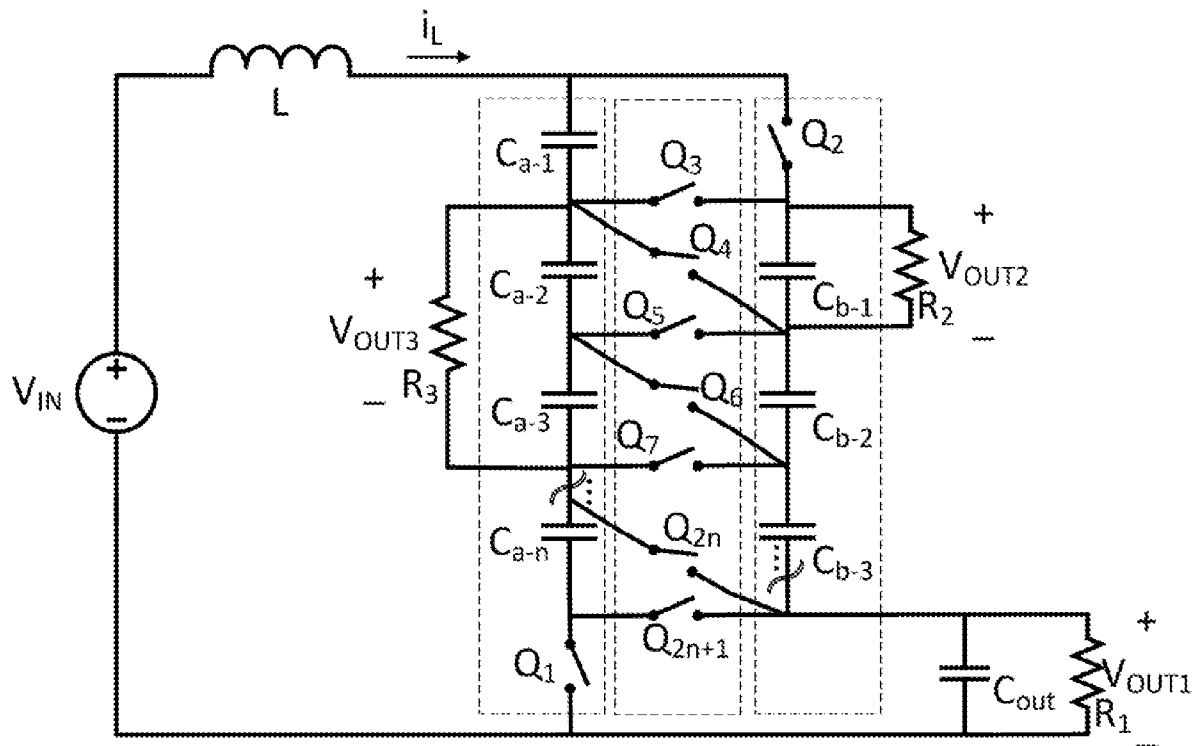


FIG. 12

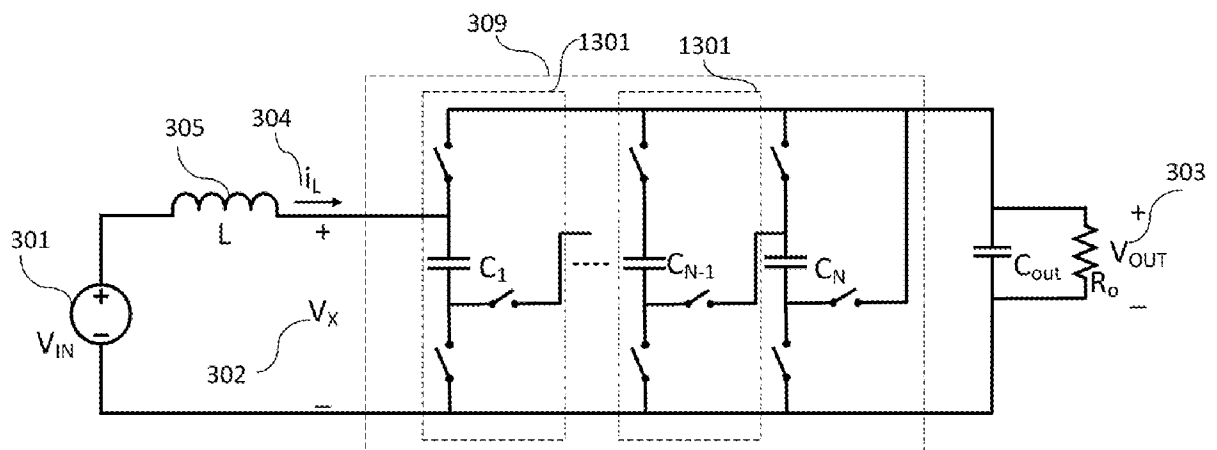


FIG. 13A

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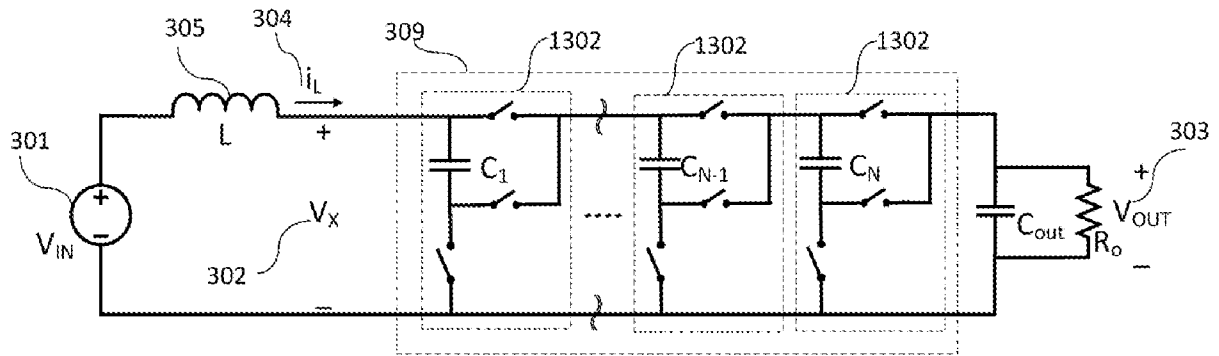


FIG. 13B

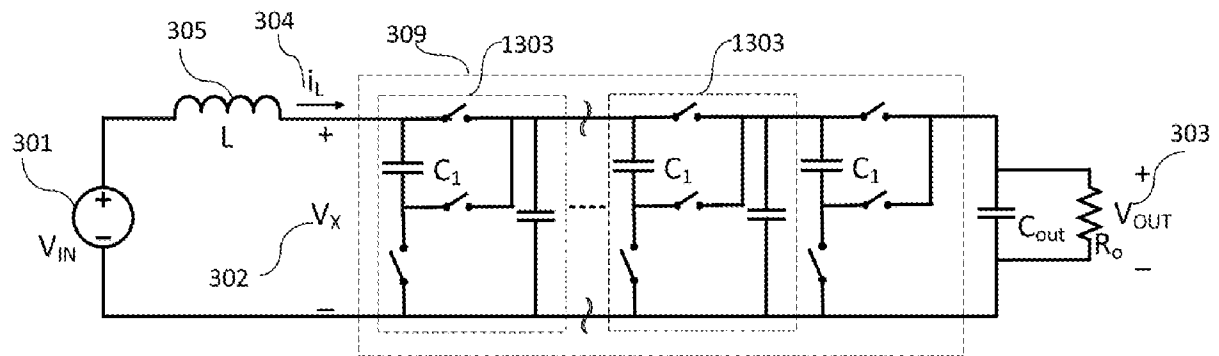


FIG. 13C

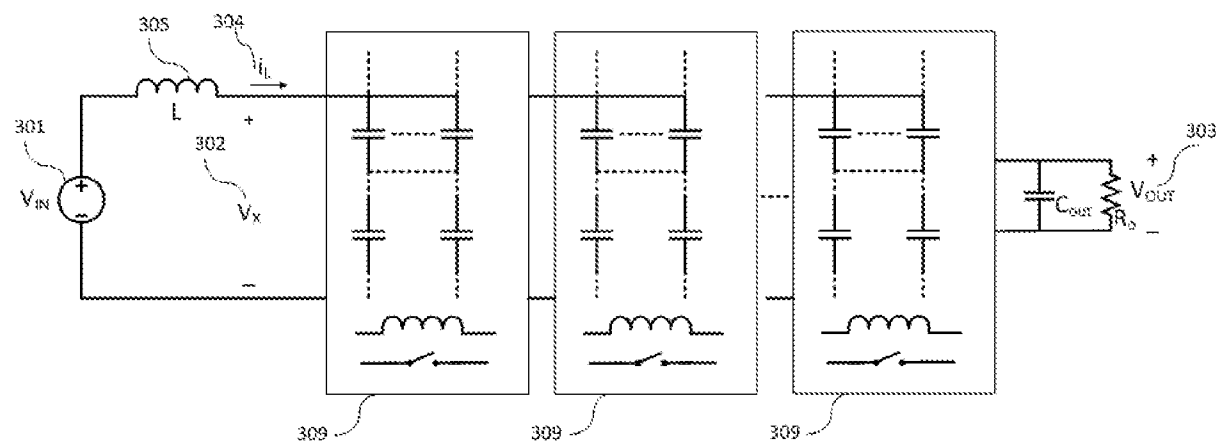


FIG. 14

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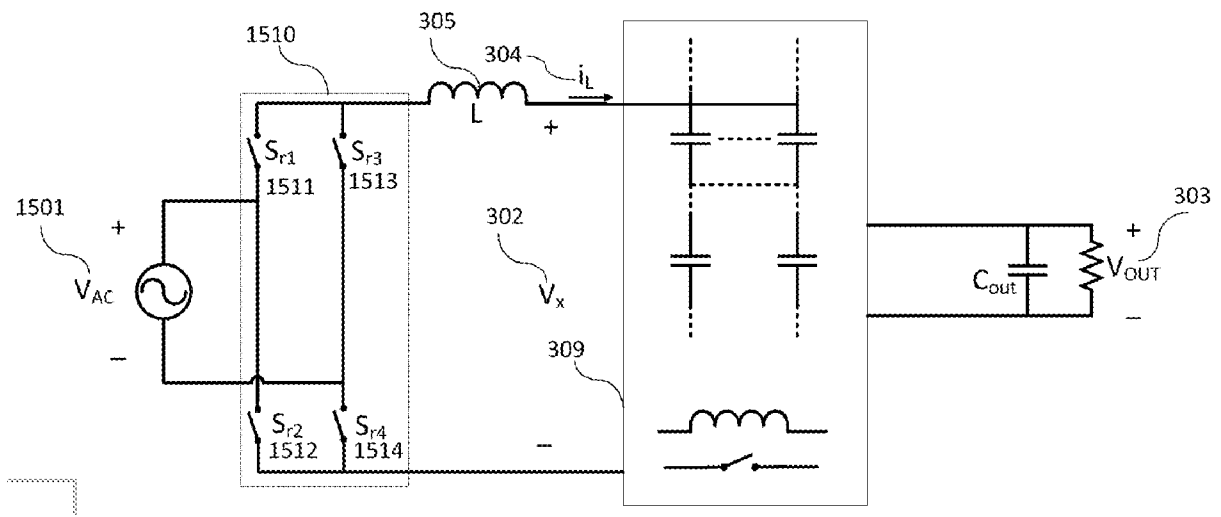


FIG. 15A

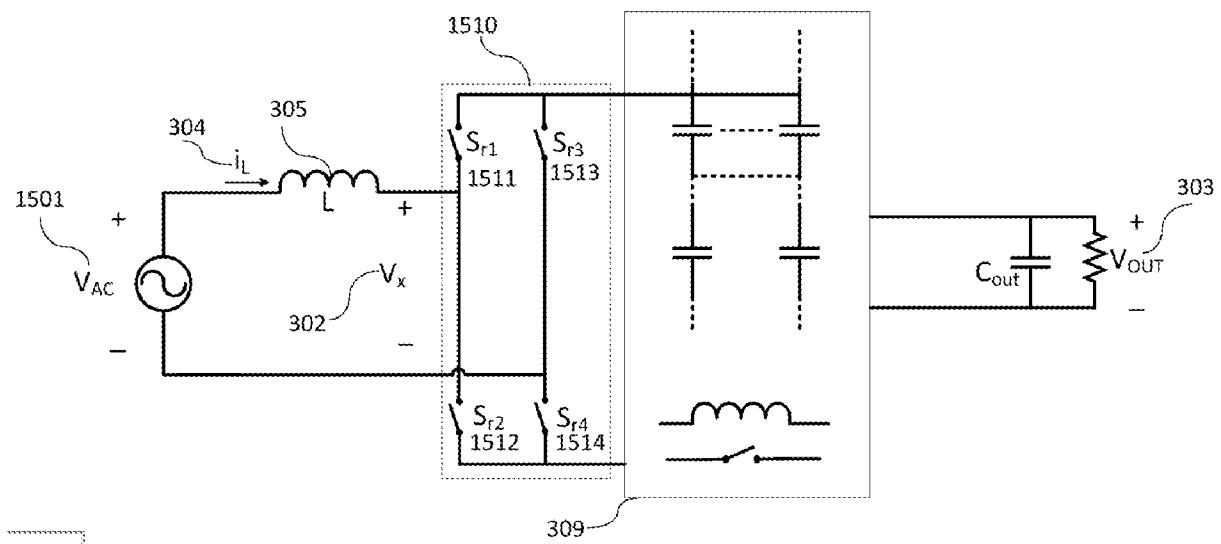


FIG. 15B

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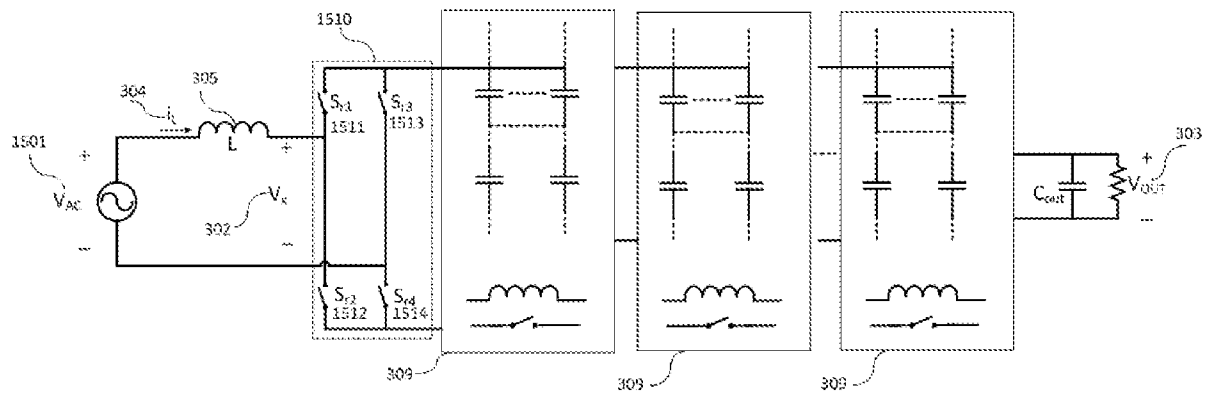


FIG. 15C

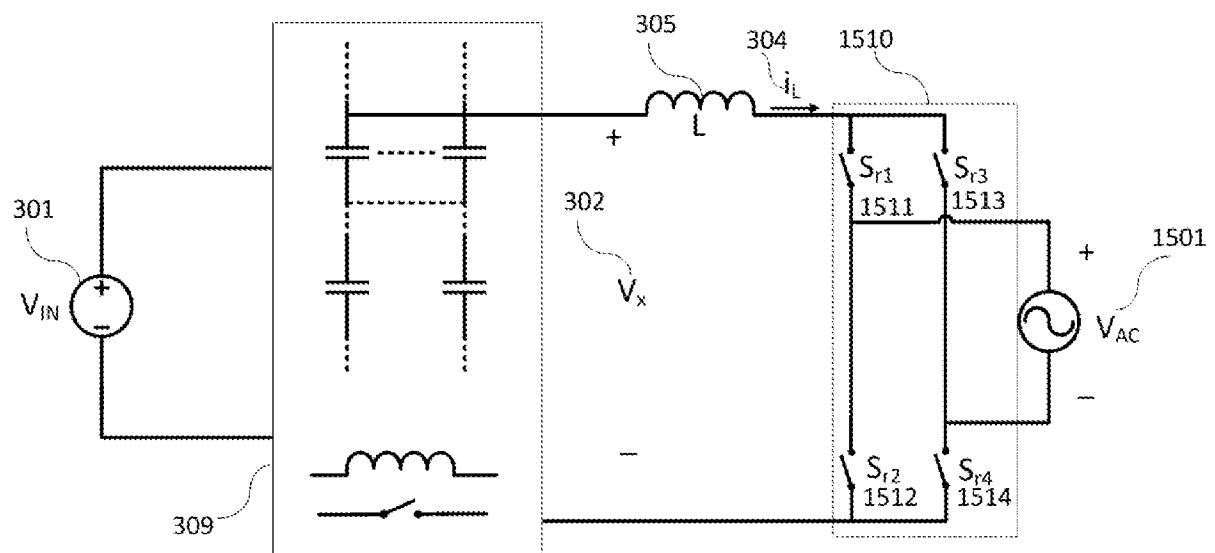


FIG. 16

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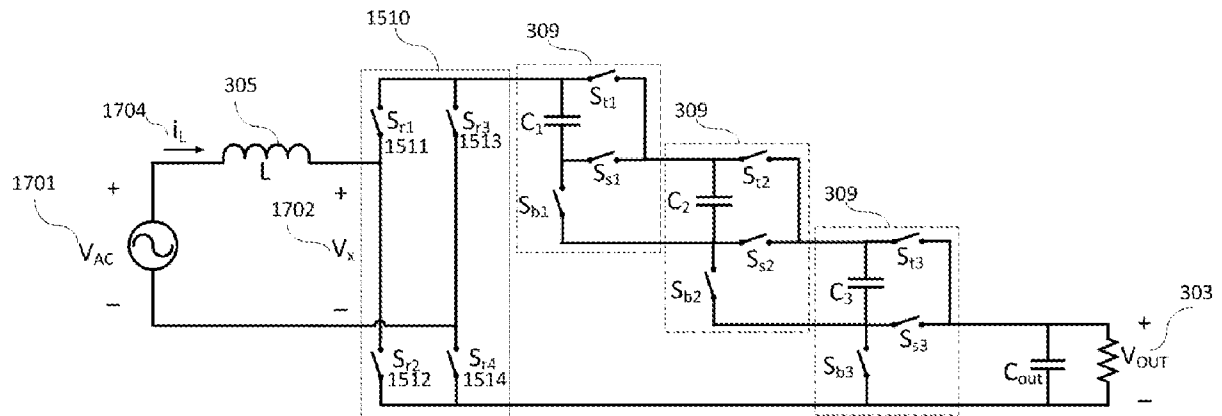


FIG. 17A

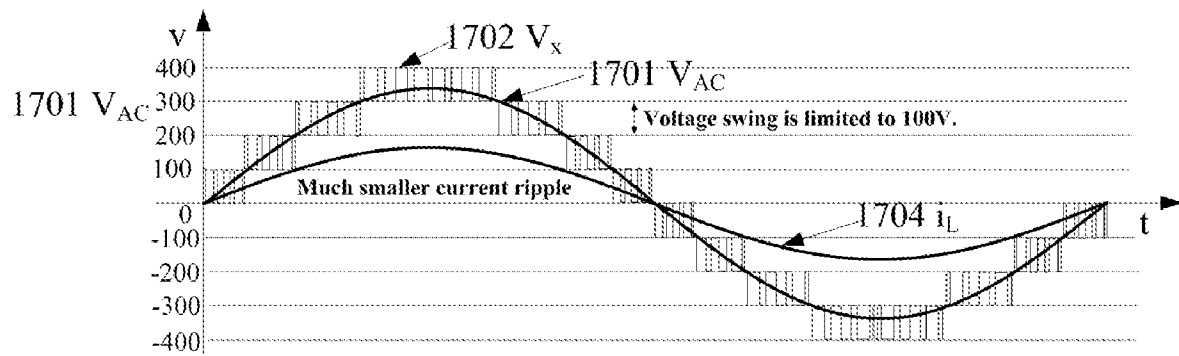


FIG. 17B

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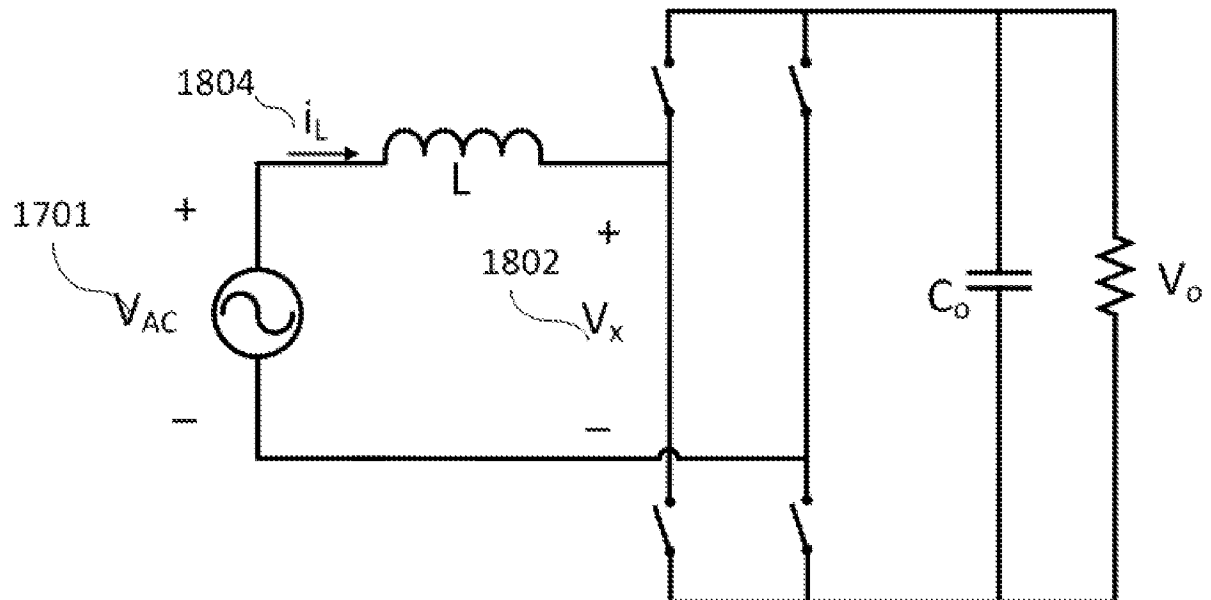


FIG. 18A

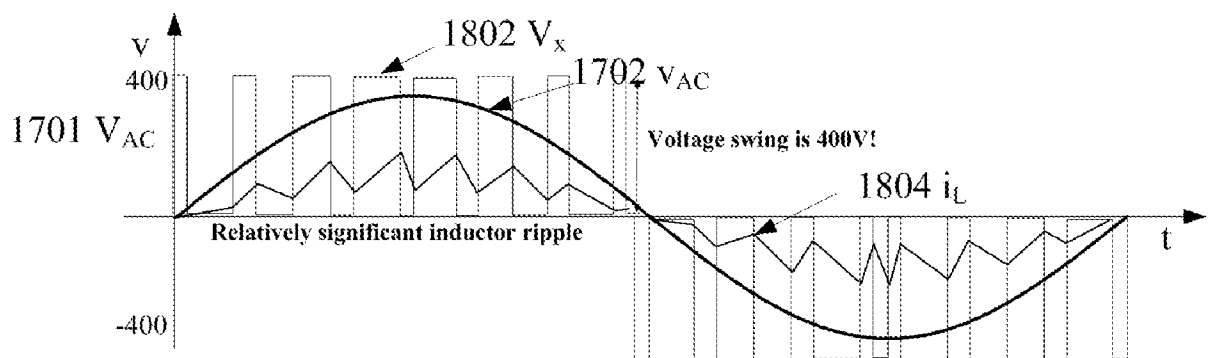


FIG. 18B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 17/35282

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H02M 3/06, H02M 3/07, H02M 3/18, H02M 3/335 (2017.01)

CPC - H02M3/06, H02M3/07, H02M3/18, H02M3/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y --- A	US 2005/0174098 A1 (WATANABE et al.) 11 August 2005 (11.08.2005), entire document, especially FIG. 13A,B, 14A,B, para. [0159]-[0172]	1, 3, 4, 16-22 ----- 5-11 ----- 15
X --- Y	US 2014/0184189 A1 (LOAI GALAL BAHGAT SALEM) 03 July 2014 (03.07.2014), entire document, especially FIG. 10, para. [0103]-[0111]	1, 2, 12 ----- 13, 14
Y --- A	US 2009/0278520 A1 (PERREAULT et al.) 12 November 2009 (12.11.2009), FIG. 2, para. [0052]-[0055]	5-10 ----- 15
Y --- A	US 2014/0346962A1 (THE REGENTS OF THE UNIVERSITY OF CALIFORNIA) 27 November 2014 (27.11.2014), FIG. 14, para. [0072]	7, 10 ----- 15
Y	US 6,963,497 B1 (HERBERT) 08 November 2005 (08.11.2005), col. 1, ln. 59 to col. 2, ln. 8	11
Y	US 2012/0294056 A1 (TEMESI et al.) 22 November 2012 (22.11.2012), FIG. 1, para. [0071]	13, 14
A	US 2016/056714 A1 (ERICSSON TELEFON AB) 25 February 2016 (25.02.2016), FIG. 9A-B	1-22

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 July 2017

Date of mailing of the international search report

28 AUG 2017

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