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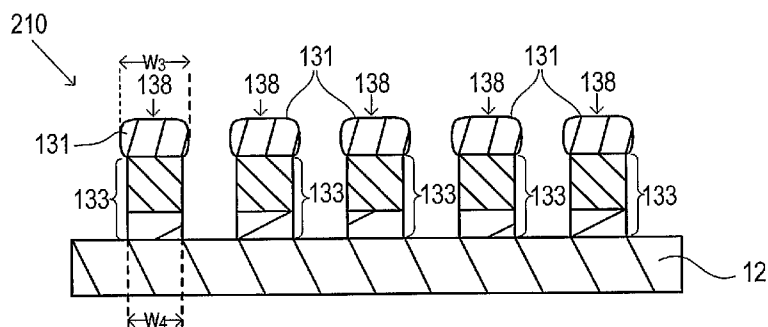
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(54) Title: METHOD OF CONTROLLING THE CRITICAL DIMENSION OF STRUCTURES FORMED ON A SUBSTRATE



(57) Abstract: The present invention provides a method of patterning a substrate, the method including, inter alia, forming a multi-layered structure on the substrate formed from first, second and third materials. The first, second and third materials are exposed to an etch chemistry, with the first and second materials having a common etch rate along a first direction, defining a first etch rate, and the first and third materials having a similar etch rate along a second direction, transversely extending to the first direction, defining a second etch rate. Typically, the etch rate is selected to be different in furtherance of facilitating control of the dimensions of features formed during the etching process.

METHOD OF CONTROLLING THE CRITICAL DIMENSION OF STRUCTURES FORMED ON A SUBSTRATE

BACKGROUND OF THE INVENTION

5 [0001] The field of the invention relates generally to semiconductor processing. More particularly, the present invention is directed to a method of controlling the critical dimension of structures formed on a substrate.

10 [0002] Micro-fabrication involves the fabrication of very small structures, e.g., having features on the order of micro-meters or smaller. One area in which micro-fabrication has had a sizeable impact is in the processing of integrated circuits. As the semiconductor processing industry continues to strive for larger production yields while increasing the circuits per unit area formed on a substrate,
15 micro-fabrication becomes increasingly important. Micro-fabrication provides greater process control while allowing increased reduction of the critical dimension of the structures formed. Other areas of development in which micro-fabrication has been employed include biotechnology, optical technology, mechanical systems, and the like.

20 [0003] As the critical dimension of structures formed on substrates is reduced, there is an increasing desire to control the same. A method of controlling the critical dimension of semiconductor devices is described in U.S. patent number 6,245,581 to Bonser et al. Bonser et al. describes a method and an apparatus for controlling critical dimensions.
25 More specifically, a run of semiconductor devices is processed, a critical dimension measurement is performed upon at least one of the processed semiconductor devices, an analysis of the critical dimension is performed, and a second process upon the semiconductor devices in response to the critical dimension analysis is performed.

30 [0004] Another method of controlling the critical dimension of semiconductor devices is described in U.S. patent number 5,926,690 to Toprac et al. Toprac et al. describes a control method employing a control system using photoresist etch time as a manipulated variable in either a feed-forward or a feedback control configuration to control
35 critical dimension variation during semiconductor fabrication.

[0005] It is desired, therefore, to provide an improved method of controlling the critical dimension of structures formed on a substrate.

SUMMARY OF THE INVENTION

40 [0006] The present invention provides a method of patterning a substrate, the method including, *inter alia*, forming a multi-layered structure on the substrate formed from first, second and third

materials. The first, second and third materials are exposed to an etch chemistry, with the first and second materials having a common etch rate along a first direction, defining a first etch rate, and the first and third materials having a similar etch rate along a second direction, transversely extending to the first direction, defining a second etch rate. Typically, the etch rate is selected to be different in furtherance of facilitating control of the dimensions of features formed during the etching process. These embodiments and others are described more fully below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Fig. 1 is a cross-sectional view of a prior art bi-layer structure;

[0008] Fig. 2 is a cross-sectional view of the bi-layer structure, shown in Fig. 1, having a planarization layer disposed thereon to form a multi-layered structure;

[0009] Fig. 3 is a cross-sectional view of the multi-layered structure, shown in Fig. 2, after being subjected to a blanket etch, forming etched structure, in accordance with the prior art;

[0010] Fig. 4 is a cross-sectional view of the etched structure, shown in Fig. 3, after being subjected to an anisotropic etch process, in accordance with the prior art;

[0011] Fig. 5 is a cross-sectional view of the etched structure, shown in Fig. 3, demonstrating critical-dimension control characteristics that were recognized and attenuated, in accordance with the present invention;

[0012] Fig. 6 is a cross-sectional view of a multi-layered structure formed in accordance with the present invention;

[0013] Fig. 7 is a cross-sectional view of the multi-layered structure, shown in Fig. 6, after being subjected to a blanket etch process, in accordance with the present invention;

[0014] Fig. 8 is a simplified plan view of an etch chamber that may be employed to practice the present invention;

[0015] Fig. 9 cross-sectional view of the multi-layered structure, shown in Fig. 7, after being subjected to an anisotropic etch process, in accordance with the prior art; and

[0016] Fig. 10 is a cross-sectional view of the multi-layered structure, shown in Fig. 9, after subjecting the same to etch processes to expose areas of the underlying substrate.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Referring to Fig. 1, a multi-layered structure 10 is shown. Multi-layered structure 10 comprises a substrate 12, having one or more existing layers thereon, shown as a layer 14, and a patterned layer 16. Layer 14 is disposed between substrate 12 and patterned layer 16. Substrate 12 may be formed from materials including, but not limited to, silicon, gallium arsenide, quartz, fused-silica, sapphire, organic polymers, siloxane polymers, borosilicate glass, fluorocarbon polymers or a combination thereof.

[0018] Primer layer 14 may be formed from any known material, such as aluminum, silicon nitride, a native oxide and the like. In the present example, layer 14 functions to provide a standard interface between substrate 12 and patterned layer 16, thereby reducing the need to customize each process to the material upon which patterned layer 16 is to be deposited upon. In addition, layer 14 may be formed from a material with the same etch characteristics as patterned layer 16. Layer 14 is fabricated in such a manner so as to possess a continuous, smooth, if not planar, relatively defect-free surface that may exhibit excellent adhesion to patterned layer 16. Additionally, layer 14 has a substantially uniform thickness. An exemplary composition for layer 14 is available from Brewer Science, Inc. of Rolla, Missouri under the trade name DUV30J-6. Layer 14 may be deposited upon substrate 12 using any suitable method including, but not limited to, chemical vapor deposition (CVD), physical vapor deposition (PVD), sputter deposition, spin-coating, and dispensing of a liquid.

[0019] Patterned layer 16 may comprise protrusions 18 and recessions 20 forming a pattern on a surface 22 of patterned layer 16, with recessions 20 extending along a direction parallel to protrusions 18 providing a cross-section of patterned layer 16 with a shape of a battlement. However, protrusions 18 and recessions 20 may correspond to virtually any feature required to create an integrated circuit and may be as small as a few nanometers. The pattern on surface 22 of patterned layer 16 may be formed by such techniques including, but not limited to, photolithography, e-beam lithography, x-ray lithography, ion beam lithography, and imprint lithography. Imprint lithography is described in detail in numerous publications, such as United States published patent application 2004/0065976, entitled, "Method and a Mold to Arrange Features on a Substrate to Replicate Features having Minimal Dimensional Variability"; 2004/0065252, entitled "Method of Forming a Layer on a Substrate to Facilitate Fabrication of Metrology Standards"; and

2004/0046271, entitled "Method and a Mold to Arrange Features on a Substrate to Replicate Features having Minimal Dimensional Variability", all of which are assigned to the assignee of the present invention. An exemplary lithographic system utilized in imprint lithography is available under the trade name IMPRIO 250™ from Molecular Imprints, Inc., having a place of business at 1807-C Braker Lane, Suite 100, Austin, Texas 78758. The system description for the IMPRIO 250™ is available at www.molecularimprints.com and is incorporated herein by reference.

[0020] Referring to Fig. 2, a planarization layer 24 is formed upon patterned layer 16, forming multi-layered structure 110. Planarization layer 24 may be formed upon patterned layer 16 in any of the methods mentioned above with respect to primer layer 14. In a first embodiment, planarization layer 26 may comprise an organic polymerizable resist. However, in a further embodiment, planarization layer 24 may be formed from a silicon-containing polymerizable material. Exemplary materials from which patterned layer 16 and planarization layer 24 may be formed are disclosed in United States patent application number 10/789,319, entitled "Composition for an Etching Mask Comprising a Silicon-Containing Material," having Frank Xu, Michael N. Miller and Michael P.C. Watts listed as inventors and which is incorporated by reference herein. For example, patterned layer 16 may be formed from a silicon-free materials and consists of the following:

COMPOSITION 1

isobornyl acrylate

n-hexyl acrylate

ethylene glycol diacrylate

2-hydroxy-2-methyl-1-phenyl-propan-1-one.

[0021] In COMPOSITION 1, isobornyl acrylate comprises approximately 55% of the composition, n-hexyl acrylate comprises approximately 27%, ethylene glycol diacrylate comprises approximately 15% and the initiator 2-hydroxy-2-methyl-1-phenyl-propan-1-one comprises approximately 3%.

The initiator is sold under the trade name DAROCUR® 1173 by CIBA® of Tarrytown, New York. The above-identified composition also includes stabilizers that are well known in the chemical art to increase the operational life of the composition.

[0022] Release properties of COMPOSITION 1 may be improved by including a surfactant. For purposes of this invention a surfactant is defined as any molecule, one tail of which is hydrophobic. Surfactants

may be either fluorine containing, e.g., include a fluorine chain, or may not include any fluorine in the surfactant molecule structure. An exemplary surfactant is available under the trade name ZONYL[®] FSO-100 from DUPONT[™] that has a general structure of R_1R_2 where $R_1 = F(CF_2CF_2)_y$, with y being in a range of 1 to 7, inclusive and $R_2 = CH_2CH_2O(CH_2CH_2O)_xH$, where x is in a range of 0 to 15, inclusive. This provides material with the following composition:

COMPOSITION 2

isobornyl acrylate
n-hexyl acrylate
ethylene glycol diacrylate
2-hydroxy-2-methyl-1-phenyl-propan-1-one
 $R_fCH_2CH_2O(CH_2CH_2O)_xH$,

The ZONYL[®] FSO-100 additive comprises less than 1% of the composition, with the relative amounts of the remaining components being as discussed above with respect to COMPOSITION 1. However, the percentage of ZONYL[®] FSO-100 may be greater than 1%.

[0023] Planarization layer 24 may be formed from a silicon-containing material that is suitable for deposition upon patterned layer 16 employing spin-coating technique. Exemplary compositions from which to form planarization layer 24 are as follows:

COMPOSITION 3

hydroxyl-functional polysiloxane hexamethoxymethylmelamine
toluenesulfonic acid
methyl amyl ketone

COMPOSITION 4

hydroxyl-functional polysiloxane hexamethoxymethylmelamine
gamma-glycidoxypropyltrimethoxysilane
toluenesulfonic acid
methyl amyl ketone

[0024] In COMPOSITION 3, hydroxyl-functional polysiloxane comprises approximately 4% of the composition, hexamethoxymethylmelamine comprises approximately 0.95%, toluenesulfonic acid comprises approximately .05% and methyl amyl ketone comprises approximately 95%. In COMPOSITION 4, hydroxyl-functional polysiloxane comprises approximately 4% of the composition, hexamethoxymethylmelamine comprises approximately 0.7%,

gamma-glycidoxypropyltrimethoxysilane comprises approximately .25%, toluenesulfonic acid comprises approximately .05%, and methyl amyl ketone comprises approximately 95%.

[0025] Both COMPOSITIONS 3 and 4 are made up of at least 4% of the silicone resin. Upon curing, however, the quantity of silicon present in conformal layer 58 is at least 5% by weight and typically in a range of 20% or greater. Specifically, the quantity and composition of the solvent present in COMPOSITIONS 3 and 4 is selected so that a substantial portion of the solvent evaporates during spin-coating application of the COMPOSITION 3 or 4 on solidified imprinting layer 134. In the present exemplary silicon-containing material, approximately 90% of the solvent evaporates during spin-coating. Upon exposing the silicon-containing material to thermal energy, the remaining 10% of the solvent evaporates, leaving conformal layer 58 with approximately 20% silicon by weight.

[0026] Referring to Figs. 1 and 2, planarization layer 24 includes first and second opposed sides. First side 26 faces patterned layer 16 and has a profile complementary to the profile of patterned layer 16. Second side 28 faces away from patterned layer 16. As shown in Fig. 2, second side 28 has a substantially normalized profile. To provide second side 28 with a substantially normalized profile, distances k_1 , k_3 , k_5 , k_7 , k_9 , and k_{11} between protrusions 18 and second side 28 are substantially the same and the distances k_2 , k_4 , k_6 , k_8 , and k_{10} between recessions 20 and second side 28 are substantially the same. One manner in which to provide second side 28 with a normalized profile is to contact planarization layer 24 with a planarizing mold (not shown) having a smooth, if not planar, surface. Planarization layer 24 is exposed to actinic energy to polymerize and, therefore, to solidify the same. Exemplary actinic energy includes ultraviolet, thermal, electromagnetic, visible light, heat, and the like. The selection of actinic energy depends on the materials from which planarization layer 24 is formed. After solidification of planarization layer, planarizing mold (not shown) is separated therefrom. To ensure that planarization layer 24 does not adhere to the planarizing mold (not shown), a low surface energy coating, such as a diamond-like layer, may be deposited upon the planarizing mold (not shown) or the planarization mold (not shown) may be formed from a material having a low surface energy, e.g., diamond. Alternatively, release properties of planarization layer 24 may be improved by including in the material from which the same is fabricated the aforementioned surfactant. The surfactant provides the desired release properties to reduce adherence of planarization layer 24

to the planarizing mold (not shown). It should be understood that the surfactant may be used in conjunction with, or in lieu of, the low surface energy coating that may be applied to the planarizing mold (not shown).

5 [0027] Referring to Figs. 2 and 3, multi-layered structure 110 is subjected to an isotropic or anisotropic etch to remove portions of planarization layer 24 to provide multi-layered structure 110 with a crown surface 30 of etched structure 111. Crown surface 30 is defined by an exposed surface 32 of each of protrusions 18 and surface 34 of
10 areas 35 of planarization layer 24 that remain after certain etch processes. Surfaces 34 have a width ' w_1 '.

[0028] Referring to Figs. 3 and 4, etched structure 111 is subjected to an anisotropic etch. The etch chemistry of the anisotropic etch is selected to maximize etching of protrusions 18 and the segments
15 of patterned layer 16 in superimposition therewith, while minimizing etching of the areas 35. As a result, regions 36 of substrate 12 in superimposition with protrusions 18 are exposed forming a multi-layered structure 210. Multi-layered structure 210 comprises protrusions 38, each of which has an upper region 31 and a nadir region 33. Upper
20 region 31 is fabricated from portions of areas 35 that remain. Nadir regions 33 comprise patterned layer 16 and primer layer 14 in superimposition with areas 35. Protrusions 138 have a width ' w_2 '. Ideally, width ' w_2 ' is substantially the same as width ' w_1 ' of portions 34.

25 [0029] Referring to Figs. 4 and 5, obtaining ideal dimensions of widths w_1 and w_2 is often problematic. For example, it has often been found that upper region 131 has a width ' w_3 ' that differs from the width ' w_4 ' of nadir region 133. As shown in Fig. 5, width ' w_3 ' is greater than width ' w_4 ,' however; width ' w_3 ' may be smaller than width ' w_4 .' The
30 variation of width ' w_3 ' as compared to width ' w_4 ' may be as a result of subjecting crown surface 30, shown in Fig. 3, to the aforementioned anisotropic etch. The difference in width may be due to any one or more of several factors, including swelling of upper region 131 in response to the etch chemistry employed to form protrusions 138. Alternatively,
35 or in addition to the aforementioned swelling, undercutting, and/or sputtering of nadir region 133 may occur during formation of protrusions 138. Nonetheless, it is desired to have width ' w_3 ' be substantially the same as width ' w_4 ,' and thus, width ' w_3 ' substantially the same as width ' w_1 ,' shown in Fig. 3. To that end, a liner layer is employed to
40 substantially surround exposed sides of the segments of upper region 131. A liner layer for purposes of the present invention is to be

defined as a layer that substantially conforms to the shape of the surface upon which it is disposed and substantially insulates the material from desired processes. Typically, liner layer is thinner than the layer upon which it is disposed.

5 [0030] Referring to Fig. 6, a liner layer 40 is formed so that same may be present between patterned layer 16 and planarization layer 24, forming multi-layered structure 310. To that end, liner layer 40 is deposited on patterned layer 16. An exemplary liner layer 40 would have a relative thickness and etch rate differential, compared to patterned
10 layer 16 and/or planarization layer 24, which enables formation of a desired pattern in primer layer 14 and/or substrate 12. Typically, the pattern formed therein corresponds to the pattern in patterned layer 16. In the present example, liner layer 40 has a thickness in a range of 5 nm to 100 nm, inclusive and provides an etch rate differential of no
15 less than 10:1. For example, the etch rate of the liner layer 40, for a given etch chemistry, may be ten times faster than the etch rate of patterned layer 16 and/or planarization layer 24. Alternatively, the etch rate of liner layer 40, for a given etch chemistry, may be ten times slower than the etch rate of patterned layer 16 and/or
20 planarization layer 24. In this manner, liner layer 40 functions as a hard mask. To that end, exemplary material from which to form liner layer 40 includes silicon dioxide (SiO_2), silicon nitride (SiN) and silicon oxynitride (SiON). It is desired that liner layer 40 be formed from processes that would not compromise the structural integrity of
25 patterned layer 16 and/or planarization layer 24. For example, were patterned layer 16 formed from COMPOSITION 1 or COMPOSITION 2, it would be desired that the process employed to deposit liner layer 40 employs temperatures no greater than 150 degrees Celsius. An exemplary process by which to deposit liner layer 40 formed from SiO_2 is discussed by J.W.
30 Klaus and S.M. George in the article entitled " SiO_2 Chemical Vapor Deposition at Room Temperatures Using SiCl_4 and H_2O with an NH_3 Catalyst," Journal of the Electrochemical Society, 147(7) 2658-2664 (2000). An exemplary process by which to deposit liner layer 40 formed from SiN is discussed by G.P. Li and Huinan Guan in an article entitled
35 "Exploring Low Temperature High Density Inductive Coupled Plasma Chemical Vapor Deposition (HDICPCVD) Dielectric Films for MMICs," project Report 2002-03 for MICRO Project 02-241, Department of Electrical & Computer Engineering, University of California, Irvine, California. After formation of liner layer 40, planarization 24 is
40 disposed atop thereof, as discussed above.

[0031] Referring to Figs. 6 and 7, multi-layered structure 310 is subjected to an etch process to remove portions of planarization layer 24 to provide a multi-layered structure 410 with a crown surface 230, wherein the isotropic etch may be an O₂ etch. To that end, multi-layered structure 310 may be deposited in an inductively coupled plasma etch reactor 330, shown in Fig. 8.

[0032] Referring to Fig. 8, reactor 330 includes upper 332 and lower 333 bodies and a cover 334, which defines a chamber 336. Cover 334 includes a dielectric window 338 and a coil 340 disposed proximate to dielectric window 338. Multi-layered structure 310 is supported within chamber 336 by a pedestal 342 or chuck, with dielectric window 338 disposed between structure 310 and coil 340. Coil 334 typically includes multiple windings and is connected to a radio frequency (RF) power generator 344 through an impedance matching network 346 to provide RF power into chamber 336. In addition, a bias RF power generator 348 and associated impedance matching circuit 350 is connected to pedestal 342 and used to impose a bias on multi-layer structure 310. Upper body 332 is composed of dielectric material, typically quartz or ceramic, so as to minimize attenuation of the RF power coupled into chamber 336. Lower body 333 surrounds pedestal 342 and is formed from electrically conductive material. Lower body 333 coupled to ground functions as the ground for the RF power supplied to pedestal 342. Also included are cooling channels 352 formed within the lower body 333 and pedestal 342. A supply of coolant fluid 353 may be pumped through channels 352 to transfer heat away from the interior of chamber 336 and/or pedestal 342 to control the temperature thereof. The temperature of upper body 332 may be controlled by forced air convection/conduction methods. A source 354 of etchant gases is in fluid communication with chamber 336 through gas injection ports 356. A vacuum pump 358 is in fluid communication with chamber 336 to control the pressure of the atmosphere therein. An exemplary reactor that may be employed is available from Oxford Instruments America, Inc. 130 Baker Avenue, Concord, Massachusetts 01742 under the product name PLASMALAB 80 PLUS.

[0033] Referring to Figs. 6, 7 and 8, assuming planarization layer 24 is formed from one of COMPOSITIONS 3 and 4, crown surface 230 is formed by exposing multi-layered structure 310 to an etch chemistry that includes oxygen flowed into chamber 336 at a rate of approximately 30 standard cubic centimeters per minute (sccm), CHF₃ flowed into chamber 336 at a rate of approximately 12 sccm. RF power 344 is established to be at 45 Watts at 13.56 MHz, and DC bias 350 is set at -185 volts. Pump 358 establishes a chamber pressure of approximately 20 Torr, and

pedestal 342 is maintained at a temperature of approximately -8 °C. With these parameters, crown surface 230 is formed in approximately 4 minutes and 40 seconds. Were planarization layer formed from one of COMPOSITIONS 1 and 2, i.e., without any silicon being present, the same
5 etch parameters mentioned above may be employed excepting that CHF₃ is not introduced into chamber 336.

[0034] As a result of etching planarization layer 24, crown surface 230 is defined by exposed regions of liner layer 40 and regions 233 that remain of planarization layer 64 after being exposed to the
10 isotropic O₂ etch. Exposed regions of liner layer 40 include surfaces of first portions 232, which are in superimposition with protrusions 18 and surfaces of second portions 235. Second portions 235 are disposed on opposed ends of first portion 232 and in superimposition with recession 20. Extending between subsets of adjacent second portions 235
15 are nadir portions 237.

[0035] Referring to Figs. 7-9, an anisotropic etch is employed to substantially remove first portion 232 and surfaces of second portions 235. To that end, multi-layered structure 410 is subjected to an etching environment in chamber 336 by establishing RF power 344 to be
20 approximately 50 Watts at 13.56 MHz, DC bias 350 to be approximately -196 volts, chamber pressure at approximately 30 Torr, with the oxygen flow being terminated. Pedestal 342 is maintained at a temperature of approximately -8 °C. With these parameters a multi-layered structure 510 having a surface with a shape of a battlement is formed by exposure
25 of multi-layered structure 410 to this etching environment for approximately 1 minute and ten seconds. The battlement surface is defined by exposed surfaces 342 in regions of patterned layer 16 that were in superimposition with protrusions 18, as well as surfaces 334 of remaining portions of regions 133 and surfaces 336 the remaining areas
30 of second portions 235. An extent of second portions 235, extending between surface 336 and surface 342 define sidewalls 344.

[0036] Referring to Figs. 9 and 10, an anisotropic etch is employed to remove portions of multi-layered structure 510 in superimposition with exposed surfaces 342, forming multi-layered structure 610. To that
35 end, multi-layered structure 510 is subjected to an etching environment in chamber 336 by establishing RF power 344 to be approximately 130 Watts at 13.56 MHz, DC bias 350 to be approximately -380 volts, chamber pressure at approximately 6 Torr, with the CHF₃ being replaced by a flow of argon and oxygen. The argon is flowed into chamber 336 at a rate of
40 approximately 30 sccm and the oxygen at a rate of approximately 3 sccm. Pedestal 342 is maintained at a temperature of approximately -8 °C.

With these parameters a multi-layered structure 610 is formed by exposure of multi-layered structure 510 to this etching environment for approximately 6 minutes. More specifically, portions of primer layer 14 and patterned layer 16 in superimposition with exposed surfaces 342 are removed. As a result, areas 548 of substrate 12 in superimposition with exposed surfaces 342 are exposed, leaving spaced-apart protrusions 650. Each protrusion 650 includes a sub-portion 614 of planarization layer 14, a sub-portion 616 of patterned layer 16 and an upper portion 610. Upper portion 610 includes a sub-portion 612 of sidewall 344, nadir portion 237 and the remaining portions of region 133 in superimposition with nadir portion 237. A width ' w_5 ' of upper portion 610 is substantially equal to a width ' w_6 ' of lower portion. Specifically, sub-portions 612 ensures that width ' w_5 ' is substantially the same as width ' w_6 ,' as desired. In this manner, width ' w_5 ' and, therefore, width ' w_6 ' may be substantially the same as width ' w_1 ,' shown in Fig. 3.

[0037] In a further embodiment, planarization layer 24 may be formed from a silicon-containing polymerizable material. More specifically, planarization layer 24 may be formed from a silicon-containing spin-on material. Therefore, the aforementioned isotropic etch to remove portions of planarization layer 24 to provide multi-layered structure 410 may be a halogen etch. Also, multi-layered structure 610 may be utilized in a lift-off process.

[0038] The embodiments of the present invention described above are exemplary. Many changes and modification may be made to the disclosure recited above, while remaining within the scope of the invention. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

WHAT IS CLAIMED IS:

1. A method of patterning a substrate, said method comprising:
forming a multi-layered structure on said substrate formed from first, second and third materials; and
exposing said first, second and third materials to an etch chemistry, with said first and second materials having a common etch rate along a first direction, defining a first etch rate, and said first and third materials having a similar etch rate along a second direction, transversely extending to said first direction, defining a second etch rate.
2. The method as recited in claim 1 wherein said first rate differs from said second etch rate.
3. The method as recited in claim 1 wherein said first etch rate is less than said second etch rate.
4. The method as recited in claim 1 wherein said first etch rate is greater than said second etch rate.
5. The method as recited in claim 1 wherein exposing further includes concurrently exposing said first, second and third material to said etch chemistry.
6. The method as recited in claim 1 wherein said substrate includes a primer layer, with forming further including forming said multi-layered structure on said primer layer.
7. The method as recited in claim 1 wherein forming further includes disposing upon said substrate a patterned layer formed from said third material, forming upon said pattern layer, a conformal layer, with said conformal layer being formed from said first material, and covering said conformal layer with a layer of said third material and removing portions of said multi-layered structure to define a first interface of said first and second materials and a second interface of said first and third materials.
8. The method as recited in claim 1 wherein forming further includes disposing upon said substrate a patterned layer formed from said third material and having a recession formed therein, said recession having a width, and forming upon said pattern layer, a liner

layer formed from said first material and a portion of which covers said recession defining a sidewall portion and a nadir portion, and generating a projection on said substrate, with said projection having a width defined by the width of said recession.

9. The method as recited in claim 1 wherein forming further includes depositing a planarization layer upon said liner layer and forming a crown surface including exposed regions of said liner layer spaced-apart by exposed regions of said planarization layer disposed between adjacent exposed regions.

10. A method of patterning a substrate, said method comprising: disposing upon said substrate a patterned layer formed from a third material and having a recession formed therein, said recession having a width, and forming upon said pattern layer, a liner layer formed from a first material, a portion of which covers said recession defining a sidewall portion and a nadir portion, and a planarization layer, formed from a second material; and

exposing said first, second and third materials to multiple etching processes to generate a projection on said substrate, with said projection having a width defined by the width of said recession.

11. The method as recited in claim 10 wherein exposing further includes concurrently exposing said first, second and third materials to a common etch chemistry, with said first and second materials having a common etch rate along a first direction to said common etch chemistry, defining a first etch rate, and said first and third materials having a similar etch rate along a second direction to said common etch chemistry, with said second direction being transverse to said first direction, defining a second etch rate, with said second etch rate differing from said first etch rate.

12. The method as recited in claim 10 wherein said substrate includes a primer layer, with disposing further including disposing upon said primer layer.

13. The method as recited in claim 10 wherein exposing further includes forming a crown surface including exposed regions of said liner layer spaced-apart by exposed regions of said planarization layer located between adjacent exposed regions of said liner layer.

14. A method of patterning a substrate, said method comprising:
creating a multi-layered structure by forming on said substrate, a patterned layer having a coating disposed thereon, said patterned layer having a plurality of protrusions and recessions, and forming upon said coating, a planarization layer; and

selectively removing portions of said multi-layered structure to form a plurality of projections on said substrate, said projections comprising a first layer having a first width associated therewith and a second layer having a second width associated therewith, said first layer comprising a pair of spaced-apart sidewalls having portions of said planarization layer disposed therebetween, with said sidewalls establishing said first width such that said first width is substantially the same as said second width.

15. The method as recited in claim 14 wherein selectively removing said portions further includes exposing a plurality of regions of said substrate in superimposition with said protrusions.

16. The method as recited in claim 15 wherein said method further includes having a region of said plurality of regions being disposed between adjacent projections of said plurality of projections.

17. The method as recited in claim 16 wherein said method further includes selectively removing portions of said coating in superimposition with said protrusions to expose an apex of said plurality of protrusions.

18. The method as recited in claim 17 further including forming a primer layer between said patterned layer and said substrate.

19. The method as recited in claim 18 wherein said plurality of protrusions have a third width associated therewith, with said sidewalls further establishing said first width such that said first width is substantially the same as said third width.

20. The method as recited in claim 19 wherein said method further includes forming said planarization layer from a group of materials including a silicon-containing polymerizable material and an organic polymerizable resist.

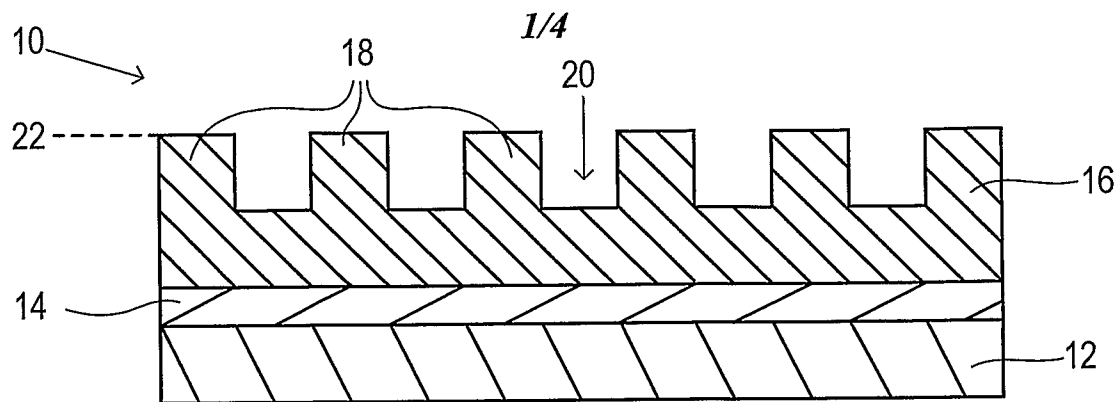


FIG. 1
(Prior Art)

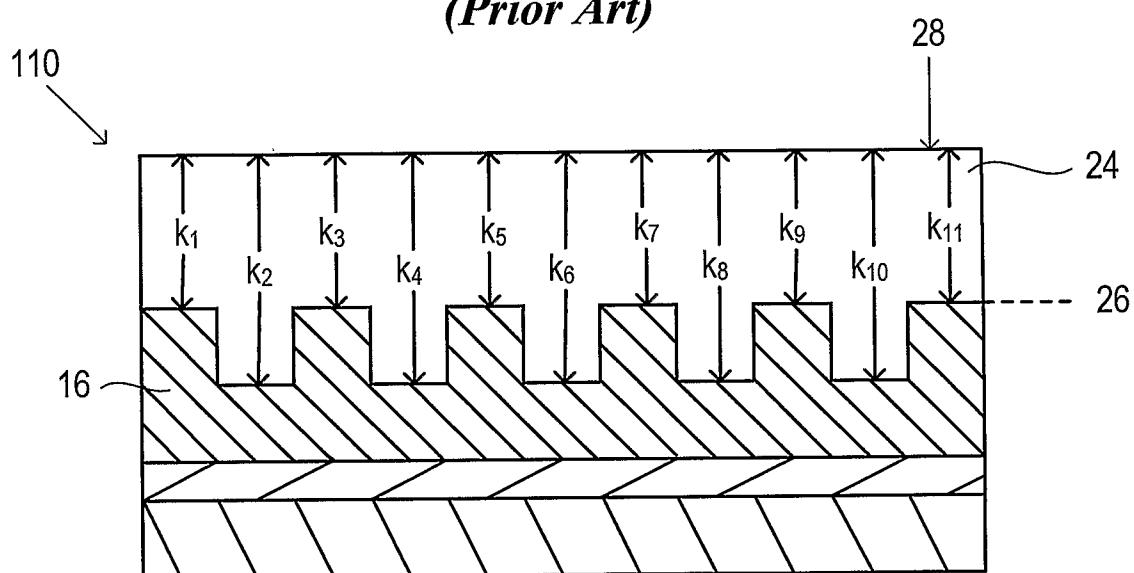


FIG. 2
(Prior Art)

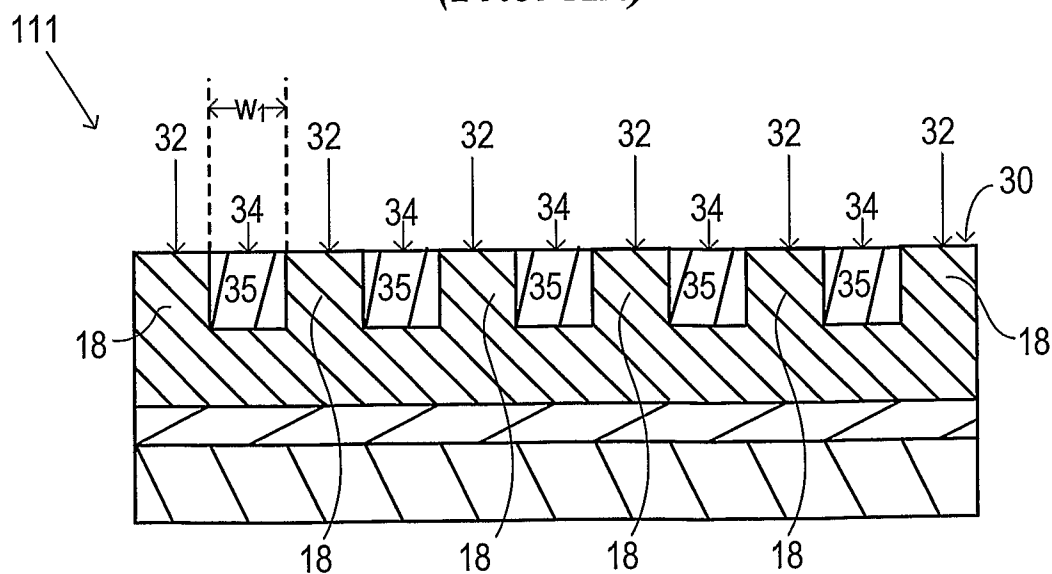


FIG. 3
(Prior Art)

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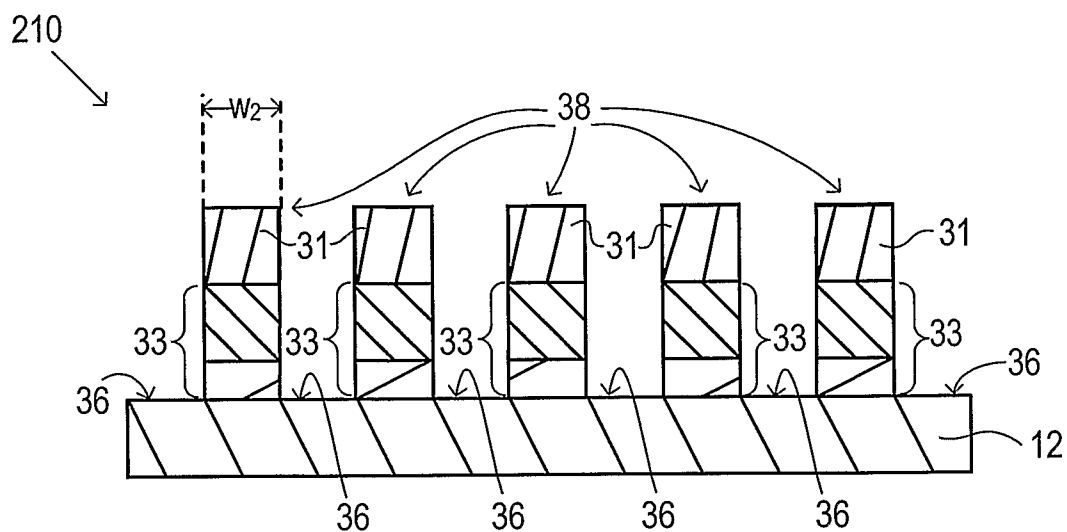


FIG. 4
(Prior Art)

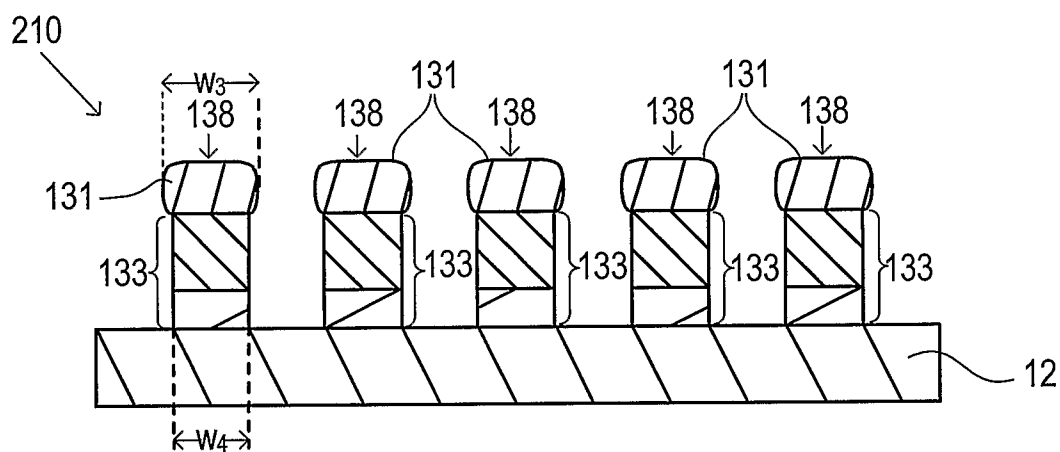


FIG. 5

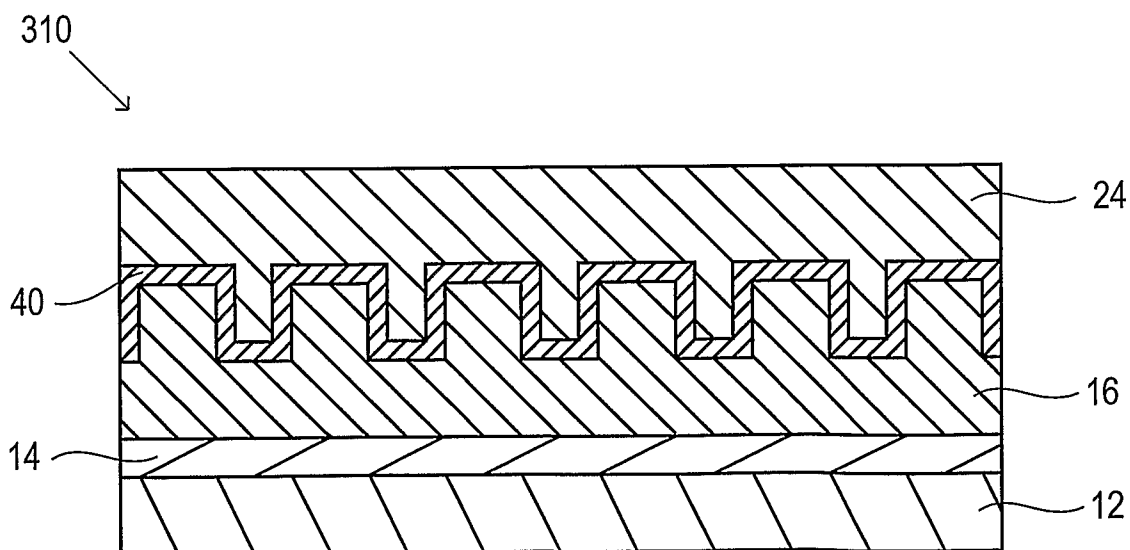


FIG. 6

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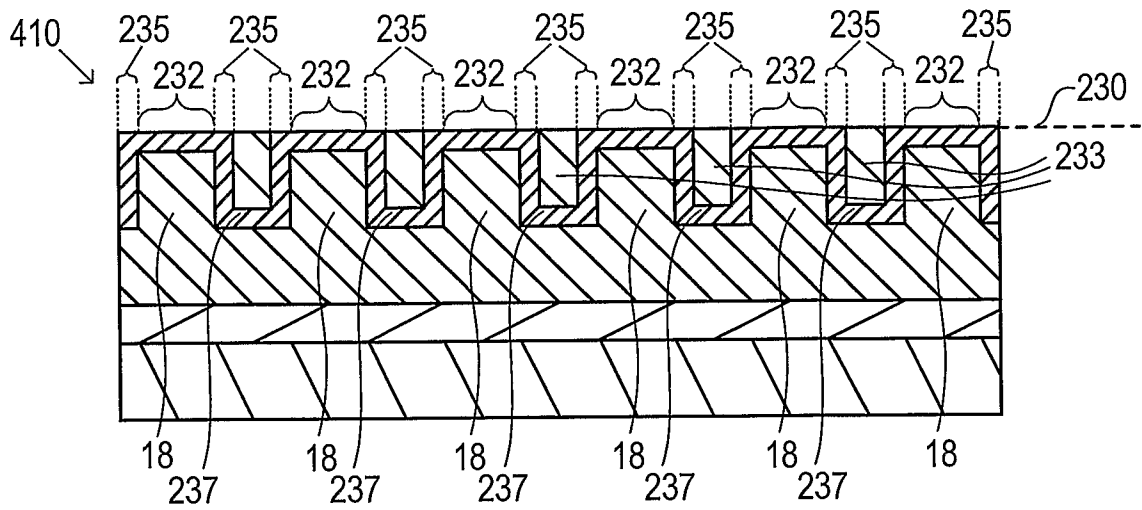


FIG. 7

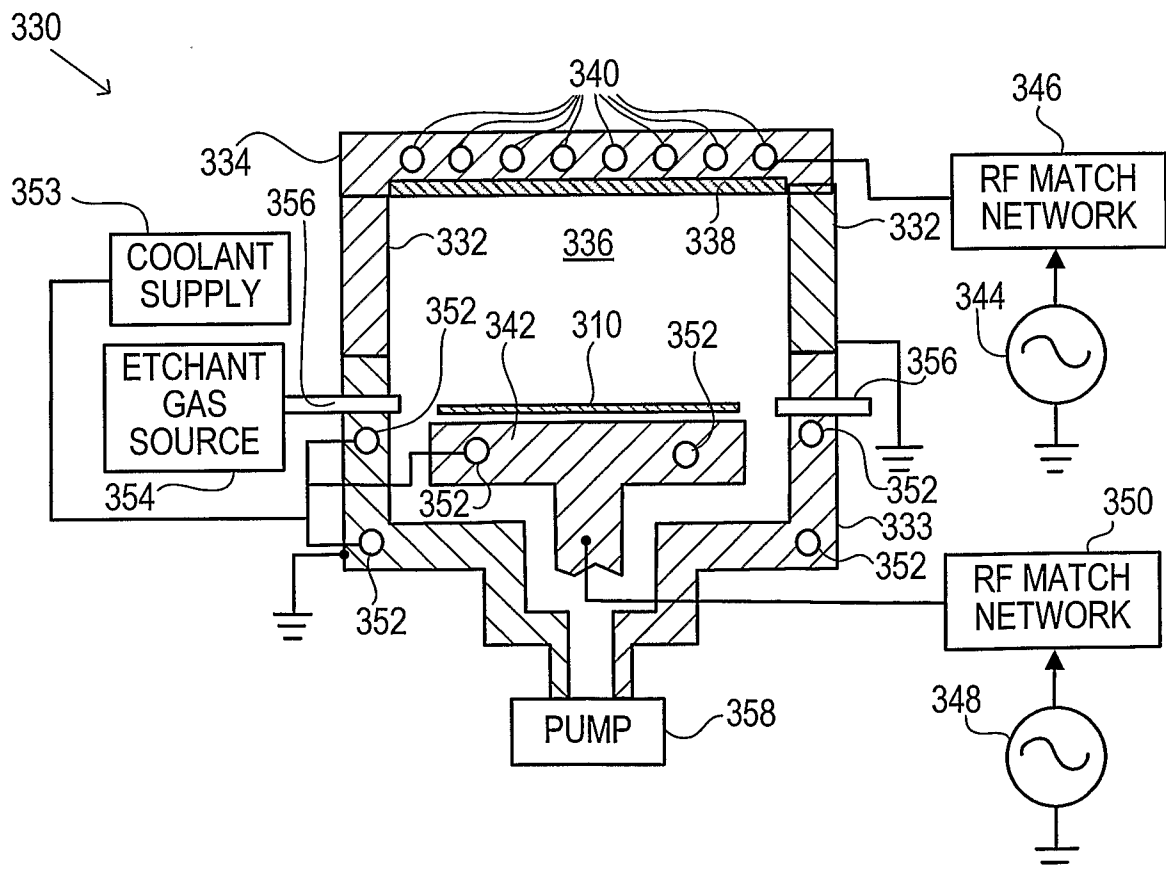
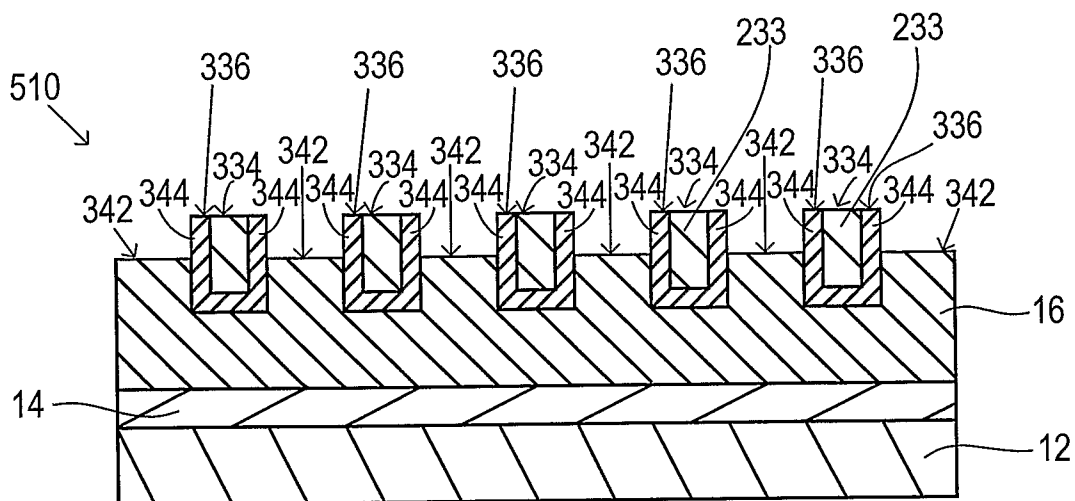
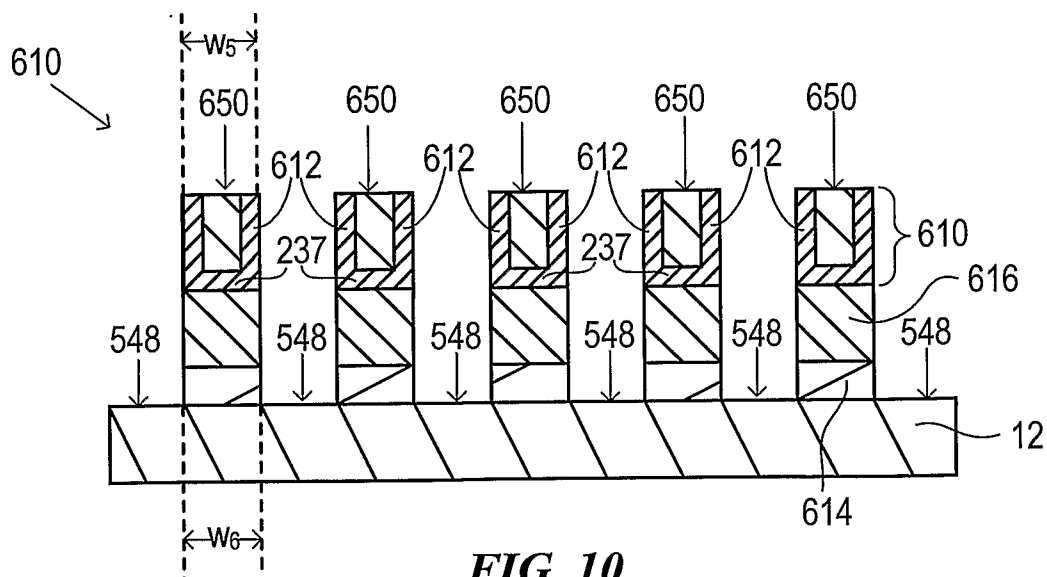


FIG. 8

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**FIG. 9****FIG. 10**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US06/21949

A. CLASSIFICATION OF SUBJECT MATTER

IPC: H01L 21/302(2006.01),21/461(2006.01)

USPC: 438/710

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/710,586,690;977/887,888,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,Y	US 5,954,997 A (KAUFMAN et al) 21 September 1999 (21.09.1999) see entire document.	1-9
X	US 2004/0029372 A1 (JANG et al) 12 February 2004 (12.02.2004) see entire document.	10 and 12-19
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Y		11
Y	Wolf et al. Silicon Processing for the VLSA Era; Process Technology; 1986, vol. 1; para.2, pages 546-547.	11
A	US 5,110,514 A (SOANE) 05 May 1992 (05.05.1992) see entire document.	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"

document member of the same patent family

Date of the actual completion of the international search

28 August 2006 (28.08.2006)

Date of mailing of the international search report

25 SEP 2006

Name and mailing address of the ISA/US

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for

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US06/21949

Continuation of B. FIELDS SEARCHED Item 3:
Search Text: EAST;US-PGPUB;EPO;JPO;DERWENT;IBM_TDB;USPAT;
Search Terms: titanium nitride, copper, alloy