



(51) International Patent Classification:

G11C 11/4063 (2006.01) G06F 7/58 (2006.01)

(21) International Application Number:

PCT/CN2019/116061

(22) International Filing Date:

06 November 2019 (06.11.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

201811325774.6 08 November 2018 (08.11.2018) CN

201821859417.3 08 November 2018 (08.11.2018) CN

(71) Applicant: **CHANGXIN MEMORY TECHNOLOGIES, INC.** [CN/CN]; Room 630, Haiheng Build-

ing, No. 6, Cuiwei Road, Economic And Technological Development Zone, Hefei, Anhui 230000 (CN).

(72) Inventors: **Ji, Kangling**; Room 630, Haiheng Building, No. 6, Cuiwei Road, Economic And Technological Development Zone, Hefei, Anhui 230000 (CN). **SHANG, Weibing**; Room 630, Haiheng Building, No. 6, Cuiwei Road, Economic And Technological Development Zone, Hefei, Anhui 230000 (CN).

(74) Agent: **SHANGHAI SAVVY INTELLECTUAL PROPERTY AGENCY**; Unit 606, Shenergy International Building, 1 Middle Fuxing Road, Huangpu District, Shanghai 200021 (CN).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,

(54) Title: SEMICONDUCTOR MEMORY

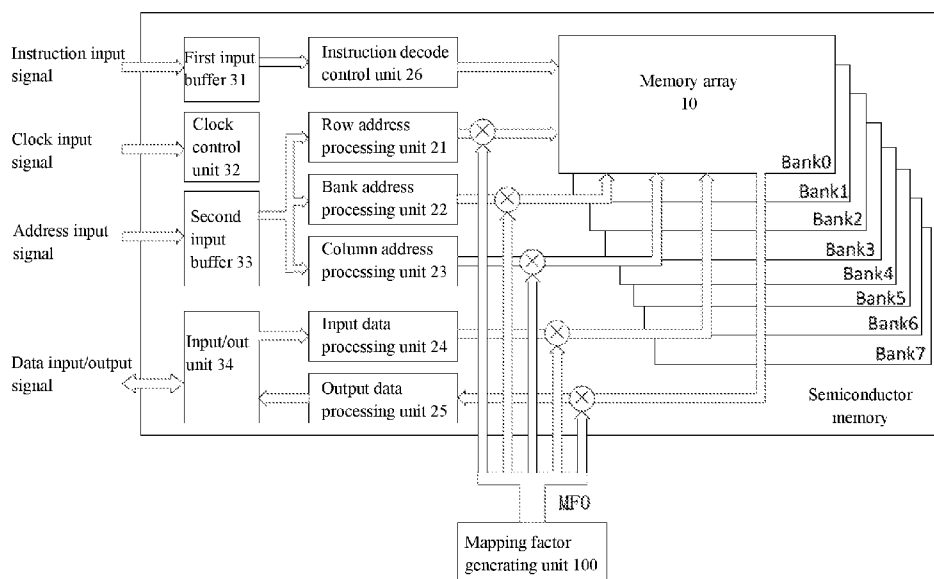


FIG. 1

(57) Abstract: A semiconductor memory is provided. The memory includes: a memory array(10); a row address processing unit(21) configured to output a row address; a bank address processing unit(22) configured to output a bank address; a column address processing unit(23) configured to output a column address; and a mapping factor generating unit(100), configured to generate a mapping factor, wherein an output of the mapping factor generating unit(100) is coupled to at least one of an output of the row address processing unit(21), an output of the bank address processing unit(22), and an output of the column address processing unit(23), and the output of the mapping factor generating unit(100) is further coupled to the memory array(10), and wherein the memory array(10) receives a result from logical processing performed on the mapping factor and at least one of the row address, the bank address, and the column address. It can improve the security, service life and reliability of the semiconductor memory.

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

SEMICONDUCTOR MEMORY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority of the Chinese Patent Application No. 201811325774.6, filed on November 8, 2018 and entitled “SEMICONDUCTOR MEMORY.” The above-referenced application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to the field of integrated circuit technologies and more specifically, to a semiconductor memory.

BACKGROUND

[0003] The information disclosed in this Background section is only for providing a background or context for the embodiments of the present invention set forth in the claims, and therefore may contain information that does not form the prior art already known to a person of ordinary skill in the art.

[0004] Semiconductor memory devices include, for example, static random access memories (SRAM), dynamic random access memories (DRAM), read only memories (ROM), flash memory, etc.

[0005] In the case of DRAM, as the feature size of DRAM becomes smaller and smaller, the reliability issues of DRAM become increasingly pronounced. DRAM has a word line decoder (WL decoder) circuit that requires a large area. If DRAM keeps performing operations on the same address for a long period of time, sequential circuits need to be added to the DRAM in order to ensure that the path function of the WL decoder circuit does not degrade or to reduce the degradation rate of its path function, thus increasing the area of the device. For example, the length or width of the device may be increased, or an auxiliary cascade transistor may be added to limit the drain-source voltage (V_{ds}) of the metal-oxide-semiconductor (MOS) transistor in a closed circuit, thereby increasing the chip size and costs of the design and

manufacturing processes.

SUMMARY

[0006] Embodiments of the present invention provide a semiconductor memory to address one or more of the technical limitations in the prior art.

[0007] In one aspect, an embodiment of the present invention provides a semiconductor memory. The semiconductor memory may comprise a memory array; a row address processing unit, configured to output a row address; a bank address processing unit, configured to output a bank address; a column address processing unit configured to output a column address; and a mapping factor generating unit, configured to generate a mapping factor. The output of the mapping factor generating unit may be coupled to at least one of an output of the row address processing unit, an output of the bank address processing unit, and an output of the column address processing unit. And the output of the mapping factor generating unit may further coupled to the memory array. The memory array may receive a result from logical processing performed on the mapping factor and at least one of the row address, the bank address, and the column address.

[0008] In some embodiments, the mapping factor generating unit may comprise a random number generator having an output serving as the output of the mapping factor generating unit, and configured to generate a pseudo random number sequence; and a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator generates the pseudo random number sequence. The mapping factor may comprise the pseudo random number sequence.

[0009] In some embodiments, the mapping factor generating unit may comprise a random number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read initial output data from the memory array after the semiconductor memory is powered up and output the initial output data; and a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator outputs the initial output data. The mapping factor may comprise the initial output data.

[0010] In some embodiments, the mapping factor generating unit may comprise a random

number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read random output data from the memory array and output the random output data; and a controller, coupled to the random number generator and the memory array, and configured to control a timing sequence according to which the random number generator outputs the random output data, and configured to turn off a word line of the semiconductor memory to allow the random number generator to read the random output data from the memory array. The mapping factor may comprise the random output data.

[0011] In some embodiments, the mapping factor generating unit may comprise a first random number generator, configured to generate a pseudo random number sequence; a second random number generator having an input coupled to the memory array, and configured to read initial output data from the memory array after the semiconductor memory is powered up and output the initial output data; a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the initial output data and output mixed data; and a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator outputs the initial output data, and control a timing sequence according to which the third random number generator outputs the mixed data. The mapping factor may comprise the mixed data.

[0012] In some embodiments, the mapping factor generating unit may comprise a first random number generator, configured to generate a pseudo random number sequence; a second random number generator having an input coupled to the memory array, and configured to read random output data from the memory array and output the random output data; a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and

the random output data and output mixed data; a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator outputs the random output data, turn off a word line of the semiconductor memory to allow the second random number generator to read the random output data from the memory array, and control a timing sequence according to which the third random number generator outputs the mixed data. The mapping factor may comprise the mixed data.

[0013] In some embodiments, the controller may comprise a disabling module, coupled to the first random number generator and the second random number generator, and configured to disable the first random number generator or the second random number generator.

[0014] In some embodiments, the controller may comprise a setting module, coupled to the third random number generator, and configured to set the output from the third random number generator as plain code. The mapping factor may comprise the plain code.

[0015] In some embodiments, the mapping factor may comprise a multi-bit mapping factor, and the mapping factor generating unit may be configured to randomly transmit a plurality of bits of the multi-bit mapping factor to at least one of the output of the row address processing unit, the output of the bank address processing unit, and the output of the column address processing unit.

[0016] In some embodiments, the logic processing may be an encryption processing configured to encrypt the memory array in accordance with at least one of the output of the row address processing unit, the output of the bank address processing unit, and the output of the column address processing unit.

[0017] In some embodiments, the memory array may be not encrypted during a testing mode.

[0018] In another aspect, an embodiment of the present invention provides a semiconductor memory. The semiconductor memory may comprise a memory array; an input data processing unit, configured to transmit input data to the memory array; an output data processing unit, configured to read output data from the memory array; and a mapping factor generating unit, configured to generate a mapping factor. The output of the mapping factor generating unit may

be coupled to an output of the input data processing unit and an input of the output data processing unit, and the output of the mapping factor generating unit may be further coupled to the memory array. The memory array may write a first result from logical processing performed on the mapping factor and the input data. And the output data may comprise a second result from reverse logical processing performed on the first result and the mapping factor.

[0019] In some embodiments, the mapping factor generating unit may comprises a random number generator, having an output serving as the output of the mapping factor generating unit, and configured to generate a pseudo random number sequence; and a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator generates the pseudo random number sequence. The mapping factor may comprise the pseudo random number sequence.

[0020] In some embodiments, the mapping factor generating unit comprises a random number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read initial output data from the memory array after the semiconductor memory is powered up and output the initial output data; and a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator outputs the initial output data. The mapping factor may comprise the initial output data.

[0021] In some embodiments, the mapping factor generating unit may comprise a random number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read random output data from the memory array and output the random output data; and a controller, coupled to the random number generator and the memory array, configured to control a timing sequence according to which the random number generator outputs the random output data, and turn off a word line of the semiconductor memory to allow the random number generator to read the random output data from the memory array. The mapping factor may comprise the random output data.

[0022] In some embodiments, the mapping factor generating unit may comprises a first random number generator, configured to generate a pseudo random number sequence; a second random number generator having an input coupled to the memory array, and configured to read initial output data from the memory array after the semiconductor memory is powered up and

output the initial output data; a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the initial output data, and output mixed data; and a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator generates the initial output data, and control a timing sequence according to which the third random number generator generates the mixed data. The mapping factor may comprise the mixed data.

[0023] In some embodiments, the mapping factor generating unit may comprise a first random number generator, configured to generate a pseudo random number sequence; a second random number generator having an input coupled to the memory array, and configured to read random output data from the memory array and output the random output data; a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the random output data, and output mixed data; and a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator outputs the random output data, turn off a word line of the semiconductor memory to allow the second random number generator to read the random output data from the memory array, and control a timing sequence according to which the third random number generator outputs the mixed data. The mapping factor may comprise the mixed data.

[0024] In some embodiments, the logic processing may be an encryption processing configured to encrypt the memory array in accordance with at least one of the output of the row address processing unit, the output of the bank address processing unit, and the output of

the column address processing unit.

[0025] In some embodiments, the memory array may be not encrypted during a testing mode.

[0026] The embodiments of the present invention adopt the above technical solutions, and can improve the security of the memory by encrypting the column address, the row address, the bank address or the input/output data, and can further improve the service life and reliability of the memory by using the random mapping factor for encryption.

[0027] The above summary is exemplary and explanatory only and is not restrictive of this present invention in any way. In addition to the illustrative aspects, embodiments and features described above, further aspects, embodiments and features of the present invention will be readily apparent by reference to the appended drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Unless otherwise specified, the same reference numbers used throughout the drawings refer to the same or similar parts/elements. The drawings are not necessarily drawn to scale. It should be understood that these drawings present only some embodiments of the present invention, and shall not be construed as a limitation to the scope of the present invention.

[0029] FIG. 1 is a schematic diagram illustrating a circuit of a semiconductor memory in accordance with Embodiment 1 of the present invention.

[0030] Fig. 2 is a schematic diagram illustrating a circuit of a mapping factor generating unit of a semiconductor memory in accordance with Embodiment 1 of the present invention.

[0031] Fig. 3 is a schematic diagram illustrating a circuit of a mapping factor generating unit of a semiconductor memory in accordance with Embodiment 2 of the present invention.

[0032] Fig. 4 is a schematic diagram illustrating a circuit of a mapping factor generating unit of a semiconductor memory in accordance with Embodiment 3 of the present invention.

[0033] Fig. 5 is a schematic diagram illustrating a circuit of a controller of a semiconductor memory in accordance with Embodiment 3 of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0034] The principles and spirit of the present invention will now be described below with

reference to some exemplary embodiments. It is to be understood that these embodiments are presented only to enable those skilled in the art to better understand and implement the present invention, and shall not be construed to limit the present invention in any way. Rather, these embodiments are presented to provide a full and thorough understanding of the present invention, and to fully convey the concepts of the present invention to those skilled in the art.

[0035] In the present invention, the number of any element in the figures is used for the purpose of exemplary illustration rather than a limitation, and any naming is used only for the purpose of distinguishing rather than a limitation.

[0036] Embodiment 1

[0037] FIG. 1 is a schematic diagram illustrating a circuit of a semiconductor memory in accordance with this embodiment of the present invention. Referring to FIG. 1, the semiconductor memory in this embodiment may include a memory array 10, a row address processing unit 21, a bank address processing unit 22, a column address processing unit 23, an input data processing unit 24, an output data processing unit 25, and a mapping factor generating unit 100.

[0038] The memory array 10 may include a plurality of banks, such as bank[0:7]. Each bank may include a plurality of memory cells arranged in an array. Further, each of the memory cells can have a row address, a column address, and a bank address, such that the semiconductor memory can input (write) data to be stored to the memory cell and output (read) the stored data from the memory cell.

[0039] The row address processing unit 21, the bank address processing unit 22, and the column address processing unit 23 may be configured to obtain a row address, a bank address, and a column address (addressing), respectively, based on an address input signal. Further, the semiconductor memory of this embodiment may further include a second input buffer 33 configured to receive and buffer the address input signal, and output the buffered address input signal to the row address processing unit 21, the bank address processing unit 22, and the column address processing unit 23.

[0040] The specific configurations of the second input buffer 33, the row address processing unit 21, the bank address processing unit 22, and the column address processing unit 23 may be adopted from various technical solutions known to those skilled in the art, which will not

described in detail herein.

[0041] The input data processing unit 24 may be configured to transmit input data. Specifically, the input data processing unit 24 may be configured to buffer and perform a serial-to-parallel conversion to the data input thereto and then transmit the data to the memory array 10. The output data processing unit 25 may be configured to transmit output data. Specifically, the output data processing unit 25 may be configured to retrieve data from the memory array 10, and to buffer and perform a parallel-to-serial conversion to the data retrieved, and then output the data. Further, the semiconductor memory of this embodiment may further include an input/output unit 34 configured to receive and transmit data input and output signals.

[0042] The specific configurations of the input data processing unit 24, the output data processing unit 25, and the input/output unit 34 may be adopted from various technical solutions known to those skilled in the art, which will not be described in detail herein.

[0043] The mapping factor generating unit 100 may be configured to generate and output a mapping factor (MF) MF0.

[0044] The output of the mapping factor generating unit 100 may be coupled to one or more of the output of the row address processing unit 21, the output of the bank address processing unit 22, the output of the column address processing unit 23, the output of the input data processing unit 24, and the input of the output data processing unit 25.

[0045] The input data of the input data processing unit 24 may correspond to the output data of the output data processing unit 25. Therefore, when the output of the mapping factor generating unit 100 is coupled to the output of the input data processing unit 24, the output of the mapping factor generating unit 100 should also be coupled to the input of the output data processing unit 25, vice versa.

[0046] When the output of the mapping factor generating unit 100 is coupled to the output of the row address processing unit 21, the result from logical processing performed on the mapping factor MF0 and the row address may be transmitted to the memory array 10 to select corresponding memory cells.

[0047] When the output of the mapping factor generating unit 100 is coupled to the output of the bank address processing unit 22, the result from logical processing performed on the mapping factor MF0 and the bank address may be transmitted to the memory array 10 to select

corresponding memory cells.

[0048] When the output of the mapping factor generating unit 100 is coupled to the output of the column address processing unit 23, the result from logical processing performed on the mapping factor MF0 and the column address may be transmitted to the memory array 10 to select corresponding memory cells.

[0049] When the output of the mapping factor generating unit 100 is coupled to the output of the input data processing unit 24 and the input of the output data processing unit 25, first logical processing may be performed on the mapping factor MF0 and the input data transmitted by the input data processing unit 24 to acquire a first result. The first result may be stored as the final input data into the selected memory cell. When the output data processing unit 25 reads the stored data (i.e., the first result) from the memory array 10, second logical processing may be performed on the first result and the mapping factor MF0 to acquire a second result, and the second result may serve as the output data. The first logic processing and the second logic processing may be mutual reverse processing. The first logic processing and the second logic processing may be the same or different encryption processing, and configured to encrypt the corresponding memory array, or portion thereof, so that the each storage unit of the semiconductor memory, such as a memory array, a bank, portion of the memory array having particular row addresses or column addresses can be independently encrypted using the mapping factor MF0, or portion thereof. Alternatively, the first logic processing may be an encryption processing, and the second logic processing may be a decryption processing that can be used decrypt the data encrypted by the first logic processing.

[0050] The semiconductor memory in this embodiment may further include a register configured to store the first logic and the mapping factor MF0. When the read operation is performed, the first logic and the mapping factor MF0 may be called from the register, then the second logical processing which is reverse to the first logic may be performed on the first result and the mapping factor MF0. The register may be arranged in the mapping factor generating unit 100, or may be arranged in other structures of the semiconductor memory, which is not limited in this embodiment.

[0051] In this embodiment, the mapping factor MF0 for logical processing with the row address, the mapping factor MF0 for logical processing with the bank address, the mapping

factor MF0 for logical processing with the column address, and the mapping factor MF0 for logical processing with the input data may be the same, or may be different.

[0052] The mapping factor MF0 output by the mapping factor generating unit 100 may be a multi-bit mapping factor. The mapping factor generating unit 100 may randomly allocate a mapping factor MF0 of a corresponding number of bits to the row address processing unit 21, the bank address processing unit 22, the column address processing unit 23, the input data processing unit 24, or the output data processing unit 25, based on their requirements to data regarding the number of bits.

[0053] It should be noted that, the mapping factor MF0 in this embodiment may be derived from a same mapping factor generating unit 100. However, this is not a limitation to the generating form of the mapping factor MF0. For example, the mapping factor MF0 for the row address, the mapping factor MF0 for the bank address, the mapping factor MF0 for the column address, and the mapping factor MF0 for the input data may be derived from different mapping factor generators, respectively, and may be controlled separately by different control units.

[0054] The mapping factor MF0 may be randomly generated. For example, referring to FIG. 2, the mapping factor generating circuit 100 of the present embodiment may include a first random number generator 110 and a controller 120.

[0055] The output of the first random number generator 110 may form the output of the mapping factor generating unit 100, that is, the mapping factor MF0 may be generated by the first random number generator 110. The first random number generator 110 may be configured to generate a set of pseudo random number sequences, such that the mapping factor MF0 may be a pseudo random number sequence. The controller 120 may be coupled to the first random number generator 110, and configured to control the timing sequence according to which the first random number generator 110 generates the pseudo random number sequence (i.e., the MF0), to the extent that the timing sequence of the mapping factor MF0 and the timing sequence of the row address (or bank address or column address or input/output data) are consistent.

[0056] Other configurations of the semiconductor memory, such as the first input buffer 31, the second input buffer 33, the clock control unit 32, and the instruction decode control unit 26 shown in FIG. 1, may be adopted from various technical solutions known to those skilled in

the art, which will not be described in detail herein.

[0057] Embodiment 2

[0058] The difference between this embodiment and Embodiment 1 is that the mapping factor MF0 is output by the mapping factor generating unit 200. Referring to FIG. 3, the mapping factor generating unit 200 in this embodiment may include a second random number generator 210 and a controller 220.

[0059] The input of the second random number generator 210 may be coupled to the memory array 10, and the output of the second random number generator 210 may serve as the output of the mapping factor generating unit 200, that is, the mapping factor MF0 may be generated by the second random number generator 210. The controller 220 may be coupled to the second random number generator 210.

[0060] Example 1: The second random number generator 210 may be configured to read initial output data from the memory array 10 after the semiconductor memory is powered up and output the initial output data, such that the mapping factor MF0 may be the initial output data after the semiconductor memory is powered up. Since no writing operation has been performed on the semiconductor memory, the data stored in the memory array remains random and unknown. Therefore, the initial output data read may also be unknown, and the mapping factor MF0 may be ensured to be random. The controller 220 may be configured to control the timing sequence according to which the second random number generator 210 generates the initial output data (i.e., the MF0), to the extent that the timing sequence of the mapping factor MF0 and the timing sequence of the row address (or bank address or column address or input/output data) are consistent. The controller 220 may also be coupled to the memory array 10 to control the read operation on the memory array 10 after the semiconductor memory is powered up.

[0061] Example 2: The second random number generator 210 may be configured to read random output data from the memory array 10 and output the random output data, such that the mapping factor MF0 may be the random output data of the semiconductor memory. The controller 220 may be configured to control the timing sequence according to which the second random number generator 210 generates the random output data (i.e., the MF0), such that the timing sequence of the mapping factor MF0 and the timing sequence of the row address (or

bank address or column address or input/output data) are consistent. The controller 220 may also be coupled to the memory array 10, and configured to turn off the word line of the semiconductor memory to allow the sense amplifier of the semiconductor memory to randomly amplify data. And the amplified data may serve as the random output data.

[0062] It should be noted that the above two examples may be used in combination for generating the mapping factor MF0. For example, the data obtained by randomly mixing the mapping factor generated in example 1 and the mapping factor generated in example 2 may serve as the mapping factor MF0.

[0063] Embodiment 3

[0064] The difference between this embodiment and Embodiment 1 and Embodiment 2 is that the mapping factor MF0 is output by the mapping factor generating unit 300. Referring to FIG. 4, the mapping factor generating unit 300 in this embodiment may include a first random number generator 110, a second random number generator 210, a third random number generator 330, and a controller 320.

[0065] The pseudo random number sequence output by the first random number generator 110 may serve as the mapping factor MF1, the initial output data or the random output data output by the second random number generator 210 may serve as the mapping factor MF2. An input of the third random number generator 330 may be coupled to the output of the first random number generator 110 and the output of the second random number generator 210, and may be configured to randomly mix the pseudo random number sequence and the random output data (or initial output data), and output the mixed data. The output of the third random number generator 330 may serve as the output of the mapping factor generating unit 300, such that the mapping factor MF0 may be the mixed data.

[0066] The third random number generator 330 may be a latch for latching and outputting the mixed data.

[0067] The controller 320 may be coupled to the first random number generator 110, the second random number generator 210, the third random number generator 330, and the memory array 10. In addition to having the functions of the controller 120 and the controller 220, the controller 320 may also be configured to control the timing sequence according to which the third random number generator 330 outputs the mixed data.

[0068] Referring to FIG. 5, the controller 320 may include a disabling module 321. The disabling module 321 may be coupled to the first random number generator 110 and the second random number generator 210, and configured to disable the first random number generator 110 or the second random number generator 210 such that either the pseudo random number sequence or the initial output data (or random output data) may be selected to serve as the mapping factor MF0. When the semiconductor memory is under testing, the disabling module 321 may be activated to disable the first random number generator 110, the second random number generator 210, first logic processing, and/or the second logic processing so that the semiconductor memory is not encrypted.

[0069] Referring to FIG. 5, the controller 320 may include a setting module 322. The setting module 322 may be coupled to the third random number generator 330, and configured to set the output from the third random number generator 330 as plain code (i.e., the data content of the mapping factor is known), such that the mapping factor MF0 may be plain code. For example, in the test phase of the semiconductor memory, the MF0 may be forced to be set as “0,” to the extent that the addresses (including the row address, bank address, and column address) may not be randomly distributed in the semiconductor memory, so as to perform specific tests or defect location to a designated address.

[0070] In conclusion, the security of the semiconductor memory according to the embodiments of the present invention can be improved by using the mapping factors to randomly process the column address, the row address, the bank address, or the input/output data. In addition, this random processing can ensure a balanced use of each of the addresses, and reduce the number of accesses to any particular address, thereby prolonging the service life and improving reliability of the semiconductor memory. In other words, the standard deviation of the use of the each of the addresses is small, such as no more than 10% of the average use (mean) of the addresses. Moreover, the degradation rate of the path functionality of the WL decoder circuit can be reduced without increasing the sizes of the timing circuit and the device, thereby reducing the cost of the design and manufacturing processes.

[0071] In the description of the present invention, it is to be understood that the terms “first” and “second” are used for descriptive purpose only, and shall not be construed as indicating or implying a relative importance or implicitly indicating the number of technical features

indicated. Thus, features defining “first” and “second” may include one or more of the features either explicitly or implicitly. In the description of the present invention, the meaning of “a plurality” is two or more unless specifically defined otherwise.

[0072] In the present invention, the terms “installation,” “coupled,” “connected,” “fixed,” and the like, shall be understood in a broad sense. For example, it may comprise either a fixed connection or a detachable connection; or a mechanical connection, an electrical connection, or a communication connection; or a direct connection, or an indirect connection through an intermediate medium; or an internal connection of two components or an interaction of two components. The specific meanings of the above terms in the present invention can be understood by those skilled in the art on a case-by-case basis.

[0073] In addition, although the spirit and the principles of the present invention have been described with reference to a number of specific embodiments, it is to be understood that the present invention is not limited to the specific embodiments disclosed. The division of the parts of the present invention does not mean that the features included in these parts cannot be combined. Such division is only for the convenience of expression. The present invention is intended to cover various modifications and equivalent arrangements without departing from the spirit and the principles of the present invention.

CLAIMS

1. A semiconductor memory, comprising:
 - a memory array;
 - a row address processing unit, configured to output a row address;
 - a bank address processing unit, configured to output a bank address;
 - a column address processing unit, configured to output a column address; and
 - a mapping factor generating unit, configured to generate a mapping factor, wherein an output of the mapping factor generating unit is coupled to at least one of an output of the row address processing unit, an output of the bank address processing unit, and an output of the column address processing unit, and the output of the mapping factor generating unit is further coupled to the memory array, and

wherein the memory array receives a result from logical processing performed on the mapping factor and at least one of the row address, the bank address, and the column address.
2. The semiconductor memory of claim 1, wherein the mapping factor generating unit is configured so that a standard deviation of a usage rate of at least one of the row address, the bank address and the column address is no more than 10% of an average usage rate of the at least one of the row address, the bank address and the column address.
3. The semiconductor memory of claim 1, wherein the mapping factor generating unit comprises:
 - a random number generator having an output serving as the output of the mapping factor generating unit, and configured to generate a pseudo random number sequence, wherein the mapping factor comprises the pseudo random number sequence; and
 - a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator generates the pseudo random

number sequence.

4. The semiconductor memory of claim 1, wherein the mapping factor generating unit comprises:

a random number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read initial output data from the memory array after the semiconductor memory is powered up and output the initial output data; wherein the mapping factor comprises the initial output data; and

a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator outputs the initial output data.

5. The semiconductor memory of claim 1, wherein the mapping factor generating unit comprises:

a random number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read random output data from the memory array and output the random output data; wherein the mapping factor comprises the random output data; and

a controller, coupled to the random number generator and the memory array, and configured to control a timing sequence according to which the random number generator outputs the random output data, and configured to turn off a word line of the semiconductor memory to allow the random number generator to read the random output data from the memory array.

6. The semiconductor memory of claim 1, wherein the mapping factor generating unit comprises:

a first random number generator, configured to generate a pseudo random number sequence;

a second random number generator having an input coupled to the memory array, and configured to read initial output data from the memory array after the semiconductor memory is powered up and output the initial output data;

a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the initial output data and output mixed data; wherein the mapping factor comprises the mixed data; and

a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator outputs the initial output data, and control a timing sequence according to which the third random number generator outputs the mixed data.

7. The semiconductor memory of claim 1, wherein the mapping factor generating unit comprises:

a first random number generator, configured to generate a pseudo random number sequence;

a second random number generator having an input coupled to the memory array, and configured to read random output data from the memory array and output the random output data;

a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the random output data and output mixed data; wherein the mapping factor comprises the mixed data; and

a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator outputs the random output data, turn off a word line of the semiconductor memory to allow the second random number generator to read the random output data from the memory array, and

control a timing sequence according to which the third random number generator outputs the mixed data.

8. The semiconductor memory of claim 6, wherein the controller comprises a disabling module, coupled to the first random number generator and the second random number generator, and configured to disable the first random number generator or the second random number generator.

9. The semiconductor memory of claim 7, wherein the memory array is configured to be not encrypted during a testing mode.

10. The semiconductor memory of claim 6, wherein the controller comprises a setting module, coupled to the third random number generator, and configured to set an output from the third random number generator as plain code; wherein the mapping factor comprises the plain code.

11. The semiconductor memory of claim 1, wherein the mapping factor comprises a multi-bit mapping factor, and the mapping factor generating unit is configured to randomly transmit a plurality of bits of the multi-bit mapping factor to at least one of the output of the row address processing unit, the output of the bank address processing unit, and the output of the column address processing unit.

12. The semiconductor memory of claim 1, wherein the logic processing is an encryption processing configured to encrypt data in accordance with at least one of the output of the row address processing unit, the output of the bank address processing unit, and the output of the column address processing unit.

13. A semiconductor memory, comprising:

a memory array;

an input data processing unit, configured to transmit input data to the memory array;

an output data processing unit, configured to read output data from the memory array; and

a mapping factor generating unit, configured to generate a mapping factor,

wherein an output of the mapping factor generating unit is coupled to an output of the

input data processing unit and an input of the output data processing unit, and the output of the mapping factor generating unit is further coupled to the memory array, and

wherein the memory array writes a first result from logical processing performed on the mapping factor and the input data; the output data comprises a second result from reverse logical processing performed on the first result and the mapping factor.

14. The semiconductor memory of claim 12, wherein the mapping factor generating unit is configured so that a standard deviation of a usage rate of at least one of the row address, the bank address and the column address is no more than 10% of an average usage rate of the at least one of the row address, the bank address and the column address.

15. The semiconductor memory of claim 13, wherein the mapping factor generating unit comprises:

a random number generator, having an output serving as the output of the mapping factor generating unit, and configured to generate a pseudo random number sequence; wherein the mapping factor comprises the pseudo random number sequence; and

a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator generates the pseudo random number sequence.

16. The semiconductor memory of claim 13, wherein the mapping factor generating unit comprises:

a random number generator, having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read initial output data from the memory array after the semiconductor memory is powered up and output the initial output data; wherein the mapping factor comprises the initial output data; and

a controller, coupled to the random number generator, and configured to control a timing sequence according to which the random number generator outputs the initial output data.

17. The semiconductor memory of claim 13, wherein the mapping factor generating unit comprises:

a random number generator having an input coupled to the memory array and an output serving as the output of the mapping factor generating unit, and configured to read random output data from the memory array, and output the random output data; wherein the mapping factor comprises the random output data; and

a controller, coupled to the random number generator and the memory array, configured to control a timing sequence according to which the random number generator outputs the random output data, and turn off a word line of the semiconductor memory to allow the random number generator to read the random output data from the memory array.

18. The semiconductor memory of claim 13, wherein the mapping factor generating unit comprises:

a first random number generator, configured to generate a pseudo random number sequence;

a second random number generator having an input coupled to the memory array, and configured to read an initial output data from the memory array after the semiconductor memory is powered up and output the initial output data;

a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the initial output data, and output mixed data; wherein the mapping factor comprises the mixed data; and

a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator generates the initial output data, and control a timing sequence according to which the third random number generator generates the mixed data.

19. The semiconductor memory of claim 13, wherein the mapping factor generating unit comprises:

a first random number generator, configured to generate a pseudo random number sequence;

a second random number generator having an input coupled to the memory array, and configured to read random output data from the memory array and output the random output data;

a third random number generator having an output serving as the output of the mapping factor generating unit, coupled to an output of the first random number generator and an output of the second random number generator, and configured to randomly mix the pseudo random number sequence and the random output data, and output mixed data; wherein the mapping factor comprises the mixed data; and

a controller, coupled to the first random number generator, the second random number generator, and the third random number generator, and configured to control a timing sequence according to which the first random number generator generates the pseudo random number sequence, control a timing sequence according to which the second random number generator outputs the random output data, turn off a word line of the semiconductor memory to allow the second random number generator to read the random output data from the memory array, and control a timing sequence according to which the third random number generator outputs the mixed data.

20. The semiconductor memory of claim 13, wherein the logic processing is an encryption processing configured to encrypt the memory array in accordance with at least one of the output of the row address processing unit, the output of the bank address processing unit, and the output of the column address processing unit.

21. The semiconductor memory of claim 20, wherein the memory array is configured to be not encrypted during a testing mode.

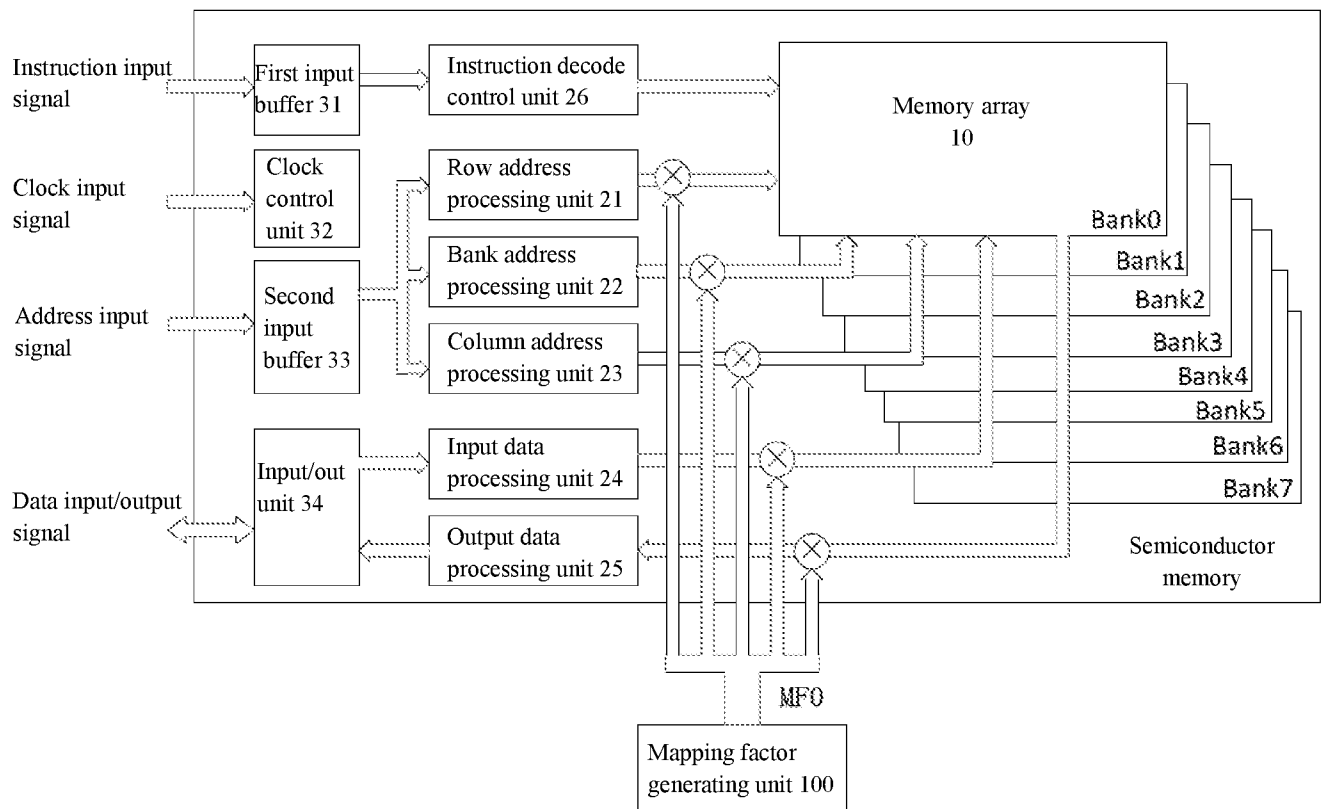


FIG. 1

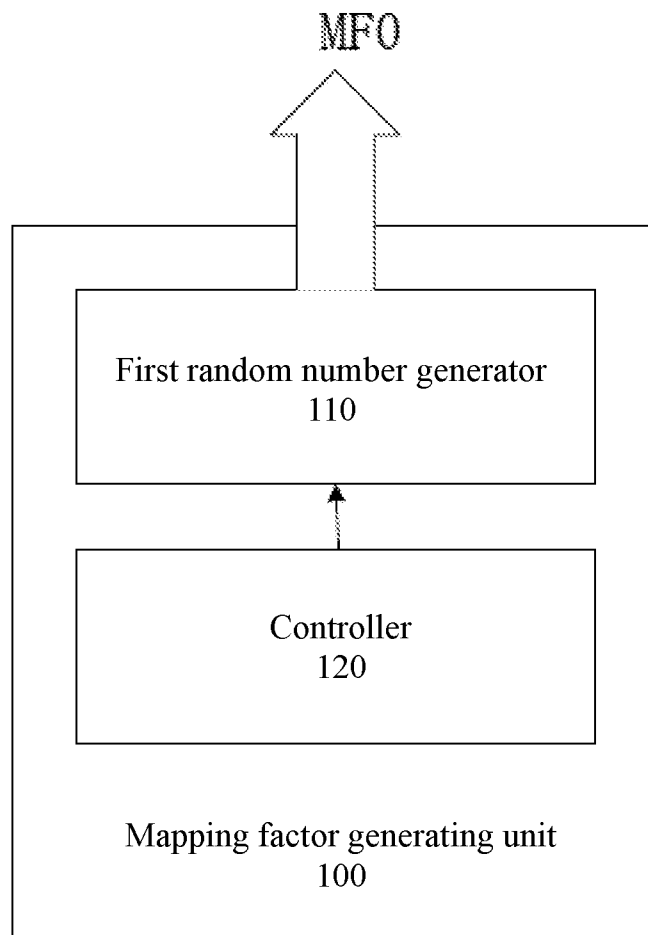


FIG. 2

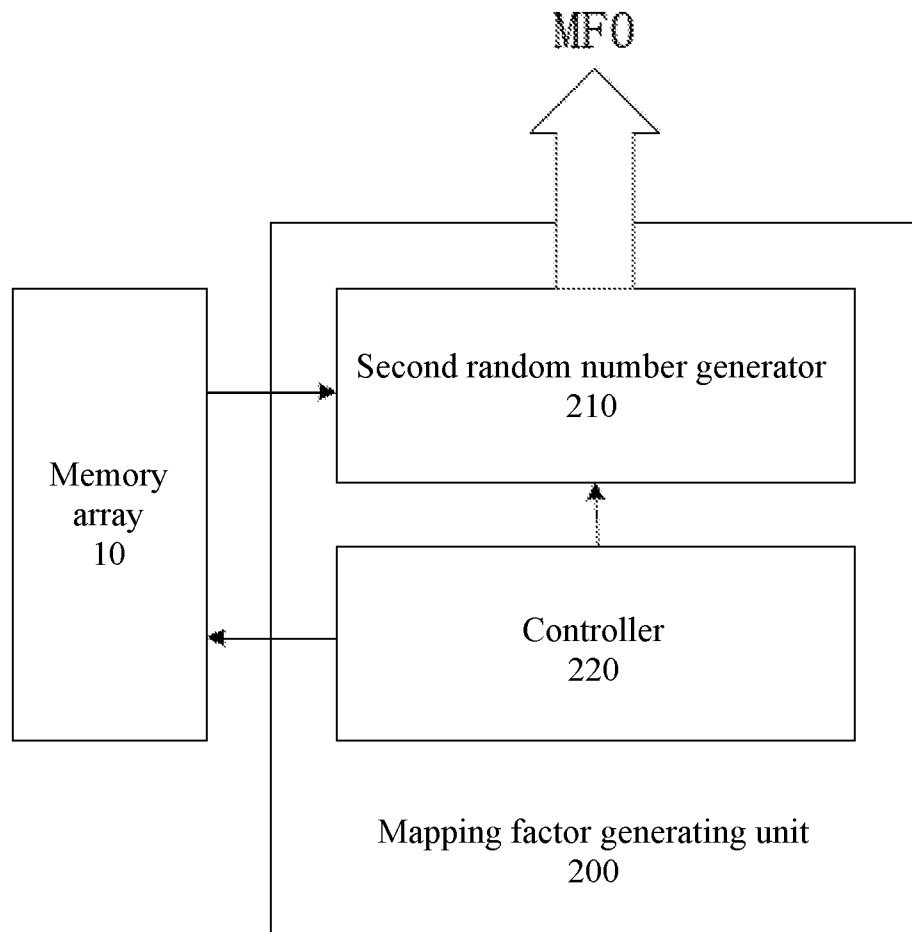


FIG. 3

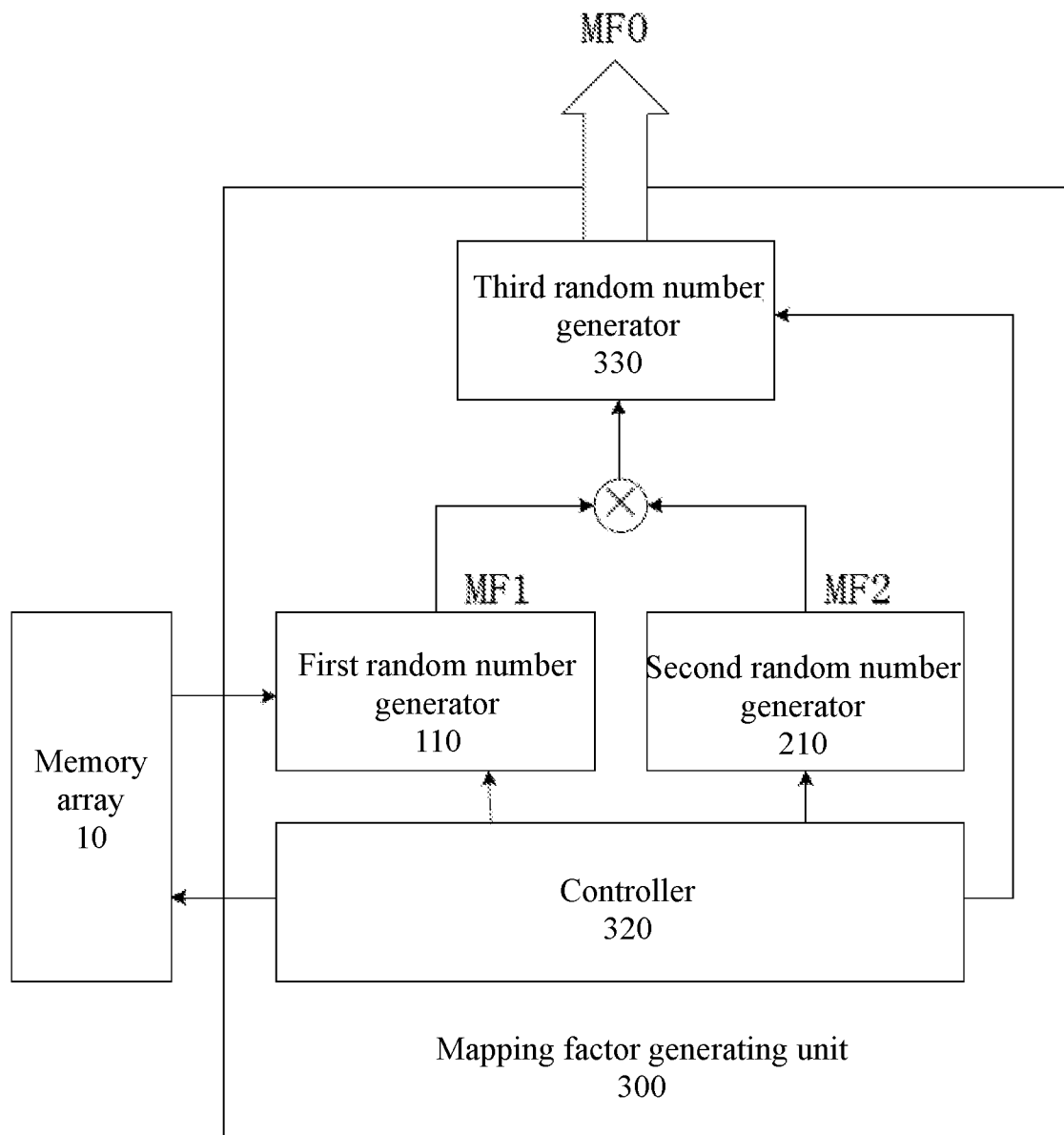


FIG. 4

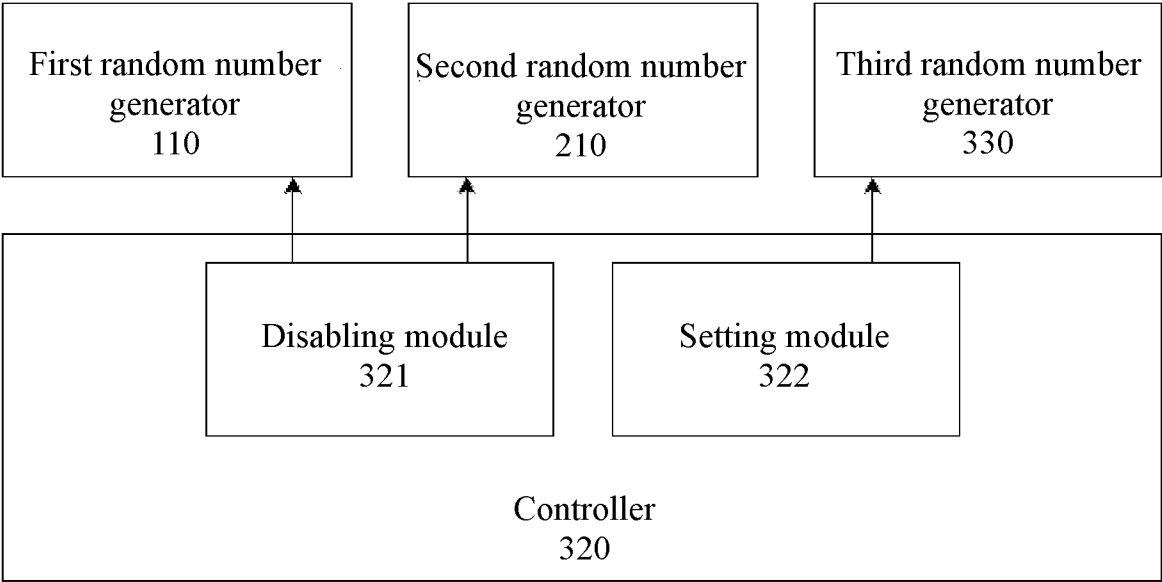


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/116061

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/4063(2006.01)i; G06F 7/58(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C.; G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,WPI,IEEE:row address, block address, map, address, column address, safety, mapping factor, random number, memory

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 208922741 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 31 May 2019 (2019-05-31) description, paragraphs [0071]-[0104] and figures 1-5	1-21
X	CN 105679365 A (INST. MICROELECTRONICS CHINESE ACAD. SCI.) 15 June 2016 (2016-06-15) description, paragraphs [0005]-[0029] and figures 1-7	13-17
Y	CN 105679365 A (INST. MICROELECTRONICS CHINESE ACAD. SCI.) 15 June 2016 (2016-06-15) description, paragraphs [0005]-[0029] and figures 1-7	1-5, 11-12, 20-21
Y	CN 101556561 A (SHENGQUN SEMI-CONDUCTOR CO., LTD.) 14 October 2009 (2009-10-14) description, page 8, line 9-page 9, line 14	1-5, 11-12, 20-21
A	CN 102568575 A (SAMSUNG ELECTRONICS CO., LTD.) 11 July 2012 (2012-07-11) the whole document	1-21
A	CN 101533671 A (HYNIX SEMICONDUCTOR INC.) 16 September 2009 (2009-09-16) the whole document	1-21



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

15 January 2020

Date of mailing of the international search report

03 February 2020

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088
China

Authorized officer

SHU,Qi

Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961220

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/116061

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	208922741	U	31 May 2019	None			
CN	105679365	A	15 June 2016	US	2018315484	A1	01 November 2018
				WO	2017067038	A1	27 April 2017
CN	101556561	A	14 October 2009	CN	101556561	B	06 April 2011
CN	102568575	A	11 July 2012	DE	102011056776	A8	13 September 2012
				US	8751729	B2	10 June 2014
				US	2012166714	A1	28 June 2012
				DE	102011056776	A1	28 June 2012
				JP	2012133877	A	12 July 2012
				KR	20120072289	A	03 July 2012
				TW	201232261	A	01 August 2012
CN	101533671	A	16 September 2009	KR	20090097107	A	15 September 2009
				CN	101533671	B	13 March 2013
				US	7826277	B2	02 November 2010
				US	2009225596	A1	10 September 2009
				KR	101015731	B1	22 February 2011