(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 January 2012 (12.01.2012)

PCT

(10) International Publication Number
WO 2012/004068 A1

(51) International Patent Classification:
H01L 21/60 (2006.01) *H01L 23/498* (2006.01)
B82Y 40/00 (201 1.01) *B82Y 10/00* (201 1.01)
H01L 21/58 (2006.01)

(21) International Application Number:
PCT/EP20 11/059133

(22) International Filing Date:
1 June 201 1 (01 .06.201 1)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/83 1,656 7 July 2010 (07.07.2010) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available):* AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available):* ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,

[Continued on nextpage]

(54) Title: A METHOD TO FABRICATE HIGH PERFORMANCE CARBON NANOTUBE TRANSISTOR INTEGRATED CIRCUITS BY THREE-DIMENSIONAL INTEGRATION TECHNOLOGY

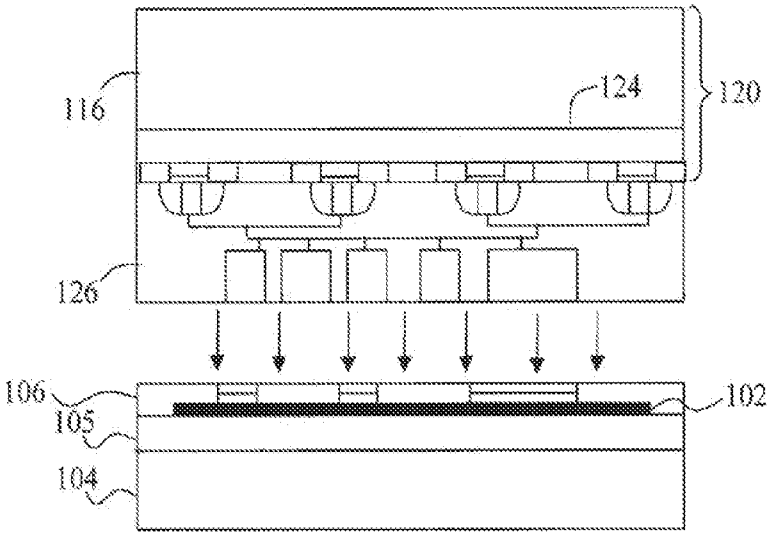

FIG. 10

(57) Abstract: Techniques for fabricating carbon nanotube-based devices are provided. In one aspect, a method for fabricating a carbon nanotube-based integrated circuit is provided. The method comprises the following steps. A first wafer comprising carbon nanotubes is provided. A second wafer comprising one or more device elements is provided. One or more of the carbon nanotubes are connected with one or more of the device elements by bonding the first wafer and the second wafer together. A carbon nanotube-based integrated circuit is also provided.

WO 2012/004068 A1

LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

A METHOD TO FABRICATE HIGH PERFORMANCE CARBON NANOTUBE TRANSISTOR INTEGRATED CIRCUITS BY THREE-DIMENSIONAL INTEGRATION TECHNOLOGY

Field of the Invention

The present invention relates to carbon nanotube technology and more particularly, to techniques for fabricating carbon nanotube-based devices.

Background of the Invention

Carbon nanotubes possess extraordinary electronic properties that are attractive for high-speed and high-performance circuits. One of the major challenges in utilizing devices and complex circuits involving carbon nanotubes lies in the incompatibility of the carbon nanotube growth conditions and the process limitation of current complementary metal-oxide-semiconductor (CMOS) technology. For example, chemical vapor deposition (CVD) grown carbon nanotubes require a growth condition of at least 600 °C for producing high quality nanotubes, which exceeds the temperature capacity of about 350 °C to about 400 °C for CMOS processes.

One possible solution to work around this temperature limitation is to deposit pre-formed carbon nanotubes on the substrate from a solution. However, during the subsequent processing, the deposited carbon nanotubes may be destroyed via oxidation and the properties of the carbon nanotubes may also be altered due to surface treatments.

Another practical challenge of realizing integrated circuits based on carbon nanotubes is the alignment of carbon nanotubes with the rest of the circuit components. While there has been much progress in controlling the growth orientation and/or the deposition location of nanotubes, their alignment with the rest of the circuits has not been addressed.

Therefore, techniques for three-dimensional carbon nanotube-based integrated circuit device integration would be desirable.

Summary of the Invention

The present invention provides techniques for fabricating carbon nanotube-based devices. In one aspect of the invention, a method for fabricating a carbon nanotube-based integrated circuit is provided. The method comprises the following steps. A first wafer comprising carbon nanotubes is provided. A second wafer comprising one or more device elements is provided. One or more of the carbon nanotubes are connected with one or more of the device elements by bonding the first wafer and the second wafer together.

The carbon nanotubes can be deposited on a first substrate. A first oxide layer can be deposited onto the substrate covering the carbon nanotubes. One or more first electrodes can be formed that extend at least part way through the first oxide layer and are in contact with one or more of the carbon nanotubes. One or more device elements can be fabricated on a second substrate. A second oxide layer can be deposited over the device elements. One or more second electrodes can be formed that extend at least part way through the second oxide layer connected to one or more of the device elements.

In another aspect of the invention, a carbon nanotube-based integrated circuit is provided. The carbon nanotube-based integrated circuit includes a first wafer comprising carbon nanotubes; and a second wafer comprising one or more device elements, wherein the first wafer is bonded to the second wafer such that one or more of the carbon nanotubes are connected with one or more of the device elements.

A more complete understanding of the present invention, as well as further features and advantages of the present invention, will be obtained by reference to the following detailed description and drawings.

Brief Description of the Drawings

FIG. 1 is a cross-sectional diagram illustrating a carbon nanotube wafer with carbon nanotubes having been deposited onto an oxide covered substrate according to an embodiment of the present invention;

FIG. 2 is a diagram illustrating a top-down view of the carbon nanotube wafer of FIG. 1 according to an embodiment of the present invention;

FIG. 3 is a cross-sectional diagram of the carbon nanotube wafer illustrating an oxide layer having been deposited onto the oxide covered substrate covering the carbon nanotubes according to an embodiment of the present invention;

FIG. 4 is a cross-sectional diagram of the carbon nanotube wafer illustrating a mask layer having been deposited over the oxide layer and patterned according to an embodiment of the present invention;

FIG. 5 is a cross-sectional diagram of the carbon nanotube wafer illustrating the oxide layer having been etched through the patterned mask layer forming vias that expose regions of the carbon nanotubes to receive metal electrodes according to an embodiment of the present invention;

FIG. 6 is a cross-sectional diagram of the carbon nanotube wafer illustrating metal having been deposited over the oxide layer and filling the vias according to an embodiment of the present invention;

FIG. 7 is a cross-sectional diagram of the carbon nanotube wafer illustrating the metal having been polished down to a desired thickness according to an embodiment of the present invention;

FIG. 8 is a cross-sectional diagram illustrating a device wafer with one or more device elements fabricated on a silicon-on-insulator (SOI) substrate according to an embodiment of the present invention;

FIG. 9 is a cross-sectional diagram of the device wafer illustrating an oxide layer having been deposited over the device elements, one or more metal layers having been formed in the oxide layer in contact with device elements and one or more electrodes having been

formed in the oxide layer in contact with the metal layers according to an embodiment of the present invention;

FIG. 10 is a cross-sectional diagram illustrating the device wafer having been flipped for face-to-face bonding with the carbon nanotube wafer according to an embodiment of the present invention;

FIG. 11 is a cross-sectional diagram illustrating a resulting device layout after the device wafer and the carbon nanotube wafer have been bonded together according to an embodiment of the present invention;

FIG. 12 is a cross-sectional diagram illustrating a majority of the substrate having been removed from the device wafer according to an embodiment of the present invention;

FIG. 13 is a cross-sectional diagram illustrating the substrate having been removed from the carbon nanotube wafer according to an embodiment of the present invention;

FIG. 14 is a cross-sectional diagram illustrating additional device layers/metal layers having been formed adjacent to the device wafer according to an embodiment of the present invention; and

FIG. 15 is a cross-sectional diagram illustrating additional device layers/metal layers having been formed adjacent to the carbon nanotube wafer according to an embodiment of the present invention.

Detailed Description of Preferred Embodiments

In order to successfully use carbon nanotubes as active elements in a practical device and/or circuit, a new fabrication scheme is required to combine existing complementary metal-oxide-semiconductor (CMOS) technology and the carbon nanotubes. The present teachings provide such a fabrication scheme.

FIGS. 1-15 are diagrams illustrating an exemplary methodology for fabricating a carbon nanotube-based integrated circuit. In this particular example, carbon nanotube-based transistors are formed by providing carbon nanotubes fabricated on one substrate (referred to herein as a carbon nanotube wafer) and CMOS device elements (and associated wiring) on another substrate (referred to herein as a device wafer), then connecting the carbon nanotubes with one or more of the device elements through the use of face-to-face bonding to bond the carbon nanotube wafer and the device wafer together in a three-dimensional configuration.

Three-dimensional integration has become a very promising candidate to fulfill packaging and integrated circuit (IC) technology gaps for carbon nanotube-based electronics. The ability to stack CMOS state-of-the-art active device layers has been demonstrated. Three-dimensional integration technology can increase system performance even in the absence of scaling. Specifically, three-dimensional integration offers decreased total wiring length (and thus reduced interconnect delay times), a dramatically increased number of interconnects between chips and the ability to allow dissimilar materials, process technologies and functions to be successfully integrated. In addition, it has been noted that in carbon nanotube-based circuits, system performance is drastically affected by the parasitic capacitance and the resistance of interconnects.

As shown in FIG. 1, a cross-sectional view, the carbon nanotube wafer can be formed by first depositing carbon nanotubes 102 onto an oxide covered substrate. According to an exemplary embodiment, the oxide covered substrate includes a silicon (Si) substrate 104 covered with an oxide 105. In this example, carbon nanotubes 102 are deposited onto oxide 105. These carbon nanotubes can be grown using a chemical vapor deposition (CVD) process or deposited from a solution. These CVD and solution deposition processes are well-known in the art. According to an exemplary embodiment wherein the CVD process is employed, metal catalysts (e.g., molybdenum (Mo), iron (Fe), nickel (Ni)) are first deposited on the oxide covered substrate, followed by flowing high-temperature (e.g., between about 450 degrees Celsius (°C) to about 900 °C) carbon-containing gas, such as ethanol or methane, over the substrate surface to form the carbon nanotubes.

For applications where carbon nanotubes are used as active components in the circuit, such as transistor channels, semiconducting nanotubes are needed. In practice, a mixture of semiconducting and metallic carbon nanotubes is generally attained. In this instance, carbon nanotube films with a high purity (greater than 99 percent (%)) of semiconducting nanotubes deposited from purified nanotube solutions are used. The term purity as used herein refers to a ratio between semiconducting and metallic carbon nanotubes. Methods to separate metallic from semiconducting carbon nanotubes in a solution are well-known to those of skill in the art. In one example, the buoyant density difference between metallic and semiconducting nanotubes in aqueous solutions after functionalizing with proper surfactants, such as sodium cholate, could be utilized to separate the two type of nanotubes with ultracentrifugation. Solutions containing high purity (greater than 99.9 %) of semiconducting carbon nanotubes can be prepared by this approach.

A top view (from vantage point A) of the carbon nanotube wafer is shown in FIG. 2. As shown in FIG. 2, carbon nanotubes 102 are aligned along a top surface of oxide 105 (of the oxide covered substrate). However, it is not necessary for all nanotubes to be aligned. They are drawn in parallel in FIG. 2 only for the sake of clarity.

As shown in FIG. 3, a cross-sectional diagram, oxide layer 106 is then deposited onto the oxide covered substrate covering carbon nanotubes 102. This oxide layer will serve two purposes. First, oxide layer 106 will serve as a gate dielectric for the carbon nanotubes. Second, oxide layer 106 will be used later in the fabrication process to protect the carbon nanotubes from damage by subsequent processing. Oxide layer 106 can be deposited using atomic layer deposition (ALD) or by a low-temperature (less than 300°C) CVD, or by a combination of the two deposition processes. A low-temperature oxide CVD process is preferred over high-temperature CVD processes to minimize potential adverse effects on the nanotube quality.

As shown in FIG. 4, a cross-sectional diagram, a mask layer 108 is deposited over oxide layer 106. Mask layer 108 can comprise a photoresist material, such as poly(methyl methacrylate) (PMMA) (i.e., an electron beam (e-beam) resist), or a hard mask (metal) material. Mask layer 108 is then patterned with a footprint and location of a number of vias

that will be used to define source and drain electrodes of the carbon nanotube-based transistors (see below). Processes for depositing and patterning a mask layer are known to those of skill in the art and thus are not described further herein.

As shown in FIG. 5, a cross-sectional diagram, oxide layer 106 is etched, using a wet etch process through patterned mask layer 108, forming vias 110 that expose regions of carbon nanotubes 102 to receive metal electrodes (see below). After the wet etch is completed, patterned mask layer 108 is removed, for example, using acetone.

As shown in FIG. 6, a cross-sectional diagram, metal is deposited over oxide layer 106, filling vias 110. According to an exemplary embodiment, the metal is made up of two layers. The layer which is deposited first, i.e., metal layer 112, is a thin metal layer used to enable good contact with the carbon nanotubes and comprises a metal such as palladium (Pd). Metal layer 112 has a thickness of from about 1 nanometer (nm) to about 100 nm and as shown in FIG. 6 lines a top surface of oxide layer 106/the exposed regions of carbon nanotubes 102. The second layer, i.e., metal layer 114, deposited over metal layer 112 is used to permit adhesion in a wafer bonding step (see below) and comprises copper (Cu). Metal layer 114 is deposited over metal layer 112 and fills vias 110. As shown in FIG. 6, metal layer 114 can extend above the surface of oxide layer 106. Metal layer 114 has a thickness of from about 5 nm to about 300 micrometers (μιη). By way of example only, metal layer 112 can be formed by thermal evaporation, while the metal layer 114 can be formed by electrochemical deposition so as to form a thicker metal film.

As shown in FIG. 7, a cross-sectional diagram, metal layers 112 and 114 are then polished (e.g., using chemical mechanical polishing (CMP)) to thin metal layer 114 down to a desired thickness. This polishing process will also remove any excess metal from metal layer 112 and can further thin oxide layer 106. According to an exemplary embodiment, oxide layer 106, after thinning, has a thickness of from about 5 nm to about 1 μm. The amount of oxide layer 106 that is removed is controlled by the duration of the CMP process. At this step in the process distinct transistor contact regions 115 are defined. Exemplary source and drain electrode regions are shown labeled in FIG. 7. The result is a completed carbon nanotube wafer which will be bonded using face-to-face bonding to a device wafer (see below).

The device wafer is then provided. As shown in FIG. 8, a cross-sectional diagram, the device wafer can be formed by first fabricating one or more device elements 118 on a, i.e., silicon-on-insulator (SOI) substrate 120 having a SOI layer 122 over a buried oxide (BOX) 124 and Si layer 116. According to an exemplary embodiment, each device element comprises a source region 118s connected to a drain region 118d by a channel 118c, and a gate region 118g over the channel. According to an exemplary embodiment, device elements 118 comprise silicon-based CMOS device components, such as memory and/or logic transistors. Techniques for fabricating such device elements in an SOI substrate are known to those of skill in the art and thus are not described further herein. As shown in FIG. 9, a cross-sectional diagram, an oxide layer 126 is deposited over device elements 118. Oxide layer 126 will serve as a bonding oxide layer during the wafer bonding step detailed below. One or more metal layers 128 are then formed in oxide layer 126 in contact with device elements 118.

Next, one or more electrodes 130 are formed in oxide layer 126 in contact with metal layers 128 (metal layers 128 connect device elements 118 with electrodes 130). Electrodes 130 form source/drain/gate electrodes to device elements 118 and comprise Cu. An exemplary configuration of source (S)/drain (D)/gate (G) electrodes is shown labeled in FIG. 9.

As shown in FIG. 10, a cross-sectional diagram, the device wafer is flipped for face-to-face bonding with the carbon nanotube wafer (i.e., the wafers are aligned to permit a top surface or "face" of each wafer to bond with a corresponding top surface or "face" of the other wafer). While in this example the device layer is flipped, the same processes can be carried out by flipping the carbon nanotube wafer instead. The resulting device layout after the two wafers are bonded together is shown in FIG. 11, a cross-sectional diagram. The bonding approach here is based on Cu-to-Cu (between contact regions 115 of the carbon nanotube wafer and source/drain/gate electrodes 130 of the device wafer) and oxide-to-oxide bonding (between oxide layer 106 of the carbon nanotube wafer and oxide layer 126 of the device wafer) simultaneously. The bonding temperature employed is below 400°C so as not to destroy components in the device layer during the bonding process. Cu-to-Cu bonding and oxide-to-oxide bonding processes are known to those of skill in the art and thus are not described further herein.

After the two wafers are bonded together, the next step is the substrate removal process. Since now there are two substrates from two wafers after the bonding, the choice of which substrate to remove relies on the design of circuits (i.e., to permit the fabrication of additional layers of the structure). In FIG. 12, a cross-sectional diagram, substrate 120 is thinned (i.e., Si layer 116 is removed from the device wafer). According to an exemplary embodiment, the desired substrate is removed using CMP or other similar polishing and/or grinding process. As highlighted above, substrate 120 is an SOI substrate, and as such BOX 124 is the stopping layer for the CMP process.

In FIG. 13, a cross-sectional diagram, substrate 104 is removed from the carbon nanotube wafer, leaving oxide 105. As highlighted above, the carbon nanotube wafer is based on an oxide covered Si substrate. The oxide can act as a stopping layer during the substrate removal. This type of selective etch can be achieved by using an etching process which removes silicon but not oxide.

An additional device layer(s) or a next metal layer Mn can be fabricated on the bonded wafer structure. The surface on which the fabrication takes place can depend on which substrate was removed above. Specifically, if substrate 120 has been removed (see FIG. 12 described above), then additional device layers/metal layers, represented schematically by layer 132, are formed adjacent to BOX 124. This configuration is shown in FIG. 14, a cross-sectional diagram. On the other hand, if substrate 104 has been removed (see FIG. 13 described above), then additional device layers/metal layers, represented schematically by layer 134, are formed adjacent to oxide layer 105. This configuration is shown in FIG. 15, a cross-sectional diagram. It is notable that in the configuration shown in FIG. 15, the bonded wafer structure has been flipped to permit top-down fabrication of the additional device layers/metal layers.

In conclusion, the present techniques offer a successful and easily-implemented solution to three-dimensional carbon nanotube-based IC device integration. Advantages of the present techniques include, but are not limited to, (1) carbon nanotubes can be prepared by a wide range of different approaches, including but not limited to CVD grown nanotubes, nanotubes from solution deposition, nanotube thin films, (2) complex circuits can be pre-fabricated in

standard clean-room facilities without the potential contamination from carbon nanotubes and metal catalysts, (3) the alignment in the wafer bonding process ensures the nanotubes are always incorporated at the desirable positions of the circuit, (4) the requirements of existing CMOS devices, such as temperature, wet etching environment, gas ambient during process, still can be kept since nanotubes are fabricated separately on another wafer and (5) the circuit delay time, which is dominated by interconnects in the case of carbon nanotube circuits, can be significantly reduced.

Although illustrative embodiments of the present invention have been described herein, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be made by one skilled in the art without departing from the scope of the invention.

CLAIMS

1. A method for fabricating a carbon nanotube-based integrated circuit, comprising the steps of:

providing a first wafer comprising carbon nanotubes;

providing a second wafer comprising one or more device elements; and

connecting one or more of the carbon nanotubes with one or more of the device elements by bonding the first wafer and the second wafer together.

2. The method of claim 1, further comprising the steps of:

depositing the carbon nanotubes on a first substrate;

depositing a first oxide layer onto the first substrate covering the carbon nanotubes;

forming one or more first electrodes that extend at least part way through the first oxide layer and are in contact with one or more of the carbon nanotubes.

fabricating one or more device elements on a second substrate;

depositing a second oxide layer over the device elements; and

forming one or more second electrodes that extend at least part way through the second oxide layer connected to one or more of the device elements.

3. The method of claim 2, further comprising the step of:

forming one or more metal layers in the second oxide layer in contact with the device elements.

4. The method of claim 2, wherein both the first electrodes and the second electrodes comprise copper and wherein the step of connecting the carbon nanotubes with the device elements further comprises the steps of:

forming an oxide-to-oxide bond between the first oxide layer and the second oxide layer; and

forming a copper-to-copper bond between the first electrodes and the second electrodes.

5. The method of claim 2, wherein the first substrate comprises an oxide covered substrate.

6. The method of claim 2, wherein the second substrate comprises a silicon-on-insulator substrate.

7. The method of claim 2, wherein the carbon nanotubes are deposited on the first substrate using chemical vapor deposition.

8. The method of claim 2, wherein the carbon nanotubes are deposited on the first substrate from a solution.

9. The method of claim 2, wherein the carbon nanotubes comprise a mixture of semiconducting and metallic carbon nanotubes and wherein the mixture contains greater than 99 percent semiconducting carbon nanotubes.

10. The method of claim 2, further comprising the steps of;

forming vias through the first oxide layer that expose regions of the carbon nanotubes;

depositing a first metal layer that lines the exposed regions of the carbon nanotubes; and

depositing a second metal layer over the first metal layer and filling the vias.

11. The method of claim 10, wherein the step of forming the vias through the first oxide layer further comprises the steps of:

depositing a mask layer over the first oxide layer;

patterning the mask layer with a footprint and location of each of the vias;

etching the first oxide layer through the patterned mask layer to form the vias; and

removing the mask layer.

12. The method of claim 11, wherein the step of etching the first oxide layer through the patterned mask layer to form the vias is performed using a wet etch process.

13. The method of claim 10, wherein the first metal layer comprises palladium.

14. The method of claim 10, wherein the first metal layer has a thickness of from about 1 nanometer to about 100 nanometers.

15. The method of claim 10, wherein the second metal layer comprises copper.

16. The method of claim 10, further comprising the steps of:
thinning the second metal layer.

17. The method of claim 16, wherein the second metal layer is thinned using chemical mechanical polishing.

18. The method of claim 1, further comprising the step of:
flipping one of the first wafer or the second wafer to permit face-to-face bonding between the first wafer and the second wafer.

19. The method of claim 2, further comprising the step of:
thinning one of the first substrate or the second substrate.

20. A carbon nanotube-based integrated circuit, comprising:
a first wafer comprising carbon nanotubes; and
a second wafer comprising one or more device elements, wherein the first wafer is bonded to the second wafer such that one or more of the carbon nanotubes are connected with one or more of the device elements.

21. The carbon nanotube-based integrated circuit of claim 20, wherein the first wafer comprises:
a first substrate on which the carbon nanotubes are disposed;
a first oxide layer covering the carbon nanotubes;
one or more first electrodes that extend at least part way through the first oxide layer and are in contact with one or more of the carbon nanotubes,

and wherein the second wafer comprises:

a second substrate on which the device elements are fabricated;

a second oxide layer over the device elements; and

one or more second electrodes that extend at least part way through the second oxide layer connected to one or more of the device elements.

22. The carbon nanotube-based integrated circuit of claim 21, wherein the second wafer further comprises:

one or more metal layers in the second oxide layer in contact with the device elements.

23. The carbon nanotube-based integrated circuit of claim 21, wherein both the first electrodes and the second electrodes comprise copper and wherein the carbon nanotubes are connected with one or more of the device elements by way of an oxide-to-oxide bond between the first oxide layer and the second oxide layer, and a copper-to-copper bond between the first electrodes and the second electrodes.

24. The carbon nanotube-based integrated circuit of claim 21, wherein the first substrate comprises an oxide covered substrate.

25. The carbon nanotube-based integrated circuit of claim 21, wherein the second substrate comprises a silicon-on-insulator substrate.

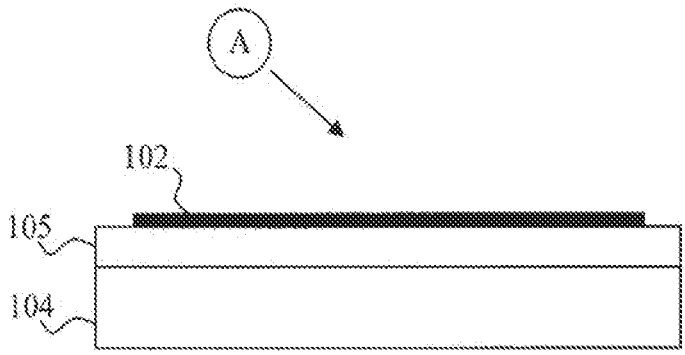

FIG. 1

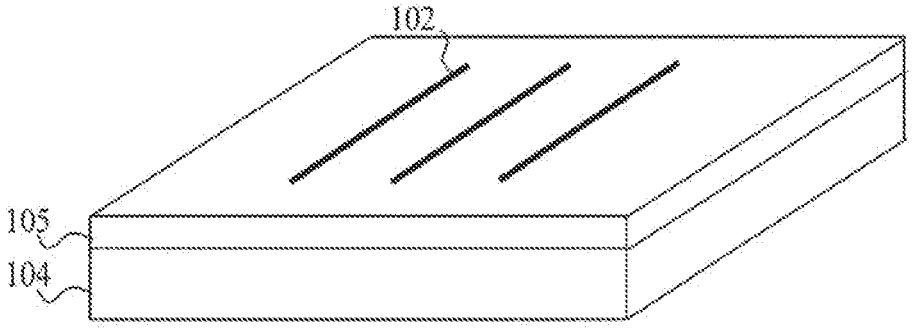

FIG. 2

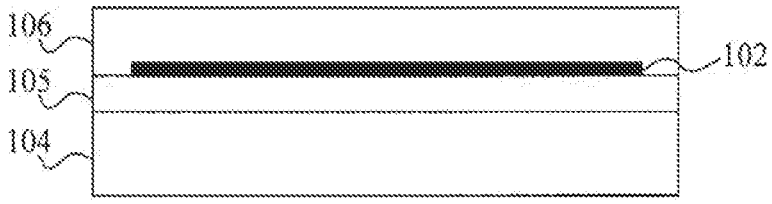

FIG. 3

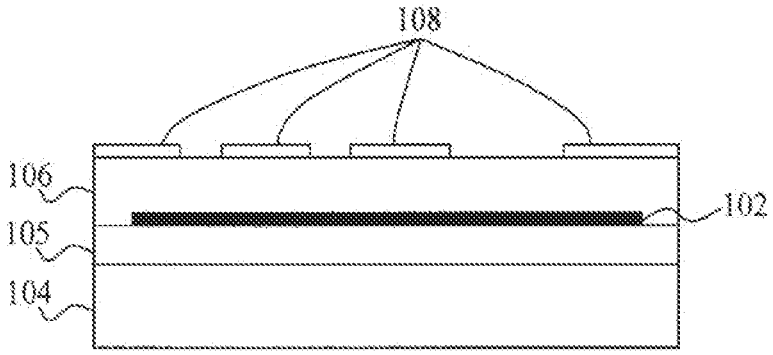

FIG. 4

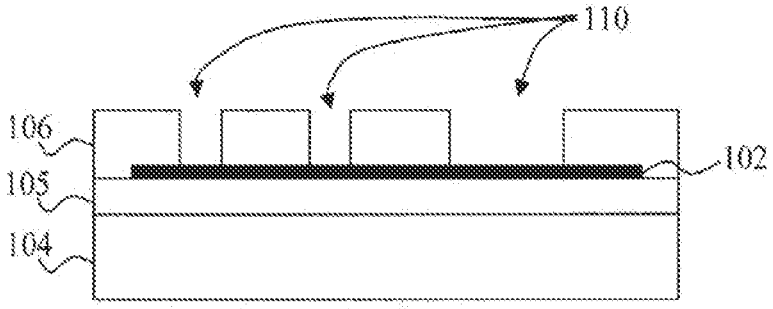

FIG. 5

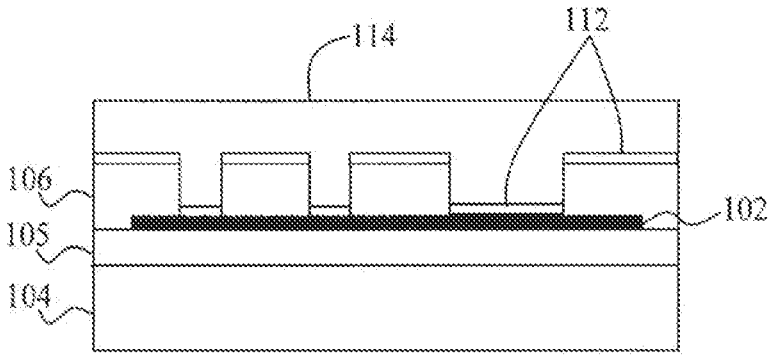

FIG. 6

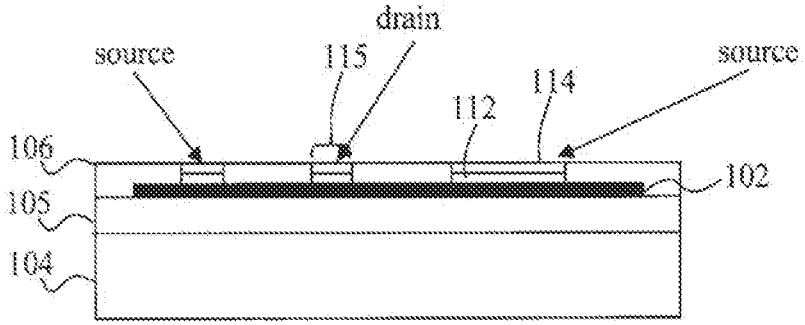

FIG. 7

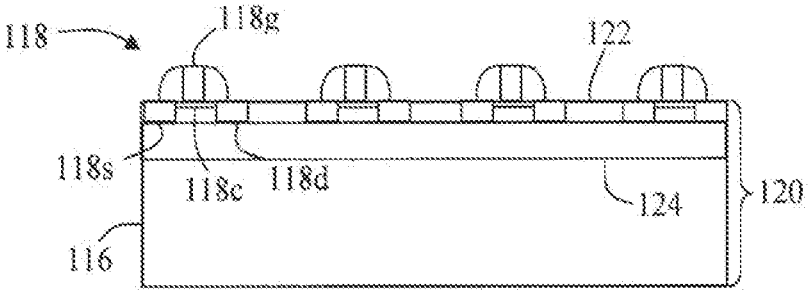

FIG. 8

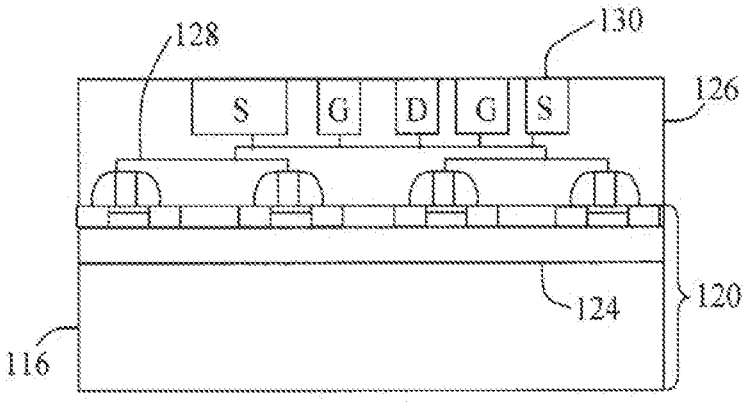

FIG. 9

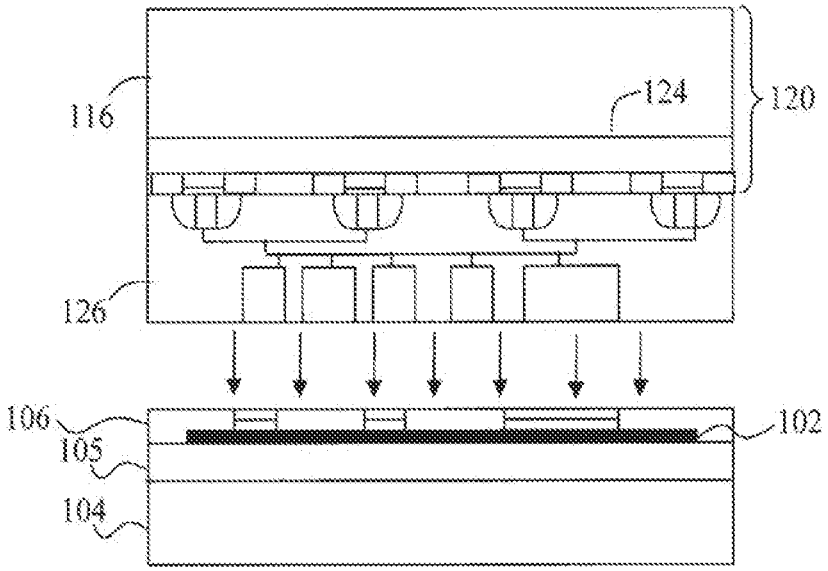

FIG. 10

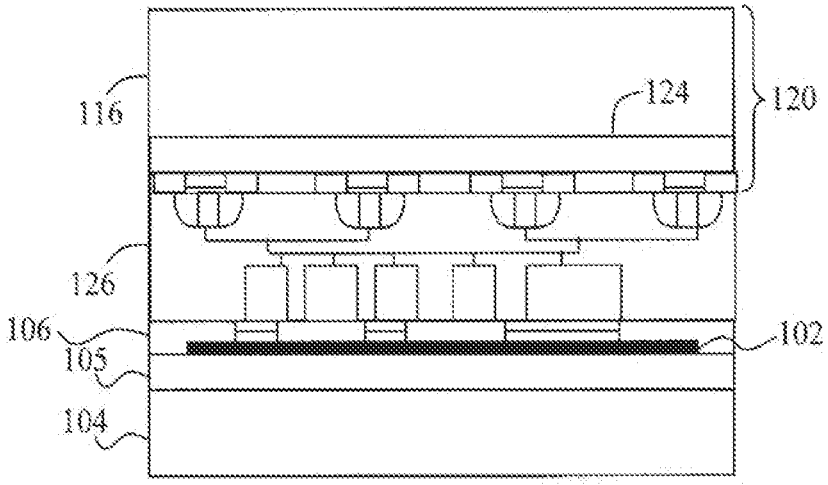

FIG. 11

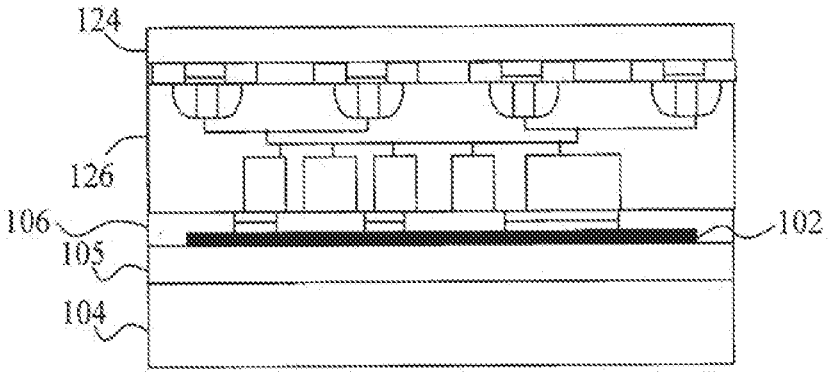

FIG. 12

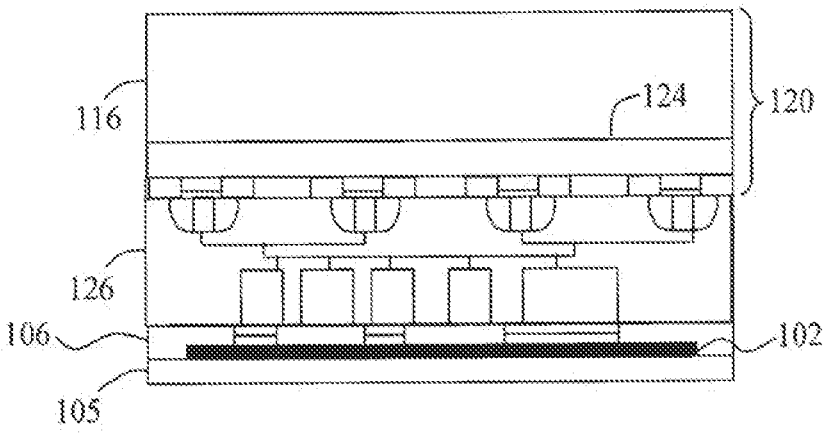

FIG. 13

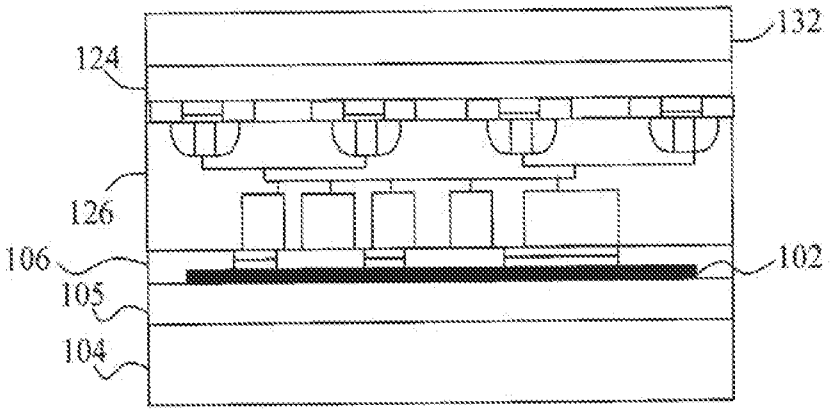

FIG. 14

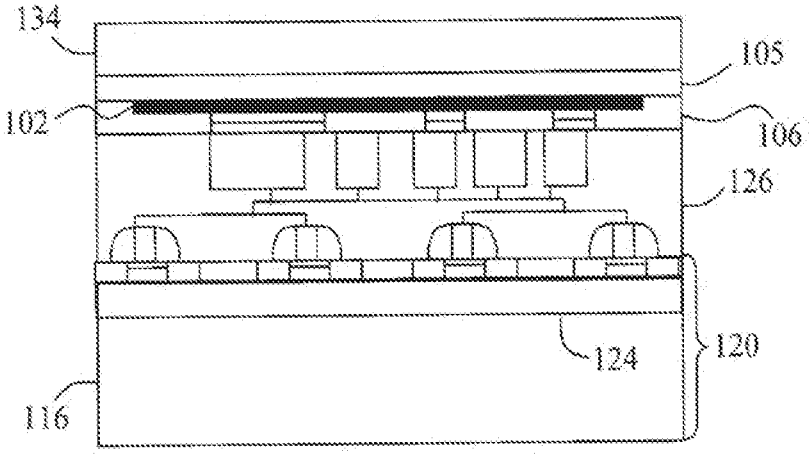

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/059133

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/60 B82Y40/00 H01L21/58 H01L23/498 B82Y10/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L B82Y

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal , WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/156320 Al (MASTROMATTEO UBALDO [IT]) 21 July 2005 (2005-07-21) Figures 1-3 and correspondi ng text.	1-8, 10-25
Y	US 2007/205450 Al (0KITA Y0ICHI [JP]) 6 September 2007 (2007-09-06) Fig. 11 and correspondi ng text, ; paragraph [0003]	1-8, 10-25
Y	US 5 640 049 A (R0ST0KER MICHAEL D [US] ET AL) 17 June 1997 (1997-06-17) Fig. 16 and correspondi ng text. ; column 5, lines 46-51 column 11, lines 12-17 column 11, lines 45-65	1-8, 10-25

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 October 2011	26/10/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Dauw, Xavi er

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/059133

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2006/007819 A1 (INFINEON TECHNOLOGIES AG [DE]; BEER GOTTFRIED [DE]; DANGELMAIER JOCHEN) 26 January 2006 (2006-01-26) Figs. 1, 8, 9 and correspondi ng text. ---	1-8, 10-25
A	W0 2007/082854 A1 (INFINEON TECHNOLOGIES AG [DE]; KN0RR ANDREAS [US]) 26 July 2007 (2007-07-26) Figs. 10, 12, 13 and correspdoni ng text. ---	1-25
A	PL0SZL A ET AL: "Wafer direct bondi ng: tai lori ng adhesi on between bri ttl e Ħat Θria1s", MATERIALS SCIENCE AND ENGINEERING R: REPORTS, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 25, no. 1-2, 10 March 1999 (1999-03-10), pages 1-88, XP004167445, ISSN: 0927-796X, D0I: 10. 1016/S0927-796X(98)00017-5 Sections 3.4, 5, 6.5-6.8 ---	1-25

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Information on patent family members

International application No
PCT/EP2011/059133

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		WO 2007082854 A1	26-07-2007