

Aug. 19, 1958

W. H. BURKHART ET AL
PRINTING CONTROL MEANS FOR ELECTRONIC
COMPUTERS AND THE LIKE

2,848,708

Filed June 4, 1953

5 Sheets-Sheet 2

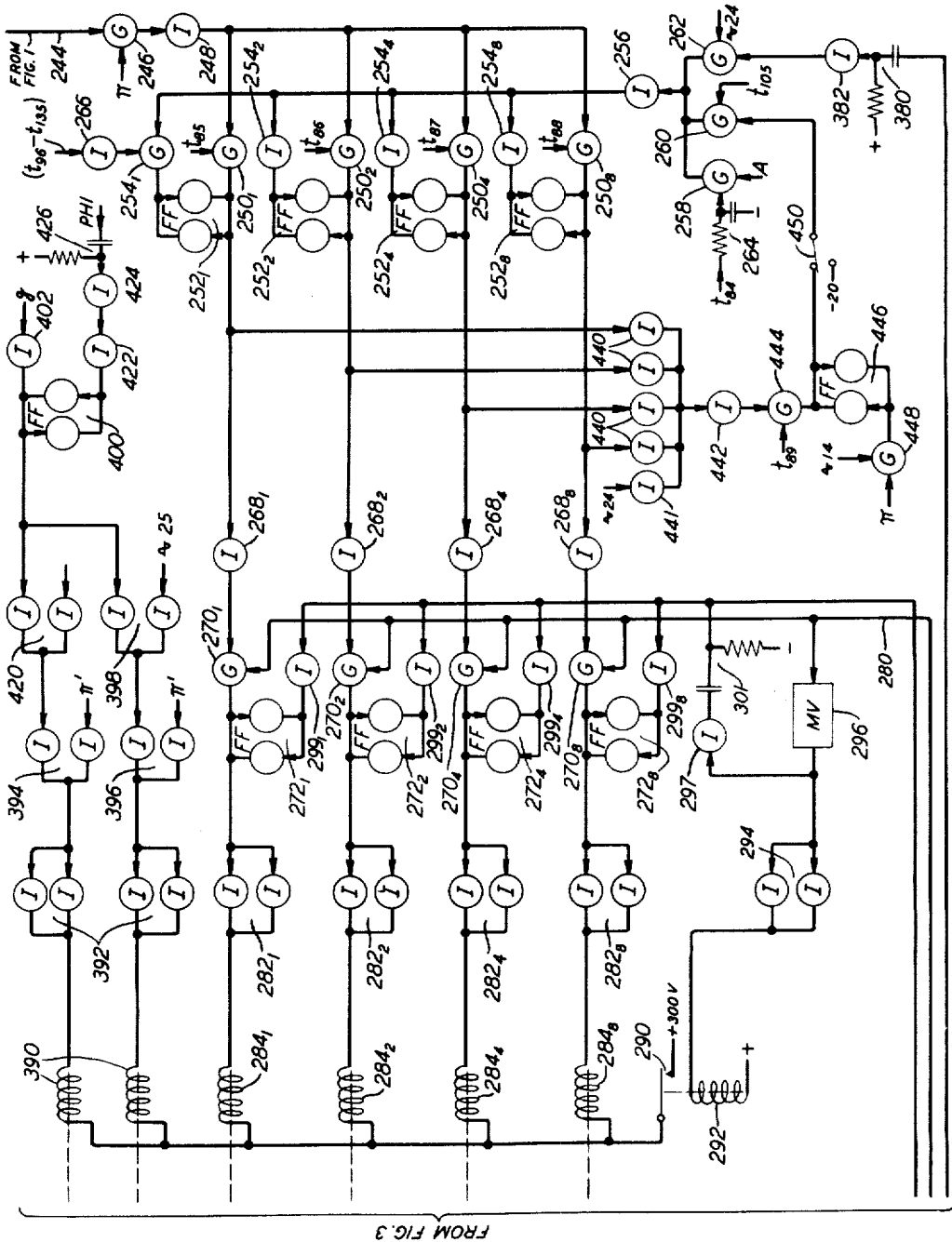


FIG. 2

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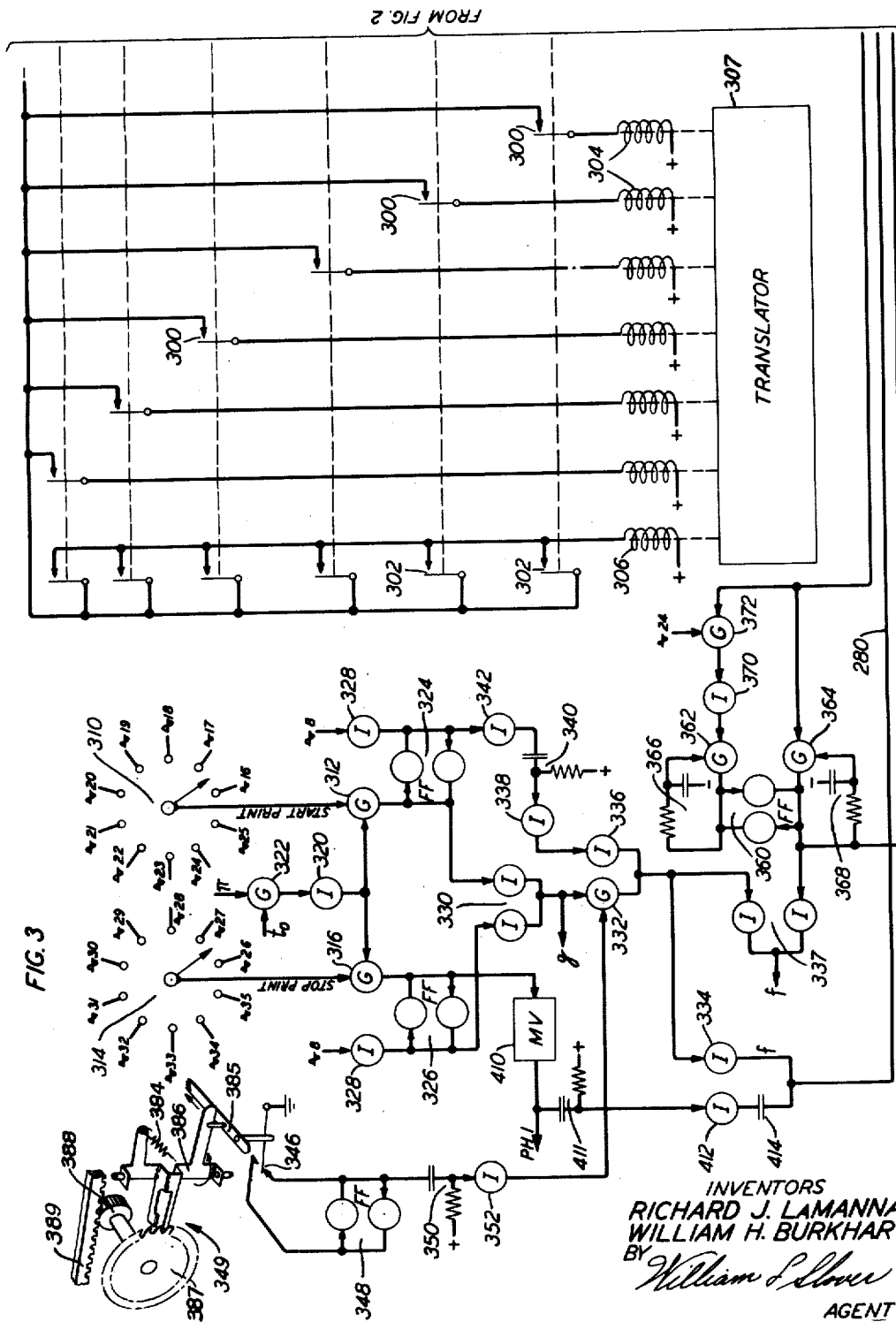
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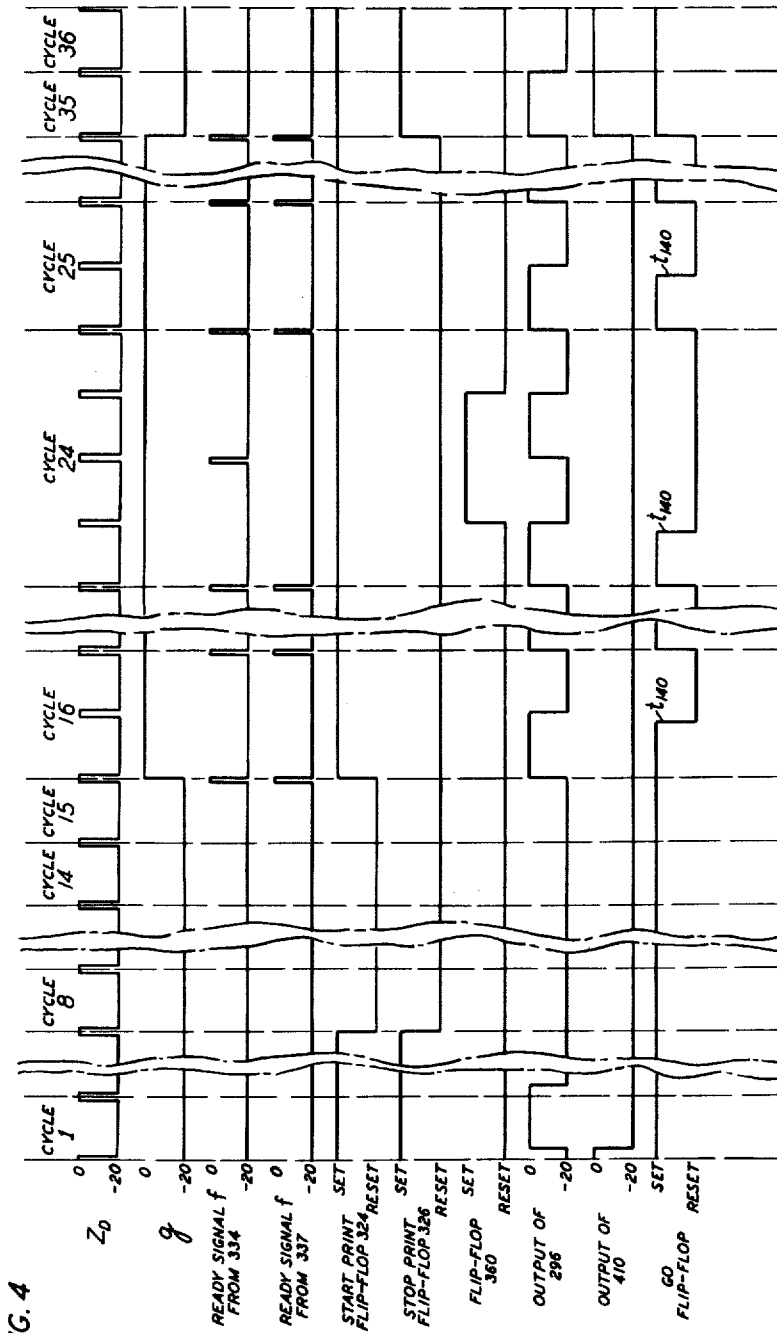


FIG. 4

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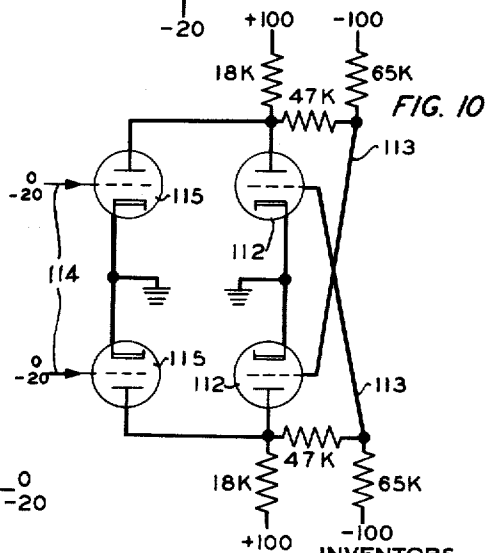
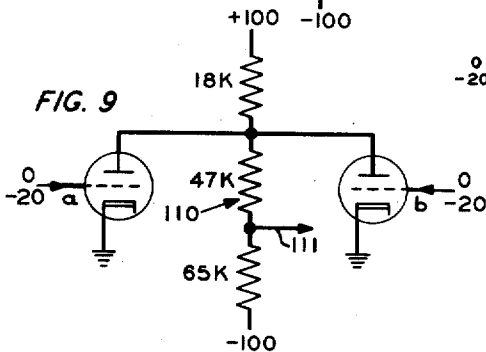
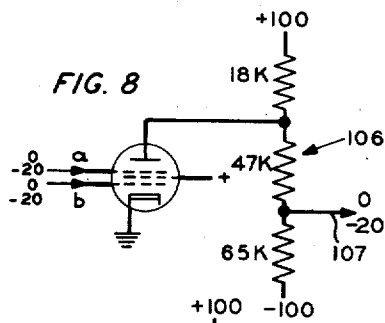
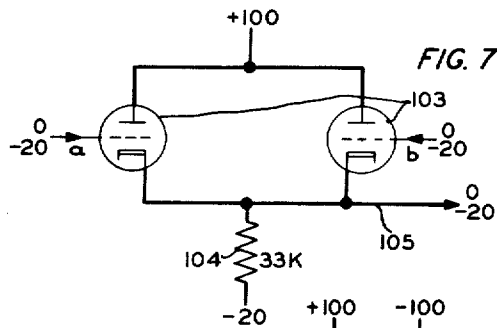
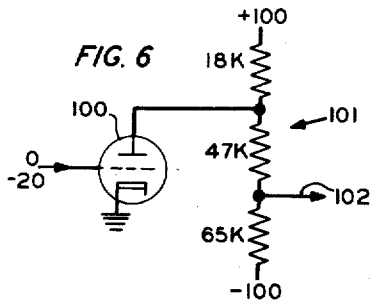
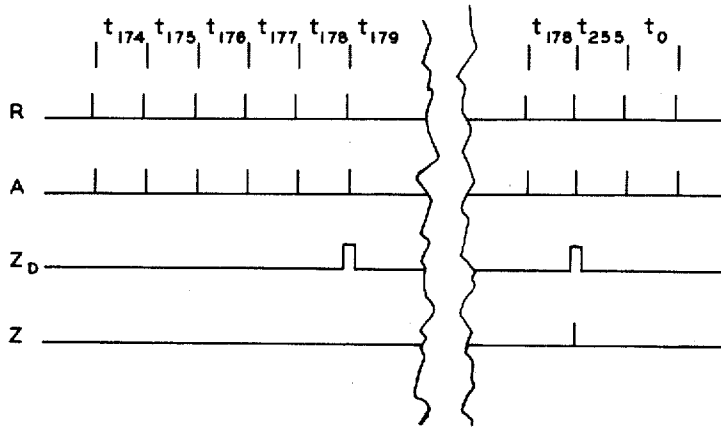
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FIG. 5



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2,848,708

PRINTING CONTROL MEANS FOR ELECTRONIC COMPUTERS AND THE LIKE

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Application June 4, 1953, Serial No. 359,532

8 Claims. (Cl. 340-173)

This invention relates to printing control means for electronic computers and the like.

One of the chief problems faced by the designers of electronic computers is that of recording the results of computations performed by the computers in a form which is intelligible to a human operator, preferably printing. In general, two different kinds of printing machines are available for use with computers, namely, serial type printers, for example, electric typewriters, and parallel type printers capable of printing a large number of characters simultaneously. The parallel printers are usually much more expensive than the serial type printers due to the amount of mechanism and electronic controls required therefor. The present invention is concerned chiefly with serial type printers such as electric typewriters. In a known electric typewriter, alphanumeric and symbol printing and other machine operations such as, "space" and "tabulate" are controlled by a translator unit which is operable by a plurality of electromagnets. One of the chief disadvantages of printing machines of this type is that the speed thereof is very limited as compared to the rapid output rate of modern electronic computers. For example, the speed at which a printing machine of this type can print, may be in the neighborhood of ten characters per second, whereas the rate at which electronic computers are capable of presenting the results of computations may be anywhere from several thousand digits per second to millions of digits per second.

The principal object of the invention is the provision of means for controlling the operations of a relatively slow, serial type printing machine in accordance with the output of an electronic computer which operates at a much faster cyclic rate.

It has been found that in many instances, it is not desired to print all of the digits of each number which appears as an output of a computer but only to print a selected group of digits thereof. In other instances, it is not desirable to print zeros to the left of the most significant digit of a number except for a zero located immediately to the left of the decimal point, and those to the right thereof when no significant digit appears to the left of the decimal point.

Other objects of the invention are to provide means whereby these modes of operation may be performed by a serial type writer under control of an electronic computer or the like.

According to the invention, means are provided to reduce the effective cyclic rate of an electronic computer to that of a serial type printer of the sort described. The computer is provided with means whereby the successive digits of a number to be printed are presented to control circuits for the printer one digit per cycle of the latter. Means are also provided to further modify the cyclic rate of the computer when it is desired to print a decimal point, said means, in effect, permitting but a single cycle of the computer for two cycles of the printer, during the first of which the two digits immediately to

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the left of the decimal point are printed and during the second of which the decimal point itself is printed.

Means are provided to block printing of the zeros to the left of the most significant digit of a number except where the said most significant digit occurs to the right of the decimal point, in which case one zero is printed to the left of the decimal point and all of the digits to the right of the decimal point are printed. Preferably the means for eliminating zeros from either end of a number are so arranged as to automatically effect carriage space operations so that the decimal points of numbers printed one above the other are aligned. Further means are provided to drop any desired number of digits from either end of a number to be printed, that is, not to print said digits. Means also are provided to effect automatic "tabulate" operations following printing of the last to be printed digit of each number.

Other objects and features of the invention will become apparent from the following description when read in the light of the drawings of which:

Figs. 1, 2 and 3, taken together as indicated thereon, constitute a schematic wiring diagram of the control circuit of the invention and of those fragments of the computer and of the typewriter which are essential to an understanding of the invention;

Fig. 4 is a timing diagram for the means of the invention;

Fig. 5 is a pulse diagram illustrating the relation of several pulse trains utilized in the computer;

Fig. 6 is a detailed wiring diagram of an inverter which is shown in the other figures of the drawings by an encircled I;

Fig. 7 is a detailed wiring diagram of an "or" gate which in the other figures of the drawings is indicated by an encircled "V";

Fig. 8 is a detailed wiring diagram of a coincidence or "and" gate which in the other figures of the drawings is indicated by an encircled "G";

Fig. 9 is a detailed wiring diagram of a plate connected type coincidence gate which in the other figures of the drawings is indicated by a pair of circles having a common output line extended therefrom; and,

Fig. 10 is a detailed wiring diagram of a flip-flop which is initiated in the other figures of the drawings by a pair of circles interposed in opposite sides of a rectangular loop.

In order to facilitate an understanding of the invention, the drawings have been simplified by the substitution of block symbols for certain circuits which are used repetitively, and Figs. 6-10 have been added to illustrate the circuits represented by the blocks.

Referring to Fig. 6 there is illustrated an electronic inverter which in the other figures is represented by an encircled "I." As shown, the inverter consists of a triode 100 of suitable type having its cathode grounded and its anode applied to the juncture of the two positive-most sections of a three-section voltage divider 101. Said voltage divider is connected across sources of +100 and -100 volt potentials and has an output line 102 projected from the center tap thereof. Utilizing the resistor values indicated in the drawings, the application of a 0 volt potential to the grid of the triode to effect conduction of the latter causes output line 102 to assume a potential of approximately -20 volts. Application of a -20 volt potential to the grid of the triode, however, cuts off the latter and the potential of output line 102 rises to approximately 0 volt. In the present embodiment of the invention, potentials of 0 volt and -20 volts are used throughout and, for convenience, will hereinafter be referred to as "high" and "low" respectively.

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Referring now to Fig. 7, there is disclosed an Or gate which in the other figures is represented by an encircled "V." As shown, the Or gate consists of a pair of triodes 103 having their cathodes commonly connected through a resistor 104 to a source of negative potential, say -20 volts. An output line 105 is projected from the connected cathodes. Application of a low potential (-20 volts) to the grids of both triodes maintains both in cut-off condition and output line 105 assumes a potential of approximately -20 volts. However, if a high potential (0 volt) is applied to the grid of either triode, the potential of output line 105 is raised by cathode follower action to approximately 0 volt. Obviously, several triodes may be connected with a common resistor 104 and output line 105.

Referring to Fig. 8, there is illustrated a coincidence gate which in the other figures is represented by an encircled "G." As shown, the coincidence gate consists of a pentode of suitable type having its anode connected to a three-section voltage divider 106 of the sort described above, and its cathode connected to ground. As before, an output line 107 is projected from the center tap of the voltage divider. The screen grid of the pentode is connected to a source of positive potential in the normal manner. The control and suppressor grids of the pentode, however, are connected to signal sources which assume the high and low potential levels of 0 and -20 volts. The simultaneous application of high potentials to both grids of the pentode effects conduction thereof and output line 107 assumes a low potential (-20 volts). Application of a low potential to either or both grids of the pentode effects cutoff of the latter and output line 107 assumes a high potential (0 volt).

Referring now to Fig. 9, there is illustrated a plate connected type gate which in the other figures is represented by a plurality of circles coupled to a single output line. As shown, a pair of triodes have their anodes applied to a single voltage divider 110 which is provided with an output line 111 in the usual manner. A high output is produced on line 111 only when low potentials are simultaneously applied to the grids of both triodes. A low output is produced on line 111 when a high potential is applied to either or both triodes. Of course more than two triodes may be connected in this manner if desired, and also the triodes may be replaced by pentodes of the type used in the coincidence gates.

Referring now to Fig. 10, there is illustrated a bistable flip-flop which in the other figures is represented by a pair of circles interposed in opposite sides of a rectangular loop and which will hereinafter be referred to as a flip-flop. As shown, the flip-flop consists merely of two inverters 112 of the type shown in Fig. 6, with the output 113 of each applied to the grid of the other. Input lines 114 are provided to the grids of puller tubes 115, plate to plate connected each with one of the flip-flop triodes. Puller triodes 115 are illustrated in Fig. 10 to indicate the connection thereof with the flip-flop, but it is to be understood that the term "puller" means any device to set or reset the flip-flop, for example, pentodes of the sort utilized as coincidence gates. Conduction of one of the flip-flop triodes maintains the other triode non-conductive by reason of the low potential (-20 volts) on the output line 113 of the conducting tube. Application of a high potential (0 volt) on the input line 114 of the puller for the non-conducting tube effects conduction of the former and lowers the potential at its anode and, therefore, the potential of the output line of the non-conducting flip-flop tube, to the point where the conducting flip-flop tube is cut off, and the conductive states of the tubes reverse. Application of a low potential (-20 volts) to one of the input lines 114 is ineffective in so far as changing the state of the flip-flop is concerned.

It is to be understood, of course, that the circuits described above are merely by way of example and are readily replaceable by other circuits which accomplish the same results.

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The means of the invention, although not limited to use therein, are disclosed as embodied in the computer described and claimed in the copending applications to W. Burkhart et al., Serial Nos. 270,876, 298,526 and 255,712. This computer is serial in form of operation and utilizes the binary coded decimal (1, 2, 4, 8) system of notation. Two internal storage devices are provided; a precessing intermediate storage device into which and from which information may be transmitted a digit at a time, and a general storage device wherein a plurality of multidigit numbers may be stored each in a selected location.

The general storage device (Fig. 1) is a multichannel magnetic storage drum 123 of the sort disclosed in the patent to Cohen et al., No. 2,540,654, and consists of a rotating cylindrical member having a homogeneous magnetic coating on its circumferential surface. The magnetic surface of the drum is divided into a series of contiguous peripheral channels each having recording and playback means associated therewith. The rotational speed of the drum being constant, each rotation of the drum consumes a definite number of equal time periods, in the present instance, one hundred eighty, during each of which an area or cell of each channel is positioned adjacent the recording means to be magnetized thereby. As disclosed in the Cohen patent, a cell or area is magnetized with one polarity to indicate binary one and with the opposite polarity to indicate binary zero.

In order to synchronize the recording and playback means for the several drum channels with the rotation of the drum and for other reasons to become apparent hereinafter, one channel of the drum, that designated *a* in Fig. 1, is provided with a full complement of one hundred eighty magnetized spots. A second channel of the drum, that designated *b*, is provided with a single magnetized spot empirically positioned to signify the completion of each rotation of the drum.

Drum channel *a* (Fig. 1) has associated therewith a reading head which drives a pulse generator 124 adapted to produce pulse trains R and A as shown in the pulse diagram of Fig. 5. Drum channel *b* is provided with a reading head which drives a pulse generator 125 adapted to produce the pulse train Z_D of Fig. 5. It is to be noted that the pulse trains produced by pulse generator 124 have a frequency of 180 per revolution of the drum, whereas the Z_D pulses from pulse generator 125 have a frequency of one per drum revolution.

In order to facilitate the further description of the means of the invention, it will be assumed that each A pulse from generator 124 initiates a time period which terminates on the occurrence of the next following A pulse. There are, of course, 180 such time periods and they are numbered $t_0, t_1 \dots t_{179}$. As will appear hereinafter, however, the time period t_{179} is sometimes referred to as time period t_{255} .

Pulse generators 124 and 125 may be of any suitable sort adapted to produce the type of pulses indicated in Fig. 5. For example, pulse generator 124 may include means for developing the R pulses and multivibrators or the like for developing the delayed pulses A.

One purpose of the pulse train A is to advance a time period binary counter 126 (Fig. 1) one count for each pulse. This counter may be of any ordinary sort as disclosed on pages 17-19 of "High Speed Computing Devices" by the staff of ERA, 1950, published by McGraw-Hill Book Company. In the present instance, counter 126 is advanced by negative pulses. Therefore, the positive A pulses from generator 124 are applied to an inverter 127 whose output is delivered to the counter through an Or gate 128. Inasmuch as counter 126 is advanced one count by each A pulse, the state thereof at any particular time is an accurate indication of what time period of drum revolution the general storage device has reached. Therefore, output lines from the several stages of the counter are applied to a matrix 130 whose

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outputs 131 are usable for timing purposes. Matrix 130 preferably is constructed of diodes and includes among its output lines 131 one that assumes a high potential during each time period or group of time periods that is pertinent to the timing control of the invention. Matrices of this sort are well known and need not be discussed further. See Patent No. 2,476,066.

In order for binary counter 126 to count through 180 counts (0-179) during each of selected revolutions of drum 123, the same must include eight stages which ordinarily would enable the counter to count through 256 counts, that is, from 0 to 255. Means are provided, therefore, either to stop the counter when it reaches a count of 179 during the last time period of each cycle, or to skip the counter to capacity (255) at such time. Obviously, if counter 126 is skipped to count 255 at the beginning of what would otherwise be time period t_{179} , the output of matrix 130 will not indicate time period t_{179} but rather will indicate time period t_{255} .

The means whereby counter 126 is stopped at 179 includes an output line 131 of matrix 130 (Fig. 1) which is high only when said counter stands at 179 and which is applied to Or gate 128 and maintains the output of the latter high continuously. Obviously, the inverted A pulses from pulse generator 124 are ineffective to advance the counter when this condition exists, and matrix 130 continues to indicate time period t_{179} even though drum 123 does not stop rotating.

The means whereby counter 126 is skipped to capacity (255) by supplying a pulse to set each stage of counter 126 to its on state in the manner shown in Patent No. 2,604,263 are under control of the A and Z_D pulses from pulse generators 124 and 125 and, also, under control of the printing unit which, as will appear hereinafter, initiates a cycle of operation of counter 126 each time the same is prepared to print a digit. The said means include, among other things, a binary counter 136 designated Step Counter which is advanced one count for each step of the printing operation.

An Or gate 138 (Fig. 1) whose output, when low, advances step counter 136, is under the joint control of a Go circuit flip-flop 140 and a timing control circuit that comprises a coincidence gate 141. Go flip-flop 140 is set to apply a low potential to gate 138 under control of a signal f from the printing unit. This signal f , hereinafter called the Ready pulse or signal, is applied to an inverter 142 whose output is connected through a differentiating circuit 144 to an inverter 146 which in turn controls a puller 148 for flip-flop 140. The resistor of differentiator 144 is connected to a source of positive potential which normally maintains the inverter 146 conductive. However, when the Ready signal f effects conduction of inverter 142, a negative pulse is applied to inverter 146 to cut off the same momentarily, and puller 148 sets flip-flop 140 which applies a low potential to Or gate 138. The other input of Or gate 138 stems from coincidence gate 41 to which the A pulses from pulse generator 124 and the Z_D pulses from generator 125 are applied. The Z_D pulses and the A pulses effect conduction of gate 141 and, therefore, application of a low potential to Or gate 138, at the beginning of the last time period (t_{179} or t_{255}) of each drum cycle, this being the only time at which the Z_D and A pulse lines assume high potentials coincidentally, see Fig. 5. If flip-flop 140 has also been set to apply a low potential to Or gate 138, the latter produces a low output which advances step counter 136 one count.

The output of Or gate 138, conveniently labeled Z, is also applied through an integrating or delay circuit 152 to an inverter 156 which is connected to the several stages of time period counter 126 to skip the latter to capacity (255) each time step counter 136 is advanced. It is to be noted that the advance of step counter 136 and skipping of time period counter 126 to capacity are effected by the A pulse which occurs at the beginning

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of the last time period of a drum revolution, which pulse is the one that otherwise would advance the time period counter to 179. Therefore, a time period t_{179} occurs only when the step counter is not advanced to initiate a step of operation on the next revolution of drum 123 (Fig. 5). When a time period t_{179} does occur, however, it lasts for an indefinite period of time until the A pulse occurring during the last time period of a succeeding rotation of the drum is effective to advance the step counter and to skip the time period counter to capacity, see Fig. 5. It is to be mentioned that the delay circuit 152 serves to delay the application of the Z pulse to counter 126 until it is too late for the A pulse which effected production thereof to act through gate 128 to advance the counter from the capacity count to which it was skipped by the Z pulse, to its initial count of t_0 .

The Go flip-flop 140 (Fig. 1) is reset at appropriate times to prohibit further advance of step counter 136 and to prevent skipping of time period counter 126 to capacity.

Means to this end include an inverter 158 to which an output g from the printing unit is applied to indicate that the latter is not prepared to receive a digit for printing during the next revolution of the drum. The output of inverter 158 is applied to an inverter 162 which, when the former becomes conductive, applies a high output to a coincidence gate puller 164 for flip-flop 140. Also applied to gate 164 is an output line 131 of matrix 130 that is high during time period t_{140} . Therefore, if a signal g is applied to inverter 158, then during time period t_{140} flip-flop 140 is reset and applies a high potential to Or gate 138. This high potential is passed on to the input of step counter 136 to prevent advance thereof and to the inverter 156 which controls skipping of time period counter 126 to capacity to prevent such skipping.

As will presently appear, printing operations with the means of the invention each consume 36 steps. Evidently counter 136 must be able to count to 36 which if, as here, said counter is binary in form, requires that the same have a capacity of 64 (2^6). Therefore, means are provided to reset counter 136 to its initial "one" count each time it has reached the count of 36. A matrix 167 similar to the matrix 130 described above is controlled by the several stages of counter 136 and has among its output lines 166, one which is high when the same stands at 36. This line is applied through an inverter 176 and an integrating or delay circuit 178 to a plate connected type coincidence gate 168 whose output, in turn, is applied to the grid of a cathode follower 170 whose purpose it is to reset the step counter to its initial one count in the manner shown in Patent No. 2,604,263. The cathode follower may be substantially identical with either half of the Or gate described hereinabove. The other input of gate 168 is taken from gate 141 which, it will be remembered, conducts only at A pulse time of the last time period of each cycle of drum 123. The effect of this connection is to reset step counter 136 at exactly the same time of cycle as the same would be advanced under the circumstances described earlier. In order to prevent the step counter from being reset immediately following the advance thereof to 36 under control of the same low output of gate 141 which initiated said advance, in short, to ensure that step 36 comprises a full drum rotation, the delay circuit 178 is designed to prevent application of the inverted step 36 signal to gate 168 until the input thereto from gate 141 at the beginning of step 36 goes high. Thus, the counter is not reset until gate 168 conducts during the next following drum revolution. Preferably delay circuit 178 is identical with circuit 152 described above and others to be described hereinafter.

In view of all of the above, it will be seen that there are always available to the means of the invention the several pulse trains described and also reference pulses indicative of the step and general storage device.

It is to be mentioned that other means such as those described in the aforementioned copending applications

may be provided for setting and resetting the Go flip-flop 140 and for resetting the step counter 136. Such means, however, form no part of the present invention and need not be described herein.

As described in the said copending applications, the numbers handled by the computer each include twenty decimal digits with the decimal point located between the tenth and eleventh digits. Each decimal digit is represented by a group of four binary digits in accordance with the binary coded decimal system of notation, and the eighty binary digits of each number are stored in an individual channel of drum 123 in positions appropriate to their being played back from the drum during time periods t_0 – t_{79} of a computer cycle.

Each drum channel (Fig. 1) is provided with an individual record and playback head 186 but only one record circuit 188 and one playback circuit 190 are provided. Record circuit 188 may be of the type disclosed in Patent No. 2,633,402 to Fleming, Jr., and playback circuit 190 may take the form disclosed in Patent No. 2,633,564 to Fleming, Jr. A selection circuit 192 which may be of the type disclosed in co-pending patent application Serial No. 382,167, filed September 24, 1953, by A. Sepabhan, is utilized to connect the several heads with the playback and record circuits individually under the influence of a control circuit 194. Circuit 194 is set up to effect the appropriate control, by orders or commands entered into the computer and stored on drum 123 for timely use by an Orders Control Section 196 of the computer, all as described in the aforementioned copending applications. For an understanding of the present invention it is sufficient to explain that an order or command to print a certain number stored on drum 123, is transmitted to the Orders Control Section 196 from the drum and is effective to influence an Operation Control Unit 198 to produce a print signal π , and, through the medium of control circuit 194, is effective to set up selection circuit 192 to permit playback of the number to be printed. Preferably, the print signal π remains high for substantially the whole of a printing operation and is low at other times. This is readily accomplished by taking the signal from the appropriate output of a flip-flop which is set near the beginning of a print operation and reset at the end thereof. Conveniently, a signal π' which is the inverse of the print signal π may be taken from the other output of the flip-flop.

In the instant embodiment of the invention the numbers to be printed are extracted from the drum 123 on the 14th revolution of the drum after an order to print a number has been presented. The time elapsed during these 14 drum revolutions is provided for the situations in which successive numbers are to be printed to allow the printing device to become set to start printing a number where a tabulation operation is carried out after printing each number, as will be described hereinafter. Accordingly, the number to be printed is extracted from the drum 123 when the step counter 136 is at count 14.

The number extracted from drum 123 (for printing) during time periods t_0 – t_{79} of step 14 is delayed one time period in playback circuit 190 and is applied to a coincidence gate 200 during time periods t_1 – t_{80} of the same step. The delay of one time period in the playback circuit 190 is occasioned by the construction of the latter and the manner in which the timing of information signals flowing through the computer is set up. The playback circuit includes an amplifier section which amplifies the weak signals extracted from the drum and a flip-flop which is set and reset at A pulse time of each time period in accordance with the amplified information signals.

Referring to the pulse chart of Fig. 5, it will be seen that the R pulses which control the time of recording of information occur close to the end of each time period and that the A pulses occur at the beginning of each time period. Therefore, a signal which is recorded on the drum at R pulse time of, say, time period t_0 , pro-

duces a playback signal which, due to the inherent delays in recording and playing back, and in the amplifiers of the playback circuit, does not affect the setting of the flip-flop of the playback circuit until A pulse time of time period t_1 of a subsequent drum revolution.

The gate 200 to which the numbers extracted from the drum are applied is opened during time periods t_1 – t_{80} of step 14 of printing operations. Therefore, a number played back from the drum for the purpose of printing the same is passed through the gate 200, that is, the gate conducts in response to each high (0 volt) pulse that is applied thereto to indicate the occurrence of a binary one in said number. It is to be mentioned that the gate 200 may comprise the gate 300 shown in Fig. 4 of the copending application #298,526 which is used to gate dividends and multipliers as they are transmitted from the drum but, of course, is modified for control by the π signal. The output of gate 200 is applied to a four time period delay circuit 202 which, as described in the last mentioned copending application, may include an adder-subtractor which affords a three time period delay, and a one time period flip-flop delay but which, in so far as the present invention is concerned, serves merely as a delay circuit. Circuit 202 is provided with two outputs I and I', the former of which assumes a high potential to indicate a binary one and the latter of which assumes a low potential to indicate binary one. This notation is also utilized in other parts of the description. The output of I' of circuit 202 is applied to a plate connected type coincidence gate 204 along with the output of an inverter 205 which is maintained conducting during step 14. The output of gate 204 which assumes a high potential to indicate binary one is applied to a coincidence gate 206 which is opened during time periods t_5 – t_{84} of printing operations. The timing control of gate 206 is effected by a flip-flop 208 which is set to apply a high (0 volt) potential to the gate by a coincidence gate puller 210 during time period t_5 of a printing operation and is reset to apply a low (–20 volt) potential to the gate by a puller 212 during time period t_{85} . This same type of timing control, namely a flip-flop which is set and reset at the appropriate times, may also be utilized in connection with the gate 200 described above and others to be described hereinafter.

It will be seen, therefore, that during time periods t_5 – t_{84} of step 14 of printing operations, the gate 206 conducts each time a high potential indicative of binary one is applied thereto and is cut off when a low potential indicative of binary zero is applied thereto.

The output of gate 206 is applied to a coincidence gate 214 and through an inverter 216 to a coincidence gate 218. Gates 214 and 218 control the operation of a record circuit 220 which drives a recording head 222. Record circuit 220 may be identical with record circuit 198 described hereinabove. Evidently, gate 218 conducts to effect recording of binary one while gate 214 conducts to effect recording of binary zero. The gates 214 and 218 also have applied thereto the output of a plate connected type coincidence gate comprising a triode 224 and a pentode 226 having their plates connected to a single voltage divider in the manner described above in connection with Fig. 9. Pentode 226 is caused to conduct whenever a time period t_{179} occurs during a printing operation and triode 224 has the output of an inverter 230 applied thereto, said inverter being controlled by the record pulses R from pulse generator 124 (Fig. 1). Therefore, the output of the plate connected gate 224, 226 assumes a high potential to condition gates 214 and 218 for conduction only at record pulse time of each time period except time period t_{179} of a printing operation. Other means such as those described in the last mentioned copending application may also be provided to control the operation of the gates 214 and 218, but as the same form no part of the present invention they need not be described herein.

The recording head 222 is associated with a magnetic disc 232 which may be driven synchronously with drum 123 or may be integral therewith. In either event, the disc comprises a magnetic recording channel identical with those located on the drum. Also associated with the magnetic disc is a playback head 234 which controls a playback circuit 236. Circuit 236 may be identical with the playback circuit 190 described above and, like the latter, includes a flip-flop which occasions a one time period delay of information passing through the playback circuit. The recording and playback heads 222 and 234 are positioned apart relative to one another an angular distance which affords a delay between the recording and playing back of information of 91 time periods. Adding the delay of the playback circuit to this, we obtain an overall delay of 92 time periods.

One output of playback circuit 236, that which assumes a high potential to indicate a binary one, is coupled back through a coincidence gate 240 to the gate 214 and the inverter 216 which control the operation of the record circuit 220. Gate 240 is controlled by an inverter 242 which conducts to close the gate only during step one.

The feed back loop through gate 240, whereby information initially recorded on disc 232 is fed back to the record circuit to be recorded 92 time periods later, effects precession of such information at the rate of one decimal digit (four binary digits) per step. Remembering that each step contains 180 time periods a digit originally recorded on disc 232 during time periods t_5-t_8 is rerecorded on the disc during time periods $t_{97}-t_{100}$ of the same step and again during time periods t_9-t_{12} of the next step, etc. A more complete discussion of precession is included in the copending application #298,526. For present purposes, it is sufficient to understand that on step 15 the number which was originally recorded on the disc during time periods t_5-t_{84} of step 14 is played back to be recorded again during time periods t_9-t_{88} of step 15. That digit of the number which is played back during time periods $t_{85}-t_{88}$ of step 15 is the highest order digit thereof and, as presently will appear, is the only one which affects the printing control circuits during that step. During step 16, the next to the highest order digit of the number to be printed is played back during time periods $t_{85}-t_{88}$ and effects appropriate operation of the printing control circuits. This mode of operation continues, with but one exception to be pointed out, until on step 34 the lowest order digit is played back during time periods $t_{85}-t_{88}$.

The output of playback circuit 236 which assumes a low potential to indicate binary one is connected via line 244 with a coincidence gate 246 (Fig. 2) that is held open all during printing operations by the print signal π . Gate 246 controls conduction in an inverter 248 whose output is applied to four pentode pullers 250₁, 250₂, 250₄, and 250₈, which are conditioned for conduction successively during time periods t_{85} , t_{86} , t_{87} and t_{88} respectively. Only those digit signals which control gate 246 during time periods t_{85} , t_{86} , t_{87} and t_{88} have any effect on the operation of the pullers 250. When, during one of said time periods a high potential indicative of binary zero is applied to gate 246 and effects a conduction thereof, the inverter 248 applies a high potential to all of the pullers, but only the one having the appropriate timing signal applied to it conducts. The pullers 250 are applied to flip-flops 252₁, 252₂, 252₄ and 252₈ which are preset to states indicative of binary one, to reset the same to the opposite or binary zero indicating states. The pre-setting of the flip-flops is accomplished by pullers 254 under control of an inverter 256 which is itself controlled by a plate connected type coincidence gate comprising three penodes 258, 260 and 262, having their anodes connected to a single voltage divider in the manner described above. For present purposes it will be assumed that the pentodes 260 and 262 are non-conducting and

that the operation of the gate is controlled solely by the state of conduction of pentode 258. The A pulses from pulse generator 124 are applied to one grid of pentode 258 and the output of an integrating or delay circuit 264 to which a high potential is applied during time period t_{84} is connected to the other. The arrangement is such that the high potential applied to the integrating circuit at the beginning of time period t_{84} is not reflected at its output until after the A pulse occurring during said time period has past, but is reflected at said output when the A pulse occurs during the next following time period, namely time period t_{85} . Therefore, pentode 258 conducts during A pulse time of time period t_{85} and cuts off inverter 256 to operate the pullers 254 which set the flip-flops 252 to the binary one condition. However, it is to be mentioned that the flip-flop 252₁ may not be set to the binary one state by its puller 254₁ if at the same time as puller 254₁ is operated, namely, the beginning of time period t_{85} , the puller 250₁ is operated to set the flip-flop to the binary zero state. It does not matter which puller is effective over the other during the short conductive period of the puller 254₁, since the latter, when it is cut off, relinquishes all control of the flip-flop to the puller 250₁, which remains conductive for a considerable period of time afterward. It is also to be mentioned that whereas the pullers 254₂, 254₄ and 254₈ are triodes, the puller 254₁ is a pentode which is maintained non-conducting during time periods $t_{96}-t_{135}$ of each cycle by an inverter 266. The purpose of this arrangement will be described hereinafter, it being sufficient, for the present, to understand that when pentode 258 conducts, the pentode puller 254₁, is operated along with the triode pullers 254₂, 254₄ and 254₈.

From the above it will be seen that at the end of time period t_{88} of step 15 and subsequent steps of a printing operation, the states of the four flip-flops 252 represent, in binary coded decimal notation, the decimal digit which is to be printed. It will also be seen that, as thus far described, each digital setting of the flip-flops is not disturbed until just prior to the time at which they are to receive a new setting, that is, time period t_{85} of the step following that in which they were set.

It is to be pointed out that the flip-flops 252 correspond to the flip-flops 338 described in the aforementioned application Ser. No. 298,526 and may control and be controlled by other means than those which are shown here as pertinent to printing.

The output line of each flip-flop 252 which assumes a high potential when the latter is in the binary one state is applied to an isolating inverter 268 whose output in turn is applied to a pentode puller 270 for a flip-flop 272. For convenience, the flip-flops 272 and the pullers 270 are given the same subscripts 1, 2, 4 and 8, as the associated flip-flops 252.

The pentode pullers 270, in addition to being controlled for differential operation by the isolating inverters 268 are also controlled as to the time of their operation by the Ready pulses f hereinabove referred to in connection with the "Go" circuit of Fig. 1. These pulses, as will be pointed out hereinafter, are applied to the pullers 270 via line 280, to transfer the settings of the flip-flops 252 to the flip-flops 272 as soon as the printing machine is ready for control by said flip-flops 272.

The output of each flip-flop 272 which is high to indicate binary one is applied to means 282 for energizing a relay 284. As shown, the means 282 may comprise a pair of inverters connected in parallel to provide dual current paths to ground.

In order to control the length of time for which the relays 284 are energized under control of each setting of the flip-flops 272, the coils of the same are connected to positive supply (say +300 volts) through a normally open contact 290 of a relay 292 (Fig. 2). Relay 292 is controlled by a pair of paralleled inverters 294 in the same manner as the relays 284. The inverters 294, how-

ever, are controlled by means 296 which is triggered by the Ready pulses f (see also Figs. 3 and 4) and which maintains the inverters conducting for a predetermined length of time after each Ready pulse. Preferably, the means 296 comprises a one shot multivibrator of the Phantastron type, disclosed in Patent No. 2,549,874 to F. C. Williams, adjusted to provide (on being triggered) a positive going pulse of suitable magnitude and duration to effect conduction of the inverters 294 for the required length of time. The output of circuit 296 is also applied to an inverter 297 which, through a differentiator 301, drives pullers 299 adapted to pull the four flip-flops 272 to their binary one states when the said output assumes a low potential (-20 volts) on termination of each said pulse. If desired, any other means for setting the flip-flops 272 to their binary one states may be provided so long as the same is effective prior to each operation of the pullers 279 to transfer the settings of the flip-flops 252 to the flip-flops 272.

Evidently, therefore, each Ready pulse effects the transfer of the representation of a digit to be printed into the flip-flops 272 and also initiates an operation of the timing means 296 which, through relay 292, effects energization of those relays 284, associated with the flip-flops 272 which indicate binary one.

In the illustrated instance of the invention the relays 284 are provided each with two normally open contacts 300 and 302 (Fig. 3). Each contact 300 when closed provides a path to negative supply for a solenoid coil 304. The contacts 302 serve to provide a path to negative supply for a solenoid 306. The solenoids 304 which are energized selectively in accordance with the settings of the flip-flops 272, and the solenoid 306 serve to operate a mechanical translator unit 307 for an electrical typewriter. The arrangement of the solenoids 304 and 306 will be recognized as that utilized in the well known Flexo-writer typewriter. This machine is so well known in the computer art that it is not deemed necessary to illustrate or describe the same further. It will be understood, however, that the solenoids 304, or for that matter, the relays 284, may be utilized to effect differential control of any other serial type printing device. Another relay control printing device is disclosed in Patent No. 2,461,451.

As mentioned above the numbers transmitted from the storage device to the printing circuits contain twenty digits, ten on either side of a decimal point. According to the invention, any desired number of digits may be dropped from either end of a number, that is, not printed. The means to this end also effect production of the Ready pulses f and the signals g which are used to control the Go circuit of the counters (Fig. 1) in the manner described above. Said means include a pair of selector switches 310 and 314 (Fig. 3) manually settable to positions indicative of the number of digits to be dropped from each end of a number. Switch 310 may be referred to as the Start switch inasmuch as its setting determines when printing will start, and switch 314 may be referred to as the Stop switch since it determines when printing will stop. Remembering that the highest order digit of a number to be printed is set upon the flip-flops 252 during time periods $t_{85}-t_{83}$ of step 15 for printing during step 16 and that successively lower order digits are set up in said flip-flops during succeeding steps, one per step, it will be seen that any desired number of digits can be dropped from the left-hand end of a number merely by suppressing printing until the appropriate step of the counter 136 has been attained. In like manner, digits can be dropped from the right-hand end of a number by suppressing printing after a selected step. Therefore, switches 310 and 314 are arranged to start and stop printing on steps appropriate to their setting. Switch 310 is connected with the appropriate output lines 166 of matrix 167 for step counter 136 (Fig. 1) to effect transmittal of a high potential (0 volt) through the switch to a pentode puller 312 when said counter attains the step count represented by the setting of the switch, say 16-24.

In like manner switch 314 is connected with the appropriate output lines 166 of matrix 167 to effect application of a high potential (0 volt) through the switch to a pentode puller 316 when the counter attains the step count indicated by the setting of the switch, say 27-35. Both pullers 312 and 316 are also under control of an inverter 320 which is cut off to apply a high potential to the pullers during time period t_0 of each step of a printing operation, by a coincidence gate 322 which conducts at those times. Pullers 312 and 316 serve to pull flip-flops 324 and 326, respectively, each to a set state. Each flip-flop is pulled to the opposite or reset state during step 8 by a puller 328. An output of flip-flop 324 which is low when the latter is in the set state is applied to a plate connected type gate 330 along with an output of flip-flop 326 which is low when the latter is in the reset state. The output of gate 330 is the signal g (Fig. 4) which, in addition to controlling the Go circuit (Fig. 1) in the manner described above, is also applied to one input of a pentode 332 of a plate connected type gate which also includes a triode 336. Evidently, as shown in Fig. 4, the signal g is low prior to setting of flip-flop 324 during time period t_0 of the step on which the first digit is to be printed and subsequent to setting of the flip-flop 326 during time period t_0 of the step on which the last digit is to be printed, but is high during the intervening time, that is, during printing steps.

The plate connected gate composed of pentode 332 and triode 336 controls production of the Ready pulses f , that is whenever the output of the gate goes low, a Ready pulse is produced. The said output is applied to an inverter 334 which, when it is cut off, produces the Ready pulses as applied to the timing means 296, and also to one triode of a plate connected gate 337 which produces the Ready pulses as applied to the Go circuit of Fig. 1. The said pulses are identical and are considered as one. The only reason for having the one produced by the inverter and the other by the gate is, that in one instance to be described hereinafter it is desired to block application of a Ready pulse to the Go circuit and this is an economical means to that end.

The first Ready pulse f of each printing operation is produced in response to setting of the "start print" flip-flop 324, while succeeding Ready pulses f are produced in response to the operations of a "Ready" switch 346 which, as will be described hereinafter, operates only when the printing device is prepared to print another digit. The control by flip-flop 324 is effected through an inverter 342 which conducts when the flip-flop is set by puller 312. The output of inverter 342 is applied through a differentiating circuit 340 to an inverter 338 which controls the triode 336. The resistor of the differentiator 340 is connected to a source of positive potential suitable to maintain the inverter 338 normally conducting. However, when inverter 342 becomes conducting and its output potential drops, the differentiator applies a sharp negatively directed pulse to inverter 338 to cut off the same and effect conduction of a triode 336. The control of pentode 332 by "Ready" switch 346 is effected as follows: The "Ready" switch 346 serves to apply ground potential to either grid of a flip-flop 348 having an output applied through a differentiating circuit 350 to an inverter 352 which controls the pentode 332. The resistor of differentiator 350 is connected to a source of positive potential so that inverter 352 is normally maintained conducting and, therefore, the pentode 332 non-conducting. Only when a low potential is applied to the differentiating circuit is the inverter 352 cut off momentarily to allow conduction of pentode 332. Flip-flop 348 is set to apply the said low potential to a differentiator 350 each time an operation of the printer progresses to the point at which the next digit to be printed may be set up in the flip-flops 272. In the instant embodiment of the invention, the pull up time of the relay 292 and of the relays 284 and the other delays in the system permit of the flip-flops 272 being set to represent a new digit shortly after

a printer type bar has printed a digit, that is, during the restoring movement of the type bar. Therefore, the "Ready" switch 346 is arranged to be operated by the escapement mechanism which shifts the printer carriage laterally immediately following each printing as indicated diagrammatically at 349 in Fig. 3. The escapement mechanism includes a member 385 moved a short distance in the direction of the arrowhead and then released immediately following each printing. Member 385 is provided with a depending stud which operates the switch 346 and an upwardly directed stud which serves to rotate an escapement pawl 386 in the direction indicated. On release of the pawl by said stud it is restored by a spring 384. Each operation of pawl 386 permits a ratchet wheel 387 to advance one tooth space under spring pressure exerted thereon through the familiar typewriter carriage rack 389 and the pinion 388 which meshes therewith and is mounted for rotation with the ratchet wheel. Preferably, the structural mounting for the switch is adjustable to permit of the escapement operating the switch to set the flip-flop 348 at exactly the right time and then restoring the switch to reset the flip-flop.

At this point it is deemed desirable, briefly to review the operations thus far described. During steps 1-15 step counter 136 (Fig. 1) is advanced one count for each rotation of drum 123 (see Fig. 4). During time periods $t_{85}-t_{88}$ of step 15, the highest order digit of the number to be printed is set up in the flip-flops 252 (Fig. 2). Assuming that the "Start printing" switch 310 is set to effect printing of said highest order digit, the flip-flop 324 is set during time period t_0 of step 16 and the signal g and the first Ready pulse f are produced. Said Ready pulse effects transferral of the settings of the flip-flops 252 to the flip-flops 272 and energization of the relays 284 in accordance with said settings. The relays 284, of course, effect printing of the digit represented by said settings. The signal g terminates the automatic operation and institutes a so-called one step mode of operation in which the step counter 136 is advanced one count for each digit printing no matter how many rotations the drum makes during each printing, and the time period counter 126 advances through a single cycle of operation for each count of counter 136. This control by the signal g is effected through the Go flip-flop reset puller 164 which is maintained thereby in condition to be operated during time period t_{140} of each steps 16 et seq. Resetting of flip-flop 140 during time period t_{140} of step 16 blocks gate 138 to prevent advance of step counter 136 preparatory to the next rotation of drum 123 and to prevent jumping of binary counter 126 from 178 to capacity (255) at that time. Therefore, the said counter advances to 179 preparatory to the said next rotation of drum 123 and remains at said count during said next rotation and until the next Ready pulse f occurs. While said counter stands at said count, pentode 226 (Fig. 1) disables the gates 214 and 218 through which information recorded on disc 232 is recirculated to effect precession, and the digits still to be printed, which are recorded on said disc, are not precessed.

When the printing mechanism reaches the point in its operation of printing the highest order digit, when the next digit can be set up in the flip-flops 272, the Ready switch 346 is operated and a Ready pulse f is produced. This pulse effects the same operations as attributed to the first Ready pulse but also effects an operation of puller 148 (Fig. 1) to set Go flip-flop 140. Preparatory to the next rotation of drum 123, therefore, the step counter 136 is advanced to 17 and the time period counter 126 is jumped to capacity to begin a cycle of operation in synchronism with said rotation. This causes pentode 226 to be cut off and precession of the digits recorded on disc 232 is effected. During time period t_{140} the g signal again is effective to reset the Go flip-flop 140 and the mode of operation described above in connection with step 16 is repeated.

The described mode of operation continues until step

24 when two digits are printed, instead of one, in order to reserve step 25 for printing of the decimal point.

The means whereby two digits are printed during step 24 include (Fig. 3) a flip-flop 360 and pentode pullers 362 and 364 for setting and resetting the same respectively. Integrating or delay circuits 366 and 368 couple the outputs of the flip-flop 360 which are high when the same is in the set and reset states, respectively, back to the "reset" and "set" pullers 364 and 362. Thus, the "set" puller 362 is operable only when the flip-flop is in the reset state while the "reset" puller 364 is operable only when the flip-flop is in the set state. The purpose of the integrators 366 and 368 is to prevent changes in the output potentials of the flip-flop due to a shift in the state of the latter from affecting the pullers 362 and 364 until after the said shift has been completed, and the same are designed accordingly. For example, said integrators may be identical with those designated 152 and 178 and described above.

The "set" puller 362 for flip-flop 360 is controlled by an inverter 370 which, in turn, is controlled by a coincidence gate 372 that is operable only during step 24. Gate 372 and "reset" puller 364 for the flip-flop are controlled in common by the differentiator 301 (Fig. 2) which applies a sharp positive pulse thereto when the inverter 297 which drives it is cut off following each operation of the relay timing means 296. On step 24, therefore, gate 372 conducts momentarily in response to a pulse from differentiator 301, and through the medium of the inverter 370, operates puller 362 which pulls flip-flop 360 to the set state (Fig. 4). It is assumed, of course, that flip-flop 360 was in the reset state prior to the occurrence of said pulse, with the puller 362 held enabled and the puller 364 held disabled by the feedback integrators 366 and 368 respectively. The next following pulse from differentiator 301, however, effects operation of the puller 364, and not the puller 362, and the flip-flop 360 is pulled back to the "reset" state (Fig. 4).

The output of the flip-flop 360 which is high when the same is in the "set" state is applied to the plate connected type gate 337 which, as described above, is used to produce the Ready pulses f for application to the Go circuit of Fig. 1. This connection maintains the output of said gate at a low potential as long as the flip-flop is in the "set" state. Therefore, as indicated in Fig. 4, no Ready pulse f is produced by the gate 337 during that portion of step 24 in which the flip-flop 360 is in the set state. The sequence of operations on step 24 is as follows. After the eighth from the highest order digit is printed during step 23, the Ready switch 346 is operated and Ready pulses f are generated by inverter 334 and gate 337 (see Fig. 4). The Ready pulse produced by gate 337 effects an advance of step counter 136 to 24 and initiates a cycle of operation of time period counter 126. The Ready pulse produced by inverter 334 effects setting up in the flip-flops 272 of the ninth from the highest order digit which was entered into the flip-flops 252 during time periods $t_{85}-t_{88}$ of step 23, and also effects an operation of the relay timing means 296 to energize the control relay 292. While the said relay is energized the relays 284 set up the digit to be printed in the translating unit 307 of the printing device through the medium of the solenoids 304. When the timing means 296 effects deenergization of the relay 292 it also cuts off the inverter 297 which, through the medium of the differentiator 301, applies a sharp positive pulse to gate 372. Inasmuch as it is step 24, said gate conducts and causes puller 362 to pull flip-flop 360 to the set state in which it prevents the gate 337 from producing a ready pulse f . Therefore, when the printing means has printed the ninth from the highest order digit and the Ready switch 346 is operated, a ready pulse f is produced by the inverter 334 for application to the relay timing means 296 and also to the pullers 270 for the flip-flops 272, but no Ready pulse f is produced by the gate 337 for the

application to the Go circuit of Fig. 1 to set the flip-flop 140. As a result, the step counter 136 is not advanced and the time period counter 126 remains at count 179.

The pullers 270 are enabled by the Ready pulse f applied thereto and transfer to the flip-flops 272 the settings of the flip-flops 252 which were effected during time periods $t_{85}-t_{88}$ of step 24 in accordance with the tenth highest order digit of the number to be printed. The Ready pulse also initiates an operation of the relay timing means 296, and the relay 292 is energized to permit the relays 284 to transfer the settings of the flip-flops 272 (tenth highest order digit) to the translating unit 307. However, owing to the fact that the timing pulses $t_{85}-t_{88}$ are not available, the pullers 250 are not operated to set the flip-flops 252 in accordance with the highest order post-decimal digit. When, at the appropriate time, the relay timing means 296 effects deenergization of the relay 292, it also cuts off the inverter 297, and differentiator 301 applies a sharp positive pulse to the puller 364 which pulls flip-flop 360 to the reset state (Fig. 4) in which it permits the gate 337 to produce a Ready pulse f for application to the Go circuit of Fig. 1. Therefore, when the printing unit has printed the tenth highest order digit and the Ready switch 346 is operated, the gate 337 is effective to produce a Ready pulse f which initiates an advance of step counter 136 to 25 and also a cycle of operation of time period counter 126.

It is desired that a decimal point be printed during step 25. To this end, an output of the flip-flop 360 (Fig. 3), which is low when the same is in the reset state, is applied to a differentiating circuit 380 (Fig. 2) that controls an inverter 382 whose output is applied to the pentode 262 described hereinabove. The other input to the pentode 262 is an output of the matrix 167 for step counter 136 which is high during step 24. When the flip-flop 360 is pulled to the reset state following the setting up of the tenth highest order digit in the translating unit 307 during step 24 (see Fig. 4), a sharp negatively directed pulse is applied to inverter 382 to cut off the latter and thereby to effect conduction of the pentode 262. Therefore, the output of the plate connected type gate which includes pentode 262, assumes a low potential and cuts off the inverter 256 which, it will be remembered, effects operation of the pullers 254 which pull the flip-flops 252 to their binary one states. These flip-flops remain in their binary one states until time periods $t_{85}-t_{88}$ of step 25, at which time the highest order post-decimal digit is set up therein. Before this time, however, the binary one settings of the flip-flops 252 are transferred to the flip-flops 272 to effect printing of the decimal point, as will be more fully described hereinafter.

In the Flexo-writer printer with which the means of the invention is herein associated, provisions are made for printing a variety of characters and symbols in addition to the digits 0-9 and the letters of the alphabet, and also for performing certain automatic operations such as "tabulate" and "space," all under control of the translator unit 307. Therefore, six solenoids 304 are provided to control the said translator 307 and the four relays 284 which are selectively operable under control of the flip-flops 272, each to effect energization of a said solenoid, are supplemented by a pair of relays 390 (Fig. 2) operable selectively to effect energization of the fifth and sixth solenoids. The relays 390 may be identical with the relays 284, and like the latter each is controlled by paralleled inverters 392. One pair of inverters 392 is controlled by a plate connected type gate 394 and the other pair is controlled by a similar gate 396. One triode of each gate 394 and 396 has the signal π' , which is low substantially all during printing operations, applied thereto. The other triode of gate 396 is controlled by a plate connected type gate 398 comprising one triode which conducts during step 25 and a second triode which is controlled by a flip-flop 400 to conduct only when the latter is in the reset state. Flip-flop 400 is pulled to

the set state by a puller 402 on the occurrence of the signal g which is applied thereto, and is pulled to the reset state by means to be described hereinafter, following printing of the lowest order digit of the number being printed.

It will be seen, therefore, that on step 25, and also when the flip-flop 400 is in the reset state, the gate 398 applies a low potential to gate 396 and the latter, in turn, applies a high potential to the paralleled inverters 392 which conduct and effect energization of the relay 390 associated therewith.

The sequence of operations involved in printing a decimal point during step 25 is as follows. After the relays 284 (Fig. 2) have been operated for the second time during step 24, to effect printing of the tenth highest order digit, the pullers 299 are operated to pull all of the flip-flops 272 to their binary one states. At the same time, puller 364 (Fig. 3) is operated to pull the flip-flop 360 to the "reset" state (Fig. 4), and differentiator 380 produces a pulse which through inverter 382, pentode 262 and inverter 256 operates the pullers 254 to pull the flip-flops 252 to their binary one states. Later, following printing of the said tenth highest order digit, the Ready switch 346 is operated and a Ready pulse f is produced to initiate step 25, to enable the pullers 270, and to actuate the relay timing means 296. Enabling of the pullers 270 is ineffective, of course, due to the binary one settings of the flip-flops 252, and the flip-flops 272 remain in their binary one states. As soon as step 25 is initiated, gate 398 produces a low output which, through the medium of gate 396, effects conduction of the associated, paralleled inverters 392. Thus, when the timing means 296 energizes the relay 292, all four of the relays 284 and also the relay 390 associated with gate 396 are energized and through the medium of the contacts 300 effect energization of the five associated solenoids 304. This combination of the solenoids 304 is the one which effects printing of a decimal point by the Flexo-writer and, therefore, the same is printed.

During time periods $t_{85}-t_{88}$ of step 25 the highest order post-decimal digit is set up in the flip-flops 252 for printing during step 26. Thereafter, the normal mode of operation of printing one digit per step continues until on step 35 the lowest order post-decimal digit, which was set up in the flip-flops 252 during step 34, is printed (Fig. 4); or, if the Stop Print switch 314 is set to halt printing at some other digit, on the appropriate other step. For purpose of description, it will be assumed that the switch 314 is set to effect printing of all ten decimal digits.

During time period t_0 of step 35, flip-flop 326 (Fig. 3) is set by puller 316 under control of Stop Print switch 314, and performs two functions, namely, it terminates the g signal (Fig. 4) by applying a high potential to the gate 330 which produces the same and it triggers a timing device 410 which may be of the same sort as the relay timing means 296, that is, a Phantastron. Termination of the g signal maintains pentode 332 in cutoff condition and the latter applies a high potential to the inverter 334 and the gate 337 to prevent production of Ready pulses f thereby. Also, referring to Fig. 1, absence of the g signal prevents the puller 164 from resetting the Go flip-flop 140 and the counter 136 returns to automatic operation and proceeds through step 36 and into step one of the next operation as indicated in Fig. 4.

In the illustrated instance of the invention the output of flip-flop 326 which assumes a low potential when the same is set by puller 316 is applied to the timing means 410 to trigger the same. However, if desired, the other output of the flip-flop may be utilized. The output of the timing means 410 (Fig. 3) is labeled PH_1 and is applied through a differentiator 411 to an inverter 412 whose output is connected with that of the inverter 334 through an isolating condenser 414. It will be noted that inverters 334 and 412, as connected, form an Or

gate, that is, when either is cut off a high potential is applied to the relay timing means 296 (Fig. 2) and also to the pullers 270. The purpose of the timing means 410 is to trigger the relay timing means 296 when the printing of the last digit has been completed. Therefore, said timing means 410 is adjusted to provide a positively directed output pulse which is of sufficient duration to span the printing period. The fall of this output pulse delivers a sharp negatively directed pulse to the inverter 412 which is cut off momentarily and thus applies a high pulse to the condenser 414 which, in turn, applies it to the relay timing means 296 to trigger the latter.

The reason for triggering the relay timing means 296 after the last digit of a number has been printed is to initiate an automatic, so-called "tabulate" operation wherein the paper carriage of the printing device is shifted to present some predetermined, unprinted area of the paper for printing during the next printing operation. In the Flexo-writer typewriter with which the invention is herein associated, a tabulating operation is accomplished by energizing all six of the solenoids 304 which control the translator 307. This, of course, requires that all six relays 284 and 390 be energized. The relays 284 are energized under control of the flip-flops 272 which were set to their binary one states to effect such energization by the pullers 299 following the operation of the relay timing means 296 during step 35. The means whereby the relays 390 are energized include the flip-flop 400 described above which, when in the reset state, applies a high potential to the plate connected type gate 398 to effect energization of the relay 390 associated therewith. The said output of the flip-flop is also applied to one triode of a plate connected type gate 420 (Fig. 2) which controls the other relay 390 through the gate 394 and the paralleled inverters 392 associated therewith. Gate 420 also includes a second triode, or if required, a pentode which may be controlled in any suitable way to effect energization of the associated relay 390 individually. For example, the same may be controlled in accordance with the algebraic signs of the numbers being printed, in which case, the associated relay, when operated singly, would effect an actuation of the translator 307 to print a negative sign or the like. The means whereby the flip-flop 400 is reset to effect energization of the relays 390 includes a puller 422 for the flip-flop, an inverter 424 which is cut off to operate the puller and a differentiator 426 controlled by the output PH₁ of the timing means 410 of Fig. 3 and adapted to apply a sharp, negatively directed pulse to the inverter 424 when the potential level of said output drops to effect triggering of the relay timing means 296.

Evidently, therefore, all of the relays 284 and 390 are energized when the relay timing means 296, after having been triggered by the timing means 410, effects energization of the control relay 292, and through the medium of the contacts 300 the six solenoids 304 are energized to accomplish a "tabulate" operation of the Flexo-writer.

In some instances, it is not desired to print the zeros to the left of the most significant digit of a number, but only to effect a "space" operation for each, except, possibly, when the most significant digit is located to the right of the decimal point, in which case it is desired to print one zero to the left of the decimal point and all of the zeros which follow the same. To this end, an output of each flip-flop 252 (Fig. 2) which is high when the same is in the binary one state is applied to a triode 440 of a plate connected type gate which also includes a triode 441 to which an output of the matrix 167 for step counter 136 which is high during step 24, is applied. The output of the gate 440, 441, which assumes a low potential during step 24, and also whenever one or more of the flip-flops 252 is in the binary one state, is applied

to an inverter 442 whose output, in turn, is applied to a pentode puller 444 which is operable only during time period t_{89} of each step. Puller 444 serves to reset a flip-flop 446 which is set by a pentode puller 448 during step 14 of each printing operation. Evidently, the flip-flop 446 which is set prior to entering the highest order digit of the number to be printed into the flip-flops 252 during time periods t_{85} – t_{88} of step 15 is not reset by puller 444 until on step 15, or a later step, a significant digit is entered into said flip-flops and one or more thereof are maintained in the binary one state during time period t_{89} ; or, until step 24 when the digit immediately to the left of the decimal point, which it is desired to print even though it is zero, the same as the digits to the right of the decimal point, is set up in the flip-flops 252. The output of flip-flop 446 which is high when the same is in the set state is applied through a manually operable switch 450 to the pentode 260 which also has an output of the matrix 130 for the time period counter 126 which is high during time period t_{105} , applied thereto. Thus, during time period t_{105} of each step prior to that in which the flip-flop 446 is reset, that is, until some digit other than zero is set up in the flip-flops 252 by the pullers 250, or, until step 24, pentode 260 conducts and applies a low potential to the inverter 256 which operates pullers 254₂, 254₄ and 254₈ but not the puller 254₁. Said puller 254₁, it will be remembered, is a pentode puller and is also controlled by the inverter 266 which is caused to conduct during time period t_{105} of each step. For convenience, a signal which is already available, namely that which is high during time periods t_{96} to t_{135} , is applied to the inverter 266. The purpose of the pentode puller 254₁ is to maintain flip-flop 254₁ in the binary zero state when the flip-flops 252₂, 252₄ and 252₈ are pulled to their binary one states under control of pentode 260, thus setting up the code which initiates a "space" operation without printing in the Flexo-writer typewriter. Therefore, when the said setting of the flip-flops 252 is transferred to the flip-flops 272, and thereby to the relays 284 and the solenoids 304, the typewriter accomplishes a "space" operation rather than printing zero.

Of course, as soon as the flip-flop 446 is reset in response to the setting up of a significant digit in the flip-flops 252, or on the occurrence of step 24, printing is begun.

The purpose of the switch 450 is to disable the zero suppression means if desired. To this end the switch is adapted to connect the input to the pentode 260 either with the appropriate output of flip-flop 446, or with a source of negative potential, say –20 volts.

It will be seen therefore, that there has been described control means for operating a serial type printing device in accordance with the digital output of an electronic computer and for automatically causing the said printing machine to perform the functions of "tabulate" and "space." In addition, the said means also are capable of being controlled manually to effect suppression of the zeros and also to drop desired numbers of digits from either end of a number to be printed.

The above description has been limited to the control of a serial type printing device. It is believed evident, however, that the means described are equally well adapted for use with a serial type paper tape perforator or a magnetic tape recording device, or with a serial type card punching machine. In short, the relays 284 and 390 may be used to control any desired kind of serial data recording device.

While there has been above described but a single embodiment of the invention, it is to be understood that many changes and modifications can be made therein without departing from the spirit of the invention, and it is not desired, therefore, to limit the scope of the invention except as pointed out in the appended claims or as dictated by the prior art.

We claim:

1. A system for serially indicating a number consisting of a series of digits recorded in coded form on a cyclically operating storage device comprising, a plurality of first flip-flops for receiving representations of the recorded digits from said storage device, one digit at a time, a digit indicating device, a plurality of second flip-flops each associated with a said first flip-flop for controlling said digit indicating device, timing means cyclically operated in synchronism with said storage device, first gating means enabled by said timing means to set said first flip-flops to represent a digit recorded on said storage device, means for precessing the number recorded on said storage device to apply representations of successive digits of said number to said first gating means, second gating means to set said second flip-flops in accordance with the setting of said first flip-flops, means for selecting the first digit to be indicated, means for producing a start signal when the first digit to be indicated is available in said first flip-flops, said start signal enabling said second gating means and disabling continued operation of said timing means, said digit indicating device producing a ready signal when said indicating device thereafter is conditioned for control by said second flip-flops, said ready signal enabling said second gating means and enabling said timing means for one cycle of operation.

2. The combination according to claim 1 and including a plurality of relays, each energizable under control of one of said second flip-flops, for controlling the indicating device, a control relay connected with the said relays to permit energization of the latter only when the former is energized, means triggered by each ready signal to effect energization of said control relay for a predetermined period of time, and means for setting all of the second flip-flops to a given state on deenergization of said control relay, and means controlled by said timing means for setting all of said first flip-flops to a given state prior to each operation of the timing means to set said first flip-flops to represent a digit.

3. A system according to claim 2 wherein the timing means includes a source of pulses operating in synchronism with the recordings on said storage device, a counter receiving pulses from said source, means controlled by said counter for producing timing signals, means controlled by said timing signals to enable the precessing means and said first gating means, a control flip-flop settable to one state to block application of pulses to said counter, said ready signal triggering said control flip-flop to the opposite state to permit application of pulses to said counter, and means actuated by said timing signals to set said control flip-flop to said one state.

4. A system according to claim 3 including a step counter advanced one count for each cycle of operation of said first mentioned counter, means for producing signals indicative of the count of said step counter, a start flip-flop set to one state under the control of said step counter signal producing means preparatory to indicating the first digit-to-be-indicated of a number, a stop flip-flop set to one state under control of said step counter signal producing means preparatory to indicating the last

digit-to-be-indicated of a number, means for resetting said start and stop flip-flops before the first digit of a number is presented to said first flip-flops operating under the control of said step counter signal producing means, gating means controlled by said start and stop flip-flops to effect setting of said control flip-flop by said ready signal only when said start flip-flop is in the set state and said stop flip-flop is in the reset state.

5. A system according to claim 4 including gating means for said ready signal for blocking said ready signal from triggering said control flip-flop to its opposite state, a further flip-flop set to enable said ready signal gating means to block said ready signal, gating means controlled by a predetermined signal from said step counter signal producing means to set said further flip-flop on deenergization of the control relay and to reset said further flip-flop on deenergization of the control relay when said further flip-flop is in a set state, means actuated on resetting of said further flip-flop for setting a first flip-flop to a given state, and an additional relay controlling the indicating device energizable only when said control relay is energized enabled for operation by said predetermined signal from said step counter signal producing means.

6. A system according to claim 5 including a zero control flip-flop set to one state prior to the setting of said first flip-flops to represent the first digit of a number for effecting operation of said means for setting all of said first flip-flops to a given state, means for blocking the setting of one of said first flip-flops to said given state and means controlled by said timing signals for resetting said zero control flip-flop when said first flip-flops represents a digit other than zero or when said predetermined signal from said step counter signal producing means is present.

7. A system according to claim 2 including means for triggering said control relay energization means, means triggered when the last-to-be-indicated digit of a number is transferred to said second flip-flops for operating said control relay energization means after a predetermined delay, a pair of additional relays controlling said indicating device energizable only when said control relay is energized, and a flip-flop set in one state after said time delay by said control relay energization triggering means enabling said additional relays.

8. A system according to claim 6 and including a switch settable to prevent operation by the zero control flip-flop of the means for setting all of the first mentioned flip-flops to a given state.

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