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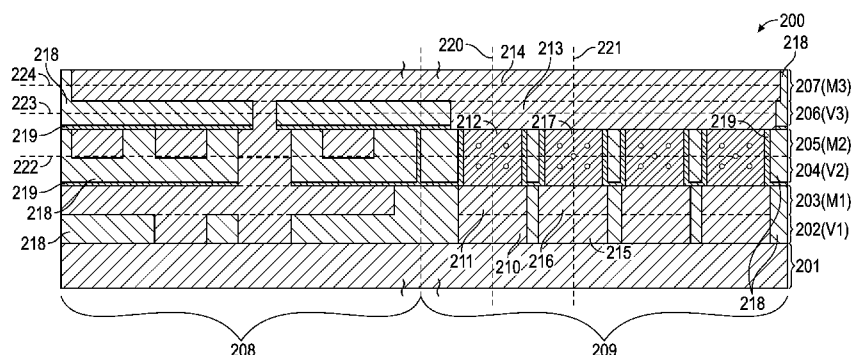


FIG. 3

(57) Abstract: An embodiment includes an apparatus comprising: a first via layer between a substrate and a first metal layer; a second via layer between the first metal layer and second metal layer; a third via layer between the second metal layer and a third metal layer; and first and second access transistors each included in the substrate; wherein (a) the second via layer and the second metal layer each include portions of a first magnetic tunnel junction (MTJ) and portions of a second MTJ, (b) the third via layer includes a metal interconnect directly contacting the first and second MTJs, and (c) the third metal layer includes a bit line that couples to the first and second access transistors through the metal interconnect and the first and second MTJs. Other embodiments are described herein.

MEMORY WITH HIGH OVERLAY TOLERANCE

Technical Field

[0001] Embodiments of the invention are in the field of semiconductor devices and, in particular, memory.

Background

[0002] Some magnetic memories, such as a spin transfer torque magnetic random access memory (STT-MRAM), utilize a magnetic tunnel junction (MTJ) for switching and detection of the memory's magnetic state. A MTJ consists of ferromagnetic (FM) layers and a tunneling barrier (e.g., MgO). The MTJ couples a bit line (BL) to selection switch (e.g., transistor), word line (WL), and sense line (SL). The MTJ memory is "read" by assessing the change of resistance (e.g., tunneling magnetoresistance (TMR)) for different relative magnetizations of the FM layers.

[0003] More specifically, in STT-MRAM each bit of data is stored in a separate MTJ. One of the FM layers is called the reference layer (RL), and it provides a stable reference magnetic orientation. The bit is stored in the second FM layer, which is called the free layer (FL), and the orientation of the magnetic moment of the free layer can be, for example, in either of two states: parallel to the reference layer or anti-parallel to the reference layer. Because of the TMR effect, the electrical resistance of the anti-parallel state is significantly higher compared to the parallel state.

[0004] To write information in a STT-MRAM device, the spin transfer torque (STT) effect is used to switch the free layer from the parallel to anti-parallel state and vice versa. The passing of current through the MTJ produces spin polarized current, which results in a torque being applied to the magnetization of the free layer. When the spin polarized current is sufficiently strong, enough torque is applied to the free layer to cause its magnetic orientation to change, thus allowing for bits to be written. To read the stored bit, the sensing circuitry measures the resistance of the MTJ.

Brief Description of the Drawings

[0005] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures, in which:

Figure 1 depicts a memory array in an embodiment of the invention;

Figure 2 depicts a memory array in an embodiment of the invention;

Figure 3 depicts a memory array stack in an embodiment of the invention;

Figures 4 and 5 each depict a top view of a memory array stack in an embodiment of the invention;

Figures 6A-6F include a method in an embodiment of the invention; and

Figure 7 depicts a system for use with embodiments of the invention.

Detailed Description

[0006] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of integrated circuit structures. Thus, the actual appearance of the fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. “An embodiment”, “various embodiments” and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. “First”, “second”, “third” and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. “Connected” may indicate elements are

in direct physical or electrical contact with each other and “coupled” may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact. Also, while similar or same numbers may be used to designate same or similar parts in different figures, doing so does not mean all figures including similar or same numbers constitute a single or same embodiment. Terms such as “upper” and “lower” “above” and “below” may be understood by reference to the illustrated X-Z coordinates, and terms such as “adjacent” may be understood by reference to X-Y coordinates or to non-Z coordinates.

[0007] Once semiconductor wafers are prepared, a large number of process steps are still necessary to produce desired semiconductor integrated circuits. In general the steps can be grouped into four areas: Front End Processing, Back End Processing, Test, and Packaging.

[0008] Front End Processing refers to the initial steps in the fabrication. In this stage the actual semiconductor devices (e.g., transistors) are created. A typical front end (also referred to herein as “frontend”) process includes: preparation of the wafer surface, patterning and subsequent implantation of dopants to obtain desired electrical properties, growth or deposition of a gate dielectric, and growth or deposition of insulating materials to isolate neighboring devices.

[0009] Once the semiconductor devices have been created they must be interconnected to form the desired electrical circuits. This “Back End Processing” (BEOL) of the back end (also referred to herein as “backend”) involves depositing various layers of metal (sometimes referred to herein as M layers used to form traces, BL, WL, and the like) and insulating material (sometimes referred to herein as V layers because such layers often include vias) in the desired pattern. Typically the metal layers consist of aluminum, copper, and the like. The insulating material may include SiO₂, low-K materials, and the like. The various metal layers are interconnected by etching holes, called “vias”, in the insulating material and depositing metal (e.g., Tungsten) in them. Thus, a backend portion may include, for example, 12 metal layers: a bottom metal layer (M0), a top metal layer (M11), and a plurality of metal layers (M1, M2, M3, M4, M5, M6, M7, M8, M9, and/or M10) between the bottom and top metal layers. The “bottom metal layer” is so named

because the backend portion includes no metal layer between the bottom metal layer and a top of the frontend portion. The “top metal layer” is so named because the backend portion includes no metal layer between the top metal layer and the top of the backend portion. Having 12 metal layers is just an example and backend portions may include more (e.g., 14, 16, 18, 20 or more) or less (e.g., 4, 6, 8) metal layers.

[0010] Once the Back End Processing has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. Finally, the wafer is cut into individual die, which are then packaged in packages (e.g., ceramic or plastic packages) with pins or other connectors to other circuits, power sources, and the like.

[0011] The various M layers and insulative layers must be aligned over each other. However, sometimes any of the various layers may not align properly with each other. As scaling is intensified, the margin of error for misalignment decreases. For example, it may be difficult to align an aggressively scaled MTJ in a V layer with an overlying M layer. However, an embodiment of the invention addresses these types of scaling issues.

[0012] Figure 1 includes a memory array 100 in an embodiment of the invention. Array 100 includes MTJs 112, 117. MTJ 112 consists of FM layers 142, 144 (one of which is a free layer such as, for example, layer 144, and the other of which is a reference layer) and a tunneling barrier 143 (e.g., MgO). MTJ 112 couples BL 114 to selection switch 134 (e.g., transistor), WL 132 (through gate node 133), and SL 135 (through a switch node 136, such as a drain or source node). MTJ 117 consists of FM layers 145, 147 (one of which is a free layer such as, for example, layer 147, and the other of which is a reference layer) and tunneling barrier 146 (e.g., MgO). MTJ 117 couples BL 114 to selection switch 139 (e.g., transistor), WL 137 (through gate node 138), and SL 135 (through a switch node 141, such as a drain or source node).

[0013] MTJs 112, 117 both couple to BL 114 through or by way of “MTJ via bus bar” 113. In an embodiment, bar 113 is a single monolithic interconnect that couples a row or series of MTJs to a bit line, rather than including a separate interconnect for

each MTJ that needs to couple to a BL as is found in conventional arrays. This is important as MTJs continue to scale smaller, meaning properly aligning an overlaying M layer (which itself is continuing to scale smaller) with the small MTJs is becoming increasingly difficult as both MTJs and M layer lines (e.g., BL) aggressively scale smaller. Using the bus bar 113 helps achieve a higher tolerance for mismatch between the V layer that includes the interconnects for the MTJs (and/or portions of the MTJs themselves) and the overlying or underlying M layer.

[0014] The embodiment of Figure 1 may further include individual interconnects 111, 116 (e.g., electrodes or contacts) to couple MTJs 112, 117 to switches 134, 139. In that sense, interconnects 111, 116 are similar to the individual interconnects conventionally used to couple MTJs to a BL. Reading and writing to the MTJs occurs in a manner similar to method described above. In other words, an entire row of MTJs may receive a signal from BL 114. However, only the column whose WL is activated will make the MTJ accessible. For example, MTJ 112 may be read or written to while WL 132 is selected and MTJ 117 will not be read or written to when WL 137 is not selected.

[0015] Figure 2 includes a memory array similar to the array of Figure 1, and therefore like components include similar numbers (e.g., SL 135 is the same in each array so it maintains the same number). However, the embodiment of Figure 2 provides for another embodiment that may include a second BL 130. Thus, BL 114 may be reserved for reads of the MTJs while BL 130 is reserved for writes of the MTJs. An analogous concept is addressed in PCT Patent Application Publication Number WO 2014/204492 assigned to Intel Corp. of Santa Clara, California, USA.

[0016] Figure 3 includes a memory array in an embodiment of the invention. Array 200 includes a via layer 202 (V1) between a substrate 201 and a metal layer 203 (M1); a via layer 204 (V2) between the metal layer 203 and metal layer 205 (M2); a via layer 206 (V3) between the metal layer 205 and a metal layer 207 (M3). Array 200 further includes first and second access transistors (not shown but analogous to switches 134, 139 of Figure 1) each included in the substrate 201. The V2 via layer and the M2 metal layer each include portions of MTJ 212 and portions of MTJ 217. For example, one or two layers of a MTJ may be in the V2 layer while other layers of

the same MTJ may be in the M2 layer and/or some additional V and M layers located between the M2 and V3 layers. The V3 layer includes a metal interconnect 213 (sometimes referred to as "via bus bar") directly contacting the MTJs 212, 217. The M3 layer includes bit line 214 that couples to the first and second access transistors through the metal interconnect 213 and MTJs 212, 217. In an embodiment the M1 metal layer includes an additional metal interconnect 211 that directly contacts MTJ 212 but not MTJ 217 and the bit line 214 couples to the first access transistor through the additional interconnect 211. Also, array 200 includes etch stop (e.g., SiN) 219 and interlayer dielectric (ILD) 218. In addition, contacts 211, 216 couple to substrate 201 through vias 210, 215.

[0017] In an embodiment vertical axis 220 intersects the MTJ 212 and metal interconnect 213 and vertical axis 221 intersects the MTJ 217 and metal interconnect 213.

[0018] In an embodiment, metal interconnect 213 is monolithic. In other words, interconnect 213 is formed as a single unit or piece.

[0019] In an embodiment horizontal axis 222 intersects MTJs 212, 217 but not metal interconnect 213. Vertical axes 220, 221 both intersect bit line 214.

[0020] In an embodiment, bit line 214 directly contacts metal interconnect 213 but other embodiments do not have direct contact but instead provide indirect contact (e.g., through a via or other interconnect).

[0021] As mentioned above, the M and V layers need not be arranged strictly as shown in figures such as Figure 3. For example, the sequence and/or naming of metal and via layers may change from that of Figure 3. Specifically, in Figure 3 layer 205 may be referred to as Metal N (where $N = 2$) and layer 204 may be referred to as Via (N-1) such that M2 is above V1.

[0022] As seen in Figures 4 and 5, MTJs 212, 217 are generally located collinearly with each other along the horizontal axis 222 and the bit line 214 is generally located along horizontal axis 224. In Figure 4, when M3, M2, and V2 layers are aligned axes 222, 224 are collinear and parallel with each other. However, in Figure 5 when M3, M2, and V2 layers are not aligned axes 222, 224 are not collinear and not parallel

with each other. In Figure 4, the metal interconnect 213 is generally located along a horizontal axis 223 that is parallel with horizontal axis 222 and is parallel with horizontal axis 224. In Figure 5, the metal interconnect 213 is generally located along horizontal axis 223 that is parallel with horizontal axis 222 and is not parallel with horizontal axis 224. As can be seen in Figure 5, good electrical connectivity between the MTJ top electrodes and the M3 is maintained with the disclosed array structure with the “MTJ Via Busbar” feature even when the M2 and MTJs are severely misaligned with M3.

[0023] In the embodiment of Figure 3, the V1 layer directly contacts M1 metal layer, via layer V2 directly contacts the M1 and M2 metal layers, and V3 via layer directly contacts M3 metal layer. However, in other embodiments there may be an additional via layer, located between the M1 metal layer and the V2 via layer, which includes an additional metal interconnect directly contacting the first and second MTJs.

[0024] As a general matter, M3 is the top metal layer shown in the example of Figure 3. However, that is not implying that M3 is the top layer in general or that there is no metal above M3. Instead, an embodiment may include a “top metal layer” that is topmost of not all layers or any layer with metal but of the “metal layers” as those of ordinary skill in the art would construe that term. That top metal layer may be M3 or may be M11 or some other layer not shown in Figure 3. In other words, the “top metal layer” in the context addressed herein is a top interconnect metal layer that includes dielectric material. The top metal layer may include a top damascene formed interconnect layer that includes dielectric material. This top metal layer is formed using an interconnect formation process performed in a semiconductor fabrication (FAB) facility. Layers above this “top metal layer” are classified as part of Far BEOL wiring layers (e.g., typified by layers supported at outsourced assembly and test (OSAT) houses, not FABs). Also, while M3 is shown as including BL please note M3 may only be the third M layer shown in Figure 3. In other words, there may be metal layers M4, M5 that are between M1 and M2 layers so purposes of this application embodiments are not limited to placing a BL or MTJ in any particular M layer.

[0025] In the embodiment of Figure 3, the M1 metal layer includes metal interconnect 216 that directly contacts MTJ 217 but not MTJ 212, and bit line 214 couples to the second access transistor through the metal interconnect 216 but not the interconnect 211. Other embodiments are not so limited.

[0026] In the embodiment of Figure 3 the bit line 214 directly contacts the metal interconnect 213. In other words, bit line 214 directly contacts the metal interconnect 213 with no via between the bit line and the metal interconnect.

[0027] In an embodiment an additional BL (not shown but analogous to BL 130 of Figure 1) couples to the metal interconnect 211.

[0028] In the embodiment of Figure 3 a system on a chip (SoC) includes embedded memory that comprises memory array 200. The SoC may include logic portion 208 (e.g., a processor or controller) and array portion 209 with the array serving as embedded memory.

[0029] In an embodiment, a word line couples to a gate node of access transistor and a sense line coupled to node of the access transistor. A word line is coupled to a gate node of the access transistor and sense line is coupled to node of the access transistor.

[0030] In an embodiment, the backend portion is coupled to a plurality of contact bumps, such as Controlled Collapse Chip Connection ('C4') bumps.

[0031] Access transistors including, for example, switches 134, 139, may be FinFETs. A FinFET is a transistor built around a thin strip of semiconductor material (referred to as the "fin"). The transistor includes the standard field effect transistor (FET) nodes/components: a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both "sidewalls" of the fin as well as along the top side of the fin. Because the conductive channel essentially resides along the three different outer, planar regions of the fin, such a FinFET is typically referred to as a "tri-gate" FinFET. Other types of FinFETs exist (such as "double-gate" FinFETs in which the conductive channel principally resides only along both sidewalls of the fin and not along the top side of the fin).

[0032] Various embodiments disclosed herein have addressed MTJs. Such MTJs include perpendicular MTJs. Further, the STT memory cells addressed herein may couple to a sense amplifier.

[0033] Thus, embodiments address herein disclose a STT-MRAM array structure with a special “MTJ Via busbar” that provides a greatly increased overlay tolerance compared to prior art STT-MRAM arrays. In an embodiment the bus bar electrically connects the top electrodes of rows of MTJs and the bus bar is connected directly to one or more above metal interconnect wires. This is in contrast to conventional systems where the top electrode of each individual MTJ is electrically connected to the interconnect wiring above it by way of an individual via. Providing better overlay tolerance leads to better die yield which translates directly into reduced costs.

[0034] Figures 6A-6F include a method in an embodiment of the invention.

[0035] Figure 6a addresses the process after conventional methods are used to form layers 201, 202, 203, 204, 205, MTJs 212, 217, ILD 218, and etch stop 219 in a SoC with logic 208 and embedded memory 209 portions as described above with regard to Figure 3. The fabrication method begins with substrate 201 that may have completed transistor fins, transistor gates, contacts, and interconnect layer(s), as is well-known in the art. On top of the substrate are layers that cover both the memory array area and logic area of the die. For example, layer M1 may include interconnects for both logic and memory.

[0036] In Figure 6B ILD is formed in layer 206 and then resist 207 is formed and patterned in layer 207. The patterning is to form a void where the via bus bar will be formed. More specifically, additional etch stop is deposited onto the wafer surface, followed by ILD in layer 206. The etch stop material may consist of silicon nitride, silicon carbide, or silicon oxynitride. The dielectric material may consist of a silicon dioxide, silicon nitride, fluorinated silicon oxide (SiOF), borophosphosilicate glass (BPSG), or a low k dielectric (e.g., $k < 3$) such as carbon-doped oxide (CDO). Photoresist 207' is applied to the wafer surface and patterned. After patterning there are holes in the photoresist layer where “MTJ Via Busbars” are desired. The photoresist layer may consist not only of photoresist material, but also may include

other patterning materials such as anti-reflective coatings (ARCs) and gap-fill and planarizing materials that are applied using methods and techniques that are well-known in the art, and an underlying metallization hardmask material may also be present to aid in the subsequent transfer of the resist patterned to the underlying ILD in the next step, as is well-known in the art.

[0037] In Figure 6C anisotropic dry etch processes are used to transfer the MTJ Via bus bar resist pattern into the dielectric layer and etchstop layer. Any remaining resist is removed using a plasma ash process and any remaining etch polymer or residue is removed using wet cleans processes that are well-known in the art.

[0038] In Figure 6D a conductive metal such as copper, tungsten or cobalt is deposited onto the entire wafer surface, filling into the source line trenches and source line via openings. Various barrier or adhesion films may be present at the interface between the conductive metal and the surrounding dielectric, such as titanium, tantalum, titanium nitride, tantalum nitride, ruthenium, titanium-zirconium nitride, cobalt, etc., as is known in the art. The conductive metal overburden is then etched back using wet etch, dry etch and/or CMP processes that are well known in the art, leaving patterned MTJ Via Busbar features embedded in the ILD. More ILD 218' is deposited onto the wafer surface. The dielectric material may consist of a silicon dioxide, silicon nitride, fluorinated silicon oxide (SiOF), borophosphosilicate glass (BPSG), or a low k dielectric (e.g., $k < 3$) such as carbon-doped oxide (CDO), and may or may not be the same material as the ILD material deposited in Figure 6B.

[0039] In Figure 6E photoresist 207' is applied to the wafer surface and patterned. After patterning there are holes in the photoresist layer where M4 interconnect lines are desired. The photoresist layer may consist not only of photoresist material, but also may include other patterning materials such as ARCs and gap-fill and planarizing materials that are applied using methods and techniques that are well-known in the art, and an underlying metallization hardmask material may also be present to aid in the subsequent transfer of the resist patterned to the underlying ILD in the next step, as is well-known in the art. Anisotropic dry etch processes are then used to transfer the M4 resist pattern into the dielectric layer.

[0040] In Figure 6F any remaining resist is removed using a plasma ash process and any remaining etch polymer or residue is removed using wet cleans processes that are well-known in the art. Photoresist 207' is applied to the wafer surface and patterned. After patterning there are holes in the photoresist layer where vias in the V3 layer are desired. The photoresist layer may consist not only of photoresist material, but also may include other patterning materials such as ARC and gap-fill and planarizing materials that are applied using methods and techniques that are well-known in the art, and an underlying metallization hardmask material may also be present to aid in the subsequent transfer of the resist patterned to the underlying ILD in the next step, as is well-known in the art.

[0041] Anisotropic dry etch processes are then used to transfer the V3 resist pattern into the dielectric layer and etchstop layer. Any remaining resist is removed using a plasma ash process and any remaining etch polymer or residue is removed using wet cleans processes that are well-known in the art. A conductive metal such as copper, tungsten or cobalt is deposited onto the entire wafer surface, filling into the source line trenches and source line via openings to yield the embodiment of Figure 3. Various barrier or adhesion films may be present at the interface between the conductive metal and the surrounding dielectric, such as titanium, tantalum, titanium nitride, tantalum nitride, ruthenium, titanium-zirconium nitride, cobalt, as is known in the art. The conductive metal overburden is then etched back using wet etch, dry etch and/or CMP processes that are well known in the art, leaving patterned M4/V3 features embedded in the ILD.

[0042] Figure 7 includes a system that may include any of the above described embodiments. Figure 7 includes a block diagram of a system embodiment 1000 in accordance with an embodiment of the present invention. System 1000 may include hundreds or thousands of the above described memory cells and be critical to memory functions in system 1000. System 1000 may be included in, for example, a mobile computing node such as a cellular phone, smartphone, tablet, Ultrabook®, notebook, laptop, personal digital assistant, and mobile processor based platform. The stability and power efficiency of such memory cells accumulates when the memory cells are deployed in mass and provides significant performance

advantages (e.g., longer battery life, longer memory state storage in a broader range of operating temperatures) to such computing nodes.

[0043] Shown is a multiprocessor system 1000 that includes a first processing element 1070 and a second processing element 1080. While two processing elements 1070 and 1080 are shown, it is to be understood that an embodiment of system 1000 may also include only one such processing element. System 1000 is illustrated as a point-to-point interconnect system, wherein the first processing element 1070 and second processing element 1080 are coupled via a point-to-point interconnect 1050. It should be understood that any or all of the interconnects illustrated may be implemented as a multi-drop bus rather than point-to-point interconnect. As shown, each of processing elements 1070 and 1080 may be multicore processors, including first and second processor cores (i.e., processor cores 1074a and 1074b and processor cores 1084a and 1084b). Such cores 1074, 1074b, 1084a, 1084b may be configured to execute instruction code.

[0044] Each processing element 1070, 1080 may include at least one shared cache or memory unit which may include pMTJs and/ or MTJs described herein (e.g., MTJs may be in embedded memory). The shared cache may store data (e.g., instructions) that are utilized by one or more components of the processor, such as the cores 1074a, 1074b and 1084a, 1084b, respectively. For example, the shared cache may locally cache data stored in a memory 1032, 1034 for faster access by components of the processor. In one or more embodiments, the shared cache may include one or more mid-level caches, such as level 2 (L2), level 3 (L3), level 4 (L4), or other levels of cache, a last level cache (LLC), and/or combinations thereof.

[0045] While shown with only two processing elements 1070, 1080, it is to be understood that the scope of the present invention is not so limited. In other embodiments, one or more additional processing elements may be present in a given processor. Alternatively, one or more of processing elements 1070, 1080 may be an element other than a processor, such as an accelerator or a field programmable gate array. For example, additional processing element(s) may include additional processors(s) that are the same as a first processor 1070, additional processor(s) that are heterogeneous or asymmetric to first processor

1070, accelerators (such as, e.g., graphics accelerators or digital signal processing (DSP) units), field programmable gate arrays, or any other processing element.

There can be a variety of differences between the processing elements 1070, 1080 in terms of a spectrum of metrics of merit including architectural, microarchitectural, thermal, power consumption characteristics, and the like. These differences may effectively manifest themselves as asymmetry and heterogeneity amongst the processing elements 1070, 1080. For at least one embodiment, the various processing elements 1070, 1080 may reside in the same die package.

[0046] First processing element 1070 may further include memory controller logic (MC) 1072 and point-to-point (P-P) interfaces 1076 and 1078. Similarly, second processing element 1080 may include a MC 1082 and P-P interfaces 1086 and 1088. MCs 1072 and 1082 couple the processors to respective memories, namely a memory 1032 and a memory 1034, which may be portions of main memory locally attached to the respective processors. Memory 1032, 1034 may include MTJs/pMTJs described herein. While MC logic 1072 and 1082 is illustrated as integrated into the processing elements 1070, 1080, for alternative embodiments the MC logic may be discrete logic outside the processing elements 1070, 1080 rather than integrated therein.

[0047] First processing element 1070 and second processing element 1080 may be coupled to an I/O subsystem 1090 via P-P interfaces 1076, 1086 via P-P interconnects 1062, 10104, respectively. As shown, I/O subsystem 1090 includes P-P interfaces 1094 and 1098. Furthermore, I/O subsystem 1090 includes an interface 1092 to couple I/O subsystem 1090 with a high performance graphics engine 1038. In one embodiment, a bus may be used to couple graphics engine 1038 to I/O subsystem 1090. Alternately, a point-to-point interconnect 1039 may couple these components.

[0048] In turn, I/O subsystem 1090 may be coupled to a first bus 10110 via an interface 1096. In one embodiment, first bus 10110 may be a Peripheral Component Interconnect (PCI) bus, or a bus such as a PCI Express bus or another third generation I/O interconnect bus, although the scope of the present invention is not so limited.

[0049] As shown, various I/O devices 1014, 1024 may be coupled to first bus 10110, along with a bus bridge 1018 which may couple first bus 10110 to a second bus 1020. In one embodiment, second bus 1020 may be a low pin count (LPC) bus. Various devices may be coupled to second bus 1020 including, for example, a keyboard/mouse 1022, communication device(s) 1026 (which may in turn be in communication with a computer network), and a data storage unit 1028 such as a disk drive or other mass storage device which may include code 1030, in one embodiment. The code 1030 may include instructions for performing embodiments of one or more of the methods described above. Further, an audio I/O 1024 may be coupled to second bus 1020.

[0050] Note that other embodiments are contemplated. For example, instead of the point-to-point architecture shown, a system may implement a multi-drop bus or another such communication topology. Also, the elements of Figure 7 may alternatively be partitioned using more or fewer integrated chips than shown in the Figure 7. For example, a field programmable gate array may share a single wafer with a processor element and memory including MTJs described herein.

[0051] Various embodiments addressed herein include a semiconductive substrate. Such a substrate may be a bulk semiconductive material that is part of a wafer. In an embodiment, the semiconductive substrate is a bulk semiconductive material as part of a chip that has been singulated from a wafer. In an embodiment, the semiconductive substrate is a semiconductive material that is formed above an insulator such as a semiconductor on insulator (SOI) substrate. In an embodiment, the semiconductive substrate is a prominent structure such as a fin that extends above a bulk semiconductive material.

[0052] The following examples pertain to further embodiments.

[0053] Example 1 includes an apparatus comprising: a first via layer between a substrate and a first metal layer; a second via layer between the first metal layer and second metal layer; a third via layer between the second metal layer and a third metal layer; and first and second access transistors each included in the substrate; wherein (a) the second via layer and the second metal layer each include portions of

a first magnetic tunnel junction (MTJ) and portions of a second MTJ, (b) the third via layer includes a metal interconnect directly contacting the first and second MTJs, and (c) the third metal layer includes a bit line that couples to the first and second access transistors through the metal interconnect and the first and second MTJs.

[0054] In example 2 the subject matter of the Example 1 can optionally include (a) the first metal layer includes an additional metal interconnect that directly contacts the first MTJ but not the second MTJ, and (b) the bit line couples to the first access transistor through the additional interconnect.

[0055] In example 3 the subject matter of the Examples 1-2 can optionally include wherein a first vertical axis intersects the first MTJ and the metal interconnect and a second vertical axis intersects the second MTJ and the metal interconnect.

[0056] In example 4 the subject matter of the Examples 1-3 can optionally include wherein the metal interconnect is monolithic.

[0057] In example 5 the subject matter of the Examples 1-4 can optionally include wherein a first horizontal axis intersects the first and second MTJs but not the metal interconnect.

[0058] In example 6 the subject matter of the Examples 1-5 can optionally include wherein the first and second vertical axes both intersect the bit line.

[0059] In example 7 the subject matter of the Examples 1-6 can optionally include wherein the bit line directly contacts the metal interconnect.

[0060] In example 8 the subject matter of the Examples 1-7 can optionally include wherein the first and second MTJs are generally located collinearly with each other along the first horizontal axis and the bit line is generally located along a second horizontal axis that is not parallel with the first horizontal axis.

[0061] In example 9 the subject matter of the Examples 1-8 can optionally include wherein the metal interconnect is generally located along a third horizontal axis that is parallel with the first horizontal axis and is not parallel with the second horizontal axis.

[0062] In example 10 the subject matter of the Examples 1-9 can optionally include wherein the first via layer directly contacts the first metal layer, the second via layer directly contacts the second metal layer, and the third via layer directly contacts the third metal layer.

[0063] In example 11 the subject matter of the Examples 1-10 can optionally include wherein (a) the first metal layer includes another metal interconnect that directly contacts the second MTJ but not the first MTJ, and (b) the bit line couples to the second access transistor through the another metal interconnect but not the additional interconnect.

[0064] In example 12 the subject matter of the Examples 1-11 can optionally include wherein the bit line directly contacts the metal interconnect with no via between the bit line and the metal interconnect.

[0065] In example 13 the subject matter of the Examples 1-12 can optionally include an additional bit line that couples to the additional metal interconnect.

[0066] In example 14 the subject matter of the Examples 1-13 can optionally include a system on a chip with embedded memory including a memory array comprising the first and second MTJs and the metal interconnect.

[0067] In example 15 the subject matter of the Examples 1-14 can optionally include a first word line coupled to a gate node of the first access transistor and a first sense line coupled to another node of the first access transistor; and a second word line coupled to a gate node of the second access transistor and at least one of the first sense line and a second sense line coupled to another node of the second access transistor.

[0068] Example 16 includes an apparatus comprising: a first via layer between a substrate and a first metal layer; a second via layer between the first metal layer and second metal layer; and a third via layer between the second metal layer and a third metal layer; wherein (a) the second metal layer includes portions of a first magnetic tunnel junction (MTJ) and portions of a second MTJ, (b) the third via layer includes a metal interconnect directly contacting the first and second MTJs, and (c) the third metal layer includes a bit line.

[0069] In example 17 the subject matter of the Example 16 can optionally include wherein (a) the first metal layer includes an additional metal interconnect that directly contacts the first MTJ but not the second MTJ, and (b) the bit line couples to a first access transistor through the additional metal interconnect.

[0070] In example 18 the subject matter of the Examples 16-17 can optionally include wherein a first vertical axis intersects the first MTJ and the metal interconnect and a second vertical axis intersects the second MTJ and the metal interconnect.

[0071] In example 19 the subject matter of the Examples 16-18 can optionally include wherein the first and second vertical axes both intersect the bit line.

[0072] In example 20 the subject matter of the Examples 16-19 can optionally include wherein the bit line directly contacts the metal interconnect.

[0073] Example 21 includes a semiconductor processing method comprising: an apparatus comprising: at least one processor; and at least memory array, coupled to the at least one processor, comprising: a first via layer between a substrate and a first metal layer; a second via layer between the first metal layer and second metal layer; and a third via layer between the second metal layer and a third metal layer; wherein (a) the second metal layer includes portions of a first memory cell and portions of a second memory cell, (b) the third via layer includes a metal interconnect directly contacting the first and second memory cells, and (c) the third metal layer includes a bit line.

[0074] Thus, embodiments are not limited to MTJs and may include, for example, resistive random access memory (RRAM) such as resistive switching memories, which include, without limitation, oxide vacancy filament RRAM, conductive bridging RAM (CBRAM), phase change memory (PCM) RAM, and interfacial switching RRAM. Such examples of RRAM have a thermal component to be managed. Not all RRAM require forming events and embodiments include such RRAMs.

[0075] In example 22 the subject matter of the Example 21 can optionally include wherein (a) the first metal layer includes an additional metal interconnect that directly contacts the first memory cell but not the second memory cell, and (b) the bit line couples to a first access transistor through the additional metal interconnect.

[0076] In example 23 the subject matter of the Examples 21-22 can optionally include wherein a first vertical axis intersects the first memory cell and the metal interconnect and a second vertical axis intersects the second memory cell and the metal interconnect.

[0077] In example 24 the subject matter of the Examples 21-23 can optionally include wherein the first and second vertical axes both intersect the bit line.

[0078] In example 25 the subject matter of the Examples 21-24 can optionally include wherein the bit line directly contacts the metal interconnect.

[0079] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

- 1 1. An apparatus comprising:
2 a first via layer between a substrate and a first metal layer;
3 a second via layer between the first metal layer and second metal layer;
4 a third via layer between the second metal layer and a third metal layer; and
5 first and second access transistors each included in the substrate;
6 wherein (a) the second via layer and the second metal layer each include
7 portions of a first magnetic tunnel junction (MTJ) and portions of a second MTJ, (b)
8 the third via layer includes a metal interconnect directly contacting the first and
9 second MTJs, and (c) the third metal layer includes a bit line that couples to the first
10 and second access transistors through the metal interconnect and the first and
11 second MTJs.
- 1 2. The apparatus of claim 1, wherein (a) the first metal layer includes an
2 additional metal interconnect that directly contacts the first MTJ but not the second
3 MTJ, and (b) the bit line couples to the first access transistor through the additional
4 metal interconnect.
- 1 3. The apparatus of claim 2, wherein a first vertical axis intersects the first MTJ
2 and the metal interconnect and a second vertical axis intersects the second MTJ and
3 the metal interconnect.
- 1 4. The apparatus of claim 3, wherein the metal interconnect is monolithic.
- 1 5. The apparatus of claim 3, wherein a first horizontal axis intersects the first and
2 second MTJs but not the metal interconnect.
- 1 6. The apparatus of claim 5, wherein the first and second vertical axes both
2 intersect the bit line.

- 1 7. The apparatus of claim 5, wherein the bit line directly contacts the metal
2 interconnect.
- 1 8. The apparatus of claim 5, wherein the first and second MTJs are generally
2 located collinearly with each other along the first horizontal axis and the bit line is
3 generally located along a second horizontal axis that is not parallel with the first
4 horizontal axis.
- 1 9. The apparatus of claim 8, wherein the metal interconnect is generally located
2 along a third horizontal axis that is parallel with the first horizontal axis and is not
3 parallel with the second horizontal axis.
- 1 10. The apparatus of claim 2, wherein the first via layer directly contacts the first
2 metal layer, the second via layer directly contacts the second metal layer, and the
3 third via layer directly contacts the third metal layer.
- 1 11. The apparatus of claim 2, wherein (a) the first metal layer includes another
2 metal interconnect that directly contacts the second MTJ but not the first MTJ, and
3 (b) the bit line couples to the second access transistor through the another metal
4 interconnect but not the additional interconnect.
- 1 12. The apparatus of claim 2, wherein the bit line directly contacts the metal
2 interconnect with no via between the bit line and the metal interconnect.
- 1 13. The apparatus of claim 2 comprising an additional bit line that couples to the
2 additional metal interconnect.
- 1 14. The apparatus of claim 1 including a system on a chip with embedded
2 memory including a memory array comprising the first and second MTJs and the
3 metal interconnect.

- 1 15. The apparatus of claim 1 comprising:
2 a first word line coupled to a gate node of the first access transistor and a first
3 sense line coupled to another node of the first access transistor; and
4 a second word line coupled to a gate node of the second access transistor
5 and at least one of the first sense line and a second sense line coupled to another
6 node of the second access transistor.
- 1 16. An apparatus comprising:
2 a first via layer between a substrate and a first metal layer;
3 a second via layer between the first metal layer and second metal layer; and
4 a third via layer between the second metal layer and a third metal layer;
5 wherein (a) the second metal layer includes portions of a first magnetic tunnel
6 junction (MTJ) and portions of a second MTJ, (b) the third via layer includes a metal
7 interconnect directly contacting the first and second MTJs, and (c) the third metal
8 layer includes a bit line.
- 1 17. The apparatus of claim 16, wherein (a) the first metal layer includes an
2 additional metal interconnect that directly contacts the first MTJ but not the second
3 MTJ, and (b) the bit line couples to a first access transistor through the additional
4 metal interconnect.
- 1 18. The apparatus of claim 17, wherein a first vertical axis intersects the first MTJ
2 and the metal interconnect and a second vertical axis intersects the second MTJ and
3 the metal interconnect.
- 1 19. The apparatus of claim 18, wherein the first and second vertical axes both
2 intersect the bit line.
- 1 20. The apparatus of claim 19, wherein the bit line directly contacts the metal
2 interconnect.

- 1 21. An apparatus comprising:
2 at least one processor; and
3 at least memory array, coupled to the at least one processor, comprising:
4 a first via layer between a substrate and a first metal layer;
5 a second via layer between the first metal layer and second metal
6 layer; and
7 a third via layer between the second metal layer and a third metal
8 layer;
9 wherein (a) the second metal layer includes portions of a first memory
10 cell and portions of a second memory cell, (b) the third via layer includes a metal
11 interconnect directly contacting the first and second memory cells, and (c) the third
12 metal layer includes a bit line.
- 1 22. The apparatus of claim 21, wherein (a) the first metal layer includes an
2 additional metal interconnect that directly contacts the first memory cell but not the
3 second memory cell, and (b) the bit line couples to a first access transistor through
4 the additional metal interconnect.
- 1 23. The apparatus of claim 22, wherein a first vertical axis intersects the first
2 memory cell and the metal interconnect and a second vertical axis intersects the
3 second memory cell and the metal interconnect.
- 1 24. The apparatus of claim 23, wherein the first and second vertical axes both
2 intersect the bit line.
- 1 25. The apparatus of claim 24, wherein the bit line directly contacts the metal
2 interconnect.

1/11

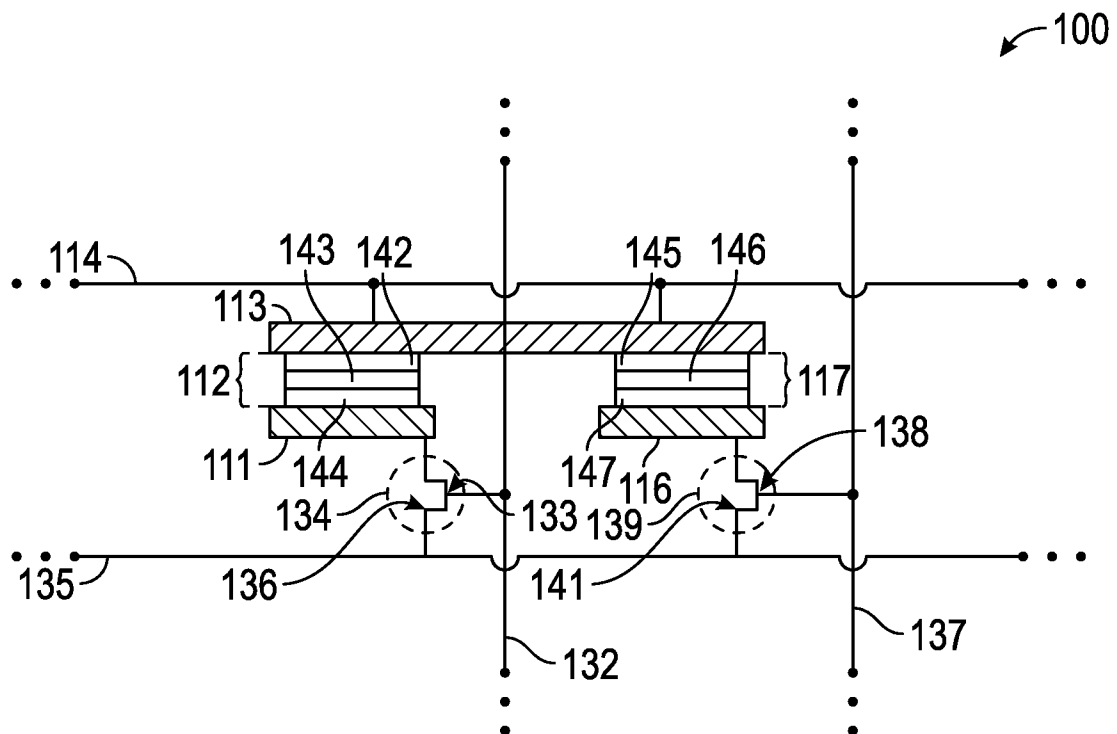


FIG. 1

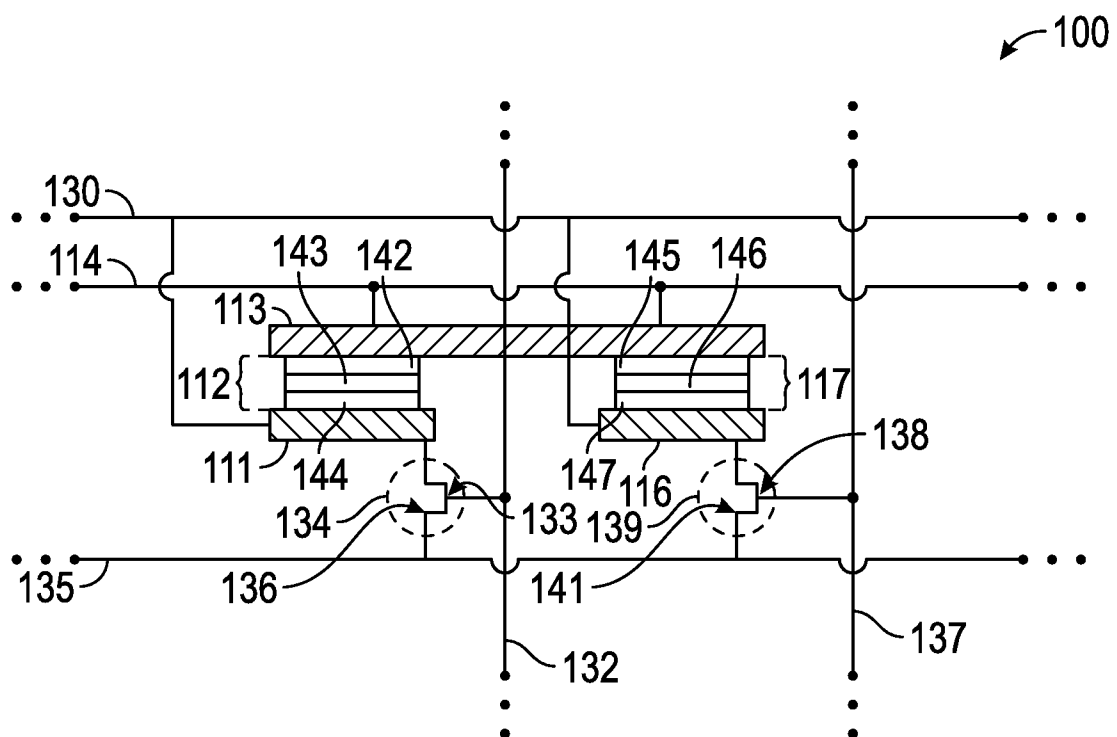


FIG. 2

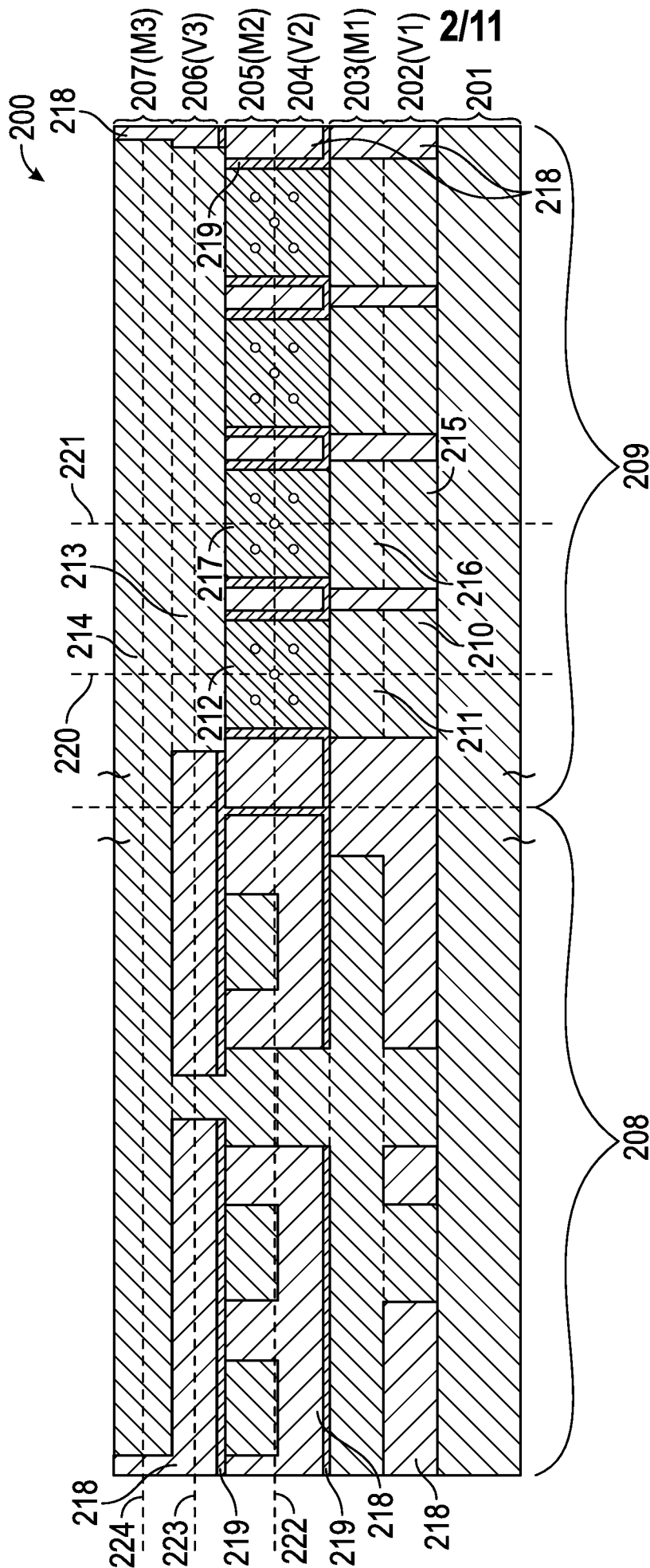


FIG. 3

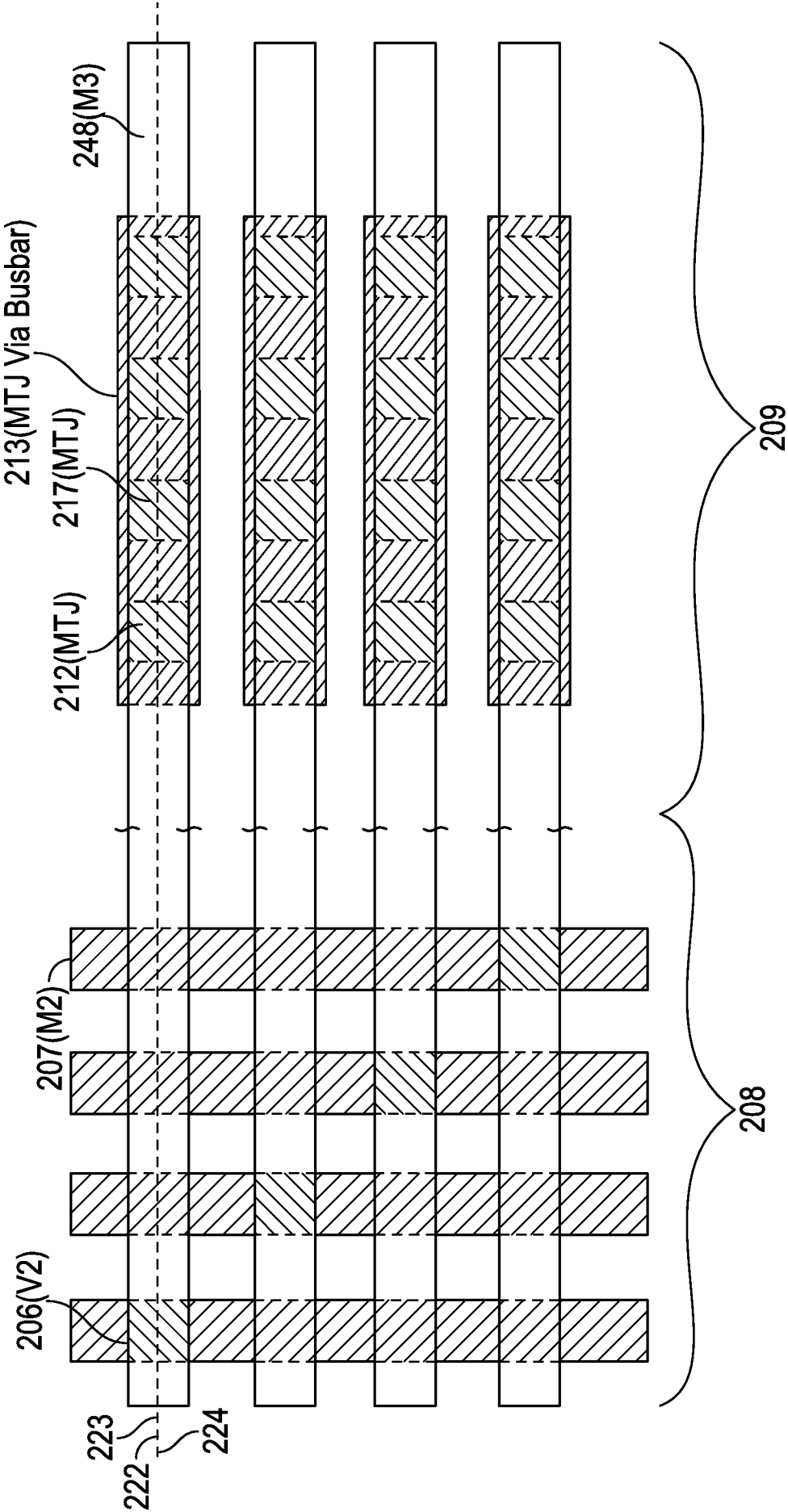


FIG. 4

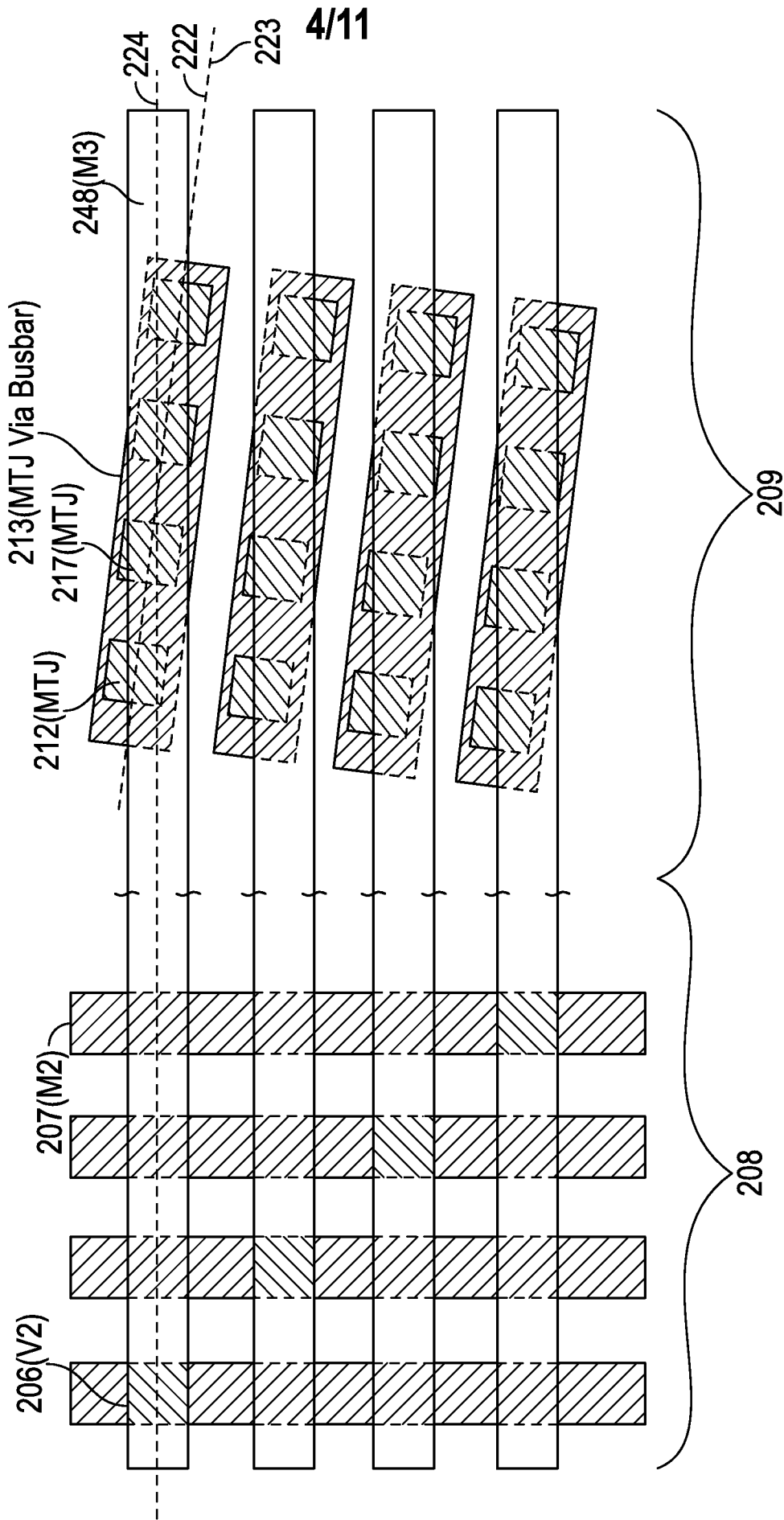
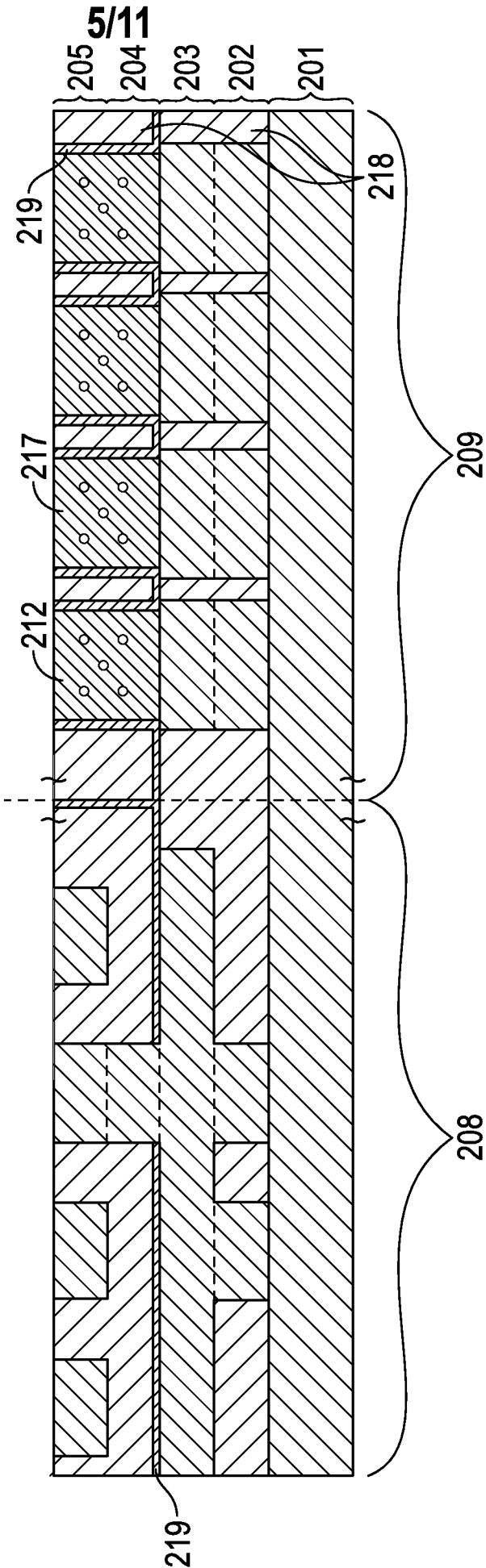


FIG. 5



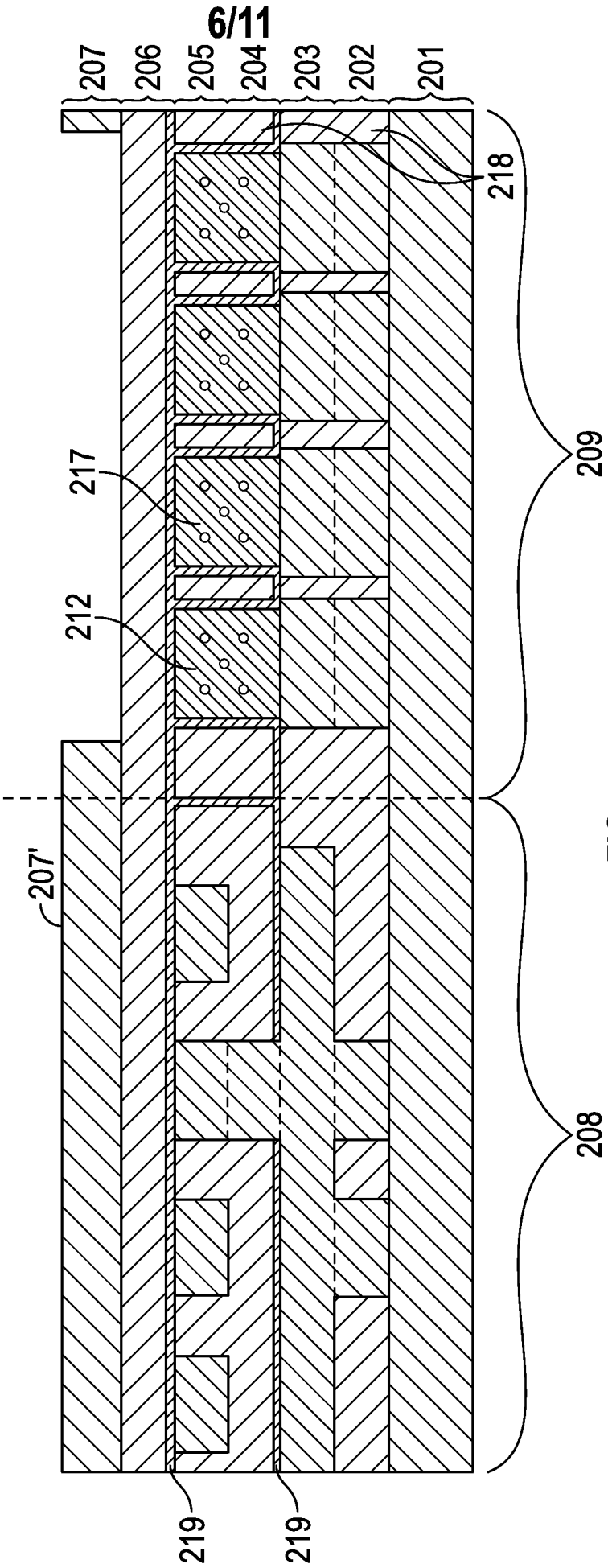


FIG. 6B

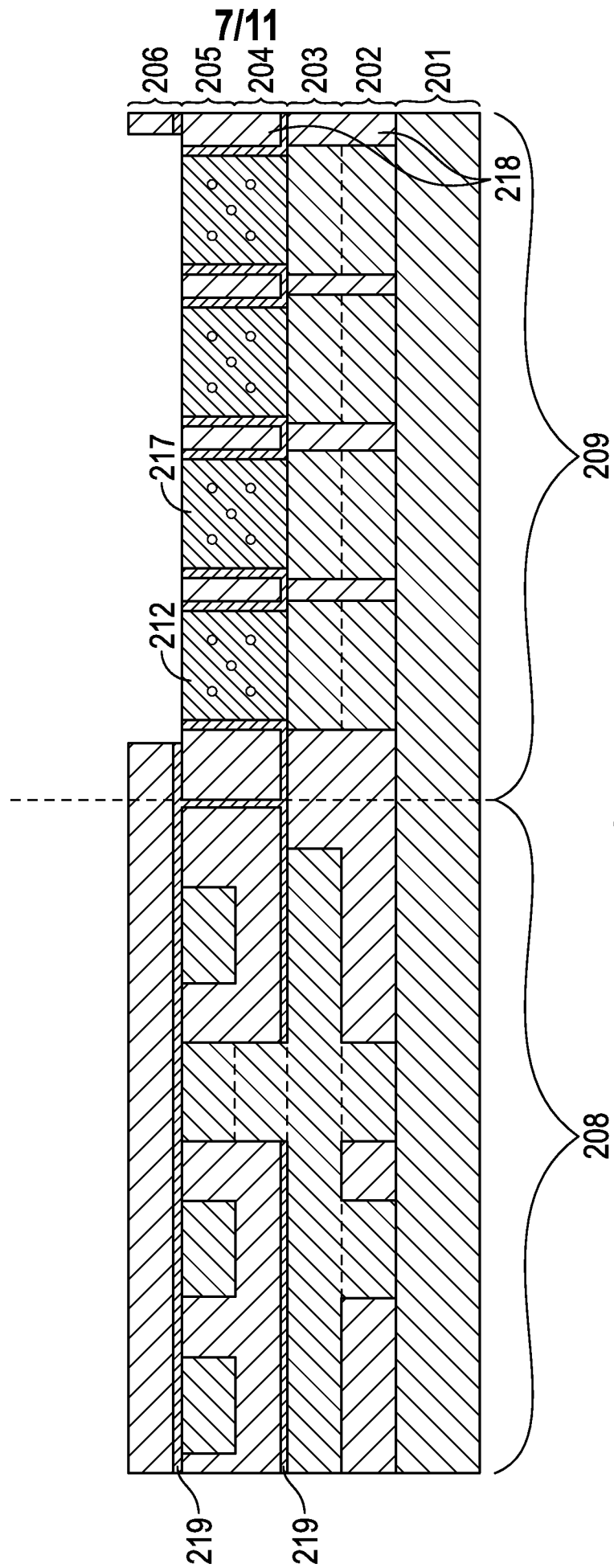


FIG. 6C

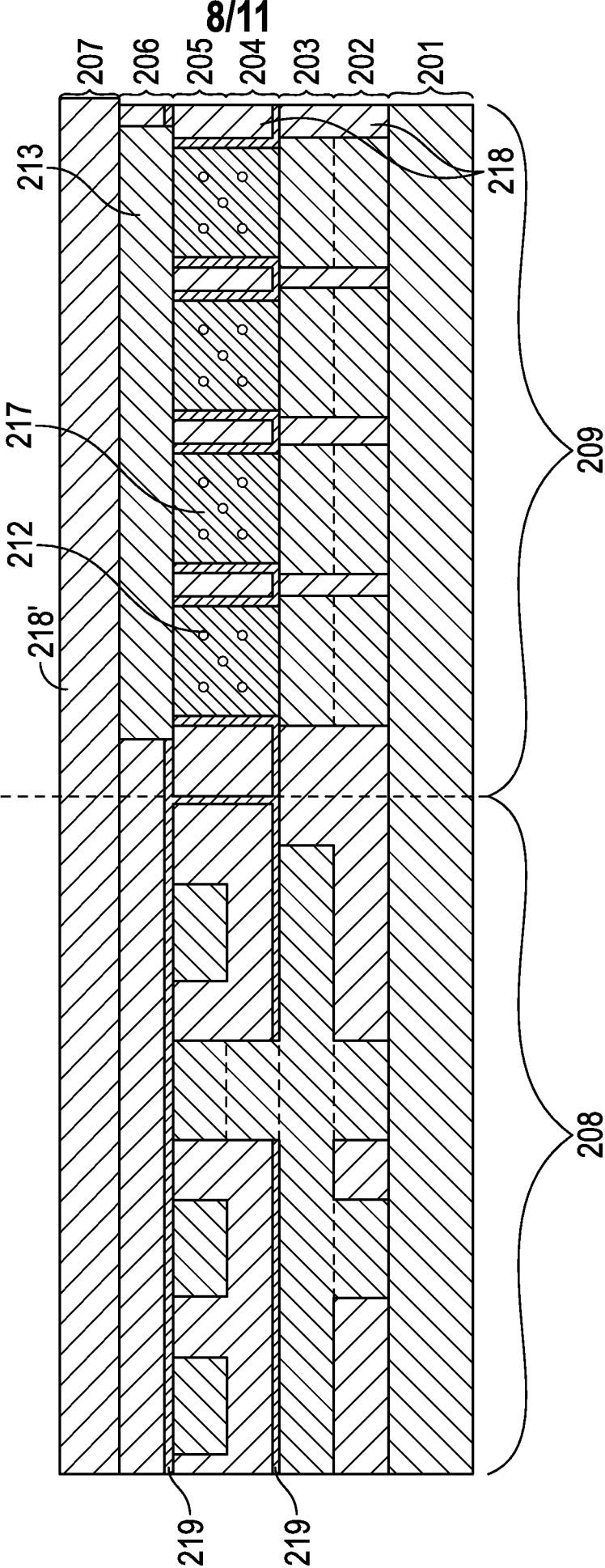
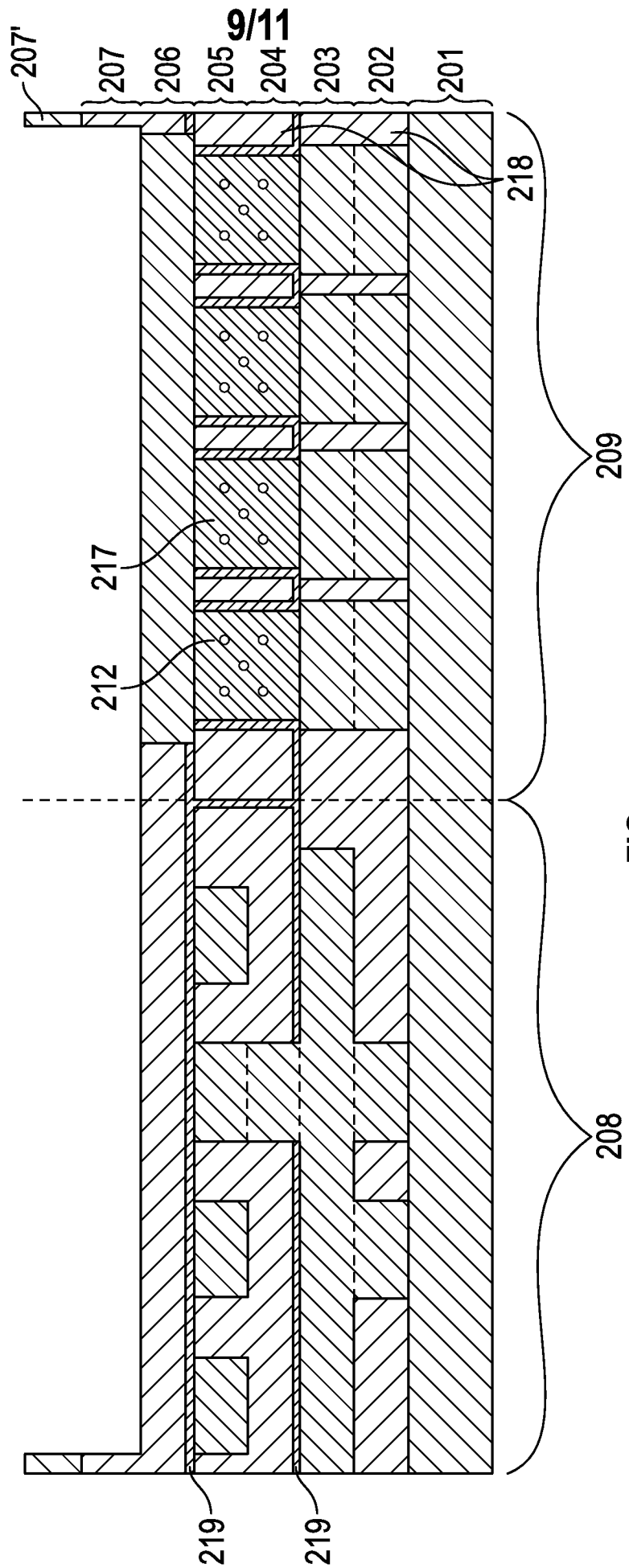
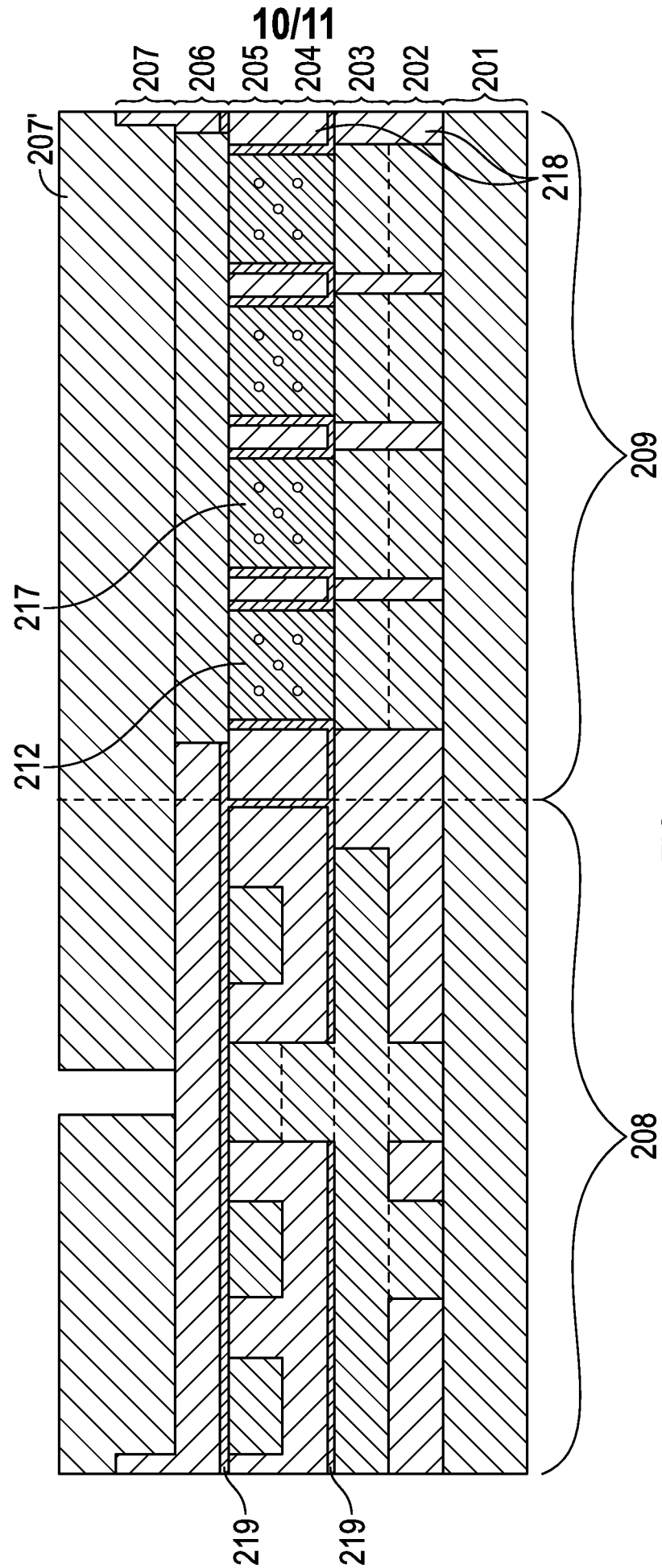


FIG. 6D





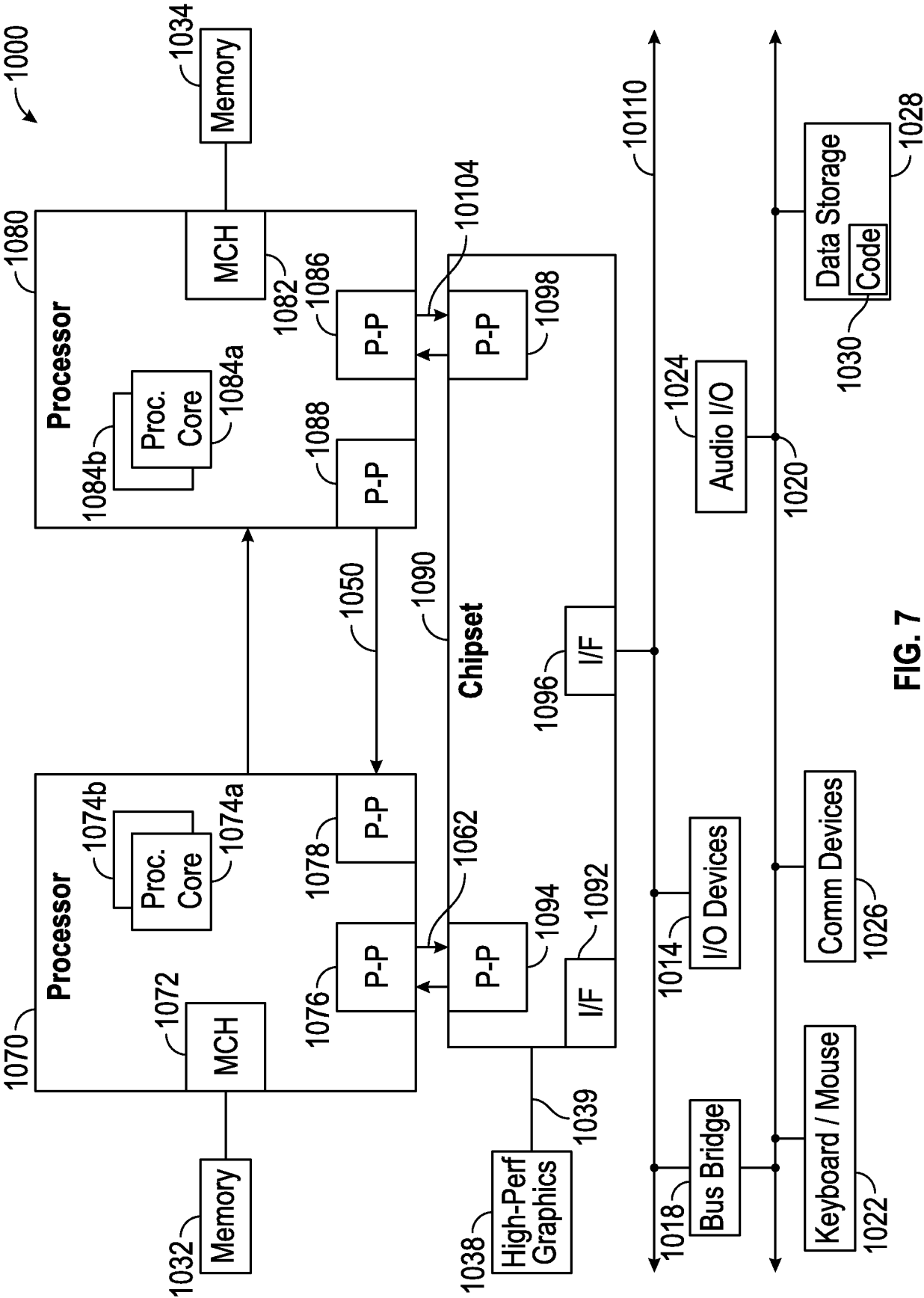


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/052032**A. CLASSIFICATION OF SUBJECT MATTER****H01L 43/02(2006.01)i, H01L 43/10(2006.01)i, H01L 43/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 43/02; H01L 27/115; H01L 21/768; H01L 21/8246; H01L 27/105; G11C 11/15; H01L 29/04; H01L 27/22; G11C 11/14; H01L 23/58; H01L 43/10; H01L 43/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: magnetic tunnel junction, via layer, metal layer, bar, bit line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013-0155759 A1 (YA-CHEN KAO et al.) 20 June 2013 See paragraphs [0021]–[0027], claim 1 and figure 2.	1–25
A	WO 2014-204492 A1 (INTEL CORPORATION) 24 December 2014 See paragraphs [0026]–[0047], claim 1 and figure 5A.	1–25
A	US 2015-0061020 A1 (SONY CORPORATION) 05 March 2015 See paragraphs [0052]–[0068], claim 1 and figure 1A.	1–25
A	US 2004-0211963 A1 (BRADLEY J. GARNI et al.) 28 October 2004 See paragraphs [0012]–[0019], claim 1 and figure 1.	1–25
A	JP 2011-519476 A (QUALCOMM INC.) 07 July 2011 See paragraphs [0024]–[0033], claim 1 and figure 10.	1–25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 June 2016 (17.06.2016)

Date of mailing of the international search report

17 June 2016 (17.06.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

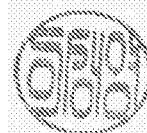
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/052032

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