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Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) **Title:** APPARATUS AND METHOD TO HOLD PLL OUTPUT FREQUENCY WHEN INPUT CLOCK IS LOST

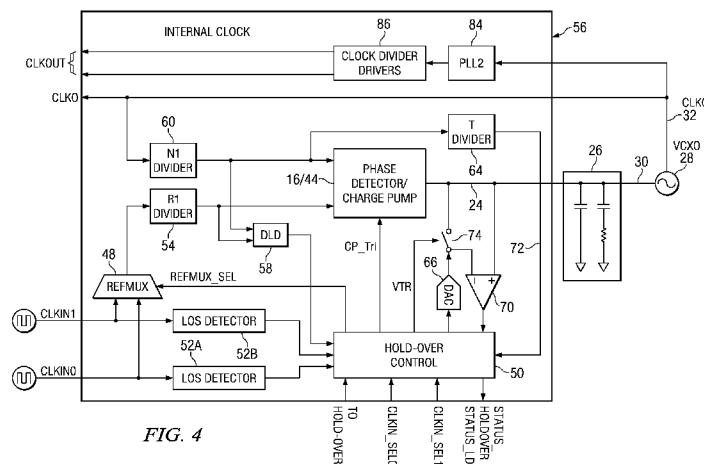


FIG. 4

(57) **Abstract:** A dock conditioning circuit including a phase detector circuit configured to provide an analog tuning signal indicative of a phase relationship between a reference dock to be conditioned and a generated clock. The controlled oscillator is configured to produce the generated clock, with the generated clock having an output frequency adjustable in response to an analog tuning signal applied to a control signal input of the controlled oscillator. Converter circuitry is provided to produce a digital representation of the analog tuning signal when the mode control circuitry is in a tracking mode. In the event the reference clock is lost, the mode control circuitry switches to a holdover mode so as to provide an analog holdover signal to the control signal input based upon the digital representations produced just prior to the loss of the reference clock.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))* — *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

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A. CLASSIFICATION OF SUBJECT MATTER**H03L 7/085(2006.01)i, H03L 7/099(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L 7/085; H03L 7/00; H03L 7/23; H03L 7/06; H03L 7/095; H03L 7/087

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: clock conditioning circuit, phase detector, oscillator, mode control, holdover, tracking

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 05473274 A (REILLY; BRIAN F. et al.) 05 December 1995 See abstract, claims 1, 7 and figure 1	1-24
A	US 6670852 B1 (HAUCK; LANE T.) 30 December 2003 See abstract, claims 1-2, 7 and figure 4	1-24
A	US 6236278 B1 (OLGAARD; CHRISTIAN) 22 May 2001 See abstract, claims 1-2, 8-9 and figure 5	1-24
A	US 06028460 A (MCCOLLUM; ROBERT L. et al.) 22 February 2000 See abstract, claims 1-2 and figure 3	1-24

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 05473274 A	05.12.1995	None	
US 6670852 B1	30.12.2003	None	
US 6236278 B1	22.05.2001	None	
US 06028460 A	22.02.2000	None	