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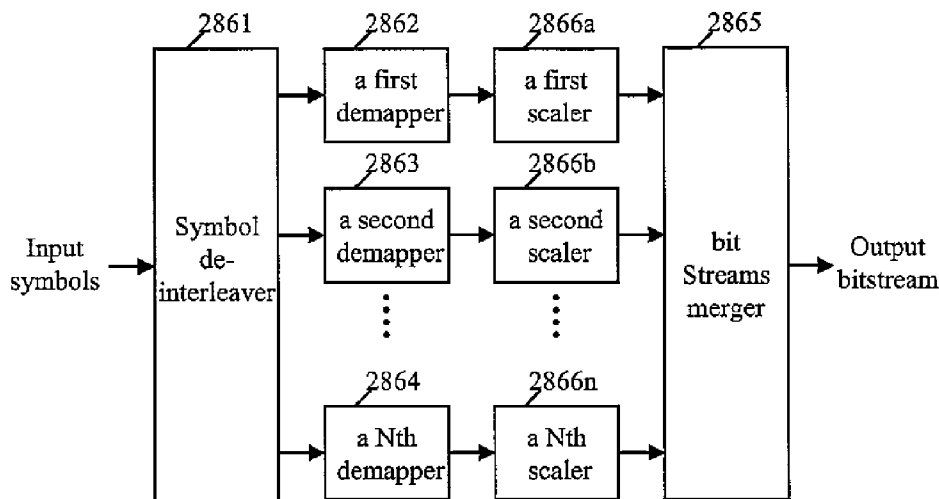
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(54) Title: METHOD OF TRANSMITTING AND RECEIVING A SIGNAL AND APPARATUS FOR TRANSMITTING AND RECEIVING A SIGNAL

[Fig. 32]



(57) Abstract: The present invention relates to a method of transmitting/receiving a signal and an apparatus for transmitting/receiving a signal. The present invention may include a symbol mapper demapping a first interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a first symbol mapping method, scaling the demapped symbol according to a constellation size of the first symbol mapping method and outputting the scaled symbol, demapping a second interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a second symbol mapping method, scaling the demapped symbol according to a constellation size of the second symbol mapping method and outputting the scaled symbol, and outputting the first bit streams and the second bit streams into one bit streams.

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Description

METHOD OF TRANSMITTING AND RECEIVING A SIGNAL AND APPARATUS FOR TRANSMITTING AND RECEIVING A SIGNAL

Technical Field

- [1] The present invention relates to a method of transmitting/receiving a signal and an apparatus for transmitting/receiving a signal, and more particularly to a method of transmitting/receiving a signal and an apparatus for transmitting/receiving a signal, which are capable of increasing a data transfer rate.

Background Art

- [2] As a digital broadcasting technology has been developed, users have received a broadcasting signal including a high definition (HD) moving image and high-quality digital sound. With continuous development of a compression algorithm and high performance of hardware, a better environment will be provided to the users in the future. A digital television (DTV) system can receive a digital broadcasting signal and provide a variety of supplementary services to users as well as a video signal and an audio signal.
- [3] With the development of the digital broadcasting technology, a requirement for a service such as a video signal and an audio signal is increased and the size of data desired by a user or the number of broadcasting channels is gradually increased.

Disclosure of Invention

Technical Problem

- [4] However, in the existing transmission frame structure, it is difficult to cope with the increase in the size of data or the number of broadcasting channels. Accordingly, a requirement for a new signal transmitting/receiving technology in which channel bandwidth efficiency is higher than that of the existing signal transmitting/receiving method and cost necessary for configuring a signal transmitting/receiving network is low.
- [5] An object of the present invention devised to solve the problem lies on a method of transmitting/receiving a signal and an apparatus for transmitting/receiving a signal, which are capable of using the existing signal transmitting/receiving network and improving data transmission efficiency.

Technical Solution

- [6] The present invention provides an apparatus for transmitting a signal, and a method thereof. The apparatus includes an forward error correction encoder performing error

correction encoding for input data, an interleaver interleaving the error-correction encoded data, a symbol mapper mapping a first interval data of the interleaved data to symbol data in accordance with a symbol mapping method in which distances between a first symbol and neighboring symbols of the first symbol in a first constellation are constant, and mapping a second interval data of the interleaved data to symbol data in accordance with a symbol mapping method in which distances between a second symbol and neighboring symbols of the second symbol in a second constellation are constant, and a transmitter modulating the mapped symbol data and transmitting the modulated data.

- [7] In another aspect of the present invention, the present invention provides an apparatus for receiving a signal, and a method thereof. The apparatus includes a demodulator demodulating a received signal, a frame parser parsing the demodulated signal and output the parsed data, a symbol mapper demapping a first interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a first symbol mapping method, scaling the demapped symbol according to a constellation size of the first symbol mapping method and outputting the scaled symbol, and demapping a second interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a second symbol mapping method, scaling the demapped symbol according to a constellation size of the second symbol mapping method and outputting the scaled symbol, and outputting the first bit streams and the second bit streams into one bit streams, a deinterleaver deinterleaving the bit streams, and a forward error correction decoder performing forward error correction decoding on the deinterleaved data.
- [8] According to the first symbol mapping method or the second symbol mapping method, three neighboring symbols in the constellation are mapped to an equilateral triangle.
- [9] The symbol mapper may include a symbol deinterleaver splitting the first interval of the symbol data and the second interval of the symbol data in the parsed data, a first demapper demapping the first interval of the symbol data in accordance with the symbol demapping method corresponding to the first symbol mapping method, a first scaler multiplying a reliability value demapped by the first symbol mapping method by a scaling value according to the constellation size of the first symbol mapping method, a second demapper demapping the second interval of the symbol data in accordance with the symbol demapping method corresponding to the second symbol mapping method, a second scaler multiplying a reliability value demapped by the second symbol mapping method by a scaling value according to the constellation size of the second symbol mapping method, and a bit stream merger restoring the first bit streams according to the scaled reliability value output by the first scaler, restoring the second

bit streams according to the scaled reliability value output by the second scaler, and outputting the first bit streams and the second bit streams to one bit streams.

[10] One of the first scaler and the second scaler may include a scaling factor generator generating a scaling factor and a multiplier multiplying the generated scaling factor by the demapping result.

[11] The scaling factor is one a reciprocal of average symbol size in the constellation or average power of the constellation.

Advantageous Effects

[12] According to a method of transmitting/receiving a signal and an apparatus for transmitting/receiving a signal of the present invention, it is possible to facilitate the switching of a signal transmitting/receiving system using the existing signal transmitting/receiving network and reduce cost.

[13] In addition, it is possible to improve a data transfer rate on the basis of a SNR gain and estimate a channel with respect to a transmission channel having a long delay spread property so as to increase a signal transmission distance. Accordingly, it is possible to more accurately estimate the channel using the suggested frame structure.

[14] Accordingly, it is possible to improve the signal transmitting/receiving performance of the transmitting/receiving system.

Brief Description of the Drawings

[15] FIG. 1 is a schematic block diagram showing an apparatus for transmitting a signal according to an embodiment of the present invention.

[16] FIG. 2 is a schematic block diagram showing an interleaver and a forward error correction (FEC) encoder according to an embodiment of the present invention.

[17] FIG. 3 is a view showing the interleaver for interleaving input data according to an embodiment of the present invention.

[18] FIG. 4 is a view showing another example of the interleaver according to an embodiment of the present invention.

[19] FIG. 5 is a view showing a detailed example of the interleaver of FIG. 4 according to an embodiment of the present invention.

[20] FIG. 6 is a view showing an example of a multi-input/output encoding method according to an embodiment of the present invention.

[21] FIG. 7 is a view showing a structure of a transmission frame according to an embodiment of the present invention.

[22] FIG. 8 is a view showing a structure of a pilot symbol interval according to an embodiment of the present invention.

[23] FIG. 9 is a view showing another structure of the pilot symbol interval according to an embodiment of the present invention.

- [24] FIG. 10 is a schematic block diagram showing an apparatus for receiving a signal according to an embodiment of the present invention.
- [25] FIG. 11 is a view showing an example of a multi-input/output decoding method according to an embodiment of the present invention.
- [26] FIG. 12 is a view showing a detailed example of FIG. 11 according to an embodiment of the present invention.
- [27] FIG. 13 is a schematic block diagram showing a deinterleaver and a FEC decoder according to an embodiment of the present invention.
- [28] FIG. 14 is a schematic block diagram showing another example of the apparatus for transmitting the signal according to an embodiment of the present invention.
- [29] FIG. 15 is a schematic block diagram showing another example of the apparatus for receiving the signal according to an embodiment of the present invention.
- [30] FIG. 16 is a schematic view showing the positions of points of an optimal constellation according to an embodiment of the present invention.
- [31] FIG. 17 is a flowchart illustrating a method of deciding points of an optimal constellation according to an embodiment of the present invention.
- [32] FIG. 18 is a schematic view showing an optimal constellation having 16 points according to an embodiment of the present invention.
- [33] FIG. 19 is a schematic view showing an optimal constellation having 64 points according to an embodiment of the present invention.
- [34] FIG. 20 is a schematic view showing an optimal constellation having 256 points according to an embodiment of the present invention.
- [35] FIG. 21 is a schematic view showing another optimal constellation having 256 points according to an embodiment of the present invention.
- [36] FIG. 22 is a schematic block diagram showing decision boundaries of the optimal constellation having 64 points.
- [37] FIG. 23 is a schematic block diagram showing a symbol demapper for demapping a received optimal constellation symbol according to an embodiment of the present invention.
- [38] FIG. 24 is a schematic block diagram showing another symbol demapper for demapping a received optimal constellation symbol according to an embodiment of the present invention.
- [39] FIG. 25 is a schematic view showing a process of demapping a received optimal constellation symbol according to an embodiment of the present invention.
- [40] FIG. 26 is a schematic view showing a process of demapping a received optimal constellation symbol of an edge region according to an embodiment of the present invention.
- [41] FIG. 27 is a schematic block diagram showing an apparatus for transmitting a signal

according to an embodiment of the present invention.

[42] FIG. 28 is a schematic block diagram showing a multi-demapper according to an embodiment of the present invention.

[43] FIG. 29 is a view showing a bitstream distributing method according to an embodiment of the present invention.

[44] FIG. 30 is a schematic block diagram showing an apparatus for receiving a signal according to an embodiment of the present invention.

[45] FIG. 31 is a schematic block diagram showing a multi-demapper according to an embodiment of the present invention.

[46] Fig. 32 is a view representing another embodiment of the multi-demapper.

[47] Fig. 33 is a view representing an embodiment of the exemplified scaler.

[48] FIG. 34 is a schematic block diagram showing an apparatus for transmitting a signal using multi-encoding according to an embodiment of the present invention.

[49] FIG. 35 is a schematic block diagram showing a multi-encoder according to an embodiment of the present invention.

[50] FIG. 36 is a schematic block diagram showing an apparatus for receiving a multi-encoded signal according to an embodiment of the present invention.

[51] FIG. 37 is a schematic block diagram showing a multi-decoder according to an embodiment of the present invention.

[52] FIG. 38 is a schematic block diagram showing an apparatus for transmitting a signal using a multi-encoding method and a multi-mapping method according to an embodiment of the present invention.

[53] FIG. 39 is a schematic block diagram showing an apparatus for receiving a multi-encoded and multi-mapped signal according to an embodiment of the present invention.

[54] FIG. 40 is a schematic block diagram showing another example of an apparatus for receiving a multi-encoded and multi-mapped signal according to an embodiment of the present invention.

[55] FIG. 41 is a schematic block diagram showing a channel estimator according to an embodiment of the present invention.

[56] FIG. 42 is a schematic block diagram showing an equalizer according to an embodiment of the present invention.

[57] FIG. 43 is a schematic block diagram showing an apparatus for transmitting a signal by a data symbol channel estimation method according to an embodiment of the present invention.

[58] FIG. 44 is a schematic block diagram showing an apparatus for receiving a signal by a data symbol channel estimation method according to an embodiment of the present invention.

- [59] FIG. 45 is a schematic block diagram showing another example of an apparatus for transmitting a signal by a data symbol channel estimation method according to an embodiment of the present invention.
- [60] FIG. 46 is a schematic block diagram showing another example of an apparatus for receiving a signal by a data symbol channel estimation method according to an embodiment of the present invention.
- [61] FIG. 47 is a view showing the structure of a transmission frame according to an embodiment of the present invention.
- [62] FIG. 48 is a view showing the number of tracking pilots in a frame according to an embodiment of the present invention.
- [63] FIG. 49 is a view showing a frame including tracking pilots according to an embodiment of the present invention.
- [64] FIG. 50 is a view showing margins of the frame of FIG. 47 according to an embodiment of the present invention.
- [65] FIG. 51 is a view showing another frame including tracking pilots according to an embodiment of the present invention.
- [66] FIG. 52 is a view showing margins of the frame of FIG. 51 according to an embodiment of the present invention.
- [67] FIG. 53 is a view showing the number of symbols included in a low density parity check (LDPC) block according to an embodiment of the present invention.
- [68] FIG. 54 is a view showing the number of LDPC blocks included in an LDPC frame according to an embodiment of the present invention.
- [69] FIG. 55 is a view showing the number of OFDM blocks included in an LDPC frame according to an embodiment of the present invention.
- [70] FIG. 56 is a view showing the number of LDPC blocks included in an LDPC frame of another mode according to an embodiment of the present invention.
- [71] FIG. 57 is a view showing the number of OFDM blocks included in an LDPC frame of another mode according to an embodiment of the present invention.
- [72] FIG. 58 is a view showing the number of OFDM blocks included in an LDPC frame of another mode according to an embodiment of the present invention.
- [73] FIG. 59 is a view showing the structure of an LDPC frame according to an embodiment of the present invention.
- [74] FIG. 60 is a view showing the structure of a transmission parameter signal (TPS) according to an embodiment of the present invention.
- [75] FIG. 61 is a view showing constellation information according to an embodiment of the present invention.
- [76] FIG. 62 is a view showing LDPC mode information according to an embodiment of the present invention.

[77] FIG. 63 is a view showing the structure of a TPS including the information of FIGs. 60 and 61 according to an embodiment of the present invention.

[78] FIG. 64 is a view showing OFDM block index information according to an embodiment of the present invention.

[79] FIG. 65 is a view showing the structure of a TPS including OFDM block index information according to an embodiment of the present invention.

[80] FIG. 66 is a view showing LDPC block information according to an embodiment of the present invention.

[81] FIG. 67 is a view showing OFDM block information according to an embodiment of the present invention.

[82] FIG. 68 is a view showing the structure of a TPS including suggested information according to an embodiment of the present invention.

[83] FIG. 69 is a view showing preamble period information according to an embodiment of the present invention.

[84] FIG. 70 is a view showing a structure of a TPS including the preamble period information according to an embodiment of the present invention.

[85] FIG. 71 is a view showing a relationship between a pilot symbol interval and a single frequency network according to an embodiment of the present invention.

[86] FIG. 72 is a view showing a structure of a pilot symbol according to an embodiment of the present invention.

[87] FIG. 73 is a schematic block diagram showing another example of an apparatus for transmitting a signal according to an embodiment of the present invention.

[88] FIG. 74 is a schematic block diagram showing another example of an apparatus for receiving a signal according to an embodiment of the present invention.

[89] FIGs. 75 and 76 are views showing suggested frame structures according to an embodiment of the present invention.

[90] FIGs. 77 to 79 are views showing insertion positions of continual pilot (CP) information of modes, according to an embodiment of the present invention.

[91] FIGs. 80 and 81 are views showing the structures of the frames having the same CP positions according to an embodiment of the present invention.

[92] FIG. 82 is a view showing insertion positions of common CP information according to an embodiment of the present invention.

[93] FIGs. 83 to 85 are views showing the structures of multi-input/output transmission frames according to an embodiment of the present invention.

[94] FIG. 86 is a view showing a pseudo random binary sequence (PRBS) generator according to an embodiment of the present invention.

[95] FIG. 87 is a schematic block diagram showing another example of an apparatus for transmitting a signal according to an embodiment of the present invention.

- [96] FIG. 88 is a schematic block diagram showing another example of an apparatus for receiving a signal according to an embodiment of the present invention.
- [97] FIG. 89 is a view showing a descrambling device according to an embodiment of the present invention.
- [98] FIG. 90 is a view showing the comparison of the TPS transmission bit per symbol according to an embodiment of the present invention.
- [99] FIG. 91 is a schematic block diagram showing an apparatus for transmitting a signal using scramble according to an embodiment of the present invention.
- [100] FIG. 92 is a schematic block diagram showing a multi-mapper of block units according to an embodiment of the present invention.
- [101] FIG. 93 is a schematic block diagram showing a multi-mapper according to another embodiment of the present invention.
- [102] FIG. 94 is a view showing a block distributing method according to an embodiment of the present invention.
- [103] FIGS. 95 and 96 are view showing a method of interleaving symbol data according to an embodiment of the present invention.
- [104] FIG. 97 is a view showing the length of a column of a memory according to an embodiment of the present invention.
- [105] FIG. 98 is a schematic block diagram showing an apparatus for receiving a signal using descramble according to an embodiment of the present invention.
- [106] FIG. 99 is a schematic block diagram showing a multi-demapper of block units according to an embodiment of the present invention.
- [107] FIG. 100 is a schematic block diagram showing a multi-demapper according to another embodiment of the present invention.
- [108] FIGS. 101 to 103 are views showing experimental results of the performance of a transmitting/receiving system according to a plurality of symbol mapping methods.
- [109] FIGS. 104 and 105 are views showing times necessary for frame synchronization according to an error correction encoding frame.
- [110] FIGS. 106 and 107 are views showing times necessary for synchronizing an error correction encoding frame in the case of using a plurality of symbol mapping methods.
- [111] FIG. 108 is a view showing power enhancement in the case that a pilot is transmitted by the above-described preamble structure.
- [112] FIG. 109 is a view showing power enhancement according to the consecutive pilot structure.
- [113] FIG. 110 is a view showing power enhancement of a data symbol carrier in the above-described frame structure.
- [114] FIG. 111 is a view showing the decrease rate of a data transfer rate according to the above-described frame structure.

- [115] FIGs. 112 and 113 are views showing mobility characteristics according to the above-described frame structure.
- [116] FIG. 114 is a flowchart illustrating a method of transmitting a signal according to an embodiment of the present invention.
- [117] FIG. 115 is a flowchart illustrating a method of receiving a signal according to an embodiment of the present invention.
- [118] FIG. 116 is a view showing a plot signal structure according to an embodiment of the present invention.
- [119] FIG. 117 is a view showing an example of estimating a channel using two symbols according to an embodiment of the present invention.
- [120] FIG. 118 is a view showing an example of estimating a channel using four symbols according to an embodiment of the present invention.
- [121] FIG. 119 is a view showing an example of estimating a channel using eight symbols according to an embodiment of the present invention.
- [122] FIG. 120 is a schematic block diagram showing an apparatus for transmitting a signal according to an embodiment of the present invention.
- [123] FIG. 121 is a schematic block diagram showing a pilot index generator according to an embodiment of the present invention.
- [124] FIG. 122 is a schematic block diagram showing an apparatus for receiving a signal according to an embodiment of the present invention.
- [125] FIG. 123 is a view showing another example of a symbol mapping method.
- [126] FIG. 124 is a view showing remapped symbols after symbols are rotated on a constellation.
- [127] FIG. 125 is a view showing an embodiment of a symbol mapper for mapping symbols according to a symbol mapping method.
- [128] FIG. 126 is a view showing an embodiment of a symbol demapper for demapping a signal according to a symbol mapping method.
- [129] FIG. 127 is a view showing an example of deciding rotated symbols by a first symbol demapping unit.
- [130] FIG. 128 is a view showing still another example of a symbol mapping method.
- [131] FIG. 129 is a view showing an example of deciding a mapped symbol according to a non-uniform symbol mapping method.

Best Mode for Carrying Out the Invention

- [132] A method of transmitting/receiving data according to the present invention and the operation of a frame structure will be described in detail with reference to the accompanying drawings.
- [133] FIG. 1 is a schematic block diagram showing an apparatus for transmitting a signal

according to an embodiment of the present invention. The transmitting/receiving system may use a multi-input multi-output (MIMO) method.

[134] For example, the signal transmitting apparatus of FIG. 1 may be a signal transmitting system for transmitting video data such as a broadcasting signal, for example, a signal transmitting system according to a digital video broadcasting (DVB) system. The signal transmitting system according to the embodiment of the present invention now will be described with reference to FIG. 1.

[135] The embodiment of FIG. 1 includes an outer encoder 100, a first interleaver 110, an inner encoder 120, a second interleaver 130, a symbol mapper 140, a linear pre-coder 150, a third interleaver 160, a multi-input/output encoder 170, a first frame builder 180, a second frame builder 185, a first modulator 190, a second modulator 192, a first transmitter 194, and a second transmitter 196.

[136] The outer encoder 100 and the inner encoder 120 encode respective input signals and output the encoded signals such that an error generated in transmitted data is detected and corrected by a receiving apparatus. That is, as the encoder, a forward error correcting (FEC) encoder may be used.

[137] The first interleaver 110 shuffles the data stream output from the outer encoder 100 to random positions. For example, the first interleaver 110 may use a convolution interleaving method or a block interleaving method, which may be changed according to the signal transmitting system. The first interleaver 110 may not be used according to implementation examples.

[138] The second interleaver 130 shuffles the FEC-encoded data stream to random positions so as to become robust against a burst error which occurs in the data when the signal is transmitted. For example, the second interleaver 130 may use a convolution interleaver or a block interleaver, which may be changed according to the signal transmitting system.

[139] The data interleaved by the second interleaver 130 is input to the symbol mapper 140. The symbol mapper 140 may map the transmitted signal to symbols in consideration of a transmission parameter signal and a pilot signal according to a transmission mode. As the mapping method, a quadrature amplitude modulation (QAM), a quadrature phase shift keying (QPSK), an amplitude phase shift keying (APSK), a pulse amplitude modulation (PAM) or an optimal constellation may be used. Alternatively, an encoded symbol mapping method may be used in the symbol mapper 140. For example, the data may be mapped to symbols encoded using a trellis coded modulation method.

[140] The linear pre-coder 150 disperses input symbol data into several pieces of output symbol data so as to decrease a probability that all information is lost due to fading when experiencing frequency-selective fading of a channel. The linear pre-coder 150

converts the input data into parallel data, disperses parallel data into several pieces of data via an encoding matrix, and converts the parallel data into serial data.

- [141] An encoding matrix is designed by comparing an output symbol with an input symbol such that a pairwise error probability (PEP) that the two symbols are different from each other is minimized. If the encoding matrix is designed such that the PEP is minimized, a diversity gain and a coding gain obtained via the linear pre-coding are maximized. In addition, if a minimum Euclidean distance of the linearly pre-coded symbol is maximized by the encoding matrix, it is possible to minimize an error probability when the receiving apparatus uses a maximum likelihood (ML) decoder.
- [142] Examples of the encoding matrix may include a vanderMonde matrix, a Hadamard matrix and a Golden code. The matrix is exemplary and the data may be dispersed using a proper matrix according to implementation examples.
- [143] The linear pre-coder 150 may not be used according to implementation examples.
- [144] The third interleaver 160 interleaves the symbol data output from the linear pre-coder 150 again. That is, the third interleaver 160 performs the interleaves process such that the symbol data dispersed in the data output from the linear pre-coder 150 does not experience the same frequency-selective fading. The third interleaver 160 may use a convolution interleaving method or a block interleaving method.
- [145] The linear pre-coder 150 and the third interleaver 160 process the data to be transmitted so as to become the frequency-selective fading of the channel.
- [146] The multi-input/output decoder 170 encodes the data interleaved by the third interleaver 160 so as to be transmitted via a plurality of transmission antennas. The multi-input/output encoding method is largely classified into a spatial multiplexing method and a spatial diversity method. In the spatial multiplexing method, since a transmitter and a receiver may simultaneously transmit/receive different data using a plurality of antennas, the data can be transmitted at a high speed without further increasing the bandwidth of the system. In the spatial diversity method, data having the same information is transmitted by a plurality of transmission antennas so as to obtain transmission diversity.
- [147] At this time, as the multi-input/output encoder 170 of the spatial diversity method, a space-time block code (STBC), a space-frequency block code (SFBC), or a space-time trellis code (STTC) may be used. As the multi-input/output encoder 170 of the spatial multiplexing method, a method of dividing a data stream by the number of transmission antennas and transmitting the divided data, a full-diversity full-rate (FDFR) code, a linear dispersion code (LDC), a Vertical-Bell Lab layered space-time (V-BLAST), or a diagonal-BLAST (D-BLAST) may be used.
- [148] The multi-input/output encoder 170 encodes the input symbol data so as to be transmitted via the plurality of transmission antennas. For example, if two transmission

paths exist, the multi-input/output encoder 170 outputs the encoded data to the first frame builder 180 or the second frame builder 185. The number of transmission paths is only exemplary and the number of transmission paths may be changed according to the multi-input/output encoding method.

- [149] The first frame builder 180 and the second frame builder 185 inserts a pilot signal into a data interval to build a frame such that the signal output from the multi-input/output encoder 170 is modulated by an orthogonal frequency division multiplex (OFDM) method.
- [150] The first modulator 190 and the second modulator 192 inserts a guard interval into the data output from the first frame builder 180 and the second frame builder 185 and modulates the inserted data such that the data is transmitted in a state of being carried in OFDM subcarriers.
- [151] The first transmitter 194 and the second transmitter 196 convert the digital signals having the guard interval and the data interval, which are output from the first modulator 190 and the second modulator 192, into analog signals and transmit the converted analog signals.
- [152] The signal transmitting apparatus of FIG. 1 is only exemplary, and a necessary component may be further included or an unnecessary component may not be used, according to the transmitting system.
- [153] FIG. 2 is a schematic block showing the interleaver and a forward error correction (FEC) encoder according to an embodiment of the present invention. The FEC encoder includes a Bose-Chaudhuri-Hocquenghem (BCH) encoder 100 and a low density parity check (LDPC) encoder 120 as an outer encoder and an inner encoder, respectively.
- [154] A LDPC code is an error correction code which can reduce a probability that data information is lost. The LDPC encoder 120 encodes the signal in a state in which the length of an encoding block is large such that the transmitted data is robust against a transmission error. In order to prevent hardware complexity from being increased due to the increase of the block size, the density of the parity bit is decreased so as to decrease the complexity of the encoder.
- [155] In order to prevent an error floor from occurring in the output data of the receiving apparatus, the BCH encoder 100 is used as the additional outer encoder. If the LDPC encoder 120 which can ignore error floor is used, the BCH encoder 100 may not be used. Alternatively, other encoders may be used as the outer encoder, instead of the BCH encoder.
- [156] The data which is encoded by the BCH encoder 100 and is interleaved by the first interleaver 110 is output to the second interleaver 130 via the LDPC encoder 120.
- [157] FIG. 3 is a view showing an interleaver for interleaving input data according to an embodiment of the present invention. The interleaver of FIG. 3 is a block interleaver,

which is an example of the interleaver and may be used in the second interleaver 130.

[158] The interleaver of FIG. 3 stores input data in a matrix-shaped memory space in a pre-determined pattern and reads and outputs the data in a pattern different from the pattern used for storing the data. For example, the interleaver of FIG. 3 has an $N_r \times N_c$ memory space composed of N_r rows and N_c columns and the data input to the interleaver is filled from a position corresponding to a first row and a first column of the memory space. The data is stored from the first row and the first column to an N_r^{th} row and the first column and, if the first column is filled up, is then stored from the first row to the N_r^{th} row of a next column (second column). In this sequence, the data may be stored up to the N_r^{th} row of an N_c^{th} column.

[159] In the case that the stored data is read, the data is read and output from the first row and the first column to the first row and the N_c^{th} column. If all the data of the first row is read, the data is read and output from the first column of a next row (second row) in the column direction. In this sequence, the data may be read and output up to the N_c^{th} column of the N_r^{th} row. At this time, the position of a most significant bit (MSB) of the data block is a left uppermost side and the position of a least significant bit (LSB) thereof is a right lowermost side.

[160] The size of the memory block, the storage pattern and the read pattern of the interleaver are only exemplary and may be changed according to implementation embodiments.

[161] FIG. 4 is a view showing an example of the interleaver. The interleaver of FIG. 4 is an example of the interleaver of the OFDM system having a symbol length N , which can be used in the third interleaver 160 of the transmitting apparatus shown in FIG. 1.

[162] N denotes the length of the interleaver and i has a value corresponding to the length of the interleaver, that is, an integer from 0 to $N-1$. n denotes the number of valid transmission carriers in the transmitting system. $\Pi(i)$ denotes a permutation obtained by a modulo- N operation, and d_n has a $\Pi(i)$ value which is located in a valid transmission carrier area excluding a value $N/2$ in sequence. k denotes an index value of an actual transmission carrier. $N/2$ is subtracted from d_n such that the center of the transmission bandwidth becomes DC. P denotes a permutation constant which may vary according to implementation embodiments.

[163] FIG. 5 is a view showing a detailed example of the interleaver of FIG. 4 according to an embodiment of the present invention. In the example of FIG. 5, the length of the OFDM symbol and the length N of the interleaver are set to 2048 and the number of valid transmission carriers are set to 1536 (1792-256).

[164] Accordingly, i is an integer from 0 to 2047 and n is an integer from 0 to 1535. $\Pi(i)$ denotes a permutation obtained by a modulo-2048 operation. d_n has a $\Pi(i)$ value with respect to a value $256 \leq i \leq 792$ excluding a value $1024(N/2)$ in sequence. k denotes a

value obtained by subtracting 1024 from dn . P has a value of 13.

- [165] Using the above-described interleaver, since data k corresponding to the input data i is output, the data having the length N of the interleaver may be transmitted in a state in which the sequence thereof is changed.
- [166] FIG. 6 is a view showing an example of the multi-input/output encoding method according to an embodiment of the present invention. The embodiment of FIG. 6 is the STBC which is one of the multi-input/output encoding methods and may be used in the transmitting apparatus shown in FIG. 1. The encoding method is exemplary and other multi-input/output encoding methods may be used.
- [167] In the example of the STBC encoder, T denotes a symbol transmission period, s denotes an input symbol to be transmitted, and y denotes an output symbol. " $*$ " denotes a complex conjugate, and a first antenna (Tx #1) and a second antenna (Tx #2) denote a first transmission antenna and a second transmission antenna 2, respectively.
- [168] In this example, at a time t , the first antenna Tx #1 transmits s_0 and the second antenna Tx #2 transmits s_1 . At a time $t+T$, the first antenna Tx #1 transmits $-s_1^*$ and the second antenna Tx #2 transmits s_0^* . The transmission antennas transmit data having the same information of s_0 and s_1 in the transmission period. Accordingly, the receiving apparatus can obtain spatial diversity effect using the signals output from the multi-input/output encoder according to the shown method.
- [169] The signals transmitted by the first antenna and the second antenna are examples of the multi-input/output encoded signals. When FIG. 30 is described from a different viewpoint, the signals transmitted by the first antenna and the second antenna may be transmitted by a multi-input single-output method.
- [170] In this example, it may be considered that two temporally consecutive signals s_0 and $-s_1^*$ are input to a path of the first antenna and signals s_1 and s_0^* are input to a path of the second antenna. Accordingly, since the signals s_0 and $-s_1^*$ are consecutively output to the first antenna and the signals s_1 and s_0^* are output to the second antenna, it may be considered that the output symbols are transmitted by the multi-input single-output method. The above example shows a simplest example using two antennas. The signals may be transmitted using more antennas.
- [171] That is, when the above example is described by the multi-input single-output method, the first symbol and the second symbol consecutive to the first symbol (s_0 , $-s_1^*$) are multi-input and a minus of a complex conjugate of the second symbol (s_0 , $-s_1^*$) and a complex conjugate (s_1 , s_0^*) of the first symbol are simultaneously output. The multi-input symbols may be encoded according to an Alamouti algorithm and the encoded symbols may be output.
- [172] The multi-input/output encoder may transmit the signals which are interleaved by the second interleaver in the frequency domain, by the multi-input single-output method.

The multi-input/output (including the multi-input single-output) shown in the above example may be not applied to the pilot symbol interval shown in FIGs. 31 and 32 and may be applied to only the data symbol interval.

[173] FIG. 7 is a view showing a structure of a transmission frame. The transmission frame may include a pilot symbol interval including pilot carrier information and a data symbol interval including only data information.

[174] In the example of FIG. 7, a frame includes M intervals and is divided into M-1 data symbol intervals and a pilot symbol interval which is used as a preamble. The frame having the above-described structure is repeated.

[175] Each symbol interval includes carrier information by the number of OFDM subcarriers. The pilot carrier information of the pilot symbol interval is composed of random data in order to decrease a peak-to-average power ratio (PAPR). An auto-correlation value of the pilot carrier information has an impulse shape in a frequency domain.

[176] The pilot carrier information may not be included in the data symbol interval, and, accordingly, it is possible to increase a data capacity. In the DVB, for example, since a percentage of pilot carriers in all the valid carriers is about 10%, the increasing rate of the data capacity is expressed by Math Figure 1.

[177] [Math Figure 1]

[178]

$$\Delta = 100 \times \left(\frac{1}{10} - \frac{1}{M} \right) \%$$

[179] In Math Figure 1, Δ denotes the increasing rate and M denotes the number of intervals included in a frame.

[180] When the transmitting system of FIG. 1 performs multi-input/output encoding using the plurality of antennas, the structure of the pilot symbol is decided such that the receiving apparatus distinguishes between the transmission paths.

[181] FIG. 8 is a view showing a structure of the pilot carriers in the pilot symbol intervals built by the first and second frame builders of FIG. 1, according to an embodiment of the present invention. The pilot symbol intervals built by the frame builders of FIG. 8 may be output as shown in FIG. 1.

[182] In FIG. 8, in the pilot symbol intervals output from the first and second frame builders, even-numbered and odd-numbered pilot carriers are interleaved as shown in FIG. 31 and are output to the first and second antennas (antenna #1 and antenna #2). For example, only the even-numbered pilot carrier information of the built pilot carriers is included in the pilot symbol interval built by the first frame builder and the even-numbered pilot carriers are transmitted via the first antenna #0. In addition, only

the odd-numbered pilot carrier information of the built pilot carriers is included in the pilot symbol interval built by the second frame builder and the odd-numbered pilot carriers are transmitted via the first antenna #1. Accordingly, the receiving apparatus can distinguish between the transmission paths using the carrier indexes of the pilot symbol intervals received via the two signal paths. The structure of the pilot symbol intervals of Fig. 8 may be used when the multi-input/output encoding is performed so as to have two transmission paths.

- [183] In the above embodiment, a channel corresponding to a subcarrier of a half of a frame may be estimated from a symbol. Accordingly, high channel estimation performance can be obtained with respect to a transmission channel having a short coherence time.
- [184] FIG. 9 is a view showing another structure of the pilot symbol intervals according to an embodiment of the present invention. Even in the example of FIG. 9, different pilot carriers are transmitted to the pilot symbol intervals with respect to the paths according to the multi-input/output encoding method.
- [185] The pilot carrier transmission structure of the pilot symbol intervals shown in FIG. 9 is called a Hadamard type pilot carrier transmission structure. In the embodiment of FIG. 9, Hadamard conversion is performed in the unit of a symbol interval in order to distinguish between the two transmission paths. For example, pilot carriers obtained by adding the two pieces of pilot carrier information for the transmission paths are transmitted to the even-numbered symbol interval and a difference between the two pieces of pilot carrier information is transmitted to the odd-numbered symbol interval.
- [186] It can be explained along with the pilot symbol intervals including even-numbered intervals and odd-numbered intervals. The even-numbered symbol of the pilot carriers is transmitted via the first path (denoted by the first antenna (antenna #0)) and the second path (denoted by the second antenna (antenna #1)). Accordingly, the receiving apparatus can use the pilot carriers obtained by adding the pilot carriers transmitted via the two paths. The odd-numbered symbol of the pilot carrier is transmitted via a first path (first antenna (denoted by antenna #0)) and the pilot carrier having a phase difference of 180 degrees with respect to the odd-numbered symbol is transmitted via a second path (second antenna (denoted by antenna #1)). Accordingly, the receiver can recognize the sum of or the difference between the two pieces of pilot carrier information via the received pilot index so as to distinguish between the transmission paths.
- [187] In this embodiment, a channel corresponding to all subcarriers can be estimated and the estimation length of delay spread of the channel which can be processed by each transmission path can be extended by a symbol length.
- [188] The example of FIG. 9 is shown for facilitating the distinguishment between the two

pieces of pilot carrier information and shows both the two pieces of pilot carrier information in the frequency domain. In the even-numbered symbol interval and the odd-numbered symbol interval, impulses of the two pieces of pilot carrier information are located at the same frequency point.

[189] The embodiments of FIGs. 8 and 9 are examples of having two transmission paths. If the number of transmission paths is larger than 2, the pilot carrier information may be divided so as to be distinguished by the number of transmission paths similar to FIG. 8 or may be subjected to Hadamard conversion in the unit of a symbol interval and the converted information may be transmitted similar to FIG. 9.

[190] FIG. 10 is a schematic block diagram showing an apparatus for receiving a signal according to an embodiment of the present invention. The embodiment of FIG. 10 may be included in the DVB receiving apparatus.

[191] The embodiment of FIG. 10 includes a first receiver 900, a second receiver 905, a first synchronizer 910, a second synchronizer 915, a first demodulator 920, a second demodulator 925, a first frame parser 930, a second frame parser 935, a multi-input/output decoder 940, a first deinterleaver 950, a linear pre-coding decoder 960, a symbol demapper 970, a second deinterleaver 980, an inner decoder 990, a third interleaver 992, and an outer decoder 994.

[192] The first receiver 900 and the second receiver 905 receive RF signals, down-convert frequency bands, convert the signals into digital signals, and output the digital signals, respectively. The first synchronizer 910 and the second synchronizer 915 acquire synchronizations of the received signals output from the first receiver 900 and the second receiver 905 in the frequency domain and the time domain and output the synchronizations, respectively. The first synchronizer 910 and the second synchronizer 915 may use offset results of the data output from the first demodulator 920 and the second demodulator 925 in the frequency domain, for acquiring the synchronizations of the signal in the frequency domain, respectively.

[193] The first demodulator 920 demodulates the received data output from the first synchronizer 910. The first demodulator 920 converts the received data into the frequency domain and decodes the data dispersed in the subcarriers to the data allocated to the subcarriers. The second demodulator 925 demodulates the received data output from the second synchronizer 915.

[194] The first frame parser 930 and the second frame parser 935 distinguish between the reception paths according to the frame structures of the signals demodulated by the first demodulator 920 and the second demodulator 925 and output symbol data of the data symbol interval excluding the pilot symbol, respectively.

[195] The multi-input/output decoder 940 receives the data output from the first frame parser 930 and the second frame parser 935, decodes the data, and outputs a data

stream. The multi-input/output decoder 940 decodes the data stream received via the plurality of transmission antennas according to a method corresponding to the transmitting method of the multi-input/output encoder 170 shown in FIG. 1 and outputs a data stream.

- [196] The first deinterleaver 950 deinterleaves the data stream output from the multi-input/output decoder 940 and decodes the data into the sequence of the data before interleaving. The first deinterleaver 950 deinterleaves the data stream according to a method corresponding to the interleaving method of the third interleaver 160 shown in FIG. 1 and restores the sequence of the data stream.
- [197] The linear pre-coding decoder 960 performs an inverse process of the process of dispersing the data in the apparatus for transmitting the signal. The linear-pre-coding decoder 960 performs the decoding process in a manner corresponding to the encoding method of the linear pre-coder 150 of FIG. 1.
- [198] The linear pre-coding decoder 960 converts the input data into parallel data and restores the original data from the data dispersed via a decoding matrix. The decoding matrix for performing decoding becomes an inverse matrix of the encoding matrix of the apparatus for transmitting the signal. Alternatively, the received symbol data may be ML-decoded so as to correspond to the transmitting method and restored to the original data dispersed in the parallel data. That is, the received symbol data may be ML-decoded in consideration of an encoding rule of the transmitting apparatus. The restored data is converted into serial data and the serial data is output.
- [199] The linear pre-coding decoder 930 may be used or may not be used depending on whether or not the linear pre-coder 150 is used in the transmitting apparatus.
- [200] The symbol demapper 970 may restore the coded symbol data output from the linear pre-coding decoder 960 into a bit stream. The second deinterleaver 980 deinterleaves the data stream output from the symbol mapper 970 and restores the data into the sequence of the data before interleaving. The second deinterleaver 980 deinterleaves the data according to a method corresponding to the interleaving method of the second interleaver 130 shown in FIG. 1 and restores the sequence of the data stream.
- [201] The inner decoder 990 and the outer decoder 994 FEC-decodes the data, in which the sequence of the data stream is restored, detects an error which occurs in the received data, and corrects the error. The third interleaver 992 deinterleaves the data decoded by the inner decoder 990 and restores the sequence of the data. The third deinterleaver 992 deinterleaves the data according to a method corresponding to the interleaving method of the first interleaver 110 shown in FIG. 1. Similarly, the third interleaver 992 may be used or may not be used depending on whether or not the first interleaver 110 is used in the transmitting apparatus.
- [202] FIG. 11 is a view showing an example of the multi-input/output decoding method

according to an embodiment of the present invention. That is, FIG. 11 shows a decoding example of the receiving apparatus when the transmitting apparatus multi-input/output encodes data by the STBC method and transmits the encoded data. The transmitting apparatus may use two transmission antennas. This is only exemplary and another multi-input/output method may be applied.

[203] In the equation, $r(k)$, $h(k)$, $s(k)$ and $n(k)$ represent a symbol received by the receiving apparatus, a channel response, a symbol value transmitted by the transmitting apparatus, and channel noise, respectively. Subscripts s , i , 0 and 1 represent a s^{th} transmission symbol, an i^{th} reception antenna, 0^{th} transmission antenna and 1^{st} transmission antenna, respectively. "*" represents a complex conjugate. For example, $h_{s,i}^{s,i}(k)$ represents a response of a channel experienced by the transmitted symbol when a s^{th} symbol transmitted via the first transmission antenna is received by the i^{th} reception antenna. $R_{s+1,i}^{s+1,i}(k)$ represents a $s+1^{\text{th}}$ reception symbol received by the i^{th} reception antenna.

[204] According to the equation of FIG. 11, $r_{s,i}^{s,i}(k)$ which is a s^{th} reception symbol received by the i^{th} reception antenna becomes a value obtained by adding the s^{th} symbol value transmitted from the 0^{th} transmission antenna to the i^{th} reception antenna via the channel, the s^{th} symbol value transmitted from the 1^{st} transmission antenna to the i^{th} reception antenna via the channel and a sum $n_s(k)$ of the channel noises of the channels.

[205] $r_{s+1,i}^{s+1,i}(k)$ which is the $s+1^{\text{th}}$ reception symbol received by the i^{th} reception antenna becomes a value obtained by adding the $s+1^{\text{th}}$ symbol value $h_{s+1,0,i}^{s+1,0,i}$ transmitted from the 0^{th} transmission antenna to the i^{th} reception antenna via the channel, the $s+1^{\text{th}}$ symbol value $h_{s+1,1,i}^{s+1,1,i}$ transmitted from the 1^{st} transmission antenna to the i^{th} reception antenna via the channel and a sum $n_{s+1}(k)$ of the channel noises of the channels.

[206] FIG. 12 is a view showing a detailed example of FIG. 11 according to an embodiment of the present invention. FIG. 12 shows a decoding example when the transmitting apparatus multi-input/output encodes data by the STBC method and transmits the encoded data, that is, shows an equation which can obtain the received symbol when the data is transmitted using two transmission antennas and the data transmitted via the two transmission data is received using one antenna.

[207] If the transmitting apparatus transmits a signal using two transmission antennas and the receiving apparatus receives the signal using one transmission antenna, the number of transmission channels may be two. In the equation, h_0 and s_0 respectively represent a transmission channel response from the 0^{th} transmission antenna to the reception antenna and a symbol transmitted from the 0^{th} transmission antenna, and h_1 and s_1 respectively represent a transmission channel response from the 1st transmission antenna to the reception antenna and a symbol transmitted from the 1^{st} transmission antenna.

"*" represents a complex conjugate and s_0' and s_1' of the following equation represent restored symbols.

- [208] In addition, r_0 and r_1 respectively represent a symbol by the reception antenna at a time t and a symbol received by the reception antenna at a time $t+T$ after a transmission period T is elapsed, and n_0 and n_1 represent values of sums of channel noises of the transmission paths at reception times.
- [209] The signal (r_0, r_1) received via the reception antenna may be expressed by a value obtained by adding a value in which the signals transmitted via the transmission antennas are distorted by the respective transmission channels. The restored symbol (s_0', s_1') may be calculated using the received signal (r_0, r_1) and the channel response value (h_0, h_1) .
- [210] FIG. 13 is a schematic block diagram showing the deinterleaver and the FEC decoder according to an embodiment of the present invention. The inner decoder 990, the third deinterleaver 992 and the outer decoder 994 correspond to the inner decoder 120, the first interleaver 110 and the outer encoder 100 of FIG. 1, respectively. As the inner decoder and the outer decoder, the LDPC decoder 990 and the BCH decoder 994 are included, respectively.
- [211] The LDPC decoder 990 detects a transmission error which occurs in a channel and corrects the error, and the third deinterleaver 992 deinterleaves the input data and outputs the deinterleaved data. The BCH decoder 994 corrects the remaining error of the data decoded by the LDPC decoder 990 and removes an error floor.
- [212] FIG. 14 is a schematic block diagram showing another example of the apparatus for transmitting the signal according to an embodiment of the present invention. FIG. 15 is a schematic block diagram showing another example of the apparatus for receiving the signal according to an embodiment of the present invention.
- [213] FIGS. 14 and 15 show examples of applying a single-input single-output (SISO) method, instead of the multi-input multi-output method.
- [214] The signal transmitting apparatus of FIG. 14 includes an outer encoder 1300, a first interleaver 1310, an inner encoder 1320, a second interleaver 1330, a symbol mapper 1340, a linear pre-coder 1350, a third interleaver 1360, a frame builder 1370, a modulator 1380 and a transmitter 1390.
- [215] The signal receiving apparatus of FIG. 15 includes a receiver 1400, a synchronizer 1410, a demodulator 1420, a frame parser 1430, a first deinterleaver 1440, a linear pre-coding decoder 1450, a symbol demapper 1460, a second deinterleaver 1470, an inner decoder 1480, a third deinterleaver 1490 and an outer decoder 1495.
- [216] The signal transmitting apparatus and the signal receiving apparatus perform the same processes as FIGS. 1 and 10. Since the SISO method is applied to the signal transmitting/receiving apparatus of FIGS. 14 and 15 instead of the MIMO, the multi-

input/output encoding process and the multi-input/output decoding process are not used.

- [217] That is, the symbol data interleaved by the third interleaver 1370 so as to become robust against the frequency-selective fading of the channel is input to the frame builder 1370 and the frame builder 1370 builds frame data using the input symbol data and outputs the frame data. Similarly, the first interleaving process or the linear pre-coding process may not be used according to implementation embodiments. In the SISO method, the distinction between the transmission paths according to the multi-input/output of FIGs. 8 and 9 is not required.
- [218] In the signal receiving apparatus, the symbol data parsed by the frame parser 1430 is output to the first deinterleaver 1440 which performs the inverse process of the process of processing the data so as to become the robust against the frequency-selective fading of the channel by the transmitting apparatus.
- [219] In the signal transmitting apparatus of FIG. 1 or FIG. 14, the symbol mapper 140 or 1340 may map the input signal to symbols according to an optimal constellation method and output the mapped symbols.
- [220] FIG. 16 is a schematic view showing the positions of points of an optimal constellation according to an embodiment of the present invention. For optimal constellation mapping, the above-described constellation points shown in FIG. 2 may be used. The constellation points indicate the positions of the symbols mapped in the constellation. The numerals described on the constellation points indicate powers of the points.
- [221] The x-axis (horizontal axis of $y=0$) values of the optimal constellation points may be odd numbers (1, 3, 5, ...) or even numbers (2, 4, 6, ...) and the y-axis (vertical axis of $x=0$) values thereof may be an integral multiple of $\sqrt{3}$.
- [222] For example, the points positioned on the x axis have the odd numbers of 1, 3, 5, ... and the powers thereof are 1, 9, 25.... The points positioned on the y axis have the values of $\sqrt{3}$, $3\sqrt{3}$, $5\sqrt{3}$... and the powers thereof are 3, 27, 75, In the point having a power of 13, the x-axis value is 1 and the y-axis value is $2\sqrt{3}$. In the point having a power of 7, the x-axis value is 2 and the y-axis value is $\sqrt{3}$.
- [223] As shown, the transmission power of the symbols can be efficiently used by arranging points close to a circle form and arranging points as far as possible from a DC position. If the symbols are arranged according to the shown constellation, gaps between neighboring symbols are equalized and thus a SNR gain can be obtained. Accordingly, it is possible to minimize the transmission power of the symbols by arranging the symbols in a circle form centered on a DC (an original point of the constellation) according to the shown constellation. Hereinafter, a constellation in which the symbols are arranged such that the gaps between neighboring symbols are

equalized is called an optimal constellation. In the example of FIG. 16, three neighboring symbols are arranged in a regular triangle form in the constellation.

- [224] Instead of the positions of the points shown in FIG. 16, the positions obtained by symmetrically arranging the points with respect to the x axis, the y axis or the original point may be used. Alternatively, the positions obtained by rotating the points about the original point by any angle may be used. This may vary according to implementation embodiments.
- [225] FIG. 17 is a flowchart illustrating a method of deciding points of an optimal constellation according to an embodiment of the present invention. A necessary number of optimal constellation points are obtained from the constellation points shown in FIG. 17.
- [226] First, constellation points having a smallest power are selected from the constellation points shown in FIG. 17 (S1600). The number of constellation points selected is compared with the number of necessary constellation points (S1610). If the number of constellation points selected is smaller than the number of necessary constellation points, the step S1600 is performed again such that constellation points having a smallest power are selected from the points which are not previously selected. If the number of constellation points selected is larger than the number of necessary constellation points, the constellation points are removed in descending order of the power by the excessive number of points (S1620). A desired number of constellation points can be obtained by the above-described process, and the input data can be mapped to symbol data using the obtained constellation points.
- [227] FIGs. 18 to 21 are schematic views showing optimal constellations having points selected by the above-described process, according to the embodiments of the present invention. That is, FIGs. 18 to 21 are schematic views showing the positions of optimal constellations having 16 points, 64 points, 256 points and 256 points, respectively.
- [228] FIG. 20 shows another embodiment having positions different from the constellation point positions shown in FIG. 16, in which a symbol is arranged on the DC or symbols are arranged very close to the DC. In contrast, FIG. 21 shows an example in which 256 symbols are arranged such that a symbol is not arranged on the DC.
- [229] As described above, instead of the point positions of FIGs. 18 to 21, the positions obtained by symmetrically arranging points positioned according to the method described with reference to FIG. 3 with respect to the x axis, the y axis or the original point may be used. Alternatively, the positions obtained by rotating the points about the original point by any angle may be used. This may vary according to implementation embodiments.
- [230] In the case that the symbols are mapped according to the optimal constellation method, in the signal receiving apparatus of FIG. 9 or 14, the symbol demapper 970 or

1460 demaps the input signal to the symbol according to the optimal constellation method. Hereinafter, for convenience of description, it is assumed that the symbol mapper 140 or 1340 of FIG. 13 maps the symbol data according to the optimal constellation mapping method having 64 points. The number of points is decided for convenience of description and is only exemplary.

- [231] FIG. 22 is a schematic block diagram showing decision boundaries of the optimal constellation having 64 points. The symbol demapper 970 or 1460 demaps the received symbol data using the decision boundaries shown in FIG. 21. In the optimal constellation mapping method, the constellation has a honeycomb shape in order to efficiently use the transmission power, and, in the symbol demapper 970 or 1460, each symbol has a hexagonal decision boundary as shown in FIG. 21. Each of symbols corresponding to points positioned at outermost sides has a decision boundary of which one side is opened, instead of the hexagonal decision boundary.
- [232] If it is recognized that the input symbol data is positioned in a specific hexagon of the decision boundary shown in FIG. 22, the symbol demapper 970 or 1460 demaps the input symbol data to a symbol of the point corresponding to the specific hexagon.
- [233] FIG. 23 is a schematic block diagram showing the symbol demapper for demapping a received optimal constellation symbol according to an embodiment of the present invention. FIG. 24 is a schematic block diagram showing another symbol demapper for demapping a received optimal constellation symbol according to an embodiment of the present invention.
- [234] The symbol demapper 970 or 1460 may demap the symbol using all the decision boundaries of the optimal constellation shown in FIG. 22 at a time or may demap the symbol using a rectangular decision boundary like the symbol demapper of FIG. 23 or 24.
- [235] The symbol demapper of FIG. 23 includes a decision unit 2200, a second decision unit 2202, a first rotation unit 2204, a third decision unit 2206, a fourth decision unit 2208, a second rotation unit 2210, a fifth decision unit 2212, a sixth decision unit 2214, and a bit converter 2216.
- [236] When the symbol data is input to the symbol demapper 970 or 1460, the first decision unit 2200 decides whether the input symbol data is positioned in a rectangular decision boundary region using the rectangular decision boundary region formed by two opposite sides of each of hexagonal decision boundary regions. The second decision unit 2202 decides whether the input symbol data is positioned in a constellation edge region, that is, in an edge region, of which one side is opened, in all the decision boundaries shown in FIG. 22. The second decision unit 2202 decides whether the symbol is positioned in a decision boundary region denoted by a solid line among the edge regions of the constellation. The first decision unit 2200 and the second

decision unit 2202 decide the position of the input symbol data using the decision boundaries which are not rotated.

[237] The first rotation unit 2204 rotates the decision boundaries used in the first decision unit 2200 and the second decision unit 2202 by 60 degrees. The data output from the first rotation unit 2204 is input to the third decision unit 2206. The third decision unit 2206 decides whether the input symbol data is positioned in the rectangular decision boundary region using the rectangular decision boundary region formed by two opposite sides of the hexagonal decision boundary region among all the decision boundary regions rotated by 60 degrees. The fourth decision unit 2208 decides whether the input symbol data is positioned in the constellation edge region. The fourth decision unit 2208 decides whether the symbol is positioned in a decision boundary region denoted by a dashed dotted line, among the constellation edge regions. The third decision unit 2206 and the fourth decision unit 2208 decide the position of the input symbol data using the decision boundaries rotated by 60 degrees.

[238] The second rotation unit 2210 rotates all the decision boundaries used in the third decision unit 2206 and the fourth decision unit 2208 by 60 degrees. The data output from the second rotation unit 2210 is input to the fifth decision unit 2212. The fifth decision unit 2212 decides whether the input symbol data is positioned in the rectangular decision boundary using the rectangular decision boundary formed by two opposite sides in each of the hexagonal decision boundary regions among all the decision boundary regions rotated by 60 degrees again. The sixth decision unit 2214 decides whether the input symbol data is positioned in the constellation edge region. The sixth decision unit 2214 decides whether the symbol is positioned in a decision boundary region denoted by a dotted line, among the constellation edge regions. The fifth decision unit 2212 and the sixth decision unit 2214 may decide the position of the input symbol data using the decision boundaries rotated two times, that is, using the decision boundaries rotated from the original decision boundaries by 120 degrees.

[239] If the constellation edge regions are decided by the second decision unit 2202, the fourth decision unit 2208 and the sixth decision unit 2214, the decision of the position parallel to the x axis and the y axis is performed using a saturation method and the decision of the position of an oblique line is performed using a linear equation corresponding to the oblique line.

[240] The bit converter 2216 converts the information decided by the determination units, that is, the value decided to the symbol of the point corresponding to the input symbol data, into bit data corresponding to the decided symbol value.

[241] All the two times of rotation processes and the six times of decision processes may be performed. Alternatively, if the symbol of the point corresponding to the received symbol data is decided by a specific decision of six times of decision processes, the

decision information may be output to the bit converter 2216 and may be converted to the bit data without further performing the rotation or decision process. This may vary according to implementation examples. Although the rotation units rotate the decision boundaries by 60 degrees in this embodiment, the decision boundaries may be rotated by -60 degrees.

[242] FIG. 23 is a schematic block diagram showing another symbol demapper for demapping a received optimal constellation symbol according to an embodiment of the present invention. The symbol demapper of FIG. 23 uses a recursive decoding method using a feedback.

[243] The symbol demapper of FIG. 23 includes a buffer 2220, a selector 2222, a first decision unit 2224, a second decision unit 2226, a rotation unit 2228, and a bit converter 2230.

[244] The buffer 2220 temporarily stores and outputs the input symbol data. The selector 2222 receives the symbol data output from the buffer 2220 and the symbol data output from the rotation unit 2228 and outputs one piece of symbol data. The selector 2222 outputs the symbol data fed back from the rotation unit 2228 when the recursive decoding method is performed and outputs the symbol data received from the buffer 2220 when a decision process is performed with respect to new symbol data.

[245] The first decision unit 2224 decides whether the input symbol data is positioned in the rectangular decision boundary region using the rectangular decision boundary region formed by two opposite sides in each of the hexagonal decision boundary regions. The second decision unit 2226 decides whether the input symbol data is positioned in a constellation edge region, that is, an edge region, of which one side is opened, in the decision boundaries shown in FIG. 21. The second decision unit 2226 decides whether the input symbol data is positioned in a decision boundary region denoted by a solid line (non-rotation), a dashed dotted line (one time of rotation), or a dotted line (two times of rotation) according to the number of times of rotation. The rotation unit 1028 may rotate the decision boundaries used in the first decision unit 2224 and the second decision 2226 by 60 degrees. Alternatively, the decision boundaries are rotated by -60 degrees according to implementation embodiments.

[246] The bit converter 2230 converts the information decided by the decision units, that is, the value decided to the symbol of the point corresponding to the input symbol data, into bit data corresponding to the decided symbol value.

[247] The symbol demapper of FIG. 24 may perform all the two times of rotation processes and the six times of decision processes. Alternatively, if the symbol of the point corresponding to the received symbol data is decided by the first decision unit 2224 and the second decision unit 2226 during the recursive decoding process, the decision information may be output to the bit converter 2230 and may be converted into the bit

data. This may vary according to implementation examples.

[248] FIG. 25 is a schematic view showing a process of demapping a received symbol according to an embodiment of the present invention. FIG. 25 shows four hexagonal decision boundary regions in all the decision boundaries.

[249] FIG. 25 shows a deciding process of a decision unit which decides whether the symbol data is positioned in the rectangular decision boundary region using the rectangular decision boundary region formed by two opposite sides in the hexagonal boundary region, among the decision units of FIG. 24 or 25.

[250] First, in a first decision boundary form which is not rotated, it is decided whether the input symbol data is positioned in the rectangular decision boundary region, using the rectangular decision boundary region formed by two opposite right and left sides of each of the hexagonal decision boundary regions. If the decision is completed, all the decision boundaries are rotated by 60 degrees and it is decided whether the input symbol data is included in the rectangular decision boundary region, using the rectangular decision boundary region formed by two opposite right and left sides of each of the hexagonal decision boundary regions. Then, all the decision boundaries are rotated by 60 degrees again and it is decided whether the input symbol data is included in the rectangular decision boundary region, using the rectangular decision boundary region formed by two opposite sides of each of the hexagonal decision boundary regions. In FIG. 25, a second decision boundary form and a third decision boundary form represent regions which are subjected to the decision process while performing the rotation process.

[251] By two times of rotation processes, the rectangular decision boundary regions cover the whole hexagonal region. Accordingly, each of the hexagonal decision boundary regions can be demapped to the symbols corresponding to the points having the hexagonal decision boundary region.

[252] According to the implementation example, if it is determined that the input symbol data is positioned in the rectangular decision boundary region, the decision process may be completed without further performing the rotation and the decision. Although the rectangular decision boundary region formed by two opposite right and left sides of the hexagon is used, a region using two opposite sides other than the right and left sides, for example, a parallelogram decision boundary region may be first used or a rectangular decision boundary region formed by two upper and lower sides may be first used.

[253] FIG. 26 is a schematic view showing a process of demapping a received optimal constellation symbol in an edge region according to an embodiment of the present invention.

[254] FIG. 26 is a view showing all the decision boundaries of a 64-point optimal constell

ation mapping method. FIG. 26 shows a deciding process of the decision unit which decides whether input symbol data is positioned in the constellation edge region, that is, the edge region of which one side is opened, by the decision units of FIGS. 23 and 24.

[255] First, in a first decision boundary form which is not rotated, it is decided whether the input symbol data is positioned in a region denoted by a solid line among the constellation boundary regions. If the decision is completed, all the decision boundaries are rotated by 60 degrees and it is decided whether the input symbol data is included in a region denoted by a dashed dotted line among the constellation boundary regions. Then, all the decision boundaries are rotated by 60 degrees again and it is decided whether the input symbol data is included in a region denoted by a dotted line among the constellation boundary regions.

[256] According to the implementation embodiments, the sequence of the region denoted by the solid line, the region denoted by the dashed dotted line and the region denoted by the dotted line may be changed. For example, after the region denoted by the dotted line is decided in the first decision boundary form of FIG. 24, the region denoted by the solid line (one time of rotation) and the region denoted by the dashed dotted line (two times of rotation) may be decided.

[257] Similarly, although the decision boundaries are rotated by 60 degrees in the examples of FIGS. 23 and 24, the decision boundaries may be rotated by -60 degrees according to implementation embodiments.

[258] FIG. 27 is a schematic block diagram showing another example of an apparatus for transmitting a signal according to an embodiment of the present invention. FIG. 27 shows an example of applying a multi-mapping method to the signal transmitting apparatus of FIG. 1.

[259] The embodiment of FIG. 27 includes an outer encoder 2500, an inner encoder 2510, a first interleaver 2520, a multi-mapper 2530, a linear pre-coder 2540, a second interleaver 2550, a frame builder 2560, a modulator 2570 and a transmitter 2580. According to implementation examples, an outer interleaver may be inserted between the outer encoder 2500 and the inner encoder 2510 and a multi-input encoder may be inserted between the second interleaver 2550 and the frame builder 2560.

[260] The outer encoder 2500 and the inner encoder 2510 encode an input signal and output the encoded signal such that an error generated in transmitted data is detected and corrected by the receiving apparatus. That is, the outer encoder 2500 and the inner encoder 2510 configure a FEC encoder. The type of the encoder may be changed according to the coding method used in the signal transmitting system.

[261] The first interleaver 2520 shuffles the data output from the inner encoder 2510 to random positions so as to become robust against a burst error which occurs in the data

when the signal output from the inner coder 2510 is transmitted. For example, the first interleaver 2520 can use a convolution interleaver or a block interleaver. The interleaving method of the first interleaver 2520 may be changed according to the method used in the signal transmitting system.

- [262] The multi-mapper 2530 maps the data interleaved by the first interleaver 2520 to symbols according to the transmitting method. The multi-mapper 2530 maps the input data to symbol data using a mixture of a plurality of mapping methods. As the mapping method, a quadrature amplitude modulation (QAM), a quadrature phase shift keying (QPSK), an amplitude phase shift keying (APSK), a pulse amplitude modulation (PAM) or an optimal constellation may be used.
- [263] Using the multi-mapping method, a signal-to-noise ratio (SNR) gain can be obtained by a method of mapping to a small constellation size and a capacity gain can be obtained by a method of mapping to a large constellation size. Accordingly, it is possible to adjust the SNR gain and the capacity gain and increase transmission efficiency by adjusting the mixture ratio of the mapping methods.
- [264] The linear pre-coder 2540 disperses input symbol data into several pieces of output symbol data so as to decrease a probability that all information is lost due to fading when experiencing frequency-selective fading of a channel. The linear pre-coder 2540 may not be used according to implementation embodiments.
- [265] The second interleaver 2550 interleaves the symbol data output from the linear pre-coder 2540 again such that the symbol data does not experience the same frequency-selective fading. The second interleaver 2550 may use a convolution interleaver or a block interleaver.
- [266] The frame builder 2560 inserts a pilot signal into a data interval to build a frame such that the interleaved signal is modulated by an orthogonal frequency division multiplex (OFDM) method. The modulator 2570 inserts a guard interval into the data output from the frame builder 2560 and modulates the inserted data such that the data is transmitted in a state of being carried in OFDM subcarriers. The transmitter 2580 converts the digital signal having the guard interval and the data interval, which is output from the modulator 2570, into an analog signal and transmits the converted analog signal.
- [267] FIG. 28 is a schematic block diagram showing the multi-mapper according to the embodiment of the present invention. The multi-mapper 2530 includes a bitstream distributor 2531, a first mapper 2532, a second mapper 2533, ..., an N^{th} mapper 2534 and a symbol interleaver 2535.
- [268] The bitstream distributor 2531 distributes the input bit data into several mappers. The bitstream distributor 2531 distributes a necessary number of bit data in order to map the bit data to the symbols according to the mapping methods of the mappers.

- [269] The bit data distributed by the bitstream distributor 2531 is output to the mappers (the first mapper 2532 to the N^{th} mapper 2534). The first mapper 2532 to the N^{th} mapper 2534 configure a mapping unit for mapping the input bit data to the symbol data. The mappers map the input bit data to the symbol data according to the respective mapping methods. As the mapping methods, the QAM, the QPSK, the APSK, the PAM, and the optimal constellation may be used.
- [270] The mappers (the first mapper 2532 to the N^{th} mapper 2534) may be equal to one another in the mapping method and different from one another in the number of bit data included in one symbol or may be different from one another in the mapping method. For example, while all the first mapper 2532 to the N^{th} mapper 2534 use the QAM method, the first mapper 2532 may map the symbol by the 16QAM method, the second mapper 2533 may map the symbol by the 64QAM method, and the N^{th} mapper 2534 may map the symbol by the 256QAM method. Alternatively, the first mapper 2532 may map the symbol by the QAM method and the N^{th} mapper 2534 may map the symbol by the optimal constellation method. This may vary according to the implementation embodiments.
- [271] The mappers (the first mapper 2532 to the N^{th} mapper 2534) map the input data to symbols according to predetermined mapping methods and output the mapped data.
- [272] The symbol interleaver 2535 interleaves and aligns the symbol data output from the mappers to one symbol stream and outputs the symbol stream. As the interleaving method, a block interleaving method, a convolution interleaving method or an interleaving method using bit-reversed addressing, which sets the symbols to one block and outputs the addresses corresponding to the order of the block in bit-reversed order, may be used. Alternatively, the symbol data output from the mappers may be aligned and output without interleaving the symbol data. This may vary according to the implementation embodiments.
- [273] FIG. 29 is a view showing a bitstream distributing method according to an embodiment of the present invention. That is, the bitstream distributing method is an example of the method of distributing the bitstream by the bitstream distributor 2531.
- [274] In the bitstream distributing method of FIG. 29, the input bit data is stored in a memory space having a matrix shape in a predetermined pattern and the data is read and output in a pattern different from the storage pattern. In this case, a virtual interleaver function can be obtained.
- [275] For convenience of description, it is assumed that the number of mappers to which the input bit data will be distributed is 2. For example, if the length of one block input to the bitstream distributor 2531 is MN bits, the block is divided by M and data is stored in the memory space from a first row and a first column. The data is stored from the first row of the first column to an M^{th} row of the first column and, when all the

rows of the first column are filled up, the data is stored from the first row to the M^{th} row of a next column (second column). The data may be stored in the above-described order up to the M^{th} row of an N^{th} column. At this time, the position of a most significant bit (MSB) of the memory space is an uppermost left part and the position of a least significant bit (LSB) thereof is a lowermost right part.

[276] In the two mappers, if a ratio of bits to symbols of the first mapper and the second mapper is $M\text{-}R\text{:}R$, the data stored in the memory space is divided into $M\text{-}R$ rows and R rows. The divided bit data is output in a row direction. That is, the data is read and output from the first row and the first column to the first row and the N^{th} column and, when all the data of the row is read, the data is read and output from the first column of a next row (the second row) in the right direction. The data is read in the above-described order up to the $M\text{-}R^{\text{th}}$ row and is output to the first mapper. Even with respect to the R rows, the data is read in the row direction and is output to the second mapper.

[277] In the present embodiment, the size of the block, the storage pattern, and the read pattern are only exemplary and may vary according to the implementation examples. For example, the input bit data can be distributed to the mappers in input order.

[278] FIG. 30 is a schematic block diagram showing an apparatus for receiving a signal according to an embodiment of the present invention. The embodiment of FIG. 30 is the receiving apparatus corresponding to the transmitting apparatus of FIG. 27 and shows the case of using a multi-mapping method in the signal receiving apparatus of FIG. 10.

[279] The embodiment of FIG. 30 includes a receiver 2800, a synchronizer 2810, a demodulator 2820, a frame parser 2830, a first deinterleaver 2840, a linear pre-coding decoder 2850, a multi-demapper 2860, a second deinterleaver 2870, an inner decoder 2880 and an outer decoder 2890. According to implementation embodiments, an outer interleaver may be inserted between the inner decoder 2880 and the outer decoder 2890 and a multi-input/output decoder may be inserted between the frame parser 2830 and the first deinterleaver 2840.

[280] The receiver 2800 down-converts the frequency band of a received RF signal, converts the signal into a digital signal, and outputs the digital signal. The synchronizer 2810 acquires synchronization of the received signal output from the receiver 2800 in a frequency domain and a time domain and outputs the synchronization. The synchronizer 2810 may use an offset result of the data output from the demodulator 2820 in the frequency domain, for acquiring the synchronization of the signal in the frequency domain.

[281] The demodulator 2820 demodulates the received data output from the synchronizer 2810 and removes the guard interval. The demodulator 2820 may convert the received

data into the frequency domain and decode data values dispersed into the subcarriers to the values allocated to subcarriers. The frame parser 2830 may output symbol data of the data symbol interval excluding the pilot symbol according to the frame structure of the signal demodulated by the demodulator 2820.

- [282] The first deinterleaver 2840 deinterleaves the data stream output from the frame parser 2830 and restores the data into the sequence of the data before interleaving. The first deinterleaver 2840 deinterleaves the data stream according to a method corresponding to the interleaving method of the second interleaver 2550 shown in FIG. 25 and restores the sequence of the data stream.
- [283] The linear pre-coding decoder 2850 performs an inverse process of the linear pre-coding process of dispersing the data in the apparatus for transmitting the signal and restores original data dispersed in the data input to the linear pre-coding decoder 2850. The linear pre-coding decoder 2850 is used only when the linear pre-coder is used in the transmitting apparatus.
- [284] The multi-demapper 2860 may restore the symbol data restored by the linear pre-coding decoder 2850 into a bitstream. As the demapping method of the multi-demapper 2860, a method corresponding to the mapping method used by the symbol mapper 2530 included in the apparatus for transmitting the signal shown in FIG. 27 is used.
- [285] The second deinterleaver 2870 performs the inverse process of the interleaving process of the bit data stream demapped by the multi-demapper 2860. The second deinterleaver 2870 performs the deinterleaving process corresponding to the first interleaver 2520 of FIG. 27. The inner decoder 2880 may decode the deinterleaved data and correct the error included in the data. The outer decoder 2890 performs an error correction decoding process with respect to the bit data decoded by the inner decoder 2880 and outputs the decoded bit data. The inner decoder 2880 and the outer decoder 2890 decode the data according to the decoding methods corresponding to the inner encoder 2510 and the outer encoder 2500 of FIG. 27.
- [286] The first interleaver 3020 shuffles the data stream to random positions so as to become robust against a burst error which may occur in the data when the signal output from the inner encoder 3010 is transmitted. The symbol mapper 3030 maps the data interleaved by the first interleaver 3020 to symbol data according to the transmitting method. Alternatively, an encoded symbol mapping method may be used in the symbol mapper 3030. For example, the data may be mapped to the encoded symbols using a trellis coded modulation method.
- [287] The linear pre-coder 3040 disperses input symbol data into several pieces of output symbol data so as to decrease a probability that all information is lost due to fading when experiencing frequency-selective fading of a channel. The linear pre-coder 3040

may not be used according to implementation embodiments.

- [288] The second interleaver 3050 interleaves the symbol data output from the linear precoder 3040 again such that the symbol data does not experience the same frequency-selective fading. The second interleaver 3050 may use a convolution interleaving method or a block interleaving method.
- [289] The frame builder 3060 inserts a pilot signal into a data interval to build a frame such that the interleaved signal is modulated by an orthogonal frequency division multiplex (OFDM) method. The modulator 3070 inserts a guard interval into the data output from the frame builder 3060 and modulates the inserted data such that the data is transmitted in a state of being carried in OFDM subcarriers. The transmitter 3080 converts the digital signal having the guard interval and the data interval, which is output from the modulator 3070, into an analog signal and transmits the converted analog signal.
- [290] FIG. 31 is a schematic block diagram showing the multi-demapper according to the embodiment of the present invention. The multi-demapper 2860 includes a symbol deinterleaver 2861, a first demapper 2862, a second demapper 2863, ..., an N^{th} demapper 2864, and a bitstream merger 2865.
- [291] The symbol deinterleaver 2861 deinterleaves the input symbol data and restores an original symbol data sequence. The deinterleaving method of the deinterleaver 2861 corresponds to the interleaving method of the symbol interleaver 2535 in the multi-mapper 2530 of FIG. 26. The symbol deinterleaver 2861 transmits the deinterleaved symbol data to the demappers corresponding to the mapping methods.
- [292] The demappers (the first demapper 2862 to the N^{th} demapper 2864) convert the received symbol data into bit data according to the respective demapping methods. The first demapper 2862 to the N^{th} demapper 2864 configure a demapping unit for demapping the input symbol data to the bit data. The demapping methods of the first demapper 2862 to the N^{th} demapper 2864 correspond to the mapping methods of the first mapper 2532 to the N^{th} mapper 2534 of FIG. 28, respectively.
- [293] The bitstream merger 2865 receives the bit data output from the demappers and outputs one bitstream. The bitstream merger 2865 merges the bit data to the bitstream using the method corresponding to the method distributed by the bit stream distributor 2531 of FIG. 28.
- [294] As described the above, if the symbol mapping is different from a service to another service, the multi-demapper 2860 may obtain the identification information of the service and may allocate the symbols according to each of the identification information. According to the above embodiment, the multi-demapper 2860 may split respectively the symbols for a first program and a second program and may output the split symbols to the first demapper 2862 and the second demapper 2864. And, the first

demapper 2862 demaps the its input data to symbols, and the second demapper 2864 demaps the its input data to symbols according to their symbol mapping methods. And the bitstream merger 2865 may output the interleaved data after interleaving the respective program data. Although the symbol mapping methods are different along with programs, contents and channels, the same embodiment as this can be applied.

[295]

[296] Fig. 32 is a view representing another embodiment of the multi-demapper. The symbol deinterleaver 2861 receives the interleaved symbol, deinterleaves the received symbols and outputs the deinterleaved symbols. A first demapper 2862 demaps the symbols mapped by a first symbol mapping method among the deinterleaved symbols. Similarly, a second demapper 2863 and a Nth demapper 2864 demap the symbols according to each of the respective symbol mapping methods (hybrid symbol mapping method) among the deinterleaved symbols, and output the demapped symbols, respectively. For example, the first demapper 2862 to the Nth demapper 2864 can demap symbols, which are mapped according to different optimal constellation symbol mapping methods. The demapping values demapped by each of the demapper 2862, ..., 2864 may be reliability values for soft decision like log likelihood ratio (LLR) values. The reliability value output by each of the demappers (for example, LLR) can be influenced by each of constellation sizes. Namely, when the symbols are mapped by the hybrid symbol mapping methods, the demapped values can be determined to the bit streams along with reliability values, each of which is determined by the corresponding constellation size.

[297] Therefore, a first scaler 2866a can scale an LLR value by the demapping result and output the scaled LLR value. Similarly, each of a second scaler 2866n to a Nth scaler can scale a reliability value which is output by the corresponding demapper into a scaling value which is inversely proportional to each of the corresponding constellation sizes.

[298] The bit stream merger 2865 merges the bit streams based on normalized reliability values output by the scalers, and output the merged bit streams to one bit stream. The embodiment can be used to the multi-demapper in Fig. 30.

[299]

[300] Fig. 33 is a view representing an embodiment of the exemplified scaler. The scaler may include a scaling factor generator 2867 and a multiplier 2868. The scaling factor generator 2867 generates a scaling factor depending on a constellation size. The scaling factor can be a reciprocal of an average symbol amplitude in each of the constellation sizes or a reciprocal of an average power of each constellation.

[301] The multiplier 2868 multiplies a reliability value output by one demapper among a plurality of the demappers by the scaling factor according to the constellation size used

by the corresponding demapper. When the outputs from the demappers in the multi-demapper are multiplied by the scaling factors along with the constellation sizes corresponding to the symbol mapping methods, respectively, each of the values multiplied by the scalers can be the reliability value, which is the normalized value of the output from each of the demappers. Therefore, if this embodiment is included in the multi-demapper, the inner decoder 2880 and the outer decoder 2890 in Fig. 30 can perform the error correction more exactly.

[302]

[303] FIG. 34 is a schematic block diagram showing an apparatus for transmitting a signal using multi-encoding according to an embodiment of the present invention. FIG. 34 shows an example of applying a multi-encoding method to the signal transmitting apparatus of FIG. 1.

[304] The embodiment of FIG. 34 includes an outer encoder 3000, an multi-encoder 3010, a first interleaver 3020, a symbol mapper 3030, a linear pre-coder 3040, a second interleaver 3050, a frame builder 3060, a modulator 3070 and a transmitter 3080.

[305] The outer encoder 3000 and the inner encoder 3010 encode respective input signals and output the encoded signals such that an error generated in transmitted data is detected and corrected by a receiving apparatus. The outer encoder 3000 encodes the input data in order to improve transmission performance of the input signal. The types of the encoders vary according to the coding methods used in the signal transmission system.

[306] The multi-encoder 3010 codes the data encoded by the outer encoder 3000 again in order to prevent an error from being generated in the transmitting process. The multi-encoder 3010 encodes the input data by using a hybrid of a plurality of encoding methods. For example, as the encoding method, a convolution coding method, a Reed-Solomon (RS) coding method, a low density parity check (LDPC) coding method, a turbo coding method or the like may be used.

[307] Using the multi-encoding method, a SNR gain can be obtained by an encoding method having a lower code rate and a capacity gain can be obtained by an encoding method having a high code rate. Accordingly, it is possible to adjust the SNR gain and the capacity gain and increase transmission efficiency by adjusting the mixture ratio of the encoding methods.

[308]

[309] FIG. 35 is a schematic block diagram showing the multi-encoder according to the embodiment of the present invention. The multi-encoder 3010 includes a bitstream distributor 3011, a first encoder 3012, a second encoder 3013, ..., an Nth encoder 3014 and a bitstream merger 3015.

[310] The bitstream distributor 3011 distributes the input bit data into several encoders.

The bitstream distributor 3011 distributes a necessary number of bit data according to the encoding methods of the encoders. The bitstream distributor 3011 may distribute the input bit data to the encoders according to the bitstream distributing method of FIG. 29 or in the input order of the input bit data. The distributing method may vary according to the implementation embodiments.

[311] The bit data distributed by the bitstream distributor 3011 is output to the encoders (the first encoder 3012 to the N^{th} encoder 3014). The first encoder 3012 to the N^{th} encoder 3014 configure an encoding unit for encoding the input bit data and outputting the encoded data. The encoders encode the input bit data according to the respective encoding methods. As the encoding methods, the channel coding methods such as the convolution coding method, the RS coding method, the LDPC coding method and the turbo coding method may be used.

[312] The encoders (the first encoder 3012 to the N^{th} encoder 3014) may be equal to one another in the encoding method and different from one another in the code rate or may be different from one another in the encoding method. For example, while all the first encoder 3012 to the N^{th} mapper 3014 use the LDPC method, the code rates of the encoders may be different from one another. Alternatively, the first encoder 3012 may encode the data using the LDPC and the N^{th} encoder 3014 may encode the data using the turbo coding method. This example may vary according to the implementation embodiments.

[313] The bitstream merger 3015 receives the bit data output from the encoders and merges the bit data to one bit data stream. The bitstream merger 3015 may merge the bit data to one bit data stream in the manner inverse to the distributing method of the bitstream distributor 3015 or another predetermined rule. This may vary according to the implementation embodiments, and the virtual interleaving effect can be obtained according to the merging method.

[314] FIG. 36 is a schematic block diagram showing an apparatus for receiving a multi-encoded signal according to an embodiment of the present invention. The receiving apparatus of FIG. 36 corresponds to the transmitting apparatus of FIG. 34.

[315] The embodiment of FIG. 34 includes a receiver 3200, a synchronizer 3210, a demodulator 3220, a frame parser 3230, a first deinterleaver 3240, a linear pre-coding decoder 3250, a symbol demapper 3260, a second deinterleaver 3270, a multi-decoder 3280 and an outer decoder 3290.

[316] The components of the receiving apparatus of FIG. 34 are substantially similar to those of the receiving apparatus shown in FIG. 32. Hereinafter, the portions different from those of FIG. 32 will be described.

[317] The symbol demapper 3260 may restore the symbol data restored by the linear pre-coding decoder 3250 to a bitstream. The symbol demapper 3260 demaps the symbol

data using the method corresponding to the mapping method of the symbol mapper 3030 of FIG. 32.

- [318] The multi-decoder 3280 receives the bit data deinterleaved by the second deinterleaver 3270 and decodes the bit data according to the methods corresponding to the encoding methods of the transmitting apparatus.
- [319] FIG. 37 is a schematic block diagram showing the multi-decoder according to the embodiment of the present invention. The multi-decoder 3280 includes a bitstream distributor 3281, a first decoder 3282, a second decoder 3283, ..., an N^{th} decoder 3284, and a bitstream merger 3285.
- [320] The bitstream distributor 3281 distributes the input bit data into several decoders. The bitstream distributor 3281 distributes the bit data according to the method corresponding to the method of merging the bit data to one bit data stream by the bitstream merger 3015 of the multi-encoder of FIG. 35. That is, the bitstream distributor 3281 distributes the bit data in the manner inverse to the method of receiving and merging the bit data to the bit data stream by the bitstream merger 3015 of the multi-encoder.
- [321] The bit data distributed by the bitstream distributor 3281 is output to the decoders (the first decoder 3282 to the N^{th} decoder 3284). The first decoder 3282 to the N^{th} decoder 3284 configure a decoding unit for decoding the input bit data and outputting the decoded data. The decoders decode the input bit data according to the respective decoding methods. The decoding methods correspond to the encoding methods of the multi-encoder of FIG. 35.
- [322] The bitstream merger 3285 receives the bit data output from the decoders and merges the bit data to one bit data stream. The bitstream merger 3285 merges the bit data in the manner inverse to the method of distributing the bit data by the bitstream distributor 3011.
- [323] The outer decoder 3290 performs an error correction decoding process with respect to the bit data decoded by the multi-decoder 3280 and outputs the decoded data. That is, the multi-decoder 3280 and the outer decoder 3290 decode the data by the decoding methods corresponding to the multi-encoder 3010 and the outer encoder 3000 of FIG. 30.
- [324] FIG. 38 is a schematic block diagram showing an apparatus for transmitting a signal using a multi-encoding method and a multi-mapping method according to an embodiment of the present invention. As shown in FIG. 38, the signal transmitting apparatus can be implemented using both the multi-encoding method and the multi-mapping method described in FIGS. 27 and 34.
- [325] The signal transmitting apparatus includes an outer encoder 3400, a multi-encoder 3410, a first interleaver 3420, a multi-mapper 3430, a linear pre-coder 3440, a second

interleaver 3450, a frame builder 3460, a modulator 3470, and a transmitter 3480. The blocks are equal to those of FIGs. 27 and 34 and thus the description thereof will be omitted.

[326] FIG. 39 is a schematic block diagram showing an apparatus for receiving a multi-encoded and multi-mapped signal according to an embodiment of the present invention. The signal receiving apparatus of FIG. 39 corresponds to the signal transmitting apparatus of FIG. 38 and includes a receiver 3500, a synchronizer 3510, a demodulator 3520, a frame parser 3530, a first deinterleaver 3540, a linear pre-coding decoder 3550, a multi-demapper 3560, a second deinterleaver 3570, a multi-decoder 3580 and an outer decoder 3590. Similarly, the blocks of the signal receiving apparatus are equal to those of FIGs. 30 and 36 and thus the description thereof will be omitted.

[327] FIG. 40 is a schematic block diagram showing another example of an apparatus for receiving a multi-encoded and multi-mapped signal according to an embodiment of the present invention. The signal receiving apparatus includes a receiver 3600, a synchronizer 3610, a demodulator 3620, a frame parser 3630, a first deinterleaver 3640, an equalizer 3650, a linear pre-coding decoder 3660, a multi-demapper 3670, a channel estimator 3680, a second deinterleaver 3690, a multi-decoder 3692 and an outer decoder 3694.

[328] In a system using a multi-mapping method, a symbol having a small constellation size has a minimum required SNR which is relatively lower than that of a symbol having a large constellation size at the time of mapping the symbols. Accordingly in order to further increase the capacity, the symbol having the small constellation size can be utilized as a pilot symbol. That is, if separate pilot signals are not used or the function of some of the pilot symbols is performed using the symbol having the small constellation size, the capacity is increased by the number of pilot signals removed. In the case that the symbol having the small constellation size is used, the channel is estimated on the basis of a value decided by receiving the symbol.

[329] The minimum required SNR of the symbol having the large constellation size is relatively higher than that of the symbol having the small constellation size. Accordingly, since the reliability of the symbol having the small constellation size is relatively high in the SNR period in which the symbol having the large constellation size is decoded, the symbol having the small constellation size may be used as the pilot symbol.

[330] The distinguishment between the symbol having the small constellation size and the symbol having the large constellation size may vary according to the implementation embodiments. For example, in the case that the symbol having at least a predetermined number of constellation points is recognized as the symbol having the large constellation size, the number of points which is a criterion for distinguishing between the

symbols may vary according to the implementation embodiments.

- [331] In the case that the symbol data having the small constellation size and the symbol data having the large constellation size are multi-mapped, the signal transmitting apparatus can insert the pilot into the multi-mapped symbol data and transmit the inserted symbol data. As described above, in the case that the symbol data having the small constellation size is used as the pilot symbol, the signal transmitting apparatus may insert the symbol data having the small constellation size into the pilot insertion position instead of the pilot and may transmit the inserted data.
- [332] In the case that the symbol data having the small constellation size is inserted into the pilot insertion position, the symbol data having the small constellation size may be inserted into the overall pilot insertion position or the symbol data having the small constellation size may be inserted into a portion of the pilot insertion position and the pilot may be inserted into the remaining portion of the pilot insertion position.
- [333] For example, in the signal transmitting apparatus of FIG. 38 the frame builder 3460 may insert the symbol data having the small constellation size into the overall the pilot insertion position of the frame so as to build the frame. Alternatively, the frame builder 3460 may insert the symbol data having the small constellation size into a portion of the pilot insertion position of the frame and insert the pilot into the remaining portion of the frame, thereby building the frame. In consideration of a channel state and the transmitting/receiving system, any one of the above-described methods may be selected and implemented.
- [334] Although the multi-encoding method is used in FIG. 38, the inner encoding method using only one encoding method may be used instead of the multi-encoding method using the plurality of encoding methods.
- [335] FIG. 40 is a view showing the apparatus for receiving and processing the signal in the case that the signal transmitting apparatus of FIG. 38 transmits the signal using the symbol data having the small constellation size as the pilot symbol.
- [336] Hereinafter, for convenience of description, the blocks of FIG. 40 which do not overlap with the blocks of FIG. 39 will be described.
- [337] The frame parser 3630 parses the frame data demodulated by the demodulator 3620. In the case that the symbol data having the small constellation size is inserted into the overall pilot insertion position so as to build the frame in the signal transmitting apparatus, the frame parser 3630 extracts the symbol data inserted into the pilot position and restores the symbol data together with the remaining symbol data. If the symbol data having the small constellation size is inserted into a portion of the pilot insertion position and the pilot is inserted into the remaining portion so as to build the frame in the signal transmitting apparatus, the frame parser 3630 extracts the pilot and the symbol data having the small constellation size and restores the symbol data.

[338] Hereinafter, for convenience of description, the case that the symbol data having the small constellation size is inserted into a portion of the pilot insertion position and the pilot is inserted into the remaining portion so as to build the frame will be described.

[339] The channel estimator 3680 estimates a transmission channel using the input/output information of the multi-demapper 3670 and the pilot output from the frame parser 3630. In the case that the channel is estimated using the pilot output from the frame parser 3630, if the pilot carried in a k^{th} carrier is $P_r(k)$ and the promised pilot known by the receiver is $P_t(k)$, a channel transfer function (CTF) is expressed by Math Figure 2.

[340] [Math Figure 2]

[341]

$$\Delta = 100 \times \left(\frac{1}{10} - \frac{1}{M} \right) \%$$

[342] $H_p(k)$ denotes a CTF estimated using the pilot.

[343] In the case that the channel is estimated using the symbol data having the small constellation size, which is inserted into the pilot insertion position, if the received symbol data, that is, the symbol data input to the multi-demapper 3670, is $Y_r(k)$ and the decided symbol data, that is, the symbol data output from the multi-demapper 3670, is $Y_t(k)$, the CTF is expressed by Math Figure 3.

[344] [Math Figure 3]

[345]

$$H_d(k) = \frac{Y_r(k)}{Y_t(k)}$$

[346] $H_d(k)$ denotes a CTF estimated using the symbol data having the small constellation size. The division may be performed by designing a divider, by computing the reciprocal of a denominator or multiplying a numerator by the reciprocal of the denominator. Alternatively, the division may be performed by referring to a ROM table for storing the reciprocal of the denominator and multiplying the numerator by the reciprocal of the denominator. The division may be performed by multiplying the denominator and the numerator by a conjugate complex number of the denominator, obtaining the reciprocal of the denominator multiplied by the conjugate complex number using the ROM table and multiplying the numerator multiplied by the conjugate complex number of the denominator by the reciprocal. This may vary according to the implementation embodiments.

[347] In the case that the pilot symbol is not used in the signal transmitting apparatus, only the CTF using the symbol data having the small constellation size expressed by Math Figure 3 can be obtained.

[348] The CTF estimated by Math Figures 2 and 3 may be used for channel equalization. In

the receiving apparatus, the channel may be equalized by selecting one of the estimated values or by interpolating the two estimated values. For example, the selecting method may vary according to the implementation examples, that is, one estimated value may be selected in consideration of the channel state. The other estimated value may be selected and used if a specific estimated value is rapidly changed. Alternatively, the channel may be equalized by a value obtained by interpolating the two estimated values by linear interpolation.

[349] The first deinterleaver 3640 deinterleaves the symbol data output from the frame parser 3630 and restores the sequence of the symbol data. The deinterleaved data is output to the equalizer 3650. The equalizer 3650 compensates for transmission channel distortion of the symbol data, of which the sequence is restored, using the CTF of the channel estimated by the channel estimator 3680.

[350] For example, the equalizer 3650 may use a zero forcing equalizing method for compensating for the channel distortion. Since the symbol received by the receiver can be expressed by a product of the transmitted symbol and the CTF, the transmitted symbol data value can be restored by dividing the received symbol by the estimated CTF. That is, if the received symbol data value is $Y_r(k)$ and the estimated CTF is $H(k)$, the restored symbol data value $Y_{eq}(k)$ is expressed by Math Figure 4.

[351] [Math Figure 4]

[352]

$$Y_{eq}(k) = \frac{Y_r(k)}{H(k)}$$

[353] The detailed embodiment of the equalizer 3650 will be described with reference to FIG. 42.

[354] The symbol data equalized by the equalizer 3650 is output to the linear pre-coding decoder 3660. The linear pre-coding decoder 3660 restores the dispersed symbol data and outputs the restored symbol data. The restored symbol data is input to the multi-demapper 3670 and the channel estimator 3680.

[355] The multi-demapper 3670 demaps the received symbol data using the demappers and outputs the bit data corresponding thereto. The multi-demapper 3670 transmits the symbol data value which is decided with respect to the symbol data having the small constellation size to the channel estimator 3680. Alternatively, the bit data demapped with respect to the symbol data having the small constellation size may be output to the channel estimator 3680. Since the estimation of the channel is performed in units of symbol data, in the case that the bit data demapped with respect to the symbol data having the small constellation size is output to the channel estimator 3680, the decision unit 3700 of FIG. 41 decides the symbol data corresponding to the received bit data

again.

- [356] The second deinterleaver 3690 deinterleaves the bit data received from the multi-demapper 3670 and restores the sequence of the bit data. The multi-decoder 3692 multi-decodes the bit data, of which the sequence is restored, according to the multi-encoding method and outputs the multi-encoded data. If one encoding method is used in the signal transmitting apparatus instead of the multi-encoding method, the multi-decoder is not used and one decoding method corresponding to the encoding method is used.
- [357] FIG. 41 is a schematic block diagram showing a channel estimator according to an embodiment of the present invention. The channel estimator includes a decision unit 3700, a first operation unit 3710, a first multiplier 3720, a second multiplier 3730, a second operation unit 3740, a pilot generator 3750, a third operation unit 3760, a third multiplier 3770, a fourth multiplier 3780, and a fourth operation unit 3790. If the method which does not insert the pilot symbol is used, the pilot generator 3750, the third operation unit 3760, the third multiplier 3770, the fourth multiplier 3780 and the fourth operation unit 3790 are not used.
- [358] The channel estimator of FIG. 41 multiplies the denominator and the numerator by the conjugate complex number of the denominator so as to obtain the reciprocal of the denominator multiplied by the conjugate complex number and multiplies the numerator multiplied by the conjugate complex number of the denominator by the reciprocal so as to obtain the CTF.
- [359] First, the pilot symbol data (the symbol data having the small constellation size in the above example) input to the symbol demapper 3670 and the pilot symbol data output from the symbol demapper 3670 are input to the decision unit 3700. The decision unit 3700 outputs the symbol data output from the symbol demapper 3670 to the first operation unit 3710 and the first multiplier 3720.
- [360] The first operation unit 3710 obtains the conjugate complex number of the received input data and outputs the conjugate complex number to the first multiplier 3720 and the second multiplier 3730. The first multiplier 3720 multiplies the symbol data output from the decision unit 3700 by the conjugate complex number output from the first operation unit 3710 and outputs the multiplied value to the second operation unit 3740. The second multiplier 3730 multiplies the symbol data input to the symbol demapper 3670 in the symbol data input to the decision unit 3700 by the conjugate complex number output from the first operation unit 3710 and outputs the multiplied value to the second operation unit 3740.
- [361] The second operation unit 3740 obtains the reciprocal of the value output from the first multiplier 3720, multiplies the value output from the second multiplier 3730 by the reciprocal, and outputs the multiplied value.

- [362] In the case that the CTF is estimated using the pilot symbol, the pilot symbol extracted by the frame parser 3630 is used. The pilot generator 3750 generates the pilot symbol which is previously promised with the transmitter. The generated pilot symbol is output to the third operation unit 3760 and the third multiplier 3770.
- [363] The third operation unit 3760 obtains the conjugate complex number of the received pilot symbol and outputs the conjugate complex number to the third multiplier 3770 and the fourth multiplier 3780. The third multiplier 3770 multiplies the pilot symbol output from the pilot generator 3750 by the conjugate complex number output from the third operation unit 3760 and outputs the multiplied value to the fourth operation unit 3790. The fourth multiplier 3780 multiplies the pilot symbol extracted from the frame parser 3730 by the conjugate complex number output from the third operation unit 3760 and outputs the multiplied value to the fourth operation unit 3790.
- [364] The fourth operation unit 3790 obtains the reciprocal of the value output from the third multiplier 3770, multiplies the value output from the fourth multiplier 3780 by the reciprocal, and outputs the multiplied value.
- [365] FIG. 42 is a schematic block diagram showing an equalizer according to an embodiment of the present invention. The equalizer 3650 includes an interpolator 3800, a fifth operation unit 3810, a fifth multiplier 3820, a sixth multiplier 3830, and a sixth operation unit 3840. The equalizer of FIG. 42 is an example of implementing the zero forcing equalization method.
- [366] The division may be performed by various methods as described above and the equalizer of FIG. 42 uses the same process as the division of FIG. 41.
- [367] The interpolator 3800 interpolates the received CTF value with the value of the whole bandwidth. The CTF value interpolated by the interpolator 3800 is output to the fifth operation unit 3810 and the fifth multiplier 3820. The fifth operation unit 3810 computes the conjugate complex number of the CTF output from the interpolator 3800 and outputs the conjugate complex number.
- [368] The fifth multiplier 3820 multiplies the CTF value output from the interpolator 3800 by the conjugate complex number of the CTF output from the fifth operation unit 3810 and outputs the multiplied value to the sixth operation unit 3840. The sixth multiplier 3830 multiplies the conjugate complex number output from the fifth operation unit 3810 by the received symbol data and outputs the multiplied value to the sixth operation unit 3840.
- [369] The sixth operation unit 3840 obtains the reciprocal of the value output from the fifth multiplier 3820, multiplies the value output from the sixth multiplier 3830 by the reciprocal, and outputs the multiplied value.
- [370] Since the estimation of the channel is performed in the units of symbol data, in the case where the bit data demapped with respect to the symbol data having the small

constellation size is output to the channel estimator 3680, the decision unit 3700 of FIG. 41 decides the symbol data corresponding to the received bit data again.

[371] FIG. 43 is a schematic block diagram showing an apparatus for transmitting a signal by a data symbol channel estimation method according to an embodiment of the present invention. The signal transmitting apparatus includes an outer encoder 3900, an inner encoder 3910, a first interleaver 3920, a symbol mapper 3930, a linear pre-coder 3940, a second interleaver 3950, a frame builder 3960, a modulator 3970 and a transmitter 3980.

[372] In the case that the symbol data having the small constellation size is inserted into the overall pilot insertion position or the symbol data having the small constellation size is inserted into a portion of the pilot insertion position and the pilot is inserted into the remaining portion of the pilot insertion position as described above, the symbol data inserted into the pilot insertion position may be decided and the channel may be estimated on the basis of the decided symbol data. By the above-described method, if the pilot symbols are not used or some of the pilot symbols are used, it is possible to improve the channel estimation performance and increase the capacity of the system.

[373] However, if a decision error occurs in a low SNR environment, an error may occur in the channel estimation. The error of the data compensated for by the channel estimation value having an error is further increased and thus an error propagation phenomenon occurs.

[374] In order to prevent the error propagation phenomenon, the channel can be estimated using only a decision value having high reliability among the decision values of the received symbol data.

[375] For example, it is assumed that the symbol data having the small constellation size is inserted into the overall pilot insertion position in the signal transmitting apparatus of FIG. 43. The blocks of the signal transmitting apparatus of FIG. 43 are equal to those of the signal transmitting apparatus of FIG. 38, except that another symbol mapping method is used instead of the multi-mapping method. For example, the symbol mapping method such as a QAM method, a QPSK or an optimal constellation may be used and the trellis coded modulation method may be used as the encoded symbol mapping method. The signal transmitting apparatus of FIG. 41 is similar to the signal transmitting apparatus of FIG. 36 and thus the description thereof will be omitted.

[376] Since the frame builder 3960 of FIG. 43 does not insert the pilot and inserts the symbol data having the small constellation size to the pilot insertion position, the symbol data inserted into the pilot insertion position is extracted and is restored together with the remaining symbol data.

[377] FIG. 44 is a schematic block diagram showing an apparatus for receiving a signal by a data symbol channel estimation method according to an embodiment of the present

invention. The signal receiving apparatus includes a receiver 4000, a synchronizer 4002, a demodulator 4004, a frame parser 4008, a first deinterleaver 4010, an equalizer 4012, a linear pre-coding decoder 4014, a symbol demapper 4016, a channel state estimator 4018, a channel estimator 4020, a second deinterleaver 4022, an inner decoder 4024, and an outer decoder 4026. The signal receiving apparatus of FIG. 44 receives and processes the signal transmitted by the signal transmitting apparatus of FIG. 43.

[378] The signal receiving apparatus of FIG. 44 corresponds to the signal receiving apparatus of FIG. 41 and, for convenience of description, the common portions between FIG. 44 and FIG. 41 will be omitted.

[379] Since the pilot is not inserted and the symbol data having the small constellation size is inserted into the pilot insertion position in the received frame data, the frame parser 4008 of FIG. 42 extracts the symbol data inserted into the pilot insertion position and restores the symbol data together with the remaining symbol data.

[380] The channel state estimator 4018 estimates the symbol data position, that is, the state of the transmission channel of the subcarriers. In order to estimate the channel state, a log-likelihood ratio (LLR) value used for the decision of the symbol data or the SNR of the channel may be used. The subcarriers for estimating the channel state may be subcarriers for transmitting the symbol data inserted into the pilot insertion position or subcarriers for transmitting the other symbol data included in the frame.

[381] The channel estimator 4020 determines a channel having a good state using the states of the channels estimated by the channel state estimator 4018 and estimates the channel using the symbol data received via the channel having the good state. For example, in the channel having the good state, the SNR of the channel is high and the LLR value is large. If high reliability is applied to the channel via which the symbol data having the small constellation size or the symbol data coded at a low code rate is received in addition to the above information, a channel estimation error can be reduced.

[382] The channel estimator 4020 can obtain the channel estimation function using the symbol data decided by the trellis coded decoder 4016 and the symbol data received via the channel having the good state. The equalizer 4012 compensates for the channel distortion of the received symbol data using the channel estimation function output from the channel estimator 4020.

[383] The multi-encoding method or the multi-mapping method may be used together with the method of estimating the channel using the decided symbol data. That is, any one or both of the multi-encoding method and the multi-mapping method may be used together with the method of estimating the channel using the decided symbol data.

[384] FIG. 45 is a schematic block diagram showing another example of an apparatus for

transmitting a signal by a data symbol channel estimation method according to an embodiment of the present invention. FIG. 46 is a schematic block diagram showing another example of an apparatus for receiving a signal by a data symbol channel estimation method according to an embodiment of the present invention.

[385] The signal transmitting apparatus of FIG. 45 includes an outer encoder 4100, a multi-encoder 4110, a first interleaver 4120, a multi-mapper 4130, a linear pre-coder 4140, a second interleaver 4150, a frame builder 4160, a modulator 4170, and a transmitter 4180, and the signal receiving apparatus of FIG. 46 includes a receiver 4200, a synchronizer 4202, a demodulator 4204, a frame parser 4206, a first deinterleaver 4208, an equalizer 4210, a linear pre-coding decoder 4212, a multi-demapper 4214, a channel state estimator 4216, a channel estimator 4218, a second deinterleaver 4220, a multi-decoder 4222, and an outer decoder 4224.

[386] In the examples of FIGs. 45 and 46, both the multi-encoding method and the multi-mapping method are used together with the method of estimating the channel using the decided symbol data. The blocks are equal to those of the above-described embodiments and thus the description thereof will be omitted.

[387] In the embodiments described with reference to FIGs. 27 to 46, a multi input multi output (MIMO) method may be used. Like FIG. 1 or 9. If the MIMO method is used, the multi-input/output encoder is inserted between the interleaver and the frame builder in the transmitting apparatus and the multi-input/output decoder is inserted between the frame parser and the deinterleaver in the receiving apparatus.

[388] FIG. 47 is a view showing the structure of a transmission frame according to an embodiment of the present invention. The frame builders of the transmitting apparatuses of the above-described embodiments build and output transmission frame data having the structure shown in FIG. 47.

[389] The transmission frame of FIG. 47 includes a pilot symbol interval including pilot carrier information and a data symbol interval including data information and tracking pilot information. FIG. 47 shows an embodiment in which a pilot signal is inserted into (or mapped to) the data symbol interval of the transmission frame of FIG. 7.

[390] In the case that the frame having the structure shown in FIG. 47 is transmitted, the receiving apparatus performs channel estimation of the frame using the pilot carrier information located at the pilot symbol interval. However, in the case that a channel state is changed, it is difficult to accurately perform the channel estimation using only the pilot carrier information located at the pilot symbol interval by the receiving apparatus. Accordingly, the channel estimation of the interval including the tracking pilot can be accurately performed using the tracking pilot included in the data symbol interval in addition to the pilot carrier information located at the pilot symbol interval. The tracking pilot is inserted (or mapped) in a scattered pilot form as shown in FIG. 49.

- [391] FIG. 48 is a view showing the number of tracking pilots in a frame according to an embodiment of the present invention. In the OFDM method, symbols may be transmitted in a state of being carried in subcarriers using Fourier Transform.
- [392] FIG. 48 shows the number of available subcarriers, the number of tracking pilots and the number of pieces of symbol data according to a Fast Fourier Transform (FFT) mode in the case that the symbols are transmitted using the FFT. The number of available subcarriers denotes a value obtained by subtracting the number of subcarriers for a transmission parameter signal (TPS) from the total number of subcarriers, and the number of tracking pilots denotes the number of tracking pilots inserted into the data symbol interval. The number of pieces of symbol data denotes a value obtained by subtracting the number of tracking pilots from the number of available subcarriers, that is, the number of subcarriers which can transmit the symbol data. For example, in a 2k mode, among 1688 available subcarriers, 68 subcarriers are used for transmitting the tracking pilots and the remaining 1620 subcarriers are used for transmitting the symbol data.
- [393] FIG. 49 is a view showing a frame including tracking pilots according to an embodiment of the present invention. FIG. 49 shows a state in which the tracking pilots are inserted into one data symbol interval according to the 2k mode among transmission modes of FIG. 48.
- [394] In FIG. 48, among 1688 subcarriers excluding the subcarriers for the TPS from 1710 (0th to 1709th) subcarriers, 68 subcarriers are used for transmitting the tracking pilot information and 1620 subcarriers are used for transmitting the symbol data.
- [395] The tracking pilots have five patterns (pattern 0 to pattern 4) according to a time and are inserted in the scattered pilot form. The symbol distance between the tracking pilots of one pattern and another pattern is 5 and the symbol distance between the tracking pilots of one pattern is 25.
- [396] FIG. 50 is a view showing margins of the frame of FIG. 49 according to an embodiment of the present invention. In the case that the tracking pilots are inserted in the form shown in FIG. 49, a left margin is a symbol distance of 4 and a right margin is a symbol distance of 5. In a region in which the margin is generated, since the channel estimation cannot be performed using the tracking pilots, the margin should be reduced in order to accurately perform the channel estimation.
- [397] FIG. 50 shows the number of tracking pilots, the left margin and the right margin according to the FFT modes with respect to the frame shown in FIG. 49. For example, in the 2k mode, the left margin and the right margin are symbol distances of 4 and 5, respectively. In an 8k mode, the left margin and the right margin are symbol distances of 48 and 58, respectively. That is, it can be seen that, as the length of the symbol is increased according to the FFT mode, the margin region is increased.

- [398] FIG. 51 is a view showing another frame including tracking pilots according to an embodiment of the present invention. FIG. 51 shows another state in which the tracking pilots are inserted into one data symbol interval according to the 2k mode among transmission modes of FIG. 48.
- [399] In FIG. 51, among 1688 subcarriers excluding the subcarriers for the TPS from 1710 (0th to 1709th) subcarriers, 71 subcarriers are used for transmitting the tracking pilot information and 1617 subcarriers are used for transmitting the symbol data.
- [400] The tracking pilots have six patterns (pattern 0 to pattern 5) and are inserted in the scattered pilot form. The symbol distance between the tracking pilots of one pattern and another pattern is 4 and the symbol distance between the tracking pilots of one pattern is 24.
- [401] FIG. 52 is a view showing margins of the frame of FIG. 50 according to an embodiment of the present invention. In the case that the tracking pilots are inserted in the form shown in FIG. 50, a left margin is a symbol distance of 2 and a right margin is a symbol distance of 2.
- [402] FIG. 52 shows the number of tracking pilots, the left margin and the right margin according to the FFT modes with respect to the frame shown in FIG. 51. For example, in the modes (2k, 4k and 8k modes), the left margin and the right margin are symbol distances of 2 and 2, respectively. That is, in the frame shown in FIG. 51, the number of tracking pilots is slightly increased, but the margin region is reduced. Accordingly, the channel can be accurately estimated.
- [403] FIG. 53 is a view showing the number of symbols included in a low density parity check (LDPC) block according to an embodiment of the present invention. In the case that an LDPC encoder is used as the inner encoders of the transmitting apparatuses of the above-described embodiments, since the size of the LDPC frame is different from that of the OFDM frame, the receiving apparatus needs to perform a separate process of synchronizing the LDPC frame. Accordingly, it is possible to readily realize the synchronization of the LDPC frame, by efficiently building the OFDM frame.
- [404] FIG. 53 shows the number of symbols corresponding to one LDPC block according to a symbol mapping mode and the LDPC mode. The LDPC mode includes the cases where the length of the LDPC codeword is 64800 bits and 16200 bits and the multi-mapping method is used as the symbol mapper. FIG. 53 shows the multi-mapping method using a hybrid of 256-quadrature amplitude modulation (256QAM), 64QAM, 16QAM and 4QAM. That is, the data LDPC-encoded by the inner encoder is mapped to the symbols according to the hybrid of the 256QAM, 64QAM, 16QAM and 4QAM. The mapping method is exemplary and the value or the method described herein does not restrict the scope of the present invention.
- [405] In FIG. 53, the constellation column shows the mapping methods used in the multi-

mapping and rates of the mapping methods. For example, 256QAM shows the case where only the 256QAM method is used and Hyb256-64_r8 shows the case where two mapping methods, that is, the 256QAM method and the 64QAM method are used and the rate of the 256QAM method is 80%. The second column shows the rate of the mapping method having the larger constellation. If the rate is 1, only the mapping method having the larger constellation is used.

- [406] Referring to FIG. 53, the case that the data is mapped by only the 256QAM method and is transmitted will be described. Since 8 bits per symbol can be transmitted in the 256QAM method, if the length of the LDPC codeword is 64800, the number of symbols corresponding to one LDPC block becomes $64800/8=8100$. In addition, in the case that the length of the LDPC codeword is 16200, the number of symbols corresponding to one LDPC block becomes 2025.
- [407] The case that the rate of the 256QAM method is 80% and the rate of the 64QAM method is 20%, that is, the multi-mapping method of Hyb256-64_r8, will be described. In this case, the number of symbols corresponding to one LDPC block is 8640 if the length of the LDPC codeword is 64800 and the number of symbols corresponding to one LDPC block is 2160 if the length of the LDPC codeword is 16200. The numbers of symbols of the remaining examples are shown in FIG. 51. The types and the number of mapping methods of FIG. 53 are exemplary. The case where the rate of the 256QAM method is 80% and the rate of the 16QAM method is 20%, that is, the multi-mapping method of Hyb256-16_r8, may be used. A hybrid of two types of mapping methods may be used as shown in FIG. 53 and a hybrid of at least two types of mapping methods may be used.
- [408] FIG. 54 is a view showing the number of LDPC blocks included in an LDPC frame according to an embodiment of the present invention. FIG. 54 shows the number of LDPC blocks necessary for building one LDPC frame according to the multi-mapping mode and the transmission mode (the FFT mode) if the length of the LDPC codeword is 64800.
- [409] If the data is mapped to the symbols using only the 256QAM method as shown in FIG. 54, four LDPC blocks are included in the case of the 8k FFT mode and one LDPC block is included in the case of the 2k FFT mode. In the case that the rate of the 256QAM method is 80% and the rate of the 64QAM method is 20%, three LDPC blocks are included in the case of the 8k FFT mode and three LDPC blocks are included in the case of the 2k FFT mode.
- [410] FIG. 55 is a view showing the number of OFDM blocks included in an LDPC frame according to an embodiment of the present invention. FIG. 55 shows the number of OFDM blocks necessary for building one LDPC frame according to the symbol mapping mode and the FFT mode if the length of the LDPC codeword is 64800.

- [411] If the data is mapped to the symbols using only the 256QAM as shown in FIG. 55, five OFDM blocks are included in the case of the 8k FFT mode and five OFDM blocks are included in the case of the 2k FFT mode. In the case that the rate of the 256QAM method is 80% and the rate of the 64QAM method is 20%, four OFDM blocks are included in the case of the 8k FFT mode and 16 OFDM blocks are included in the case of the 2k FFT mode.
- [412] FIG. 56 is a view showing the number of LDPC blocks included in an LDPC frame of another mode according to an embodiment of the present invention. FIG. 57 is a view showing the number of OFDM blocks included in an LDPC frame of another mode according to an embodiment of the present invention. FIG. 58 is a view showing the number of OFDM blocks included in an LDPC frame of another mode according to an embodiment of the present invention.
- [413] FIGs. 56 to 58 show the case that the length of the LDPC codeword is 16200. The values of FIGs. 53 to 58 are obtained by calculation and, for convenience of description, the method of the calculating values will be omitted.
- [414] FIG. 59 is a view showing the structure of an LDPC frame according to an embodiment of the present invention. FIG. 59 shows a relationship among an LDPC frame, LDPC blocks and OFDM blocks.
- [415] In FIG. 59, the length of the LDPC codeword is 64800, the symbol mapping mode is 256QAM, and the FFT mode is 8k. One LDPC frame includes four LDPC blocks and corresponds to five OFDM blocks. Under the above-described condition, it can be seen that the number of LDPC blocks included in one LDPC frame is 4 in FIG. 54 and the number of OFDM blocks included in one LDPC frame is 5 in FIG. 55.
- [416] In FIG. 59, it can be seen that the start point of the LDPC block is not matched with that of the OFDM block. Accordingly, the frame parser of the receiving apparatus requires a synchronization process of detecting the start point of the LDPC block in order to build the LDPC block from the received OFDM blocks again.
- [417] That is, a point in which the start point of the OFDM block is matched with the start point of the LDPC block may become the start point of the LDPC frame. Accordingly, at the start point of the LDPC frame, the start point of the OFDM block is matched with the start point of the LDPC block. In other words, the start point of the LDPC block can be obtained by the start point of the OFDM block matched with the start point of the LDPC frame. For synchronization, a method of transmitting an OFDM block index used for building one LDPC frame may be used. Hereinafter, this method will be described.
- [418] FIG. 60 is a view showing the structure of a TPS according to an embodiment of the present invention. The TPS is transmitted one bit by one bit in each of the OFDM blocks and one TPS frame includes total 68 bits. Accordingly, one TPS frame is

transmitted via 68 OFDM blocks. FIG. 57 shows 68 bit numbers included in one TPS frame. The bit numbers are matched with OFDM block numbers for transmitting the bits.

- [419] The information shown in the right column of FIG. 59 may be transmitted using the 68 bits included in one TPS frame. For example, initialization information may be transmitted using a 0th bit, and constellation information, that is, mapping method, may be transmitted using 25th and 26th bits. 38th and 39th bits may transmit transmission mode information.
- [420] FIG. 61 is a view showing constellation information according to an embodiment of the present invention. Since a maximum of four types of constellation information may be transmitted using the 25th and 26th bits among the TPS bits of FIG. 57, the number of bits should be increased in the case that more types of constellation information are transmitted. FIG. 61 shows the constellation information identified using four bits.
- [421] That is, symbol data mapped by only the QPSK method is transmitted if the 25th to 28th bits are "0000" (the 25th bit is "0", the 26th bit is "0", the 27th bit is "0" and the 28th bit is "0"), and symbol data mapped by the multi-mapping method in which the rate of the 64QAM method is 40% and the rate of the 16QAM method is 60% is transmitted if the 25th to 28th bits are "0111".
- [422] Since 16 types of multi-mapping methods shown in FIGs. 53 to 57 are used in the example of FIG. 61, four bits (the 25th to 28th bits) are used. In the case that the types of the multi-mapping methods are increased or decreased, the number of bits used according to the number of types may be adjusted.
- [423] For synchronization for detecting the start point of the LDPC block by the receiving apparatus, LDPC mode information may be further included in the TPS in addition to the mapping information.
- [424] FIG. 62 is a view showing LDPC mode information according to an embodiment of the present invention. In FIG. 60, the bits for transmitting the LDPC mode information are not included. Accordingly, among the bit numbers 40 to 53, that is, the reserved bits, the LDPC mode information may be transmitted using a 42nd bit and a 43rd bit. FIG. 62 shows the LDPC information identified using the two bits.
- [425] That is, the used LDPC has a codeword length of 64800 if the 42nd and 43rd bits are "00" and has a codeword length of 16200 if the 40th and 41st bits are "01". Since two modes of 64800 and 16200 are described in the above example, the two bits (42nd and 43rd bits) are used. If the number of modes is increased, the number of bits may be increased according to the number of modes.
- [426] FIG. 63 is a view showing the structure of an extended TPS according to an embodiment of the present invention. FIG. 63 shows the extended TPS structure including the information of FIGs. 61 and 62. In the TPS frame of FIG. 52, as the con-

stellation information is further increased by two bits as shown in FIG. 61, the sequence of bits after the constellation information is shifted by two bits such that the position is adjusted. The receiving apparatus can receive the TPS frame shown in FIG. 62 and obtain the constellation information, the LDPC mode information and the transmission mode information.

[427] FIG. 64 is a view showing OFDM block index information according to an embodiment of the present invention. In the TPS frame of FIG. 60, bits for transmitting the OFDM block index information are not included. Accordingly, among the reserved bits, the OFDM block index information is transmitted using 44th to 48th bits. FIG. 63 shows the OFDM block index information identified using the five bits.

[428] In the examples of FIGs. 55 and 57, one LDPC frame may include a maximum of 28 OFDM blocks. Accordingly, the TPS frame including the TPS frame OFDM block indexes for distinguishing between the 28 OFDM blocks is transmitted. The OFDM block indicated by the OFDM block index may become any block from a first OFDM block to a last OFDM block of the TPS frame. For example, the index may be an index indicating a first block or an index indicating a last block among the 28 OFDM blocks. This may vary according to implementation examples if the block can be identified by the promise between the transmitting apparatus and the receiving apparatus.

[429] In FIG. 64, the OFDM block index is 1 if the 44th to 48th bits are "00000" and the OFDM block index is 32 if the 44th to 48th bits are "11111". As the bit value is increased one by one, the index value is increased one by one. Since the maximum of 28 blocks are identified in the above example, the five bits (the 44th to 48th bits) are used, but the number of bits used may be adjusted according to the maximum number of blocks.

[430] FIG. 65 is a view showing the structure of a TPS including OFDM block index information according to an embodiment of the present invention. The TPS frame includes the information described in FIGs. 61 and 62 and the information described in FIG. 63.

[431] The receiving apparatus can receive the TPS frame shown in FIG. 64 and obtain the constellation information, the LDPC mode information, the transmission mode information, and the index information of a specific OFDM block included in one LDPC frame. Accordingly, the number of OFDM blocks and the number of LDPC blocks included in one LDPC frame can be obtained using the constellation mode, the LDPC mode information and the transmission mode information obtained from the TPS frame, and the information shown in FIGs. 54 to 57. In addition, the start point of the LDPC block can be obtained using the number of OFDM blocks and the number of LDPC blocks included in one LDPC frame and the index information of the specific OFDM block included in the LDPC frame.

- [432] For example, it is assumed that the OFDM block index information indicates a third block of the OFDM blocks included in one LDPC frame. As described above, it can be seen that the number of OFDM blocks and the number of LDPC blocks included in one LDPC frame can be checked and the LDPC block and the OFDM block are started from the block which precedes the block indicated by the OFDM block index by two blocks.
- [433] As described above, the receiving apparatus can check the start point of the LDPC block using the TPS frame information having the structure shown in FIG. 65. The receiving apparatus should previously know information of FIGs. 54 to 57 and the start point of the LDPC block can be checked using the above information and the information included in the received TS frame.
- [434] Hereinafter, a method of obtaining the start point of the LDPC block without using the information shown in FIGs. 54 to 57 will be described.
- [435] FIG. 66 is a view showing LDPC block information according to an embodiment of the present invention. In FIG. 66, information on the number of LDPC blocks included in one LDPC frame may be transmitted using the bits of the reserved region, which is not used, among the bits of the TPS frame.
- [436] For example, the information on the number of LDPC blocks may be transmitted using 49th and 52nd bits. As can be seen from FIGs. 54 and 56, the maximum number of LDPC blocks which may be included in one LDPC frame according to the LDPC modes is 48. However, since the number of types of the number of blocks used is 10 (1, 2, 3, 4, 6, 8, 12, 16, 24 and 48), the information on the number of LDPC blocks is transmitted using four bits, in FIG. 63.
- [437] In FIG. 66, the number of LDPC blocks included in one LDPC frame is 1 if the 49th to 52nd bits are "0000" and is 16 if the 49th to 52nd bits are "0111". In FIG. 66, the values excluding the values corresponding to the 10 types of the number of blocks used in FIGs. 54 and 56 become the reserved region. Since the 10 types of values are distinguished in the above example, four bits (49th to 52nd bits) are used. However, the number of bits used may be adjusted according to the types of the values of the number of blocks used. The bit value corresponding to the number of blocks is exemplary and may vary according to implementation embodiments.
- [438] FIG. 67 is a view showing OFDM block information according to an embodiment of the present invention. In FIG. 67, the information on the number of OFDM blocks may be transmitted using 53rd to 57th bits. As can be seen from FIGs. 53 to 55, the maximum number of OFDM blocks which may be included in one LDPC frame according to the LDPC modes is 28. Accordingly, in FIG. 67, the information on the number of OFDM blocks is transmitted using five bits. Although the five bits are used in FIG. 66, a necessary number of bits may be used according to the types of the number of blocks

as shown in FIG. 66.

- [439] In FIG. 67, the number of OFDM blocks included in one LDPC frame is 1 if the 53rd to 57th bits are "00000" and is 32 if the 53rd to 57th bits are "11111". As the bit value is increased one by one, the number of types of the number of blocks is increased one by one.
- [440] Although the maximum of the 28 types of the number of blocks should be distinguished using the five bits (53rd to 57th bits) in the above example, the number of bits used may be adjusted according to the number of types of the number of blocks.
- [441] FIG. 68 is a view showing the structure of a TPS including suggested information according to an embodiment of the present invention. FIG. 68 shows the structure including the information of FIGs. 60, 61, 62, 65 and 66 in the structure of the TPS frame of FIG. 63. Accordingly, the receiving apparatus may receive the TPS frame having the structure shown in FIG. 68 and obtain the constellation information, the LDPC mode information, the transmission mode information, the index information of the specific OFDM block included in one LDPC frame, the number of LDPC blocks included in one LDPC frame, and the number of OFDM blocks included in the LDPC frame.
- [442] The receiving apparatus can directly check the start point of the LDPC block using the information included in the received TPS frame without using the information of FIGs. 54 and 57.
- [443] In the TPS structure of FIG. 68, 58th to 71st bits include BCH error protection information. In the DVB, the BCH error protection information can be obtained using an original systematic code having the BCH (127, 113, t=2). 127 represents the total number of transmission bits, 113 represents the number of message bits, and the number of bits obtained by subtracting the number of message bits from the total number of transmission bits represents the number of parity bits. In addition, t=2 represents the number of bits of which the error can be corrected.
- [444] In order to obtain the BCH error protection information, 60-bit zero is inserted into the input bitstream of the BCH encoder and is encoded. If the inserted 60-bit zero is removed from the encoded output bits, a shortened BCH code having the BCH (67, 53, t=2) can be obtained.
- [445] In order to obtain the BCH code with respect to 57-bit message bits and the TPS having the total transmission bit number of 71 as shown in FIG. 68, 56-bit zero is inserted into the input bitstream of the BCH encoder and is encoded. If the inserted 56-bit zero is removed from the encoded output bits, a shortened BCH code having the BCH (71, 57, t=2) can be obtained.
- [446] FIG. 69 is a view showing preamble period information according to an embodiment of the present invention. In FIG. 69, the preamble period information may be included

in the TPS frame. As described above, the pilot symbol interval may be used in the transmission frame of FIG. 7 or 47 as the preamble. In this case, the period of the preamble indicates the period of the pilot symbol interval.

- [447] The pilot symbol interval includes a known signal which may be used as the pilot. The receiving apparatus performs signal synchronization, channel estimation and channel compensation using the pilot signal. The data symbol interval including data to be transmitted is transmitted in a state of being included between the pilot symbol interval and a next pilot symbol interval. The transmitting apparatus can obtain trade-off between the data capacity and the transmission reliability by adjusting the period of the pilot symbol interval.
- [448] For example, if the channel environment is bad or the channel environment is changed like a mobile reception environment, the pilot symbol interval is more frequently inserted so as to increase the period. Alternatively, if the channel environment is good or the channel environment is not changed, the pilot symbol interval is less frequently inserted.
- [449] The period of the pilot symbol interval may vary according to implementation embodiment. Accordingly, the transmitting apparatus transmits the preamble period information shown in FIG. 69 to the receiving apparatus such that the receiving apparatus checks the period of the pilot symbol interval. The example of FIG. 69 shows the case that the preamble is inserted into every 10 symbols, 15 symbols, 20 symbols and 25 symbols using two bits including a 58th bit and a 59th bit. The number of bits or the period information is exemplary and does not restrict the scope of the present invention.
- [450] FIG. 70 is a view showing a structure of a TPS including the preamble period information according to an embodiment of the present invention. FIG. 70 shows the structure of the TPS in which the preamble period information is further included.
- [451] In order to obtain a BCH code with respect to the TPS having 59-bit message bits and 73-bit transmission bits shown in FIG. 69 using an original systematic code having the BCH (127, 113, t=2), 54-bit zero is inserted into the input bitstream of the BCH encoder and is encoded. If the inserted 54-bit zero is removed from the encoded output bits, a shortened BCH code having the BCH (73, 59, t=2) can be obtained.
- [452] FIG. 71 is a view showing a relationship between a pilot symbol interval and a single frequency network according to an embodiment of the present invention. In the transmission frame described with reference to FIG. 7 or 47, the pilot symbol interval may have the structure shown in FIG. 8.
- [453] The pilot symbol interval shown in FIG. 71 is divided into even pilots and odd pilots by interleaving the pilot carrier information. The single frequency network (SFN) is divided into an even carrier region A and an odd carrier region B, which transmit data

using information corresponding to the even pilots and the odd pilots.

[454] FIG. 72 is a view showing a structure of a pilot symbol according to an embodiment of the present invention. The upper side of FIG. 72 shows the structure of the pilot symbol interval including the even pilot carrier and the lower side thereof shows the structure of the pilot symbol interval including the odd pilot carrier. In addition, the even pilot carrier and the odd pilot carrier, null carrier information is included.

[455] That is, in the antenna of the even carrier region A, the data is transmitted using the pilot symbol interval including the even pilot carrier as shown in the upper side of FIG. 72 and, in the antenna of the odd carrier region B, the data is transmitted using the pilot symbol period including the odd pilot carrier as shown in the lower side of FIG. 72. The data of the data symbol interval transmitted in the even carrier region A is equal to that transmitted in the odd carrier region B are identical to each other and the pilot carrier information of the pilot symbol interval of the even carrier region A is different from that of the odd carrier region B.

[456] In the case that the even pilot and the odd pilot configure the pilot symbol interval, the total power is not changed by doubling the power of the pilot included in the pilot symbol interval. Accordingly, the receiving apparatus can estimate the channel using the pilot having the doubled power and more accurately estimate the channel.

[457] In a region C which the even carrier region A and the odd carrier region B overlap with each other as shown in FIG. 71, the even pilot signal and the odd pilot signal can be simultaneously received. Accordingly, the channel can be more accurately estimated using the even pilot signal and the odd pilot signal in the region C. For example, the channel may be estimated using the pilot of the better channel state or the channel may be compensated for using the both pilots and estimated. Accordingly, as shown in FIG. 71, when the antenna is provided such that the carrier region (i.e., B) partially overlaps with the carrier region (i.e., A), the channel can be accurately estimated even in a region which is relatively far apart from the antenna.

[458] In the case that the pilot symbol intervals including the even pilot and the odd pilot are used, the receiving apparatus can readily detect the pilot symbol intervals so as to perform synchronization. As shown in FIG. 71, since the null information (energy 0) is included in the pilot symbol interval but the carrier having energy of 0 is not included in the data symbol interval, the pilot symbol intervals (or the preambles) are synchronized by only the method of detecting the power of the carrier.

[459] FIG. 73 is a schematic block diagram showing another example of an apparatus for transmitting a signal according to an embodiment of the present invention. FIG. 73 shows the apparatus for transmitting the signal using the multi-encoding method, the multi-mapping method and the pilot symbol structure shown in FIG. 72, among the signal transmitting apparatuses of the above-described embodiments. That is, the pilot

symbol structure shown in FIG. 71 may be used in all the embodiments of FIGs. 1, 14, 27, 34, 38, 43 and 45. In the components of FIG. 73, a necessary component may be added or an unnecessary component may not be used according to implementation embodiments such an embodiment in which an interleaving process is performed between the outer encoder and the inner encoder or an embodiment in which the linear pre-coding process is not performed. The components of the signal transmitting apparatus of FIG. 73 are described in the above-described embodiments and thus only portions different from those of the above-described embodiments will be described.

[460] The symbol data interleaved by a second interleaver 6850 is input to a frame builder 6860. The frame builder 6860 inserts a pilot signal so as to build a frame such that the output signal can be modulated by the OFDM method. At this time, the frame builder 6860 builds the frame including the pilot symbol interval having the structure shown in FIG. 71. For example, the frame builder of the even carrier region builds the frame including the pilot symbol interval having the structure shown in the upper side of FIG. 71 and the frame builder of the odd carrier region builds the frame including the pilot symbol interval having the structure shown in the lower side of FIG. 71. The transmission frame built by the frame builder 6860 is OFDM-modulated by a modulator 6870 and is transmitted.

[461]

[462] FIG. 74 is a schematic block diagram showing another example of an apparatus for receiving a signal according to an embodiment of the present invention. FIG. 74 shows the apparatus for receiving the signal using the multi-encoding method, the multi-mapping method and the pilot symbol structure shown in FIG. 72, among the signal receiving apparatuses of the above-described embodiments. The receiving apparatus of FIG. 74 corresponds to the transmitting apparatus of FIG. 73.

[463] Similarly, the components of the signal receiving apparatus of FIG. 74 are described in the above-described embodiments and thus only portions different from those of the above-described embodiment will be described.

[464] The data demodulated by a demodulator 6920 is input to a frame parser 6930. The frame parser 6930 may parse the frame received from the demodulator 6902 and output the symbol data of the data symbol interval excluding the pilot symbol. At this time, the frame parser 6930 may perform the synchronization of the pilot symbol intervals (or the preambles) by only the method of detecting the power of the carrier.

[465] The symbol data parsed by the frame parser 6930 is output to a first deinterleaver 6950. The first deinterleaver 6950 deinterleaves the symbol data by the method corresponding to the interleaving method of the second interleaver 6850 of FIG. 73 and restores the sequence of the symbol data.

[466] The pilot data parsed by the frame parser 6930 is output to a channel estimator 6940.

The channel estimator 6940 estimates the channel using the known pilot information and the pilot output from the frame parser 6930 and outputs the estimated value to an equalizer 6960. The equalizer 6960 equalizes the symbol data, of which the sequence is restored by the first deinterleaver 6950, using the channel estimating value.

[467]

[468] FIGs. 75 and 76 are views showing suggested frame structures according to an embodiment of the present invention. The frame structures may be applied to the above-described embodiment. In FIGs. 75 and 76, one row represents a pilot symbol interval (preamble). Data symbol intervals of the number (1 to P-1) less than that of a preamble period P by one are included between the preamble and the preamble.

[469] As described above, only even or odd pilot carrier information may be transmitted in a state of being included in the pilot symbol interval of the frame shown in FIG. 7 or FIG. 47. FIG. 75 is a view showing the frame composed of a pilot symbol interval including only even pilot carrier information and a data symbol interval including symbol data to be transmitted and continual pilot (CP) information. The CP may be used for tracking a channel variation and estimating a frequency offset.

[470] In a 2k mode, 1688 subcarriers which can transmit data are included in the data symbol interval. In FIG. 75, 68 subcarriers are used for transmitting the CP and the 1620 remaining subcarriers may be used for transmitting the symbol data.

[471] As shown in FIG. 75, in the 2k mode, one symbol interval includes 1705 (0 to 1704) pieces of subcarrier information. The pilot information is included in the pilot symbol interval at positions of the even carriers ($k=0, 2, 4, \dots, 1704$) of the carriers. The symbol data and the CP information are included in the data symbol interval. In the data symbol interval, the CP information is inserted into 68 subcarriers. FIG. 75 shows an example in which 68 subcarriers are inserted into the even carrier positions. For example, the CP information is inserted into $0^{\text{th}}, 24^{\text{th}}, \dots, 1682^{\text{nd}},$ and 1704^{th} subcarriers. The positions of the CP information are exemplary. The CP information is irregularly arranged such that the SNR of the average CP is maintained in all channels. Thus, it is possible to ensure channel tracking performance regardless of the channel. In FIG. 75, the CP information may be inserted into the odd carrier positions instead of the even carrier positions or may be inserted regardless of the even or odd carrier positions.

[472]

[473] FIG. 76 is a view showing a frame composed of a pilot symbol interval including only odd pilot carrier information and a data symbol interval including symbol data to be transmitted and CP information. In FIG. 76, among 1688 subcarriers which can transmit data, 68 subcarriers are used for transmitting the CP information and 1620 remaining subcarriers are used for transmitting the symbol data.

[474] The pilot information is included in the pilot symbol interval at positions of the odd

carriers ($k=1, 3, 5, \dots, 1703$) of the carriers. The symbol data and the CP information are included in the data symbol interval. In the data symbol interval, the CP information is inserted into 68 subcarriers. FIG. 76 shows an example in which 68 subcarriers are inserted to the odd carrier positions. Similarly, the positions of the CP information are exemplary. The CP information may be inserted into the even carrier positions instead of the odd carrier positions or may be inserted regardless of the even or odd carrier positions.

[475]

[476] FIGs. 77 to 79 are views showing insertion positions of the CP information of modes according to an embodiment of the present invention. FIG. 77 shows the positions where 68 pieces of CP information are inserted in the 2k mode, FIG. 78 shows the positions where 135 pieces of CP information are inserted in a 4k mode, and FIG. 79 shows the positions where 269 pieces of CP information are inserted in an 8k mode. The positions of the 4k mode of FIG. 78 and the 8k mode of FIG. 79 are obtained by repeating the arrangement of the 2k mode of FIG. 77 two times or four times. In the 4k mode and the 8k mode, the positions obtained by repeating the arrangement of the 2k mode two times or four times as shown in FIGs. 78 and 79 may be used or other positions may be used.

[477]

Although the CP information is inserted into the even carrier positions in the examples of FIGs. 77 to 79, the CP information may be inserted into the odd carrier positions or may be inserted regardless of the even or odd carrier positions.

[478]

[479] FIGs. 80 and 81 are views showing the structures of the frames having the same CP positions according to an embodiment of the present invention. In the pilot symbol intervals (preambles) of FIG. 80 and 81, the pilot information is inserted to the even carrier positions and the odd carrier positions, respectively. In the data symbol interval, the CP information (common CP information) is inserted to the same carrier positions such that data is transmitted. For example, in FIGs. 80 and 81, the CP information is inserted into 0^{th} , 25^{th} , \dots , 1682^{nd} and 1704^{th} subcarrier positions. The positions of the CP information are exemplary. The CP information may be inserted into the even carrier positions or the odd carrier positions or may be inserted regardless of the even or odd carrier positions.

[480]

As described with reference to FIG. 71, the frames having the structures shown in FIGs. 80 and 81 may be used when the signal is transmitted while distinguishing between the even carrier region A and the odd carrier region B in a single frequency network. In the transmitted signal of the even carrier region A, the even pilot carrier information is included in the pilot symbol interval and, in the transmitted signal of the odd carrier region B, the odd pilot carrier information is included in the pilot symbol

interval. At this time, the CP information is inserted into the data symbol interval included in the transmitted signals of the regions and the CP information is inserted into the same positions.

[481] For example, the frame including the even pilot carrier information in the pilot symbol interval as shown in FIG. 80 may be transmitted via the antenna of the even carrier region A and the frame including the odd carrier information in the pilot symbol interval as shown in FIG. 80 may be transmitted via the antenna of the odd carrier region B.

[482]

[483] FIG. 82 is a view showing insertion positions of common CP information according to an embodiment of the present invention. FIG. 82 shows the positions where 68 pieces of CP information are inserted in the 2k mode. In the 4k mode and the 8k mode, the positions obtained by repeating the arrangement of the 2k mode of FIG. 82 two times or four times may be used or other positions may be used. Similarly, the common CP information may be inserted into the even carrier positions or the odd carrier positions or may be inserted regardless of the even or odd carrier positions.

[484] Although the SISO transmission/reception using the single frequency network is described in FIGs. 80 and 81, the frame structure may be applied to the MIMO transmission/reception.

[485]

[486] FIGs. 83 to 85 are views showing the structures of multi-input/output transmission frames according to an embodiment of the present invention. FIGs. 83 to 85 show the pilots of the preamble and the positions of the CP information according to the transmission paths. In the examples of FIGs. 83 to 85, the data is transmitted using two transmission paths ant 1 and ant 2. The subcarrier positions of the CP information inserted into the data symbol interval are identical with respect to the two transmission paths.

[487] As described with reference to FIG. 1, in the MIMO method, the receiving apparatus distinguishes between the transmission paths. In the examples of FIGs. 83 to 85, the transmission paths can be distinguished using the pilot insertion position of the pilot symbol interval (preamble).

[488] For example, in the transmitted signal of the first transmission path ant 1, the even pilot carrier information is included in the pilot symbol interval and, in the transmitted signal of the second transmission path ant 2, the odd pilot carrier information is included in the pilot symbol interval. The receiving apparatus can distinguish between the transmission paths using the position of the pilot inserted into the pilot symbol interval of the received frame.

[489] The CP information is inserted into the data symbol interval of the signal transmitted

via each transmission path. The CP information may be inserted into the same positions or different positions of each transmission path.

[490] FIGs. 83 to 85 show examples in which the CP information is inserted into the same positions of each transmission path. FIG. 83 shows an example in which the CP information is inserted into the even carrier positions and FIG. 84 shows an example in which the CP information is inserted into the odd carrier positions. FIG. 85 shows an example in which the CP information inserted regardless of the even or odd carrier positions.

[491] The positions of the CP information of FIGs. 83 to 85 are exemplary and other positions may be used according to implementation embodiments.

[492] In the frame structure including the pilot symbol interval and the CP information, the pilot of the pilot symbol interval and the CP information of the data symbol interval may be scrambled and used. A DC component of the transmitted signal is removed by scrambling the pilot information such that the receiving apparatus readily detect the preamble and correct the frequency offset.

[493] For example, in order to scramble the pilot information, a pseudo random binary sequence (PRBS) may be used. At this time, the same PRBS or different PRBS may be used with respect to the pilot of the pilot symbol interval and the CP information of the data symbol interval.

[494] Math Figure 5 shows an embodiment for scrambling. The pilot of the pilot symbol interval and the CP information of the data symbol interval may be scrambled using Math Figure 5. Alternatively, the CP information may be scrambled using Math Figure 5 and the pilot of the pilot symbol interval may be scrambled or may not scrambled using Math Figure. The pilot which is scrambled using Math Figure may be changed according to implementation embodiments.

[495] [Math Figure 5]

$$[496] \quad \text{Re}(c_k) = bf \times 2\left(\frac{1}{2} - w_k\right), \quad bf = \frac{4}{3}$$

$$\text{Im}(c_k) = 0$$

[497] In Math Figure 5, C_k denotes the pilot information at the position corresponding to k and W_k denotes the PRBS for scrambling. In addition, $\text{Re}(C_k)$ denotes the real value of the C_k value and $\text{Im}(C_k)$ denotes an imaginary value of the C_k value. bf denotes a power boosting factor. The value of the power boosting factor is exemplary and is adjusted such that the channel estimation performance and the SNR performance of the data are adjusted.

[498] In the case that the CP information of the above-described frame structure is

scrambled using Math Figure 5, since only the CP information is used, the decrease in power of the data due to boosting is reduced compared with the DVB-T. In addition, since more CPs are used compared with the DVB-T, it is possible to obtain better channel tracking performance.

[499]

[500] FIG. 86 is a view showing a PRBS generator according to an embodiment of the present invention. The PRBS value W_k of Math Figure 5 can be obtained using the generator.

[501] The PRBS generator includes a bit delay unit 700 and an operation unit 7710. In the embodiment of FIG. 85, the PRBS generator includes 11 1-bit delay units and an XOR gate. The number of bit delay units and the type of the gate are exemplary and the number of delay units or the type and position of the gate may be changed according to implementation examples.

[502] An initial value of 1 is input to the bit delay units of the PRBS generator of FIG. 86. The XOR gate 7710 receives the output of the ninth bit delay unit and the output of the eleventh bit delay unit and performs an XOR operation. The output of the XOR gate 7710 is input to the first bit delay unit and the output value of the eleventh bit delay unit may be used as the PRBS value W_k of Math Figure 5. In the PRBS generator of FIG. 79, after all 11 initial values are output, the value operated by the XOR gate 7710 is output.

[503] The PRBS generator may output a value 0 or 1. If the value 1 or 0 is substituted for Math Figure 5,

$$-\frac{4}{3}$$

or

$$\frac{4}{3}$$

can be obtained as the real value $Re(C_k)$ of the pilot.

[504]

[505] FIG. 87 is a schematic block diagram showing another example of an apparatus for transmitting a signal according to an embodiment of the present invention. FIG. 87 shows the apparatus for transmitting the signal using the frame structure including the above-described CP information using the multi-encoding method and the multi-mapping method, among the signal transmitting apparatuses of the above-described embodiments.

[506] The signal transmitting apparatus of FIG. 87 is equal to the signal transmitting

apparatus of FIG. 73 except that the CP information is inserted into the data symbol interval of the transmission frame. In the signal transmitting apparatus of FIG. 87, a necessary component may be added or an unnecessary component may not be used according to implementation embodiments such an embodiment in which an interleaving process is performed between the outer encoder and the inner encoder or an embodiment in which the linear pre-coding process is not performed. Thus, only portions different from those of the above-described embodiments will be described.

[507] The symbol data interleaved by a second interleaver 7850 is input to a frame builder 7860. The frame builder 7860 inserts a pilot signal so as to build a frame such that the output signal can be modulated by the OFDM method. At this time, the frame builder 7860 builds the frame including the pilot symbol interval and the data symbol interval as described in the above-described embodiments. The above-described CP information is inserted into the data symbol interval. The transmission frame built by the frame builder 7860 is OFDM-modulated by a modulator 7870 and is transmitted.

[508]

[509] FIG. 88 is a schematic block diagram showing another example of an apparatus for receiving a signal according to an embodiment of the present invention. The receiving apparatus of FIG. 88 corresponds to the transmitting apparatus of FIG. 87. In the signal receiving apparatus of FIG. 87, a necessary component may be added or an unnecessary component may not be used according to implementation embodiments.

[510] Similarly, the components of the signal receiving apparatus of FIG. 88 are equal to those of the above-described embodiments and thus only portions different from those of the above-described embodiments will be described.

[511] A first synchronizer 7910 may use an offset result of the frequency domain of the data output from a demodulator 7920 and a second synchronizer 7930, for acquiring the synchronization of the frequency domain signal. The second synchronizer 7930 parses the frame output from the demodulator 7920, extracts the CP information, and tracks the channel. That is, the second synchronizer 7930 outputs frequency offset correction information of the received signal to the first synchronizer 7910 using the CP information included in the data symbol interval of the frame. The first synchronizer 7910 can accurately perform the synchronization using the frequency offset correction information output from the second synchronizer 7930.

[512] The data demodulated by the demodulator 7920 is output to a frame parser 7940. The frame parser 7940 may parse the frame received from the demodulator 7920 and output symbol data of the data symbol interval excluding the pilot symbol. At this time, the frame parser 7940 can perform the synchronization of the pilot symbol interval (or the preamble) by only the method of detecting the power of the carrier.

[513] If the CP information or the pilot information of the pilot symbol interval is

scrambled using the PRBS in the transmitting apparatus, the second synchronizer 7930 or the frame parser 7940 may descramble the CP information or the pilot information of the pilot symbol interval.

[514]

[515] FIG. 89 is a view showing a descrambling device according to an embodiment of the present invention. The descrambling device includes a PRBS generator 8000, a selective output unit 8010 and an operation unit 8020.

[516] The PRBS generator 8000 generates and outputs a binary sequence like the PRBS generator of FIG. 86. The PRBS generator 8000 outputs 0 or 1, and the output value is input to the selective output unit 8010.

[517] The selective output unit 8010 selectively outputs one of two input values 1 and -1 using the value 0 (false) or 1 (true) as a control value. For example, in FIG. 89, if the value 0 is received from the PRBS generator 8000, the selective output unit 8010 outputs the value 1 and, if the value 1 is received from the PRBS generator 8000, the selective output unit 8010 outputs the value -1. The value output from the selective output unit 8010 is input to the operation unit 8020.

[518] The operation unit 8020 multiplies the pilot received via the channel by the value output from the selective output unit 8010 and outputs the multiplied value. If the pilot is scrambled by Math Figure 5 and is transmitted, the pilot received via the channel has a value

$$bf \times 2\left(\frac{1}{2} - w_k\right) * CTF$$

. That is, the pilot received via the channel is obtained by convolution of the channel transfer function (CTF) with the scrambled pilot

$$bf \times 2\left(\frac{1}{2} - w_k\right)$$

[519] As described in Math Figure 5, the scrambled pilot has a value $bf \times 1$ if w_k is 0 and has a value $bf \times -1$ if w_k is 1. The selective output unit 8010 of FIG. 82 outputs the value 1 if the value 0 is received and outputs the value -1 if the value 1 is received.

[520] Accordingly, the operation unit 8020 may descramble the pilot scrambled according to the PRBS of the transmitting apparatus and output the descrambled value. In FIG. 89, the descrambled value becomes

$$bf * CTF$$

- [521] The symbol data parsed by the frame parser 7940 is output to the first deinterleaver 7960. The first deinterleaver 7960 deinterleaves the symbol data by the method corresponding to the interleaving method of the second interleaver 7850 of FIG. 87 and restores the sequence of the symbol data.
- [522] The pilot data parsed by the frame parser 7940 is output to a channel estimator 7950. The channel estimator 7950 estimates the channel using the pilot output from the frame parser 7940 and known pilot information. The estimated value is output to an equalizer 7970. The equalizer 7970 equalizes the symbol data, of which the sequence is restored, using the estimated channel value.
- [523]
- [524] FIG. 90 is a view showing the comparison of the TPS transmission bit per symbol according to an embodiment of the present invention. The receiving apparatus should receive all TPS information of a period in order to decode the TPS information. In the TPS, one symbol is transmitted in a state in which one TPS bit is included therein. In this case, a symbol time is consumed for the synchronization of the TPS by the number of TPS bits.
- [525] Accordingly, if the data symbol interval is transmitted in a state in which the TPS information is further included therein, the time for the TPS synchronization can be reduced. For example, if a portion of the CP insertion positions is used for transmitting the TPS, the time for the TPS synchronization can be reduced. That is, in addition to the subcarriers for transmitting the existing TPS information, at least one piece of TPS information may be further included in the CP information insertion positions of the data symbol interval instead of the pilot information. The TPS bits may be included in one CP pilot information insertion position of the data symbol interval and the TPS bits may be repeatedly included in a plurality of CP information insertion positions of one data symbol interval.
- [526] For example, it is assumed that one TPS bit is repeatedly included in one data symbol interval 17 times. In this case, in the 2k mode, the TPS bits may be included in 17 subcarriers and the CP information may be included in the 51 remaining subcarriers, among the 68 pilot carriers. In the 4k mode and the 8k mode, the CP information may be included in 101 and 201 subcarriers, respectively.
- [527] FIG. 90 is a view showing a TPS synchronization latency consumed for transmitting 2 TPB bits and transmitting one TPS bit to one symbol on the basis of the TPS suggested in FIG. 68. In the drawing, the time is an expected latency when it is assumed that one symbol length is 1120 usec (DVB-T, 8k-mode), and is obtained by multiplying the total symbol by the symbol length.
- [528] In the case that one TPS bit is transmitted to one symbol, 72 symbols should be received for the TPS synchronization. In the 8k mode, a maximum of 19 symbols

should be received for the LDPC synchronization as shown in FIG. 57. The total symbol indicates a maximum symbol time for next synchronization when one symbol is missed. For example, if a first symbol is missed, the maximum symbol time for next synchronization is consumed. If one TPS bit is transmitted to one symbol, the maximum symbol time becomes $72(\text{TPS synchronization}) \times 2 + 19(\text{LDPC synchronization}) - 1 = 162$. If two TPS bits are transmitted to one symbol, the maximum symbol time becomes $36(\text{TPS synchronization}) \times 2 + 19(\text{LDPC synchronization}) - 1 = 90$. In this case, the data can be efficiently transmitted in view of the latency or the data.

[529]

[530] FIG. 91 is a schematic block diagram showing an apparatus for transmitting a signal using scramble according to an embodiment of the present invention. The signal transmitting apparatus includes an energy scrambler 8200, an outer encoder 8210, an inner encoder 8220, a first interleaver 8230, a multi-mapper 8240, a second interleaver 8250, a frame builder 8260, a modulator 8270, a D/A converter 8280 and a transmitter 8290.

[531] The signal transmitting signal of FIG. 91 can a peak to average power ration (PARP) of the transmitted signal using energy dispersal scramble.

[532] The energy scrambler 8200 scrambles input bit data and disperses the energy of the data. For example, the input bit data and a scramble pattern value generated which is randomly generated are XOR-operated and the result value is output. The scramble pattern value or the operation method may be changed according to implementation embodiments. The correlation of the input bitstream can be reduced by the energy scramble.

[533] The outer encoder 8210 and the inner encoder 8220 encode the respective input signals and output the encoded signals such that an error generated in transmitted data is detected and corrected by the receiving apparatus. That is, as the outer encoder 8210 and the inner encoder 8220, a BCH encoder and an LDPC encoder may be used, respectively. An interleaver may be interposed between the outer encoder 8210 and the inner encoder 8220 according to implementation embodiments. Alternatively, the above-described multi-encoding method may be used in the outer encoder 8210 and the inner encoder 8220.

[534] The first interleaver 8230 shuffles the data stream output from the outer encoder 8210 to random positions. The multi-mapper 8240 maps the data interleaved by the first interleaver 8230 to symbols according to the transmitting method. The multi-mapper 8240 maps the input data to symbol data using a hybrid of a plurality of mapping methods. As the mapping method, a QAM, a QPSK, an APSK, a PAM or an optimal constellation may be used.

[535] In the multi-mapper 8240, a method of mapping the data to the symbols according to

the respective mapping methods in the bit data units or the block units may be used. For example, the input bit data may be mapped in a state of being sequentially divided by the number of pieces of bit data necessary for the respective mapping methods or may be mapped according to the respective mapping methods in a state of being divided in the block units.

[536]

[537] FIG. 92 is a schematic block diagram showing a multi-mapper of block units according to an embodiment of the present invention. The multi-mapper includes a block distributor 8241, a first symbol mapper 8242, a second symbol mapper and a block interleaver 8244. Although two symbol mappers are used in the example of FIG. 92, this is only exemplary and at least one symbol mapper may be used.

[538]

The block distributor 8214 distributes the input bit data to several mappers in the block units. The block distributor 8241 divides the data into a necessary number of blocks for mapping the symbols according to the mapping methods of the mappers and distributes the bit data.

[539]

[540] FIG. 93 is a schematic block diagram showing a multi-mapper according to another embodiment of the present invention. The multi-mapper includes a variable symbol mapper 8247 and a symbol pattern generator 8246. The symbol pattern generator 8246 generates a symbol pattern identifier. Therefore, the variable symbol mapper 8247 maps input data to a symbol according to the symbol pattern identifier generated from the symbol pattern generator 8246. As a result, the input data can be mapped to the symbol according to a plurality of symbol mapping methods using one variable symbol mapper 8247 without the need of equipping symbol mappers according to respective symbol mapping methods. The symbol pattern generator 8246 may generate different symbol patterns according to program identification information, service identification information, and channel identification information. The variable symbol mapper 8247 may map the input data to the symbol by different symbol mapping methods according to the identification information.

[541]

[542] FIG. 94 is a view showing a block distributing method according to an embodiment of the present invention. That is, the distributing method is an example of the method of distributing the bitstreams by the block distributor 8214. In A_n of the upper side of FIG. 94, the bit data input to the block distributor 8241 is divided into five blocks SubBlocks 0 to 4. In B_n of the lower side of FIG. 94, the divided blocks are distributed to the symbol mappers.

[543]

If two symbol mapping methods are divided by five levels (100:0($r=5$), 80:20($r=4$), 60:40($r=3$), 40:60($r=2$), 20:80($r=1$)) as shown in FIG. 61, the input bitstreams are

divided into five equal blocks as shown in the upper side of FIG. 94. For example, in the case that the encoded data is distributed according to the LDPC, the length of one block is 12,960 bits if the length of the LDPC codeword is 64,800 bits and the length of one block is 3,240 bits if the length of the codeword is 16,200.

[544] The blocks divided according to the value 'r' are merged and the merged block is output. That is, 'r' blocks and '5-r' blocks are distributed to the two symbol mapping methods according to the value 'r'. The 'r' blocks and the '5-r' blocks may be sequentially merged or blocks may be extracted from the divided blocks according to the promise and may be merged. The example of the merging the blocks may be changed according to implementation embodiments.

[545] For example, in the case that the multi-mapper 8240 maps the input data to the symbols by mixing the 256QAM mapping method and the 64QAM mapping method by a ratio of 80%:20%, the value 'r' becomes 4. Accordingly, four blocks are distributed in the 256QAM mapping method and one block is distributed in the 64QAM mapping method. The lengths of the bit data mapped according to the symbol mapping methods become $4 \times \text{SubBlock}$ and $1 \times \text{SubBlock}$, respectively.

[546] The first symbol mapper 8242 and the second symbol mapper 8243 map the bit data of the block units distributed by the block distributor 8241 to the symbols according to the respective symbol mapping methods.

[547] The block interleaver 8244 interleaves the symbol data output from the first symbol mapper 8242 and the second symbol mapper 8243 and disperses the symbol data to random positions. The symbol data output from the first symbol mapper 8242 and the second symbol mapper 8243 may be sequentially aligned and output without using the interleaver.

[548]

[549] FIGs. 95 and 96 are views showing a method of interleaving symbol data according to an embodiment of the present invention.

[550] In the embodiment of FIG. 95, the symbol data is written in a matrix memory in a column direction and the written symbol data is read and output in a row direction. Accordingly, the data output from the first symbol mapper 8242 and the second symbol mapper 8243 may be randomly shuffled and output. The symbol data output from the first symbol mapper 8242 may be first written or the symbol data output from the second symbol mapper 8243 may be first written. The writing order may be changed according to implementation embodiments. In FIG. 87, a position corresponding to a first row and a first column is a most significant symbol (MSS) and a position corresponding to a last row and a last column is a least significant symbol (LSS).

[551]

[552] FIG. 96 is a view showing another method of interleaving the symbol data. Similar to

FIG. 95, the input symbol data is written in a memory in a column direction and the written symbol data is read and output in a row direction. However, when the written symbol data is read, a position where the reading of the symbol data is started in each row is changed.

[553] For example, in FIG. 96, the symbol data from a first column to a last column is read and output in a first row. In a second row, the symbol data from a second column to the last column is read and output and the symbol data of the first column is then read and output. In a third row, the symbol data from a third column to the last column is read and output and the symbol data from the first column to the second column is then read and output. That is, in an n^{th} row, the symbol data from the n^{th} column to the last column is read and output and the symbol data from the first column to an $n-1^{\text{th}}$ column is then read and output. The example of FIG. 95 is exemplary and the read start position may be changed according to implementation embodiments.

[554]

[555] FIG. 97 is a view showing the length of the column of the memory according to an embodiment of the present invention. In FIGs. 95 and 96, the size of the memory may be changed according to implementation embodiments. For example, FIG. 97 shows the case that the length of the row is 540 symbols if the LDPC codeword is 64,800 bits and the case that the length of the row is 135 symbols if the LDPC codeword is 16,200 bits. That is, in the example of FIG. 97, the length of the column of the memory is 16 if the input data is mapped to the symbols by mixing the 256QAM mapping method and the 64QAM mapping method by a ratio of 80%:20% (Hyb256-64_r8).

[556] The symbol data mapped by the multi-mapper 8240 is output to the second interleaver 8250. The second interleaver 8250 disperses the input symbol data to random positions. The interleavers described in the above-described embodiments may be used in the first interleaver 8230 and the second interleaver 8250.

[557] The frame builder 8260 inserts a pilot signal so as to build a frame such that the symbol data output from the second interleaver 8250 is modulated by the OFDM method. Similarly, the frame builder 8260 may build the frame using the frame structures described in the above-described embodiments.

[558] The modulator 8270 OFDM-modulates the built frame and outputs the modulated signal, and the D/A converter 8280 converts the modulated signal from a digital signal into an analog signal. The converted analog signal is transmitted via the transmitter 8290 as a radio frequency (RF) signal.

[559]

[560] FIG. 98 is a schematic block diagram showing an apparatus for receiving a signal using descramble according to an embodiment of the present invention. The signal receiving apparatus corresponds to the signal transmitting apparatus of FIG. 91. The

signal receiving apparatus includes a tuner 8800, an A/D converter 8810, a synchronizer 8820, a demodulator 8830, a frame parser 8840, a channel estimator/equalizer 8850, a first deinterleaver 8860, a multi-demapper 8870, a second deinterleaver 8880, an inner decoder 8890, an outer decoder 8892, and an energy descrambler 8894.

[561] The tuner 8800 tunes to and receives a signal of a selected channel. The RF signal received by the tuner 8800 is converted into a digital signal by the A/D converter 8810 and the digital signal is output. The synchronizer 8820 acquires synchronization of a frequency-domain signal using an offset result of the frequency domain of the demodulated data. The demodulator 8830 demodulates the signal of which the synchronization is acquired and outputs the demodulated signal. The frame parser 8840 parses the demodulated frame and extracts the symbol data and the pilot.

[562] The channel estimator/equalizer 8850 estimates the channel using the pilot extracted by the frame parser 8840 and equalizes the symbol data using the estimated channel. The first deinterleaver 8860 deinterleaves the symbol data equalized by the channel estimator/equalizer 8850 and restores the symbol data before interleaving. The first deinterleaver 8860 corresponds to the second interleaver 8250 of FIG. 84.

[563] Although the channel estimator and the equalizer are represented by one block in FIG. 98 and the equalized symbol data is deinterleaved, the channel estimator and the equalizer may be represented by different blocks and the symbol data extracted from the frame may be deinterleaved and equalized. That is, this may be changed according to implementation embodiments.

[564] The deinterleaved symbol data is demapped to the bit data by the multi-demapper 8870 and the demapped bit data is output. The multi-demapper 8870 demaps the symbol data by the method corresponding to the method of the multi-mapper 8240 of FIG. 91 and outputs the demapped data.

[565]

[566] FIG. 99 is a schematic block diagram showing a multi-demapper of block units according to an embodiment of the present invention. The multi-demapper includes a block deinterleaver 8871, a first symbol demapper 8872, a second symbol demapper 8873, and a block merger 8874. Although two symbol demappers are used in the example of FIG. 99, this is exemplary and the symbol demappers may be used by the number of symbol mappers of the multi-mapper 8240.

[567] The block deinterleaver 8871 deinterleaves the input symbol data to several symbol demappers. The block deinterleaver 8271 deinterleaves the symbol data according to the method corresponding to the interleaving method of the block interleaver 8244 of FIG. 92 and distributes the symbol data.

[568] The first symbol demapper 8872 and the second symbol demapper 8873 demap the

symbol data, which is deinterleaved and distributed, to the bit data according to the respective demapping methods. The first symbol demapper 8872 and the second symbol demapper 8873 correspond to the first symbol mapper 8242 and the second symbol mapper 8243 of FIG. 92, respectively.

[569] The block merger 8874 receives the bit data demapped by the first symbol demapper 8872 and the second symbol demapper 8873 and outputs one bit data stream. The block merger 8874 merges the bit data in a manner inverse to the distributing method of the block units by the block distributor 8241 of FIG. 85 and outputs the merged bit data.

[570] The second deinterleaver 8880 deinterleaves the data output from the multi-demapper 8870 and restores the data to the data in order before the interleaving. The second deinterleaver 8880 deinterleaves and restores the data sequence in the method corresponding to the interleaving method of the first interleaver 8230.

[571] The inner decoder 8890 and the outer decoder 8892 FEC-decode the data, of which the sequence is restored, such that an error generated in the received data is detected and corrected. A deinterleaver may be interposed between the inner decoder 8890 and the outer decoder 8892 according to implementation embodiments. That is, the deinterleaver may be used or may not be used depending on whether the interleaver is interposed between the outer encoder 8210 and the inner encoder 8220 in the transmitting apparatus of FIG. 91.

[572] The data decoded by the outer decoder 8892 is descrambled by the energy descrambler 8894. The energy descrambler 8894 performs the inverse process of the scrambling process of the energy scrambler 8200 of FIG. 91 and restores the data.

[573] In the transmitting/receiving apparatus of FIGs. 91 and 97, a necessary component may be further included or a specific component may be omitted according to implementation examples. For example, the interleaver may be interposed between the inner encoder and the outer encoder or a linear pre-coding decoder may be used. In addition, if the multi-input/output method is used, a multi-input/output encoder may be interposed between the second interleaver 8250 and the frame builder 8260. Alternatively, the first interleaver 8230 or the second interleaver 8250 may not be used. In addition, the mapping or demapping method of the block units and the energy scramble and descramble may be applied to the embodiments of FIGs. 1 to 90.

[574]

[575] FIG. 100 is a schematic block diagram showing a multi-demapper according to another embodiment of the present invention. The multi-demapper includes a variable symbol demapper 8877 and a symbol pattern generator 8876. The symbol pattern generator 8876 generates a symbol pattern identifier. Therefore, the variable symbol demapper 8877 demaps input symbols to bit data according to the symbol pattern

identifier generated from the symbol pattern generator 8876. As a result, the input symbols can be demapped to the bit data according to a plurality of symbol mapping methods using one variable symbol demapper 8877 without the need of equipping symbol demappers according to respective symbol mapping methods. The symbol pattern generator 8276 may generate different symbol patterns according to program identification information, service identification information, and channel identification information. The variable symbol demapper 8877 may demap the input symbols to the bit data using different symbol mapping methods according to the identification information.

[576]

[577] FIGs. 101 to 103 are views showing experimental results of the performance of a transmitting/receiving system according to a plurality of symbol mapping methods. In the experiments of FIGs. 101 to 103, the LDPC is used as the error correction encoding code and the data is encoded according to the LDPC mode having a length of 64800 bits.

[578] In the drawings, a horizontal axis denotes a required SNR for delivering information and a vertical axis denotes a capacity. Solid lines which travel toward the upper right side of the drawings represent information delivering rate according to the Shannon theory.

[579] The symbol mapping rates according to the plurality of symbol mapping methods are included in an upper left table. For example, FIG. 101 shows the results of the respective symbol mapping methods using 4QAM and 16QAM and the result of the symbol mapping method using the hybrid of 4QAM and 16QAM. HYB1 represents a rate of a method of mapping a small number of symbols (4QAM in FIG. 101) to a method of mapping a large number of symbols (16QAM in FIG. 101) and is 1/5 (that is, 4QAM:16QAM=1:4). HYB2 is 2:3, HYB3 is 3:2, and HYB4 is 4:1. cr denotes an error correction encoding code rate and uses 1/2, 2/3, 3/4 and 5/6.

[580] In FIG. 101, it can be seen that the plurality of symbol mapping methods can obtain a SNR gain of about 0.5 dB at a portion overlapping with a line representing information transmission rates of the 4QAM and the 16QAM with respect to the 4QAM and the 16QAM.

[581] In FIGs. 101 to 103, it can be seen that the plurality of symbol mapping methods are more excellent than a single symbol mapping method in a data transmission capacity and a larger amount of data can be transmitted with respect to the same SNR value.

[582] FIG. 102 shows the results of the respective symbol mapping methods using the 16QAM and the 64QAM and the result of the symbol mapping method using the hybrid of the 16QAM and the 64QAM, and FIG. 103 shows the results of the respective symbol mapping methods using the 64QAM and the 256QAM and the result

of the symbol mapping method using the hybrid of the 64QAM and the 256QAM.

[583] Even in FIGs. 102 and 103, according to the plurality of symbol mapping methods, a SNR gain can be obtained compared with a single symbol mapping method. That is, the plurality of symbol mapping methods have a data transmission rate larger than that of the single symbol mapping method with respect to the same SNR and the data can be transmitted by more robust characteristics.

[584] Accordingly, it is possible to improve flexibility of the transmitting/receiving system by adequately adjusting the plurality of symbol mapping methods.

[585]

[586] FIGs. 104 and 105 are views showing times necessary for frame synchronization according to an error correction encoding frame. Referring to FIG. 93, if the LDPC is used as the error correction encoding, an error correction encoding block can be generated according to one error correction encoding mode and at least one error correction encoding block can build an error correction encoding frame. The error correction encoding frame may be mapped with the rate of the plurality of symbol mapping methods.

[587] FIG. 104 shows the time necessary for synchronizing the LDPC frame according to signal transmission bandwidths and FFT modes in millisecond units. For example, if the FFT mode is the 8k mode and the bandwidth is 8 MHz, a maximum of a time of about 5.60 ms is consumed. The time does not exceed 8 ms.

[588] FIG. 105 shows a maximum time necessary for obtaining information necessary for synchronizing the error correction encoding frame from the TPS in order to obtain the error correction encoding frame and synchronizing the error correction encoding frame using the information.

[589]

[590] FIGs. 106 and 107 are equal to FIGs. 104 and 105 and show the time necessary for synchronizing the error correction encoding frame and the time necessary for synchronizing the error correction encoding frame after obtaining the TPS information in the case that the plurality of symbol mapping methods are used. In FIG. 106, in any combination of experiments, the synchronization can be obtained earlier than the maximum time by 24 ms.

[591]

[592] FIG. 108 shows power enhancement of the DVB-T in the case that the pilot is transmitted by the above-described preamble structure (denoted by "proposed").

[593] In the pilot is transmitted by the above-described preamble structure, the power is higher than that of the DVB-T by 0.512 dB. The density indicates the rate of the pilot. While the DVB-T includes power density of 1/3, the power density of 1/2 is included in the pilot is transmitted by the above-described preamble structure. Accordingly, if

the rate of the pilot is considered and the pilot is transmitted to the odd or even carriers of the preamble, the power enhancement of 2.272 can be obtained.

[594]

[595] FIG. 109 shows power enhancement according to the consecutive pilot structure of the DVB-T system, that is, the number of consecutive pilots included in the FFT modes and the power enhancements of the FFT modes in the case that a power boosting factor of 16/9 is used. For example, if the FFT mode is the 2k mode, while 45 consecutive pilots are included in one OFDM symbol in the DVB-T system, 68 consecutive pilots are included in one OFDM symbol in the embodiment of the present invention. According to the above-described consecutive pilot structure, in the case that the FFT mode is the 2k mode, the power enhancement of 1.793 dB can be obtained.

[596]

[597] FIG. 110 shows power enhancement of a data symbol carrier in the above-described frame structure. While the pilot symbol carrier occupies 10.3% of the OFDM symbols in the DVB-T system, the pilot symbol carrier occupies about 4% of the OFDM symbols in the above-described frame structure. Since the power of the data symbol data is decreased by the power boosting factor but the power of the pilot symbol carrier is increased, the power of the data symbol data is associated with the number of pilot symbol carriers. The above-described frame structure has power enhancement of about 0.27 dB compared with the DVB-T system.

[598]

[599] FIG. 111 shows the decrease rate of a data transfer rate according to the above-described frame structure. While the consecutive pilots and the dispersed pilots are included in the DVB-T system, only the consecutive pilots are included in the above-described frame structure. Here, a preamble period is 20, that is, one preamble is included in 19 data symbols. For example, in the case that the FFT mode is the 8k mode, the above-described frame structure has the data transfer rate enhancement of about 1.549% compared with the DVB-T system. FIGs. 112 and 113 are views showing mobility characteristics according to the above-described frame structure.

[600]

[601] FIGs. 112 and 113 show the mobility characteristics according to the above-described frame structure. FIG. 112 shows the mobility characteristics of the 2k FFT mode and FIG. 113 shows the mobility characteristics of the 8k FFT mode.

[602]

The Doppler effect due to the mobility is improved as the preamble period is decreased. For example, if the preamble period is 10, 216.45 Hz (2k mode) and 54.11 Hz (8k mode) are obtained in a guard interval (GI) mode of 1/32. If the preamble period is 20, 89 Hz (2k mode) and 22 Hz (8k mode) are obtained in a GI mode of 1/4.

[603]

[604] FIG. 114 is a flowchart illustrating a method of transmitting a signal according to an embodiment of the present invention.

[605] The signal transmitting apparatus energy-scrambles data to be transmitted so as to reduce correlation between data (S9000). The scrambled data is FEC-encoded data such that an error of a transmitting process is found and corrected (S9002). The FEC-encoded data is mapped to symbol data (S9004). For example, for FEC-encoding, an LDPC encoding method, a turbo encoding method or a multi-encoding method may be used. As the mapping method, the QAM, the QPSK method, the optimal constellation mapping method or the multi-mapping method may be used. The symbol mapping process may be performed in bit data units or block units.

[606] The mapped symbol data is converted into a transmission frame according to a transmitting method. The transmitting apparatus modulates the transmission frame and transmits the modulated transmission frame (S9006). For example, in the case that the data is transmitted using an OFDM method, the transmitting apparatus builds and transmits an OFDM transmission frame. The OFDM transmission frame may include above-described pilot symbol interval and data symbol interval.

[607] In the case that the signal transmitting apparatus transmits the data using the pilot symbol interval including only the even pilot carrier information and the pilot symbol interval including only the odd pilot carrier information, the data can be transmitted in a state of distinguishing between the even carrier region and the odd carrier region as shown in FIG. 70.

[608]

[609] FIG. 115 is a flowchart illustrating a method of receiving a signal according to an embodiment of the present invention.

[610] The signal receiving apparatus receives, synchronizes and demodulates the signal to frame data. The demodulated frame data is parsed such that the pilot and the symbol data included in the frame are extracted (S9010).

[611] In the receiving apparatus, the transmission channel is estimated using pilot information extracted from a pilot symbol interval and the extracted symbol data is equalized using the estimated channel.

[612] The equalized symbol data is demapped so as to be restored to bit data corresponding thereto (S9012). The signal receiving apparatus demaps symbol data according to the method corresponding to the mapping method of the signal transmitting apparatus. For example, in the case that the data is mapped in the block units in the signal transmitting apparatus, the data is demapped in the block units in the signal receiving apparatus.

[613] The signal receiving apparatus FEC-decodes the demapped bit data such that the error is corrected (S9014). The error correction decoding method may correspond to

the error correction encoding method of the transmitting apparatus. The FEC-decoded data is energy-descrambled in a manner inverse to the scrambling method of the transmitting apparatus and the descrambled data is output (S9016).

[614] The apparatus for transmitting/receiving the signal and the method of transmitting/receiving the signal are not limited to the above-described embodiments and are applicable to all the signal transmitting/receiving system such as broadcast or communication.

[615] Hereinafter, there is described an embodiment for transmitting/receiving signals by inserting, instead of a continual pilot, a scattered pilot, location of which within a symbol is regularly varied according to time, into a frame to improve the performance of channel estimation. If pilots having a constant pattern are inserted in symbols, a receiving side interpolates a pilot pattern of a narrower interval and searches channel characteristics or identifies services using the interpolated pilot pattern. A detailed description will be given with reference to the attached drawings.

[616]

[617] FIG. 116 is a view showing a plot signal structure according to an embodiment of the present invention. One pilot signal is transmitted with respect to 16 subcarriers per symbol and the pilot signal includes 16 patterns. Namely, such a pilot signal structure is repeated for symbols. The 16 patterns are just one example and other patterns are possible.

[618] In FIG. 116, a row number indicates an index of an orthogonal frequency division multiplexing (OFDM) symbol and a column number indicates an index of a subcarrier. Each dot designates a location where a pilot signal is inserted in each symbol. For example, a dot in the 0th row and 0th column indicates that a pilot signal is inserted into a location of the 0th symbol and the 0th subcarrier.

[619] A transmission distance of a signal may be related to delay spread. An estimation delay spread value necessary for a receiver to estimate a received signal is proportional to the transmission distance. The estimation delay spread value should be increased in order to increase the distance between transmitters.

[620] Generally, a maximum delay spread value which can be estimated from a pilot signal inserted per n subcarriers is

$$\frac{T_{symbol}}{n}$$

, where ' T_{symbol} ' indicates a symbol length and ' n ' indicates a decimation factor representing a distance of an inserted pilot signal. The value of n is inversely proportional to a sampling rate in a frequency domain. The estimation delay spread value in an SFN

is proportional to a distance between transmitters. To increase the distance between transmitters to minimize costs for constructing the SFN, the delay spread value which can be estimated by a receiver should also be increased.

[621] To increase the estimation delay spread value in the above equation, n is set to a small value. This means that a sampling rate of a pilot signal in a frequency domain is increased and more pilot signals should be transmitted, thereby lowering a data transmission rate.

[622] For example, it is assumed that there exist four symbols each having one pilot transmitted per 12 subcarriers, and four pilot signal patterns in which pilot signals are respectively inserted into the 0th subcarrier, 3rd subcarrier, 6th subcarrier and 9th subcarrier

[623] To perform channel estimation, a receiving side carries out interpolation using the pilot signals inserted in the four successive symbols. Therefore, it is judged that a pilot signal per three subcarriers is inserted. In this case, a maximum estimation delay spread value which can be obtained by channel estimation is

$$\frac{T_{symbol}}{3}$$

[624] In the above embodiment, each symbol transmits one pilot signal per 16 subcarriers and the pilot signal has 16 pattern types.

[625] Since each symbol repeats the above-described structure, if a pilot signal is inserted into the 0th subcarrier in the 0th symbol, the next pilot signal is inserted into a location separated from the 0th subcarrier by 16 subcarriers. That is, the next pilot signal of the 0th symbol is inserted into a location immediately to the right of the 15th subcarrier.

[626] Therefore, when inserting a pilot signal into the 0th subcarrier for the 0th symbol, a pilot signal of the 1st symbol may be inserted into the 8th subcarrier, (separated by 8 units), farthest apart from both pilot signals of the 0th symbol.

[627] A pilot signal of the 2nd symbol may be inserted into the 4th subcarrier farthest apart from the pilot signals of the 0th symbol and the 1st symbol. A pilot signal of 3rd symbol may be inserted into the 12th subcarrier farthest apart from both pilot signals of the 2nd symbol.

[628] A pilot signal of the 4th symbol may be inserted into the 2nd subcarrier farthest apart from the pilot signals of the 0th symbol and the 2nd symbol. A pilot signal of 5th symbol may be inserted into the 10th subcarrier which is farthest apart from both pilot signals of the 4th symbol (or farthest apart from the pilot signals of the 1st symbol and 3rd symbol).

- [629] Through the above-described method, one pilot signal is transmitted per 16 subcarriers in each symbol and the pilot signal has 16 pattern types.
- [630] Therefore, if a receiving side performs interpolation upon 16 OFDM symbols, an effect as if pilot signals are transmitted to all subcarriers is obtained and a decimation factor (n) is 1.
- [631] A maximum delay spread value which can be obtained through channel estimation is $T_{\text{symbol}}/1 = T_{\text{symbol}}$, and therefore channel estimation for the maximum delay spread value which can be obtained through OFDM symbols is possible.
- [632] The above-described embodiment shows one example and an index pattern may be modified into various forms to change locations of the pilot signals.
- [633] For instance, a $(2n)^{\text{th}}$ row and a $(2n+1)^{\text{th}}$ row may be interchanged. Namely, if n is 0 and pilot signals of the 0th row and 1st row are interchanged, the pilot signal in the 0th symbol may be inserted into the 8th subcarrier and the pilot signal in the 1st symbol may be inserted into the 0th subcarrier. Moreover, the locations of the pilot signals in the other 2nd to 15th symbols may be maintained.
- [634] If the locations of the pilot signals of the 2nd row and the 3rd row are changed and the locations of the pilot signals in the other symbols are maintained, the pilot signal in the 2nd symbol may be inserted into the 12th subcarrier, the pilot signal in the 3rd symbol may be inserted into the 4th subcarrier, and the other pilot symbols may be maintained.
- [635] Alternatively, all the $(2n)^{\text{th}}$ rows and $(2n+1)^{\text{th}}$ rows may be interchanged. Further, the $(2n)^{\text{th}}$ rows and $(2n+1)^{\text{th}}$ rows except for the 12th and 13th rows may be interchanged. This may be different according to combinations.
- [636] A group of the $(4n)^{\text{th}}$ row and $(4n+1)^{\text{th}}$ row and a group of $(4n+2)^{\text{th}}$ row and $(4n+3)^{\text{th}}$ row may be interchanged. A group of $(8n)^{\text{th}}$, $(8n+1)^{\text{th}}$, $(8n+2)^{\text{th}}$, and $(8n+3)^{\text{th}}$ rows and a group of $(8n+4)^{\text{th}}$, $(8n+5)^{\text{th}}$, $(8n+6)^{\text{th}}$, and $(8n+7)^{\text{th}}$ rows may be interchanged. A group of 0th to 7th rows and a group of 8th to 16th rows may be interchanged. Order may be modified for one group, all the groups, or the other groups except for one group, according to combinations.
- [637] An example of modification may be generalized as interchanging a row group of

$$(K_n, \dots, K_n + (\frac{K}{2} - 1))$$

and a row group of

$$(K_n + \frac{K}{2}, \dots, K_n + K - 1)$$

(where K is an integer satisfying $21 < K = 2m < N$).

- [638] The locations of the pilot signals may be changed by reversing the order of all rows

in the pilot signal structure (that is, from 0, 1, 2,..., 14, 15 to 15, 14,..., 2, 1, 0). For each case where the order of groups is changed as described above, the locations of the pilot signals when the order of all rows is reversed may be applied.

[639] In the above embodiment, one pilot signal is transmitted per 16 subcarriers in each symbol and indexes of the pilot signals are shown when the pilot signal has 16 pattern types.

[640] When this embodiment is generalized, an index value of the pilot signal is as follows.

[641]
$$\text{pilot_index}(i_{\text{symbol}}) = P \times k + F_{\text{bit-reverse}}(i_{\text{symbol}} \bmod P)$$

[642] In the above equation, 'i_{symbol}' indicates a symbol index, 'modulo-P' converts an output value to one of 0 to (P-1), and 'k' is an integer within the range of 0 to (

$$\frac{N}{P} - 1$$

). 'F_{bit-reverse}()' is a function for converting an input integer value into a binary value, performing bit reversal with respect to order from MSB to the LSB, and converting the binary value into the integer value. 'P' indicates a decimation factor applied to one symbol and 'N' indicates the length of an OFDM symbol.

[643] In this embodiment, a symbol index is 16 and a decimation factor P applied to one symbol is 16. In case of a pilot index of the 0th symbol, 'k' is 0. Since one pilot signal in the symbol per 16 subcarriers is inserted, 'P' is 16. Since a pilot signal of the 0th symbol is inserted into the 0th subcarrier, the function F_{bit-reverse}() is 0.

[644] When transmitting signals using the above pilot signal structure, a data transmission rate may be improved. A data transmission rate improved compared with a conventional structure is as follows.

[645] [Math Figure 6]

[646]
$$\frac{P - 12}{P \times 11} \times 100 (\%)$$

[647] In Math Figure 6, 'P' indicates a decimation factor. When 'P' is 32, the data transmission rate is improved by about 5.7% compared with the conventional structure.

[648] When transmitting signals in the above-described pilot index structure, a receiving side may adjust an area performing interpolation according to characteristics of a transmission channel. Through the adjustment of the interpolation area, a tradeoff relationship between a length for estimation delay spread and a coherence time of the transmission channel for accurate estimation can be obtained.

[649] FIG. 117 is a view showing an example of estimating a channel using two symbols

according to an embodiment of the present invention. FIG. 118 is a view showing an example of estimating a channel using 4 symbols according to an embodiment of the present invention. FIG. 119 is a view showing an example of estimating a channel using 8 symbols according to an embodiment of the present invention. The examples shown in FIGs. 117 to 119 are applied to the case when signals having the pilot signal structure shown in FIG. 116 are transmitted.

[650] As illustrated in FIG. 117, if channel estimation is performed using interpolation for two successive symbol areas, a decimation factor is 8 and an estimation delay spread value is reduced to

$$\frac{T_{symbol}}{8}$$

, thereby decreasing a signal transmission distance. However, channel estimation can be performed per two symbols, the channel estimation is improved and time resolution for the channel estimation is improved. Accordingly, a coherence time of a transmission channel is reduced and estimation performance for a channel which time-varies rapidly can be improved. For example, when the channel time-varies rapidly as in mobile receiving environments, the estimation performance can be improved.

[651] Referring to FIG. 118, a channel is estimated by performing interpolation for 4 successive symbol areas. In this case, a decimation factor is 4. An estimation delay spread value is

$$\frac{T_{symbol}}{4}$$

. The estimation delay spread value and a coherence time of a transmission channel demanded for accurate channel estimation are twice as large as when the interpolation is performed for two symbol areas. Therefore, a transmission distance is increased compared with FIG. 117 but estimation performance for a time-varying channel may be lowered.

[652] In a similar way, an interpolation area may be enlarged to 8 symbols as illustrated in FIG. 119 and may be further enlarged to all symbols (0th to 15th symbols). Therefore, optimal channel estimation can be performed according to characteristics of a transmission channel using the above pilot signal structure.

[653] The interpolation area may be selected in consideration of channel environments, a signal transmission distance, etc. The interpolation area may be fixed or varied according to user's selection or may be automatically selected by a receiving side according to characteristics of a transmission channel.

[654] FIG. 120 is a schematic block diagram showing an apparatus for transmitting a signal according to an embodiment of the present invention. FIG. 121 schematically illustrates a part of the apparatus of FIG. 87.

[655] A description of a modulator 7870 and a transmitter 7890 is as in FIG. 87.

[656] A frame builder 7860 forms a frame by inserting the above-described spread pilot signal so that the mapped symbol data can be modulated by an OFDM method. An index of the pilot signal is generated by a pilot index generator 7890. The frame builder 7860 forms a frame using the generated pilot signal index.

[657] The modulator 7870 inserts a guard interval into data output from the frame builder 7860 and modulates the inserted data such that the data is transmitted in a state of being carried in OFDM subcarriers. The transmitter 7880 converts digital signals having the guard interval and a data interval, which are output from the modulator 7870, into analog signals and transmits the converted analog signals.

[658] FIG. 120 is a schematic block diagram showing a pilot index generator according to an embodiment of the present invention.

[659] The pilot index generator 7890 includes an N/P-modulo counter 7891, a P-modulo counter 7893, a first operator 7895, a bit reverser 7897, and a second operator 7899. The N/P-modulo counter 7891 sequentially counts values from 0 to

$$\frac{N}{P}$$

and generates a count value. The first operator 7895 generates a result obtained by multiplying P by a value received from the N/P-modulo counter 7891. The P-modulo counter 523 sequentially generates values from 0 to P whenever the N/P-modulo counter 7891 ends count during one period P. 'P' indicates a decimation factor applied to one symbol and 'N' indicates the length of an OFDM symbol. In the embodiment of FIG. 116, P is 16.

[660] The bit reverser 7897 converting a value input from the P-modulo counter 7893 into a binary value, performing bit reversal with respect to order from MSB to the LSB, and converts the result value into an integer value.

[661] However, if order of a row group is changed or if order of a row is reversed, an additional mapping function according to each modification form may be used in addition to a function using the reverse bit order.

[662] The second operator 7899 generates a pilot index value by adding an output value of the first operator 7895 to an output value of the bit reverser 7897.

[663] FIG. 122 is a schematic block diagram showing an apparatus for receiving a signal according to an embodiment of the present invention. FIG. 122 schematically illustrates the embodiment of the apparatus of FIG. 98.

- [664] A description of the synchronizer 8820, demodulator 8830, frame parser 8840, and channel estimator/equalizer 8850 is as in FIG. 98.
- [665] The frame parser 8840 may output symbol data of a data symbol interval except for a pilot signal according to a frame structure of a signal demodulated by the demodulator 8830. To eliminate the pilot signal, the receiving apparatus should identify a pilot signal index value of received frame data. Therefore, the pilot signal index value uses a value generated by a pilot index generator 8895.
- [666] The pilot index generator 8895 has the same structure as the above-described pilot index generator 7890. That is, an index value of a pilot signal inserted by the transmitting apparatus should be the same as an index value for eliminating the pilot signal by the receiving apparatus.
- [667] The channel estimator/equalizer 8850 estimates a transmission channel using the received pilot signal and equalizes channel distortion of symbol data using the estimated channel. When estimating the channel, an interpolation area may be set as described in FIGs. 117 to 119 or may be set with respect to all symbols as described in FIG. 116.
- [668] The channel estimator/equalizer 8850 includes a channel estimator, a channel divider, an interpolator, and an equalizer.
- [669] The channel estimator estimates a transmission channel using a pilot signal parsed by the frame parser 8840. Information about the estimated channel is input to the channel divider.
- [670] The channel divider recognizes characteristics of a current transmission channel using the information about the estimated channel and selects a symbol area for interpolation. The channel divider may divide the transmission channel using information obtained through experiment, etc. For example, when the transmission channel is classified as having characteristics of rapidly time-varying channel, the interpolation area is narrowly set. When the transmission channel is classified as having characteristics of a high delay spread value, the interpolation area is widely set.
- [671] The interpolator performs interpolation for the channel using symbol area information for interpolation determined by the channel divider. The interpolator performs the interpolation in a time domain and a frequency domain to generate channel information about each subcarrier. The equalizer equalizes channel distortion of received data using the channel information about each subcarrier generated by the interpolator.
- [672] Hereinafter, another symbol mapping method which can improve a data transmission rate will be described. The above-described signal transmitting/receiving apparatus can transmit/receive a signal according to the symbol mapping method which will be described below. That is, a symbol mapper of the signal transmitting apparatus may

transmit a signal using the symbol mapping method, and the signal receiving apparatus may demap a symbol from a transmitted signal according to the symbol mapping method.

[673] FIG. 123 is a view showing an example of a detailed symbol mapping method. FIG. 123 illustrates a symbol mapping method according to a symbol rotation and remapping method.

[674] First, symbols, which are mapped using a specific symbol mapping method, are arranged on a constellation. A constellation on the left of FIG. 123 shows an example of mapping symbols using a 16QAM method. In this example, when projecting symbols mapped on a real axis and an imaginary axis of the constellation, values projected as 4 real values and 4 imaginary values can be obtained. That is, 4 real component values and 4 imaginary component values having independent sizes on the real axis and the imaginary axis can be obtained.

[675] The mapped symbols are rotated on the constellation. A constellation on the right of FIG. 123 shows an example of rotating 16QAM mapped on the left constellation centered around an origin. Symbols arranged on the rotated constellation are projected on the real axis and the imaginary axis. The amount of symbol rotation may be adjusted so that the projected values on the respective axes do not overlap. In this case, symbol projection values having 16 different projection values on each of the real axis and the imaginary axis can be obtained.

[676] The values obtained by projecting symbols on the respective axes have different sizes on the respective axes of the constellation with respect to the rotated symbols. Any one of the real axis and the imaginary axis has 16 symbol projection values. These symbol projection values may be used as a modulation mode with two 16PAM(pulse amplitude modulation)s. The symbol projection values on the real axis and the imaginary axis may be values identifying the rotated symbols. Therefore, if any one of the component values (projection values) on the real axis and the imaginary axis is known, the rotated symbols can be identified.

[677] FIG. 124 is a view showing remapped symbols after symbols are rotated on a constellation. For example, when a symbol of a lowest part on the right is rotated, the rotated symbol has a real component value (denoted by dotted lines) projected on the real axis and an imaginary component value (denoted by dotted lines) projected on the imaginary axis. If a value projected on the real axis after symbol rotation is called a real component value and a value projected on the imaginary axis after symbol rotation is called an imaginary component value, 16 real component values and 16 imaginary component values can be obtained. The 16 projected real component values and the 16 projected imaginary component values may be remapped to symbols. The lower part of FIG. 124 illustrates symbol positions where remapped symbols on a new constellation

may be positioned.

- [678] A symbol mapping method for transmitting/receiving a signal may be separately performed with respect to a real component value and an imaginary component value. The real component value and the imaginary component value may be remapped to symbols. Moreover, the real component value and the imaginary component value are values obtained by interleaving original data due to symbol rotation. Therefore, the remapped symbols can compensate for data loss at a specific frequency under frequency selective fading environments and a frequency diversity gain can be obtained.
- [679] FIG. 125 is a view showing an embodiment of a symbol mapper for mapping symbols according to a symbol mapping method.
- [680] A first symbol mapping unit 9101 maps input bit data to a symbol. Any method may be used for symbol mapping. For example, the first symbol mapping unit 9101 may map input data to a symbol using a specific QAM method.
- [681] The symbol generated from the first symbol mapping unit 9101 may be output to a first path.
- [682] A symbol rotator 9103 rotates the symbol mapped by the first symbol mapping unit 9101 on a constellation. A real component value (i component) and an imaginary component value (q component) are separately output from the rotated symbol.
- [683] For example, the real component value may be directly input to a remapper 9105 and the imaginary component value may be input to a delay 9104 and thereafter to the remapper 9105. Conversely, the real component value may be input to the delay 9104 and thereafter to the remapper 9105 and the imaginary component value may be directly input to the remapper 9105. Alternatively, any one of the real component value and the imaginary component value may be directly input to the remapper 9105 or the real component value and the imaginary component value may be sequentially input to the remapper 9105 without passing through the delay 9104.
- [684] The remapper 9105 may output remapped symbols on a new constellation using at least one of the real component value and the imaginary component value.
- [685] A symbol stream mapped by the first symbol mapping unit 9101 and a symbol stream mapped by the remapper 9105 may be multiplexed. Since the real component value and the imaginary component value have information about the symbol mapped by the first symbol mapping unit 9101 by symbol rotation, even if symbols of either one side are lost during transmission, the rotated symbols can be restored.
- [686] In the embodiment of FIG. 125, symbol streams according to a general symbol mapping method such as QAM and to symbol rotation and remapping (symbol rearrangement) can be output. Two symbol streams may be multiplexed through time interleaving and then output. Namely, a hybrid symbol mapping method which maps

symbols according to two or more symbol mapping methods may be used. Since the hybrid symbol mapping method has been described above, a detailed description thereof is omitted.

[687] FIG. 126 is a view showing an embodiment of a symbol demapper for receiving and demapping a signal according to the symbol mapping method shown in FIG. 125.

[688] A first symbol demapping unit 9111 demaps an input symbol according to a method corresponding to a symbol mapping method. For example, if a symbol is input according to a generally used QAM symbol mapping method, the first symbol demapping unit 9111 may demap the input symbol and output bit data. In this embodiment, a first symbol is demapped to bit data and output to a first path. The input symbol may be a channel-equalized symbol for easy decision.

[689] A second symbol demapping unit 9113 separately outputs a real component and an imaginary component of the input symbol. If the input symbol is a symbol mapped by rotation and remapping, the second symbol demapping unit 9113 decides a real component and an imaginary component of the rotated symbol. That is, if the position of the remapped symbol on a constellation is decided, a real component value and an imaginary component value according to the position of the symbol can be decided.

[690] For example, the real component value is output to a delay 9114 and the imaginary component value is output to a symbol rerotator 9115. Alternatively, the real component value is output to the symbol rerotator 9115 and the imaginary component value is output to the delay 9114. The real component value and imaginary component value of the symbol may be a real component value and an imaginary component value obtained by rotating a symbol and remapping values projected as the real component value and imaginary component value of the rotated symbol to independent symbols. Namely, the real component value and imaginary component value of a symbol may be the real component value and the imaginary component value of a symbol according to a symbol mapping method corresponding to symbol rotation and remapping. Therefore, a symbol according to an original symbol mapping method can be restored from at least one of the real component value and imaginary component value of a symbol.

[691] The delay 9114 may delay the input symbol. The symbol rerotator 9115 derotates the symbol decided as the real component value and the imaginary component value output by the delay 9114 and the second symbol demapping unit 9113 by as much as a degree corresponding to the amount of symbol rotation. The symbol rerotator 9115 decides the derotated symbol and restores bit data.

[692] The amount of symbol rotation (or the amount of symbol derotation corresponding thereto) by the symbol rerotator 9115 and the amount of delay by the delay 9114 are set to be different so that an effect of a diversity gain for a real component value and an

imaginary component value can be obtained.

[693] A signal processing process such as error correction decoding is performed by the bit data transmitted as at least one symbol stream among symbols demapped by the first symbol demapping unit 9111 and the symbol rerotator 9115.

[694] As described above, the symbol mapping method according to a symbol rotation and remapping method may use a hybrid symbol mapping method together with other symbol mapping methods (for example, QAM). Alternatively, a hybrid symbol mapping method may be used utilizing two or more symbol rotation and remapping methods employing the different degrees of symbol rotation. For example, a hybrid symbol mapping method may be performed using symbol mapping methods which arrange symbols on constellations of the same size or on constellations of different sizes. For example, the symbol mapping method performed by the symbol rotator may include two or more symbol mapping methods performed on constellations having different sizes. That is, the symbol mapping method performed by the symbol rotator may be a symbol mapping method which maps symbols on constellations having different sizes according to an input data interval. Alternatively, the symbol mapping method may be a hybrid symbol mapping method according to the first symbol mapping method and to the symbol rotation and remapping method on constellations of the same size as illustrated in FIGs. 125 and 126. Similarly, the symbols decided by the second symbol demapping unit include symbols mapped on constellations having different sizes according to the symbol interval.

[695] The hybrid symbol mapping method and the symbol demapping method corresponding thereto have already been described in the above embodiments.

[696] The above-described symbol mapping/demapping method is applied to the symbol mappers shown in FIGs. 1, 14, 27, 34, 38, 43, 45, 73, 74, and 87 and to the symbol demappers shown in FIGs. 10, 15, 30, 36, 39, 40, 44, 46, and 88. A signal transmitting/receiving process before and after symbol mapping may conform to the above-described embodiments.

[697] FIG. 127 is a view showing an example of deciding rotated symbols by a first symbol demapping unit. An input symbol corresponds to a symbol according to a real component value or an imaginary component value of a rotated symbol. The first symbol demapping unit may decide the input symbol using either the real component value or the imaginary component value. The first symbol demapping unit may decide a symbol on a remapped constellation. Once the symbol on the remapped constellation is decided, a real component value and an imaginary component value corresponding to the symbol can be determined and a symbol rotated from an original constellation can be decided by the real component value and imaginary component value for the decided symbol. Therefore, the first symbol demapping unit can decide the rotated

symbol and output a real component value and an imaginary component value of the decided symbol.

[698] FIG. 128 is a view showing still another example of a symbol mapping method. The symbol mapping method of FIG. 128 maps data to a symbol to achieve a Gaussian distribution on a constellation of the symbol. Such a symbol mapping method may be called a non-uniform symbol mapping method. FIG. 128 sequentially illustrates non-uniform 16QAM, non-uniform 64QAM, and non-uniform 256QAM. To increase a data transmission rate, a data distribution may have a distribution in which probability of uncertainty is the highest. Accordingly, if symbols are distributed before transmission as a Gaussian distribution for an origin as the distribution in which probability of uncertainty is high, a data transmission rate for a specific signal-to-noise ratio (SNR) can be further increased.

[699] A symbol mapper may map data to a symbol having a Gaussian distribution on a constellation according to a non-uniform symbol method.

[700] FIG. 129 is a view showing an example of deciding a mapped symbol according to a non-uniform symbol mapping method. An interval between symbols in the non-uniform symbol mapping method is not uniform and an interval between symbols becomes narrower as the symbols approach the origin. Therefore, a decision axis may be narrower as the symbols approach the origin.

[701] A symbol demapper performs demapping according to a method corresponding to a non-uniform symbol method which maps symbols in a Gaussian distribution on a constellation and outputs demapped bit data.

[702] The non-uniform symbol mapping methods illustrated in FIGs. 128 and 129 may use a hybrid symbol mapping method together with the above-described symbol mapping method. Namely, a third symbol mapping method including the non-uniform symbol mapping method and the above-described symbol mapping method may be used according to an input data interval. The detailed embodiments for the hybrid symbol mapping method have already been described.

[703] The method of transmitting/receiving a signal and the apparatus for transmitting/receiving a signal are not limited to the above-described embodiments but may be applied to all systems for transmitting/receiving signals such as broadcasting and communication signals. For example, when transmitting/receiving a broadcasting signal, the present invention may be applied to a transmitting/receiving system using an OFDM method such as digital video broadcasting (DVB) and digital multimedia broadcasting (DMB).

[704] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and

variations of this invention provided they come within the scope of the appended claims and their equivalents.

Mode for the Invention

[705] The embodiments of the invention are described in the best mode of the invention.

Industrial Applicability

[706] A method of transmitting/receiving a signal and an apparatus for transmitting/receiving a signal of the present invention can be used in broadcast and communication fields.

Claims

- [1] An apparatus for transmitting a signal, comprising:
an forward error correction encoder performing error correction encoding for input data;
an interleaver interleaving the error-correction encoded data;
a symbol mapper mapping a first interval data of the interleaved data to symbol data in accordance with a symbol mapping method in which distances between a first symbol and neighboring symbols of the first symbol in a first constellation are constant, and mapping a second interval data of the interleaved data to symbol data in accordance with a symbol mapping method in which distances between a second symbol and neighboring symbols of the second symbol in a second constellation are constant; and
a transmitter modulating the mapped symbol data and transmitting the modulated data.
- [2] The apparatus according to claim 1, wherein the symbol mapper maps three neighboring symbols in the constellation to a equilateral triangle.
- [3] An apparatus for receiving a signal, comprising:
a demodulator demodulating a received signal;
a frame parser parsing the demodulated signal and output the parsed data;
a symbol mapper demapping a first interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a first symbol mapping method, scaling the demapped symbol according to a constellation size of the first symbol mapping method and outputting the scaled symbol, and demapping a second interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a second symbol mapping method, scaling the demapped symbol according to a constellation size of the second symbol mapping method and outputting the scaled symbol, and outputting the first bit streams and the second bit streams into one bit streams;
a deinterleaver deinterleaving the bit streams; and
a forward error correction decoder performing forward error correction decoding on the deinterleaved data.
- [4] The apparatus according to claim 3, wherein the symbol mapper comprising:
a symbol deinterleaver splitting the first interval of the symbol data and the second interval of the symbol data in the parsed data;
a first demapper demapping the first interval of the symbol data in accordance with the symbol demapping method corresponding to the first symbol mapping method;

- a first scaler multiplying a reliability value demapped by the first symbol mapping method by a scaling value according to the constellation size of the first symbol mapping method;
- a second demapper demapping the second interval of the symbol data in accordance with the symbol demapping method corresponding to the second symbol mapping method;
- a second scaler multiplying a reliability value demapped by the second symbol mapping method by a scaling value according to the constellation size of the second symbol mapping method; and
- a bit stream merger restoring the first bit streams according to the scaled reliability value output by the first scaler, restoring the second bit streams according to the scaled reliability value output by the second scaler, and outputting the first bit streams and the second bit streams to one bit streams.
- [5] The apparatus according to claim 4, wherein one of the first scaler and the second scaler comprising:
- a scaling factor generator generating a scaling factor; and
- a multiplier multiplying the generated scaling factor by the demapping result.
- [6] The apparatus according to claim 5, wherein the scaling factor is one a reciprocal of average symbol size in the constellation or average power of the constellation.
- [7] A method of transmitting a signal, the method comprising:
- performing error correction encoding for input data;
- interleaving the error-correction encoded data;
- a symbol mapper mapping a first interval data of the interleaved data to symbol data in accordance with a symbol mapping method in which distances between a first symbol and neighboring symbols of the first symbol in a first constellation are constant, and mapping a second interval data of the interleaved data to symbol data in accordance with a symbol mapping method in which distances between a second symbol and neighboring symbols of the second symbol in a second constellation are constant; and
- modulating the mapped symbol data and transmitting the modulated data.
- [8] The method according to claim 7, wherein the symbol mapper maps three neighboring symbols in the constellation to a equilateral triangle.
- [9] A method of receiving a signal, the method comprising:
- demodulating a received signal;
- parsing a frame of the demodulated signal and output the parsed data;
- demapping a first interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a first symbol mapping method, scaling the demapped symbol according to a constellation size of the first symbol

mapping method and outputting the scaled symbol, and demapping a second interval of symbol data of the output data in accordance with a symbol demapping method corresponding to a second symbol mapping method, scaling the demapped symbol according to a constellation size of the second symbol mapping method and outputting the scaled symbol, and outputting the first bit streams and the second bit streams into one bit streams; deinterleaving the bit streams; and performing forward error correction decoding on the deinterleaved data.

[10] The method according to claim 9, wherein the outputting of the one bit streams in the demapping, comprising:

splitting the first interval of the symbol data and the second interval of the symbol data in the parsed data;

demapping the first interval of the symbol data in accordance with the symbol demapping method corresponding to the first symbol mapping method and

demapping the second interval of the symbol data in accordance with the symbol demapping method corresponding to the second symbol mapping method;

multiplying a reliability value demapped by the first symbol mapping method by a scaling value according to the constellation size of the first symbol mapping method, and multiplying a reliability value demapped by the second symbol mapping method by a scaling value according to the constellation size of the second symbol mapping method; and

outputting the respective scaled bit streams to one bit streams.

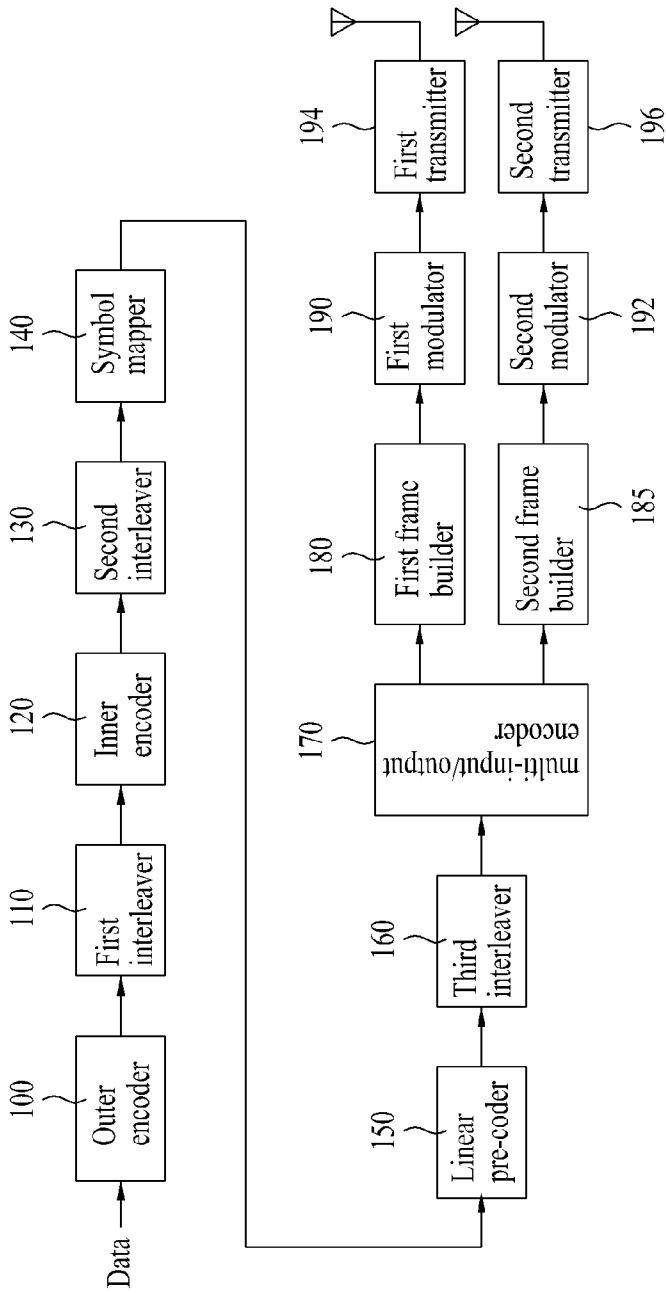
[11] The method according to claim 9, wherein the scaling in the outputting of the respective scaled bit streams to one bit streams, comprising:

generating a scaling factor; and

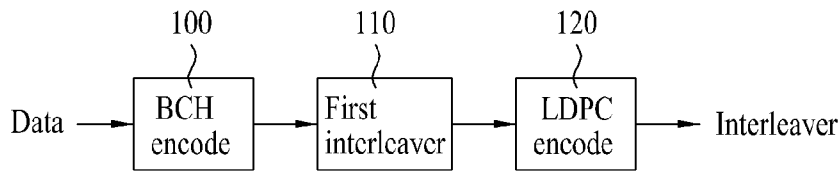
multiplying the generated scaling factor by the demapping result.

[12] The method according to claim 11, wherein the scaling factor is one a reciprocal of average symbol size in the constellation or average power of the constellation.

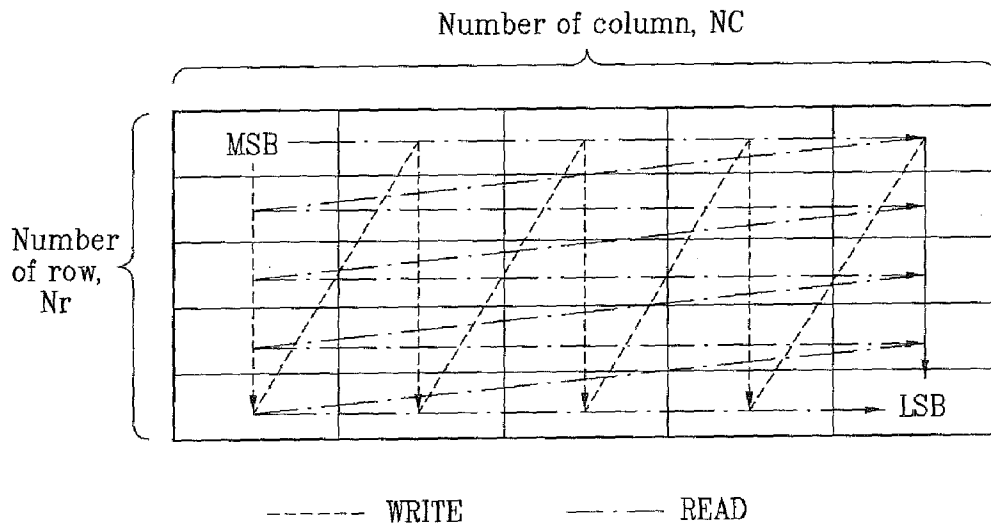
[Fig. 1]



[Fig. 2]



[Fig. 3]



[Fig. 4]

$$\Pi(i) = (P \cdot \Pi(i-1) + N/4 - 1)_{\text{mod } N}, \Pi(0) = 0;$$

$$k = F(n) = d_n - N/2$$

[Fig. 5]

$$\Pi(i) = 13 \cdot \Pi(i-1) + 511(\text{mod } 2048) \text{ and } \Pi(0)=0;$$

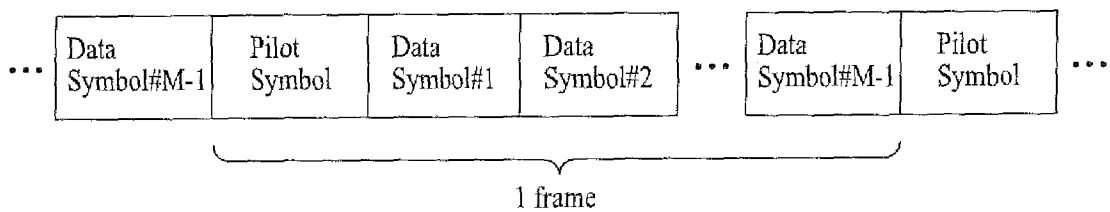
$$k = F(n) = d_n - 1024$$

i	$\Pi(i)$	d_n	n	k
0	0			
1	511	511	0	-513
2	1010	1010	1	-14
3	1353	1353	2	239
4	1716	1716	3	692
5	291	291	4	-733
6	198			
7	1037	1037	5	13
8	1704	1704	6	680
9	135			
10	218			
11	1297	1297	7	273
12	988	988	8	-36
13	1076	1067	9	43
14	46			
15	1109	1109	10	85
16	592	592	11	-432
17	15			
18	706	706	12	-318
⋮	⋮	⋮	⋮	⋮
2044	1676	1676	1533	652
2045	1819			
2046	1630	1630	1534	606
2047	1221	1221	1535	197

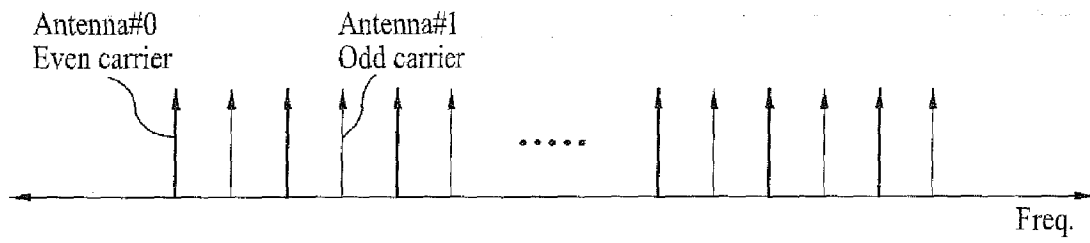
[Fig. 6]

Output	$y(t)$	$y(t+T)$
Tx. #1	s_0	$-s_1^*$
Tx. #2	s_1	s_0^*

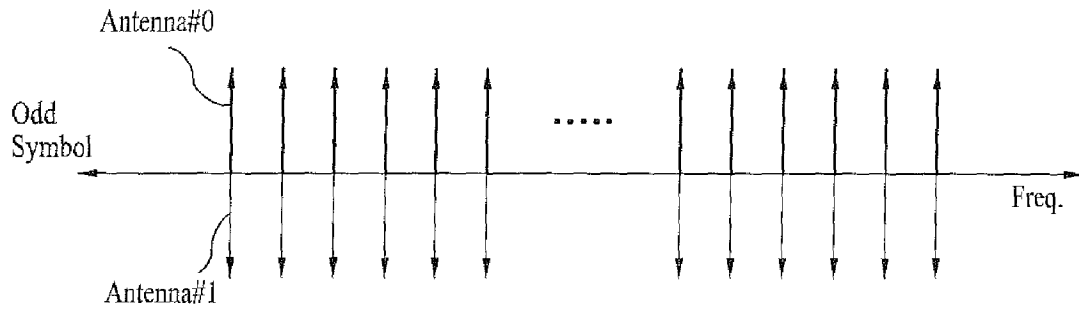
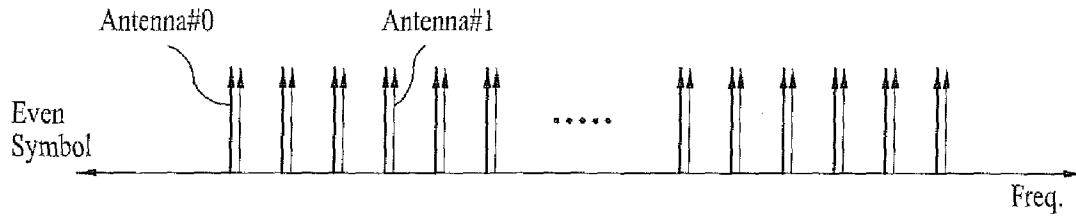
[Fig. 7]



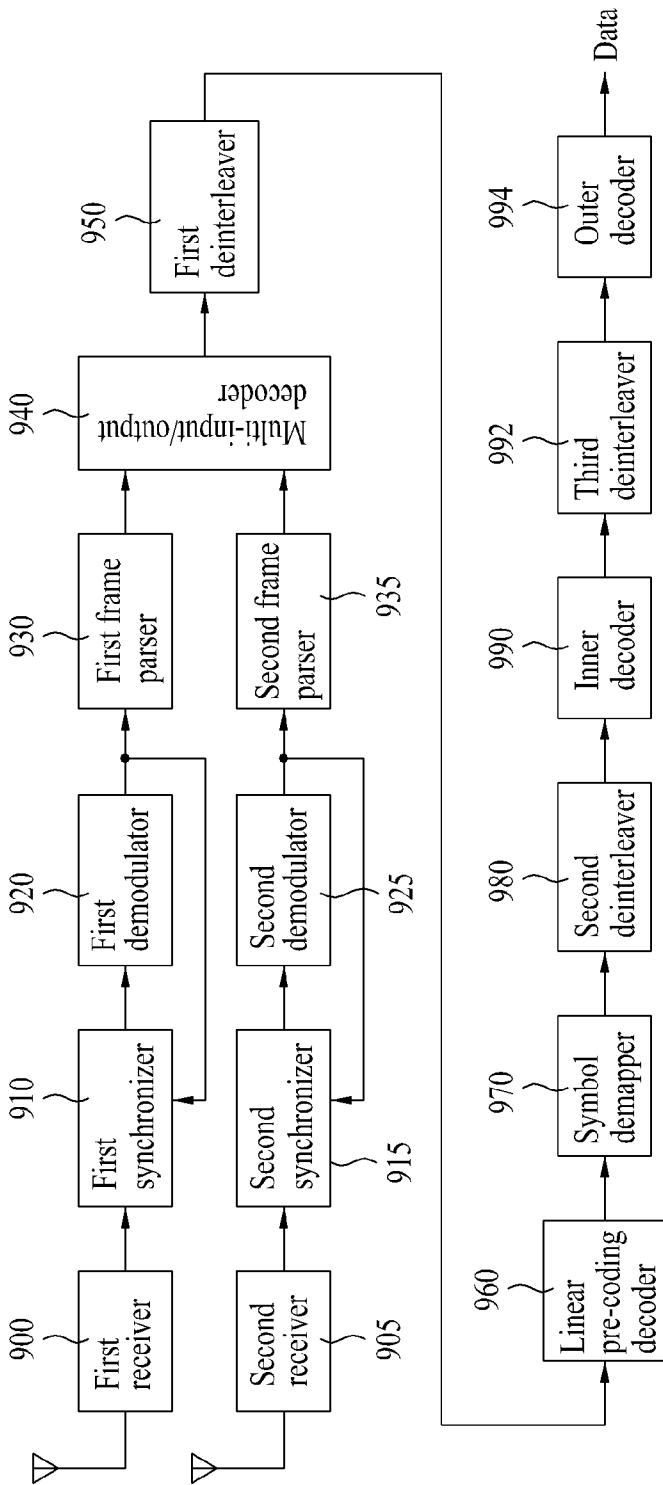
[Fig. 8]



[Fig. 9]



[Fig. 10]



[Fig. 11]

$$r_{s,i}(k) = h_{s,0,i}(k)s_s(k) + h_{s,1,i}(k)s_{s+1}(k) + n_s(k)$$

$$r_{s+1,i}(k) = -h_{s+1,0,i}(k)s_{s+1}^*(k) + h_{s+1,1,i}(k)s_s^*(k) + n_{s+1}(k)$$

[Fig. 12]

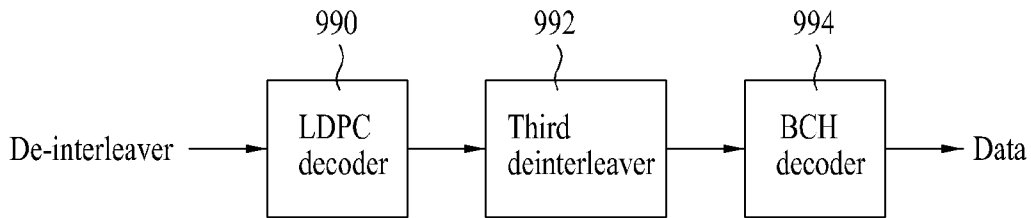
$$r_0 = r(t) = h_0s_0 + h_1s_1 + n_0$$

$$r_1 = r(t+T) = -h_0s_1^* + h_1s_0^* + n_1$$

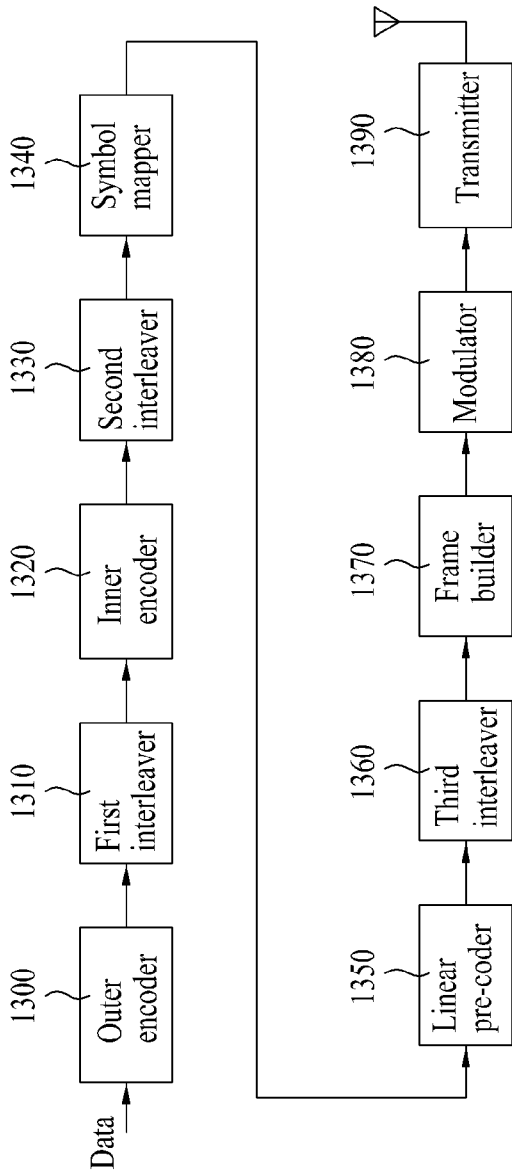
$$\bar{s}_0 = h_0^*r_0 + h_1r_1^*$$

$$\bar{s}_1 = h_1^*r_0 - h_0r_1^*$$

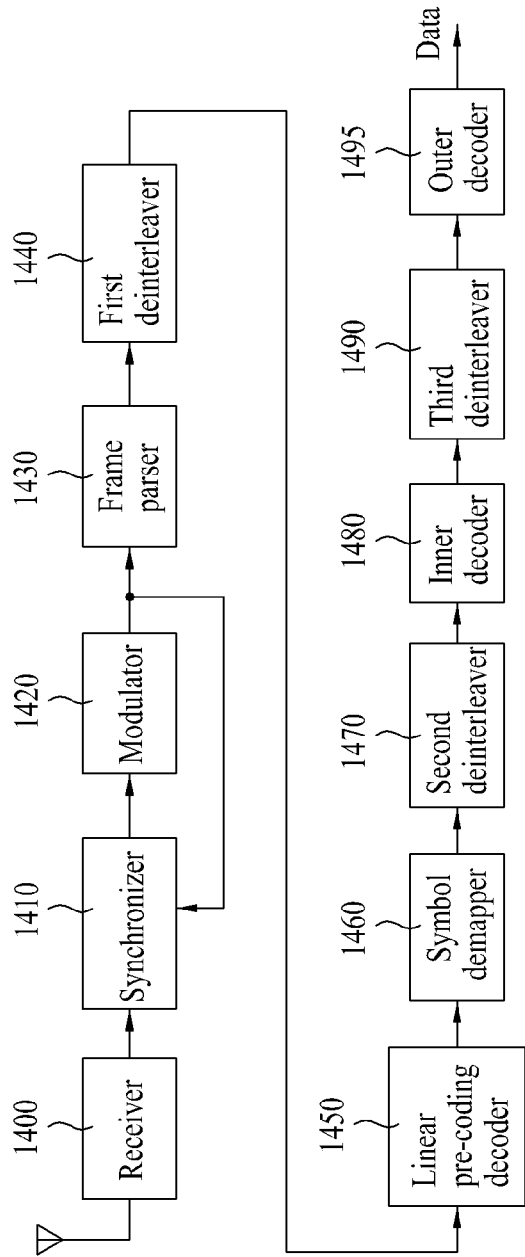
[Fig. 13]



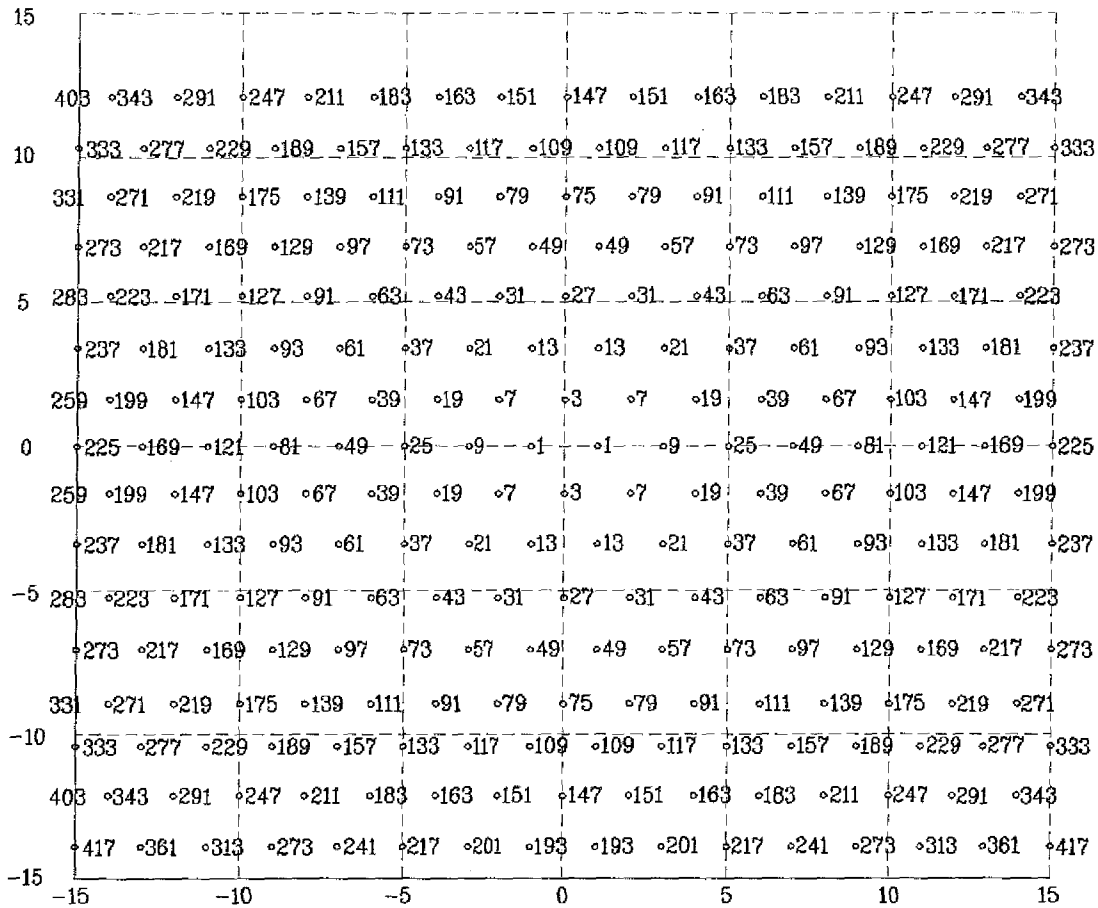
[Fig. 14]



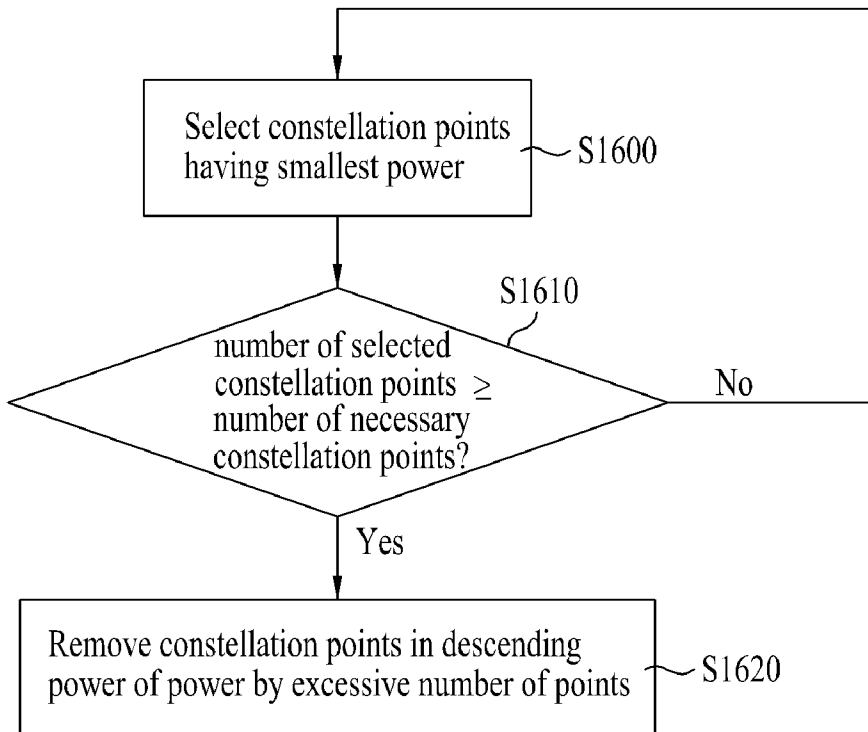
[Fig. 15]



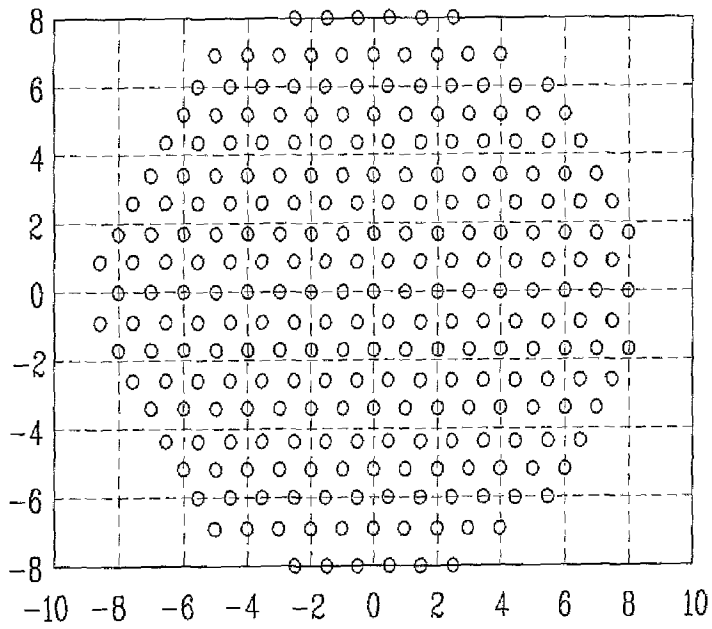
[Fig. 16]



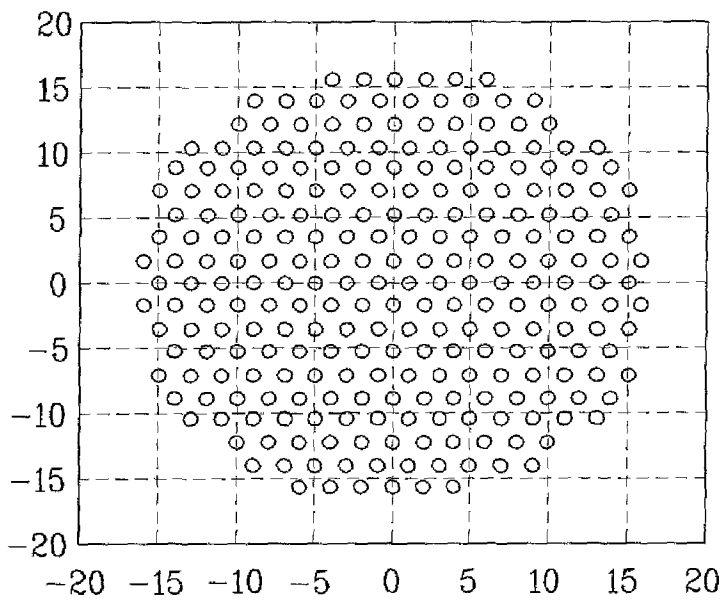
[Fig. 17]



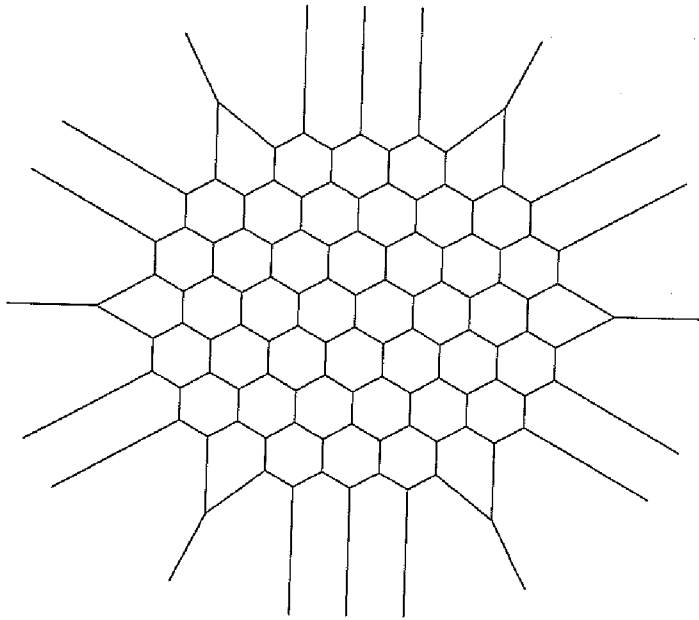
[Fig. 20]



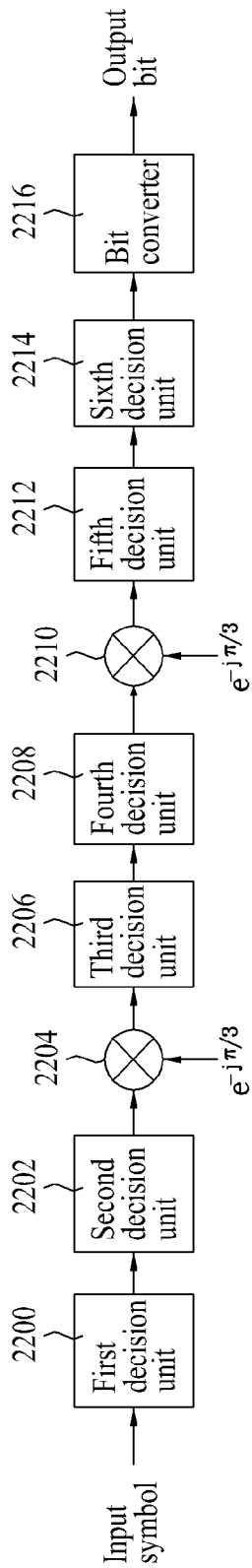
[Fig. 21]



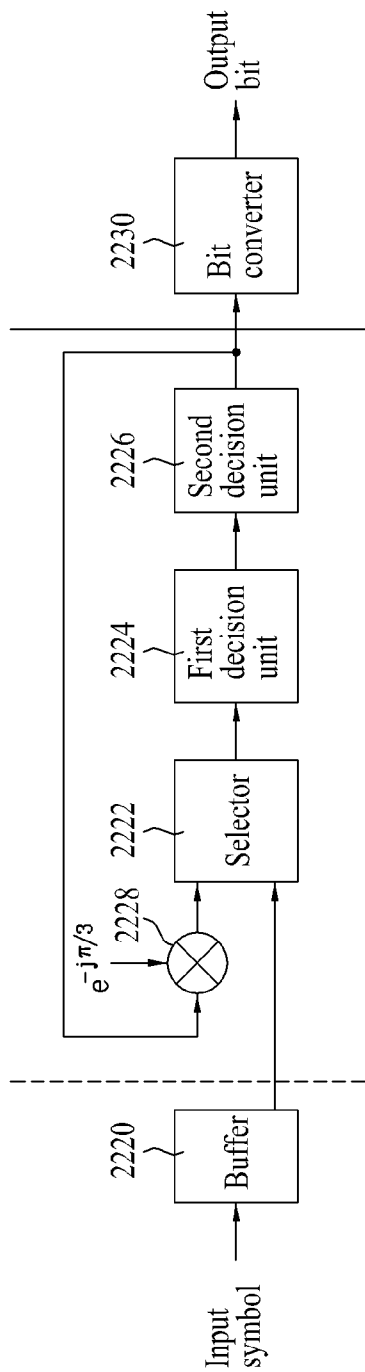
[Fig. 22]



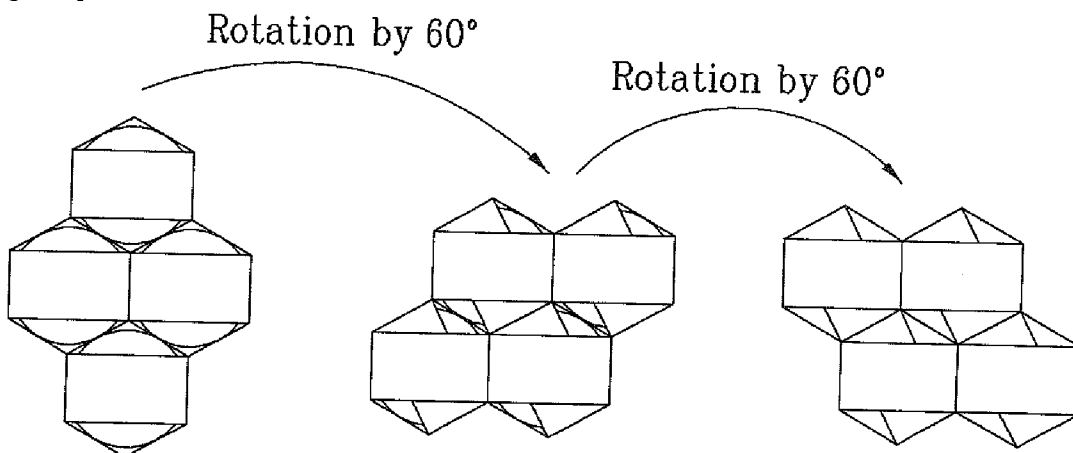
[Fig. 23]



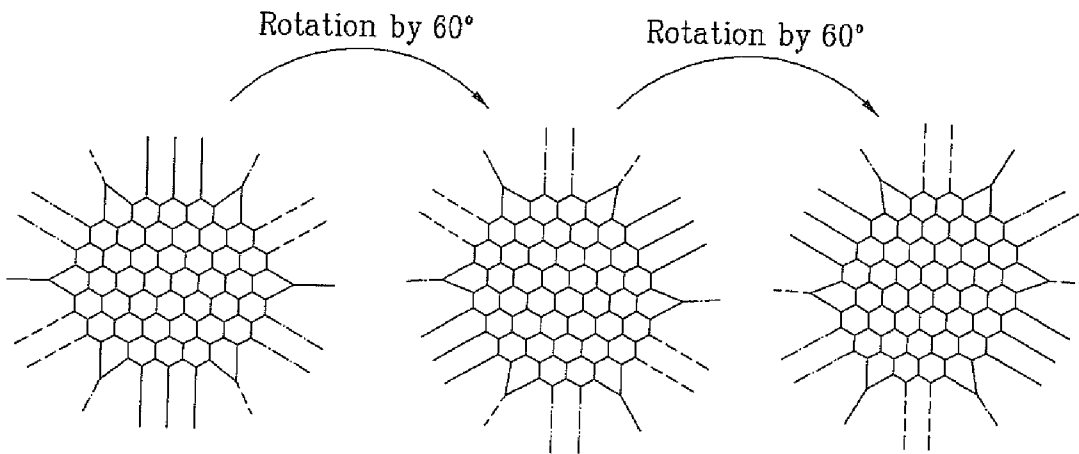
[Fig. 24]



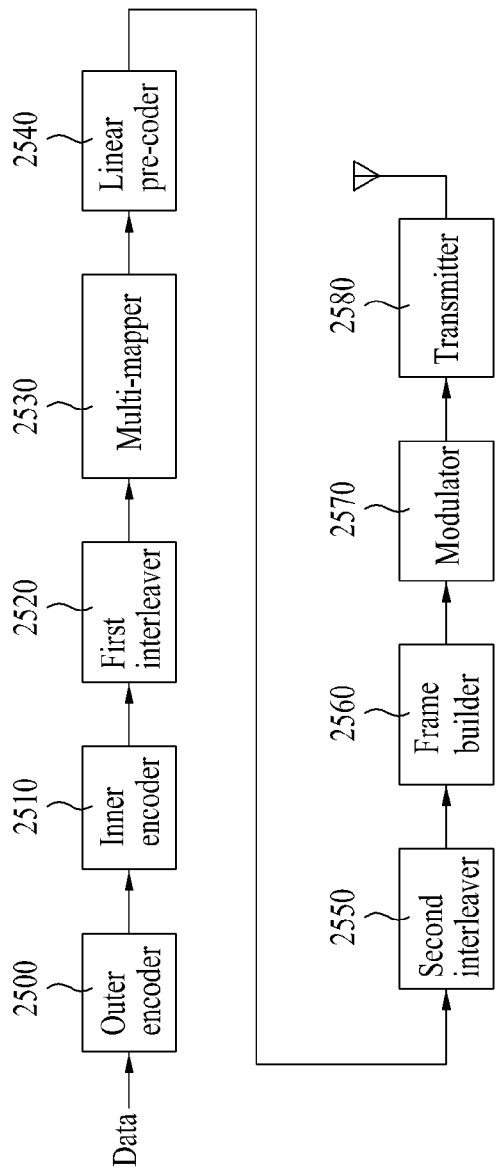
[Fig. 25]



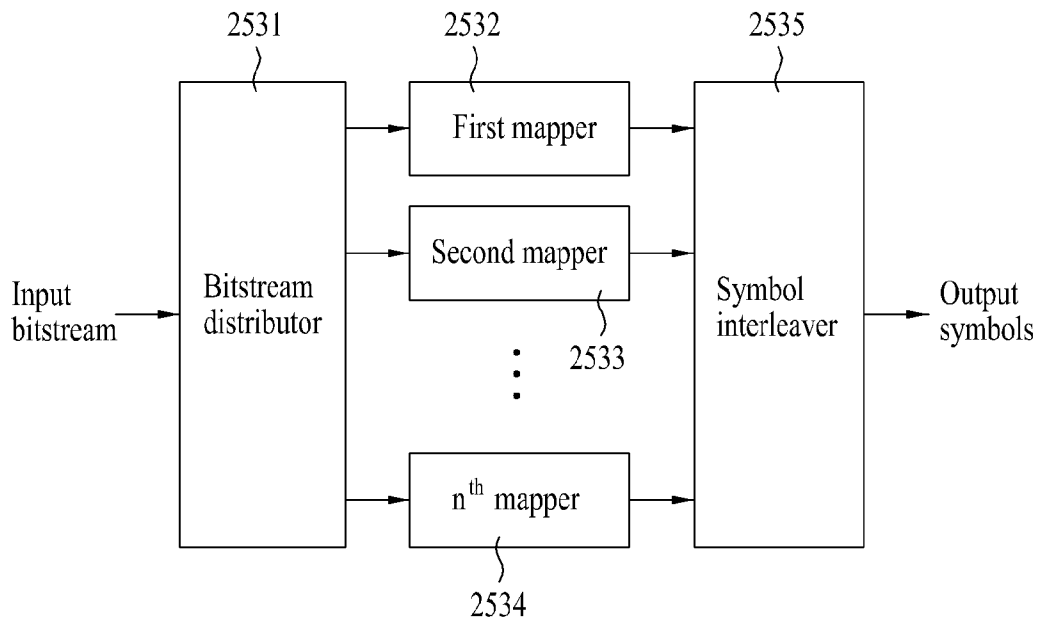
[Fig. 26]



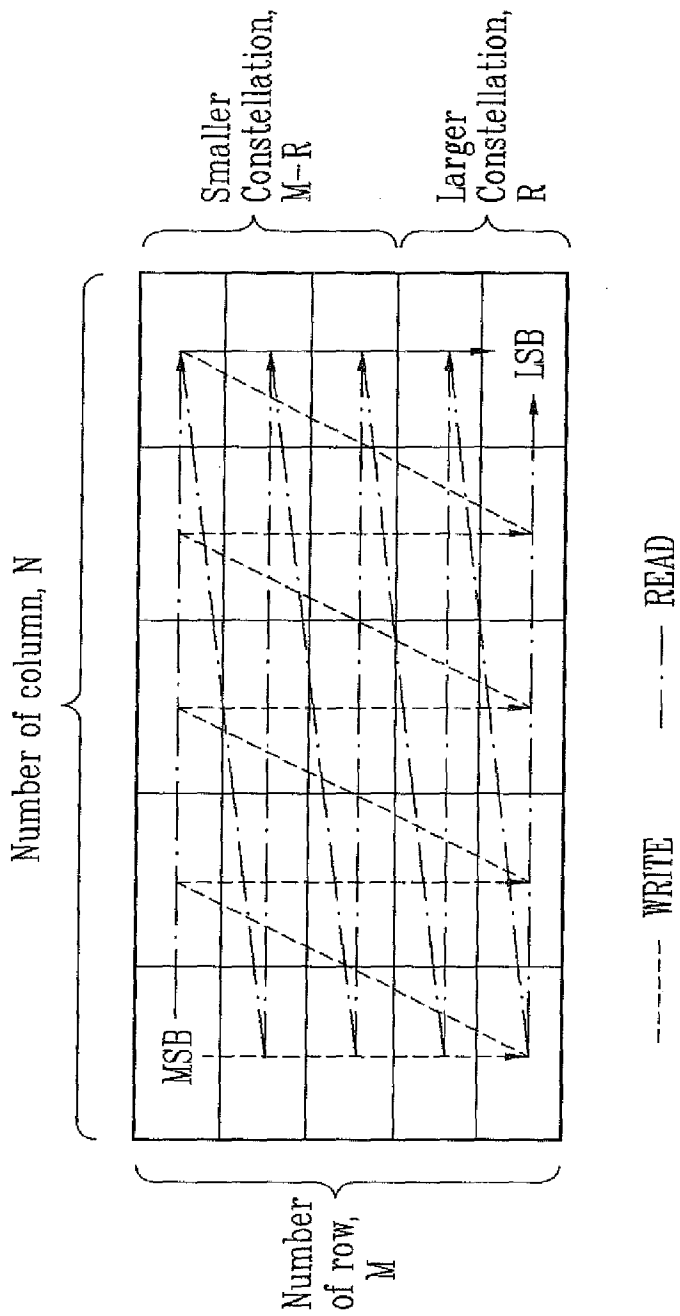
[Fig. 27]



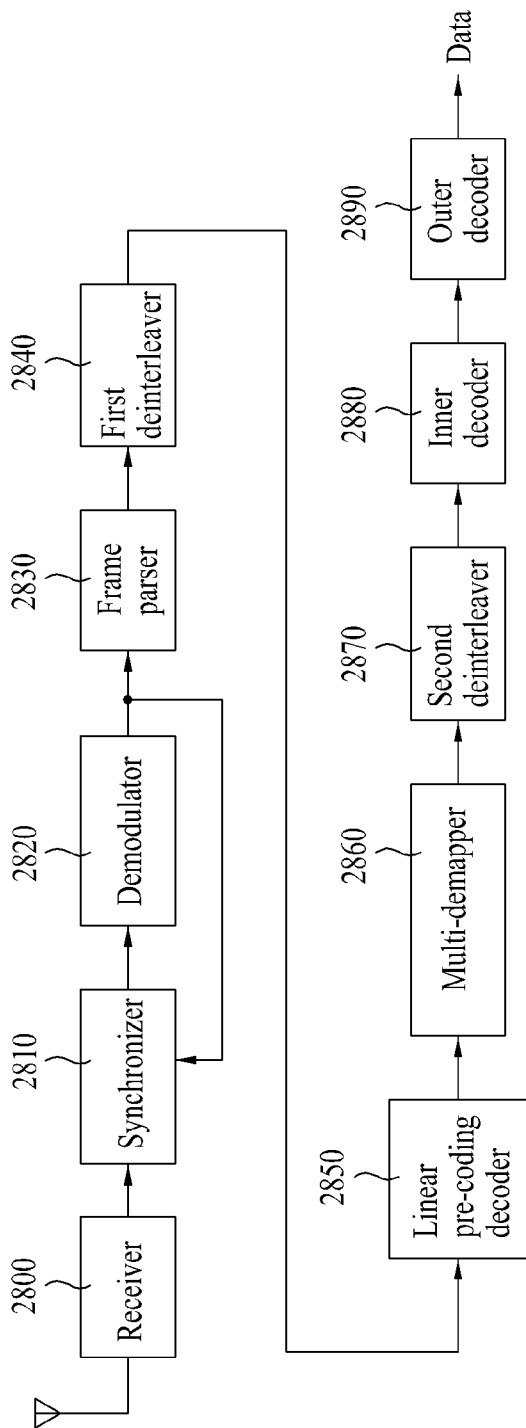
[Fig. 28]



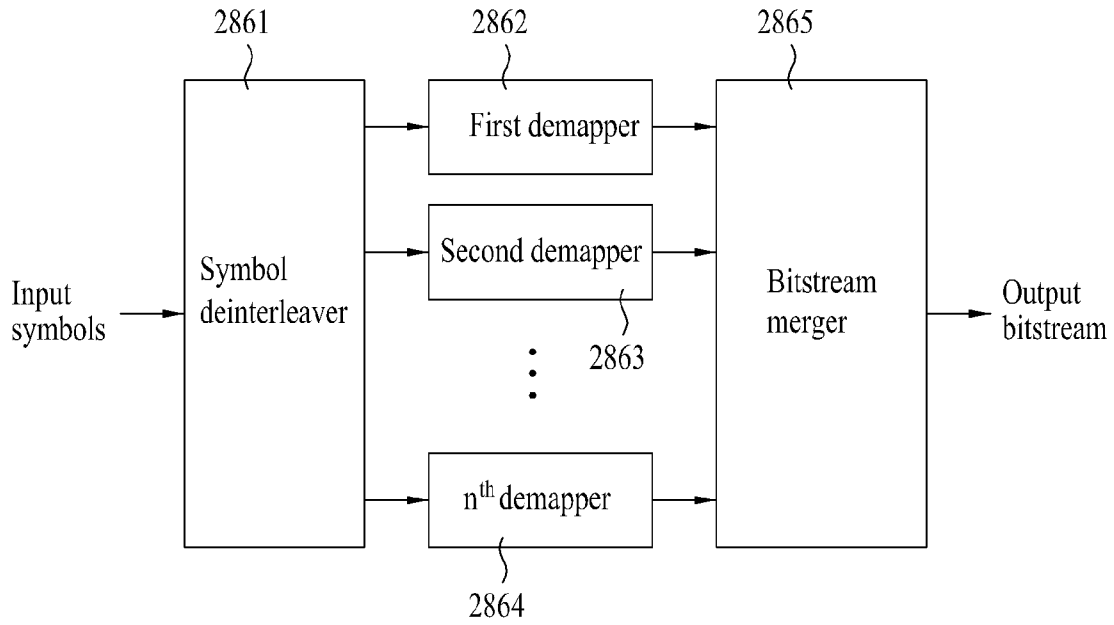
[Fig. 29]



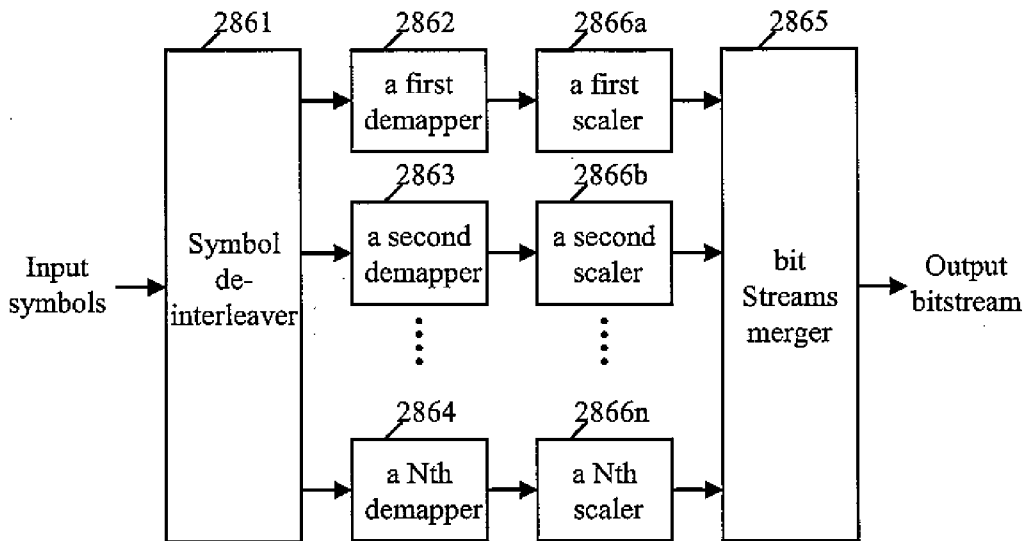
[Fig. 30]



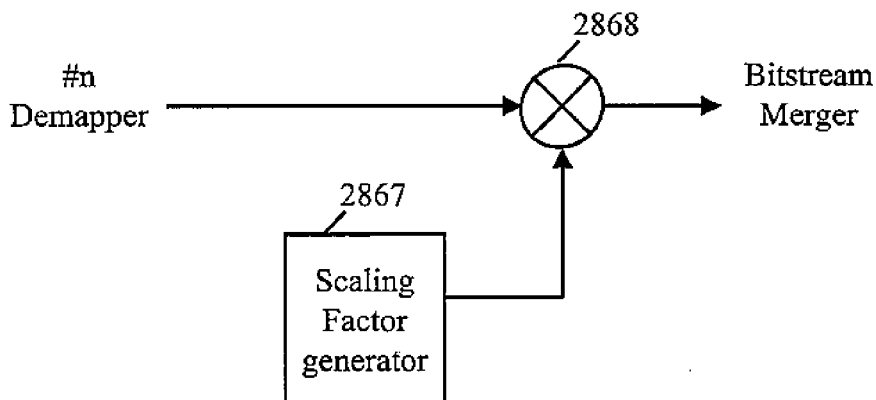
[Fig. 31]



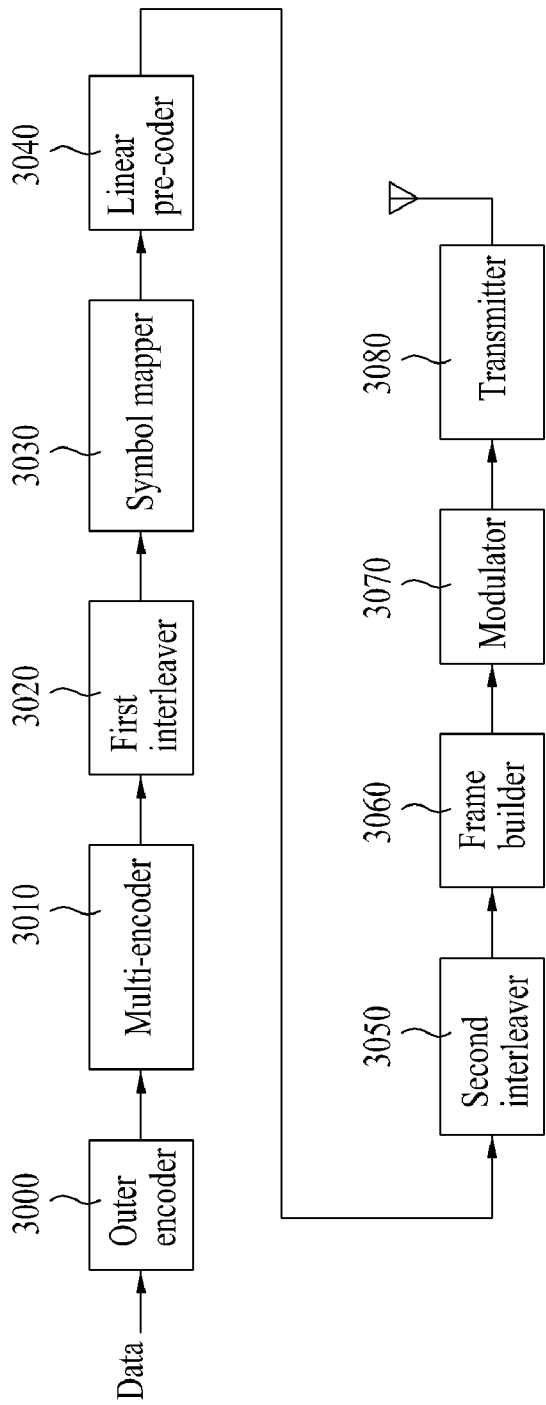
[Fig. 32]



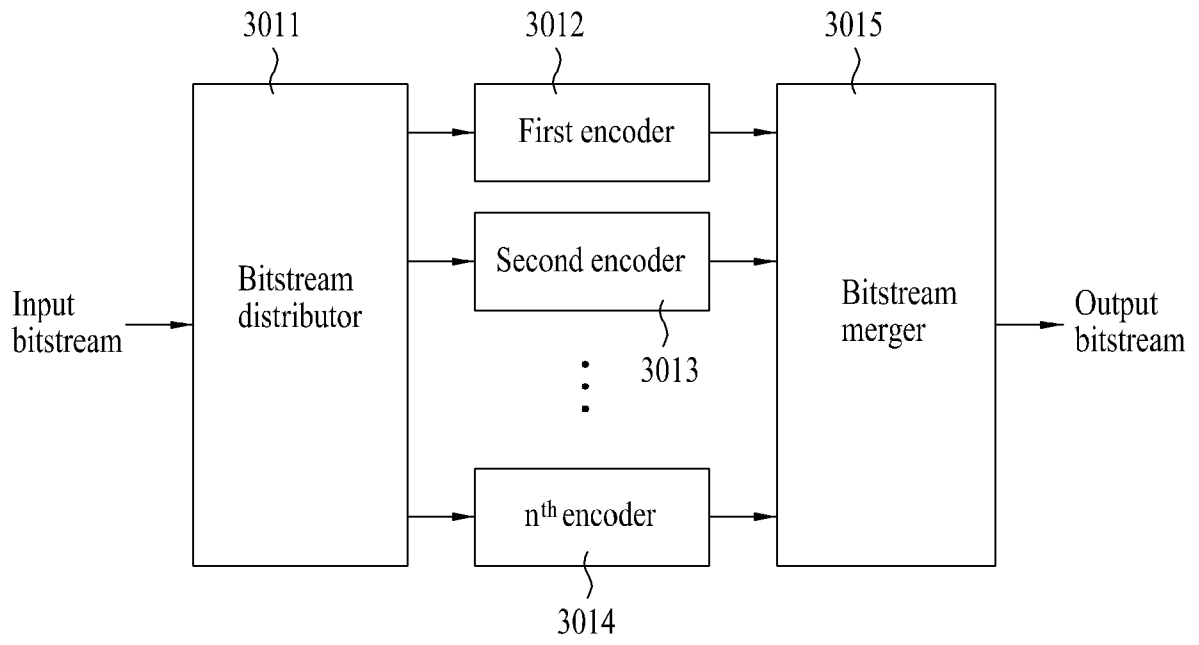
[Fig. 33]



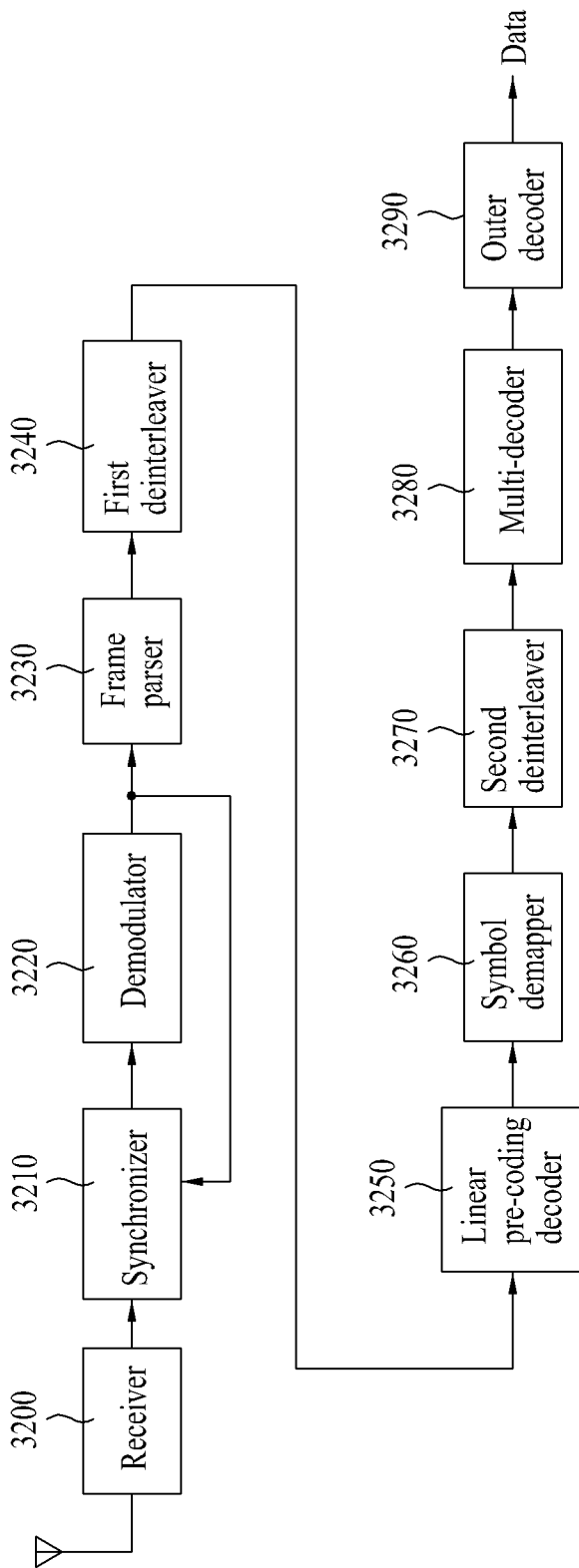
[Fig. 34]



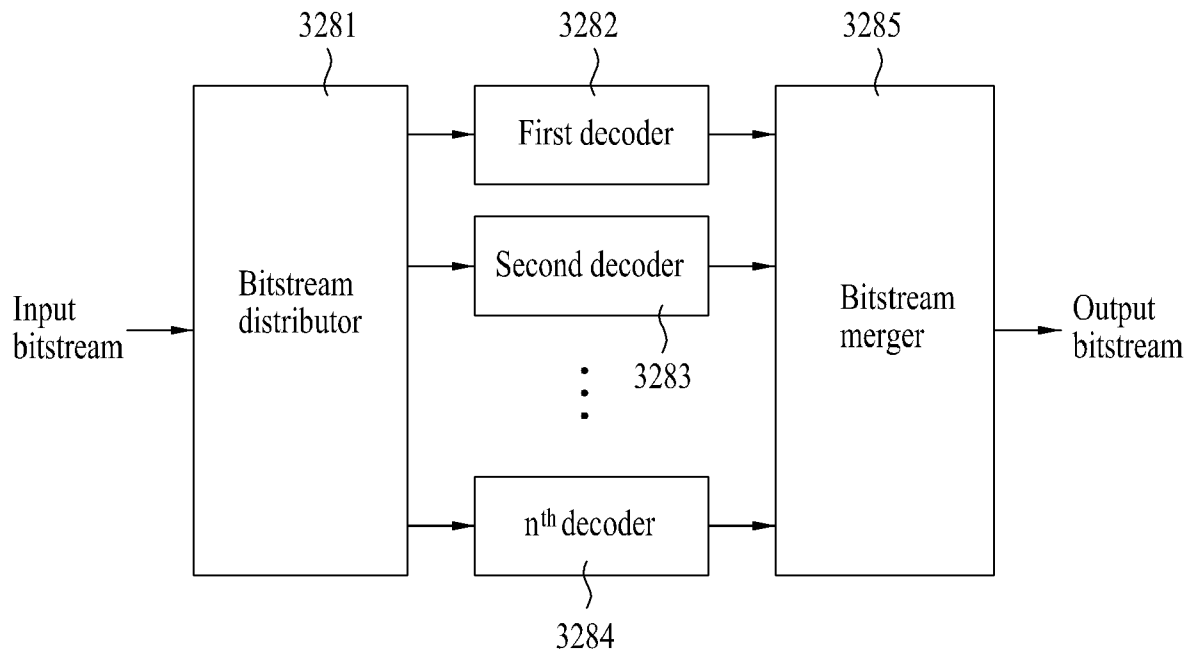
[Fig. 35]



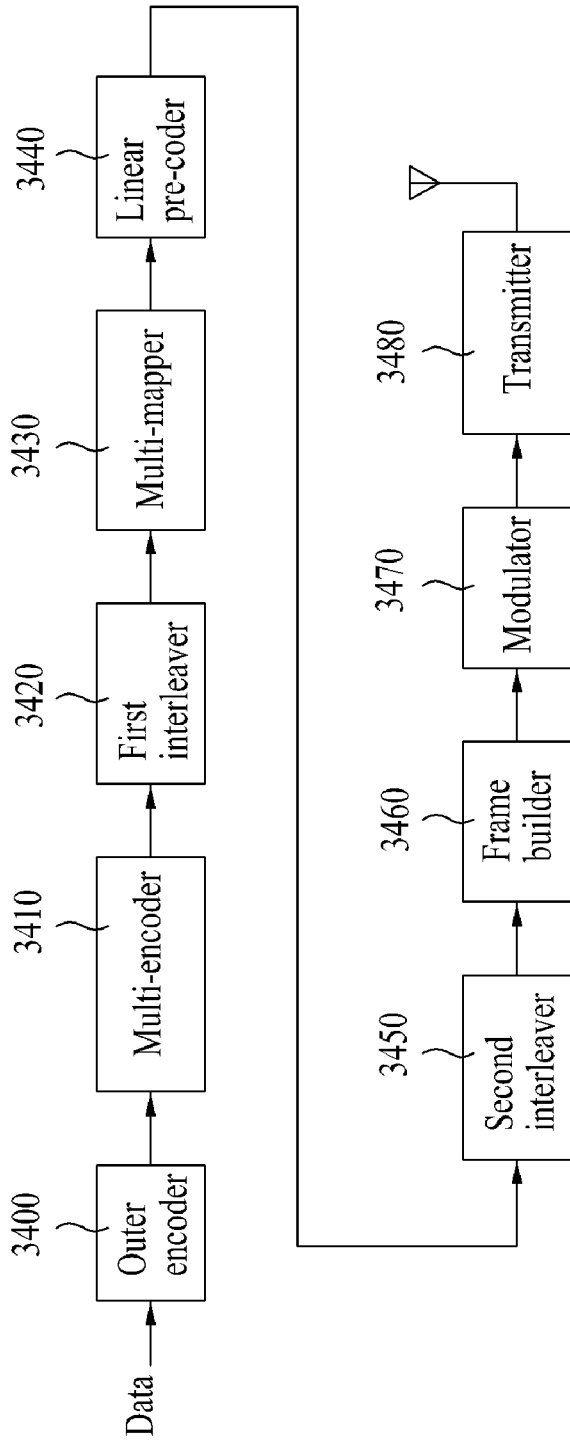
[Fig. 36]



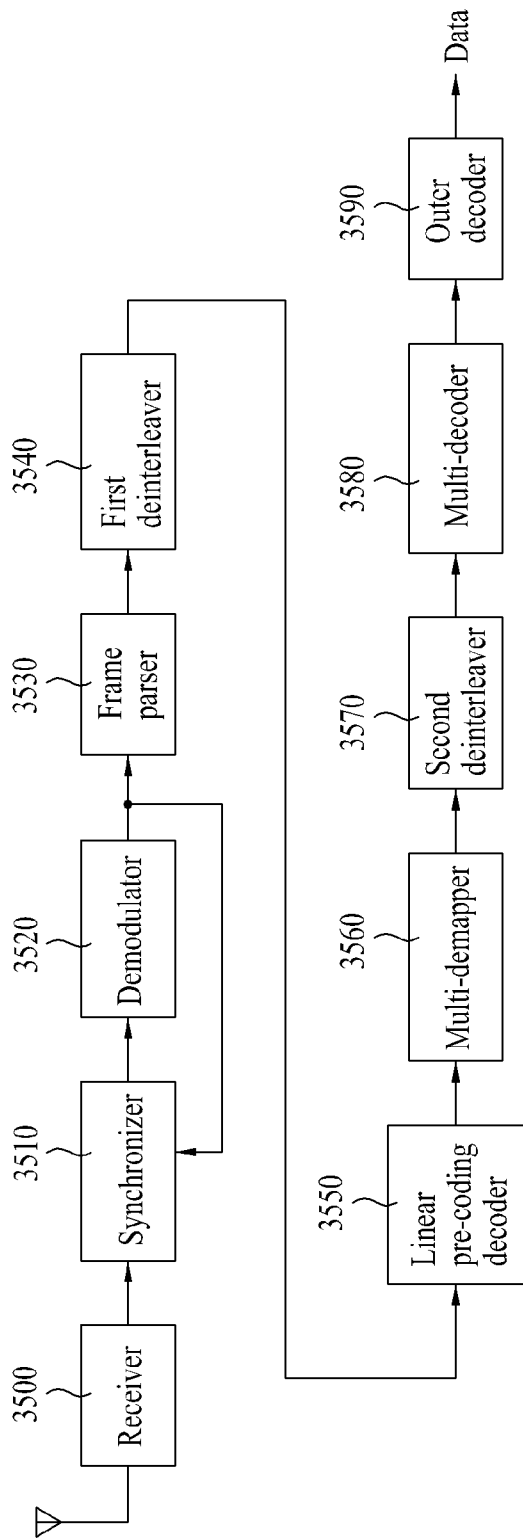
[Fig. 37]



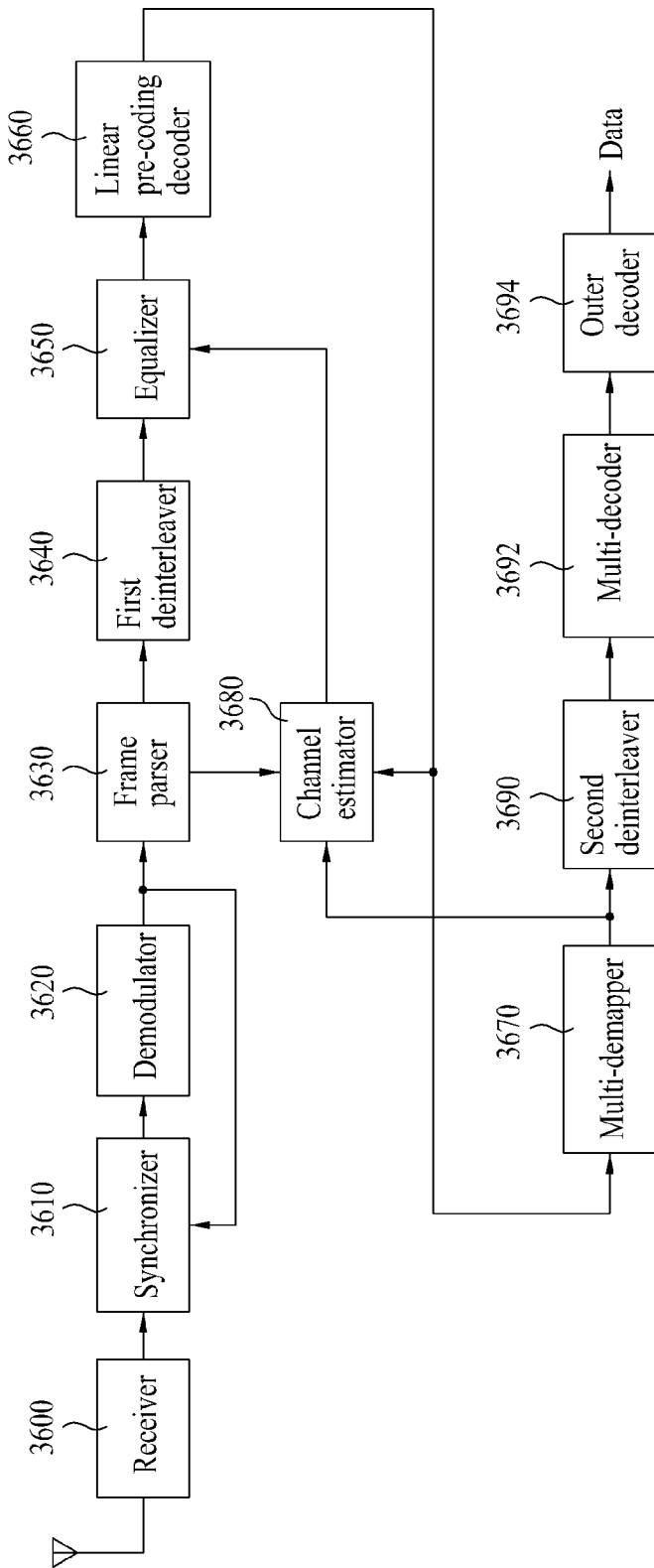
[Fig. 38]



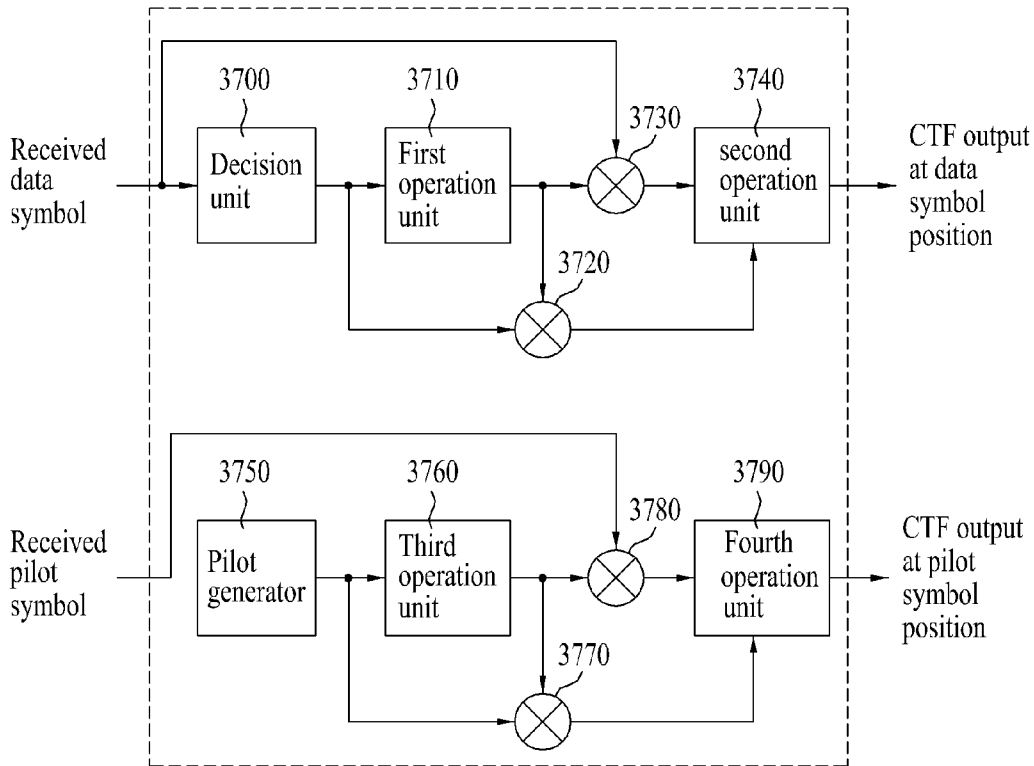
[Fig. 39]



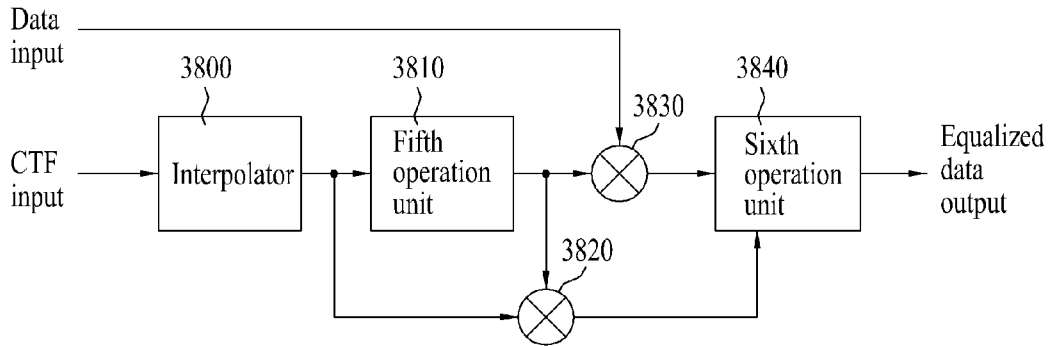
[Fig. 40]



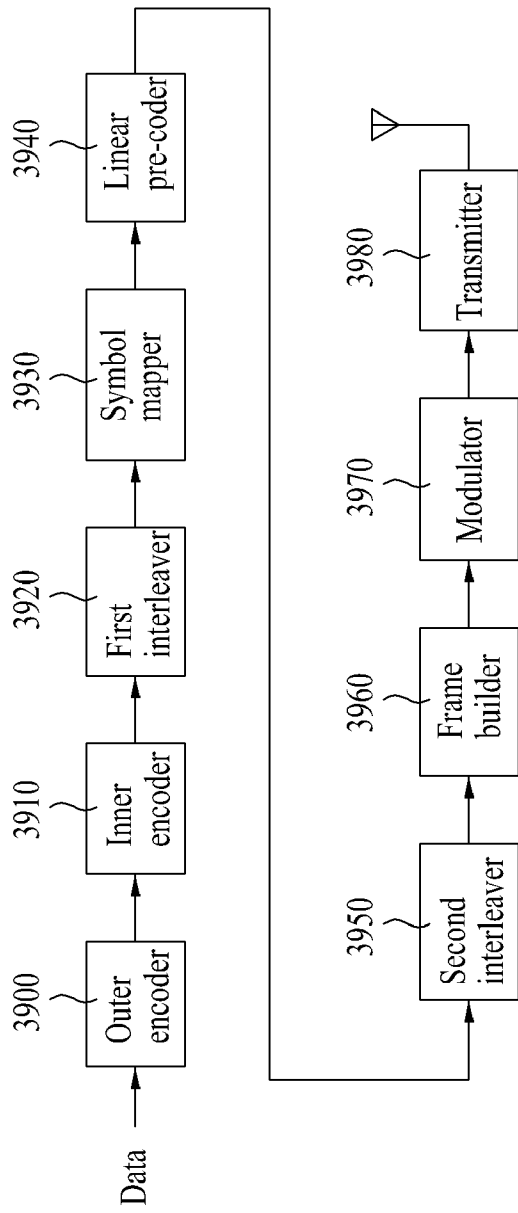
[Fig. 41]



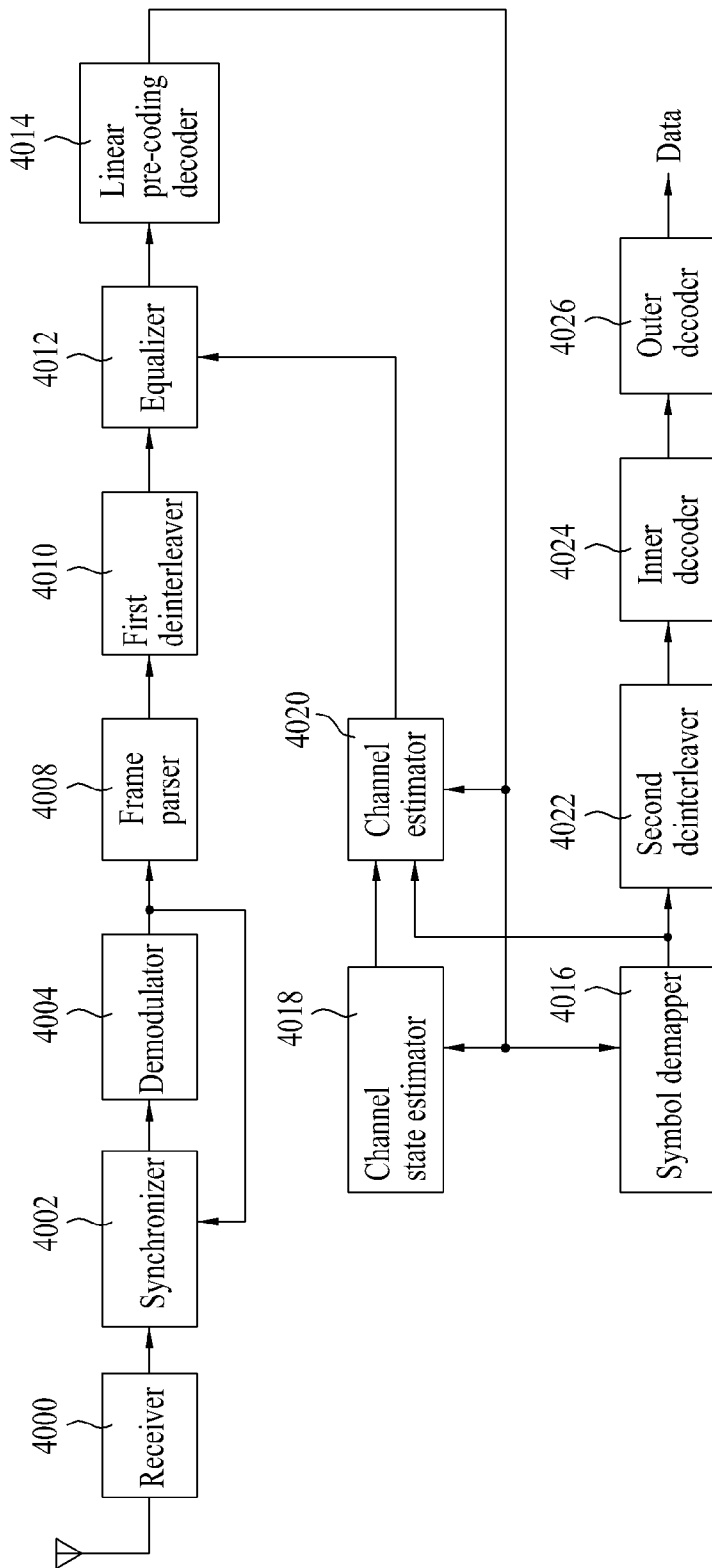
[Fig. 42]



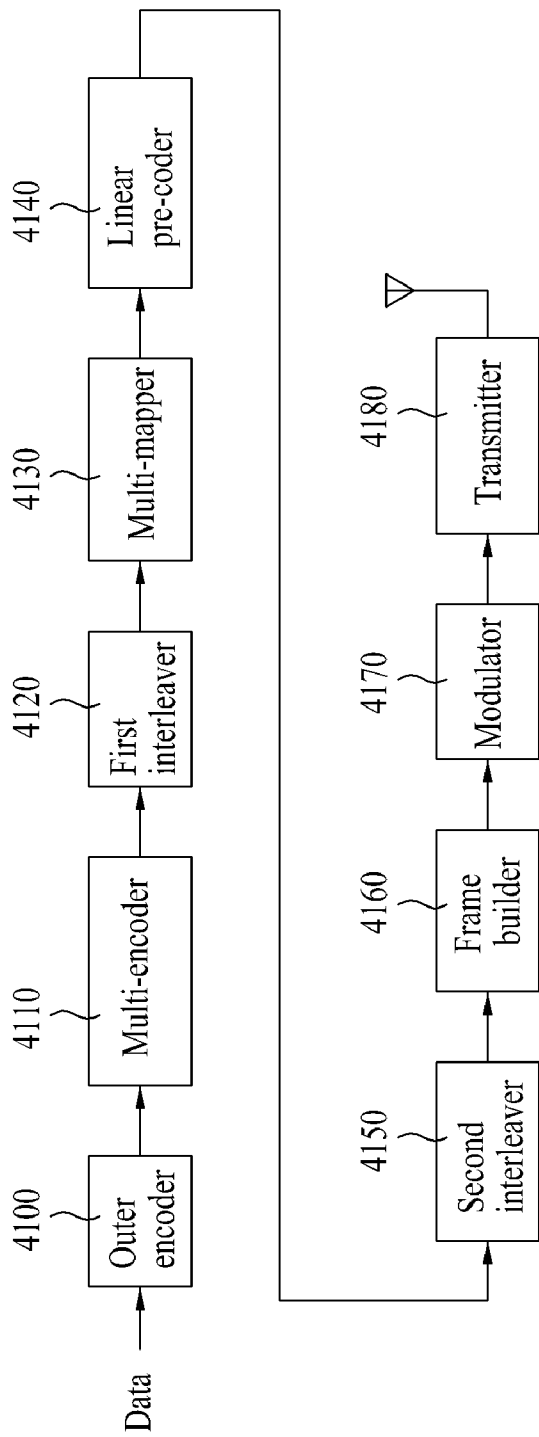
[Fig. 43]



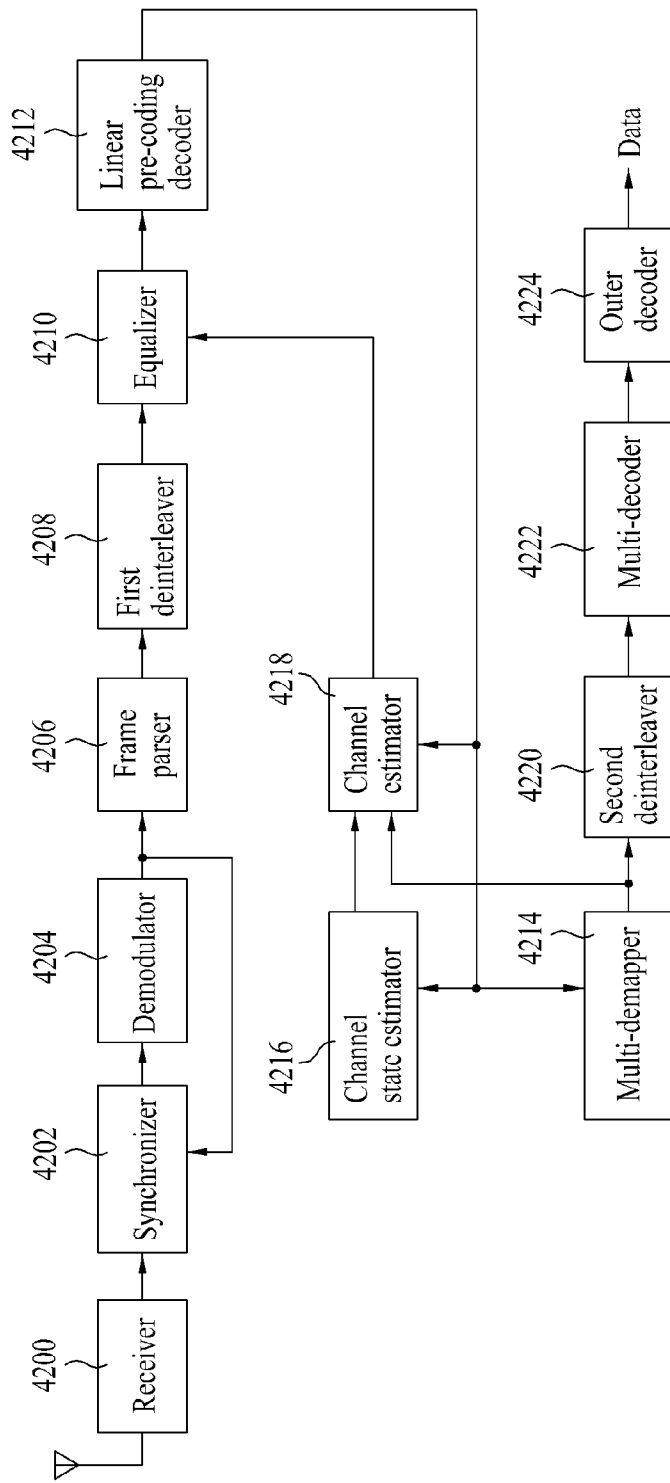
[Fig. 44]



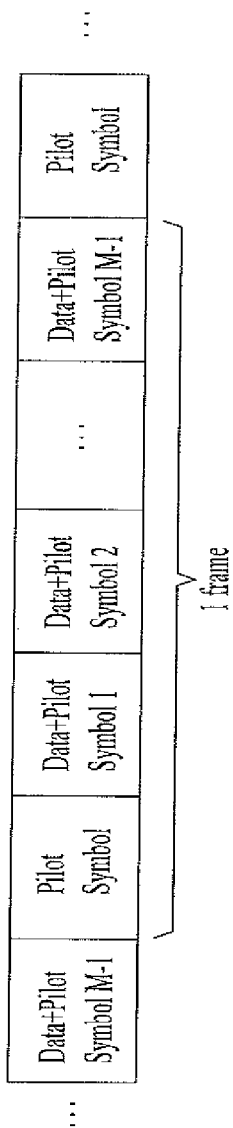
[Fig. 45]



[Fig. 46]



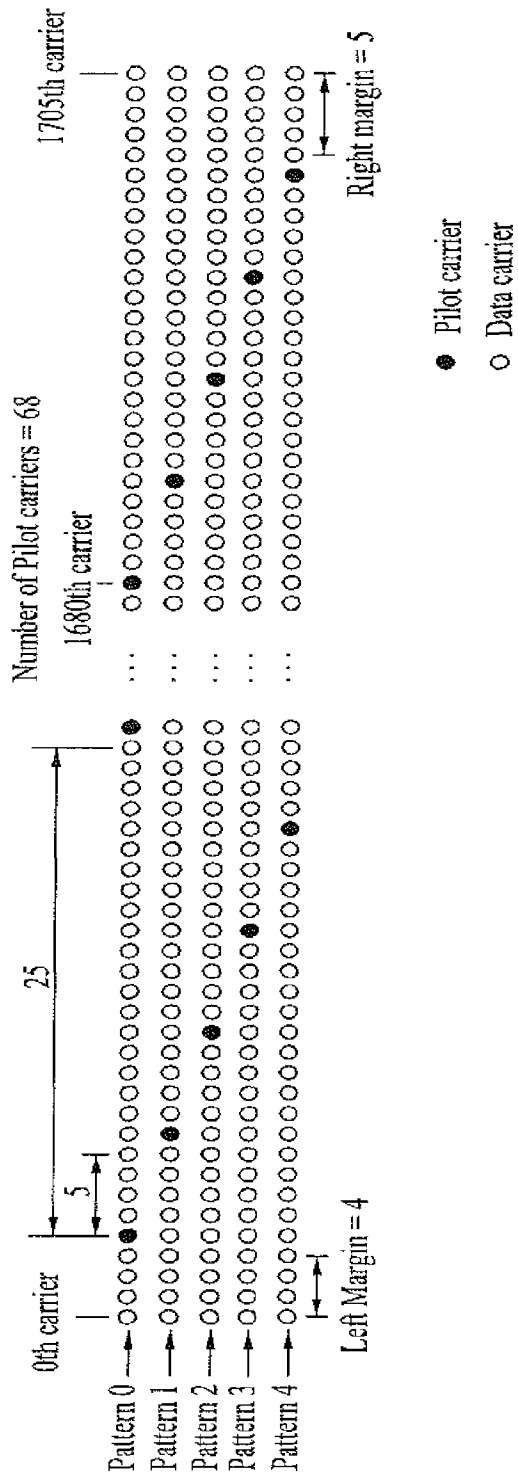
[Fig. 47]



[Fig. 48]

FFT mode	# of available carriers	# of pilot carriers	# of data carriers
8K	6749	269	6480
4K	3375	135	3240
2K	1688	68	1620

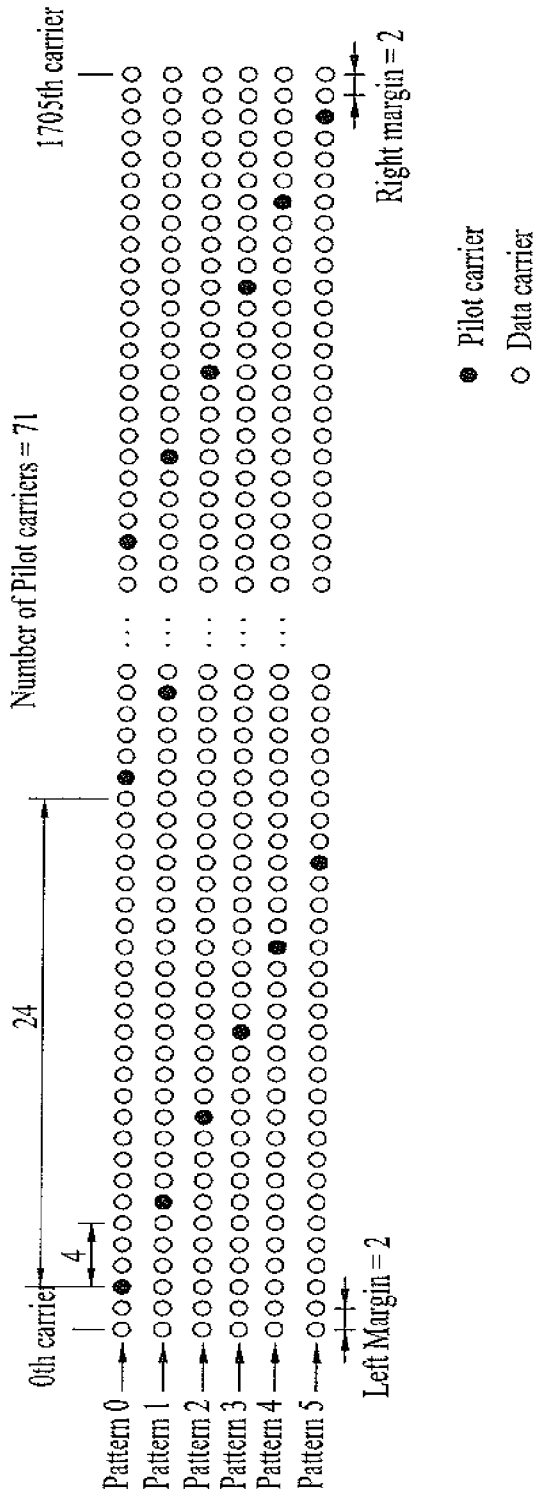
[Fig. 49]



[Fig. 50]

FFT mode	# of pilot	Left Margin	Right Margin
2K	68	4	5
4K	135	19	19
8K	269	48	48

[Fig. 51]



[Fig. 52]

FFT mode	# of pilot	Left Margin	Right Margin
2K	71	2	2
4K	142	2	2
8K	284	2	2

[Fig. 53]

Constellation		LDPC mode	64800	16200
Constellation	Rate of larger constellation		Number of symbols	Number of symbols
256-QAM	1.0		8100	2025
Hyb256-64_r8	0.8		8640	2160
Hyb256-64_r6	0.6		9180	2295
Hyb256-64_r4	0.4		9720	2430
Hyb256-64_r2	0.2		10260	2565
64-QAM	1.0		10800	2700
Hyb64-16_r8	0.8		11880	2970
Hyb64-16_r6	0.6		12960	3240
Hyb64-16_r4	0.4		14040	3510
Hyb64-16_r2	0.2		15120	3780
16-QAM	1.0		16200	4050
Hyb16-4_r8	0.8		19440	4860
Hyb16-4_r6	0.6		22680	5670
Hyb16-4_r4	0.4		25920	6480
Hyb16-4_r2	0.2		29160	7290
4-QAM	1.0		32400	8100

[Fig. 54]

QAM mode \ FFT mode	8K	4K	2K
256-QAM	4	2	1
Hyb256-64_r8	3	3	3
Hyb256-64_r6	12	6	3
Hyb256-64_r4	2	1	1
Hyb256-64_r2	12	6	3
64-QAM	3	3	3
Hyb64-16_r8	6	3	3
Hyb64-16_r6	1	1	1
Hyb64-16_r4	6	3	3
Hyb64-16_r2	3	3	3
16-QAM	2	1	1
Hyb16-4_r8	1	1	1
Hyb16-4_r6	2	1	1
Hyb16-4_r4	1	1	1
Hyb16-4_r2	2	1	1
4-QAM	1	1	1

[Fig. 55]

QAM mode \ FFT mode	8K	4K	2K
256-QAM	5	5	5
Hyb256-64_r8	4	8	16
Hyb256-64_r6	17	17	17
Hyb256-64_r4	3	3	6
Hyb256-64_r2	19	19	19
64-QAM	5	10	20
Hyb64-16_r8	11	11	22
Hyb64-16_r6	2	4	8
Hyb64-16_r4	13	13	26
Hyb64-16_r2	7	14	28
16-QAM	5	5	10
Hyb16-4_r8	3	6	12
Hyb16-4_r6	7	7	14
Hyb16-4_r4	4	8	16
Hyb16-4_r2	9	9	18
4-QAM	5	10	20

[Fig. 56]

QAM mode \ FFT mode	8K	4K	2K
256-QAM	16	8	4
Hyb256-64_r8	3	3	3
Hyb256-64_r6	48	24	12
Hyb256-64_r4	8	4	2
Hyb256-64_r2	48	24	12
64-QAM	12	6	3
Hyb64-16_r8	24	12	6
Hyb64-16_r6	2	1	1
Hyb64-16_r4	24	12	6
Hyb64-16_r2	12	6	3
16-QAM	8	4	2
Hyb16-4_r8	4	2	1
Hyb16-4_r6	8	4	2
Hyb16-4_r4	1	1	1
Hyb16-4_r2	8	4	2
4-QAM	4	2	1

[Fig. 57]

QAM mode \ FFT mode	8K	4K	2K
256-QAM	16	8	4
Hyb256-64_r8	12	12	12
Hyb256-64_r6	48	24	12
Hyb256-64_r4	8	4	4
Hyb256-64_r2	48	24	12
64-QAM	12	12	12
Hyb64-16_r8	24	12	12
Hyb64-16_r6	4	4	4
Hyb64-16_r4	24	12	12
Hyb64-16_r2	12	12	12
16-QAM	8	4	4
Hyb16-4_r8	4	4	4
Hyb16-4_r6	8	4	4
Hyb16-4_r4	4	4	4
Hyb16-4_r2	8	4	4
4-QAM	4	4	4

[Fig. 60]

Bit number	Purpose/Content
0	Initialization
1~16	Synchronization word
17~22	Length indicator
23, 24	Frame number
25, 26	constellation
27~29	Hierarchy information
30~32	Code rate, HP stream
33~35	Code rate, LP stream
36, 37	Guard interval
38, 39	Transmission mode
40~53	Reserved for future use
54~67	BCH, error protection

[Fig. 61]

S ₂₅ - S ₂₈	Constellation	Hybrid Ratio
0000	4QAM	4QAM 100%
0001	Hyb16-4_r2	4QAM 80%+16QAM 20%
0010	Hyb16-4_r4	4QAM 60%+16QAM 40%
0011	Hyb16-4_r6	4QAM 40%+16QAM 60%
0100	Hyb16-4_r8	4QAM 20%+16QAM 80%
0101	16-QAM	16-QAM 100%
0110	Hyb64-16_r2	16QAM 80%+64QAM 20%
0111	Hyb64-16_r4	16QAM 60%+64QAM 40%
1000	Hyb64-16_r6	16QAM 40%+64QAM 60%
1001	Hyb64-16_r8	16QAM 20%+64QAM 80%
1010	64-QAM	64-QAM 100%
1011	Hyb256-64_r2	64QAM 80%+256QAM 20%
1100	Hyb256-64_r4	64QAM 60%+256QAM 40%
1101	Hyb256-64_r6	64QAM 40%+256QAM 60%
1110	Hyb256-64_r8	64QAM 20%+256QAM 80%
1111	256-QAM	256-QAM 100%

[Fig. 62]

$S_{42} - S_{43}$	LDPC mode
00	64800
01	16200
10	reserved
11	reserved

[Fig. 63]

Bit number	Purpose/Content
0	Initialization
1~16	Synchronization word
17~22	Length indicator
23, 24	Frame number
25~28	constellation
29~31	Hierarchy information
32~34	Code rate, HP stream
35~37	Code rate, LP stream
38, 39	Guard interval
40, 41	Transmission mode
42, 43	LDPC mode
44~53	Reserved for future use
54~67	BCH, error protection

[Fig. 64]

$S_{44} - S_{48}$	OFDM block index
00000	Number 1
...	...
11111	Number 32

[Fig. 65]

Bit number	Purpose/Content
0	Initialization
1~16	Synchronization word
17~22	Length indicator
23, 24	Frame number
25~28	constellation
29~31	Hierarchy information
32~34	Code rate, HP stream
35~37	Code rate, LP stream
38, 39	Guard interval
40, 41	Transmission mode
42, 43	LDPC mode
44~48	OFDM symbol index
49~53	Reserved for future use
54~67	BCH, error protection

[Fig. 66]

$S_{49} - S_{52}$	Number of LDPC blocks
0000	1
0001	2
0010	3
0011	4
0100	6
0101	8
0110	12
0111	16
1000	24
1001	48
1010~1111	reserved

[Fig. 67]

$S_{53} - S_{57}$	Number of OFDM blocks
00000	Number 1
...	...
11111	Number 32

[Fig. 68]

Bit number	Purpose/Content
0	Initialization
1~16	Synchronization word
17~22	Length indicator
23, 24	Frame number
25~28	constellation
29~31	Hierarchy information
32~34	Code rate, HP stream
35~37	Code rate, LP stream
38, 39	Guard interval
40, 41	Transmission mode
42, 43	LDPC mode
44~48	OFDM symbol index
49~52	Number of LDPC blocks
53~57	Number of OFDM blocks
58~71	BCH, error protection

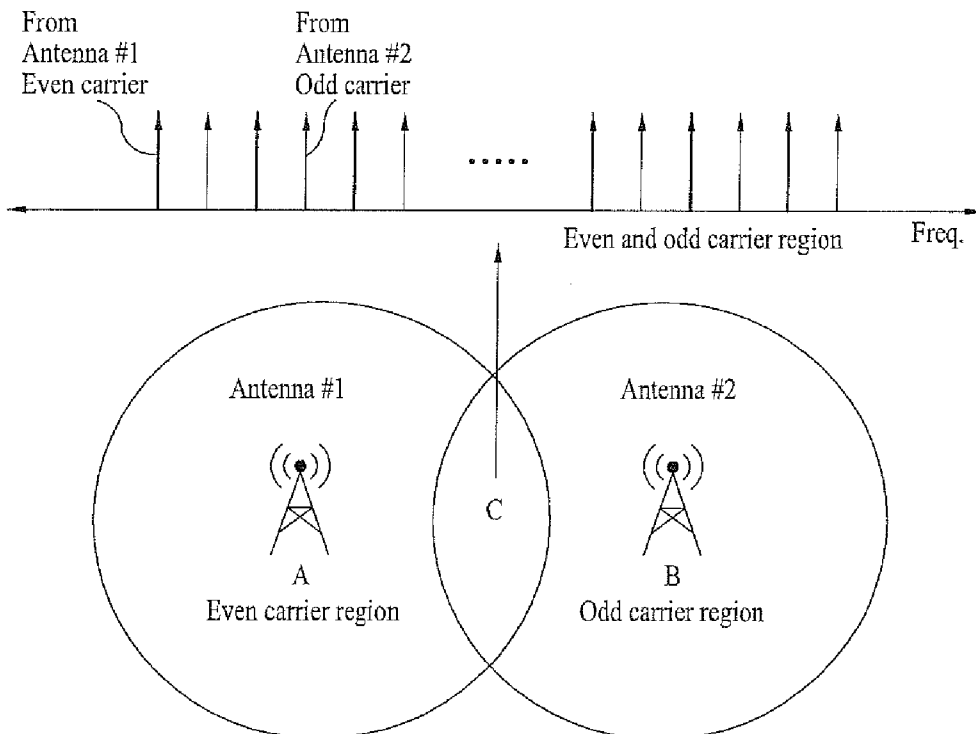
[Fig. 69]

$S_{58} - S_{59}$	Preamble duration
00	10 symbol
01	15 symbol
10	20 symbol
11	25 symbol

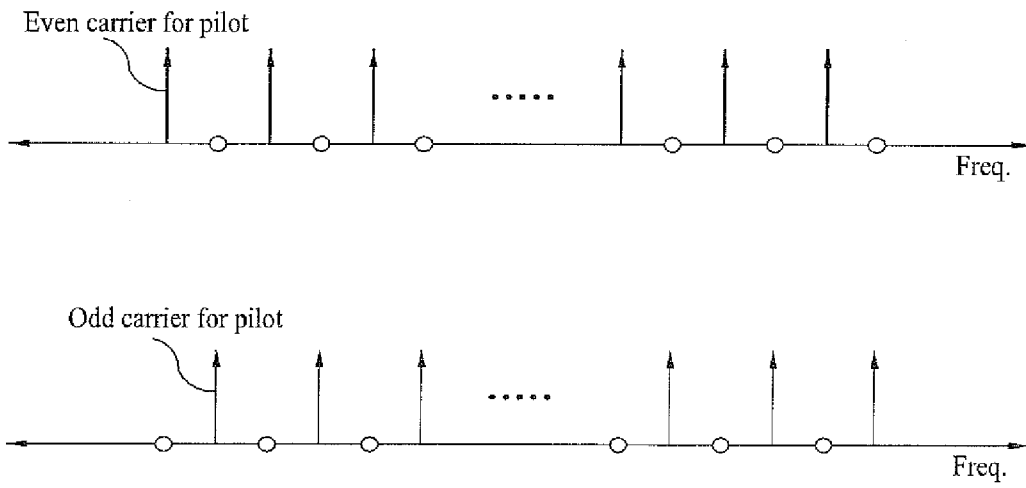
[Fig. 70]

Bit number	Purpose/Content
0	Initialization
1~16	Synchronization word
17~22	Length indicator
23, 24	Frame number
25~28	constellation
29~31	Hierarchy information
32~34	Code rate, HP stream
35~37	Code rate, LP stream
38, 39	Guard interval
40, 41	Transmission mode
42, 43	LDPC mode
44~48	OFDM symbol index
49~52	Number of LDPC blocks
53~57	Number of OFDM blocks
58~59	Preamble period
60~73	BCH, error protection

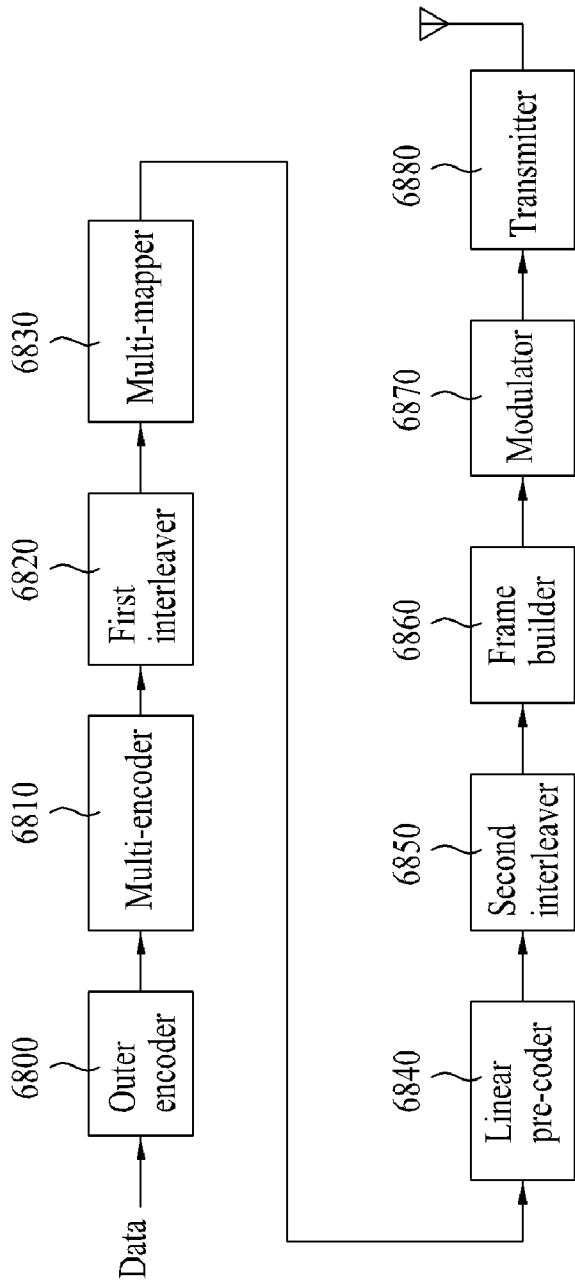
[Fig. 71]



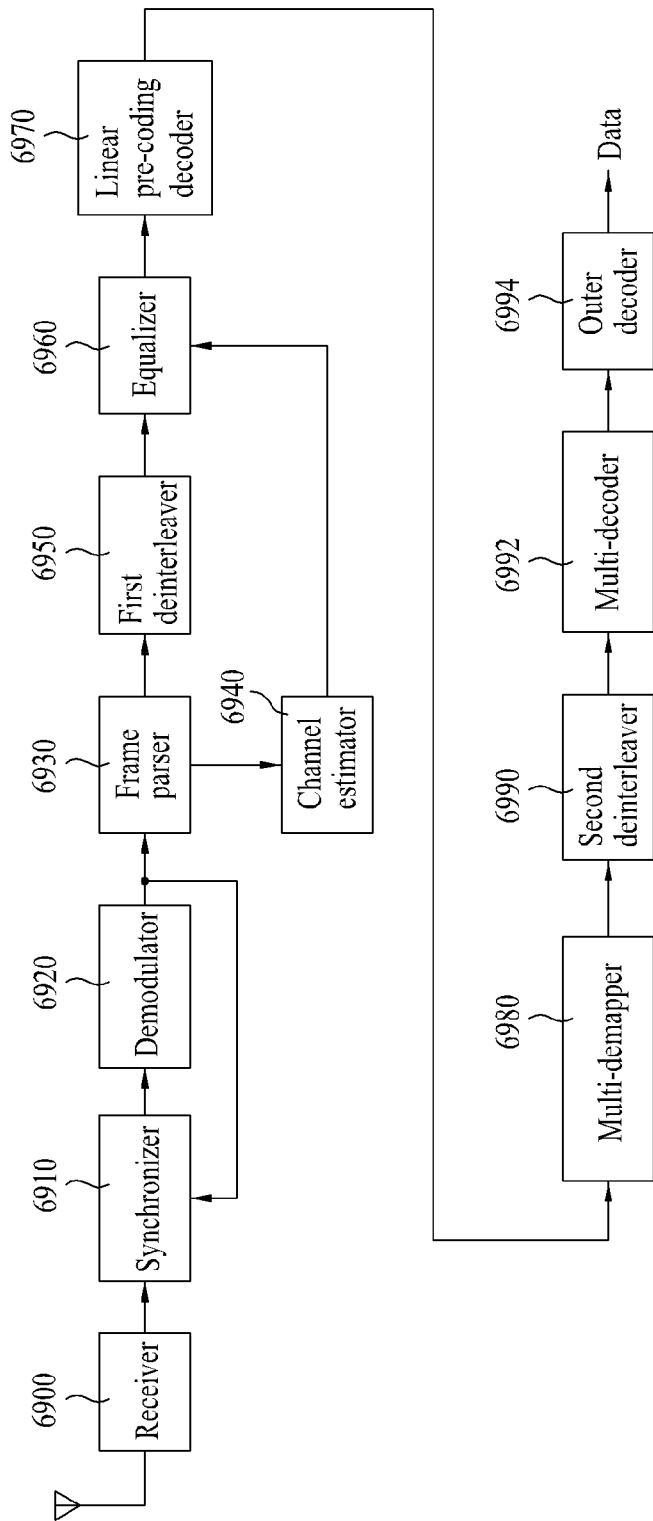
[Fig. 72]



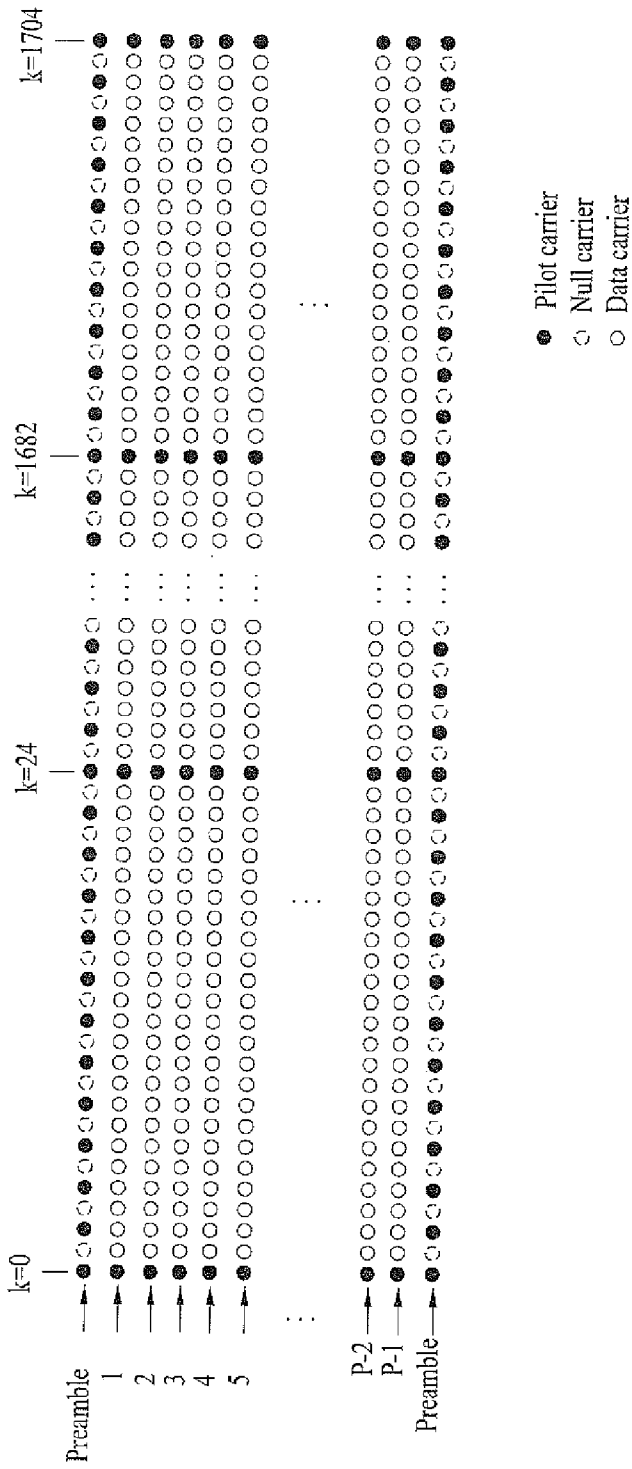
[Fig. 73]



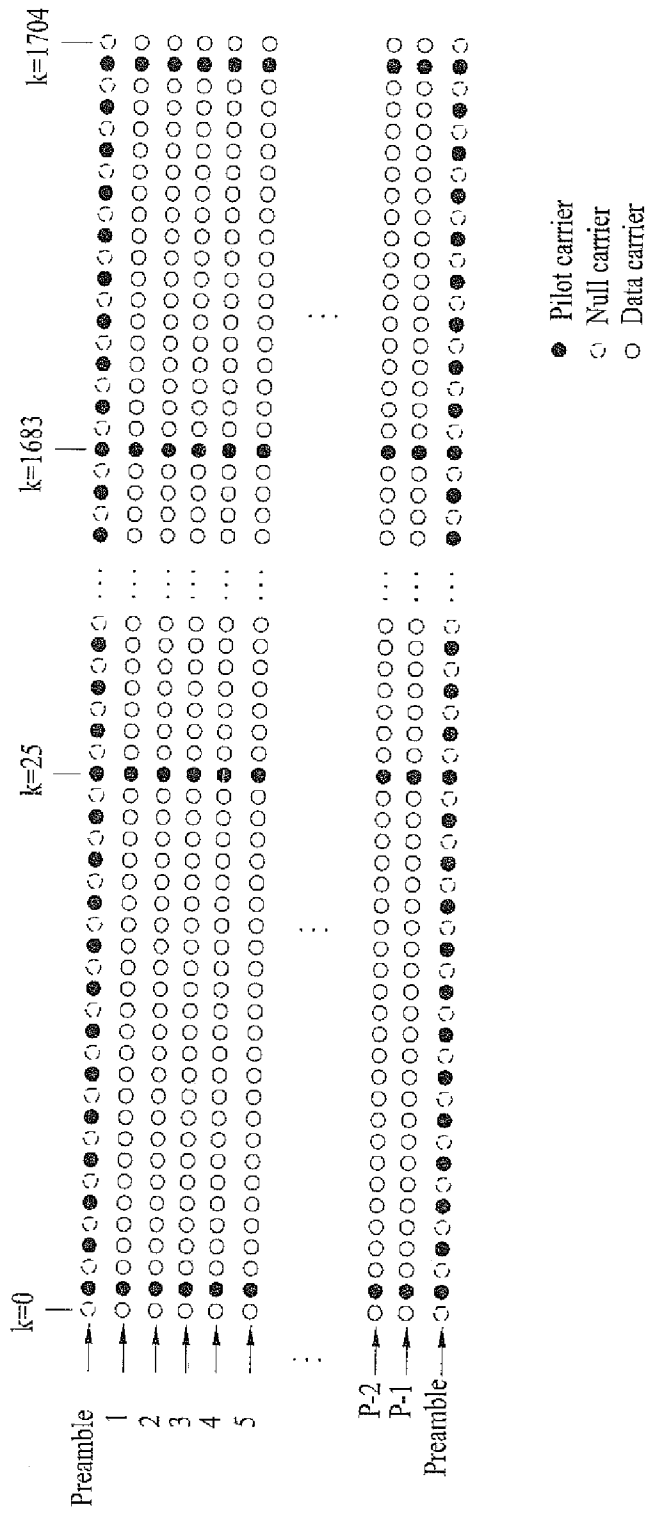
[Fig. 74]



[Fig. 75]



[Fig. 76]



[Fig. 77]

2K mode even continual pilot carrier positions (index number k)				
0	380	804	1106	1462
24	408	824	1110	1490
48	432	848	1136	1538
54	450	872	1140	1592
86	482	888	1146	1646
106	524	914	1186	1648
140	530	938	1206	1682
156	572	942	1260	1704
192	618	968	1268	
200	636	984	1300	
210	672	998	1322	
254	714	1002	1324	
278	758	1050	1376	
282	764	1072	1388	
332	780	1100	1438	

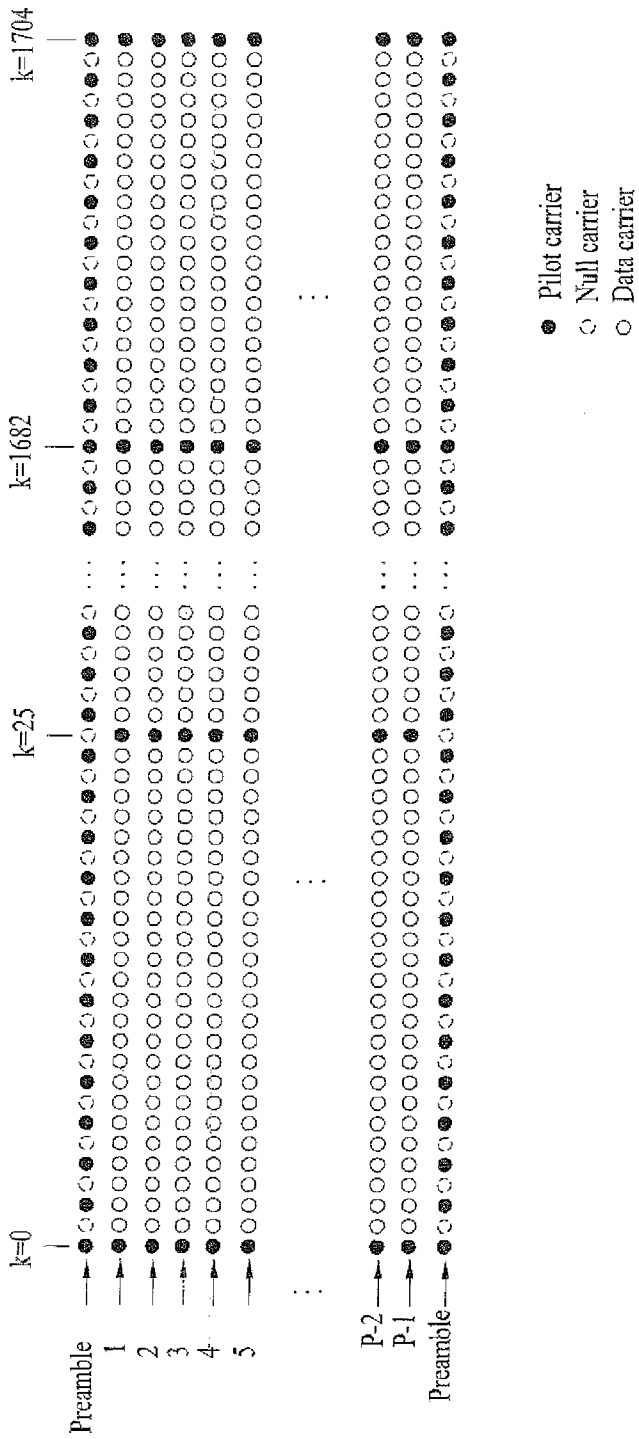
[Fig. 78]

4K mode even continual pilot carrier positions (index number k)								
0	380	804	1106	1462	1896	2322	2672	2972
24	408	824	1110	1490	1904	2340	2688	3004
48	432	848	1136	1538	1914	2376	2702	3026
54	450	872	1140	1592	1958	2418	2706	3028
86	482	888	1146	1646	1982	2462	2754	3080
106	524	914	1186	1648	1986	2468	2776	3092
140	530	938	1206	1682	2036	2484	2804	3142
156	572	942	1260	1704	2084	2508	2810	3166
192	618	968	1268	1728	2112	2528	2814	3194
200	636	984	1300	1752	2136	2552	2840	3242
210	672	998	1322	1758	2154	2576	2844	3296
254	714	1002	1324	1790	2186	2592	2850	3350
278	758	1050	1376	1810	2228	2622	2890	3352
282	764	1072	1388	1844	2234	2642	2910	3386
332	780	1100	1438	1860	2276	2646	2964	3408

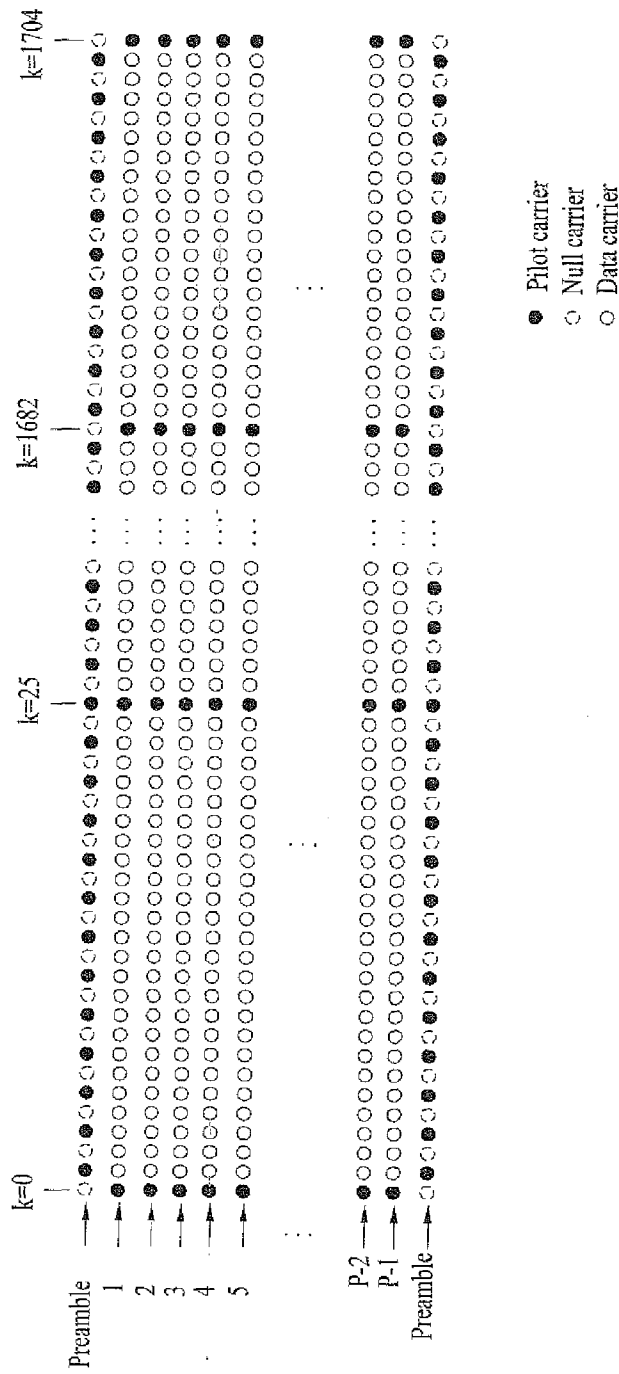
[Fig. 79]

8K mode even continual pilot carrier positions (index number k)								
0	380	804	1106	1462	1896	2322	2672	2972
24	408	824	1110	1490	1904	2340	2688	3004
48	432	848	1136	1538	1914	2376	2702	3026
54	450	872	1140	1592	1958	2418	2706	3028
86	482	888	1146	1646	1982	2462	2754	3080
106	524	918	1186	1648	1986	2468	2776	3092
140	530	938	1206	1682	2036	2484	2804	3142
156	572	942	1260	1704	2084	2508	2810	3166
192	618	968	1268	1728	2112	2528	2814	3194
200	636	984	1300	1752	2136	2552	2840	3242
210	672	998	1322	1758	2154	2576	2844	3296
254	714	1002	1324	1790	2186	2592	2850	3350
278	758	1050	1376	1810	2228	2622	2890	3352
282	764	1072	1388	1844	2234	2642	2910	3386
332	780	1100	1438	1860	2276	2646	2964	3408
3432	3816	4232	4518	4898	5312	5748	6096	6412
3456	3840	4256	4544	4946	5322	5784	6110	6434
3462	3858	4280	4548	5000	5366	5826	6114	6436
3494	3890	4296	4554	5054	5390	5870	6162	6488
3514	3932	4326	4594	5056	5394	5876	6184	6500
3548	3938	4346	4614	5090	5444	5892	6212	6550
3564	3980	4350	4668	5112	5492	5916	6218	6574
3600	4026	4376	4676	5136	5520	5936	6222	6602
3608	4044	4392	4708	5160	5544	5960	6248	6650
3618	4080	4406	4730	5166	5562	5984	6252	6704
3662	4122	4410	4732	5198	5594	6000	6258	6758
3686	4166	4458	4784	5218	5636	6030	6298	6760
3690	4172	4480	4796	5252	5642	6050	6318	6794
3740	4188	4508	4846	5268	5684	6054	6372	6816
3788	4212	4514	4870	5304	5730	6080	6380	

[Fig. 80]



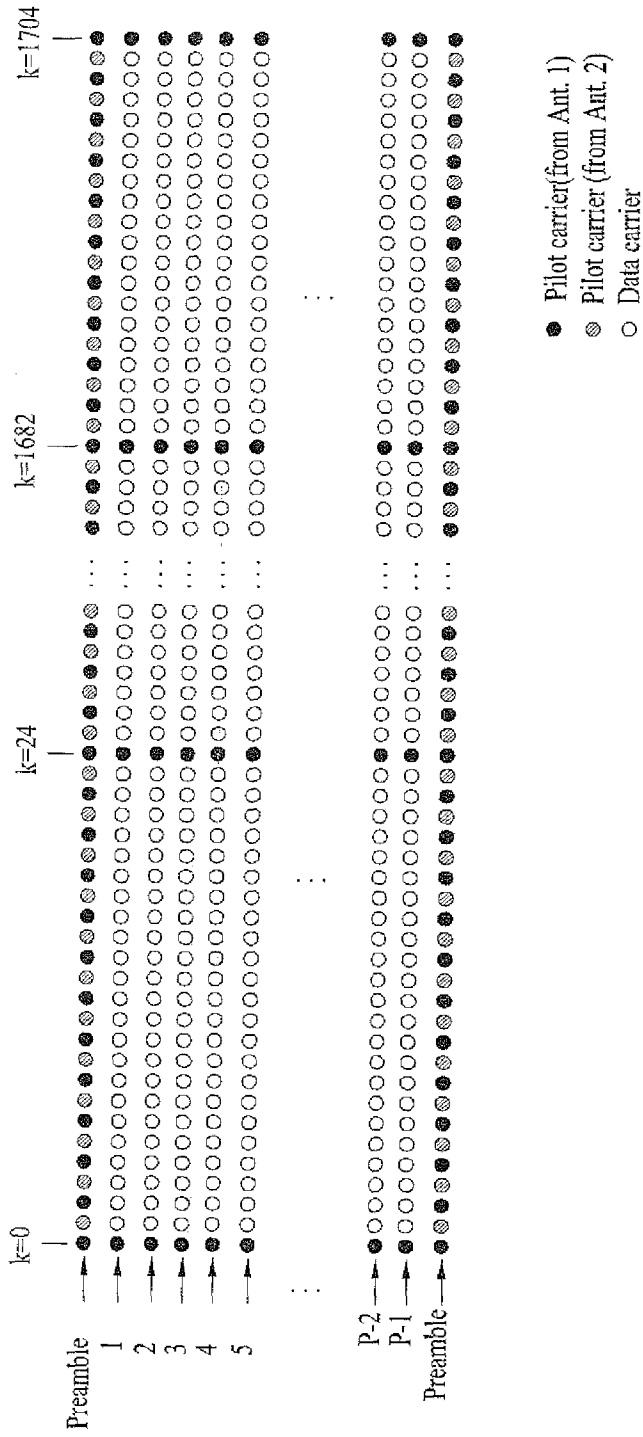
[Fig. 81]



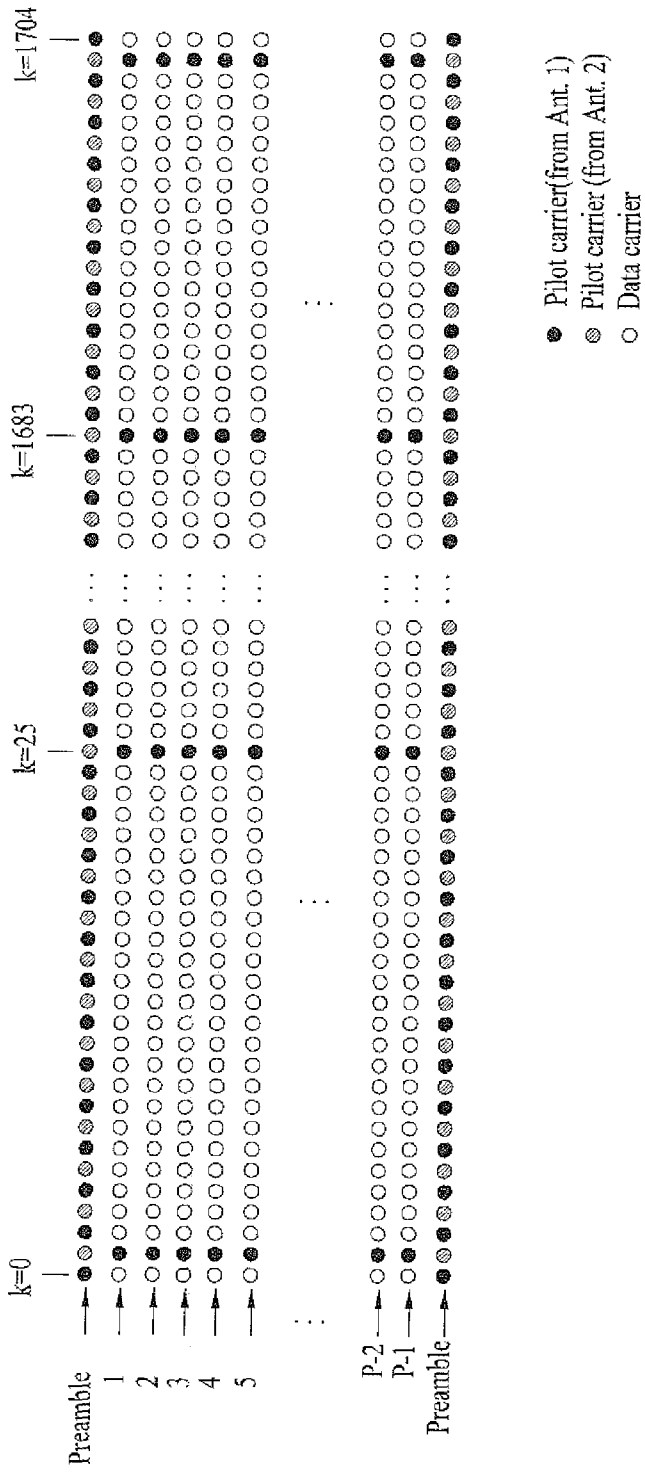
[Fig. 82]

2k mode common continual pilot				
0	381	804	1107	1462
25	408	825	1110	1491
48	433	848	1137	1538
55	450	873	1140	1593
86	483	888	1147	1646
107	524	919	1186	1649
140	531	938	1207	1682
157	572	943	1260	1704
192	619	968	1269	
201	636	985	1300	
210	673	998	1323	
255	714	1003	1324	
278	759	1050	1377	
283	764	1073	1388	
332	781	1100	1439	

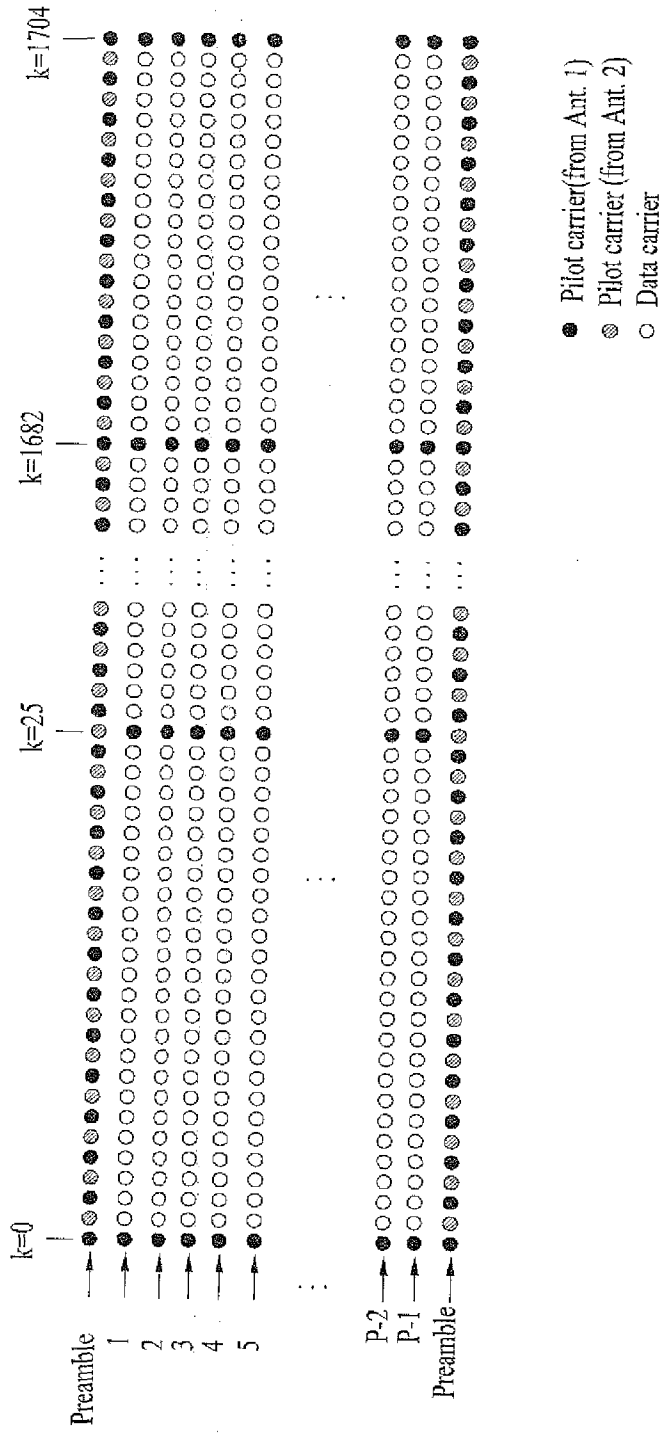
[Fig. 83]



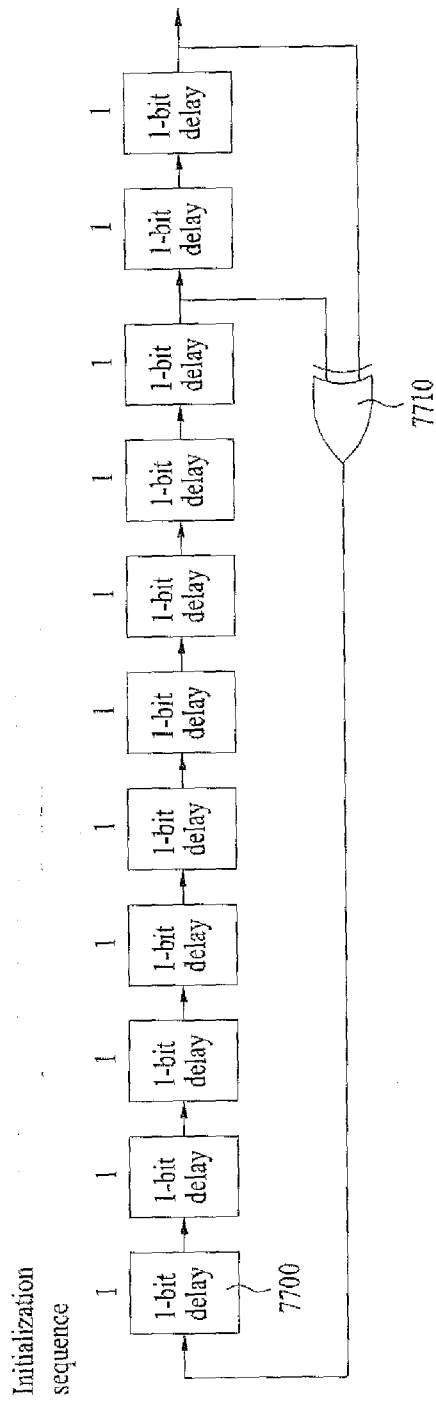
[Fig. 84]



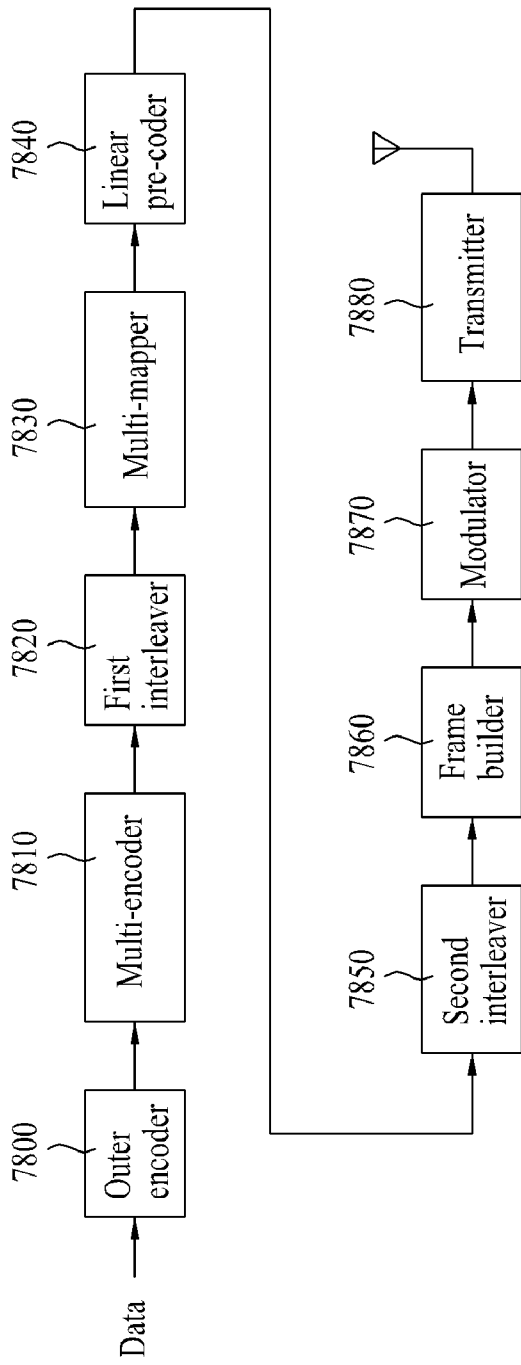
[Fig. 85]



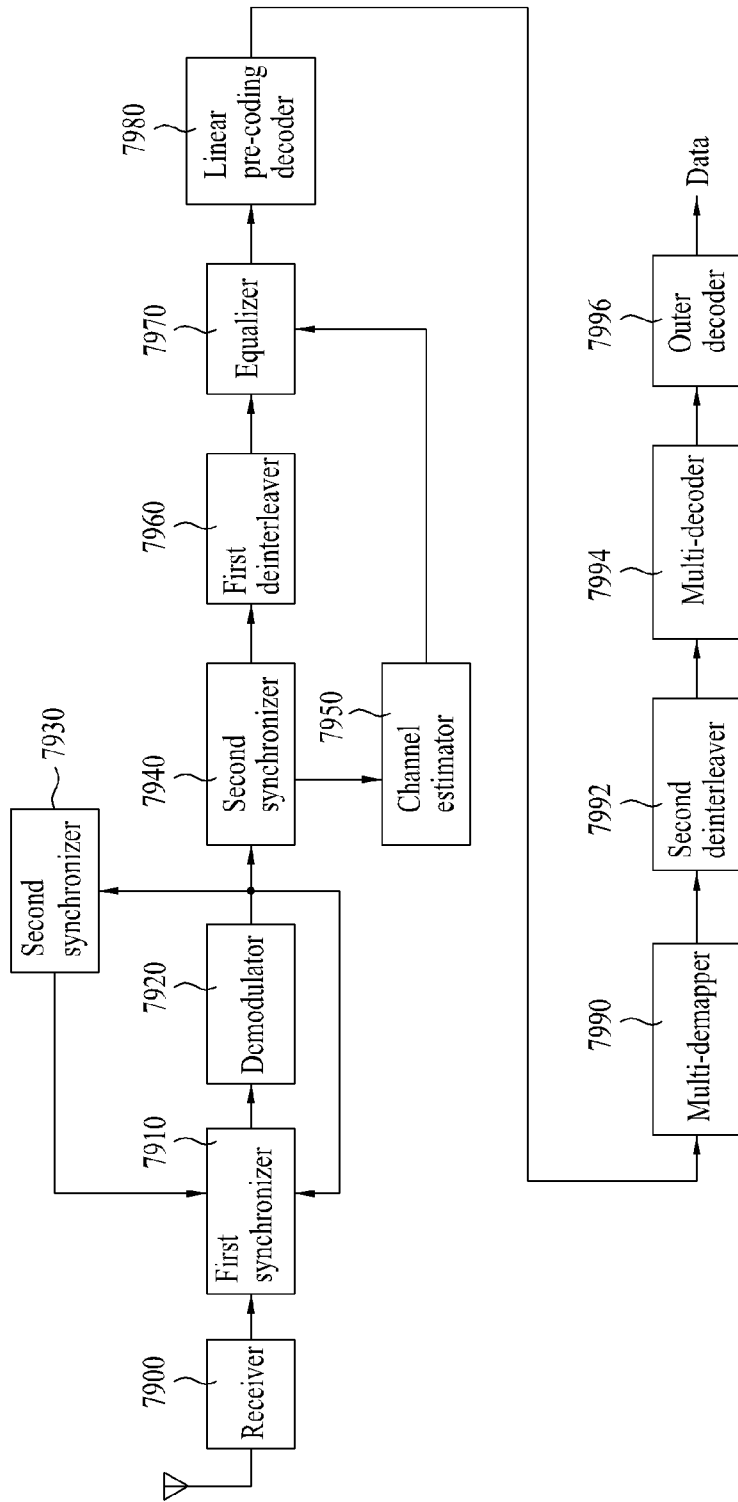
[Fig. 86]



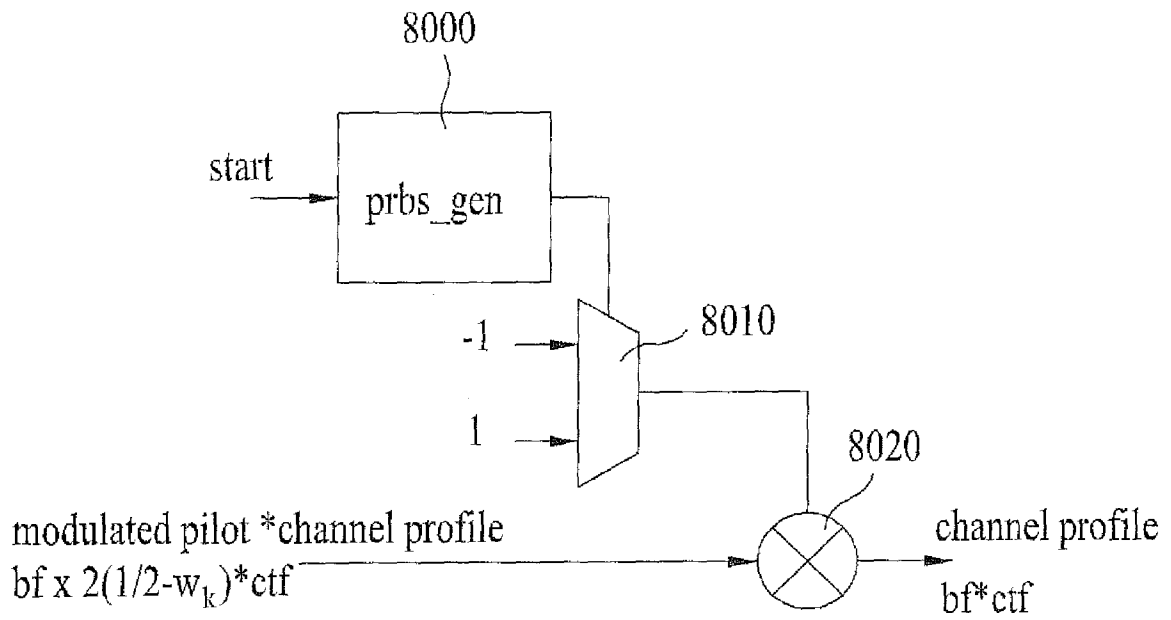
[Fig. 87]



[Fig. 88]



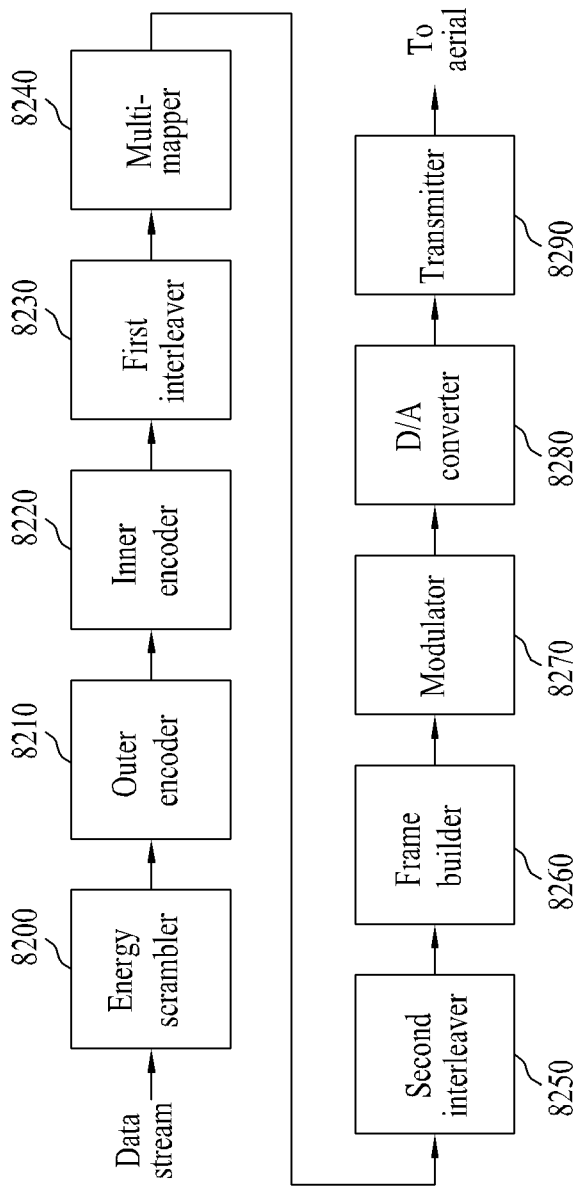
[Fig. 89]



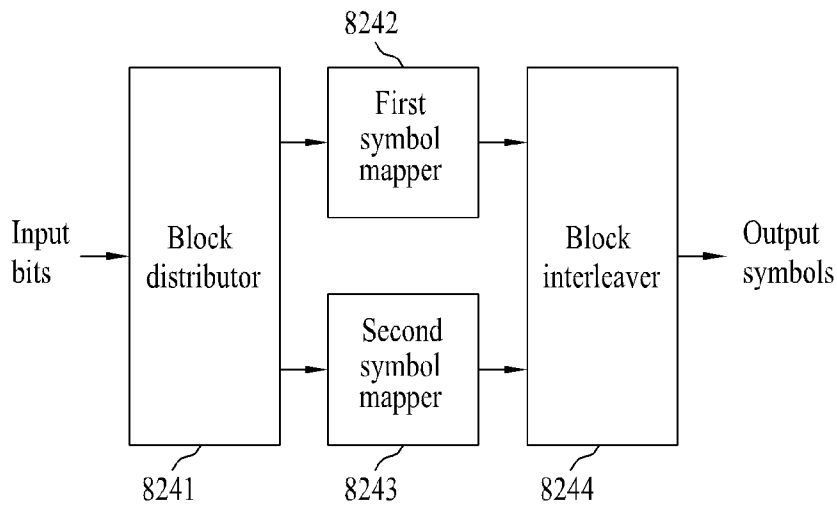
[Fig. 90]

TPS bit per symbol	For TPS sync (symbol)	For LDPC sync (symbol)	Total symbol	Time (sec) (symbol)
1	72	19	162	0.1452
2	36	19	90	0.0806

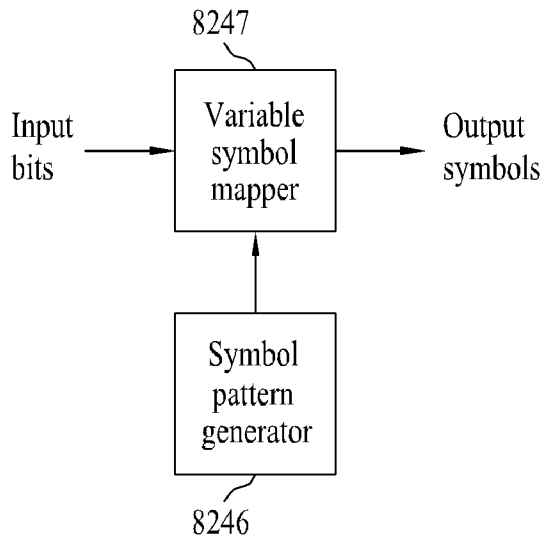
[Fig. 91]



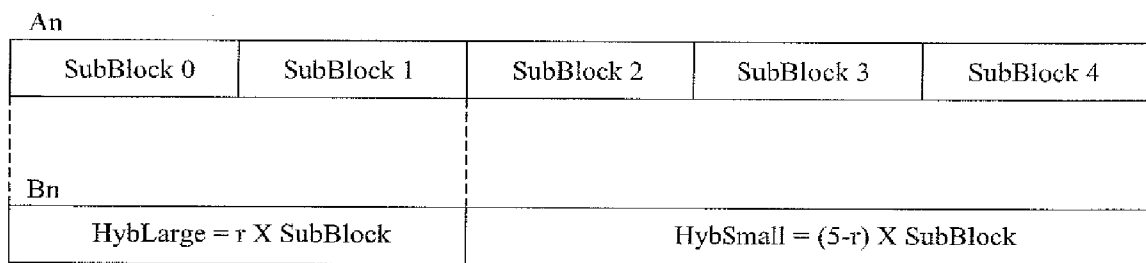
[Fig. 92]



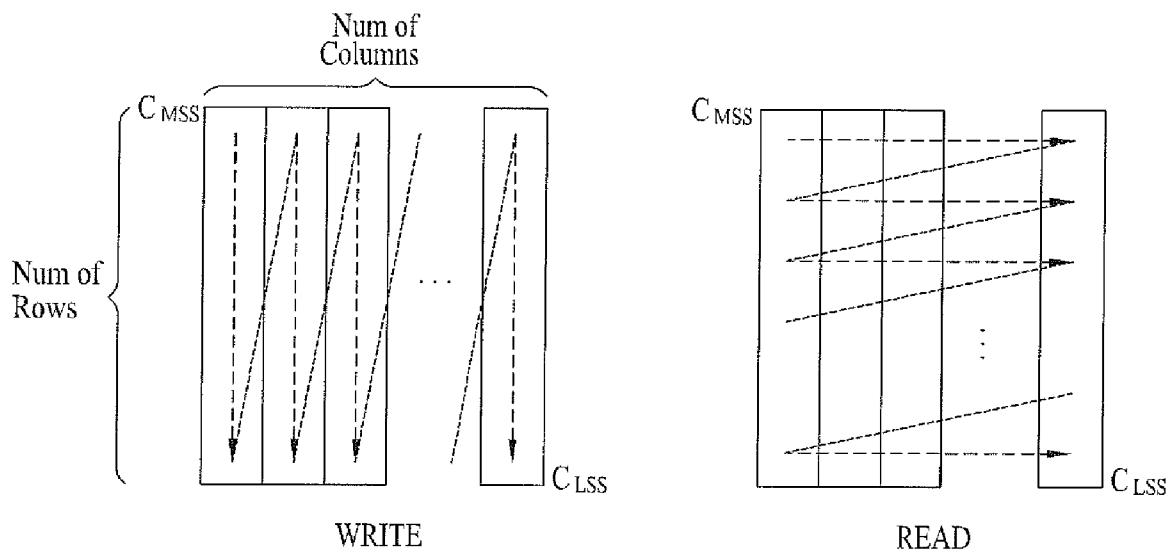
[Fig. 93]



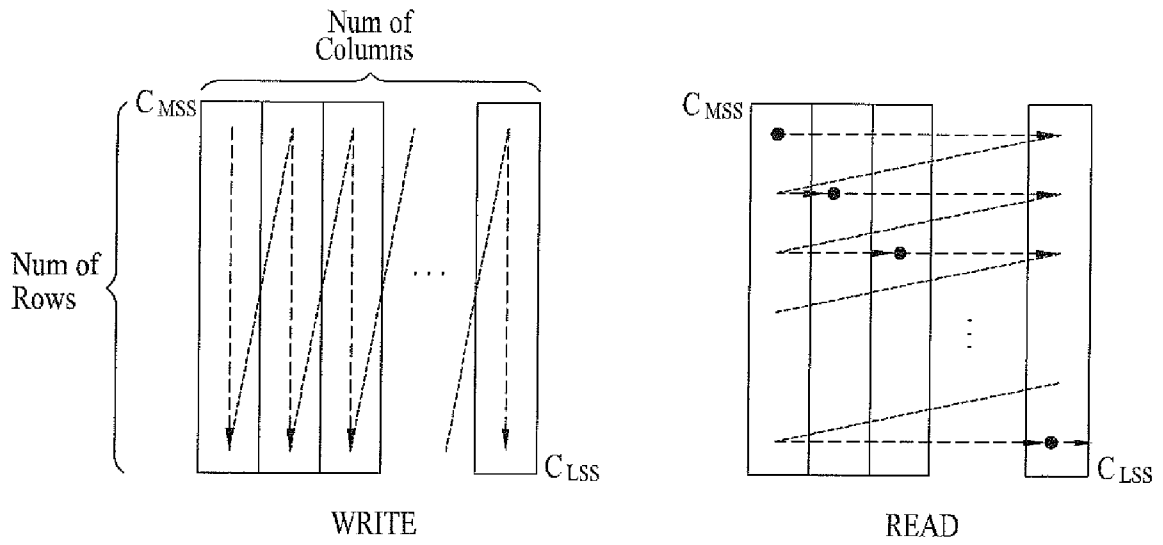
[Fig. 94]



[Fig. 95]



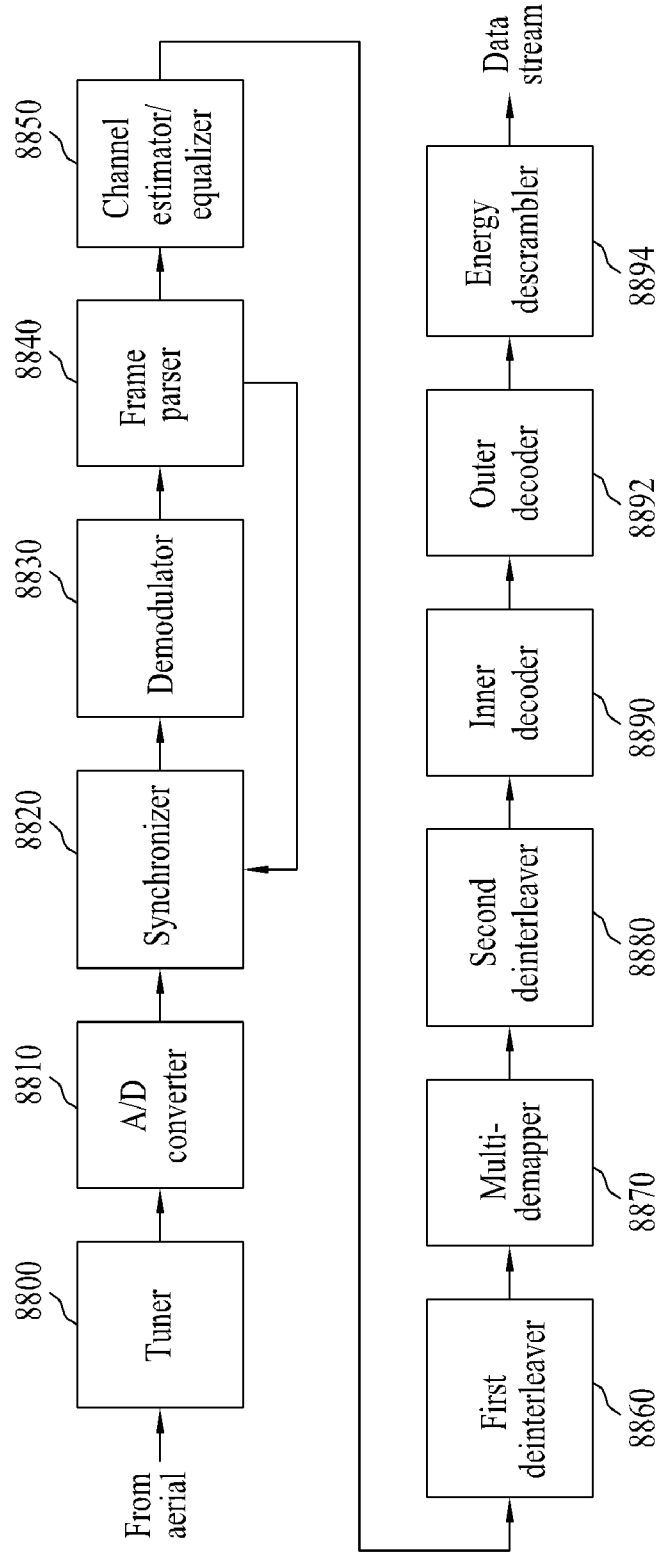
[Fig. 96]



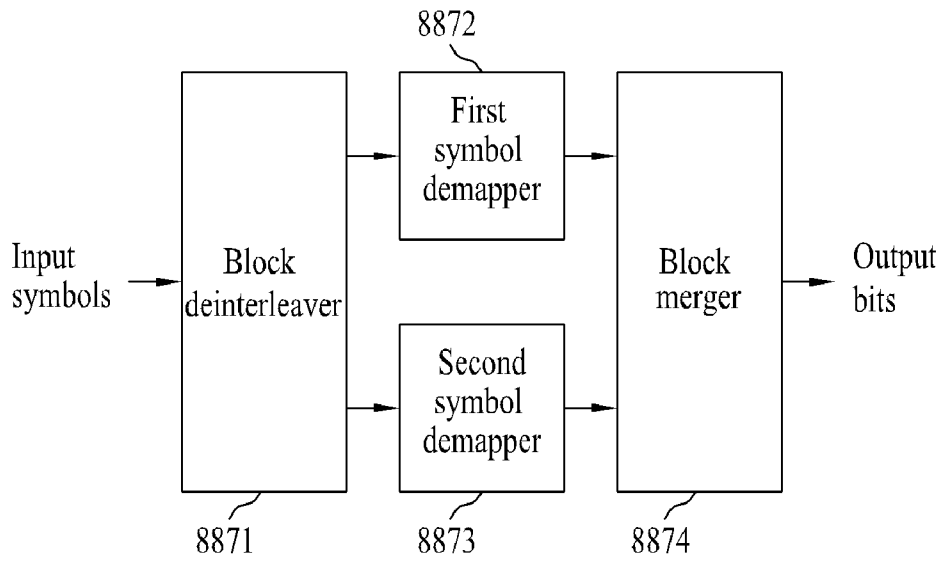
[Fig. 97]

Modulation Mode	Num of Columns
256-QAM	15
Hyb256-64_r8	16
Hyb256-64_r6	17
Hyb256-64_r4	18
Hyb256-64_r2	19
64-QAM	20
Hyb64-16_r8	22
Hyb64-16_r6	24
Hyb64-16_r4	26
Hyb64-16_r2	28
16-QAM	30
Hyb16-4_r8	36
Hyb16-4_r6	42
Hyb16-4_r4	48
Hyb16-4_r2	54
4-QAM	60

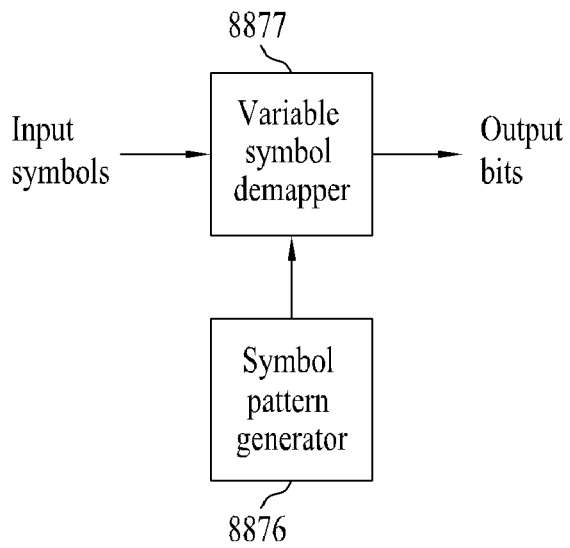
[Fig. 98]



[Fig. 99]

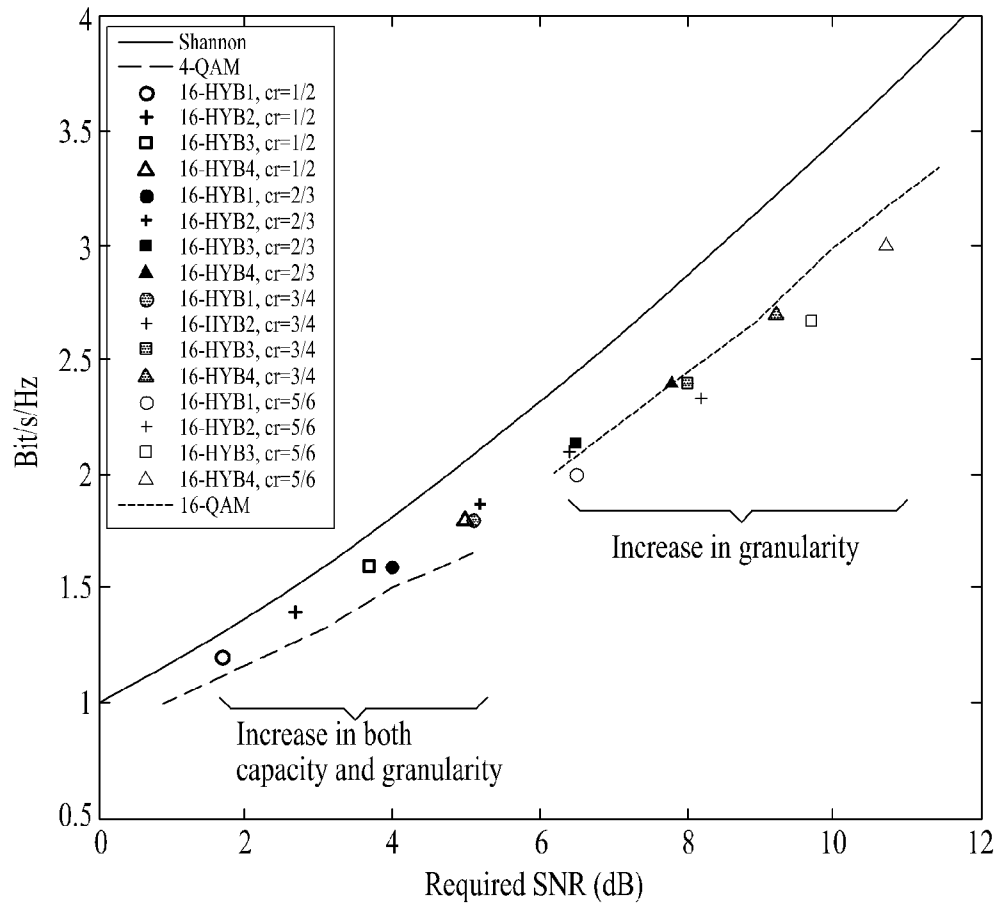


[Fig. 100]

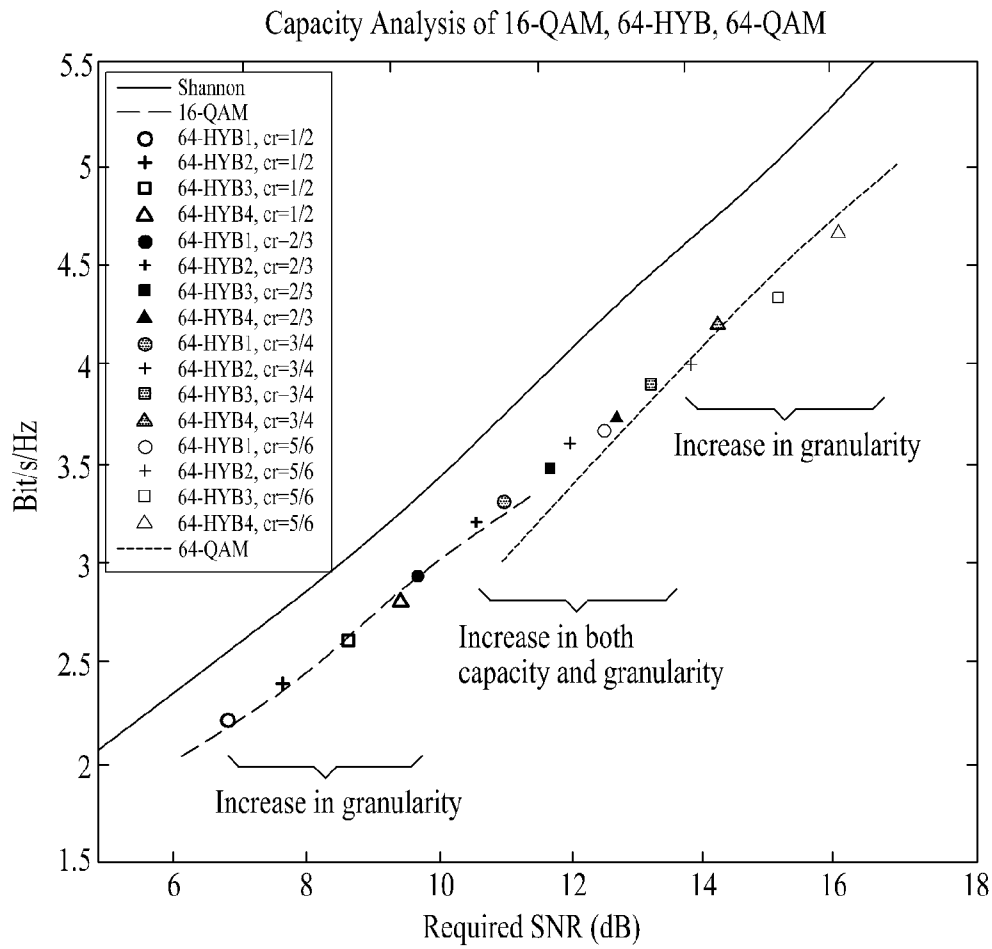


[Fig. 101]

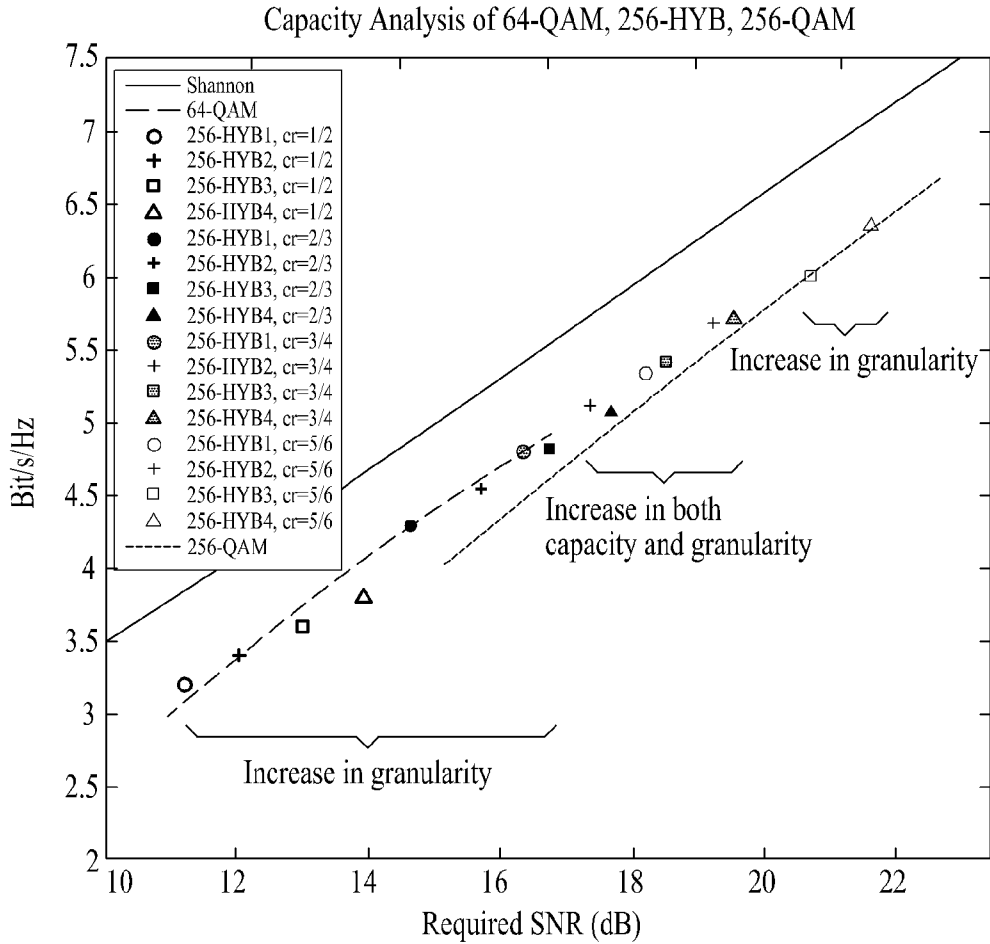
Capacity Analysis of 4-QAM, 16-HYB, 16-QAM



[Fig. 102]



[Fig. 103]



[Fig. 104]

FFT mode \ Bandwidth	8K	4K	2K
8 MHz	5.60	5.60	5.60
7 MHz	6.40	6.40	6.40
6 MHz	7.47	7.47	7.47

[Fig. 105]

FFT mode \ Bandwidth	8K	4K	2K
8 MHz	157.92	81.75	43.68
7 MHz	180.48	93.44	49.92
6 MHz	210.56	109.01	58.23

[Fig. 106]

FFT mode Bandwidth	8K	4K	2K
8 MHz	21.28	10.64	7.84
7 MHz	24.32	12.16	8.96
6 MHz	28.37	14.19	10.45

[Fig. 107]

FFT mode Bandwidth	8K	4K	2K
8 MHz	173.60	86.80	45.92
7 MHz	198.40	99.20	52.48
6 MHz	231.46	115.73	61.22

[Fig. 108]

Aspect	DVB-T	Proposed	enhancement (dB)
Power	1.778	2.000	0.512
Power + density	0.593	1.000	2.272

[Fig. 109]

mode	# of CP		enhancement (dB)
	DVB-T	Proposed	
2K	45	68	1.793
4K	89	135	1.809
8K	177	269	1.818

[Fig. 110]

mode	Avg. power of data carrier		enhancement (dB)
	DVB-T	Proposed	
2K	0.910	0.968	0.267
4K	0.910	0.968	0.266
8K	0.911	0.968	0.265

[Fig. 111]

mode	DVB-T (%)	Proposed (%)	Difference (%)
2K	10.381	8.789	1.592
4K	10.326	8.762	1.564
8K	10.298	8.749	1.549

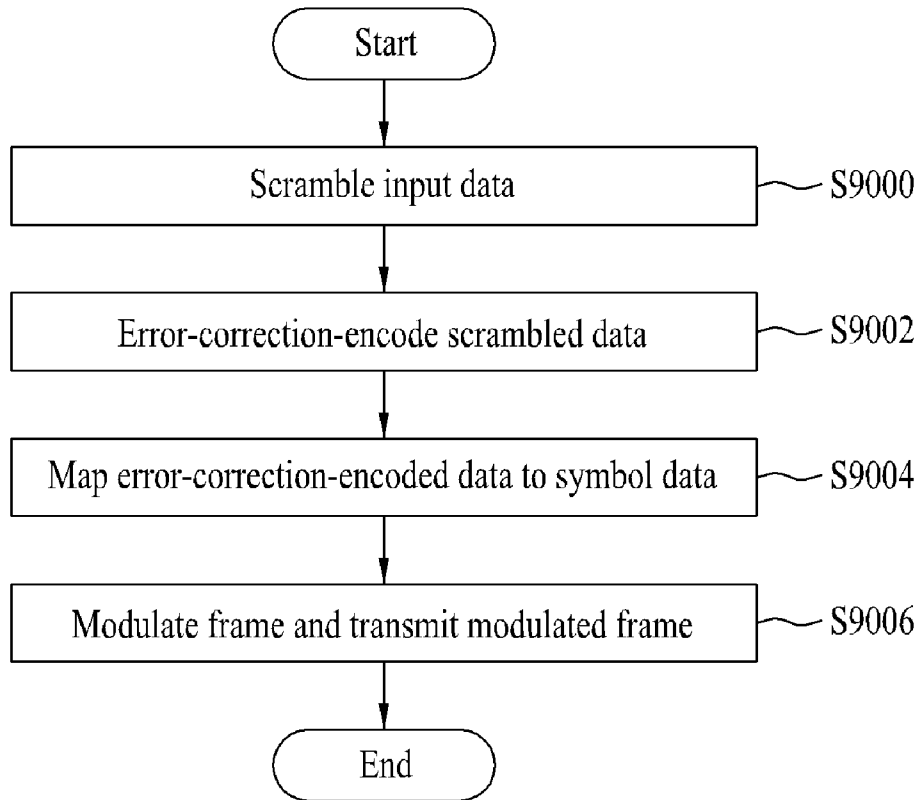
[Fig. 112]

Preamble period	GI mode			
	1/4	1/8	1/16	1/32
10	178.57	198.41	210.08	216.45
15	119.05	132.28	140.06	144.30
20	89.29	99.21	105.04	108.23
25	71.43	79.37	84.03	86.58

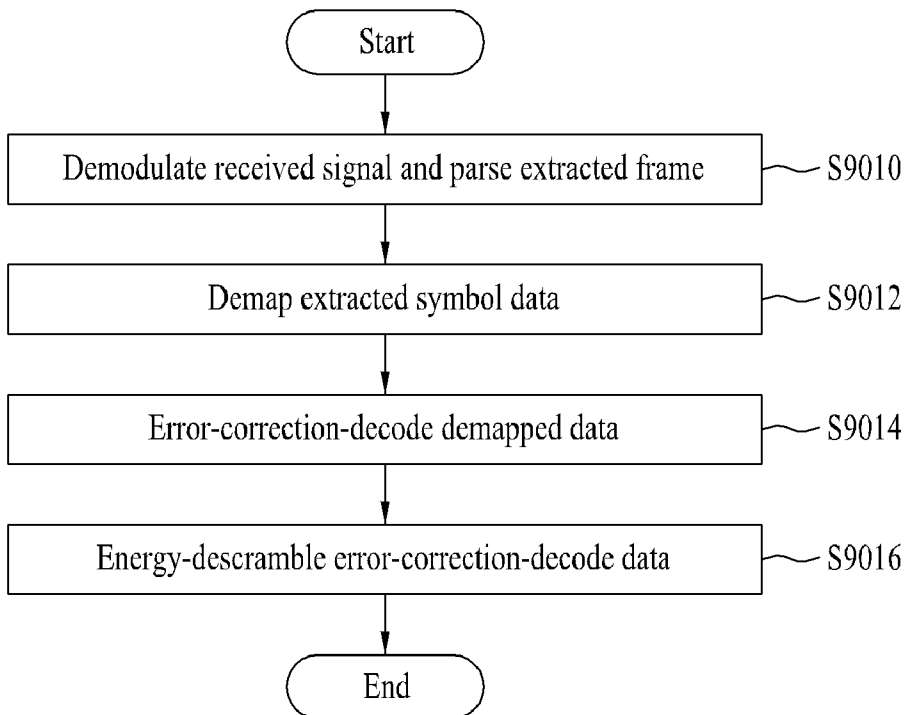
[Fig. 113]

Preamble period	GI mode			
	1/4	1/8	1/16	1/32
10	44.64	49.60	52.52	54.11
15	29.76	33.07	35.01	36.08
20	22.32	24.80	26.26	27.06
25	17.86	19.84	21.01	21.65

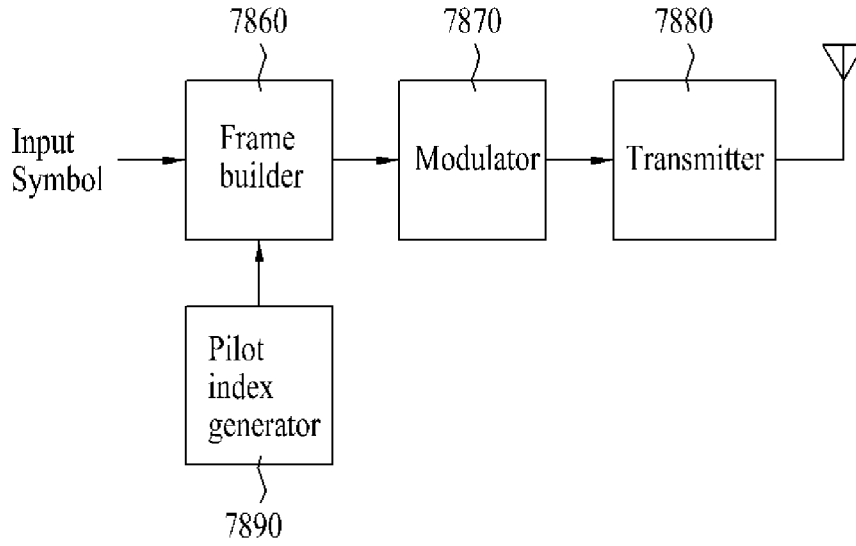
[Fig. 114]



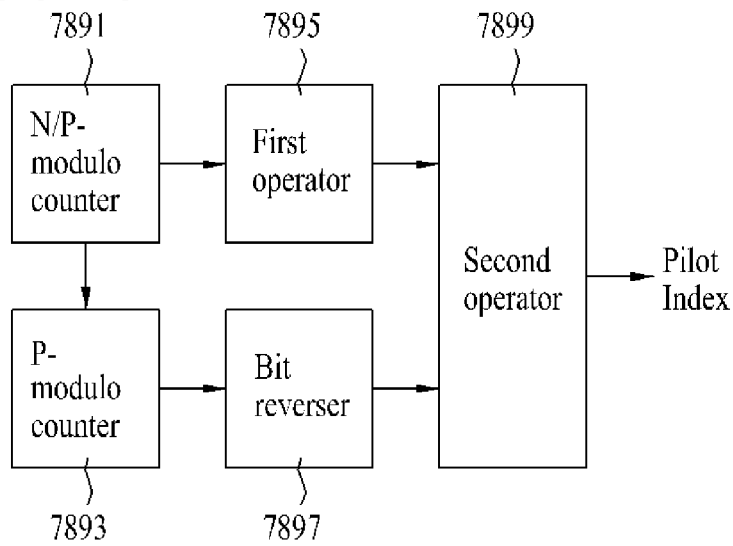
[Fig. 115]



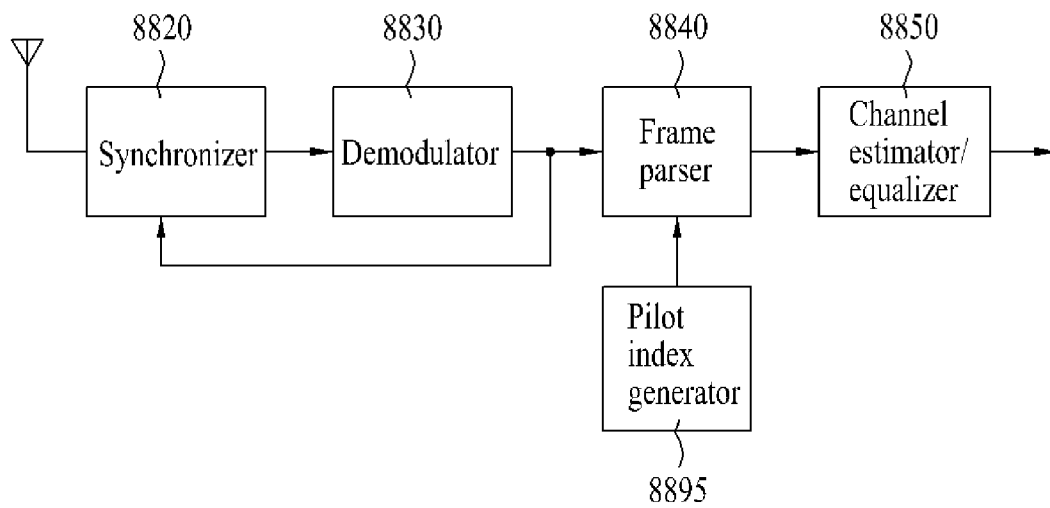
[Fig. 120]



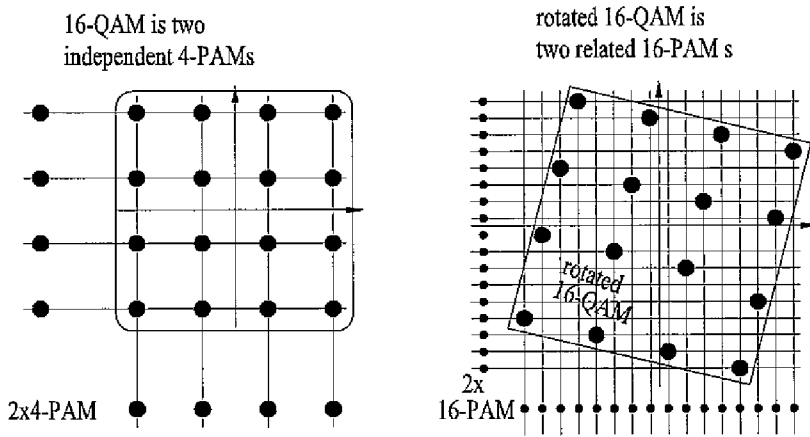
[Fig. 121]



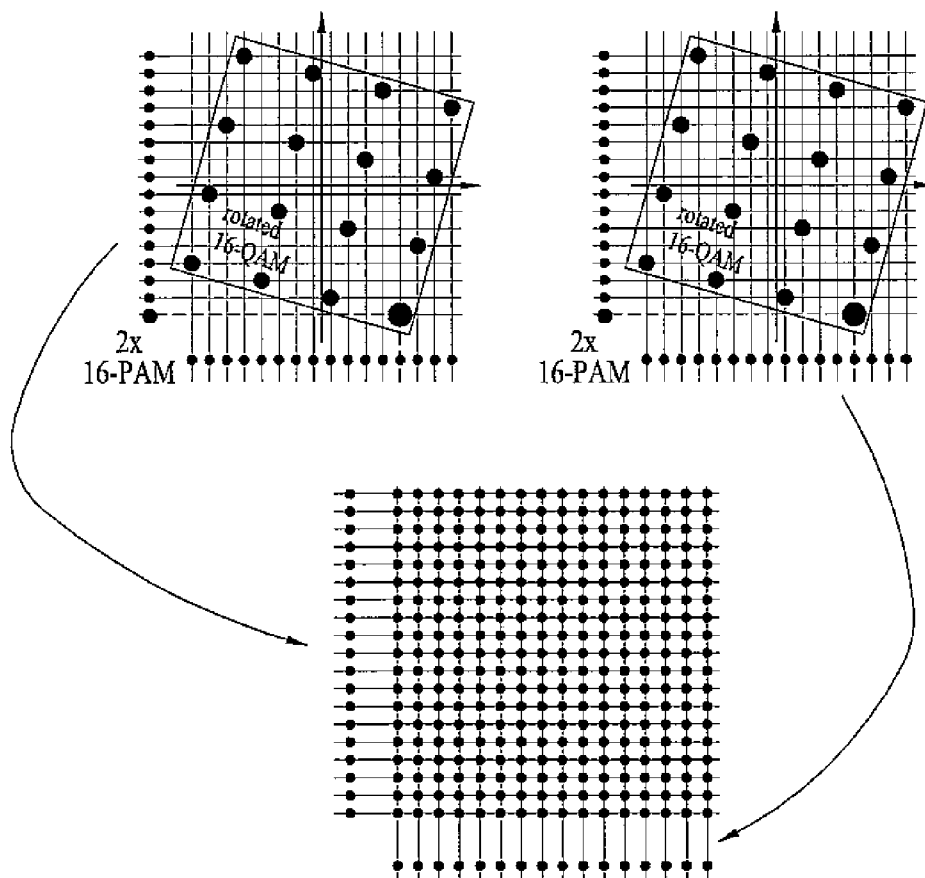
[Fig. 122]



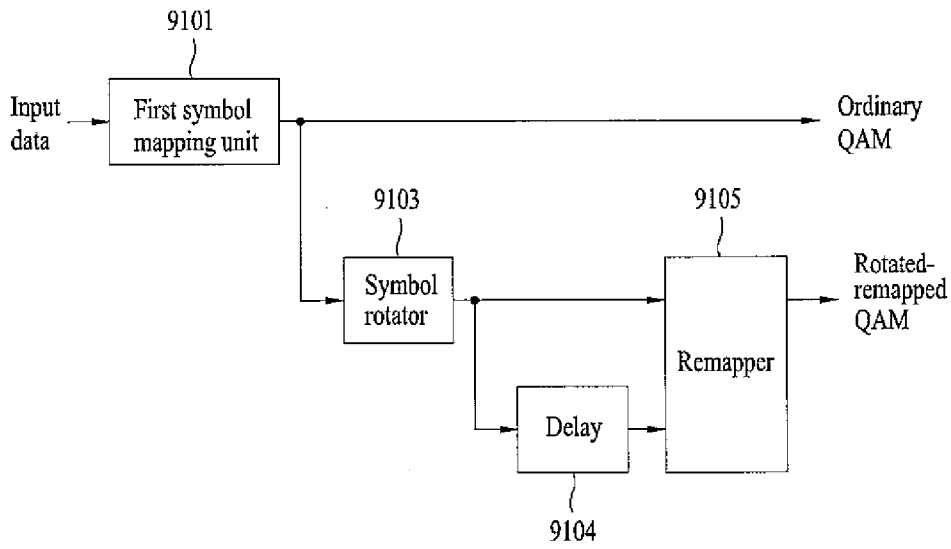
[Fig. 123]



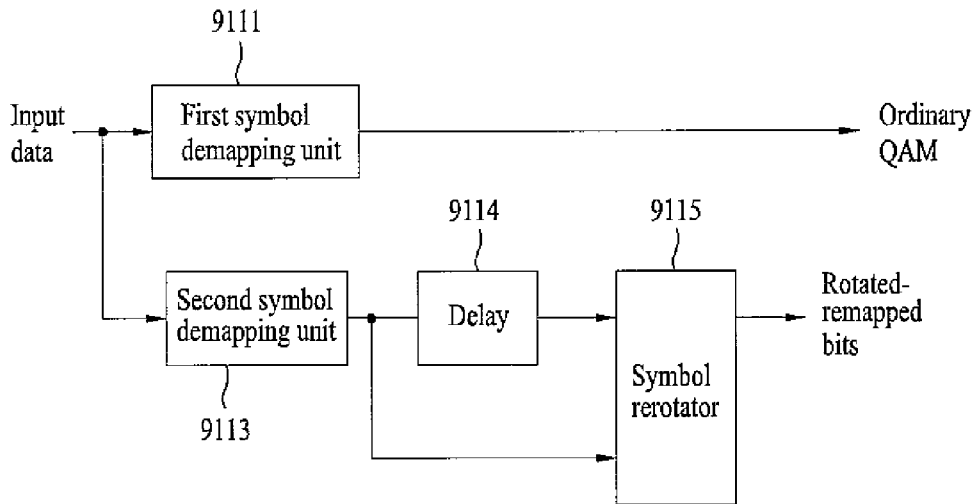
[Fig. 124]



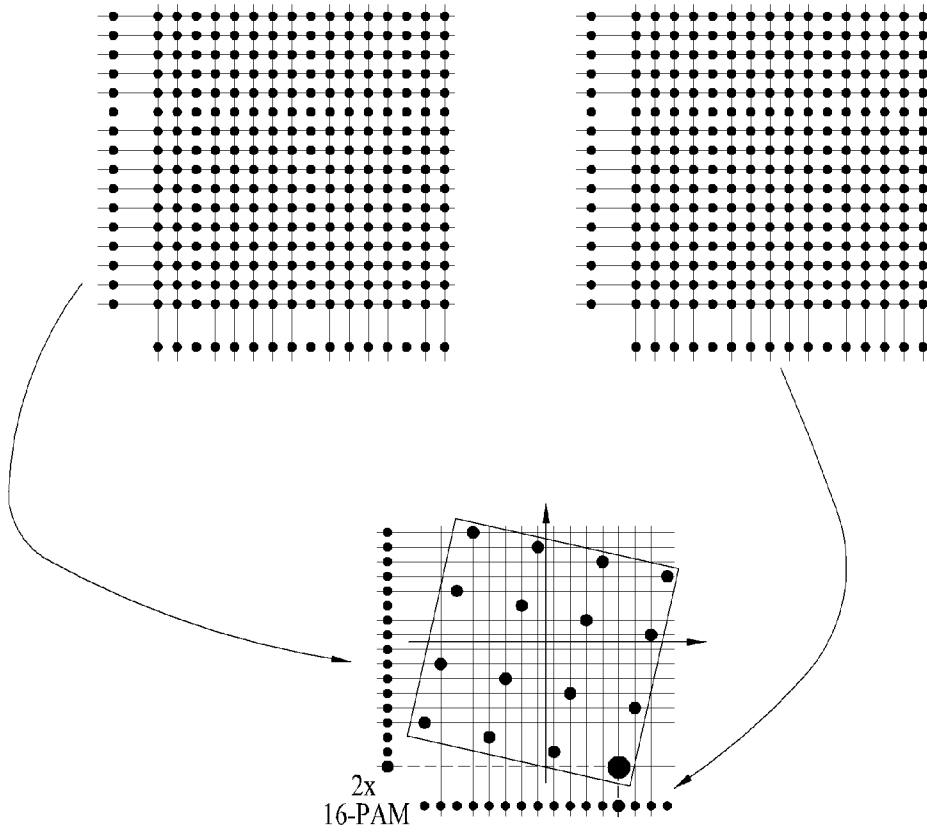
[Fig. 125]



[Fig. 126]

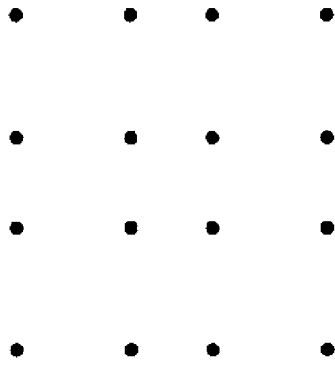


[Fig. 127]

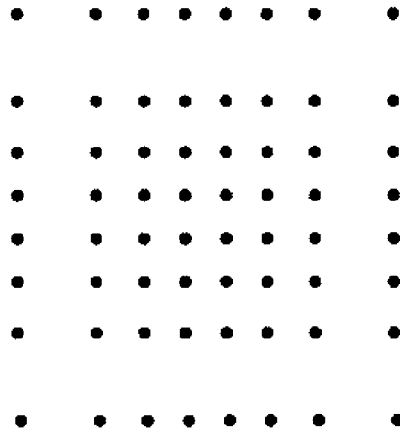


[Fig. 128]

Non-uniform
16-QAM



Non-uniform
64-QAM



Non-uniform
256-QAM

