PATENT SPECIFICATION

(11) 1 585 790

(21) Application No. 30010/77 (22) Filed 18 July 1977
(31) Convention Application No. 706 355 (32) Filed 19 July 1976 in
(33) United States of America (US)
(44) Complete Specification published 11 March 1981
(51) INT. CL.^{3} H01L 29/743
(52) Index of acceptance
H1K 1AB9 4C14 4C14A 4C1M 4C2A ABX

(19)

1 585 790

(54) HIGH VOLTAGE THYRISTOR

(71) We, WESTINGHOUSE ELECTRIC CORPORATION of Westinghouse Building, Gateway Center, Pittsburgh, Pennsylvania, United States of America, a company organised and existing under the laws of the Commonwealth of Pennsylvania, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates generally to semiconductor devices and more particularly to high voltage thyristors.

It is known that the blocking capability of a PN junction depends on both the bulk properties and the surface properties of the semiconductor body. Surface breakdown has been the principle voltage limiting factor in prior art devices.

A prior art thyristor 10 as shown in Figure 1 comprises a body of semiconductor material 12 on which electrodes 14, 16 and 18 are disposed. The wafer 12 comprises four zones of alternate conductivity type: an N-type cathode emitter zone 20 disposed at the top major surface 21 of the wafer 12, a P-type cathode base zone 22 disposed below zone 20, an N-type anode base zone 24 disposed below zone 22, and a P-type anode emitter zone 26 disposed below zone 24. Cathode electrode 14 is affixed to top major surface 21 contacting zone 20. Anode electrode 18 is affixed to bottom major surface 27 of the wafer 12 thereby contacting zone 26.

The device 10 has a beveled edge 28 produced in a known manner for the purpose of increasing surface breakdown capability. As will be appreciated by those skilled in the art, beveled edge 28 increases the blocking capability of PN junctions 31 and 33 which terminate on surface 28.

Referring now to Figure 2 there is illustrated a prior art diode 40 which achieves field spreading of the electric field around a single blocking PN junction at its intersection with a flat major semiconductor surface. Diode 40 comprises a semiconductor wafer 42, a field spreading member 44, top electrode 46 and bottom electrode 48. Disposed in the wafer 42 is an N-type zone 52 adjacent to top major surface 51, and a P-type zone 54 adjacent to bottom major surface 55. PN junction 57 interfaces N-type zone 52 and P-type zone 54. Electrode 48 is affixed to bottom major surface 55 contacting zone 54. Zone 54 extends past zone 52 to the outer periphery of major surface 51, so that PN junction 57 intersects top major surface 51. Field spreader 44 is disposed on major surface 51 covering PN junction 57.

The principal object of the invention is to provide a thyristor with higher breakdown voltage than prior art devices.

The invention resides broadly in a thyristor comprising: a semiconductor body having a cathode emitter disposed in said body along a first major surface; a cathode base extending around said cathode emitter to said first surface; an anode base extending around said cathode base to said first surface; an anode emitter extending around said anode base to said first surface and bordering a second major surface of said body; and an electric field spreader comprising a resistive path making an electrical connection between the anode emitter and the cathode base disposed on said first major surface for spreading a blocking mode field.

A preferred embodiment of the invention will now be described, by way of example only, with respect to the accompanying drawings, in which:

Figure 1 is a cross sectional view of a thyristor device of the prior art;

Figure 2 is a cross sectional view of a prior art diode employing a field spreader;

Figure 3 is a cross sectional view of a thyristor device employing field spreaders;

Figure 4 is a cross sectional view of a thyristor device; and

Figure 5 is one possible plan view of the device of Figure 4.

Figure 3 ilustrates a thyristor device 100 comprising a body of wafer 102 of semiconductor material, metallic electrodes 104, 106 and 108 and electric field spreading members 110 and 112. The wafer 102 has four zones of alternate conductivity type separated by PN junctions. Cathode emitter zone 114 of N-type conductivity is disposed in body 102 at top major surface 115. A cathode base zone 116 of P-type conductivity is disposed in body 102 beneath zone 114 and extending past zone 114 to major surface 115. Anode base zone 118 of N-type conductivity is disposed in body 102 beneath zone 116 and extending past zone 116 to an outer portion of major surface 115. An anode emitter zone 120 of P-type conductivity is disposed in body 102 beneath zone 118 and adjacent to bottom major surface 121. N-type base zone 118 encompasses the periphery of body 102 from top major surface 115 to bottom major surface 121. Cathode electrode 104 is affixed to top major surface 115 in contact with N-type emitter zone 114. Gate electrode 106 is affixed to top major surface 115 in contact with N-type emitter zone 114. Gate electrode 106 is affixed to top major surface 115 in contact with P-type base zone 116. Anode electrode 108 is affixed to bottom major surface 121 in contact with P-type emitter zone 120. PN junction 123, which separates zones 114 and 116, intersects top major surface 115 in a circle or closed loop. PN junction 125, which separates zones 116 and 118, intersects top major surface 115 in a circle or closed loop surrounding the loop of PN junction 123. PN junction 127, which separates zones 118 and 120, intersects bottom major surface 121 in a circle or closed loop.

Field spreaders 110 and 112 form annular rings on surfaces 115 and 121 overlying PN junctions 125 and 127 respectively. Field spreader 110 comprises an insulating layer 130 of silicon dioxide disposed on major surface 115 bridging PN junction 125, a resistive layer 132 of polycrystalline silicon disposed on layer 130, an inner metallic contact 134 disposed on zone 116 and overlapping the inner portion of layer 132 in juxtaposition over the intersection of PN junction 125 with major surface 115, and an outer metallic contact 136 disposed on zone 118 and overlapping the outer portion of layer 132. Field spreader 110 provides a resistive path between N-type base zone 118 and P-type base zone 116, which increases the surface breakdown capability of PN junction 125 in a known manner as described above. Similarly, field spreader 112 increases the surface blocking capability of PN junction 127, numerals 140, 142, 144 and 146 being analogous to numerals 130, 132, 134 and 136.

Now referring to Figure 4, a thyristor device 200 illustrates a presently preferred embodiment of the invention. The thyristor 200 comprises a body of wafer 202 of semiconductor material, metallic electrodes 204 and 208, and electric field spreading member 210. Cathode electrode 204 is disposed on top major surface 215 of the wafer 202 in contact with cathode emitter zone 214 of N-type conductivity. Cathode base zone 216 of P-type conductivity is disposed beneath zone 214 and extending past zone 214 to share a portion of top major surface 215 as shown. Anode base zone 218 of N-type conductivity is disposed beneath zone 216 and extends past zone 216 to top major surface 215. Anode emitter zone 220 of P-type conductivity is disposed beneath zone 218 adjacent to bottom major surface 221 of the wafer 202 where contact is made with anode electrode 208. P-type anode emitter zone 220 also encompasses the entire periphery of the wafer 202 extending past zone 218 and terminating at the periphery of top major surface 215.

Separating the four zones of alternate conductivity are three PN junctions, all of which emerge at top major surface 125. Separating zones 214 and 216 is PN junction 223, separating zones 216 and 218 is PN junction 225, and separating zones 218 and 220 is PN junction 227. PN junction 225 serves as the forward blocking junction and PN junction 227 serves as the reverse blocking junction of the thyristor device 200. Unlike PN junctions 225 and 227, PN junction 223 is not a high voltage blocking junction; rather, PN junction 223 serves to initiate conduction of the thyristor device 200.

As shown in Figure 4, field spreader 210 overlaps both high voltage blocking junctions 225 and 227. Field spreader 210 comprises an insulating layer 230 of silicon dioxide disposed on top major surface 215, a resistive layer 232 of polycrystaline silicon disposed on and conforming to insulating layer 230, and metallic contacts 234 and 236 partially overlapping resistive layer 232 and the adjacent portions of surface 215. The insulating layer 230 covers anode base zone 218 forming a closed loop on top major surface 215. Inner contact 234 electrically connects resistive layer 232 to zone 216, contact 234 being juxtaposed over PN junction 225 at its intersection with surface 215. Outer contact 236 electrically connects resistive layer 232 to zone 220, contact 236 being juxtaposed over PN junction 227 at its intersection with surface 215. Note that it is not necessary to have a separate gate electrode, since electrode 234 can also perform the gating function.

Resistive layer 232 provides a resistive path across N-type base zone 218. When the thyristor device 200 is operating in the forward blocking mode, PN junction 225 is reverse biased and PN junction 227 is forward biased. As known in the art, there exists a depletion layer around a blocking junction which spreads away from the junction as the blocking voltage is increased. Therefore, when device 200 is operating in the forward blocking mode, the depletion layer around PN junction 225, along with its corresponding electrical field, spreads in the semiconductor body 202 and along major surface 215 at the portion of surface 215 under the field spreading member 210. Resistive layer 232 and inner metallic contact 234 operate to spread the electrical field in a known manner to maximize the surface breakdown voltage of blocking junction 225. Likewise, when the device 200 is operating in a reverse blocking mode, PN junction 227 is reverse biased and PN junction 225 is forward biased. Therefore, in the reverse blocking mode, field spreader 210 similarly serves to maximize the surface breakdown voltage of PN junction 227, in which case outer metallic contact 236 and resistive layer 232 operate to spread the electric field.

The preferred embodiment of the present invention provides a novel thyristor device having a single field spreader which effectively serves to maximize the surface breakdown capability of both the forward and reverse blocking junctions. Furthermore, device 200 is easily manufactured with known techniques since only one major surface requires a field spreader. In addition, device 200 has an anode electrode 208 which supports the semiconductor wafer 202 at its fragile periphery, thereby providing a rigid commercially practical device.

It is presently preferred that the semiconductor wafer 202 be circular or disc-shaped and that the PN junctions intersect major surface 215 in concentric circles. In such an embodiment, field spreader 210 will appear as an anular ring. It is possible, however, to conceive of a number of different shapes equally suitable to practicing the present invention.

For example, in Figure 5 there is shown a plan view of device 200 wherein the semiconductor wafer 202 is in the shape of a quadrangle. In such an embodiment field spreader 210 has straight edges and rounded corners corresponding to the intersections of the blocking PN junctions with major surface 215. The straight edges are necessary to maximise the active surface area available to cathode electrode 204, and the rounded corners are necessary to prevent high field concentrations. A suitable radius of curvature at the corners would be about twice the maximum spread of the depletion layer from the blocking junctions. In any event, whatever geometrical shape is chosen for device 200, it is only necessary that the field spreader 210 form a closed loop on the semiconductor surface corresponding to the underlying closed loops delineated by the intersections of the blocking junctions with top major surface 215.

WHAT WE CLAIM IS:—

1. A thyristor comprising: a semiconductor body having a cathode emitter disposed in said body along a first major surface; a cathode base extending around said cathode emitter to said first surface; an anode base extending around said cathode base to said first surface; an anode emitter extending around said anode base to said first surface and bordering a second major surface of said body; and an electric field spreader comprising a resistive path making an electrical connection between the anode emitter and the cathode base disposed on said first major surface for spreading a blocking mode field.

2. A thyristor according to claim 1 wherein the field spreader comprises an annular shaped member spanning said anode base to provide the resistive path between said cathode base and said anode emitter.

3. A thyristor according to claim 1 or 2 wherein said field spreader comprises an insulating layer disposed on said top major surface covering said anode base and forming a closed loop on said first surface, a resistive layer disposed on and conforming to the shape of said insulating layer, and a connection between said resistive layer and said cathode base and a connection between said resistive layer and said anode emitter.

4. A thyristor according to claim 3 wherein said insulating layer comprises silicon dioxide, and said resistive layer comprises polycrystalline silicon having a resistivity from about 10^6 ohm-cm to about 10^8 ohm-cm.

5. A thyristor according to any one of claims 1-4 wherein said anode emitter encompasses the entire peripheral edge of said body.

6. A thyristor substantially as hereinbefore described with reference to and as illustrated in Fig. 4 or 5.

RONALD VAN BERLYN

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1981. Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1585790 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

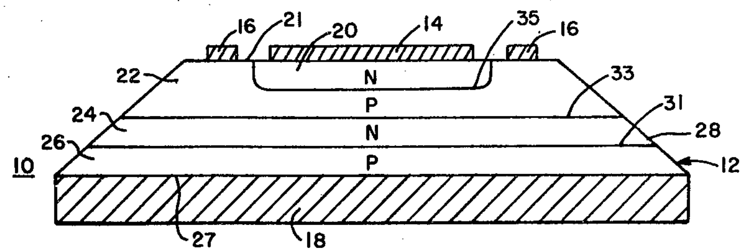

FIG. 1

PRIOR ART

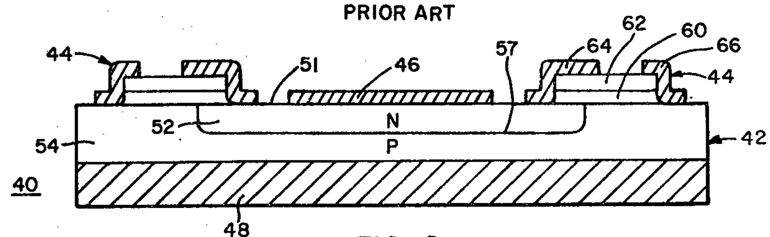

FIG. 2

PRIOR ART

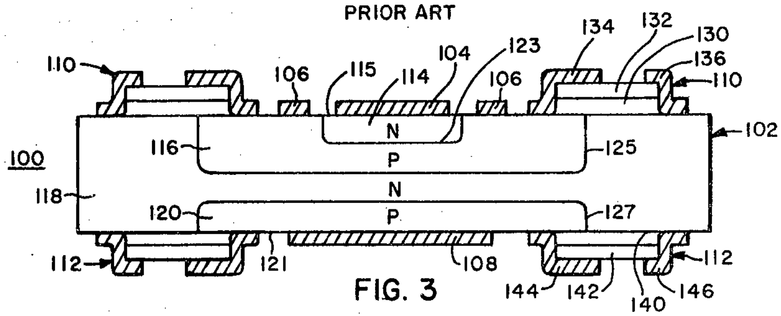

FIG. 3

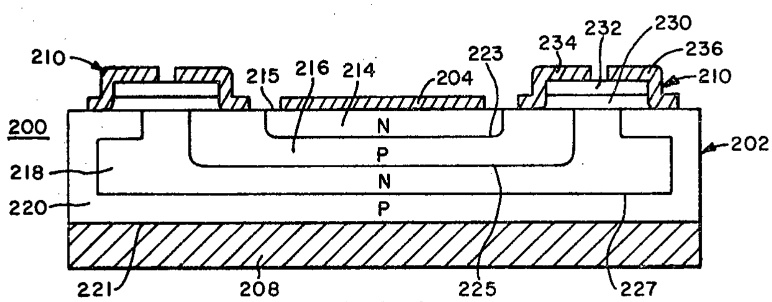

FIG. 4

1585790 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 2

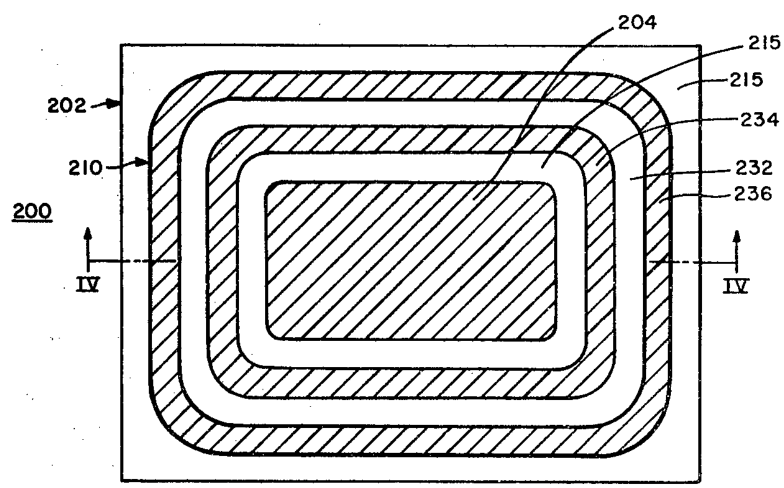

FIG. 5