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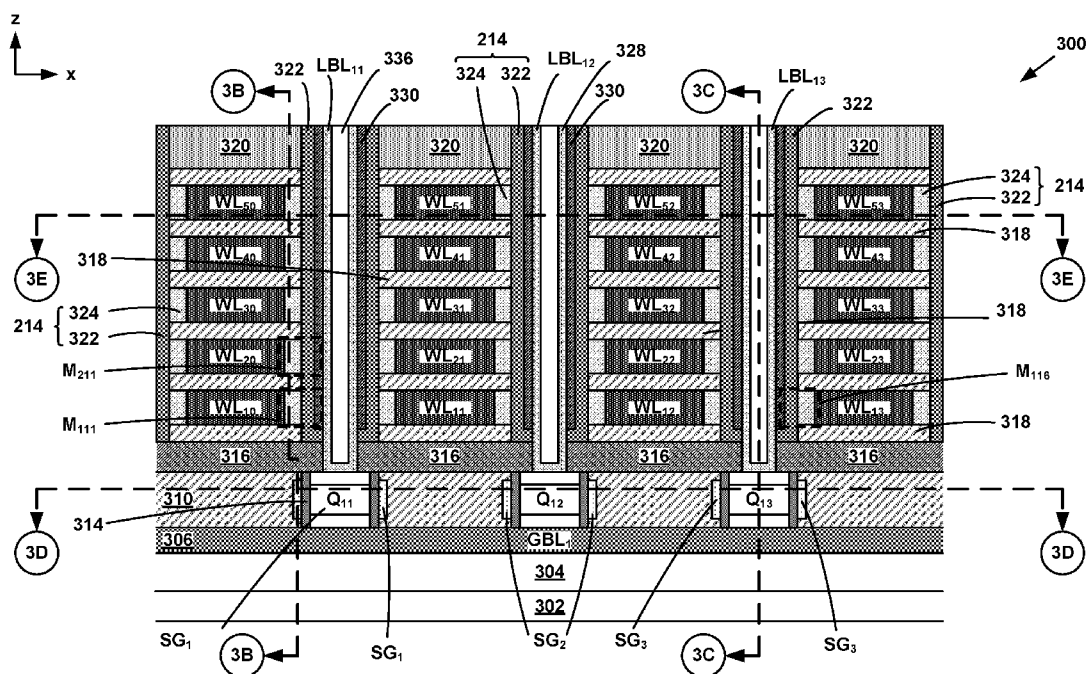


FIG. 3A

(57) Abstract: A method is provided that includes forming a word line above a substrate, the word line disposed in a first direction, forming a bit line above the substrate, the bit line disposed in a second direction perpendicular to the first direction, forming a nonvolatile memory material between the word line and the bit line by selectively forming a conductive oxide material layer adjacent the word line, and forming a semiconductor material layer adjacent the bit line, and forming a memory cell comprising the nonvolatile memory material at an intersection of the bit line and the word line.

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METHODS AND APPARATUS FOR THREE-DIMENSIONAL NONVOLATILE MEMORY

BACKGROUND

[0001] Semiconductor memory is widely used in various electronic devices such as mobile computing devices, mobile phones, solid-state drives, digital cameras, personal digital assistants, medical electronics, servers, and non-mobile computing devices. Semiconductor memory may include non-volatile memory or volatile memory. A non-volatile memory device allows information to be stored or retained even when the non-volatile memory device is not connected to a power source.

[0002] One example of non-volatile memory uses memory cells that include reversible resistance-switching memory elements that may be set to either a low resistance state or a high resistance state. The memory cells may be individually connected between first and second conductors (e.g., a bit line electrode and a word line electrode). The state of such a memory cell is typically changed by proper voltages being placed on the first and second conductors.

[0003] In recent years, non-volatile memory devices have been scaled to reduce the cost per bit. However, as process geometries shrink, many design and process challenges are presented

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1A depicts an embodiment of a memory system and a host.

[0005] FIG. 1B depicts an embodiment of memory core control circuits.

[0006] FIG. 1C depicts an embodiment of a memory core.

[0007] FIG. 1D depicts an embodiment of a memory bay.

[0008] FIG. 1E depicts an embodiment of a memory block.

[0009] FIG. 1F depicts another embodiment of a memory bay.

[0010] FIG. 2A depicts an embodiment of a portion of a monolithic three-dimensional memory array.

[0011] FIG. 2B depicts an embodiment of a portion of a monolithic three-dimensional memory array that includes vertical strips of a non-volatile memory material.

[0012] FIGS. 3A-3E depict various views of an embodiment monolithic three-dimensional memory array.

[0013] FIGS. 4A1-4J2 are cross-sectional views of a portion of a substrate during an example fabrication of the monolithic three-dimensional memory array of FIGS. 3A-3E.

DETAILED DESCRIPTION

[0014] Technology is described for forming monolithic three-dimensional nonvolatile memory arrays. In particular, technology is described for forming monolithic three-dimensional nonvolatile memory arrays that include reversible resistance-switching memory cells that have resistance-switching elements, each disposed between a word line and a bit line. Each reversible resistance-switching element includes a conductive oxide material layer and a semiconductor material layer. In an embodiment, each conductive oxide material layer is selectively formed adjacent a corresponding word line.

[0015] In some embodiments, a memory array may include a cross-point memory array. A cross-point memory array may refer to a memory array in which two-terminal memory cells are placed at the intersections of a first set of control lines (e.g., word lines) arranged in a first direction and a second set of control lines (e.g., bit lines) arranged in a second direction perpendicular to the first direction. The two-terminal memory cells may include a reversible resistance-switching memory element disposed between first and second conductors. Example reversible resistance-switching memory elements include a phase change material, a ferroelectric material, a metal oxide (e.g., hafnium oxide), a barrier modulated switching structure, or other similar reversible resistance-switching memory elements.

[0016] Example barrier modulated switching structures include a semiconductor material layer (e.g., an amorphous silicon layer) adjacent a conductive oxide material layer (e.g., a titanium oxide layer). Other example barrier modulated switching structures include a thin (e.g., less than about 2 nm) barrier oxide material (e.g., an aluminum oxide layer) disposed between a semiconductor material layer (e.g., an amorphous silicon layer) and a conductive oxide material layer (e.g., a titanium oxide layer). Still other example barrier modulated switching structures include a barrier oxide material (e.g., an aluminum oxide layer) disposed adjacent a conductive oxide material layer (e.g., a titanium oxide layer), with no semiconductor material layer (e.g., amorphous silicon) in the barrier modulated switching structure. As used herein, a memory cell that includes a barrier modulated switching structure is referred to herein as a “barrier modulated cell” (BMC).

[0017] In some embodiments, each memory cell in a cross-point memory array includes a reversible resistance-switching memory element in series with a steering element or an isolation element, such as a diode, to reduce leakage currents. In other cross-point memory arrays, the memory cells do not include an isolation element.

[0018] In an embodiment, a non-volatile storage system may include one or more two-dimensional arrays of non-volatile memory cells. The memory cells within a two-dimensional memory array may form a single layer of memory cells and may be selected via control lines (e.g., word lines and bit lines) in the X and Y directions. In another embodiment, a non-volatile storage system may include one or more monolithic three-dimensional memory arrays in which two or more layers of memory cells may be formed above a single substrate without any intervening substrates.

[0019] In some cases, a three-dimensional memory array may include one or more vertical columns of memory cells located above and orthogonal to a substrate. In an example, a non-volatile storage system may include a memory array with vertical bit lines or bit lines that are arranged orthogonal to a semiconductor substrate. The substrate may include a silicon substrate. The memory array may include rewriteable non-volatile memory cells, wherein each memory cell includes a reversible resistance-switching memory element without an isolation element in series with the reversible resistance-switching memory element (e.g., no diode in series with the reversible resistance-switching memory element).

[0020] In some embodiments, a non-volatile storage system may include a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate. The non-volatile storage system may also include circuitry associated with the operation of the memory cells (e.g., decoders, state machines, page registers, and/or control circuitry for controlling reading, programming and erasing of the memory cells). The circuitry associated with the operation of the memory cells may be located above the substrate or within the substrate.

[0021] In some embodiments, a non-volatile storage system may include a monolithic three-dimensional memory array. The monolithic three-dimensional memory array may include one or more levels of memory cells. Each memory cell within a first level of the one or more levels of memory cells may include an active area that is located above a substrate (e.g., above a single-crystal substrate or a crystalline silicon substrate). In one example, the active area may include a semiconductor junction (e.g., a P-N junction). The active area may include a portion of a source or drain region of a transistor. In another example, the active area may include a channel region of a transistor.

[0022] FIG. 1A depicts one embodiment of a memory system 100 and a host 102. Memory system 100 may include a non-volatile storage system interfacing with host 102 (e.g., a mobile computing device). In some cases, memory system 100 may be embedded within host 102. In other cases, memory system 100 may include a memory card. As depicted, memory system 100 includes a memory chip controller 104 and a memory chip 106. Although a single memory chip 106 is depicted, memory system 100 may include more than one memory chip (e.g., four, eight or some other number of memory chips). Memory chip controller 104 may receive data and commands from host 102 and provide memory chip data to host 102.

[0023] Memory chip controller 104 may include one or more state machines, page registers, SRAM, and control circuitry for controlling the operation of memory chip 106. The one or more state machines, page registers, SRAM, and control circuitry for controlling the operation of memory chip 106 may be referred to as managing or control circuits. The managing or control circuits may facilitate one or more memory array operations, such as forming, erasing, programming, and reading operations.

[0024] In some embodiments, the managing or control circuits (or a portion of the managing or control circuits) for facilitating one or more memory array operations may be integrated within memory chip 106. Memory chip controller 104 and memory chip 106 may be arranged on a single integrated circuit. In other embodiments, memory chip controller 104 and memory chip 106 may be arranged on different integrated circuits. In some cases, memory chip controller 104 and memory chip 106 may be integrated on a system board, logic board, or a PCB.

[0025] Memory chip 106 includes memory core control circuits 108 and a memory core 110. Memory core control circuits 108 may include logic for controlling the selection of memory blocks (or arrays) within memory core 110, controlling the generation of voltage references for biasing a particular memory array into a read or write state, and generating row and column addresses.

[0026] Memory core 110 may include one or more two-dimensional arrays of memory cells or one or more three-dimensional arrays of memory cells. In an embodiment, memory core control circuits 108 and memory core 110 are arranged on a single integrated circuit. In other embodiments, memory core control circuits 108 (or a portion of memory core control circuits 108) and memory core 110 may be arranged on different integrated circuits.

[0027] A memory operation may be initiated when host 102 sends instructions to memory chip controller 104 indicating that host 102 would like to read data from memory system 100 or write data to memory system 100. In the event of a write (or programming) operation, host 102 will send to memory chip controller 104 both a write command and the data to be written. The data to be written may be buffered by memory chip controller 104 and error correcting code (ECC) data may be generated corresponding with the data to be written. The ECC data, which allows data errors that occur during transmission or storage to be detected and/or corrected, may be written to memory core 110 or stored in non-volatile memory within memory chip controller 104. In an embodiment, the ECC data are generated and data errors are corrected by circuitry within memory chip controller 104.

[0028] Memory chip controller 104 controls operation of memory chip 106. In one example, before issuing a write operation to memory chip 106, memory chip controller 104 may check a status register to make sure that memory chip 106 is able to accept the data to be written. In another example, before issuing a read operation to memory chip 106, memory

chip controller 104 may pre-read overhead information associated with the data to be read. The overhead information may include ECC data associated with the data to be read or a redirection pointer to a new memory location within memory chip 106 in which to read the data requested. Once a read or write operation is initiated by memory chip controller 104, memory core control circuits 108 may generate the appropriate bias voltages for word lines and bit lines within memory core 110, and generate the appropriate memory block, row, and column addresses.

[0029] In some embodiments, one or more managing or control circuits may be used for controlling the operation of a memory array. The one or more managing or control circuits may provide control signals to a memory array to perform an erase operation, a read operation, and/or a write operation on the memory array. In one example, the one or more managing or control circuits may include any one of or a combination of control circuitry, state machine, decoders, sense amplifiers, read/write circuits, and/or controllers. The one or more managing circuits may perform or facilitate one or more memory array operations including erasing, programming, or reading operations. In one example, one or more managing circuits may include an on-chip memory controller for determining row and column address, word line and bit line addresses, memory array enable signals, and data latching signals.

[0030] FIG. 1B depicts one embodiment of memory core control circuits 108. As depicted, memory core control circuits 108 include address decoders 120, voltage generators for first control lines 122, voltage generators for second control lines 124 and signal generators for reference signals 126 (described in more detail below). Control lines may include word lines, bit lines, or a combination of word lines and bit lines. First control lines may include first (e.g., selected) word lines and/or first (e.g., selected) bit lines that are used to place memory cells into a first (e.g., selected) state. Second control lines may include second (e.g., unselected) word lines and/or second (e.g., unselected) bit lines that are used to place memory cells into a second (e.g., unselected) state.

[0031] Address decoders 120 may generate memory block addresses, as well as row addresses and column addresses for a particular memory block. Voltage generators (or voltage regulators) for first control lines 122 may include one or more voltage generators for generating first (e.g., selected) control line voltages. Voltage generators for second control lines 124 may include one or more voltage generators for generating second (e.g., unselected)

control line voltages. Signal generators for reference signals 126 may include one or more voltage and/or current generators for generating reference voltage and/or current signals.

[0032] FIGS. 1C-1F depict one embodiment of a memory core organization that includes a memory core having multiple memory bays, and each memory bay having multiple memory blocks. Although a memory core organization is disclosed where memory bays include memory blocks, and memory blocks include a group of memory cells, other organizations or groupings also can be used with the technology described herein.

[0033] FIG. 1C depicts an embodiment of memory core 110 of FIG. 1A. As depicted, memory core 110 includes memory bay 130 and memory bay 132. In some embodiments, the number of memory bays per memory core can differ for different implementations. For example, a memory core may include only a single memory bay or multiple memory bays (e.g., 16 or other number of memory bays).

[0034] FIG. 1D depicts an embodiment of memory bay 130 in FIG. 1C. As depicted, memory bay 130 includes memory blocks 140-144 and read/write circuits 146. In some embodiments, the number of memory blocks per memory bay may differ for different implementations. For example, a memory bay may include one or more memory blocks (e.g., 32 or other number of memory blocks per memory bay). Read/write circuits 146 include circuitry for reading and writing memory cells within memory blocks 140-144.

[0035] As depicted, read/write circuits 146 may be shared across multiple memory blocks within a memory bay. This allows chip area to be reduced because a single group of read/write circuits 146 may be used to support multiple memory blocks. However, in some embodiments, only a single memory block may be electrically coupled to read/write circuits 146 at a particular time to avoid signal conflicts.

[0036] In some embodiments, read/write circuits 146 may be used to write one or more pages of data into memory blocks 140-144 (or into a subset of the memory blocks). The memory cells within memory blocks 140-144 may permit direct over-writing of pages (i.e., data representing a page or a portion of a page may be written into memory blocks 140-144 without requiring an erase or reset operation to be performed on the memory cells prior to writing the data).

[0037] In one example, memory system 100 of FIG. 1A may receive a write command including a target address and a set of data to be written to the target address. Memory system 100 may perform a read-before-write (RBW) operation to read the data currently stored at the target address and/or to acquire overhead information (e.g., ECC information) before performing a write operation to write the set of data to the target address.

[0038] In some cases, read/write circuits 146 may be used to program a particular memory cell to be in one of three or more data/resistance states (i.e., the particular memory cell may include a multi-level memory cell). In one example, read/write circuits 146 may apply a first voltage difference (e.g., 2V) across the particular memory cell to program the particular memory cell into a first state of the three or more data/resistance states or a second voltage difference (e.g., 1V) across the particular memory cell that is less than the first voltage difference to program the particular memory cell into a second state of the three or more data/resistance states.

[0039] Applying a smaller voltage difference across the particular memory cell may cause the particular memory cell to be partially programmed or programmed at a slower rate than when applying a larger voltage difference. In another example, read/write circuits 146 may apply a first voltage difference across the particular memory cell for a first time period to program the particular memory cell into a first state of the three or more data/resistance states, and apply the first voltage difference across the particular memory cell for a second time period less than the first time period. One or more programming pulses followed by a memory cell verification phase may be used to program the particular memory cell to be in the correct state.

[0040] FIG. 1E depicts an embodiment of memory block 140 in FIG. 1D. As depicted, memory block 140 includes a memory array 150, row decoder 152, and column decoder 154. Memory array 150 may include a contiguous group of memory cells having contiguous word lines and bit lines. Memory array 150 may include one or more layers of memory cells. Memory array 150 may include a two-dimensional memory array or a three-dimensional memory array.

[0041] Row decoder 152 decodes a row address and selects a particular word line in memory array 150 when appropriate (e.g., when reading or writing memory cells in memory array 150). Column decoder 154 decodes a column address and selects one or more bit lines

in memory array 150 to be electrically coupled to read/write circuits, such as read/write circuits 146 in FIG. 1D. In one embodiment, the number of word lines is 4K per memory layer, the number of bit lines is 1K per memory layer, and the number of memory layers is 4, providing a memory array 150 containing 16M memory cells.

[0042] FIG. 1F depicts an embodiment of a memory bay 134. Memory bay 134 is an alternative example implementation for memory bay 130 of FIG. 1D. In some embodiments, row decoders, column decoders, and read/write circuits may be split or shared between memory arrays. As depicted, row decoder 152b is shared between memory arrays 150a and 150b because row decoder 152b controls word lines in both memory arrays 150a and 150b (i.e., the word lines driven by row decoder 152b are shared).

[0043] Row decoders 152a and 152b may be split such that even word lines in memory array 150a are driven by row decoder 152a and odd word lines in memory array 150a are driven by row decoder 152b. Row decoders 152c and 152b may be split such that even word lines in memory array 150b are driven by row decoder 152c and odd word lines in memory array 150b are driven by row decoder 152b.

[0044] Column decoders 154a and 154b may be split such that even bit lines in memory array 150a are controlled by column decoder 154b and odd bit lines in memory array 150a are driven by column decoder 154a. Column decoders 154c and 154d may be split such that even bit lines in memory array 150b are controlled by column decoder 154d and odd bit lines in memory array 150b are driven by column decoder 154c.

[0045] The selected bit lines controlled by column decoder 154a and column decoder 154c may be electrically coupled to read/write circuits 146a. The selected bit lines controlled by column decoder 154b and column decoder 154d may be electrically coupled to read/write circuits 146b. Splitting the read/write circuits into read/write circuits 146a and 146b when the column decoders are split may allow for a more efficient layout of the memory bay.

[0046] FIG. 2A depicts one embodiment of a portion of a monolithic three-dimensional memory array 200 that includes a first memory level 210, and a second memory level 212 positioned above first memory level 210. Memory array 200 is one example of an implementation for memory array 150 of FIG. 1E. Local bit lines LBL₁₁-LBL₃₃ are arranged

in a first direction (e.g., a vertical or z-direction) and word lines WL₁₀-WL₂₃ are arranged in a second direction (e.g., an x-direction) perpendicular to the first direction. This arrangement of vertical bit lines in a monolithic three-dimensional memory array is one embodiment of a vertical bit line memory array.

[0047] As depicted, disposed between the intersection of each local bit line and each word line is a particular memory cell (e.g., memory cell M₁₁₁ is disposed between local bit line LBL₁₁ and word line WL₁₀). The particular memory cell may include a floating gate memory element, a charge trap memory element (e.g., using a silicon nitride material), a reversible resistance-switching memory element, or other similar device. The global bit lines GBL₁-GBL₃ are arranged in a third direction (e.g., a y-direction) that is perpendicular to both the first direction and the second direction.

[0048] Each local bit line LBL₁₁-LBL₃₃ has an associated bit line select transistor Q₁₁-Q₃₃, respectively. Bit line select transistors Q₁₁-Q₃₃ may be field effect transistors, such as shown, or may be any other transistors. As depicted, bit line select transistors Q₁₁-Q₃₁ are associated with local bit lines LBL₁₁-LBL₃₁, respectively, and may be used to connect local bit lines LBL₁₁-LBL₃₁ to global bit lines GBL₁-GBL₃, respectively, using row select line SG₁. In particular, each of bit line select transistors Q₁₁-Q₃₁ has a first terminal (e.g., a drain/source terminal) coupled to a corresponding one of local bit lines LBL₁₁-LBL₃₁, respectively, a second terminal (e.g., a source/drain terminal) coupled to a corresponding one of global bit lines GBL₁-GBL₃, respectively, and a third terminal (e.g., a gate terminal) coupled to row select line SG₁.

[0049] Similarly, bit line select transistors Q₁₂-Q₃₂ are associated with local bit lines LBL₁₂-LBL₃₂, respectively, and may be used to connect local bit lines LBL₁₂-LBL₃₂ to global bit lines GBL₁-GBL₃, respectively, using row select line SG₂. In particular, each of bit line select transistors Q₁₂-Q₃₂ has a first terminal (e.g., a drain/source terminal) coupled to a corresponding one of local bit lines LBL₁₂-LBL₃₂, respectively, a second terminal (e.g., a source/drain terminal) coupled to a corresponding one of global bit lines GBL₁-GBL₃, respectively, and a third terminal (e.g., a gate terminal) coupled to row select line SG₂.

[0050] Likewise, bit line select transistors Q_{13} - Q_{33} are associated with local bit lines LBL_{13} - LBL_{33} , respectively, and may be used to connect local bit lines LBL_{13} - LBL_{33} to global bit lines GBL_1 - GBL_3 , respectively, using row select line SG_3 . In particular, each of bit line select transistors Q_{13} - Q_{33} has a first terminal (e.g., a drain/source terminal) coupled to a corresponding one of local bit lines LBL_{13} - LBL_{33} , respectively, a second terminal (e.g., a source/drain terminal) coupled to a corresponding one of global bit lines GBL_1 - GBL_3 , respectively, and a third terminal (e.g., a gate terminal) coupled to row select line SG_3 .

[0051] Because a single bit line select transistor is associated with a corresponding local bit line, the voltage of a particular global bit line may be selectively applied to a corresponding local bit line. Therefore, when a first set of local bit lines (e.g., LBL_{11} - LBL_{31}) is biased to global bit lines GBL_1 - GBL_3 , the other local bit lines (e.g., LBL_{12} - LBL_{32} and LBL_{13} - LBL_{33}) must either also be driven to the same global bit lines GBL_1 - GBL_3 or be floated.

[0052] In an embodiment, during a memory operation, all local bit lines within the memory array are first biased to an unselected bit line voltage by connecting each of the global bit lines to one or more local bit lines. After the local bit lines are biased to the unselected bit line voltage, then only a first set of local bit lines LBL_{11} - LBL_{31} are biased to one or more selected bit line voltages via the global bit lines GBL_1 - GBL_3 , while the other local bit lines (e.g., LBL_{12} - LBL_{32} and LBL_{13} - LBL_{33}) are floated. The one or more selected bit line voltages may correspond with, for example, one or more read voltages during a read operation or one or more programming voltages during a programming operation.

[0053] In an embodiment, a vertical bit line memory array, such as memory array 200, includes a greater number of memory cells along the word lines as compared with the number of memory cells along the vertical bit lines (e.g., the number of memory cells along a word line may be more than 10 times the number of memory cells along a bit line). In one example, the number of memory cells along each bit line may be 16 or 32, whereas the number of memory cells along each word line may be 2048 or more than 4096. Other numbers of memory cells along each bit line and along each word line may be used.

[0054] In an embodiment of a read operation, the data stored in a selected memory cell (e.g., memory cell M_{111}) may be read by biasing the word line connected to the selected memory cell (e.g., selected word line WL_{10}) to a selected word line voltage in read mode (e.g., 0V). The local bit line (e.g., LBL_{11}) coupled to the selected memory cell (M_{111}) is biased to a selected bit line voltage in read mode (e.g., 1 V) via the associated bit line select transistor (e.g., Q_{11}) coupled to the selected local bit line (LBL_{11}), and the global bit line (e.g., GBL_1) coupled to the bit line select transistor (Q_{11}). A sense amplifier may then be coupled to the selected local bit line (LBL_{11}) to determine a read current I_{READ} of the selected memory cell (M_{111}). The read current I_{READ} is conducted by the bit line select transistor Q_{11} , and may be between about 100 nA and about 500 nA, although other read currents may be used.

[0055] In an embodiment of a write operation, data may be written to a selected memory cell (e.g., memory cell M_{221}) by biasing the word line connected to the selected memory cell (e.g., WL_{20}) to a selected word line voltage in write mode (e.g., 5V). The local bit line (e.g., LBL_{21}) coupled to the selected memory cell (M_{221}) is biased to a selected bit line voltage in write mode (e.g., 0 V) via the associated bit line select transistor (e.g., Q_{21}) coupled to the selected local bit line (LBL_{21}), and the global bit line (e.g., GBL_2) coupled to the bit line select transistor (Q_{21}). During a write operation, a programming current I_{PRGM} is conducted by the associated bit line select transistor Q_{21} , and may be between about 3 uA and about 6 uA, although other programming currents may be used.

[0056] During the write operation described above, the word line (e.g., WL_{20}) connected to the selected memory cell (M_{221}) may be referred to as a “selected word line,” and the local bit line (e.g., LBL_{21}) coupled to the selected memory cell (M_{221}) may be referred to as the “selected local bit line.” All other word lines coupled to unselected memory cells may be referred to as “unselected word lines,” and all other local bit lines coupled to unselected memory cells may be referred to as “unselected local bit lines.” For example, if memory cell M_{221} is the only selected memory cell in memory array 200, word lines WL_{10} - WL_{13} and WL_{21} - WL_{23} are unselected word lines, and local bit lines LBL_{11} , LBL_{31} , LBL_{12} - LBL_{32} , and LBL_{13} - LBL_{33} are unselected local bit lines.

[0057] FIG. 2B depicts an embodiment of a portion of a monolithic three-dimensional memory array 202 that includes vertical strips of a non-volatile memory material. The portion of monolithic three-dimensional memory array 202 depicted in FIG. 2B may include an implementation for a portion of the monolithic three-dimensional memory array 200 depicted in FIG. 2A.

[0058] Monolithic three-dimensional memory array 202 includes word lines WL₁₀, WL₁₁, WL₁₂, . . . , WL₄₂ that are formed in a first direction (e.g., an x-direction), vertical bit lines LBL₁₁, LBL₁₂, LBL₁₃, . . . , LBL₂₃ that are formed in a second direction perpendicular to the first direction (e.g., a z-direction), and non-volatile memory material 214 formed in the second direction (e.g., the z-direction). A spacer 216 made of a dielectric material (e.g., silicon dioxide, silicon nitride, or other dielectric material) is disposed between adjacent word lines WL₁₀, WL₁₁, WL₁₂, . . . , WL₄₂.

[0059] Each non-volatile memory material 214 may include, for example, an oxide material, a reversible resistance-switching memory material (e.g., one or more metal oxide layers such as nickel oxide, hafnium oxide, or other similar metal oxide materials, a phase change material, a barrier modulated switching structure or other similar reversible resistance-switching memory material), a ferroelectric material, or other non-volatile memory material.

[0060] Each non-volatile memory material 214 may include a single material layer or multiple material layers. In an embodiment, each non-volatile memory material 214 includes a barrier modulated switching structure. Example barrier modulated switching structures include a semiconductor material layer (e.g., an amorphous silicon layer) adjacent a conductive oxide material layer (e.g., a titanium oxide layer). Other example barrier modulated switching structures include a thin (e.g., less than about 2 nm) barrier oxide material (e.g., an aluminum oxide layer) disposed between a semiconductor material layer (e.g., an amorphous silicon layer) and a conductive oxide material layer (e.g., a titanium oxide layer). Still other example barrier modulated switching structures include a barrier oxide material (e.g., an aluminum oxide layer) disposed adjacent a conductive oxide material layer (e.g., a titanium oxide layer), with no semiconductor material layer (e.g., amorphous silicon) in the barrier modulated switching structure. Such multi-layer embodiments may be used to form BMC memory elements.

[0061] In an embodiment, each non-volatile memory material 214 may include a single continuous layer of material that may be used by a plurality of memory cells or devices.

[0062] In an embodiment, portions of the non-volatile memory material 214 may include a part of a first memory cell associated with the cross section between WL₁₂ and LBL₁₃ and a part of a second memory cell associated with the cross section between WL₂₂ and LBL₁₃. In some cases, a vertical bit line, such as LBL₁₃, may include a vertical structure (e.g., a rectangular prism, a cylinder, or a pillar) and the non-volatile material may completely or partially surround the vertical structure (e.g., a conformal layer of phase change material surrounding the sides of the vertical structure).

[0063] As depicted, each of the vertical bit lines LBL₁₁, LBL₁₂, LBL₁₃, . . . , LBL₂₃ may be connected to one of a set of global bit lines via an associated vertically-oriented bit line select transistor (e.g., Q₁₁, Q₁₂, Q₁₃, Q₂₃). Each vertically-oriented bit line select transistor may include a MOS device (e.g., an NMOS device) or a vertical thin-film transistor (TFT).

[0064] In an embodiment, each vertically-oriented bit line select transistor is a vertically-oriented pillar-shaped TFT coupled between an associated local bit line pillar and a global bit line. In an embodiment, the vertically-oriented bit line select transistors are formed in a pillar select layer formed above a CMOS substrate, and a memory layer that includes multiple layers of word lines and memory elements is formed above the pillar select layer.

[0065] FIGS. 3A-3E depict various views of an embodiment of a portion of a monolithic three-dimensional memory array 300 that includes vertical strips of a non-volatile memory material. The physical structure depicted in FIGS. 3A-3E may include one implementation for a portion of the monolithic three-dimensional memory array depicted in FIG. 2B.

[0066] Monolithic three-dimensional memory array 300 includes vertical bit lines LBL₁₁-LBL₃₃ arranged in a first direction (e.g., a z-direction), word lines WL₁₀, WL₁₁, . . . , WL₅₃ arranged in a second direction (e.g., an x-direction) perpendicular to the first direction, and row select lines SG₁, SG₂, SG₃ arranged in the second direction, and global bit lines GBL₁, GBL₂, GBL₃ arranged in a third direction (e.g., a y-direction) perpendicular to the first and second directions.

[0067] Vertical bit lines LBL₁₁-LBL₃₃ are disposed above global bit lines GBL₁, GBL₂, GBL₃, which each have a long axis in the second (e.g., x-direction). Person of ordinary skill in the art will understand that monolithic three-dimensional memory arrays, such as monolithic three-dimensional memory array 300 may include more or fewer than twenty word lines, three row select lines, three global bit lines, and nine vertical bit lines.

[0068] In an embodiment, global bit lines GBL₁, GBL₂, GBL₃ are disposed above a substrate 302, such as a silicon, germanium, silicon-germanium, undoped, doped, bulk, silicon-on-insulator (“SOI”) or other substrate with or without additional circuitry. In an embodiment, an isolation layer 304, such as a layer of silicon dioxide, silicon nitride, silicon oxynitride or any other suitable insulating layer, is formed above substrate 302.

[0069] In an embodiment, a first dielectric material layer 308 (e.g., silicon dioxide) and a second dielectric material layer 310 (e.g., silicon dioxide) are formed above isolation layer 304. Global bit lines GBL₁, GBL₂, GBL₃ are disposed above isolation layer 304 and are separated from one another by first dielectric material layer 308.

[0070] Vertically-oriented bit line select transistors Q₁₁-Q₃₃ are disposed above global bit lines GBL₁, GBL₂, GBL₃ and are separated from one another by second dielectric material layer 310. Vertically-oriented bit line select transistors Q₁₁-Q₁₃ are disposed above and electrically coupled to global bit line GBL₁, vertically-oriented bit line select transistors Q₂₁-Q₂₃ are disposed above and electrically coupled to global bit line GBL₂, and vertically-oriented bit line select transistors Q₃₁-Q₃₃ are disposed above and electrically coupled to global bit line GBL₃.

[0071] Vertically-oriented bit line select transistors Q₁₁-Q₃₃ may be field effect transistors, although other transistors types may be used. In an embodiment, each of vertically-oriented bit line select transistors Q₃₁-Q₃₃ has a height between about 150 nm and about 500 nm. Other height values may be used.

[0072] Each of vertically-oriented bit line select transistors Q₁₁-Q₃₃ has a first terminal 312a (e.g., a drain/source terminal), a second terminal 312b (e.g., a source/drain terminal), a first control terminal 312c1 (e.g., a first gate terminal) and a second control

terminal 312c2 (e.g., a second gate terminal). First gate terminal 312c1 and second gate terminal 312c2 may be disposed on opposite sides of the vertically-oriented bit line select transistor. A gate dielectric material 314 (e.g., SiO₂) is disposed between first gate terminal 312c1 and first terminal 312a and second terminal 312b, and also is disposed between second gate terminal 312c2 and first terminal 312a and second terminal 312b.

[0073] First gate terminal 312c1 may be used to selectively induce a first electrically conductive channel between first terminal 312a and second terminal 312b of the transistor, and second gate terminal 312c2 may be used to selectively induce a second electrically conductive channel between first terminal 312a and second terminal 312b of the transistor. In an embodiment, first gate terminal 312c1 and second gate terminal 312c2 are coupled together to form a single control terminal 312c that may be used to collectively turn ON and OFF the vertically-oriented bit line select transistor.

[0074] Row select lines SG₁, SG₂, SG₃ are disposed above global bit lines GBL₁, GBL₂ and GBL₃, and form gate terminals 312c of vertically-oriented bit line select transistors Q₁₁-Q₃₃. In particular, row select line SG₁ forms the gate terminals of vertically-oriented bit line select transistors Q₁₁, Q₂₁ and Q₃₁, row select line SG₂ forms the gate terminals of vertically-oriented bit line select transistors Q₁₂, Q₂₂ and Q₃₂, and row select line SG₃ forms the gate terminals of vertically-oriented bit line select transistors Q₁₃, Q₂₃ and Q₃₃.

[0075] A first etch stop layer 316 (e.g., aluminum oxide) is disposed above second dielectric material layer 310. A stack of word lines WL₁₀, WL₁₁, . . . , WL₅₃ is disposed above first etch stop layer 316, with a third dielectric material layer 318 (e.g., silicon dioxide) separating adjacent word lines. A second etch stop layer 320 (e.g., polysilicon) may be formed above the stack of word lines WL₁₀, WL₁₁, . . . , WL₅₃. Each of word lines WL₁₀, WL₁₁, . . . , WL₅₃ includes a conductive material layer (e.g., titanium nitride, tungsten, tantalum nitride or other similar electrically conductive material, or combination thereof).

[0076] In an embodiment, non-volatile memory material 214 is disposed adjacent word lines WL₁₀, WL₁₁, . . . , WL₅₃. Non-volatile memory material 214 may include, for example, an oxide layer, a reversible resistance-switching material (e.g., one or more metal oxide layers such as nickel oxide, hafnium oxide, or other similar metal oxide materials, a phase

change material, a barrier modulated switching structure or other similar reversible resistance-switching memory material), a ferroelectric material, or other non-volatile memory material.

[0077] Non-volatile memory material 214 may include a single continuous layer of material that may be used by a plurality of memory cells or devices. For simplicity, non-volatile memory material 214 also will be referred to in the remaining discussion as reversible resistance-switching memory material 214.

[0078] Reversible resistance-switching memory material 214 may include a single material layer or multiple material layers. In an embodiment, reversible resistance-switching memory material 214 includes a barrier modulated switching structure. In some embodiments, barrier modulated switching structures include a semiconductor material layer (e.g., amorphous silicon) and a conductive oxide material layer (e.g., titanium oxide).

[0079] In an embodiment, reversible resistance-switching memory material 214 includes a barrier modulated switching structure that includes a semiconductor material layer 322 and a conductive oxide material layer 324. In an embodiment, semiconductor material layers 322 are disposed adjacent vertical bit line LBL₁₁-LBL₃₃, and conductive oxide material layers 324 are disposed in recesses 326 in word line portions WL_{10b}, WL_{11b}, . . . , WL_{53b}.

[0080] In embodiments, semiconductor material layer 322 has a thickness between about 3 nm and about 15 nm, and includes one or more of carbon, germanium, silicon, tantalum nitride, tantalum silicon nitride, or other similar semiconductor material. In embodiments, conductive oxide material layer 324 has a thickness between about 5 nm and about 25 nm, and includes one or more of aluminum-doped zinc oxide, aluminum-doped zirconium oxide, cerium oxide, indium tin oxide, niobium-doped strontium titanate, praseodymium calcium manganese oxide, titanium oxide, tungsten oxide, zinc oxide, or other similar conductive oxide material. Other semiconductor materials, conductive oxide materials, and thicknesses may be used.

[0081] In embodiments, each of semiconductor material layer 322, and conductive oxide material layer 324 may be amorphous, polycrystalline, nano-crystalline, or single crystalline, and each may be formed by chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), atomic layer deposition nanolaminates, or other

method. As described above, a BMC memory cell includes a barrier modulated switching structure.

[0082] Vertical bit lines LBL₁₁-LBL₃₃ are disposed adjacent reversible resistance-switching memory material 214, and are formed of a conductive material 328 (e.g., titanium nitride). In an embodiment, each of vertical bit lines LBL₁₁-LBL₃₃ includes an adhesion material layer 330 (e.g., titanium nitride) disposed between conductive material 328 and reversible resistance-switching memory material 214.

[0083] Vertical bit lines LBL₁₁-LBL₃₃ are separated from one another by a fourth dielectric material layer 332 (e.g., silicon dioxide). In an embodiment, a barrier material layer 334 (e.g., silicon nitride) is disposed between semiconductor material layer 322 and fourth dielectric material layer 332. In some embodiments, each of a vertical bit lines LBL₁₁-LBL₃₃ includes a vertical structure (e.g., a rectangular prism, a cylinder, or a pillar), and the vertical strip of reversible resistance-switching memory material 214 may completely or partially surround the vertical structure (e.g., a conformal layer of reversible resistance-switching material surrounding the sides of the vertical structure). In some embodiments, each of a vertical bit lines LBL₁₁-LBL₃₃ includes a non-conductive core 336 (e.g., amorphous silicon).

[0084] A memory cell is disposed between the intersection of each vertical bit line and each word line. For example, a memory cell M₁₁₁ is disposed between vertical bit line LBL₁₁ and word line WL₁₀, a memory cell M₁₁₆ is disposed between vertical bit line LBL₁₃ and word line WL₁₃, a memory cell M₅₁₁ is disposed between vertical bit line LBL₁₁ and word line WL₅₀, a memory cell M₅₃₆ is disposed between vertical bit line LBL₃₃ and word line WL₅₀, and so on. In an embodiment, monolithic three-dimensional memory array 300 includes ninety memory cells M₁₁₁, M₁₁₂, . . . , M₅₃₆. Persons of ordinary skill in the art will understand that monolithic three-dimensional memory arrays may include more or fewer than ninety memory cells.

[0085] In an example, portions of the reversible resistance-switching memory material 214 may include a part of memory cell M₁₁₁ associated with the cross section

between word line WL₁₀ and LBL₁₁, and a part of memory cell M₂₁₁ associated with the cross section between word line WL₂₀ and LBL₁₁, and so on.

[0086] Each of memory cells M₁₁₁, M₁₁₂, . . . , M₅₃₆ may include a floating gate device, a charge trap device (e.g., using a silicon nitride material), a resistive change memory device, or other type of memory device. Vertically-oriented bit line select transistors Q₁₁-Q₃₃ may be used to select a corresponding one of vertical bit lines LBL₁₁-LBL₃₃. Vertically-oriented bit line select transistors Q₁₁-Q₃₃ may be field effect transistors, although other transistors types may be used.

[0087] Thus, the first gate terminal and the second gate terminal of each of vertically-oriented bit line select transistors Q₁₁-Q₃₃ may be used to turn ON and OFF vertically-oriented bit line select transistors Q₁₁-Q₃₃. Without wanting to be bound by any particular theory, for each of vertically-oriented bit line select transistors Q₁₁-Q₃₃, it is believed that the current drive capability of the transistor may be increased by using both the first gate terminal and the second gate terminal to turn ON the transistor. For simplicity, the first and second gate terminal of each of select transistors Q₁₁-Q₃₃ will be referred to as a single gate terminal.

[0088] Vertically-oriented bit line select transistors Q₁₁, Q₁₂, Q₁₃ are used to selectively connect/disconnect vertical bit lines LBL₁₁, LBL₁₂, and LBL₁₃ to/from global bit line GBL₁ using row select lines SG₁, SG₂, SG₃, respectively. In particular, each of vertically-oriented bit line select transistors Q₁₁, Q₁₂, Q₁₃ has a first terminal (e.g., a drain./source terminal) coupled to a corresponding one of vertical bit lines LBL₁₁, LBL₁₂, and LBL₁₃, respectively, a second terminal (e.g., a source/drain terminal) coupled to global bit line GBL₁, and a control terminal (e.g., a gate terminal) coupled to row select line SG₁, SG₂, SG₃, respectively.

[0089] Row select lines SG₁, SG₂, SG₃ are used to turn ON/OFF vertically-oriented bit line select transistors Q₁₁, Q₁₂, Q₁₃, respectively, to connect/disconnect vertical bit lines LBL₁₁, LBL₁₂, and LBL₁₃, respectively, to/from global bit line GBL₁.

[0090] Likewise, vertically-oriented bit line select transistors Q₁₁, Q₂₁, . . . , Q₃₃ are used to selectively connect/disconnect vertical bit lines LBL₁₁, LBL₂₁, and LBL₃₁, respectively, to

global bit lines GBL₁, GBL₂, GBL₃, respectively, using row select line SG₁. In particular, each of vertically-oriented bit line select transistors Q₁₁, Q₂₁, Q₃₁ has a first terminal (e.g., a drain./source terminal) coupled to a corresponding one of vertical bit lines LBL₁₁, LBL₂₁, and LBL₃₁, respectively, a second terminal (e.g., a source/drain terminal) coupled to a corresponding one of global bit lines GBL₁, GBL₂, GBL₃, respectively, and a control terminal (e.g., a gate terminal) coupled to row select line SG₁. Row select line SG₁ is used to turn ON/OFF vertically-oriented bit line select transistors Q₁₁, Q₂₁, Q₃₁ to connect/disconnect vertical bit lines LBL₁₁, LBL₂₁, and LBL₃₁, respectively, to/from global bit lines GBL₁, GBL₂, GBL₃, respectively.

[0091] Similarly, vertically-oriented bit line select transistors Q₁₃, Q₂₃, Q₃₃ are used to selectively connect/disconnect vertical bit lines LBL₁₃, LBL₂₃, and LBL₃₃, respectively to/from global bit lines GBL₁, GBL₂, GBL₃, respectively, using row select line SG₃. In particular, each of vertically-oriented bit line select transistors Q₁₃, Q₂₃, Q₃₃ has a first terminal (e.g., a drain./source terminal) coupled to a corresponding one of vertical bit lines LBL₁₃, LBL₂₃, and LBL₃₃, respectively, a second terminal (e.g., a source/drain terminal) coupled to a corresponding one of global bit lines GBL₁, GBL₂, GBL₃, respectively, and a control terminal (e.g., a gate terminal) coupled to row select line SG₃. Row select line SG₃ is used to turn ON/OFF vertically-oriented bit line select transistors Q₁₃, Q₂₃, Q₃₃ to connect/disconnect vertical bit lines LBL₁₃, LBL₂₃, and LBL₃₃, respectively, to/from global bit lines GBL₁, GBL₂, GBL₃, respectively.

[0092] One previously known monolithic three-dimensional memory array, such as monolithic three-dimensional array 202 of FIG. 2B, includes BMC memory cells that include a semiconductor material layer (e.g., an amorphous silicon layer) and a conductive oxide material layer (e.g., a titanium oxide layer), with the semiconductor material layer adjacent the word lines, and the conductive oxide material layer adjacent the bit lines. In such BMC memory cells, word line driver circuitry may be unable to accurately read memory cell current because word line-word line leakage current exceeds the range of the word line driver circuitry. In particular, current leakage paths between adjacent word lines may be conducted by the semiconductor material layer.

[0093] One technique to reduce this leakage current uses word line oxidation to form an oxide between the word line and the adjacent semiconductor material layer. For example, peripheral edges of TiN word lines are oxidized to form TiO₂ regions separating the TiN word lines from the adjacent semiconductor material layer. However, TiN-oxidized TiO₂ may be too leaky to have a sufficiently large ON/OFF window for reliably reading memory cells.

[0094] Technology is described for forming BMC memory cells that include a conductive oxide material layer and a semiconductor material layer, with the conductive oxide material layer selectively formed adjacent a word line (e.g., in word line recesses), and the semiconductor material layer formed adjacent a bit line. Without wanting to be bound by any particular theory, it is believed that such BMC memory cells may sufficiently suppress word line-word line leakage so that word line driver circuitry may accurately read such BMC memory cells.

[0095] In particular, referring now to FIGS. 4A1-4J2, an example method of forming a monolithic three-dimensional memory array, such as monolithic three-dimensional array 300 of FIGS. 3A-3E, is described.

[0096] With reference to FIGS. 4A1-4A3, substrate 302 is shown as having already undergone several processing steps. Substrate 302 may be any suitable substrate such as a silicon, germanium, silicon-germanium, undoped, doped, bulk, silicon-on-insulator ("SOI") or other substrate with or without additional circuitry. For example, substrate 302 may include one or more n-well or p-well regions (not shown). Isolation layer 304 is formed above substrate 302. In some embodiments, isolation layer 304 may be a layer of silicon dioxide, silicon nitride, silicon oxynitride or any other suitable insulating layer.

[0097] Following formation of isolation layer 304, a conductive material layer 306 is deposited over isolation layer 304. Conductive material layer 306 may include any suitable conductive material such as tungsten or another appropriate metal, heavily doped semiconductor material, a conductive silicide, a conductive silicide-germanide, a conductive germanide, or the like deposited by any suitable method (e.g., CVD, PVD, etc.). In at least one embodiment, conductive material layer 306 may include between about 20 nm and about 250 nm of tungsten. Other conductive material layers and/or thicknesses may be used. In some embodiments, an adhesion layer (not shown), such as titanium nitride or other

similar adhesion layer material, may be disposed between isolation layer 304 and conductive material layer 306, and/or between conductive material layer 306 and subsequent vertically-oriented bit line select transistors layers.

[0098] Persons of ordinary skill in the art will understand that adhesion layers may be formed by PVD or another method on conductive material layers. For example, adhesion layers may be between about 2 nm and about 50 nm, and in some embodiments about 10 nm, of titanium nitride or another suitable adhesion layer such as tantalum nitride, tungsten nitride, tungsten, molybdenum, combinations of one or more adhesion layers, or the like. Other adhesion layer materials and/or thicknesses may be employed.

[0099] Following formation of conductive material layer 306, conductive material layer 306 is patterned and etched. For example, conductive material layer 306 may be patterned and etched using conventional lithography techniques, with a soft or hard mask, and wet or dry etch processing. In at least one embodiment, conductive material layer 306 is patterned and etched to form global bit lines GBL₁, GBL₂, GBL₃. Example widths for global bit lines GBL₁, GBL₂, GBL₃ and/or spacings between global bit lines GBL₁, GBL₂, GBL₃ range between about 20 nm and about 100 nm, although other conductor widths and/or spacings may be used.

[00100] After global bit lines GBL₁, GBL₂, GBL₃ have been formed, a first dielectric material layer 308 is formed over substrate 302 to fill the voids between global bit lines GBL₁, GBL₂, GBL₃. For example, approximately 300-700 nm of silicon dioxide may be deposited on the substrate 302 and planarized using chemical mechanical polishing or an etchback process to form a planar surface 400. Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric material layer thicknesses may be used. Example low K dielectrics include carbon doped oxides, silicon carbon layers, or the like.

[00101] In other embodiments, global bit lines GBL₁, GBL₂, GBL₃ may be formed using a damascene process in which first dielectric material layer 308 is formed, patterned and etched to create openings or voids for global bit lines GBL₁, GBL₂, GBL₃. The openings or voids then may be filled with conductive layer 306 (and/or a conductive seed, conductive fill

and/or barrier layer if needed). Conductive material layer 306 then may be planarized to form planar surface 400.

[00102] Following planarization, the semiconductor material used to form vertically-oriented bit line select transistors Q_{11} - Q_{33} is formed over planar surface 400 of substrate 302. In some embodiments, each vertically-oriented bit line select transistor is formed from a polycrystalline semiconductor material such as polysilicon, an epitaxial growth silicon, a polycrystalline silicon-germanium alloy, polygermanium or any other suitable material. Alternatively, vertically-oriented bit line select transistors Q_{11} - Q_{33} may be formed from a wide band-gap semiconductor material, such as ZnO, InGaZnO, or SiC, which may provide a high breakdown voltage, and typically may be used to provide junctionless FETs. Persons of ordinary skill in the art will understand that other materials may be used.

[00103] In some embodiments, each vertically-oriented bit line select transistor Q_{11} - Q_{33} may include a first region (e.g., p+ polysilicon), a second region (e.g., intrinsic polysilicon) and a third region (e.g., p+ polysilicon) to form drain/source, body, and source/drain regions, respectively, of a vertical FET. For example, a heavily doped p+ polysilicon layer 402 may be deposited on planar surface 400. P+ silicon may be either deposited and doped by ion implantation or may be doped in situ during deposition to form p+ polysilicon layer 402.

[00104] For example, an intrinsic silicon layer may be deposited on planar surface 400, and a blanket p-type implant may be employed to implant boron a predetermined depth within the intrinsic silicon layer. Example implantable molecular ions include BF_2 , BF_3 , B and the like. In some embodiments, an implant dose of about $1\text{-}10 \times 10^{13}$ ions/cm² may be employed. Other implant species and/or doses may be used. Further, in some embodiments, a diffusion process may be employed. In an embodiment, the resultant p+ polysilicon layer 402 has a thickness of from about 5 nm to about 30 nm, although other layer thicknesses may be used.

[00105] Following formation of p+ polysilicon layer 402, an intrinsic (undoped) or lightly doped polysilicon layer 404 is deposited on p+ polysilicon layer 402. In some embodiments, intrinsic layer 404 is in an amorphous state as deposited. In other embodiments, intrinsic layer 404 is in a polycrystalline state as deposited. CVD or another suitable process may be employed to deposit intrinsic layer 404. In an embodiment, intrinsic layer 404 has a

thickness between about 100 nm to about 300 nm, although other layer thicknesses may be used.

[00106] After deposition of intrinsic layer 404, a p⁺ polysilicon layer 406 may be formed over intrinsic layer 404. P-type silicon may be either deposited and doped by ion implantation or may be doped in situ during deposition to form a p⁺ polysilicon layer 406.

[00107] For example, an intrinsic silicon layer may be deposited on intrinsic layer 404, and a blanket p-type implant may be employed to implant boron a predetermined depth within the intrinsic silicon layer. Example implantable molecular ions include BF₂, BF₃, B and the like. In some embodiments, an implant dose of about $1\text{--}10 \times 10^{13}$ ions/cm² may be employed. Other implant species and/or doses may be used. Further, in some embodiments, a diffusion process may be employed. In an embodiment, the resultant p⁺ polysilicon layer 406 has a thickness of from about 5 nm to about 30 nm, although other p-type silicon layer sizes may be used.

[00108] Following formation of p⁺ polysilicon layer 406, silicon layers 402, 404 and 406 are patterned and etched to form rows of semiconductor material. For example, silicon layers 402, 404 and 406 may be patterned and etched using conventional lithography techniques, with wet or dry etch processing.

[00109] Silicon layers 402, 404 and 406 may be patterned and etched in a single pattern/etch procedure or using separate pattern/etch steps. Any suitable masking and etching process may be used to form semiconductor rows. For example, silicon layers may be patterned with about 0.1 to about 1.5 micron of photoresist ("PR") using standard photolithographic techniques. Thinner PR layers may be used with smaller critical dimensions and technology nodes. In some embodiments, an oxide hard mask may be used below the PR layer to improve pattern transfer and protect underlying layers during etching.

[00110] In some embodiments, after etching, the semiconductor rows may be cleaned using a dilute hydrofluoric/sulfuric acid clean. Such cleaning may be performed in any suitable cleaning tool, such as a Raider tool, available from Semitool of Kalispell, Montana. Example post-etch cleaning may include using ultra-dilute sulfuric acid (e.g., about 1.5 1.8 wt%) for about 60 seconds and/or ultra-dilute hydrofluoric ("HF") acid (e.g., about 0.4-0.6

wt%) for 60 seconds. Megasonics may or may not be used. Other clean chemistries, times and/or techniques may be employed.

[00111] A gate dielectric material layer 314 is deposited conformally over substrate 302, and forms on sidewalls of the semiconductor rows. For example, between about 3 nm to about 10 nm of silicon dioxide may be deposited. Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric material layer thicknesses may be used.

[00112] Gate electrode material is deposited over the semiconductor rows and gate dielectric material layer 314 to fill the voids between the semiconductor rows. For example, approximately 10 nm to about 20 nm of titanium nitride or other similar metal, a highly-doped semiconductor, such as n⁺ polysilicon, p⁺ polysilicon, or other similar conductive material may be deposited. The as-deposited gate electrode material is subsequently etched back to form row select lines SG₁, SG₂, SG₃.

[00113] In an embodiment, silicon layers 402, 404 and 406 in the semiconductor rows are patterned and etched to form vertical transistor pillars disposed above global bit lines GBL₁, GBL₂, GBL₃. The vertical transistor pillars will be used to form vertically-oriented bit line select transistors Q₁₁-Q₃₃. In an embodiment, gate dielectric material layer 314 also is etched at the same time to trim gate dielectric material layers 314 to the same width as the vertical transistor pillars.

[00114] A second dielectric material layer 310 is deposited over substrate 302. For example, approximately 500 nm to about 800 nm of silicon dioxide may be deposited and planarized using chemical mechanical polishing or an etch-back process to form planar top surface 408, resulting in the structure shown in FIGS. 4A1-4A3. Other dielectric materials and/or thicknesses may be used.

[00115] Planar surface 408 includes exposed top surfaces of vertically-oriented bit line select transistors Q₁₁-Q₃₃ and gate dielectric material layer 314 separated by second dielectric material layer 310. Other dielectric materials such as silicon nitride, silicon oxynitride, low K dielectrics, etc., and/or other dielectric material layer thicknesses may be used. Example low K dielectrics include carbon doped oxides, silicon carbon layers, or the like.

[00116] A first etch stop layer 316 is formed over planar top surface 408. First etch stop layer 316 may include any suitable etch stop layer formed by any suitable method (e.g., CVD, PVD, etc.). In an embodiment, first etch stop layer 316 may include between about 5 nm and about 50 nm of silicon nitride. Other etch stop layer materials and/or thicknesses may be used.

[00117] A stack of alternating layers of third dielectric material layer 318 and conductive material layer 410 are formed over planar top surface 408. Third dielectric material layers 318 may be silicon dioxide or other dielectric material formed by any suitable method (e.g., CVD, PVD, etc.). Conductive material layer 410 may be titanium nitride, tungsten, tantalum nitride, or other similar conductive material formed by any suitable method (e.g., CVD, PVD, etc.).

[00118] In an embodiment, each third dielectric material layer 318 may be between about 5 nm and about 25 nm of SiO₂, and each conductive material layer 410 may be between about 5 nm and about 30 nm of titanium nitride. Other dielectric materials and/or thicknesses, and/or other first electrically conductive materials and/or thicknesses may be used. In an embodiment, five conductive material layers 410 are formed over substrate 302. More or fewer than five conductive material layers 410 may be used.

[00119] Next, a second etch stop layer 320 is formed over substrate 302, resulting in the structure shown in FIGS. 4B1-4B2. Second etch stop layer 320 may include any suitable etch stop layer formed by any suitable method (e.g., CVD, PVD, etc.). In an embodiment, second etch stop layer 320 may be between about 5 nm and about 50 nm of polysilicon. Other etch stop layer materials and/or thicknesses may be used.

[00120] Next, second etch stop layer 320, third dielectric material layers 318, and conductive material layers 410 are patterned and etched to form rows 412, with voids 414 separating rows 412, resulting in the structure shown in FIGS. 4C1-4C3. Each of rows 412 may be between about 20 nm and about 100 nm wide, although other widths may be used. Voids 414 may be between about 10 nm and about 80 nm wide, although other widths may be used.

[00121] A sacrificial material 416 is deposited over substrate 302, filling voids 414 between rows 412. Sacrificial material layers 416 may include any suitable sacrificial

material layers formed by any suitable method (e.g., CVD, PVD, etc.). For example, approximately 300-700 nm of amorphous silicon may be deposited on the substrate 302 and planarized using chemical mechanical polishing or an etchback process to form a planar surface 418, resulting in the structure shown in FIGS. 4D1-4D3. Other sacrificial materials may be used. Sacrificial material 416 is patterned and etched to form holes 420 separating pillar-shaped sacrificial material 416, resulting in the structure shown in FIGS. 4E1-4E3.

[00122] Next, a barrier material layer 334 is deposited conformally over substrate 302, and forms on sidewalls of holes 420. For example, between about 3 nm to about 10 nm of silicon nitride may be deposited. Other barrier materials and/or other dielectric material layer thicknesses may be used. An anisotropic etch is used to remove lateral portions of barrier material layer 334, leaving only sidewall portions of barrier material layer 334.

[00123] A fourth dielectric material layer 332 is deposited over substrate 302, and fills holes 420. For example, approximately 300-700 nm of silicon dioxide may be deposited on the substrate 302 and planarized using chemical mechanical polishing or an etchback process to form a planar surface 422, resulting in the structure shown in FIGS. 4F1-4F3.

[00124] An etch is used to remove sacrificial material layers 416 to form holes 426. In an embodiment, a wet etch may be used to remove sacrificial material layers 416. In other embodiments, wet and/or dry etch chemistries may be used to remove sacrificial material layers 416.

[00125] Next, an etch is performed via holes 426 to form recesses 326 at ends of each conductive material layer 410, resulting in the structure shown in FIGS. 4G1-4G2. Each of recesses 326 may have a depth D of between about 5 nm and about 25 nm, although other depths may be used. In an embodiment, a wet etch is used to form recesses 326. In an embodiment, a mixed acid wet etch chemistry (e.g., 20:1:1:1 $\text{H}_3\text{PO}_4/\text{HNO}_3/\text{CH}_3\text{COOH}/\text{H}_2\text{O}$) for about 5 minutes to about 25 minutes is used to form recesses 326. Other etch chemistries and etch durations may be used.

[00126] A conductive oxide material layer 324 is selectively deposited on conductive material layer 410, filling recesses 326, resulting in the structure shown in FIG. 4H1-4H3. In an embodiment, conductive oxide material layer 324 is between about 5 nm and about 25 nm of a conductive oxide material, such as titanium oxide, nickel oxide, hafnium oxide, tantalum

oxide, tungsten oxide, or other similar conductive oxide material, or combination thereof. Other thicknesses may be used. Conductive oxide material layer 324 may be selectively deposited by any suitable method (e.g., CVD, PVD, etc.).

[00127] FIGS. 4H4-4H7 depict various selective deposition techniques that may be used to form conductive oxide material layer 324 on conductive material layer 410, filling recesses 326. For simplicity, in the examples depicted in FIGS. 4H4-4H7, third dielectric material 318 is SiO₂, conductive oxide material layer 324 is TiO₂, conductive material layer 410 is TiN.

[00128] In one embodiment, conductive oxide material (e.g., TiO₂) layer 324 is selectively grown from conductive material (e.g., TiN) layer 410 in a single step to fill recesses 326, such as depicted in FIG. 4H4.

[00129] In another embodiment, conductive oxide material (e.g., TiO₂) layer 324 is selectively grown from conductive material (e.g., TiN) layer 410 in a deposition-etch-deposition-etch process. In particular, the deposition of TiO₂ layer 324 is controlled to stop just before TiO₂ material begins to grow on third dielectric material (e.g., SiO₂) layer 318. An etch (e.g., using HCl, NF₃, or other similar etchant) is applied to remove TiO₂ precursors from SiO₂ layer 318. The TiO₂ deposition-etch process is repeated until TiO₂ layer 324 fills recesses 326, such as depicted in FIG. 4H5.

[00130] In another embodiment, conductive oxide material (e.g., TiO₂) layer 324 is selectively grown from conductive material (e.g., TiN) layer 410 in a deposition-surface-clean-deposition-surface-clean process. In particular, the deposition of TiO₂ layer 324 is controlled to stop just before TiO₂ material begins to grow on third dielectric material (e.g., SiO₂) layer 318. The surface of SiO₂ layer 318 is then reset using a wet process (e.g., dilute hydrofluoric acid, SC-1, SC-2). The TiO₂ deposition-surface-cleaning process is repeated until TiO₂ layer 324 fills recesses 326, such as depicted in FIG. 4H6.

[00131] In still another embodiment, conductive oxide material (e.g., TiO₂) layer 324 is selectively grown from conductive material (e.g., TiN) layer 410 in a deposition-anneal-surface-clean-deposition-anneal-surface-clean process. In particular, the deposition of TiO₂

layer 324 is controlled to stop just before TiO₂ material begins to grow on third dielectric material (e.g., SiO₂) layer 318. An anneal process (e.g., between about 100 °C and about 400 °C for about 50 cycles to about 250 cycles) is used to densify the deposited TiO₂ material. Following the anneal, the surface of SiO₂ layer 318 is then reset using a wet process (e.g., dilute hydrofluoric acid, SC-1, SC-2). The TiO₂ deposition-anneal-surface-clean process is repeated until TiO₂ layer 324 fills recesses 326, such as depicted in FIG. 4H7.

[00132] A semiconductor material layer 322 is deposited conformally over substrate 302. In an embodiment, semiconductor material layer 322 has a thickness between about 3 nm and about 15 nm, and includes one or more of carbon, germanium, silicon, tantalum nitride, tantalum silicon nitride, or other similar semiconductor material. In embodiments, semiconductor material layer 322 may be amorphous, polycrystalline, nano-crystalline, or single crystalline, and may be formed by CVD, PVD, ALD, atomic layer deposition nanolaminates, or other method. Semiconductor material layer 322 and conductive oxide material layer 324 constitute a non-volatile memory material 214. In an embodiment, non-volatile memory material 214 includes a barrier modulated switching structure.

[00133] An adhesion material layer 330 is deposited conformally over substrate 302, resulting in the structure shown in FIGS. 4I1-4I2. In an embodiment, semiconductor material layer 322 is titanium nitride and has a thickness between about 3 nm and about 15 nm. Other adhesion materials and/or thicknesses may be used.

[00134] An anisotropic etch is used to remove lateral portions of semiconductor material layer 322 and adhesion material layer 330, leaving only sidewall portions of semiconductor material layer 322 and adhesion material layer 330. First etch stop layer 316 is then patterned and etched to expose top surfaces of bit line select transistors Q₁₁-Q₃₁. A conductive material 328 (e.g., titanium nitride, tantalum nitride, titanium carbide, tantalum carbide, or other conductive material) is deposited over substrate 302, forming vertical bit lines LBL₁₁-LBL₃₃. A non-conductive material (e.g., amorphous silicon) is deposited over substrate, forming cores 336 within vertical bit lines LBL₁₁-LBL₃₃. The structure is then planarized using chemical mechanical polishing or an etch-back process, resulting in the structure shown in FIGS. 4J1-4J2.

[00135] Thus, as described above, one embodiment of the disclosed technology includes a method that includes forming a word line above a substrate, the word line disposed in a first direction, forming a bit line above the substrate, the bit line disposed in a second direction perpendicular to the first direction, forming a nonvolatile memory material between the word line and the bit line by selectively forming a conductive oxide material layer adjacent the word line, and forming a semiconductor material layer adjacent the bit line, and forming a memory cell comprising the nonvolatile memory material at an intersection of the bit line and the word line.

[00136] One embodiment of the disclosed technology includes a method including forming a word line layer above a substrate, the word line layer disposed in a first direction, etching a recess in the word line layer, selectively forming a conductive oxide material layer in the recess, forming a dielectric material above the substrate, forming a hole in the dielectric material, the hole disposed in a second direction perpendicular to the first direction, forming a semiconductor material layer on a sidewall of the hole, forming a local bit line in the hole, and forming a memory cell including the conductive oxide material layer and the semiconductor material layer at an intersection of the local bit line and the word line layer.

[00137] One embodiment of the disclosed technology includes a method of forming a monolithic three-dimensional memory array, the method including forming a stack of conductive material layers above a substrate, etching the stack of conductive material layers to form a row of conductive material layers, etching a recess in each of the conductive material layers, selectively forming a conductive oxide material layer in each of the recesses, forming a dielectric material above a substrate and adjacent the row of conductive material layers, forming a hole in the dielectric material, the hole disposed adjacent the row of conductive material layers, forming a semiconductor material layer on a sidewall of the hole adjacent the conductive oxide material in each of the recesses, forming a local bit line in the hole, and forming an array of memory cells, each memory cell including the conductive oxide material layer and the semiconductor material layer at an intersection of the local bit line and a corresponding one of the conductive material layers.

[00138] For purposes of this document, each process associated with the disclosed technology may be performed continuously and by one or more computing devices. Each step in a process may be performed by the same or different computing devices as those used in other steps, and each step need not necessarily be performed by a single computing device.

[00139] For purposes of this document, reference in the specification to “an embodiment,” “one embodiment,” “some embodiments,” or “another embodiment” may be used to described different embodiments and do not necessarily refer to the same embodiment.

[00140] For purposes of this document, a connection can be a direct connection or an indirect connection (e.g., via another part).

[00141] For purposes of this document, the term “set” of objects may refer to a “set” of one or more of the objects.

[00142] Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims.

CLAIMS

1. A method comprising:
 - forming a word line above a substrate, the word line disposed in a first direction;
 - forming a bit line above the substrate, the bit line disposed in a second direction perpendicular to the first direction;
 - forming a nonvolatile memory material between the word line and the bit line by selectively forming a conductive oxide material layer adjacent the word line, and forming a semiconductor material layer adjacent the bit line; and
 - forming a memory cell comprising the nonvolatile memory material at an intersection of the bit line and the word line.
2. The method of claim 1, further comprising:
 - forming a plurality of word lines above the substrate, each of the word lines disposed in the first direction; and
 - forming a plurality of memory cells comprising the nonvolatile memory material, each of the memory cells formed at an intersection of the bit line and a corresponding one of the word lines.
3. The method of claim 1, further comprising:
 - forming a plurality of bit lines above the substrate, each of the bit lines disposed in the second direction;
 - forming the nonvolatile memory material between the word line and each of the bit lines; and
 - forming a plurality of memory cells comprising the nonvolatile memory material, each of the memory cells formed at an intersection of the word line and a corresponding one of the bit lines.
4. The method of claim 1, wherein forming the word line comprises:
 - forming a conductive material layer above the substrate;
 - etching a recess in the conductive material layer; and
 - selectively forming the conductive oxide material layer in the recess.

5. The method of claim 1, further comprising:
 - etching a recess in the word line;
 - selectively forming a conductive oxide material layer in the recess;
 - forming a dielectric material above the substrate;
 - forming a hole in the dielectric material, the hole disposed in the second direction;
 - forming a semiconductor material layer on a sidewall of the hole;
 - forming the bit line in the hole; and
 - forming a memory cell comprising the conductive oxide material layer and the semiconductor material layer at an intersection of the bit line and the word line.
6. The method of claim 5, wherein selectively forming a conductive oxide material layer in the recess comprises selectively forming the conductive oxide material layer in a single step.
7. The method of claim 5, wherein selectively forming a conductive oxide material layer in the recess comprises a deposition-etch-deposition-etch process.
8. The method of claim 5, wherein selectively forming a conductive oxide material layer in the recess comprises a deposition-surface-clean-deposition-surface-clean process.
9. The method of claim 5, wherein selectively forming a conductive oxide material layer in the recess comprises a deposition-anneal-surface-clean-deposition-anneal-surface-clean process.
10. The method of any preceding claim, further comprising forming a vertically-oriented transistor above the substrate, and wherein forming the bit line comprises forming the bit line above the vertically-oriented transistor.
11. The method of any preceding claim, further comprising:
 - forming a global bit line above the substrate, the global bit line disposed in a third direction perpendicular to the first direction and the second direction; and
 - forming a transistor between the bit line and the global bit line.

12. The method of claim 11, wherein the transistor comprises a vertically-oriented transistor.
13. The method of any preceding claim, wherein:
the conductive oxide material layer comprises one or more of aluminum-doped zinc oxide, aluminum-doped zirconium oxide, cerium oxide, indium tin oxide, niobium-doped strontium titanate, praseodymium calcium manganese oxide, titanium oxide, tungsten oxide, and zinc oxide; and
the semiconductor material layer comprises one or more of carbon, germanium, silicon, tantalum nitride, tantalum silicon nitride.
14. The method of any preceding claim, wherein the word line portion comprises one or more of titanium nitride, tungsten, and tantalum nitride.
15. The method of any preceding claim, wherein the bit line comprises one or more of titanium nitride, tantalum nitride, tantalum carbide, and titanium carbide.

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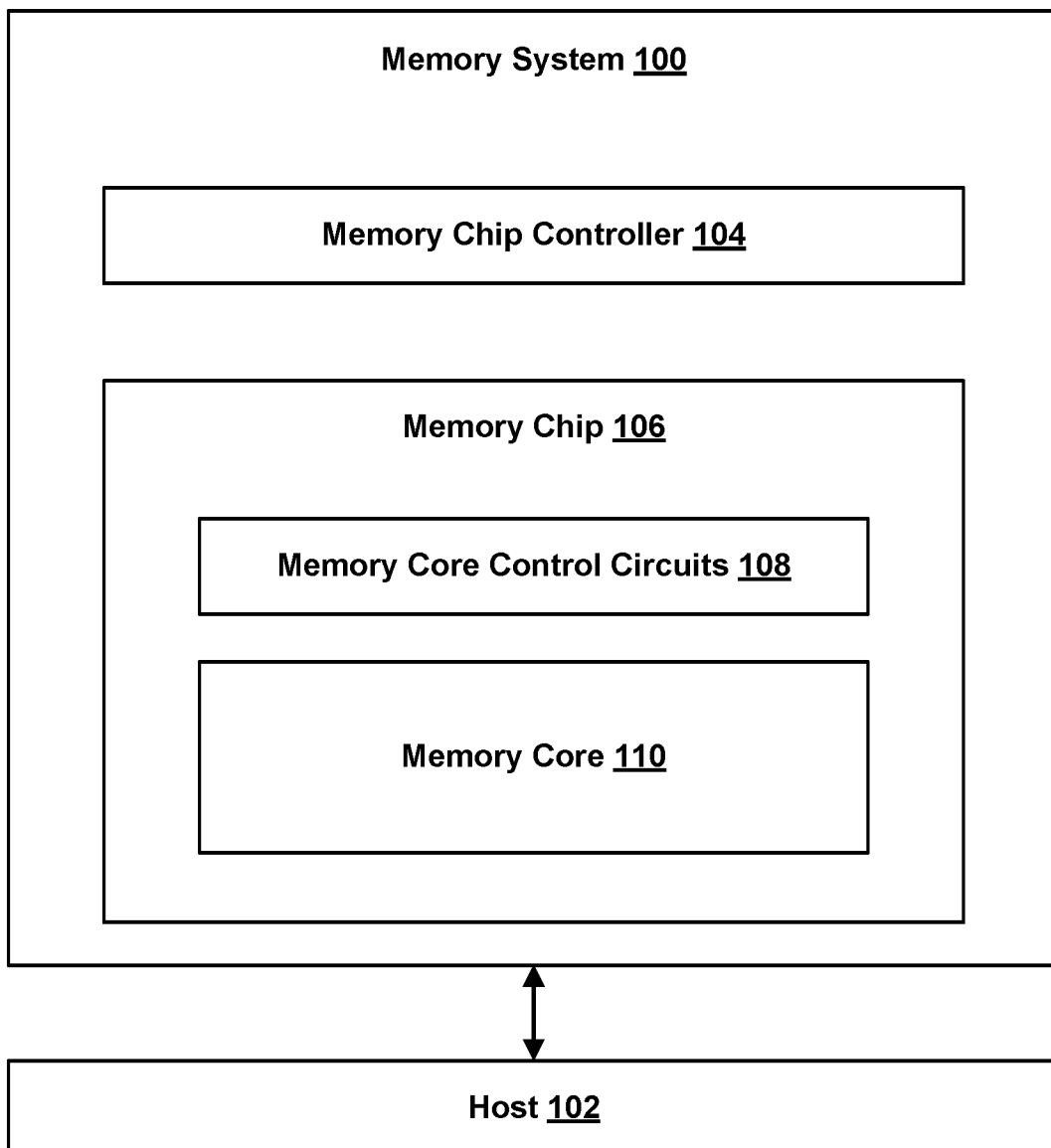


FIG. 1A

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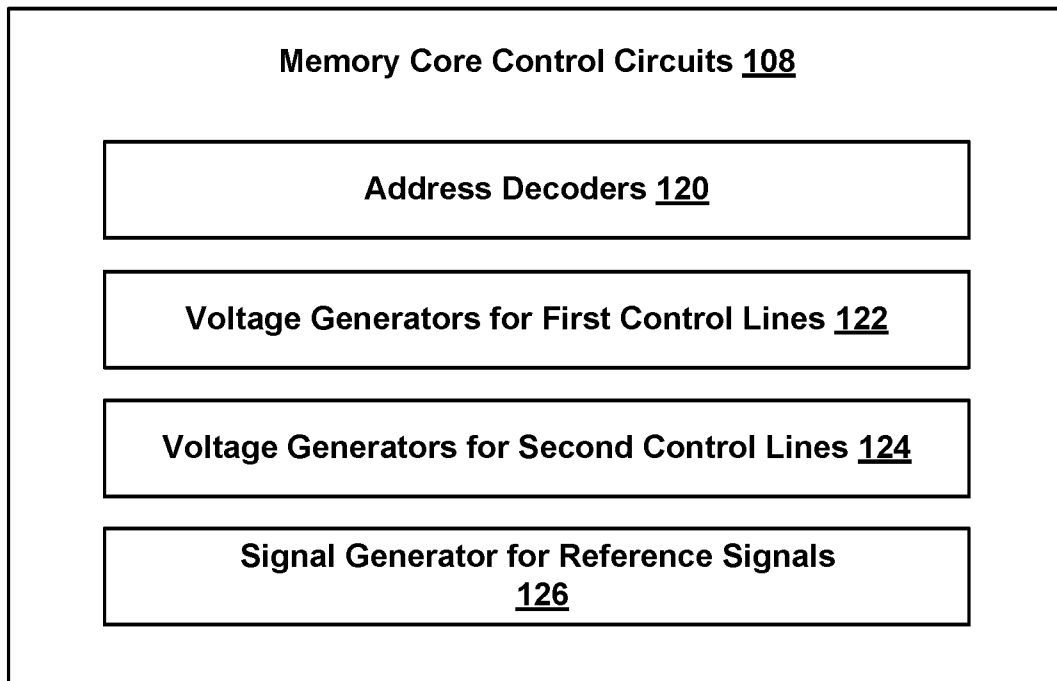


FIG. 1B

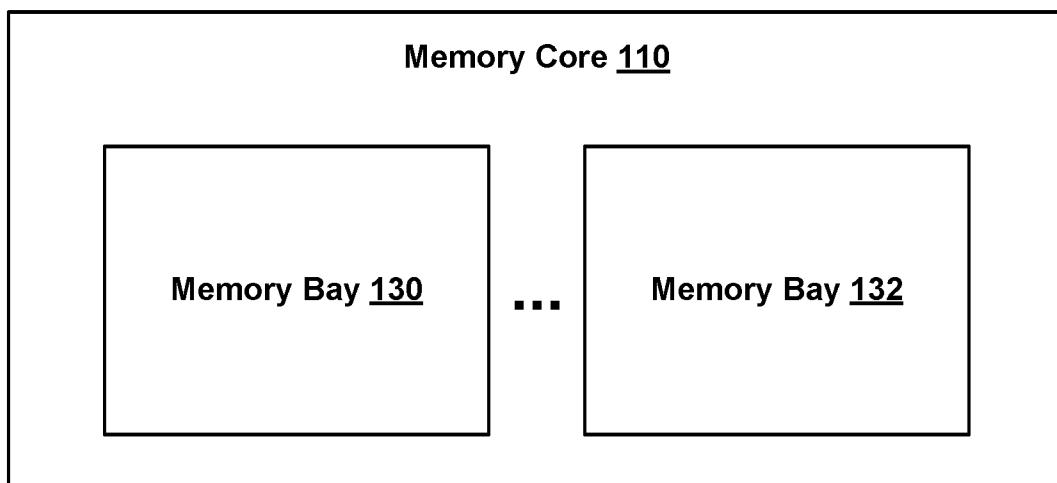


FIG. 1C

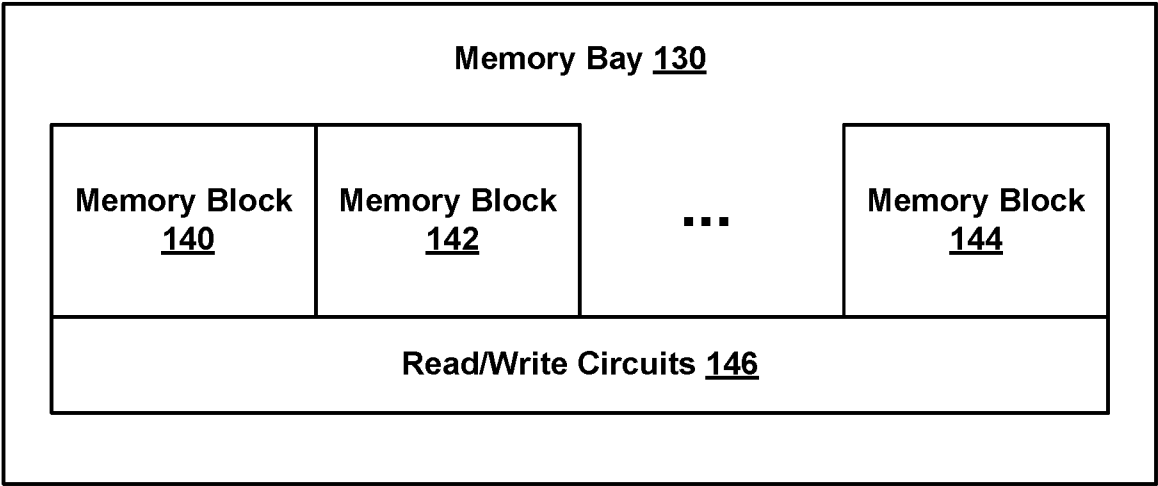


FIG. 1D

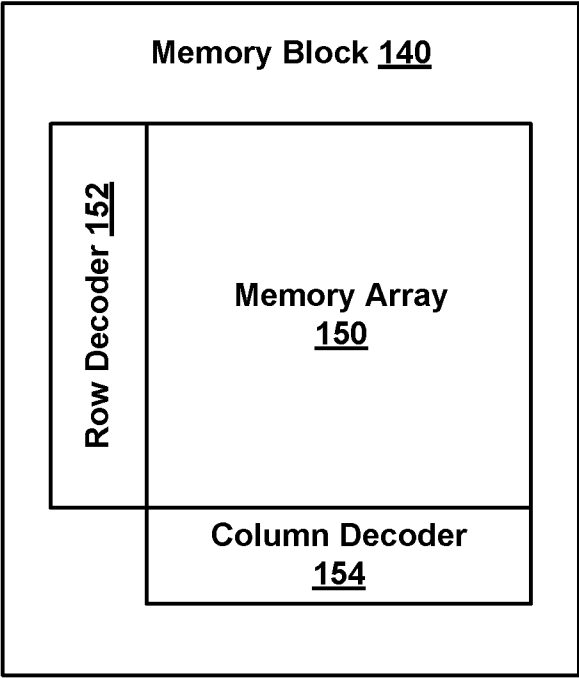


FIG. 1E

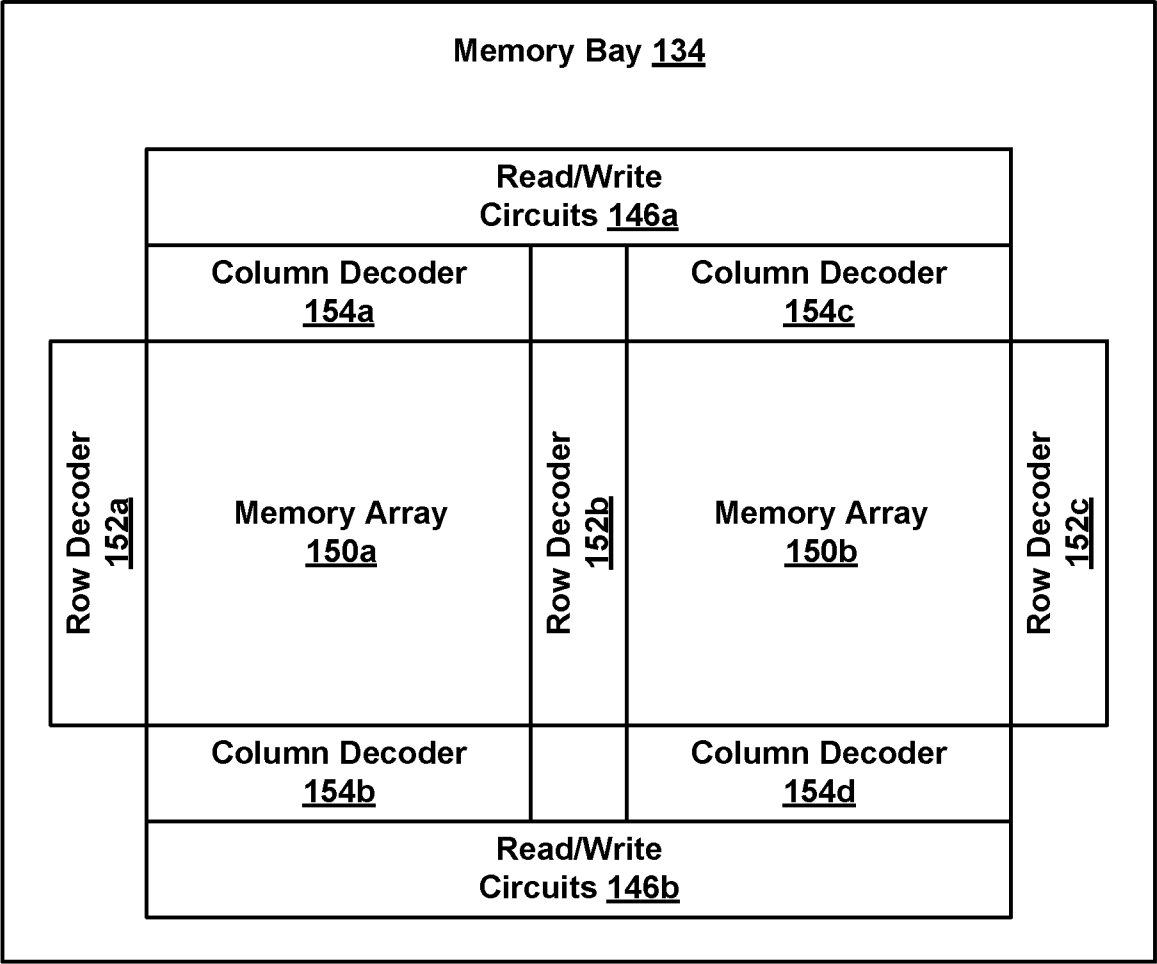


FIG. 1F

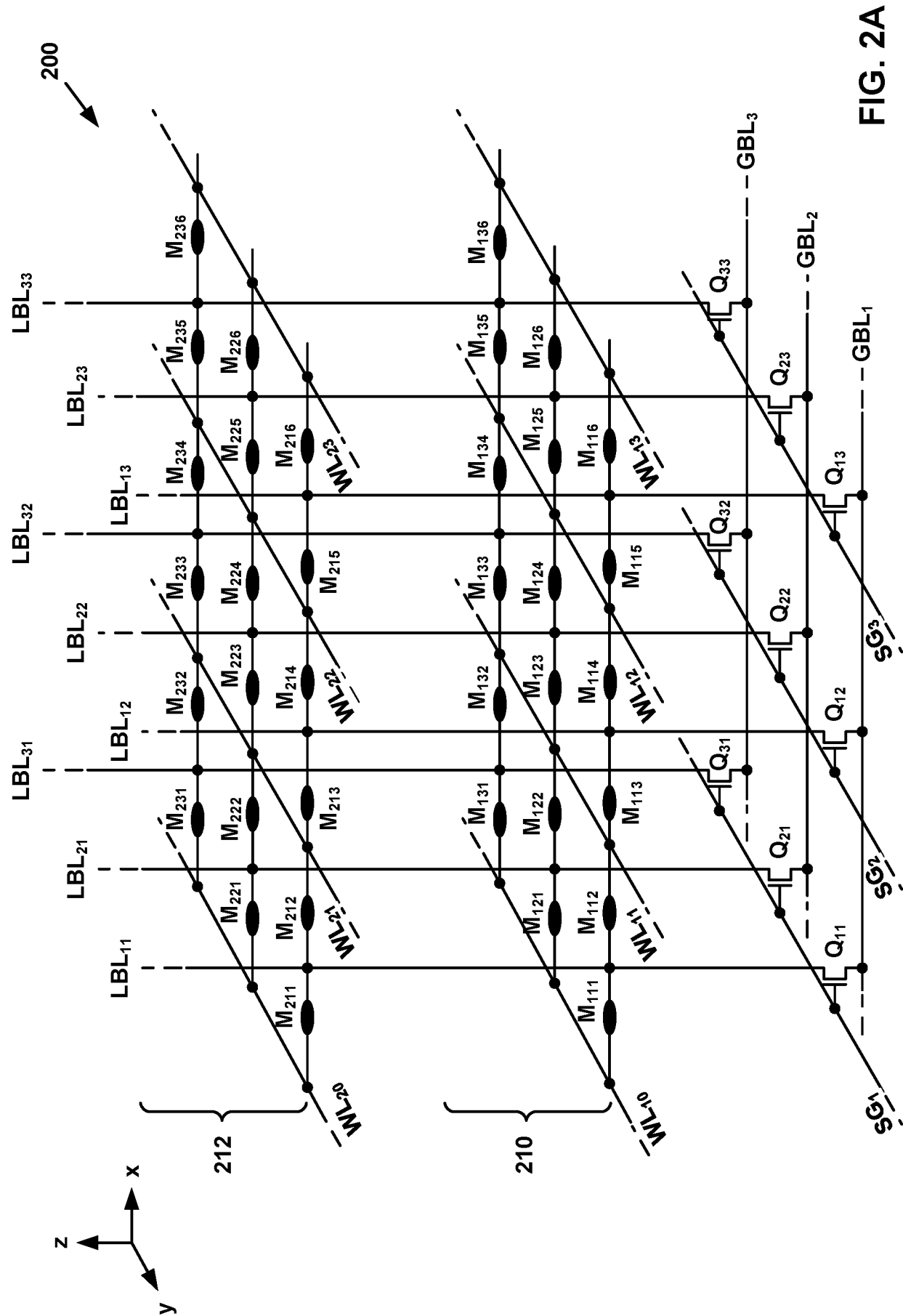


FIG. 2A

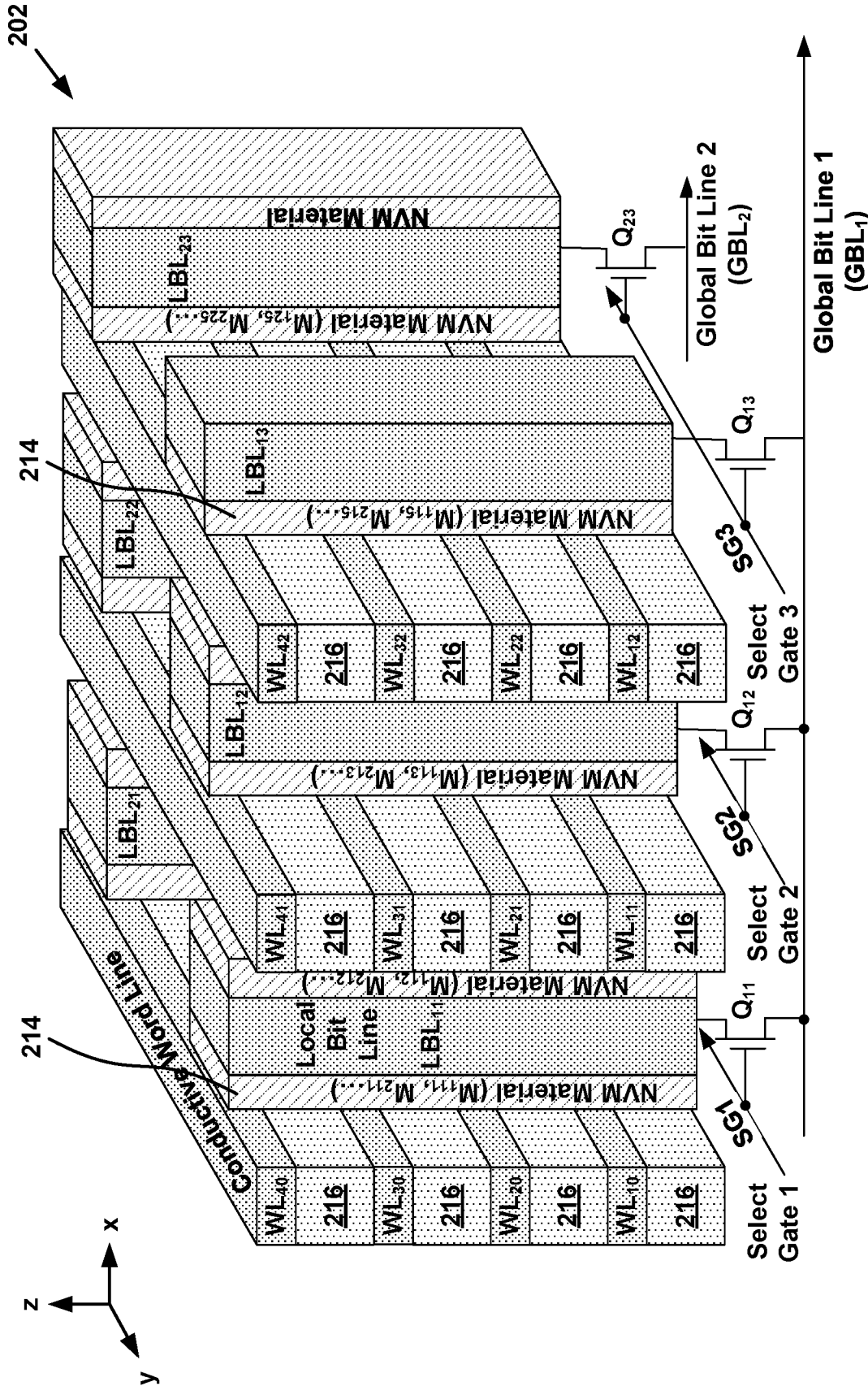


FIG. 2B

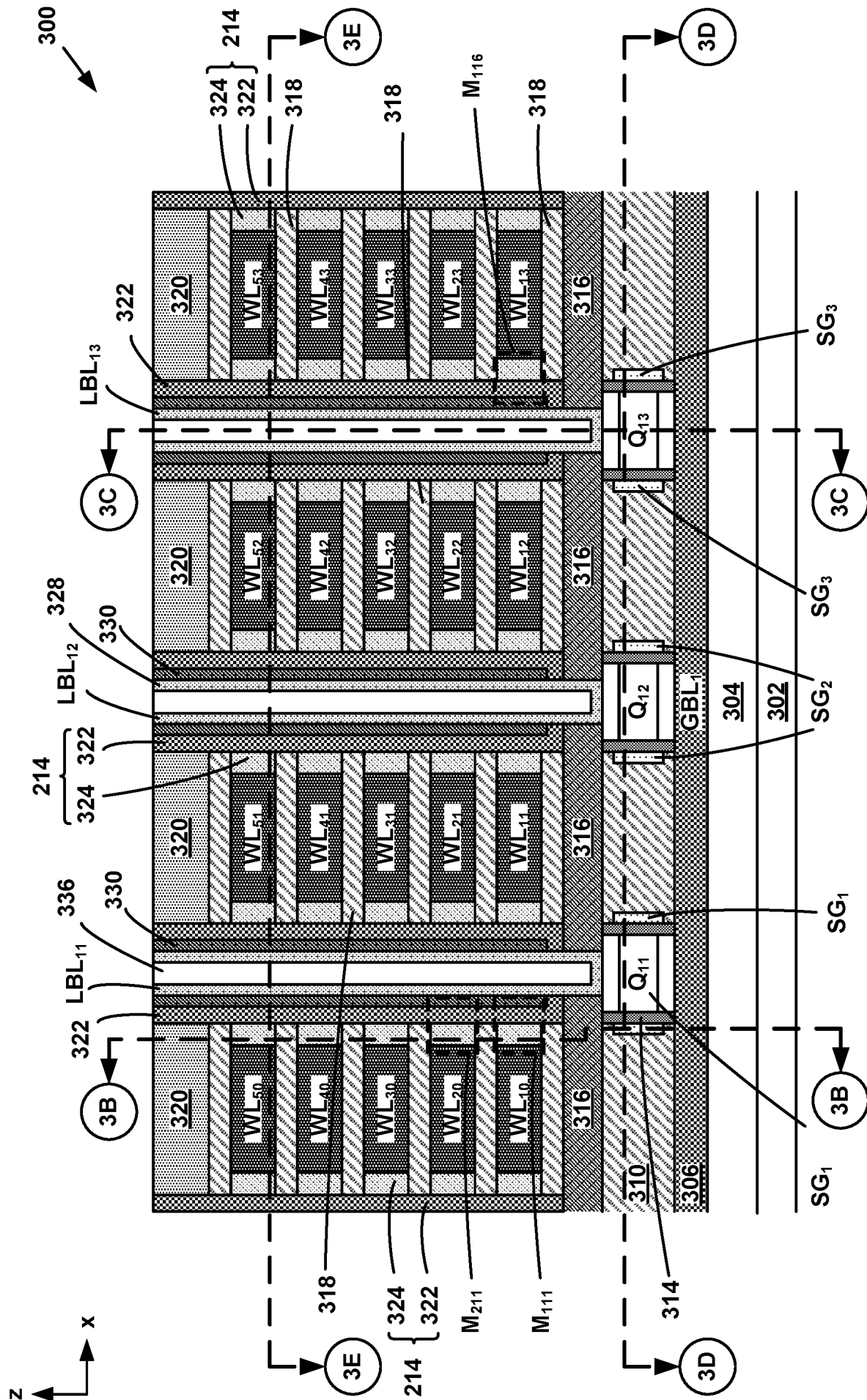


FIG. 3A

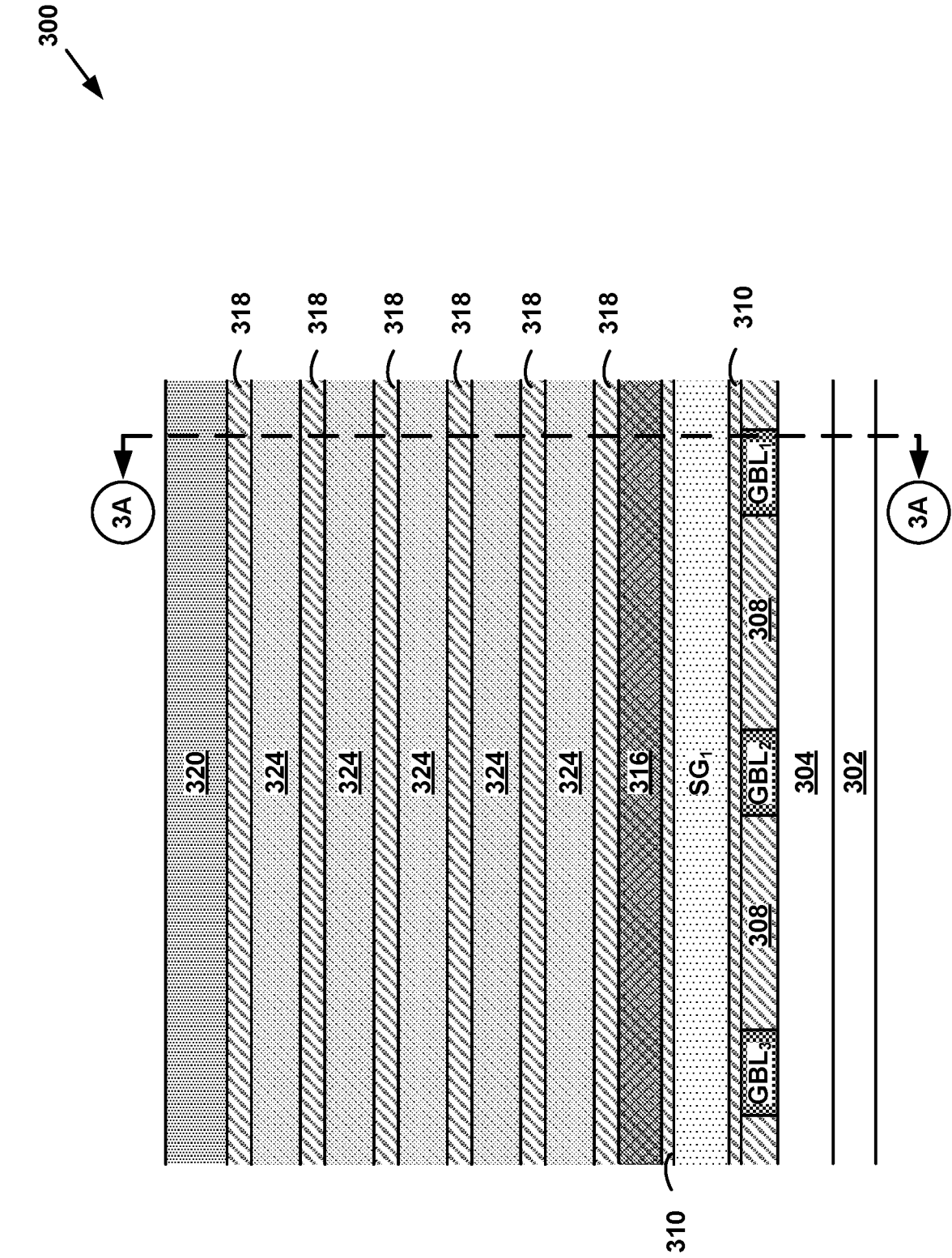


FIG. 3B

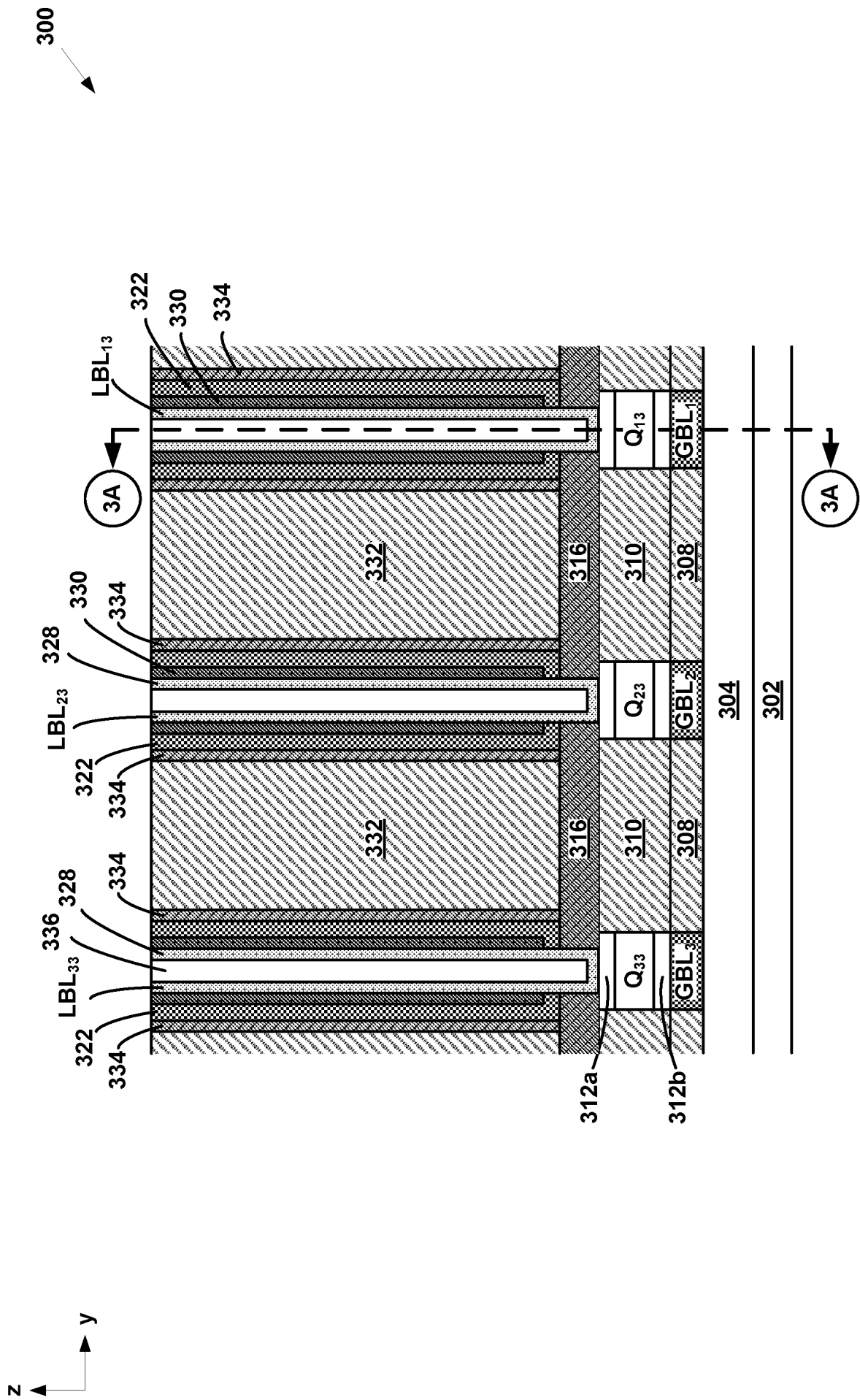


FIG. 3C

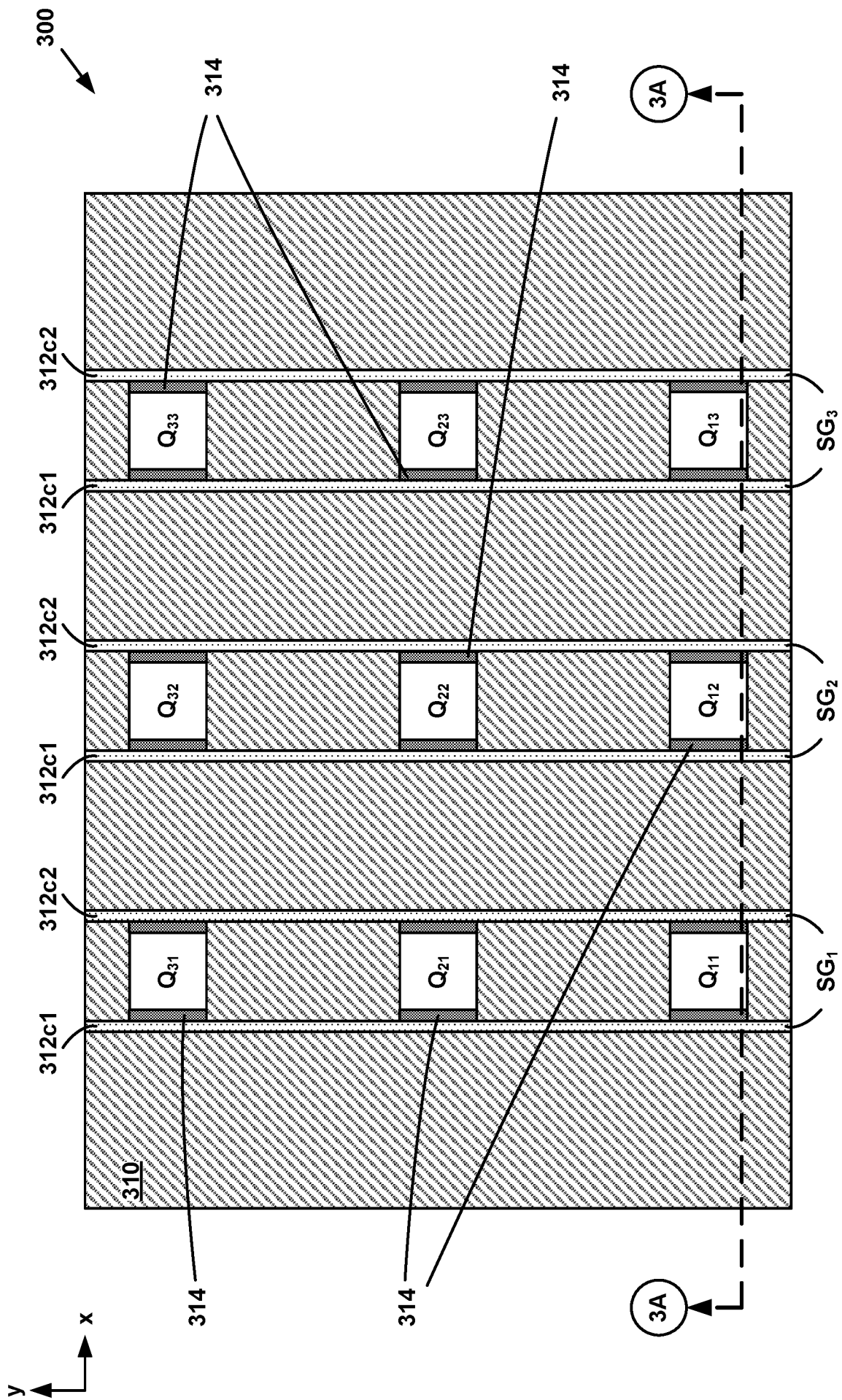


FIG. 3D

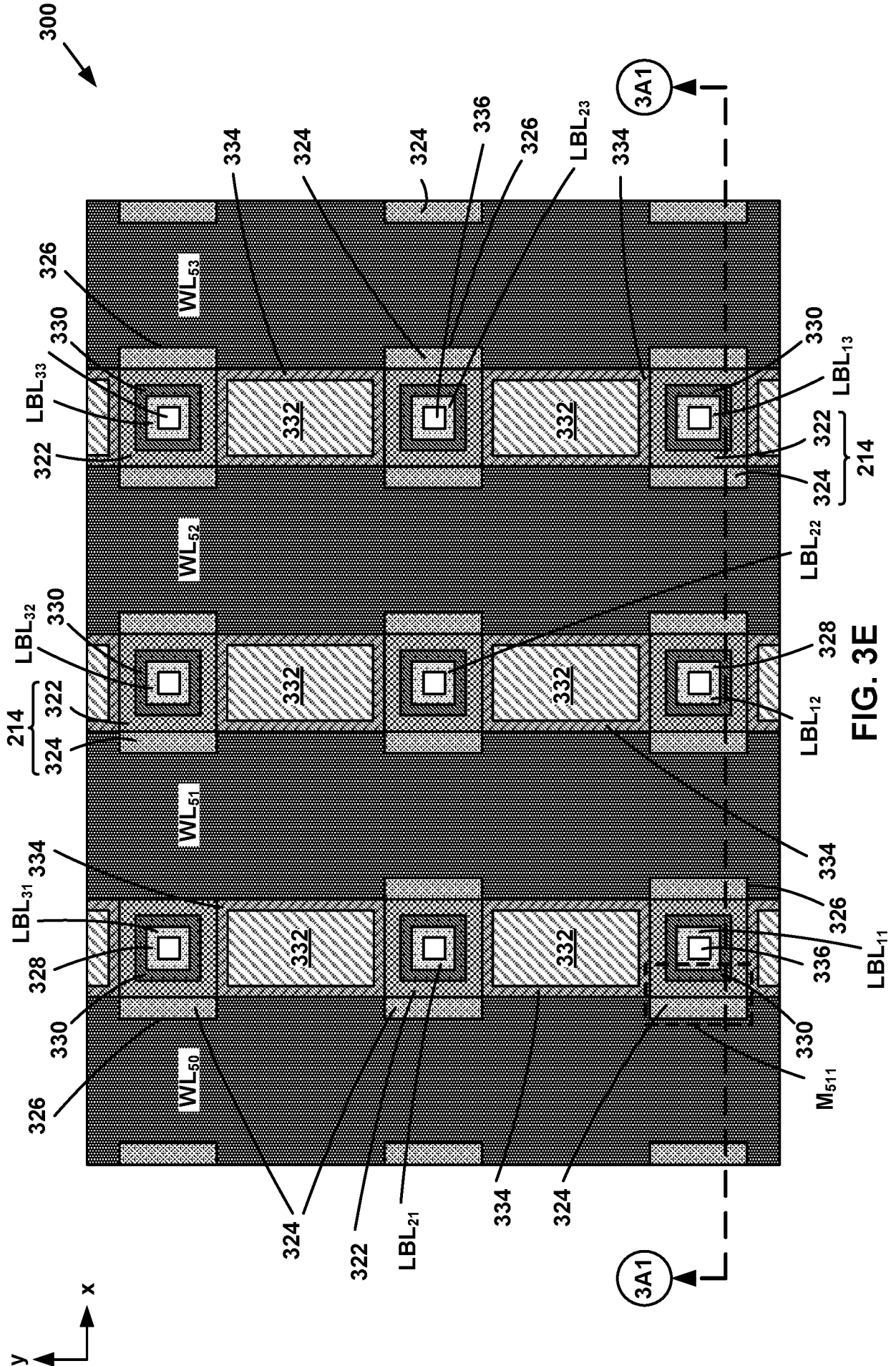


FIG. 3E

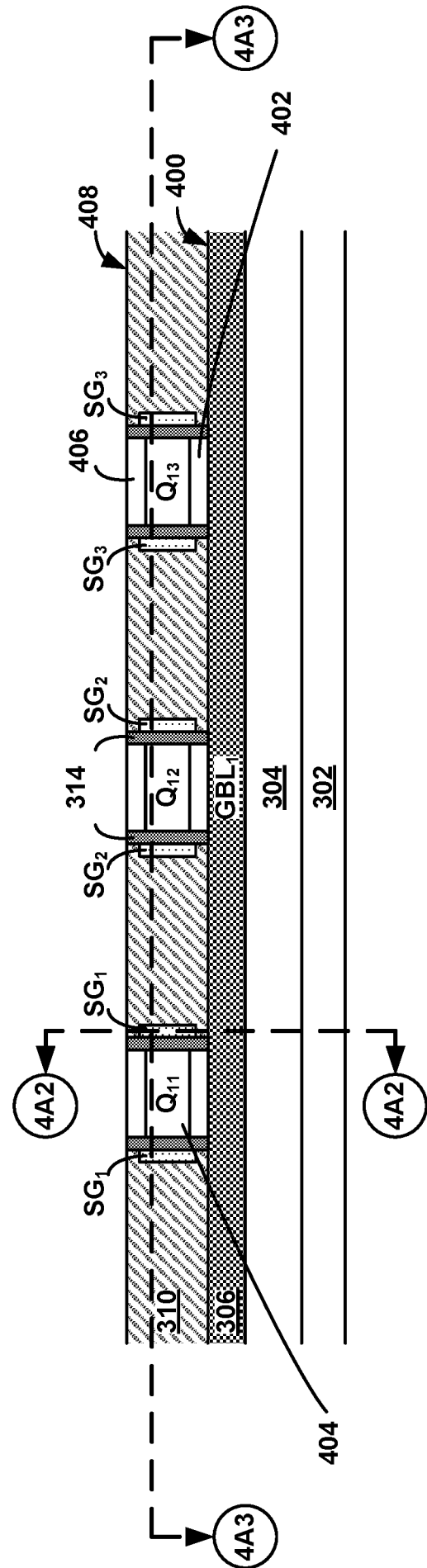
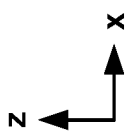


FIG. 4A1

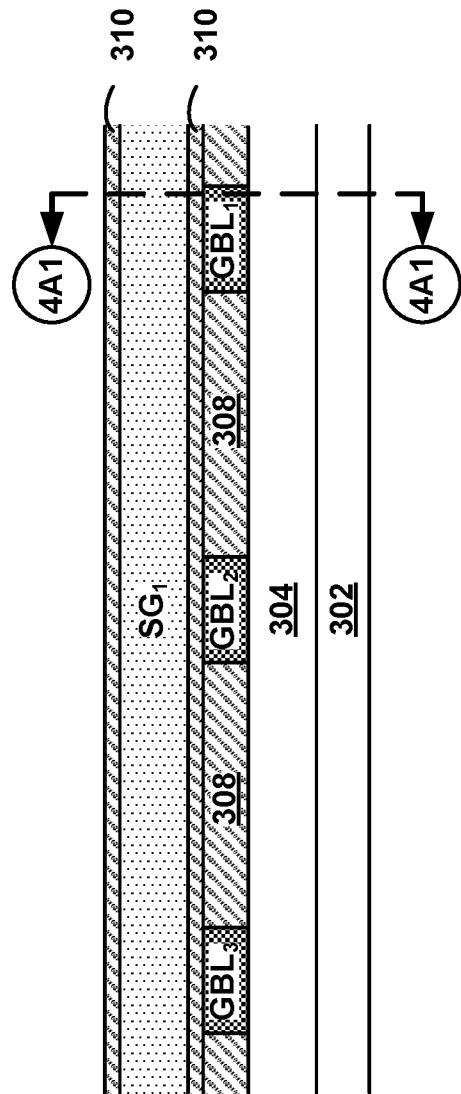
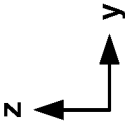


FIG. 4A2

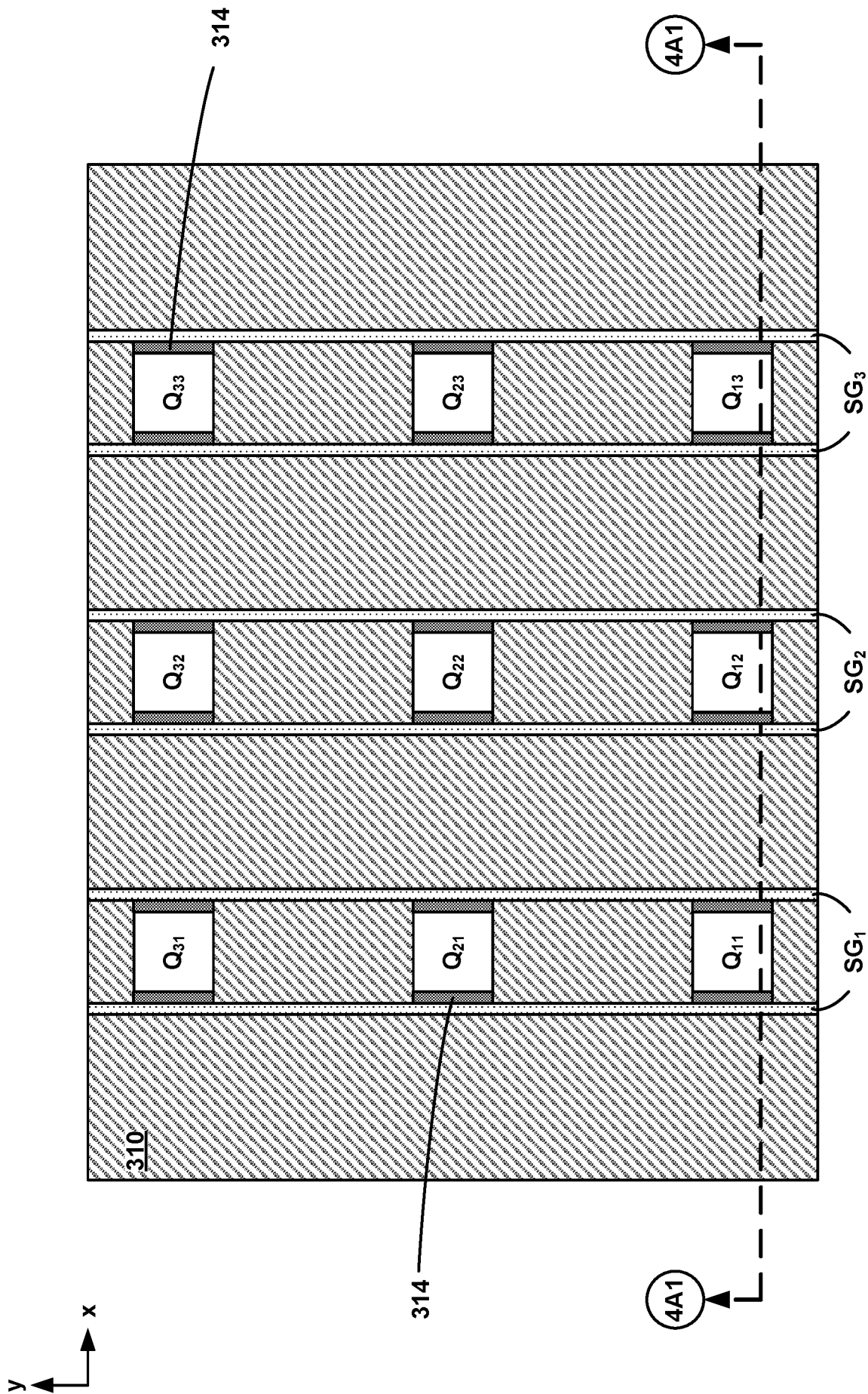
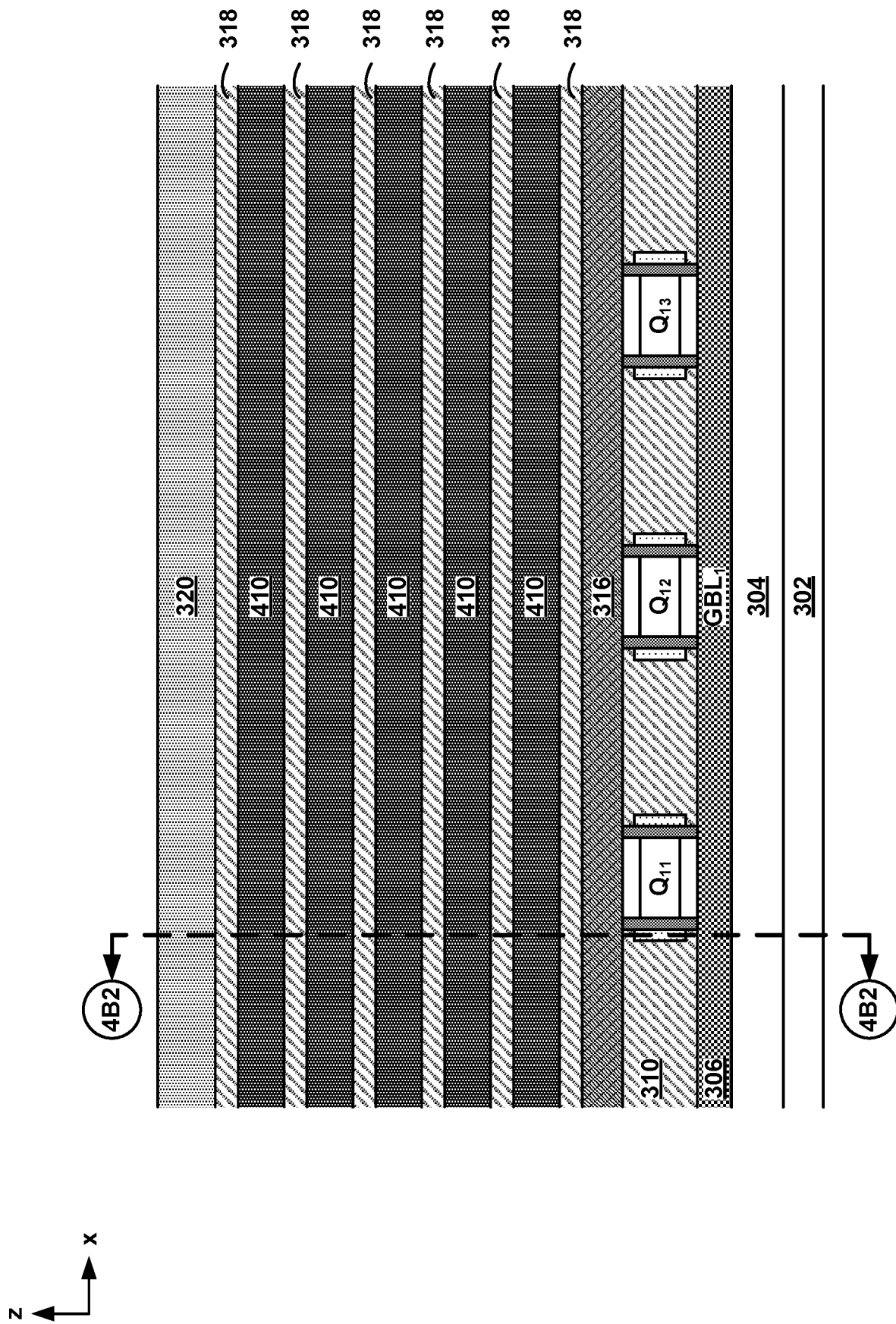


FIG. 4A3



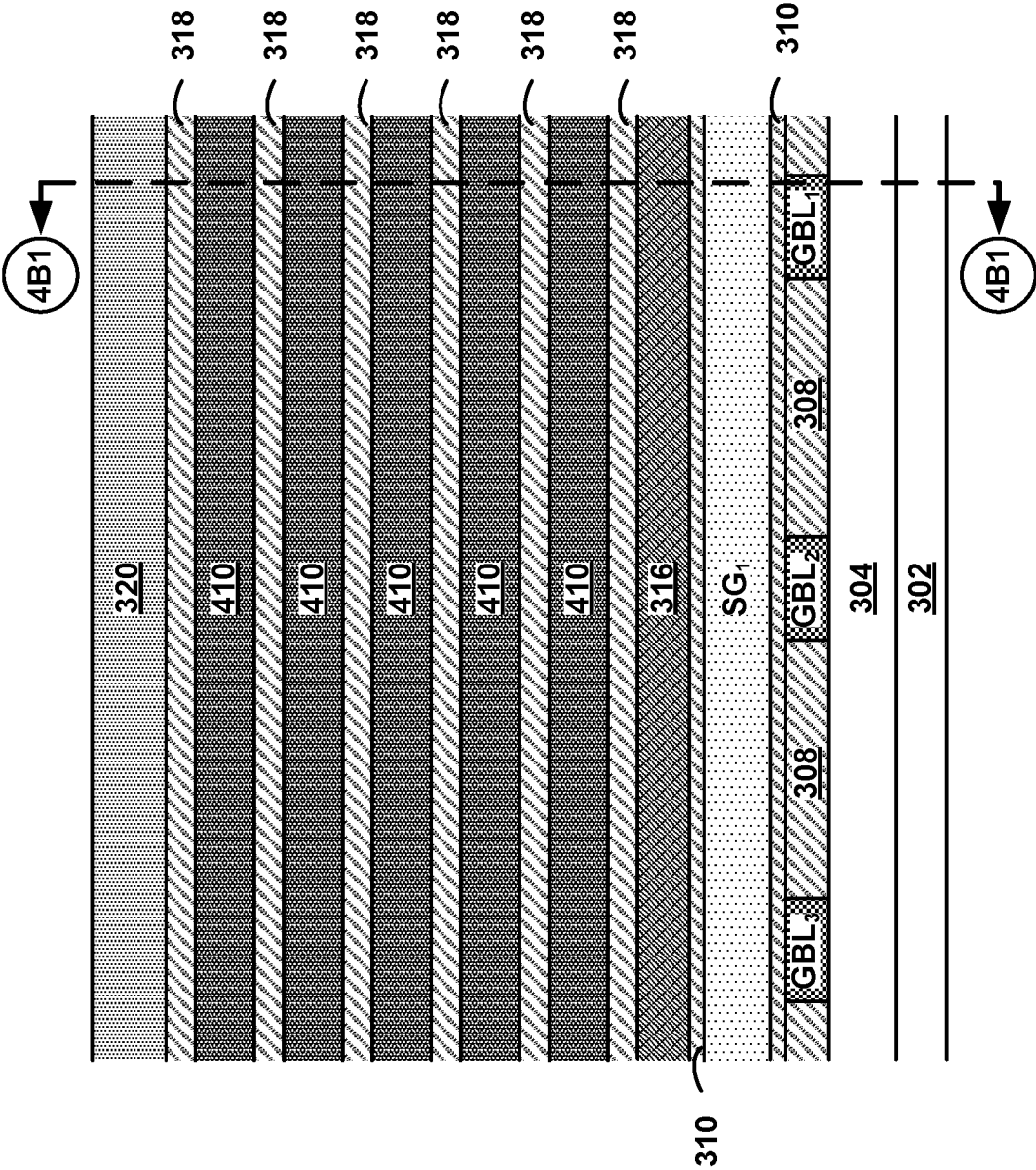
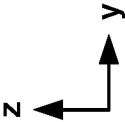
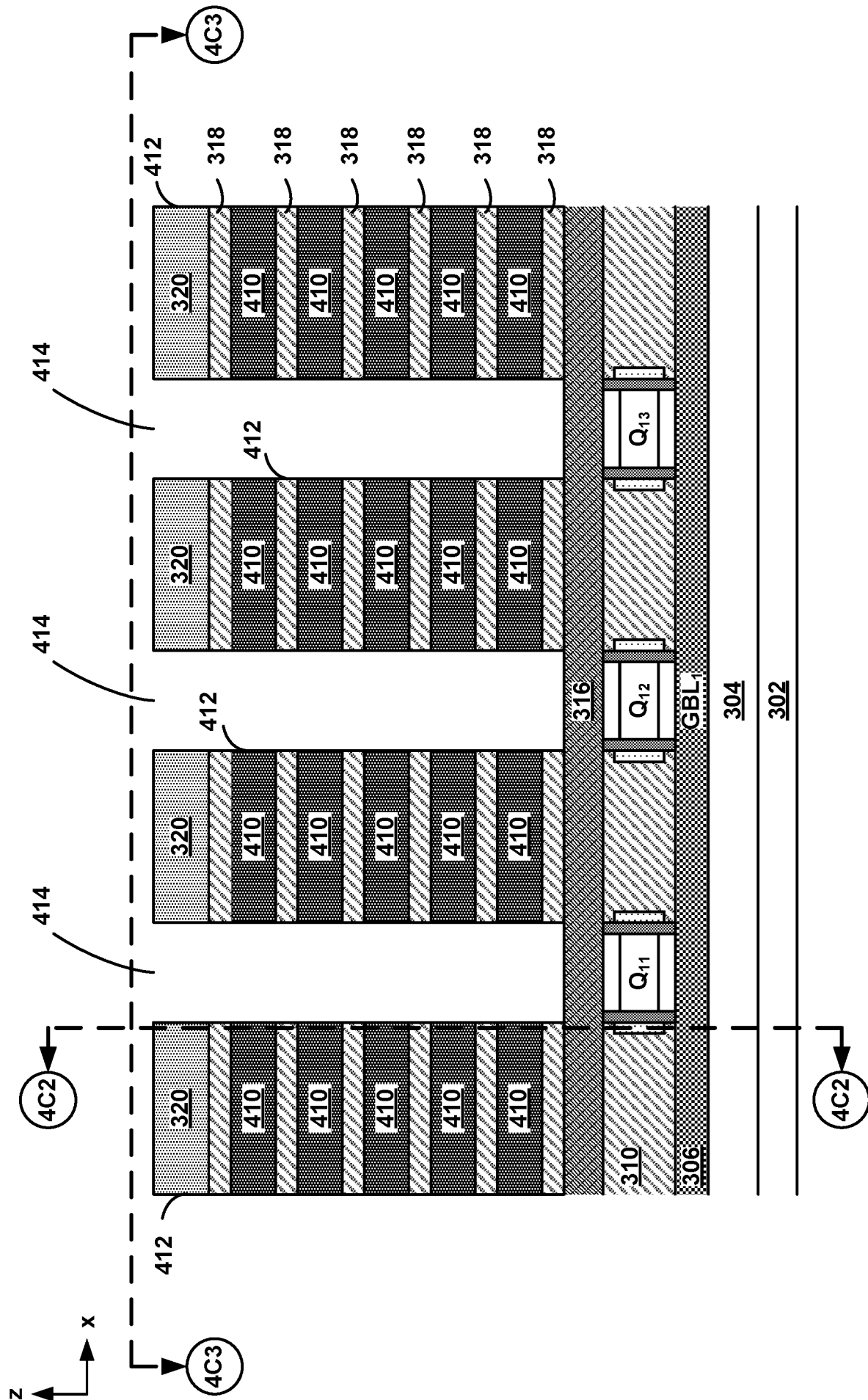


FIG. 4B2



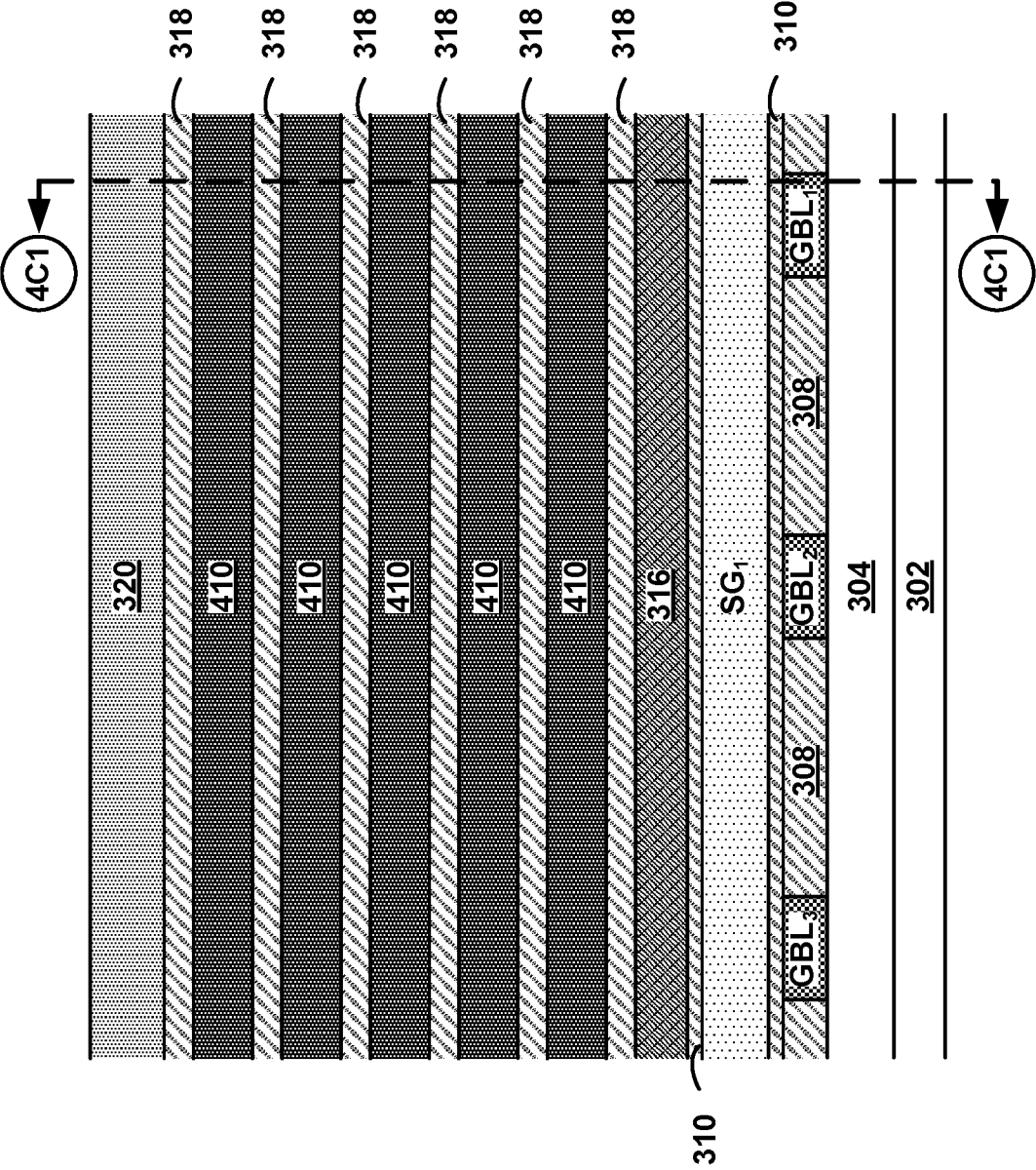
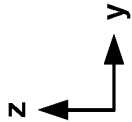


FIG. 4C2

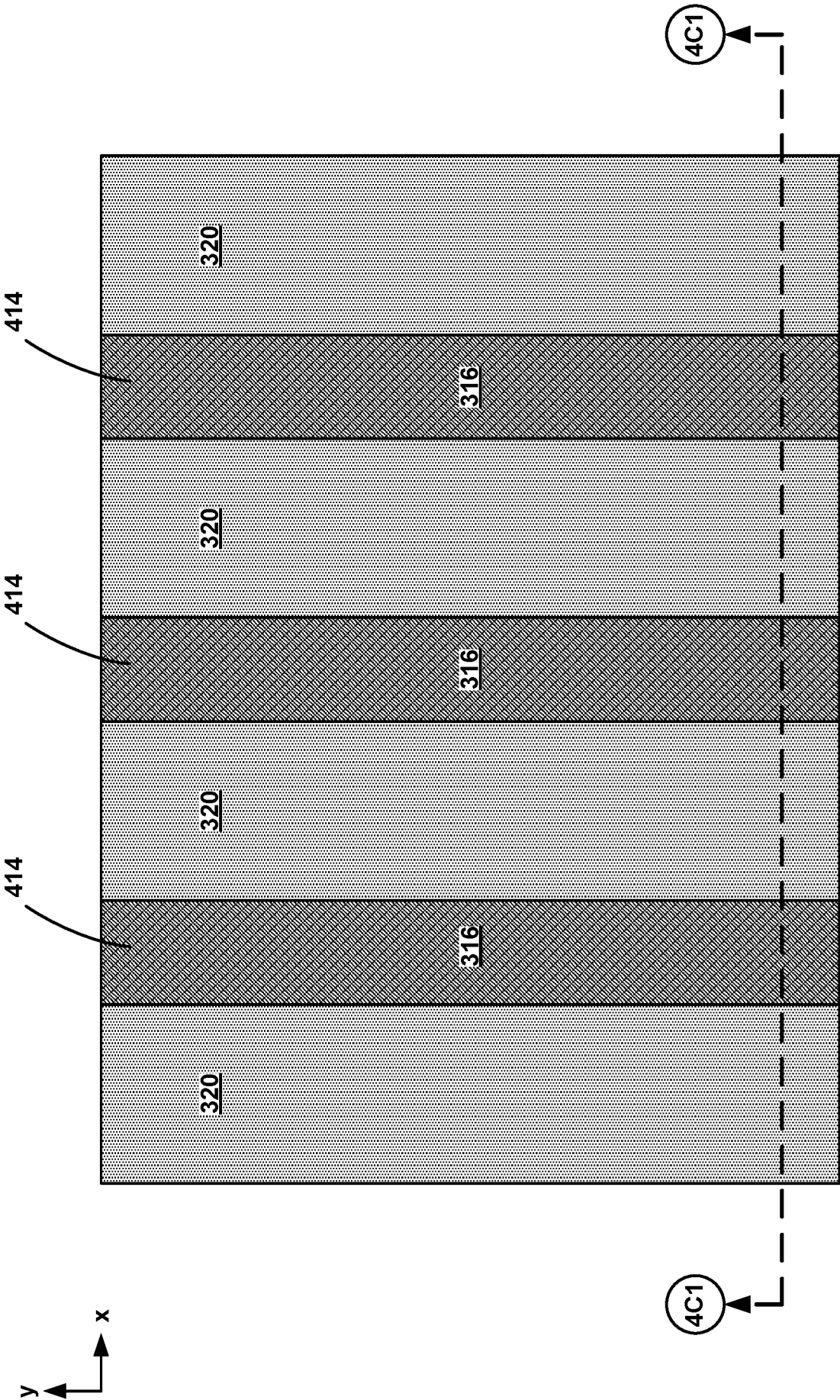


FIG. 4C3

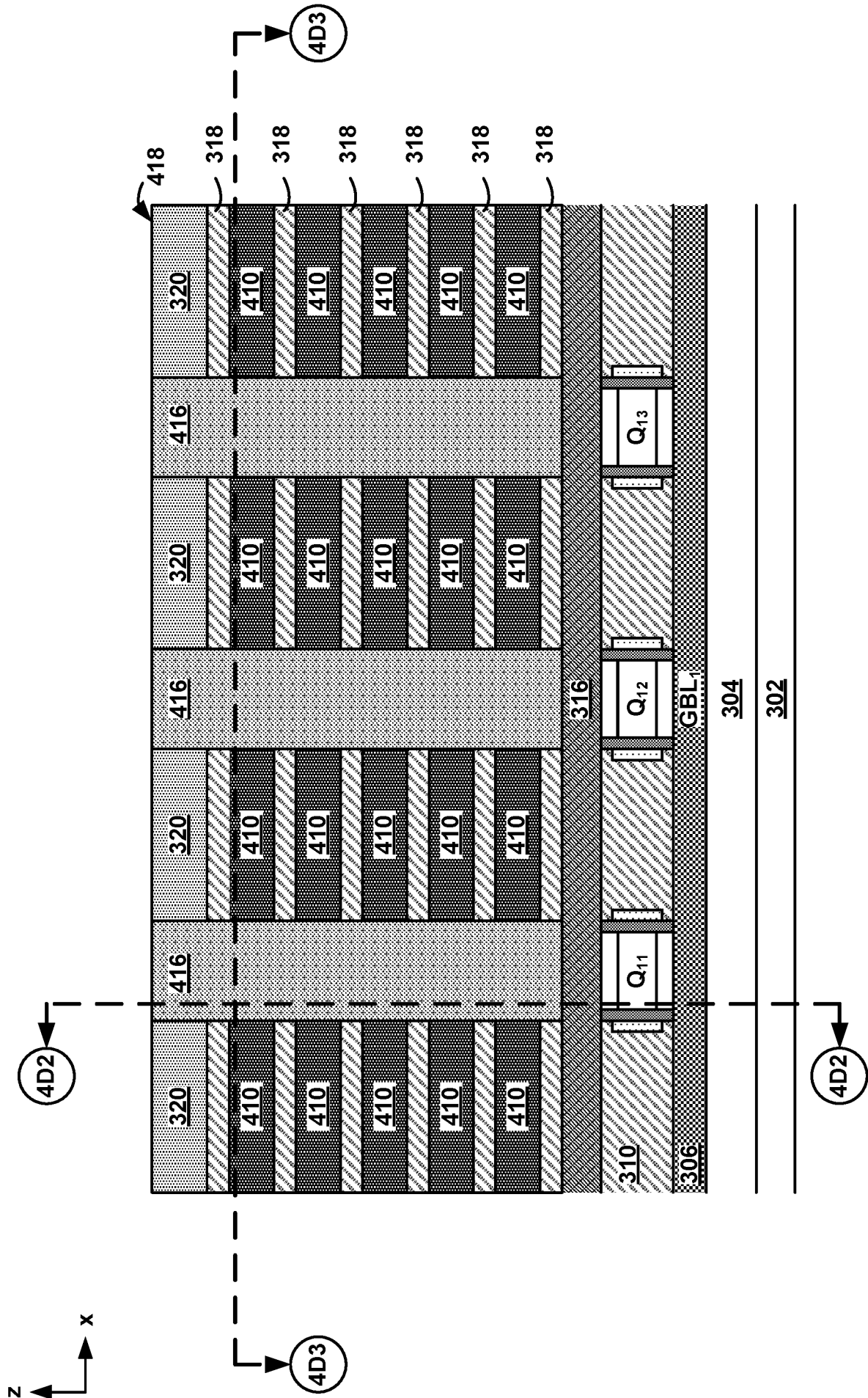


FIG. 4D1

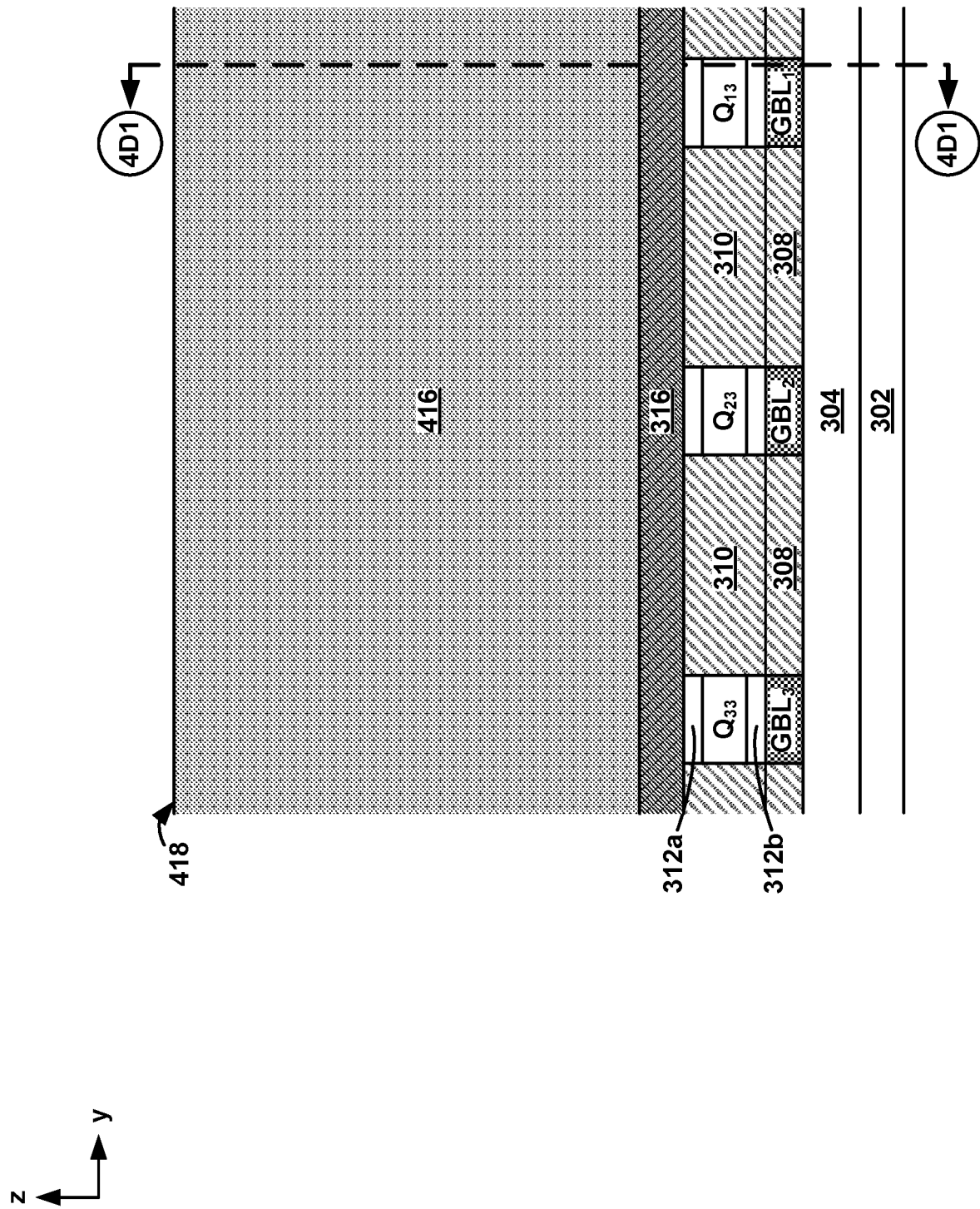


FIG. 4D2

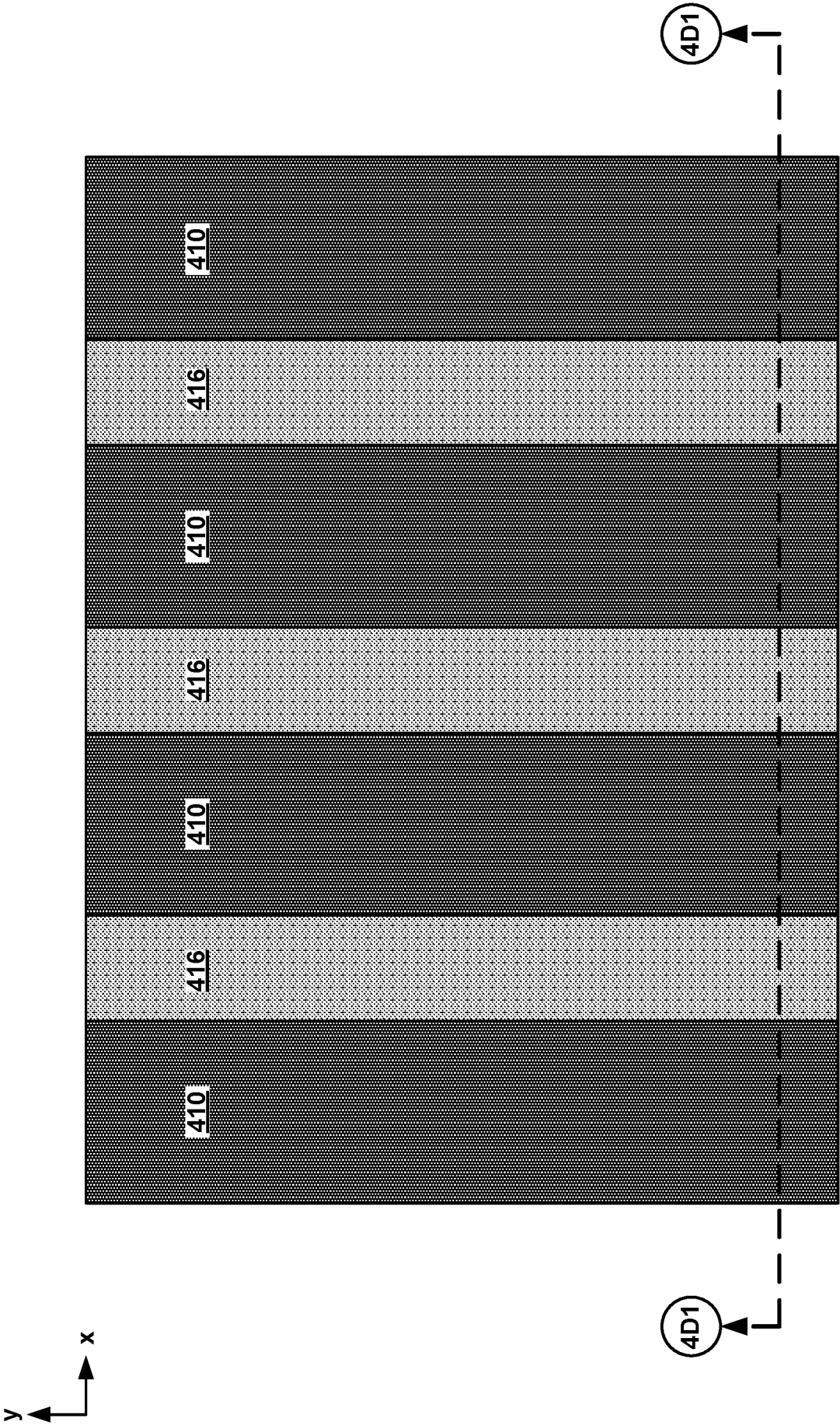
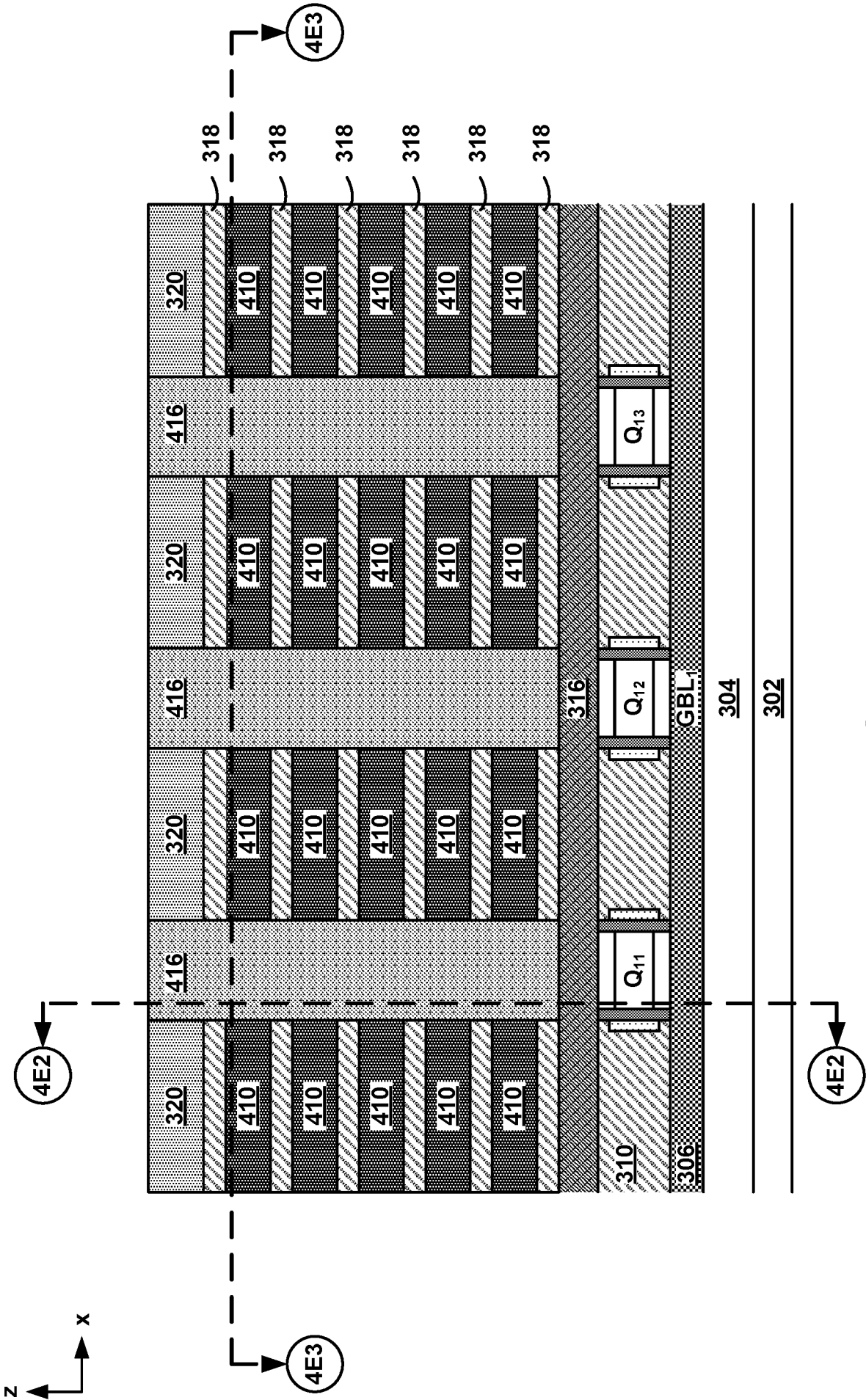


FIG. 4D3



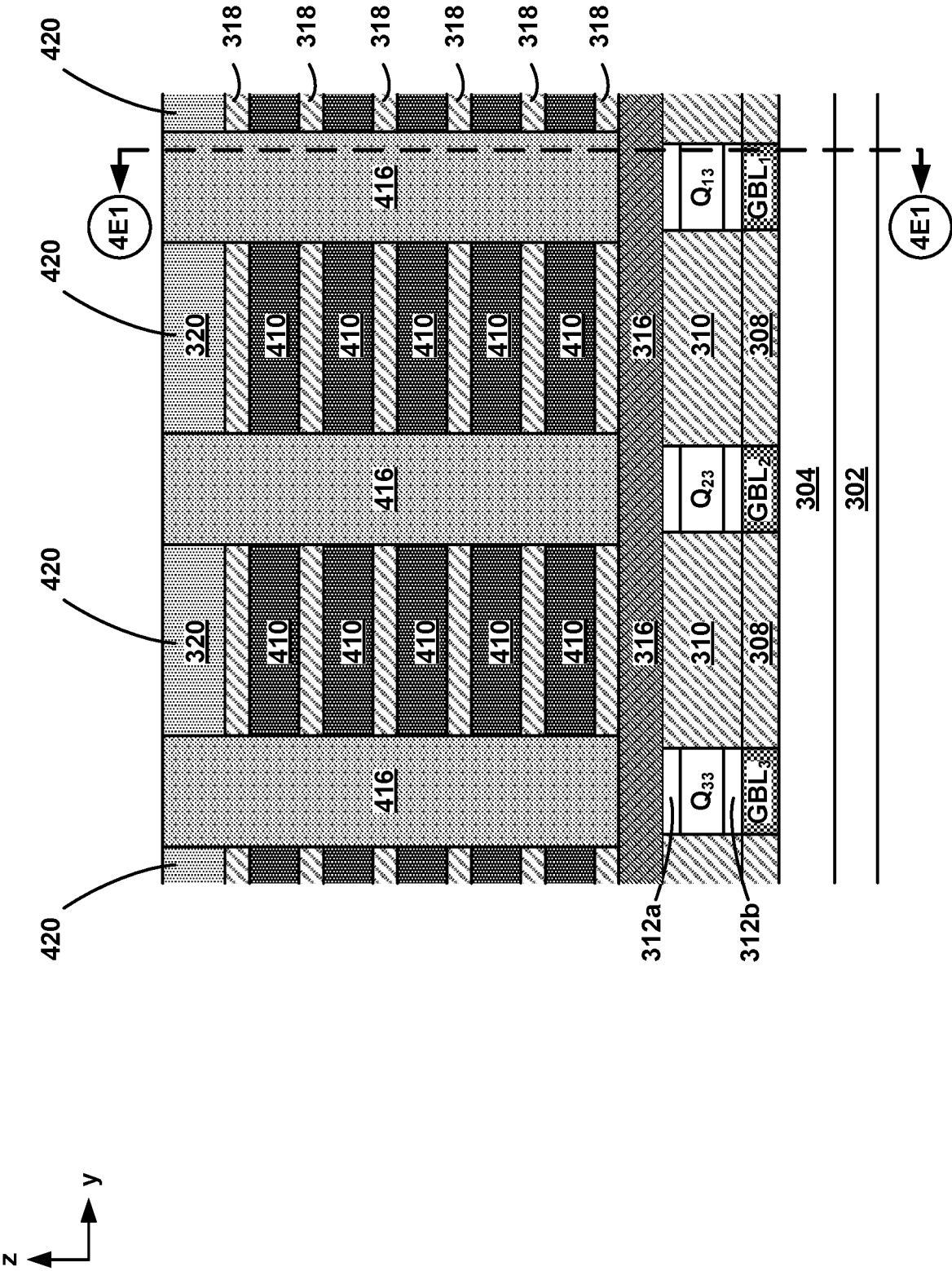


FIG. 4E2

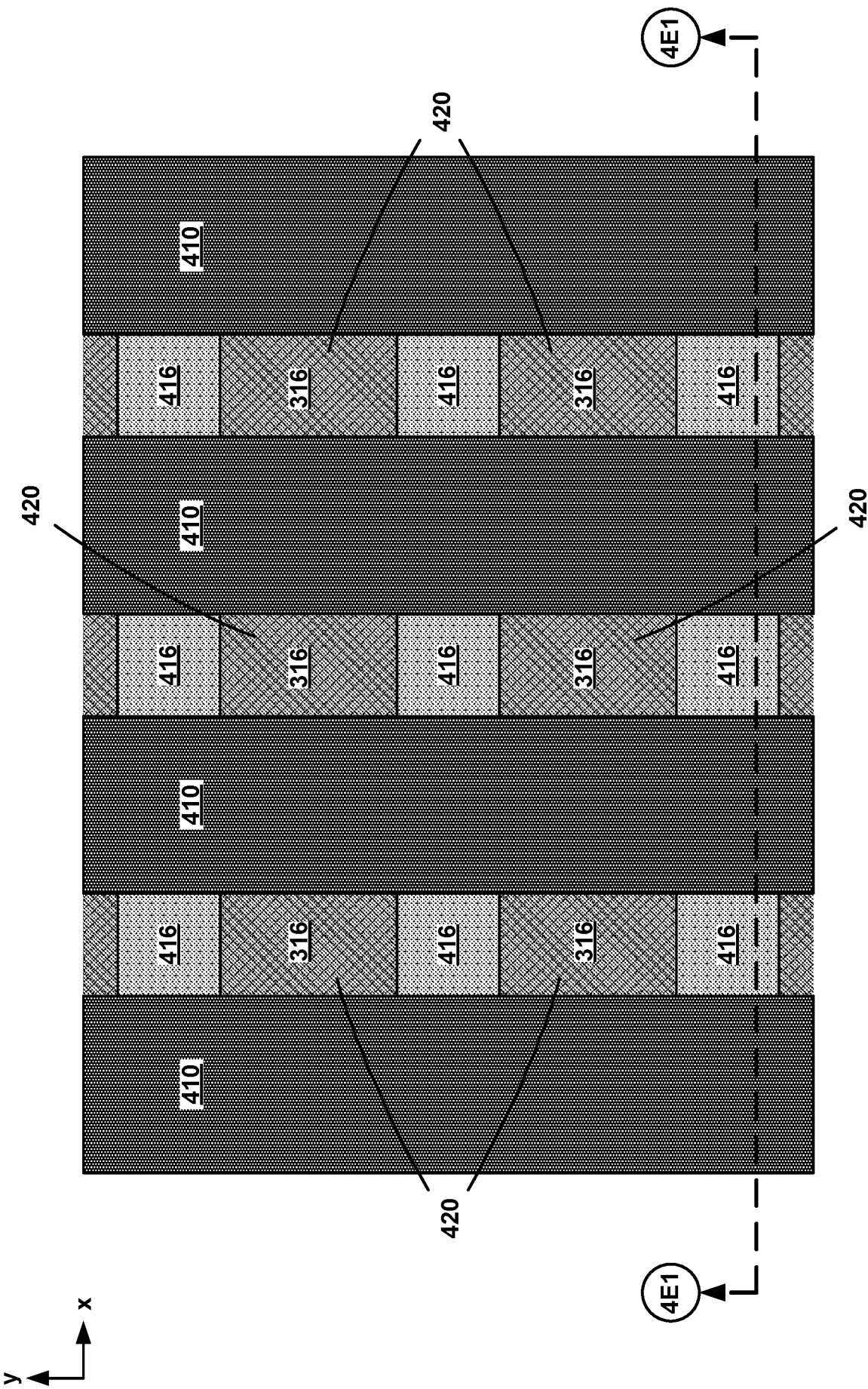


FIG. 4E3

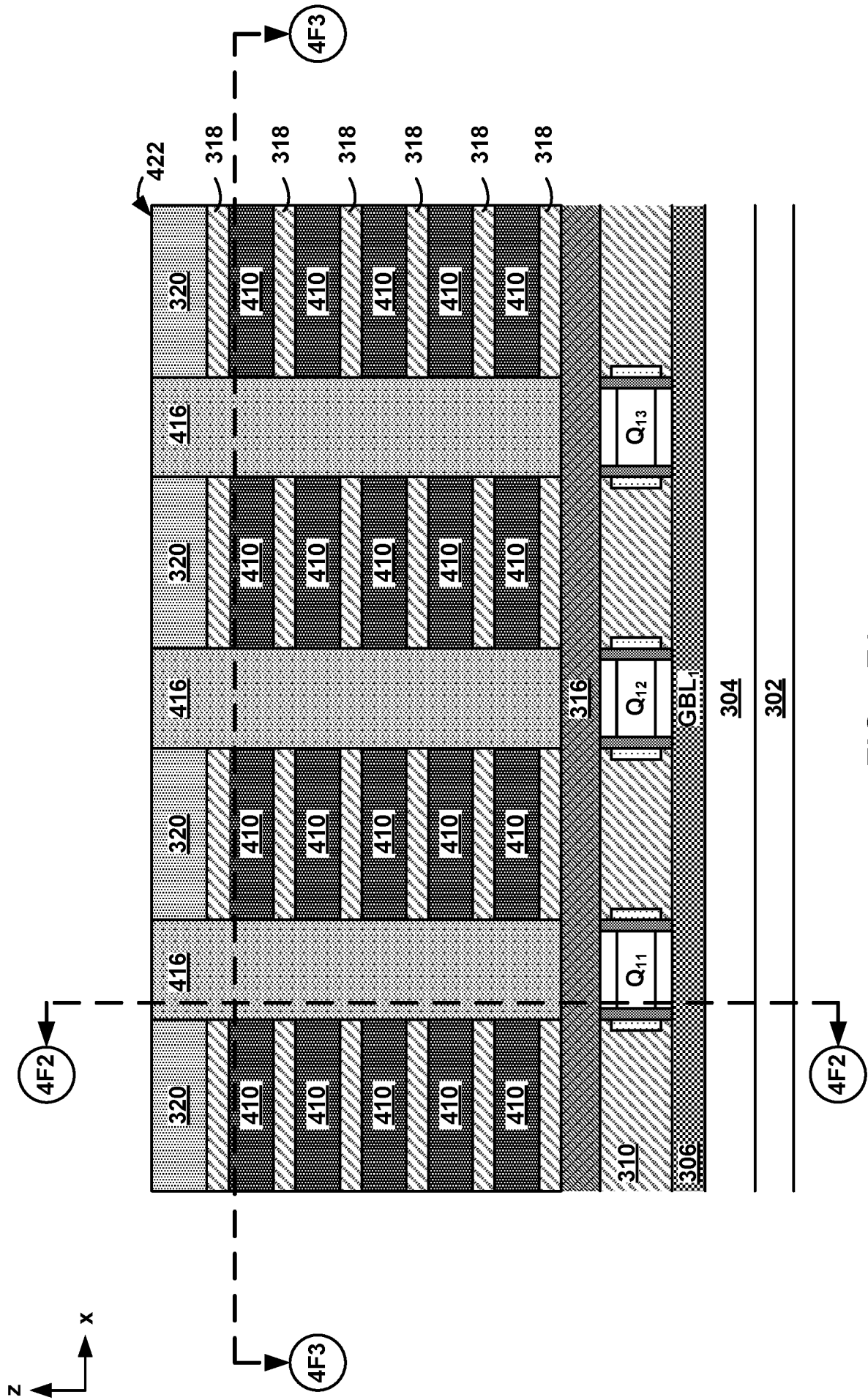


FIG. 4F1

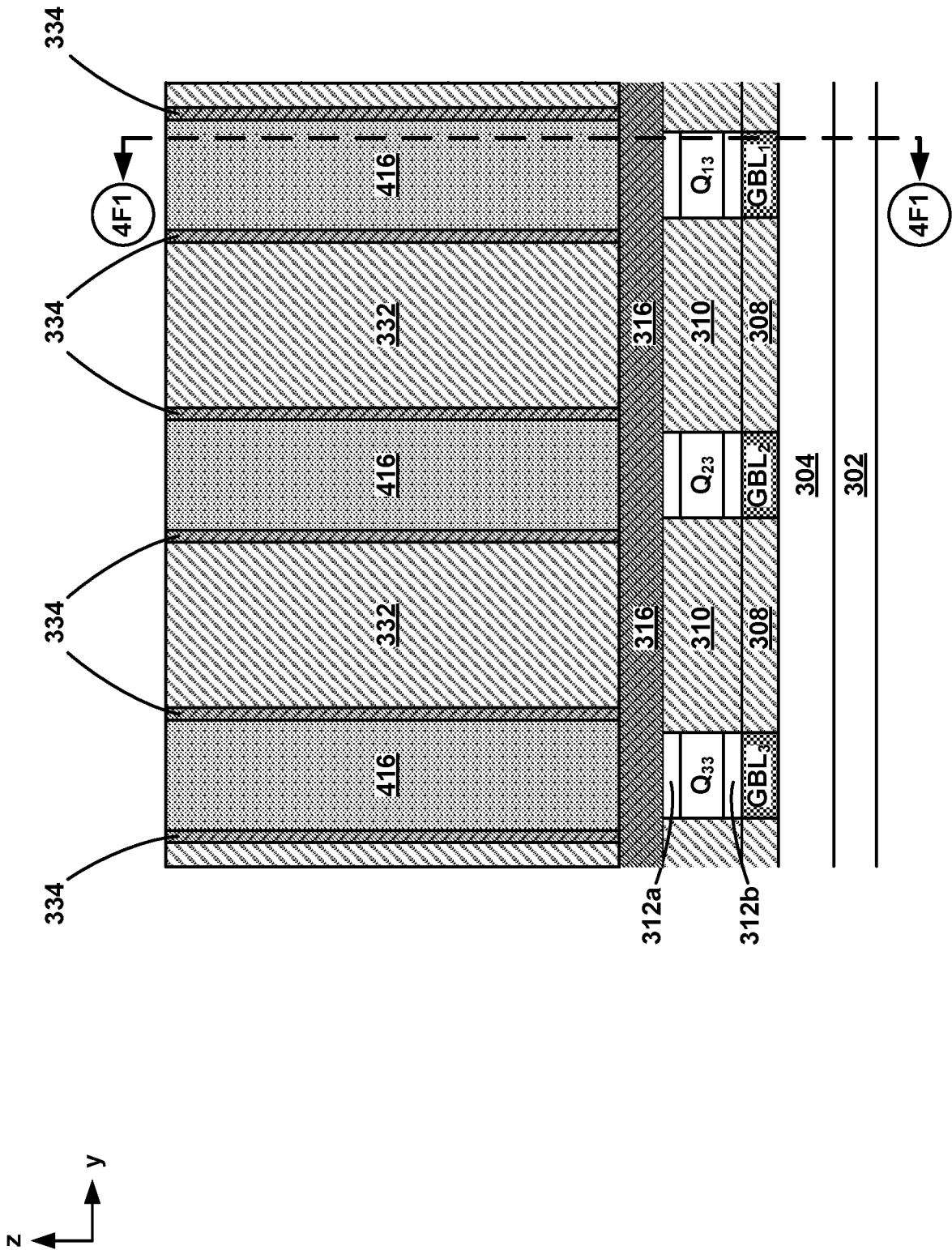


FIG. 4F2

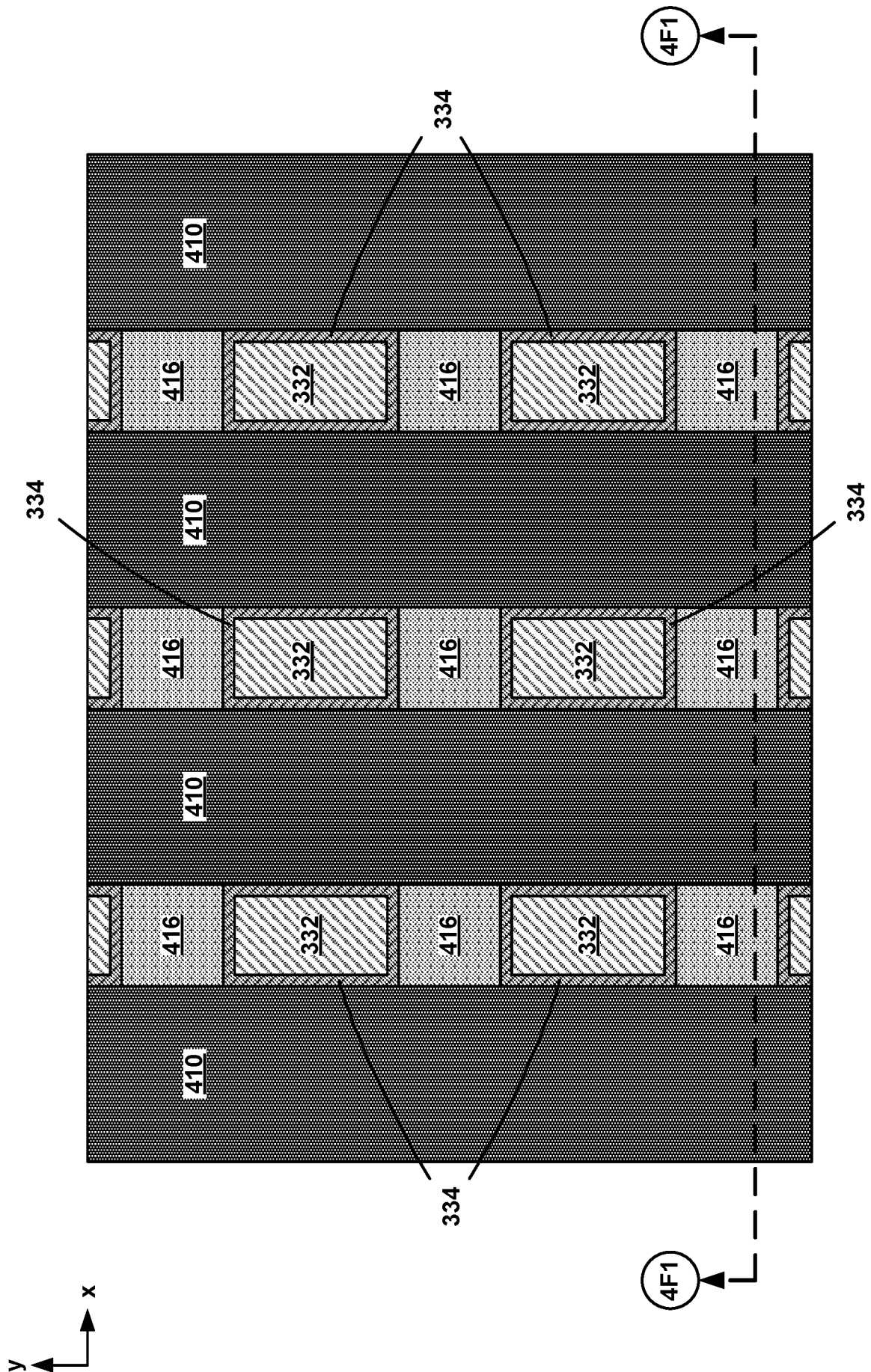


FIG. 4F3

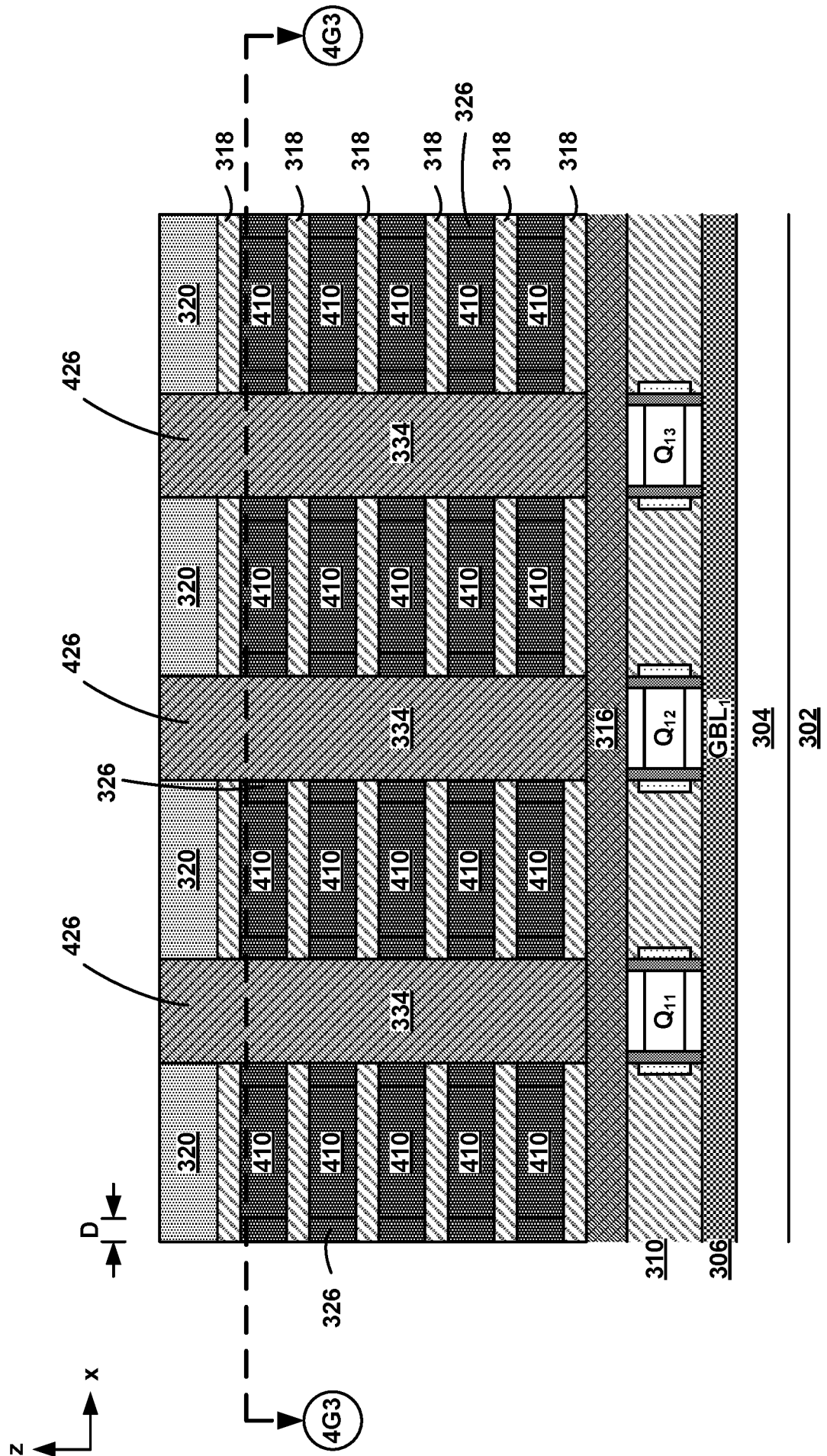
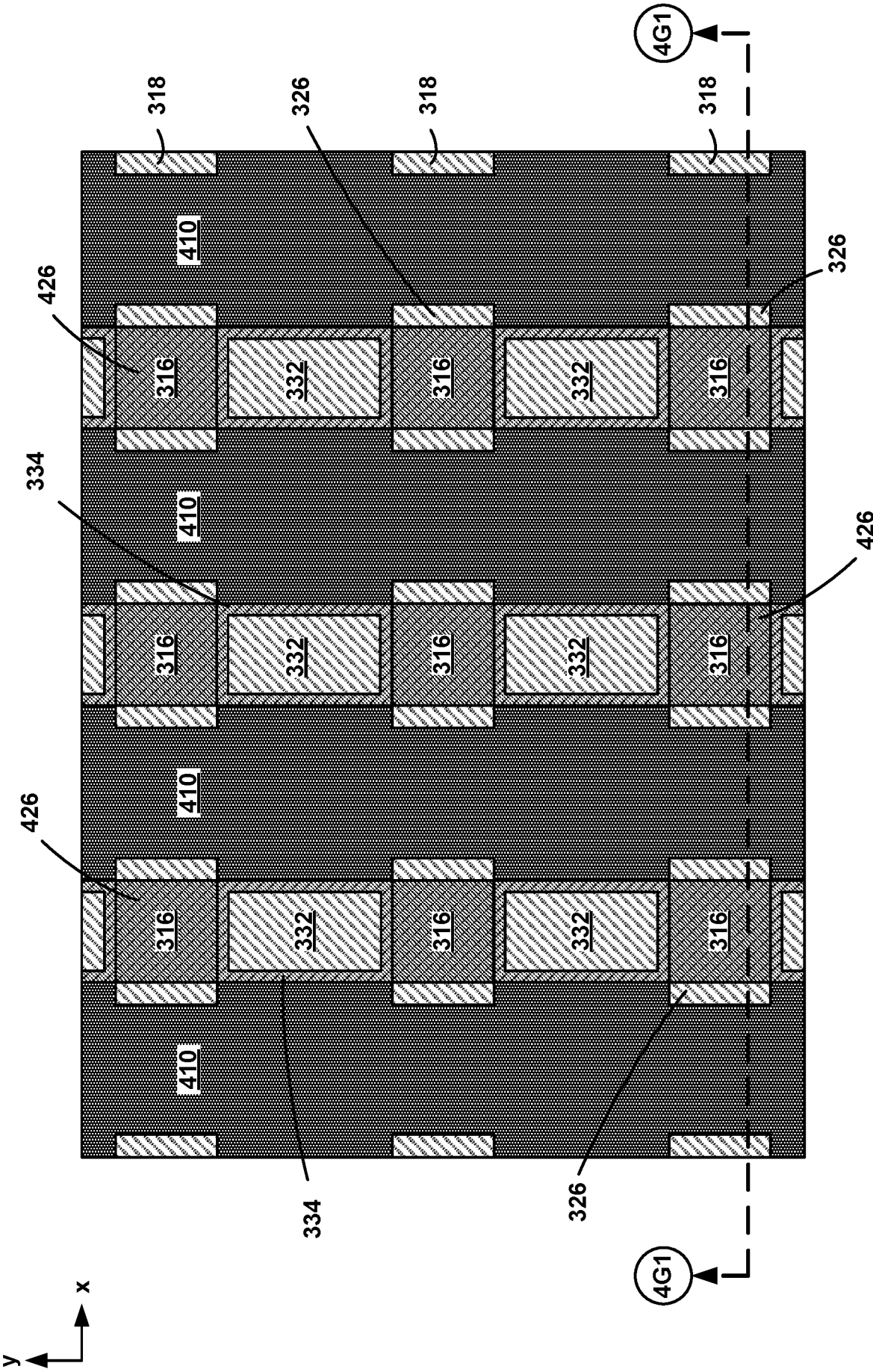
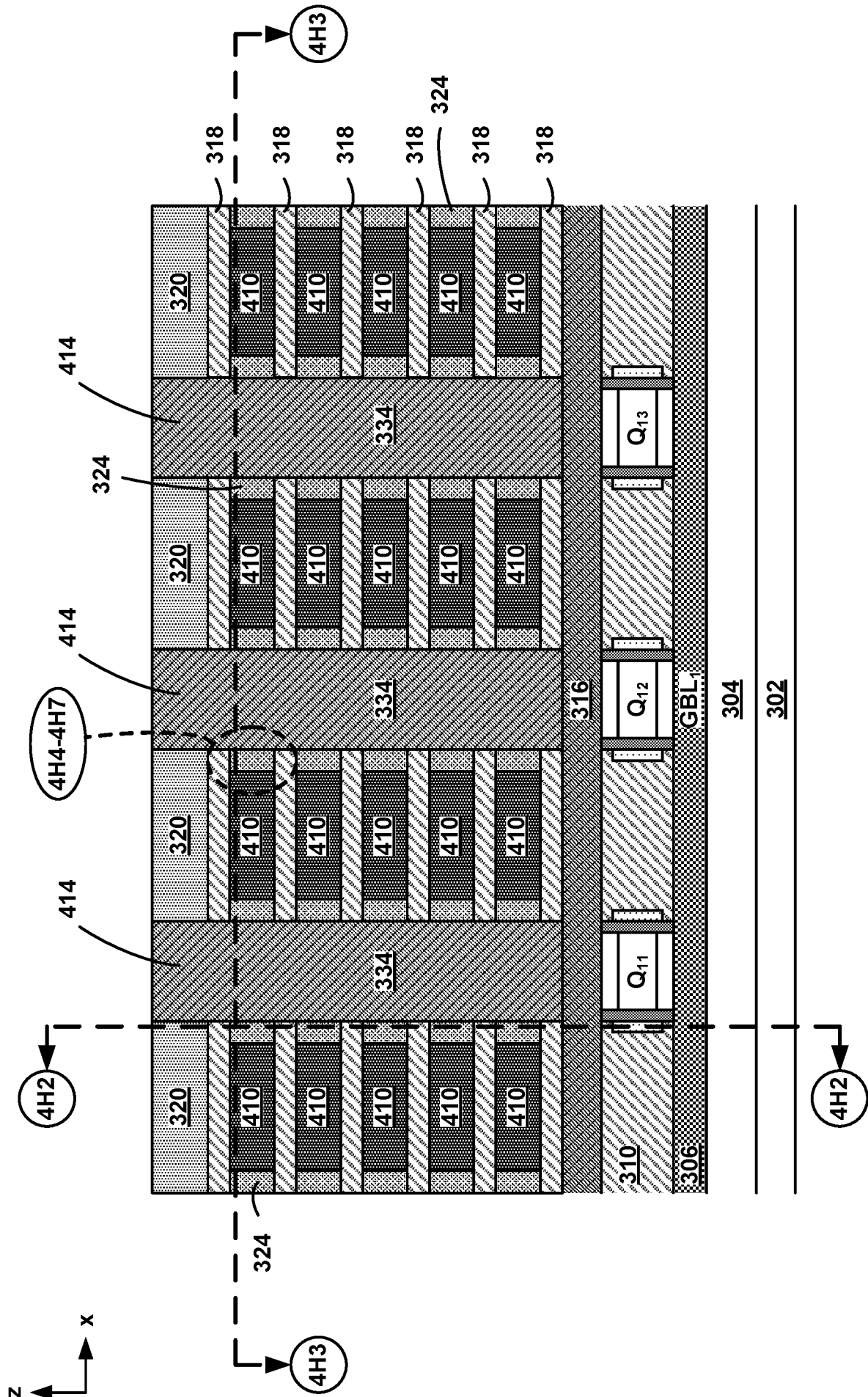


FIG. 4G1





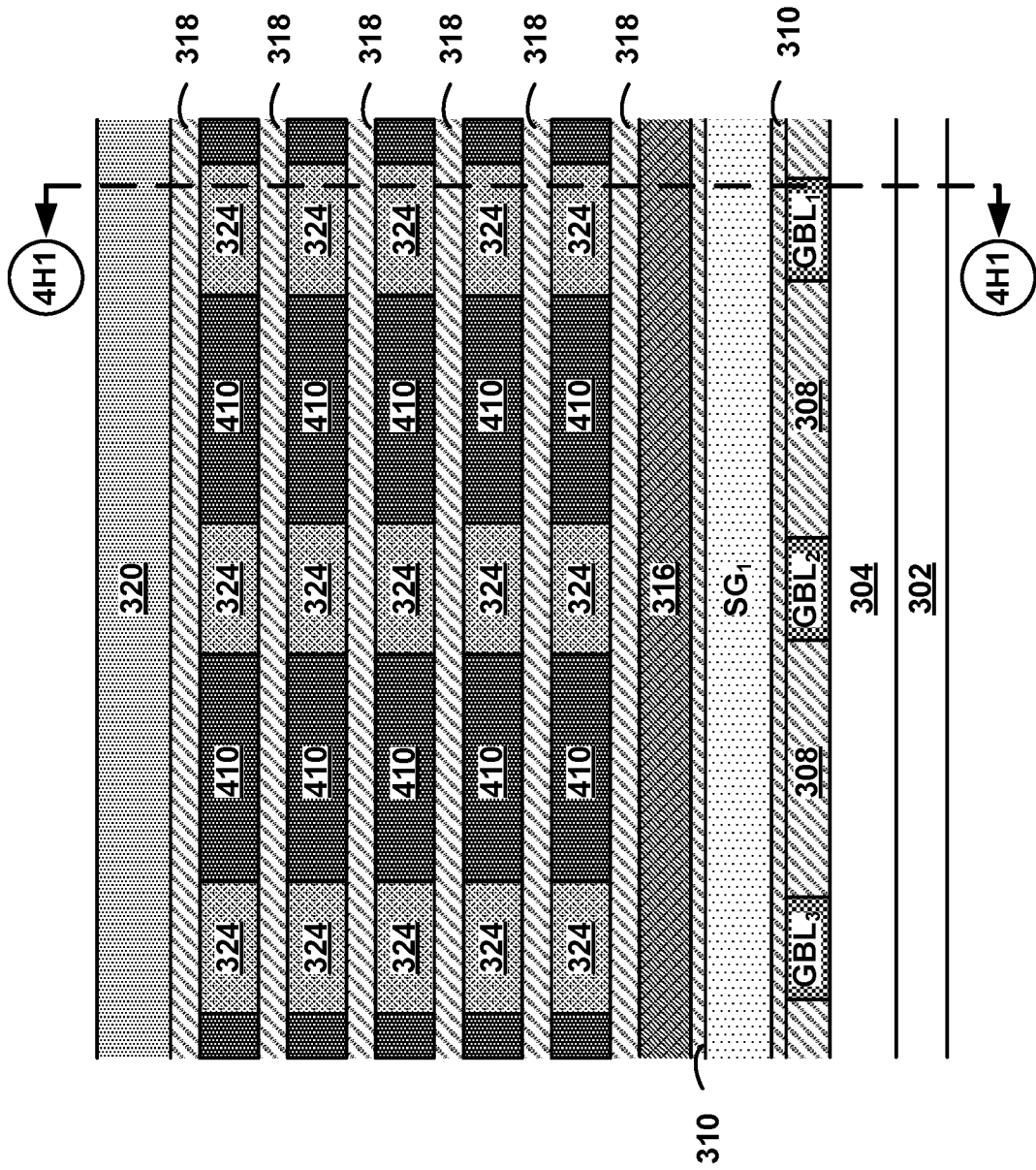
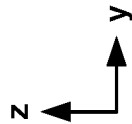
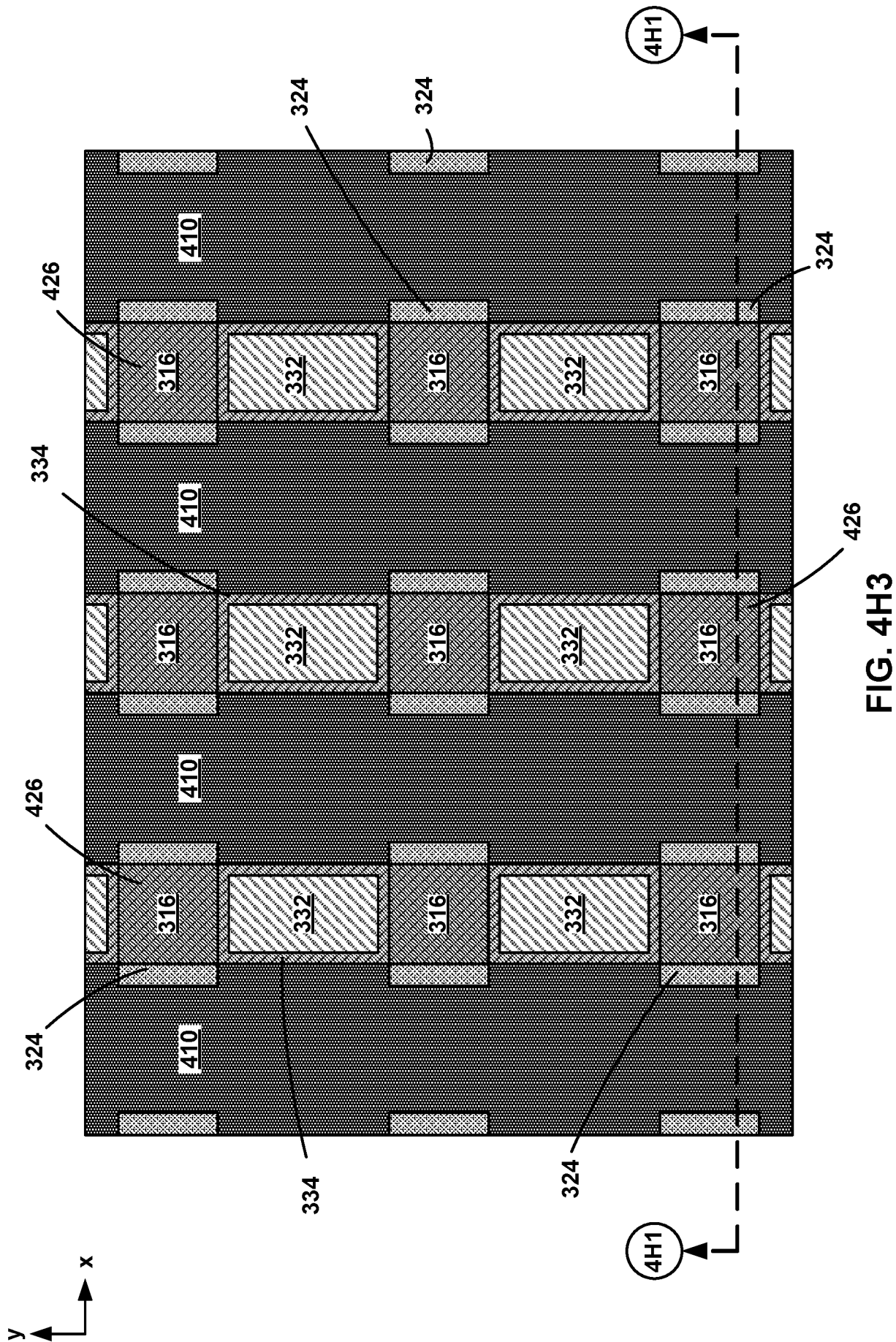


FIG. 4H2



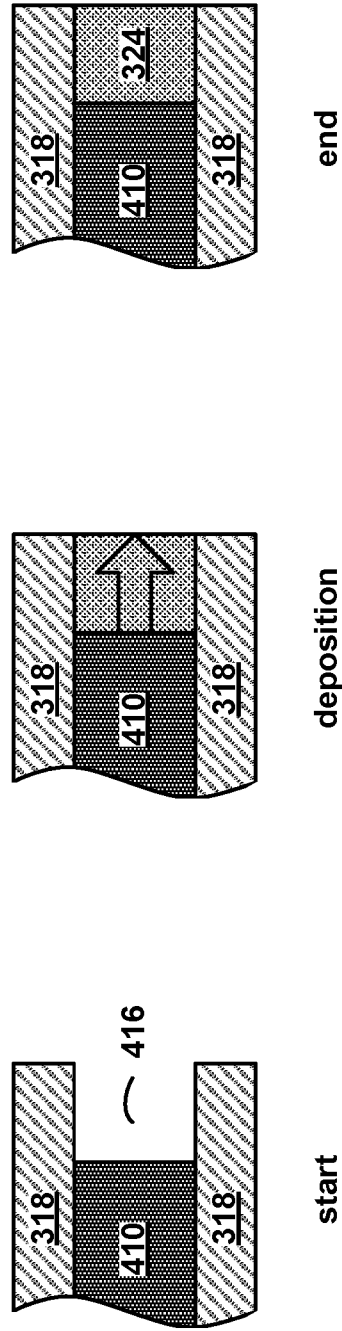


FIG. 4H4

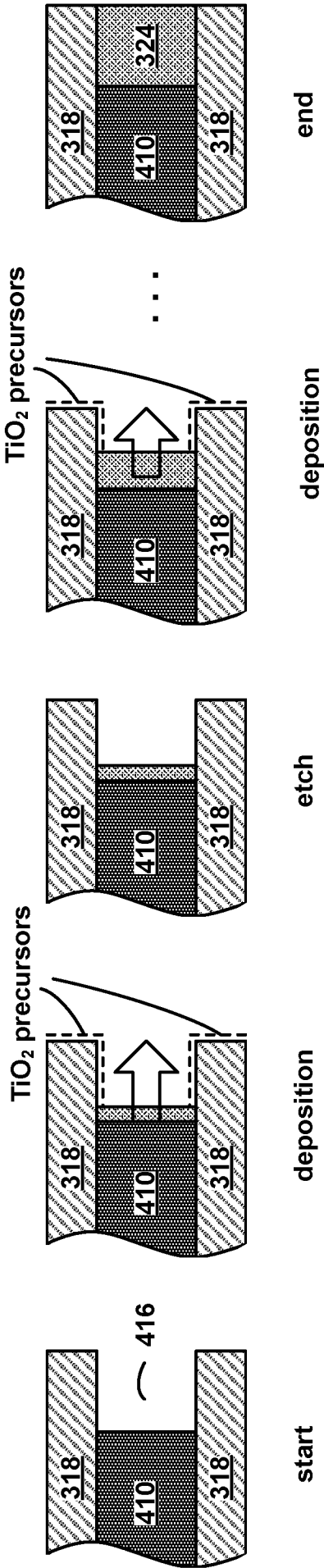


FIG. 4H5

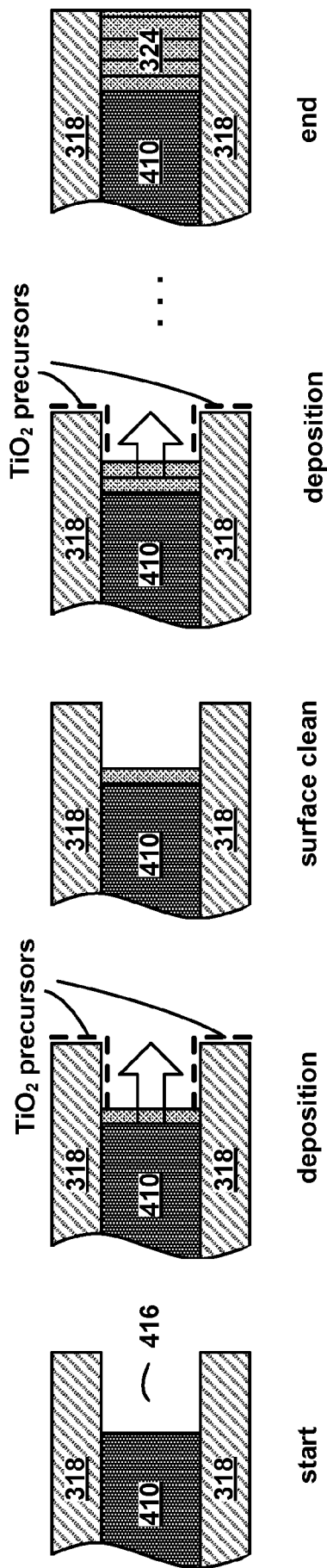


FIG. 4H6

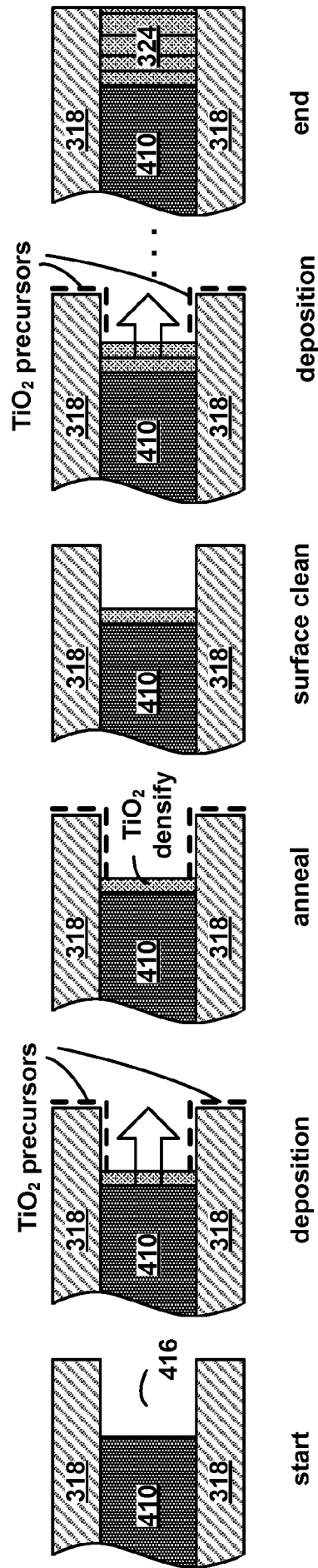


FIG. 4H7

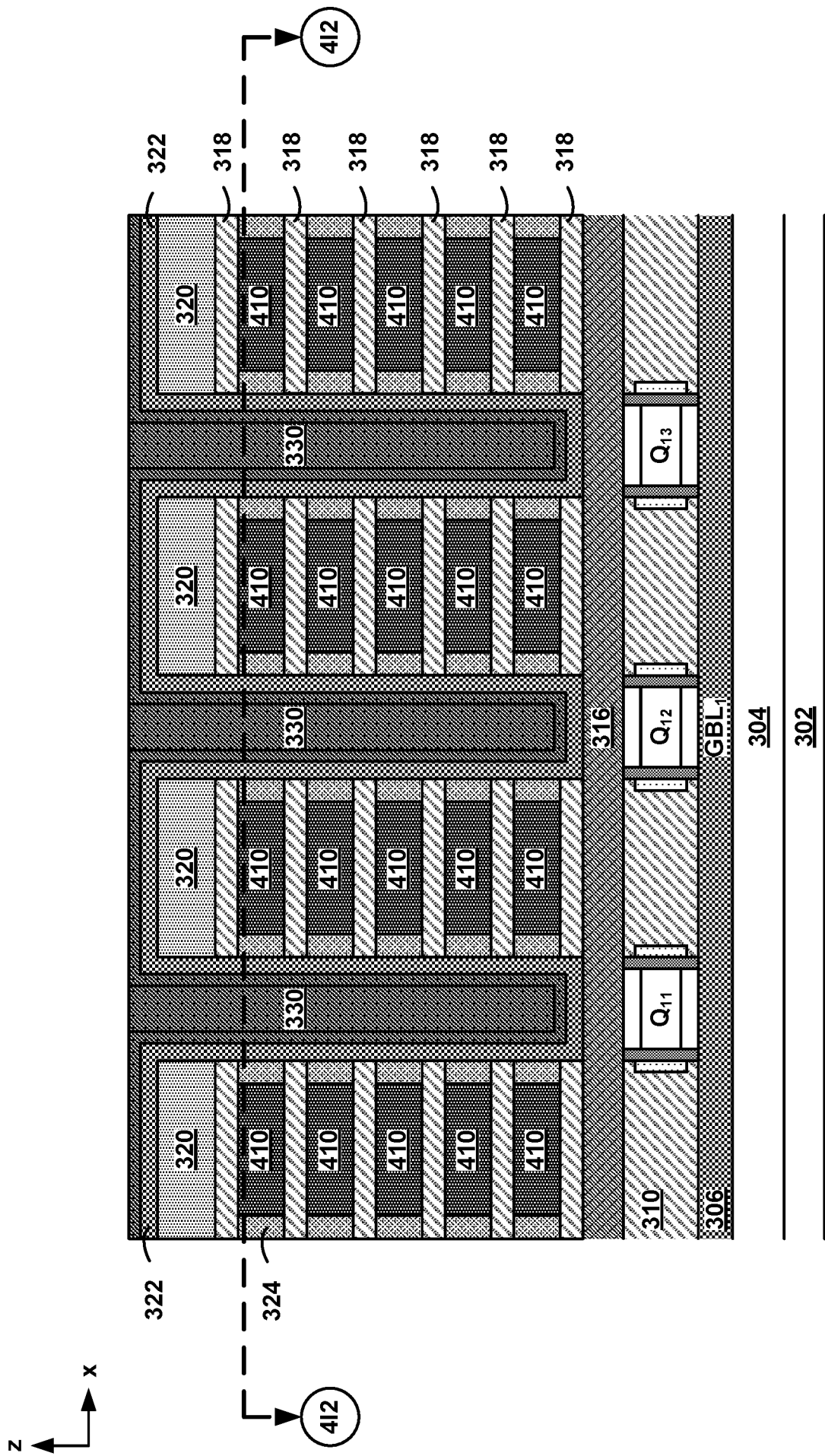
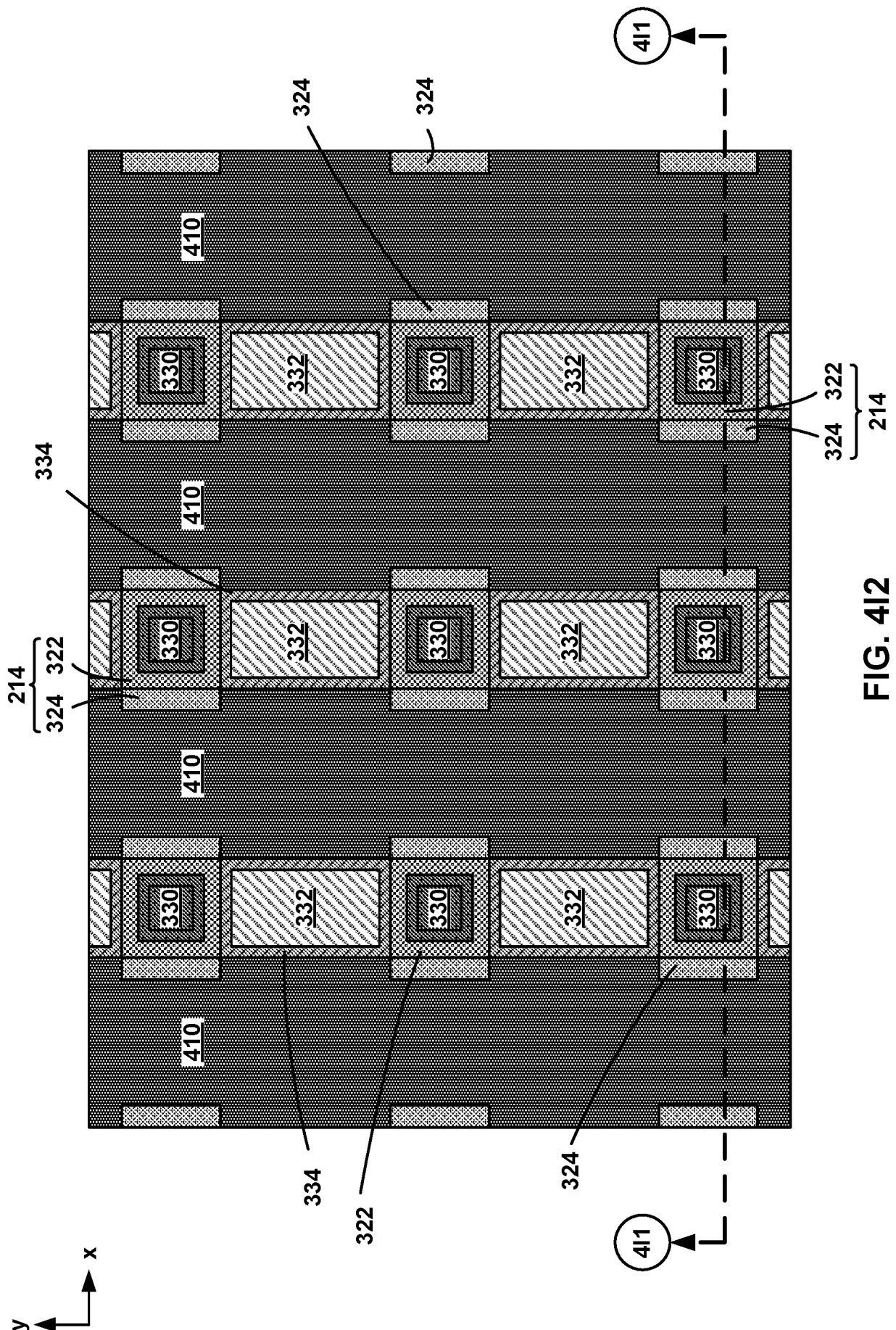
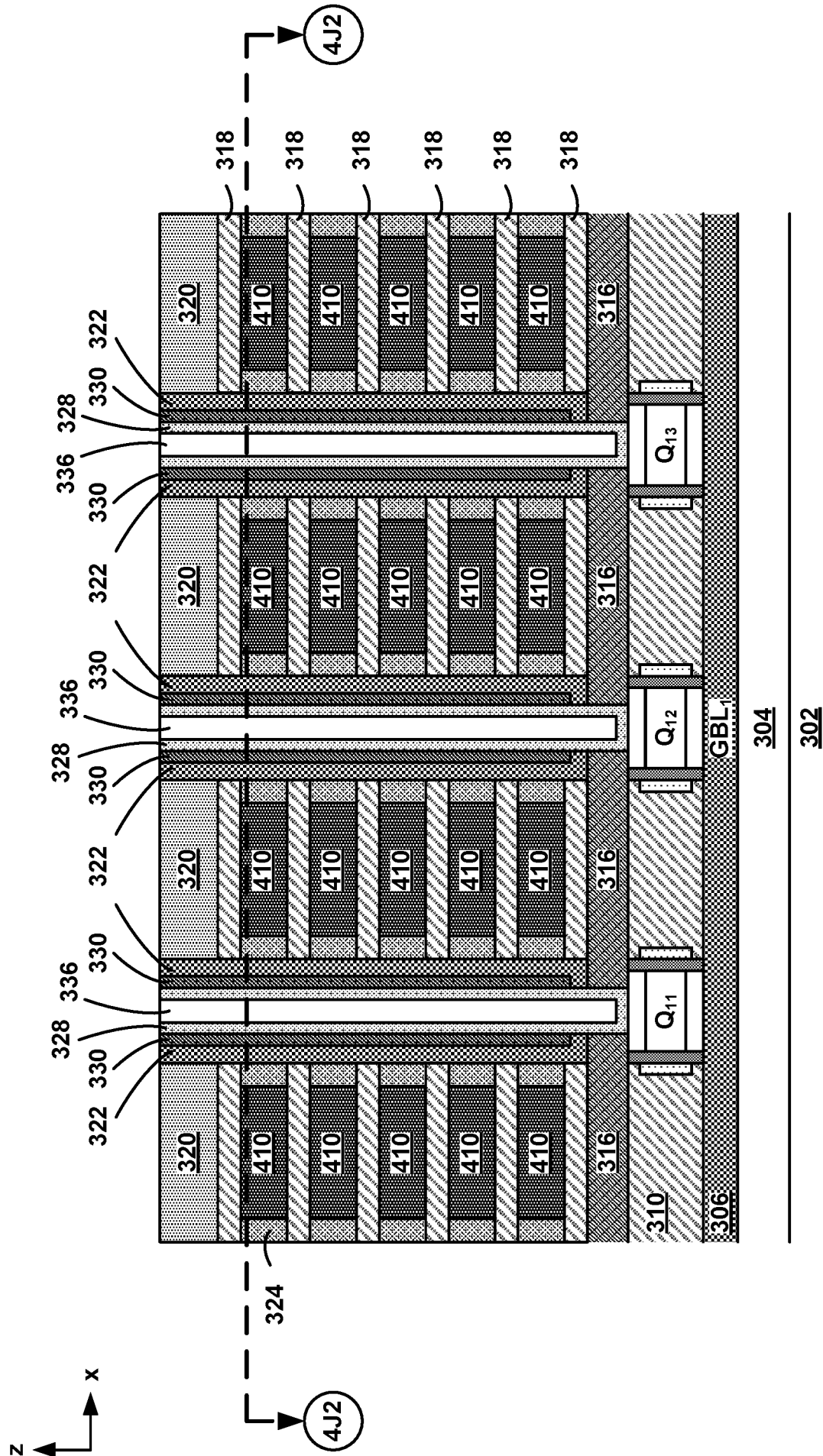
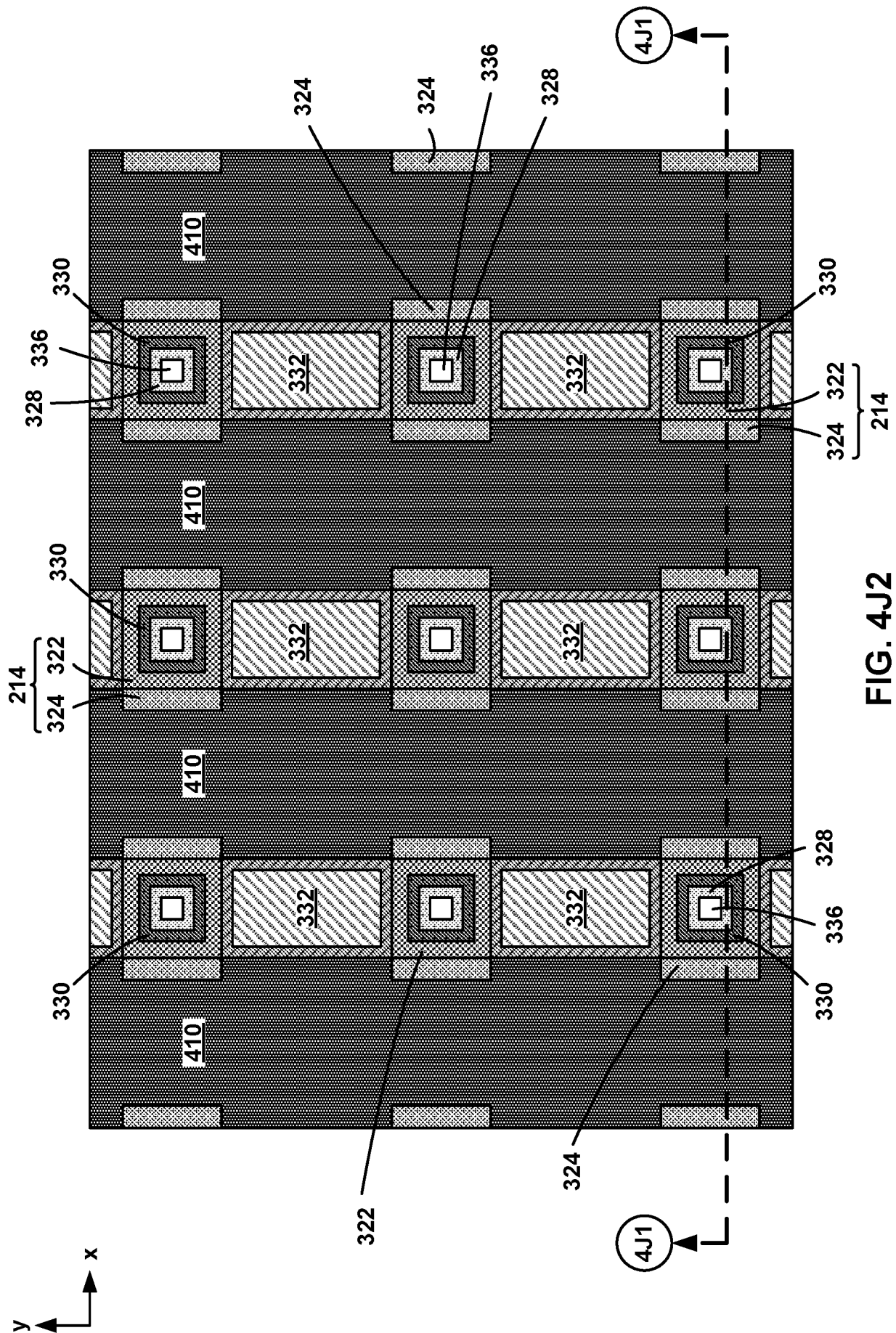


FIG. 4I1







INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/021077

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00 H01L27/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9 443 910 B1 (FUJIWARA KAN [JP] ET AL) 13 September 2016 (2016-09-13) column 9 - column 13; figures 5,6,8 -----	1-3, 10-15
X	US 9 564 587 B1 (JO SUNG HYUN [US] ET AL) 7 February 2017 (2017-02-07) column 3 - column 23; figures 3,11 -----	1
A	US 2012/211722 A1 (KELLAM MARK D [US] ET AL) 23 August 2012 (2012-08-23) -----	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2018/021077

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
US 9443910	B1	13-09-2016	US	9443910 B1		13-09-2016
			WO	2017007563 A1		12-01-2017

US 9564587	B1	07-02-2017	US	9564587 B1		07-02-2017
			US	9570683 B1		14-02-2017

US 2012211722	A1	23-08-2012	JP	2013510438 A		21-03-2013
			KR	20120104992 A		24-09-2012
			US	2012211722 A1		23-08-2012
			WO	2011056281 A1		12-05-2011
