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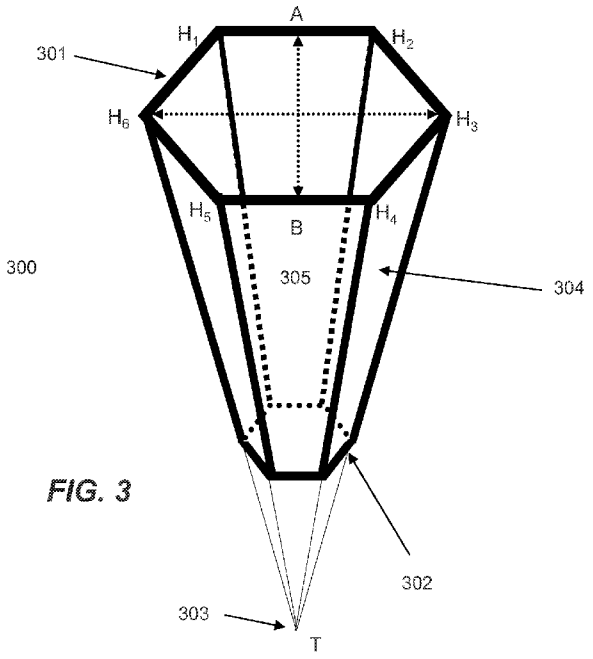

FIG. 3

(57) Abstract: The present disclosure presents a partially-transparent (see-through) three-dimensional thin film solar cell (3-D TFSC) substrate. The substrate includes a plurality of unit cells. Each unit cell structure has the shape of a truncated pyramid, and its parameters may be varied to allow a desired portion of sunlight to pass through.

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TRUNCATED PYRAMID STRUCTURES FOR SEE-THROUGH SOLAR CELLS

FIELD

[0001] This disclosure relates in general to the field of solar cells and solar cell manufacturing. Particularly, the disclosure relates to enhanced three-dimensional thin-film or crystalline-film solar cells (3-D TFSCs) and methods of manufacturing the same. Even more specifically, this disclosure relates to structural designs and methods of manufacturing aesthetically appealing, three-dimensional partially-transparent (see-through) TFSCs with relatively high conversion efficiencies and substantially uniform light transmissivities. This disclosure is applicable to building-integrated photovoltaics (BIPV) applications including power-generating solar glass as well as other solar photovoltaic power modules.

DESCRIPTION OF THE RELATED ART

[0002] Three-dimensional thin film solar cell substrates afford cost, performance, and mechanical strength advantages. Compared to traditional flat solar cells with a similar amount of silicon, 3-D TFSCs have superior mechanical strength, better light trapping, and lower cell processing costs because of their self-aligned nature.

[0003] BIPV involves the process of integrating electricity-producing photovoltaic technology into residential, commercial, and industrial building and construction designs and materials. With BIPV, the solar electricity-producing components actually become an integral part of the building or construction materials and design, often serving as the protective exterior weathering skin and/or interior building components. Semi-transparent or see-through solar PV modules comprise the most attractive segment of BIPV applications. These modules can be

used in many applications including window glazing in building windows. In some applications they are also a part of shading devices such as car parking covers. Such BIPV systems are also known as "shadow-voltaic" systems. See-through BIPV modules can be also part of energy efficient glazing, where they are used instead of usual glass.

[0004] Currently, about 80% of the BIPV applications are served by crystalline silicon cell technology, while inorganic thin-film (TF) technologies account for the remaining 20% of the total BIPV market. However, the TF technologies are projected to capture over 50% of the BIPV applications by 2015. The TF technologies include amorphous silicon (a-Si), cadmium telluride (CdTe), copper-indium-gallium-diselenide (CIGS), and organic PV (OPV). Among them, CdTe and CIGS promise higher efficiencies than a-Si. However, these TF technologies in practice offer efficiencies in the range of 5% to 12%, with the TF see-through BIPV module efficiencies being essentially limited to the single-digit efficiency range of 4% to 8%. Both OPV and dye-sensitized solar cells (DSSC) are considered to be the third generation BIPV technologies (both currently providing module efficiencies on the order of 6%). All the TF and DSSC BIPV technologies currently offer much lower efficiencies than crystalline silicon BIPV. However, the TF technologies provide better aesthetics than crystalline silicon, particularly for see-through BIPV module applications. In a typical see-through crystalline silicon BIPV module for solar glass applications, the crystalline silicon cells are spaced apart to allow for visible light transmission in between the tiled cells. While these see-through crystalline silicon PV modules can provide relatively high effective efficiencies (e.g., typically in the range of 10% to 12%), they do not offer very attractive

aesthetics, both due to the tiled design and also due to the standard busbar emitter interconnects in the cells (which may show visible metallization fingers and busbars).

[0005] DSSCs operate based on the interaction between light and a dye coated onto small grains of titanium dioxide. The grains are placed in a liquid that acts as an electrolyte, collecting the electrons released by the dye as it absorbs light, thus generating current. The whole mixture is sandwiched between a transparent glass sheet electrode doped with tin oxide to make it electrically conductive, and a rear panel. The efficiency of DSSCs designed for outdoor conditions is currently about 6%. This is far below the efficiency of standard crystalline silicon BIPV modules.

[0006] OPV and DSSC BIPV modules cannot easily compete with the conventional crystalline silicon or TF BIPV solar panels due to their relatively low conversion efficiencies and shorter operational lifetimes. Crystalline silicon solar cells and modules have proven long lifetimes in excess of 25-30 years in the field, and no TF or DSSC technology can offer or match such a track record. While the conventional crystalline silicon wafer BIPV is suitable only for rigid BIPV applications, the TF and DSSC BIPV modules can be used for both rigid and flexible substrate applications.

SUMMARY

[0007] Reference is now made to co-pending U.S. Pub. No. 2008/0295887, entitled "THREE-DIMENSIONAL THIN-FILM SOLAR CELLS," (the '887 publication) which has a common inventor with the present disclosure and which is hereby expressly incorporated by reference.

[0008] The '887 publication disclosed methods for manufacturing a 3-D TFSC. The methods comprise using a silicon substrate template to form the 3-D thin film silicon substrate (3-D TFSS). The template comprises a plurality of posts and a plurality of trenches between the plurality of posts. The 3-D TFSS is made by forming a sacrificial layer on the template, subsequently depositing a semiconductor layer, selectively etching the sacrificial layer, and releasing the semiconductor layer from the template. More specifically, the semiconductor layer is a self-supporting, free-standing three-dimensional (3-D) epitaxial silicon thin film deposited on and released from a low-cost reusable crystalline silicon substrate template. The reusable silicon template may be reused to form 3-D films numerous times before being reconditioned or recycled.

[0009] The present disclosure includes a method for manufacturing a 3-D TFSS with truncated-pyramid shaped unit cells for making partially transparent solar cells. The 3-D see-through TFSS is also a free standing, self-supporting film that is released/separated from a reusable silicon template, which comprises a plurality of truncated pyramid structures. The reusable silicon template may be reused to form 3-D TFSCs numerous times before being recycled.

[0010] The 3-D TFSCs of this disclosure can be made to be relatively rigid, semi-rigid, or flexible depending on the 3-D TFSS design parameters. This structural design and fabrication

process results in substantially reduced silicon consumption and PV manufacturing cost. In addition, compared to other flat, thin-film (TF) crystalline Si approaches, the present disclosure may offer the following advantages: (i) conventional surface texturing of flat, thin film, Si to reduce reflectance losses requires a minimum film thickness of preferably tens of microns (e.g., >30 μm) to avoid punch-through pinholes, a constraint that the present disclosure may avoid; (ii) thin flat Si films have much reduced mean optical path length, which reduces IR absorption and results in reduced cell quantum efficiency, whereas the present disclosure may trap light extremely efficiently by virtue of its 3-D nature; (iii) flat TF Si has poor mechanical strength for cell and module processing needs, whereas the present disclosure may be more mechanically robust because of its 3-D structure.

[0011] According to the teachings of the present disclosure, the design parameters of 3-D TFSSs may be varied in order to allow a desired percentage of sunlight to pass through. In this way, partially transparent solar cells having a desired transmissivity may be fabricated.

[0012] These and other advantages of the disclosed subject matter, as well as additional novel features, will be apparent from the description provided herein. The intent of this summary is not to be a comprehensive description of the claimed subject matter, but rather to provide a short overview of some of the subject matter's functionality. Other systems, methods, features and advantages here provided will become apparent to one with ordinary skill in the art upon examination of the following **FIGURES** and detailed description. It is intended that all such additional systems, methods, features and advantages included

within this description be within the scope of the accompanying claims.

BRIEF DESCRIPTIONS OF THE DRAWINGS

[0013] The features, nature, and advantages of the disclosed subject matter may become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference numerals indicate like features and wherein:

[0014] **FIGURE 1 (PRIOR ART)** shows a prior art process flow for planar silicon lift off;

[0015] **FIGURE 2 (PRIOR ART)** shows a prior art process flow for application of self-aligned selective emitter and metallization;

[0016] **FIGURE 3** shows an isometric view of an embodiment of a hexagonal truncated pyramid unit cell;

[0017] **FIGURE 4** shows a top view of a section of an embodiment of a hexagonal truncated pyramid TFSC;

[0018] **FIGURE 5** shows a top view of a section of an embodiment of a hexagonal truncated pyramid TFSC;

[0019] **FIGURE 6** shows a top view of a section of an embodiment of a triangular truncated pyramid TFSC;

[0020] **FIGURE 7** shows a top view of a section of an embodiment of a square truncated pyramid TFSC;

[0021] **FIGURE 8** shows a top view of a section of an embodiment of a trapezoidal truncated pyramid TFSC;

[0022] **FIGURE 9** shows a top view of a section of an embodiment of a truncated pyramid TFSC including hexagonal and triangular unit cells;

[0023] **FIGURE 10** shows a top view of a section of an embodiment of a truncated pyramid TFSC including octagonal and square unit cells;

[0024] **FIGURE 11** shows a top view of an embodiment of a hexagonal truncated pyramid TFSC with a planar peripheral silicon frame;

[0025] **FIGURE 12** shows an embodiment of a process flow for creating see-through holes in a 3-D TFSS;

[0026] **FIGURES 13A-13D** show a cross-sectional view of an embodiment of a formation process for a reusable template;

[0027] **FIGURES 14A-14D** show a cross-sectional view of an embodiment of creating and releasing a TFSS from a reusable template;

[0028] **FIGURES 15A-15D** show a cross-sectional view of an embodiment of creating see-through holes in a 3-D TFSS;

[0029] **FIGURE 16** shows a cross-sectional view of an embodiment of a silicon substrate with hexagonal truncated pyramid unit cells;

[0030] **FIGURE 17** shows a cross-sectional view of an embodiment of a silicon substrate with hexagonal truncated pyramid unit cells;

[0031] **FIGURE 18** shows a side view of an embodiment of a roller coating system for applying dopants;

[0032] **FIGURE 19** shows a side view of an embodiment of a spray coating system for applying dopants;

[0033] **FIGURE 20** shows a side view of an embodiment of a dip coating system for applying dopants;

[0034] **FIGURE 21** shows a cross-sectional view of an embodiment of a hexagonal truncated pyramid TFSC with a thin planar peripheral silicon frame and self-aligned base and emitter contacts;

[0035] **FIGURE 22** shows a cross-sectional view of an embodiment of a hexagonal truncated pyramid TFSC with a thick planar peripheral silicon frame;

[0036] **FIGURE 23** shows a cross-sectional view of an embodiment of a hexagonal truncated pyramid TFSC with a thick planar peripheral silicon frame and self-aligned base and emitter contacts;

[0037] **FIGURE 24** shows a cross-sectional view of an embodiment of a solar glass application of a hexagonal truncated pyramid TFSC;

[0038] **FIGURE 25** shows an isometric view of a section of an embodiment of a hexagonal truncated pyramid TFSC mounted on a glass substrate;

[0039] **FIGURES 26-27** show embodiments of process flows for patterning a reusable silicon substrate;

[0040] **FIGURES 28-31** show embodiments of process flows for fabricating self-supporting 3-D TFSCs;

[0041] **FIGURES 32-39** show embodiments of process flows for doping and metallizing self-supporting 3-D TFSCs;

[0042] **FIGURES 40-41** show embodiments of process flows for fabricating solar panels.

DETAILED DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENTS

[0043] The following description is not to be taken in a limiting sense, but is made for the purpose of describing the general principles of the present disclosure. The scope of the present disclosure should be determined with reference to the claims. Exemplary embodiments of the present disclosure are illustrated in the drawings, like numbers being used to refer to like and corresponding parts of the various drawings.

[0044] Although specific reference is made herein to a honeycomb (hexagonal) structure, the implementation of the present disclosure is generally applicable to any geometrical shape and any taper-angled trenches with arbitrary depth. The specific honeycomb implementation only serves to demonstrate the advantages and one possible implementation.

[0045] One possible semiconductor material for the 3-D TFSC is crystalline silicon (c-Si), although other semiconductor materials may also be used. One embodiment uses monocrystalline silicon as the thin film semiconductor material. Other embodiments use multicrystalline silicon, polycrystalline silicon, microcrystalline silicon, amorphous silicon, porous silicon, or a combination thereof. The designs disclosed are also applicable to other semiconductor materials such as germanium, silicon germanium, silicon carbide, a crystalline compound semiconductor, or a combination thereof. Additional applications include copper indium gallium selenide (CIGS) and cadmium telluride (CdTe) semiconductor thin films.

[0046] **FIGURE 1 (prior art)** shows an example of a prior art process flow for planar silicon lift off, to be compared to the process flows shown in **FIGURES 28-31**. At step **102**, single-crystal silicon, such as that grown by the Czochralski process,

is electrochemically etched by HF to produce two layers of porous silicon, having different porosities. The silicon is then annealed in hydrogen at step **103**.

[0047] Two new layers of differently doped silicon are then epitaxially deposited at step **104**, for a total thickness of approximately 32 microns. Wet KOH etching is used at step **105** for the surface texturing.

[0048] Step **106** is the first shadow mask step, using low-pressure chemical vapor deposition (LPCVD) to define emitter diffusion windows. Then step **107** diffuses phosphorous dopant from a solid source.

[0049] Step **108** is the second shadow mask step, providing frontside metallization. Then the emitter surface is passivated by plasma-enhanced chemical vapor deposition (PECVD) at step **109**. Step **110** provides a frontside busbar, and in step **111** the cell is glued to glass coated with MgF_2. The cell is finally separated from the silicon wafer by mechanical stress at step **112**, and back side metallization is applied in a third shadow mask step **113**. An aluminum reflector may then be applied to the back side of the cell in step **114**.

[0050] **FIGURE 2 (prior art)** shows an example of a prior art process flow for application of self-aligned selective emitter and metallization to a TFSC. First, saw damage is removed from the single-crystal p-type silicon by etching, and the surface is anisotropically etched in NaOH at step **202**. Step **203** shows application of the spin-on and dry phosphorous diffusion source, which is then rapidly annealed in step **204** to form a lightly diffused emitter. Back side metal contacts are applied in step **205** by either vacuum evaporation or screen printing. If the back side metal is screen-printed, step **206** provides for sintering to fire the metal paste and oxidize the dielectric.

[0051] In step **207**, the top dielectric layer is patterned by laser processing. Then in steps **208-212**, metal plating is applied: first the surface is etched in dilute HF to prepare it for metal plating, then electroless nickel plating is applied and sintered, then additional nickel and copper are plated, and then silver is deposited on the copper surface. Finally, edged junction isolation is performed in step **213**.

[0052] **FIGURE 3** shows an embodiment **300** of a hexagonal truncated pyramid unit cell in accordance with the present disclosure. Unit cell **300** has a top aperture **301**, a bottom aperture **302**, and 6 side walls **304**. The imaginary tip **303** of the cell is marked T and is the point at which the side walls **304** would converge if the pyramid were not truncated at its bottom aperture **302**. H_1 through H_6 denote the vertices of the hexagon defined by top aperture **301**. The empty space in the interior of the unit cell is referred to as a trench and is marked with reference number **305**.

[0053] The locations marked A and B indicate the midpoints of line segments H_1H_2 and H_4H_5, respectively. α is defined as the angle ATB, and β is defined as the angle H_6TH_3.

[0054] **FIGURES 4-10** depict several illustrative embodiments of 3-D TFSCs constructed using truncated pyramid unit cells of different shapes. **FIGURE 4** shows a substrate comprising an array of hexagonal unit cells **300**. Lines Y and Z define two planes that will be referred to when viewing cross sections of this embodiment. Although the arrangement of **FIGURE 4** will frequently be referred to to demonstrate the advantages of the present disclosure, the hexagonal structure is merely illustrative of one embodiment. **FIGURES 5-10** demonstrate some others possible embodiments, and the present disclosure is not limited to any particular choice of geometric shape for the unit cells.

[0055] **FIGURE 5** shows a substrate comprising an array of irregular hexagonal unit cells having top apertures **501** and bottom apertures **502**. As this **FIGURE** demonstrates, the unit cells need not be regular polygons.

[0056] **FIGURE 6** shows a substrate comprising an array of triangular unit cells having top apertures **601** and bottom apertures **602**.

[0057] **FIGURE 7** shows a substrate comprising an array of square unit cells having top apertures **701** and bottom apertures **702**.

[0058] **FIGURE 8** shows a substrate comprising an array of trapezoidal unit cells having top apertures **801** and bottom apertures **802**.

[0059] **FIGURE 9** shows a substrate comprising a periodic array of both hexagonal and triangular unit cells. The hexagonal unit cells have top apertures **901** and bottom apertures **902**, and the triangular unit cells have top apertures **903** and bottom apertures **904**.

[0060] **FIGURE 10** shows a substrate comprising a periodic array of both octagonal and square unit cells. The octagonal unit cells have top apertures **1001** and bottom apertures **1002**, and the square unit cells have top apertures **1003** and bottom apertures **1004**.

[0061] Although the embodiments disclosed in these **FIGURES** show periodic arrays of one or two types of unit cells, the present disclosure could be incorporated by one of ordinary skill into a substrate using any configuration of any number of differently shaped unit cells, whether periodic or non-periodic.

[0062] **FIGURE 11** shows a hexagonal truncated pyramid solar cell substrate **1100** comprising unit cells **300** and silicon

substrate frame **1101**. In one embodiment, frame **1101** has a width of between about 50 and 500 microns.

[0063] According to one aspect of the disclosed subject matter, there is provided a fabrication method for making the see-through holes on the 3-D TFSS by using self-aligned coating and etching processes. The fabrication process of making see-through holes/openings in a released 3-D TFSS includes a self-aligned thin hard mask layer coating/deposition, selective hard mask layer opening, controlled silicon etching, and subsequent cleaning steps.

[0064] **FIGURE 12** outlines the major fabrication steps of an embodiment of making see-through holes on a released 3-D TFSS. The see-through hole making process starts at step **1201** with a released and cleaned 3-D TFSS with arrayed pyramidal cavities. A hard mask layer is deposited to cover the front, back and side surfaces of the 3-D TFSS in step **1202**. The hard mask material is used to protect surfaces from the subsequent silicon etching, such a KOH etching. The mask materials may include but are not limited to thermally grown oxide (SiO_2) and LPCVD nitride. If SiO_2 is used, the oxide layer thickness may be in the range of about 0.05 um to 0.5 um. Next, at step **1203**, the hard mask layer at the bottom side (backside) of the 3-D TFSS is selectively removed by self-aligned methods, such as coating with an etch paste or liquid by, e.g., roller coating, dip coating, or screen printing. The hard mask etching material only makes contacts to the bottom tip areas of the 3-D TFSS. During the selective coating process or subsequent curing process, the hard mask layer in contact with the etchant is etched and removed. After that, the remaining etchant material is removed by cleaning. As a result, only the silicon surface at the 3-D TFSS bottom tip areas is exposed while the rest of silicon surfaces are still

covered by the hard mask layer. Next, at step **1204**, controlled silicon etching, such as KOH silicon etching, is used to form the backside openings. The size of the see-through openings is controlled by the silicon etching time. After forming the see-through holes, the remaining mask layer is removed by chemical etching and the see-through 3-D TFSS may be cleaned by standard RCA1 and RCA2 cleaning following by DI water rinsing and drying at step **1205**. The cleaned 3-D TFSS with or without see-through holes is then ready for the subsequent cell process.

[0065] **FIGURES 13A-13C** show cross-sectional views of a silicon wafer for illustrating the reusable template making process. The cross-sectional views of the template, such as the one shown in **FIGURE 4**, are cut along the ZZ plane.

[0066] **FIGURE 13A** shows a cross-sectional view of a single-crystalline or multi-crystalline silicon wafer **1250** with thickness in the range of 0.3 to 3mm. The wafer could be in a standard circular shape or a square shape of approximately 150mm x 150mm to 200mm x 200mm. If low-cost metallurgical-grade silicon is used, a gettering process may optionally be performed first. A masking layer **1251** is coated or deposited on one or both sides of the silicon wafer. A honeycomb array pattern may be made in the masking layer by photolithography. As an example, the masking layer may be a patterned photoresist layer.

[0067] **FIGURE 13B** shows a cross-sectional view of the silicon wafer after creating trenches **1255** by performing a high-rate Reactive Ion Etch (RIE). During this silicon etching, the masking layer is used to protect the silicon surfaces that are not to be etched. The silicon RIE parameters may be adjusted to produce a low-angle, near-vertical hexagonal pyramid sidewall slope. As shown here, the bottom of the trenches end within in the silicon wafer without punching through. Alternatively, the

RIE may be allowed to produce small-diameter (e.g., <5um) holes at the bottom of pyramids by punching though the substrate backside.

[0068] **FIGURE 13C** shows a cross-sectional view of the fabricated reusable silicon template after removing the remaining masking layer. A diluted HF etch may be performed to remove the native oxide and passivate the surface with hydrogen (Si-H bonds) in preparation for subsequent fabrication of 3-D TFSS.

[0069] **FIGURES 14A-14C** show cross-sectional views of a reusable silicon template for illustrating the 3-D TFSS making process. The cross-sectional views of the template, such as the one shown in **FIGURE 4**, are cut along the ZZ plane.

[0070] **FIGURE 14A** shows a cross-sectional view of the reusable template after forming a bi-layer porous silicon thin layer **1260** on its structured side. The porous silicon layer may consist of a top layer of low-porosity (20%~40%) silicon on a layer of high-porosity (40%~80%) silicon and may be formed by using electrochemical HF etching (also known as electrochemical anodization of silicon).

[0071] **FIGURE 14B** shows a cross-sectional view of the reusable template after epitaxial silicon layer **1261** has been grown in an epitaxial reactor. The epitaxial layer thickness is in the range of 2um to 50um. A hydrogen baking/annealing process may be conducted prior to the epitaxial silicon growth. The epitaxial silicon layer may be doped with p-type and/or n-type dopants during its epitaxial growing process.

[0072] **FIGURE 14C** shows a cross-sectional view of the reusable silicon template and a released 3-D TFSS **1265**. The released 3-D TFSS is ready for the subsequent cell fabrication process, while the template is cleaned by diluted silicon wet

etchant, such as diluted KOH, to remove the silicon debris. The template is then ready for the next reuse cycle.

[0073] **FIGURES 15A-15D** show cross-sectional views of a released 3-D TFSS such as the one shown in **FIGURE 4**, and cut along the ZZ plane, for illustrating the see-through hole making process.

[0074] **FIGURE 15A** shows a cross-sectional view of a released 3-D TFSS after its hard mask layer deposition process. The silicon surfaces of the 3-D TFSS are fully covered with hard mask layer **1301**, such as a thermal oxide (SiO_2) layer of 0.05um to 0.5um thickness.

[0075] **FIGURE 15B** shows a cross-sectional view of the 3-D TFSS with the hard mask layer at the bottom tip areas selectively removed by chemical etching.

[0076] **FIGURE 15C** shows a cross-sectional view of the 3-D TFSS with etched see-through holes by controlled silicon etching, such as KOH etching.

[0077] **FIGURE 15D** shows a cross-sectional view of the fabricated see-through 3-D TFSS after removal of the remaining hard mask layer, ready for subsequent cell fabrication processes.

[0078] **FIGURE 16** shows a cross-sectional view of a silicon substrate such as the one used to produce the TFSC shown in **FIGURE 4**, cut along the YY plane. Top apertures **301** and bottom apertures **302** are shown. Side walls **304** define trenches **305**. Angle α is shown, as before, as the angle that imaginary pyramid tip **303** makes with the midpoints of opposite sides of the hexagon defined by top aperture **301**.

[0079] **FIGURE 17** shows another cross-sectional view of a silicon substrate such as the one used to produce the TFSC shown in **FIGURE 4**, this time cut along the ZZ plane. Top apertures **301**

and bottom apertures **302** are shown. Side walls **304** define trenches **305**. Angle β is shown as the angle that imaginary pyramid tip **303** makes with the vertices of the hexagon defined by top aperture **301**.

[0080] **FIGURE 18** shows an embodiment of a roller setup for doping a substrate such as the partially transparent 3-D TFSCs of the present disclosure. In this embodiment, input conveyor belt **1401** moves substrate **1100** onto rollers that apply dopant paste. The rollers may rotate and press on the wafer from both sides with a controllable force. Top rollers **1402** are coated with n-type dopant paste, and bottom rollers **1403** are coated with p-type dopant paste. The wafer may then enter curing lamps **1404**, which may be infrared, ultraviolet, or another type of curing lamp. After the dopant paste has been cured, the wafer may travel out of the system by way of output conveyor belt **1410** for annealing.

[0081] **FIGURE 19** shows an embodiment of a non-contact spray coating setup for doping a substrate such as the partially transparent 3-D TFSCs of the present disclosure. In this embodiment, input conveyor belt **1401** moves substrate **1100** into a spray coating apparatus. The substrate may be air lifted or air levitated on the conveyor belt. The top side of substrate **1100** is sprayed with liquid n-type dopant by nozzles **1504**, which are fed by reservoir and pump **1502**. The bottom side is sprayed with liquid p-type dopant by nozzles **1505**, which are fed by reservoir and pump **1503**. The nozzles **1504** and **1505** may cover the entire width of the substrate as it passes between them. The nozzles **1504** and **1505** also may be angled with respect to the surface of the substrate, spraying it at a sharp angle. Then, as in **FIGURE 18**, substrate **1100** passes through curing lamps **1404**, and travels out of the system on conveyor belt **1410** for annealing.

[0082] **FIGURE 20** shows an embodiment of a dip coating setup for doping a substrate such as the partially transparent 3-D TFSCs of the present disclosure. In this embodiment, input conveyor belt **1401** moves substrate **1100** into liquid film dispensers **1604** (n-type) and **1605** (p-type). These dispensers are fed by liquid dopant source/liquid level and depth controllers **1602** and **1603**, and produce controlled-thickness liquid dopant films **1606** and **1607**, respectively. Then, as in **FIGURES 18** and **19**, substrate **1100** travels out of the system on output conveyor **1410** for annealing. All of the doping embodiments shown in **FIGURES 18-20** may be carried out at atmospheric pressure.

[0083] **FIGURE 21** shows a cross-sectional view of a 3-D TFSC such as the one of **FIGURE 4**, cut along the YY plane. A substrate may have either a thin or a thick silicon frame around its edges. The substrate shown in **FIGURE 21** has a thin silicon frame **1701** at its edges. The unit cells in **FIGURE 21** have had metallized contacts applied on both the front and back sides. Front side self-aligned base contacts **1702** cover substantially all of the hexagonal ridges making up the front of the substrate and are, in some embodiments, silver, aluminum, or some other metal. They may be formed by, for example, fire-through metallization or by plating. Front side contacts **1702** may form an interconnected hexagonal contact pattern throughout the entire substrate, because the top ridges may be in electrical contact with one another. Back side self-aligned emitter contacts **1703** may cover substantially all of the isolated hexagonal ridges making up the back side of the substrate. The back side hexagonal ridges may be isolated from one another, because the smaller back side bottom apertures do not form a continuous grid. Contacts **1703** may be made of silver, aluminum, or some other metal; they may also be formed by fire-through

metallization or by plating. The front side contacts **1702** are connected to frame-edge front side contact **1704**. Frame-edge front side contact **1704** may also be connected to frame-edge back side contact **1705** through either a wrap-around or a wrap-through connection. This connection between contact **1704** and contact **1705** may allow for simpler automation of solar module assembly. The TFSC of **FIGURE 21** may be square or rectangular with dimensions of about 150 mm to more than 200 mm.

[0084] **FIGURE 22** shows an embodiment similar to the one in **FIGURE 21**, but with a thick silicon frame **1801** in place of thin frame **1701**. The TFSC of **FIGURE 22** has not yet had metallization applied.

[0085] **FIGURE 23** shows an embodiment similar to the one in **FIGURE 22**, but after self-aligned front side base contacts and back side emitter contacts have been applied. The unit cells in **FIGURE 23** have had metallized contacts applied on both the front and back sides. Front side self-aligned base contacts **1902** cover substantially all of the hexagonal ridges making up the front of the substrate and are, in some embodiments, silver, aluminum, or some other metal. They may be formed by, for example, fire-through metallization or by plating. Front side contacts **1902** may form an interconnected hexagonal contact pattern throughout the entire substrate, because the top ridges may be in electrical contact with one another. Self-aligned back side emitter contacts **1903** may cover substantially all of the isolated hexagonal ridges making up the back side of the substrate. The back side hexagonal ridges may be isolated from one another, because the smaller back side bottom apertures do not form a continuous grid. Contacts **1903** may be made of silver, aluminum, or some other metal; they may also be formed by fire-through metallization or by plating. The front side contacts

1902 are connected to frame-edge front side contact **1904**. Frame-edge front side contact **1904** may also be connected to frame-edge back side contact **1905** through either a wrap-around or a wrap-through connection. This connection between contact **1904** and contact **1905** may allow for simpler automation of solar module assembly. The TFSC of **FIGURE 23** may be square or rectangular with dimensions of about 150 mm to more than 200 mm.

[0086] **FIGURE 24** shows a cross section along the YY plane of an embodiment of a 3-D TFSC in a solar glass application. Top window glass plate **2001** faces away from the building on which the solar glass is mounted and towards the incoming sunlight. Self-aligned front side base interconnects **2002** form a substantially continuous grid of metallization, which connects to the silicon frame at the edge of the cell (not shown). Self-aligned back side emitter contacts **2003** are in electrical contact with an electrically conductive semitransparent layer **2010**. Layer **2010** may include single or multiple layers of silver and/or metal oxide (e.g., indium tin oxide). Bottom window glass plate **2011** faces the inside of the building. The distance between top window glass plate **2001** and layer **2010** may be between approximately 6 mm and 12 mm. The space between top window glass plate **2001** and layer **2010** may be filled with, e.g., argon gas. By varying the parameters of the shape of the truncated pyramid unit cells, one may design the solar glass of **FIGURE 24** to have a desired transmissivity (e.g., from approximately 10% to approximately 90%).

[0087] **FIGURE 25** shows a view of a section of an embodiment of a partially transparent 3-D TFSC, before the application of top window glass plate **2001**. A plurality of unit cells **300** are attached to a substrate **2101**, which may be made of glass. In particular, rear emitter contacts **1703** may be either soldered or

glued to glass substrate **2101**. Glass substrate **2101** may have a thin conductive layer **2102** of, for example, silver or a transparent conductive oxide, to which rear emitter contacts **1703** may be attached. This may allow the entire solar module to be partially transparent while providing an electrical connection to all of the rear emitter contacts.

[0088] In a similar embodiment, glass substrate **2101** may be replaced with a metallic substrate, with either a rough or a specular mirror surface. This metallic substrate may serve as a light diffuser and reflector, as well as the back side interconnect plane for the rear emitter contacts **1703**.

[0089] **FIGURES 26** and **27** show two embodiments of process flows for patterning a reusable silicon substrate template, for use in producing 3-D TFSCs. The process flow of **FIGURE 26** uses direct laser micromachining to produce the surface structures of the reusable substrate template. At step **2201**, a square, unpatterned substrate of single-crystal or multi-crystalline silicon is used. The silicon may be low-cost metallurgical-grade silicon. The unpatterned substrate may be about 200 mm x 200 mm, and it may be about 200 to 600 microns in thickness. Optional gettering may be performed on the substrate to reduce the effects of impurities.

[0090] In step **2202**, a laser is used to form the micromachined patterns. A laser-assisted chemical etch may optionally be used in combination with the physical laser ablation. Then in step **2205**, the reusable substrate is cleaned by, for example, RCA cleaning. A final etch with dilute hydrofluoric acid may remove the native oxide layer and passivate the surface with Si-H bonds. The reusable substrate may then be used for fabrication of hundreds of 3-D TFSCs, as discussed in connection with **FIGURES 28-31**.

[0091] **FIGURE 27** describes an alternate process flow for patterning a reusable silicon substrate using photolithography. In this embodiment, the same low-cost metallurgical grade silicon may be used. In step **2303**, a spin-on glass hard mask layer is optionally applied to the substrate and cured, and then photoresist is applied. The photoresist is exposed through an array mask having the desired shapes for the 3-D structures to be created, and then developed. If the optional spin-on glass has been applied, it must also then be etched to expose the substrate. In step **2304**, reactive ion etching is used to pattern the trenches into the substrate. In step **2305**, the photoresist and optional spin-on glass hard layer are stripped in a wet bench. Then the substrate is cleaned and passivated as in **FIGURE 27**.

[0092] **FIGURES 28-31** show embodiments of some process flows for creating self-supported 3-D TFSCs from reusable silicon substrates such as the ones that may be made by the processes of **FIGURES 27** and **28**, by using layer release processing techniques.

[0093] In **FIGURE 28**, the process begins at step **2401** with a patterned reusable substrate. Multi-layer epitaxy is performed at step **2403**. Then a highly selective isotropic etch process is performed at step **2404** to release the newly formed silicon film.

[0094] In **FIGURE 29**, there is an initial HF electrochemical etching in a wet bench at step **2502**. This produces a bilayer stack of porous silicon with two different porosities. Then epitaxy is performed in step **2503**, and the film is released by applying mechanical stress to the substrate.

[0095] In **FIGURE 30**, a thin bottom sacrificial release layer (e.g., SiO_2) is first deposited on the reusable substrate at step **2602**. The bottom sacrificial release layer may be formed by atmospheric pressure chemical vapor deposition (APCVD), low

pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD). Then a doped silicon layer is deposited by PECVD in step **2604**. Another sacrificial layer, this time a top protective layer, is deposited in step **2605**. At step **2606**, the doped silicon layer is laser crystallized using a single-crystal silicon frame as the seed crystal. Finally, the silicon film is released by highly selective isotropic HF wet etching at step **2607**.

[0096] The process flow in **FIGURE 31** differs in that in step **2703**, the bottom holes of the reusable substrate's bottom holes. Then the laser crystallization proceeds in step **2706** by using the single-crystal islands at the bottoms of the pyramids as seed crystals.

[0097] **FIGURES 32-39** show embodiments of some process flows for doping and metallizing 3-D TFSCs, such as the ones made by the process flows of **FIGURES 28-31**.

[0098] In **FIGURE 32**, start at step **2801** with a 3-D TFSC such as one produced by the preceding processes. At step **2802**, the tops of the pyramids (hexagonal in this embodiment) are coated with n-type dopant, which is then cured. The self-aligned selective emitter is formed at step **2804** by annealing the dopant layer. At step **2805**, the dopant source and native oxide layer are stripped in dilute HF, a thin new oxide layer is formed, and a SiN_x anti-reflective coating layer is applied. At step **2807**, both sides of the pyramids are coated with metal paste, which is then cured; at step **2808**, this is then fired through the oxide and SiN_x layers to form the metallization. Optional step **2809** adds either copper or silver plating to the already-formed metallization, and optional step **2810** provides a forming gas anneal to reduce resistance and help with passivation. At step **2811**, the back side of the cell is connected to a mirror, which

also serves as the back side electrical contact; the cell is then ready to be packaged into solar modules at step **2814.**

[0099] **FIGURE 33** provides an embodiment similar to the one shown in **FIGURE 32.** In **FIGURE 33,** however, the forming gas anneal takes place before the copper/silver plating step instead of after.

[00100] **FIGURE 34** provides a similar embodiment to the one shown in **FIGURE 32.** In **FIGURE 34,** however, at step **3003,** the bottoms of the pyramids are coated with p-type dopant to form p^+ doping on the rear tips during the annealing at step **3004.**

[00101] **FIGURE 35** provides a similar embodiment to the one shown in **FIGURE 34,** but with a different method of metallization. After the anti-reflective coating is applied at step **3105,** the front ridges and rear tips of the pyramids are etched at step **3108.** Then the front and rear metallized regions are formed by plating at step **3109.** After an optional forming gas anneal at step **3110,** either copper or silver is plated onto the metallized regions on the front and the back of the cell at step **3111.**

[00102] **FIGURE 36** provides a similar embodiment to the one shown in **FIGURE 34,** but without rear side boron p^+ doping. After the etching in step **3208,** the rear side only is plated with aluminum at step **3209,** and then both sides are plated at step **3210.** The cell is annealed at step **3211** to form aluminum-doped rear tips, and to reduce resistance and passivate. After annealing, either copper or silver may be deposited on the metallized front and back surfaces at step **3212.**

[00103] **FIGURE 37** shows a different embodiment of a process flow for doping and metallizing a 3-D TFSC. As in the other embodiments, we start at step **3301** with a 3-D TFSC such as one produced by the preceding processes. At steps **3302** and **3303,**

respectively, the top and bottom portions of the pyramids are coated with dopant, which is then cured. The doped regions are then annealed at step **3304**, first in an inert gas, then in oxidizing steam. The dopant source and a small amount of oxide are then removed by etching at step **3306**. At step **3308**, the front and rear metallized regions are formed in a single plating process. Then at step **3309**, aluminum or silver may be plated onto the metallized top ridges and rear tips. At step **3310**, the cell back side is soldered onto a mirror, which also serves as an electrical connector. An anti-reflective layer is deposited on both the front and the back surfaces at step **3311**, and finally an optional forming gas anneal is performed at step **3312**.

[00104] **FIGURE 38** provides an embodiment similar to the one shown in **FIGURE 37**. In **FIGURE 38**, however, at step **3411**, the anti-reflective coating is applied only to the front surface of the cell, rather than to both surfaces concurrently.

[00105] **FIGURE 39** provides an embodiment similar to the one shown in **FIGURE 38**. However, the two plating steps **3408** and **3409** have been replaced by a single silver plating step **3508**.

[00106] **FIGURES 40** and **41** show two embodiments of process flows for fabricating solar panels from the 3-D TFSCs of the present disclosure. In **FIGURE 40**, begin with a PCB coated on both sides with copper foil at step **3601**. The copper is then patterned with interconnects, and then flash coated with reflective silver at step **3602**. The TFSCs are prepared and soldered in place at steps **3603** and **3604**. Finally, the PCB is laminated in a stack with glass, an encapsulant, the PCB itself, another encapsulant and a back sheet at step **3605**.

[00107] **FIGURE 41** is similar to the process flow shown in **FIGURE 40** up through step **3704**. It differs in that the

lamination at step **3705** omits the glass and first encapsulant layer. Then at step **3706**, the front side of the panel may be coated with a thin layer of glass and an anti-reflective coating.

[00108] The foregoing description of embodiments is provided to enable a person skilled in the art to make or use the claimed subject matter. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the innovative faculty. Thus, the claimed subject matter is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

1. A three-dimensional thin film silicon substrate comprising:

a first plurality of unit cells; and

a second plurality of unit cells; wherein each said unit cell comprises:

a top aperture having a top aperture diameter;

a bottom aperture having a bottom aperture diameter;

a wall connecting said top aperture and said bottom aperture;

wherein said top aperture and said bottom aperture comprise a single convex polygon shape; and

wherein said top aperture diameter is larger than said bottom aperture diameter.

2. The substrate of claim 1, wherein:

said convex polygon shape is a hexagon.

3. The substrate of claim 1, wherein:

said convex polygon shape is a quadrilateral.

4. The substrate of claim 1, wherein:

said convex polygon shape is a triangle.

5. The substrate of claim 1, wherein:

said top and bottom apertures of said unit cells in said first plurality of unit cells comprise a first convex polygon shape;

said top and bottom apertures of said unit cells in said second plurality of unit cells comprise a second convex polygon shape; and

said first convex polygon shape is the same as said second convex polygon shape.

6. The substrate of claim 1, wherein:

said top and bottom apertures of said unit cells in said first plurality of unit cells comprise a first convex polygon shape;

said top and bottom apertures of said unit cells in said second plurality of unit cells comprise a second convex polygon shape; and

said first convex polygon shape is not the same as said second convex polygon shape.

7. A method for making a three-dimensional thin film solar cell, comprising:

patterning a reusable semiconductor template with a plurality of convex polygonal trenches;

forming a sacrificial layer on a surface of said reusable semiconductor template;

depositing a silicon film onto said sacrificial layer;

removing said silicon film from said reusable semiconductor template;

removing a plurality of tips from said silicon film to create a plurality of holes;

doping said silicon film; and

metallizing said silicon film.

8. The method of claim 7, wherein said patterning step comprises laser micromachining.

9. The method of claim 7, wherein said patterning step comprises photolithography and reactive ion etching.

10. The method of claim 7, wherein said sacrificial layer comprises a bilayer of porous silicon.

11. The method of claim 7, wherein said forming step further comprises:

producing a layer of a silicon germanium compound.

12. The method of claim 7, wherein said forming step further comprises:

producing a layer of silicon dioxide.

13. The method of claim 7, wherein said depositing step comprises:

growing said silicon film epitaxially; and

doping said silicon film in-situ.

14. The method of claim 7, wherein said depositing step comprises a doped chemical vapor deposition step chosen from the group consisting of PECVD and LPCVD.

15. The method of claim 7, wherein said step of removing said silicon film from said reusable semiconductor template comprises:

mechanically separating said silicon film from said sacrificial layer.

16. The method of claim 7, wherein said step of removing said silicon film from said reusable semiconductor template comprises:

chemically etching said sacrificial layer.

17. The method of claim 7, wherein said doping step comprises:

doping a first side of said silicon film with a p-type dopant; and

doping a second side of said silicon film with an n-type dopant.

18. The method of claim 7, wherein said metallizing step comprises fire-through metallization.

19. A method for making holes in a silicon substrate having a plurality of tips comprising:

depositing a hard masking layer on the substrate;

selectively removing said hard masking layer from the plurality of tips;

etching the substrate to remove the plurality of tips; and

removing a remainder of said hard masking layer.

20. The method of claim 19, wherein said hard masking layer comprises silicon oxide.

21. The method of claim 19, wherein said hard masking layer comprises silicon nitride.

22. The method of claim 19, wherein said etching step comprises KOH etching.

23. The method of claim 19, further comprising a step of cleaning the substrate after said step of removing said remainder of said hard masking layer.

24. The method of claim 23, wherein said cleaning step comprises RCA1 and RCA2 cleaning.

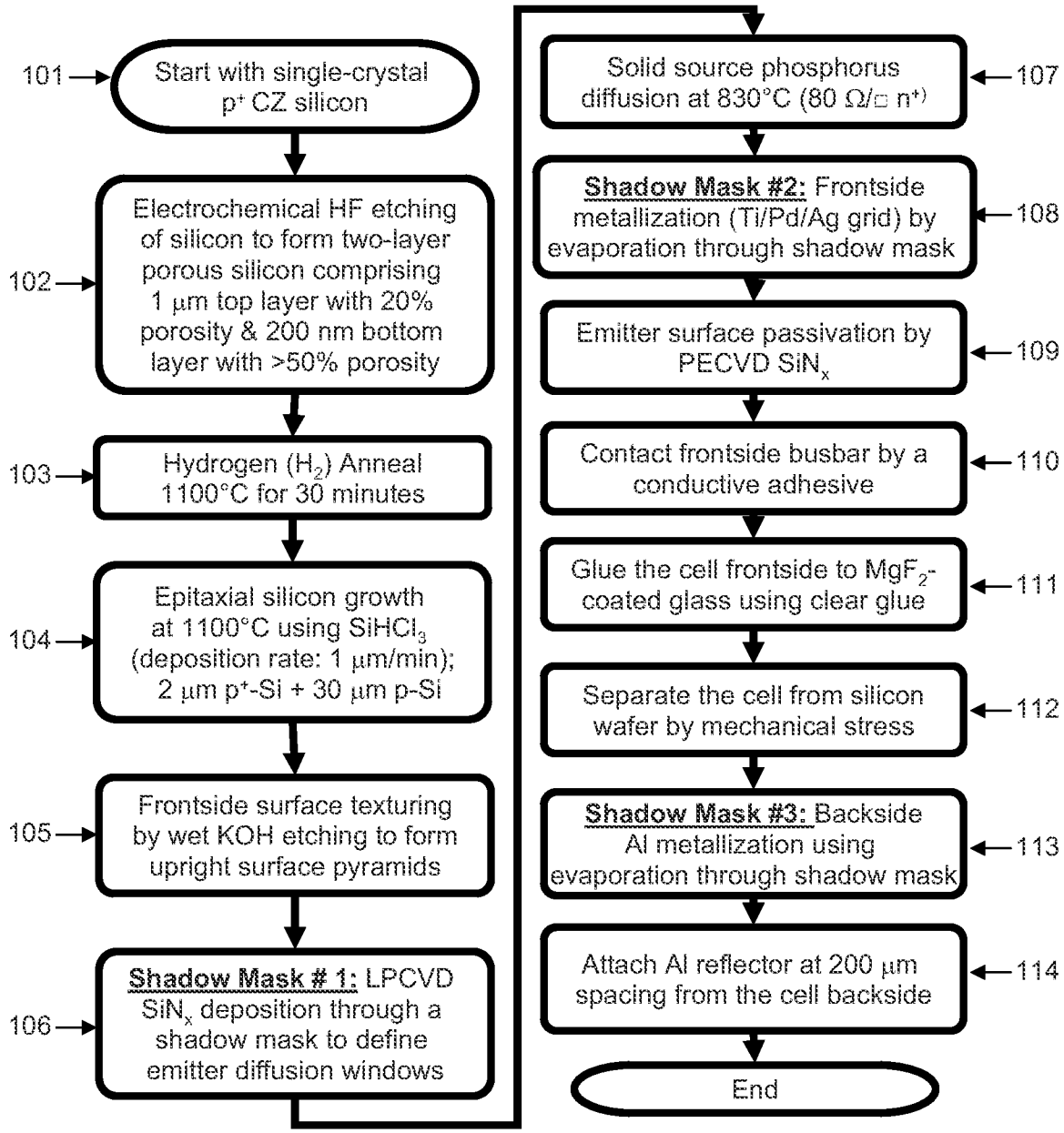


FIG. 1 (PRIOR ART)

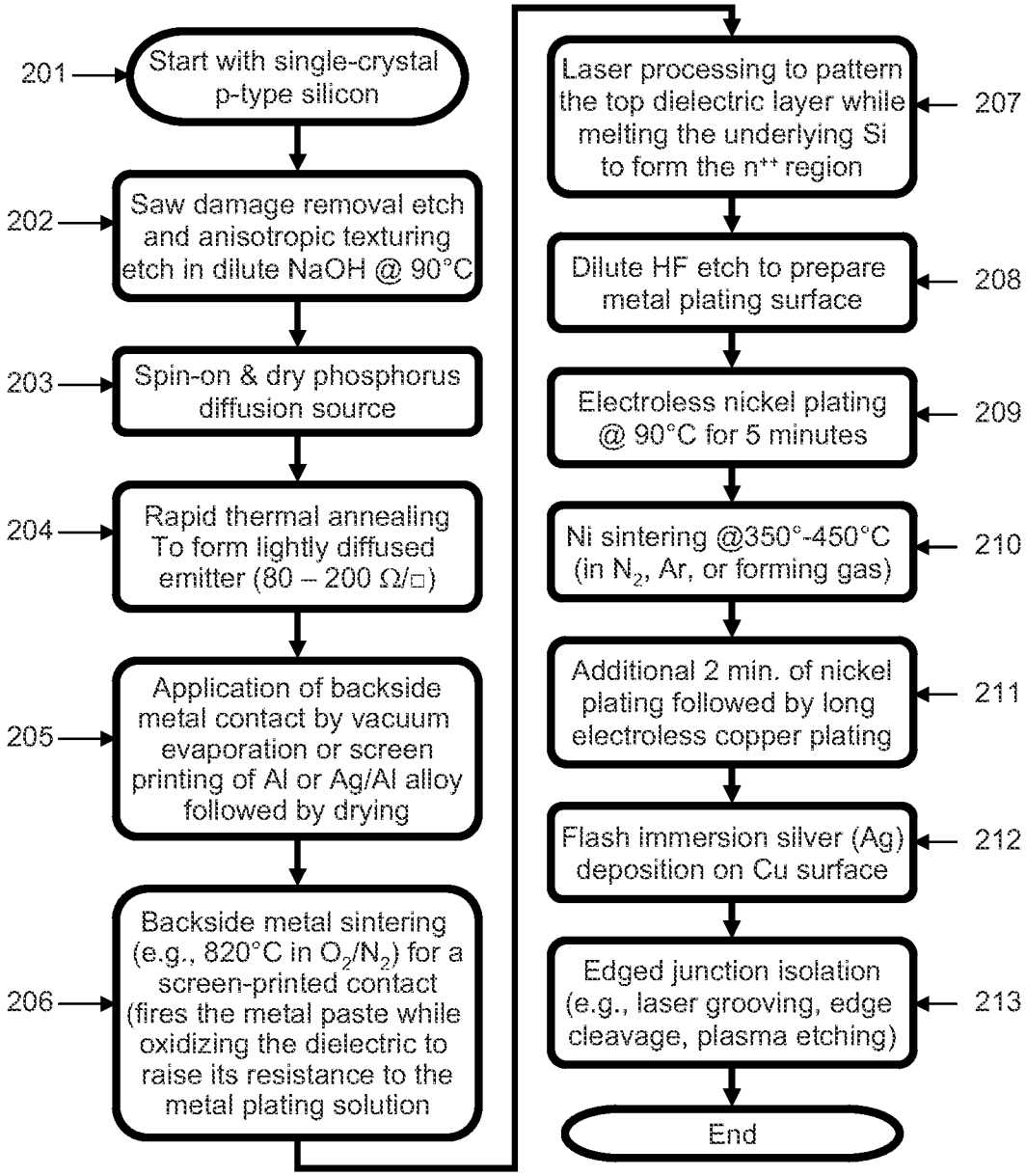
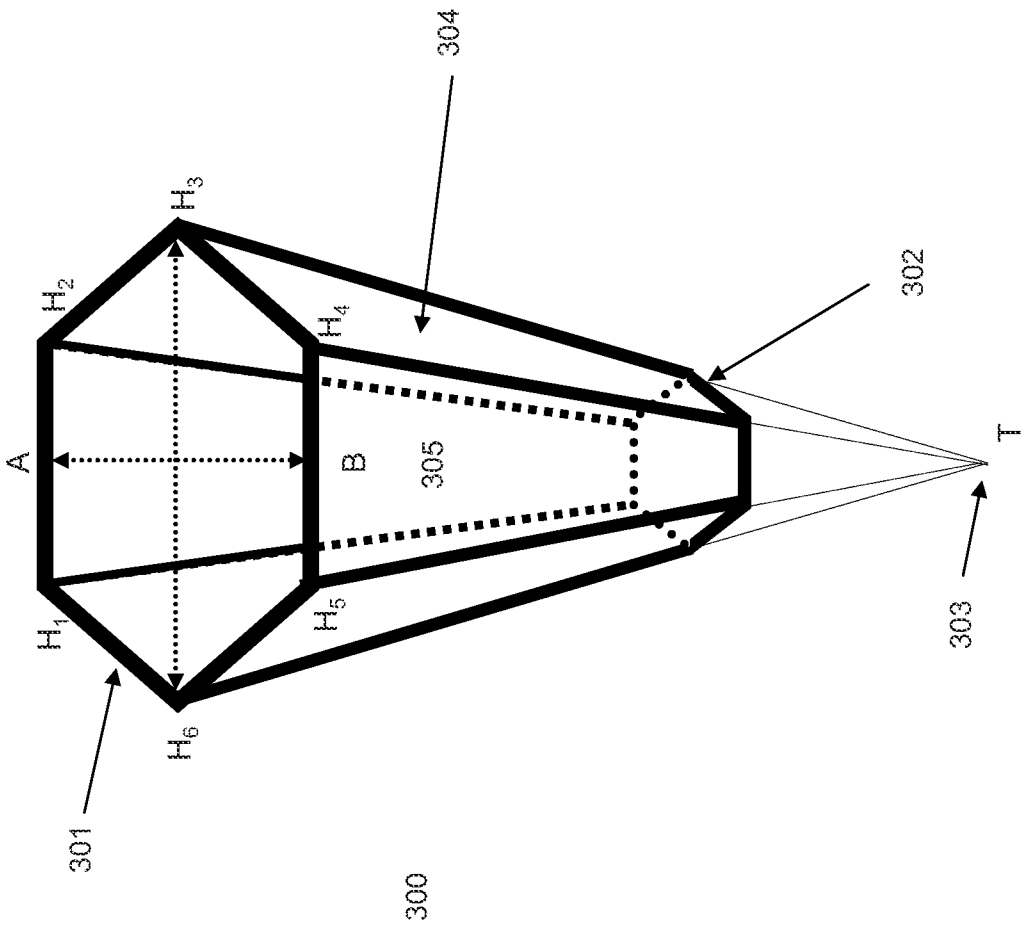


FIG. 2 (PRIOR ART)

FIG. 3



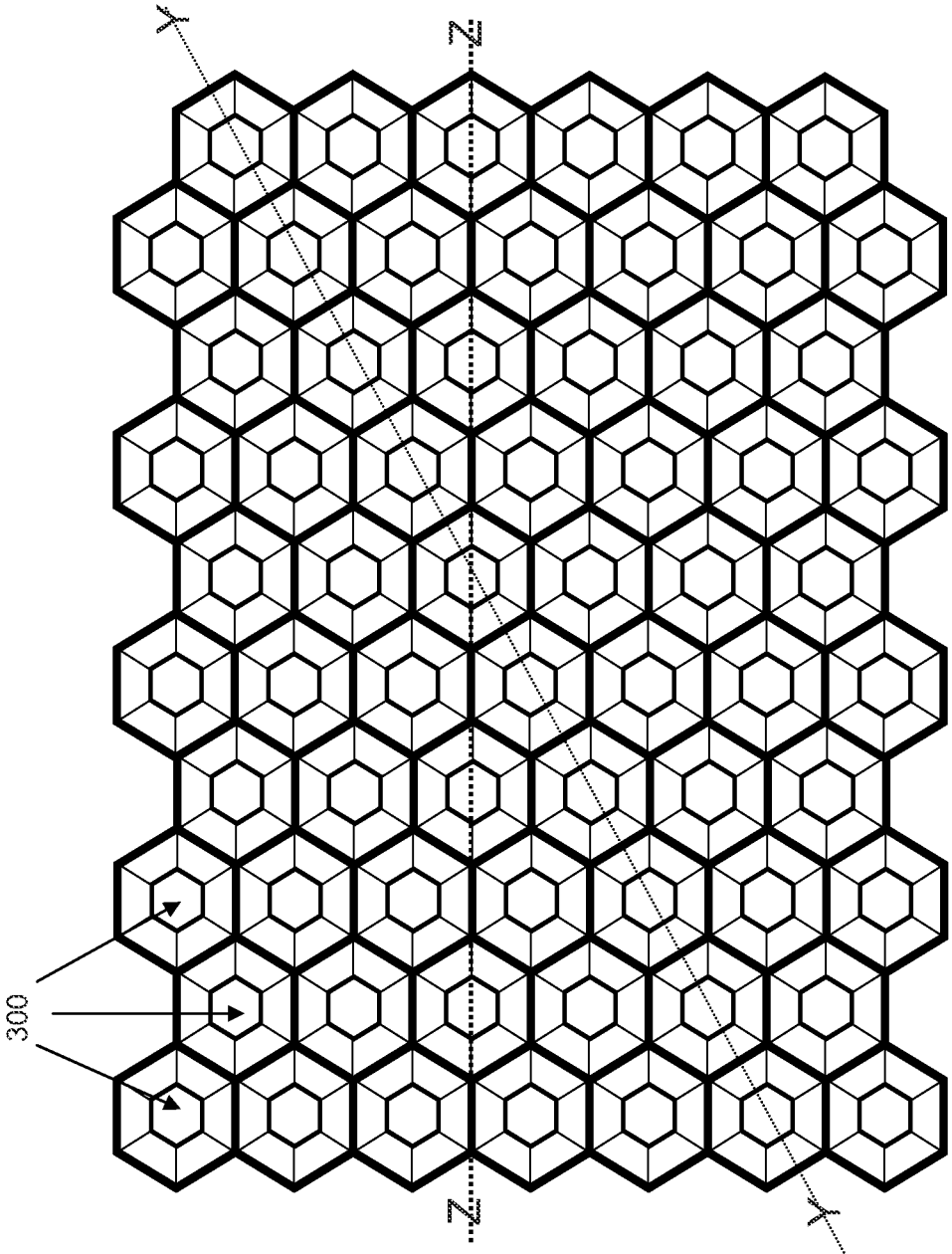


FIG. 4

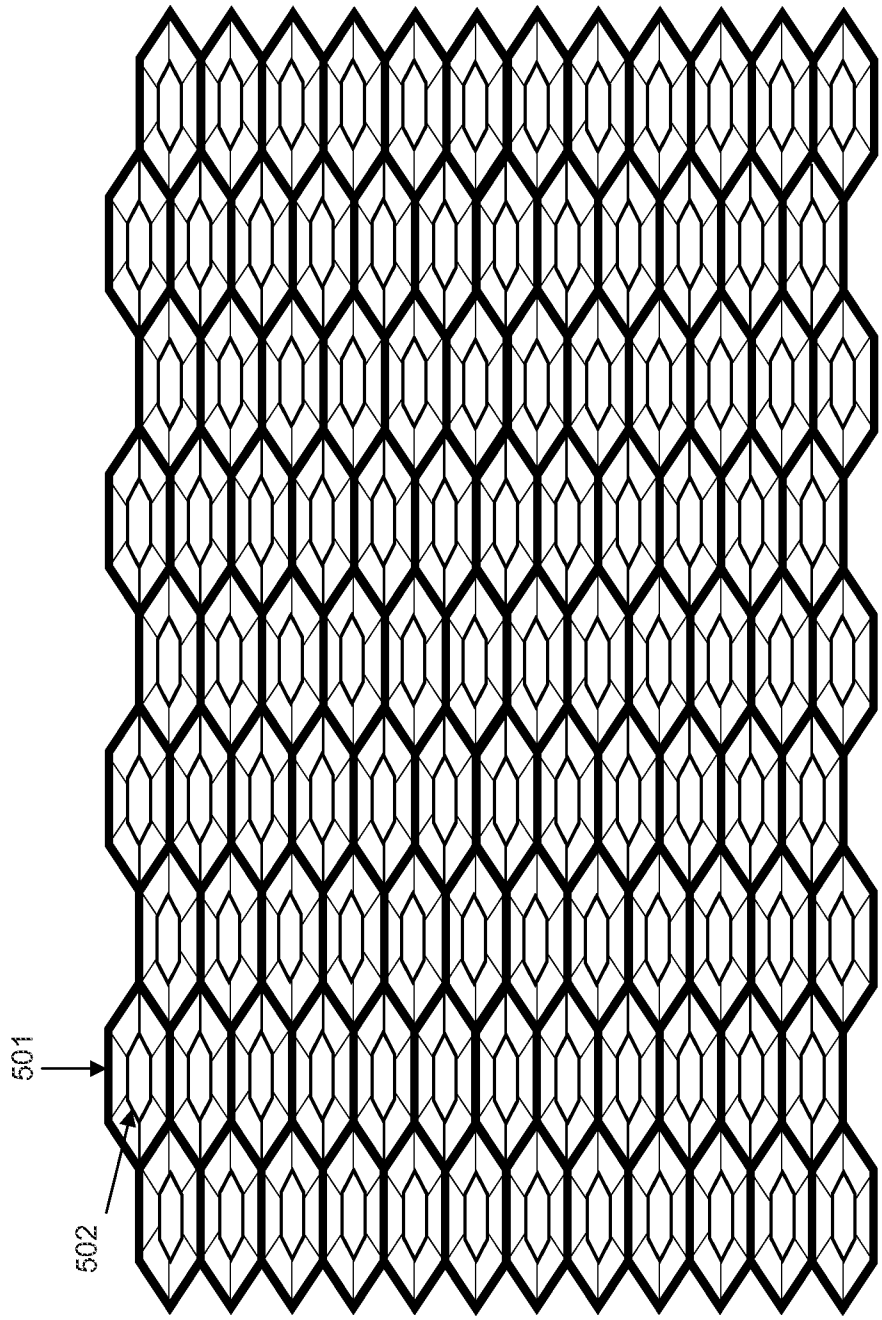


FIG. 5

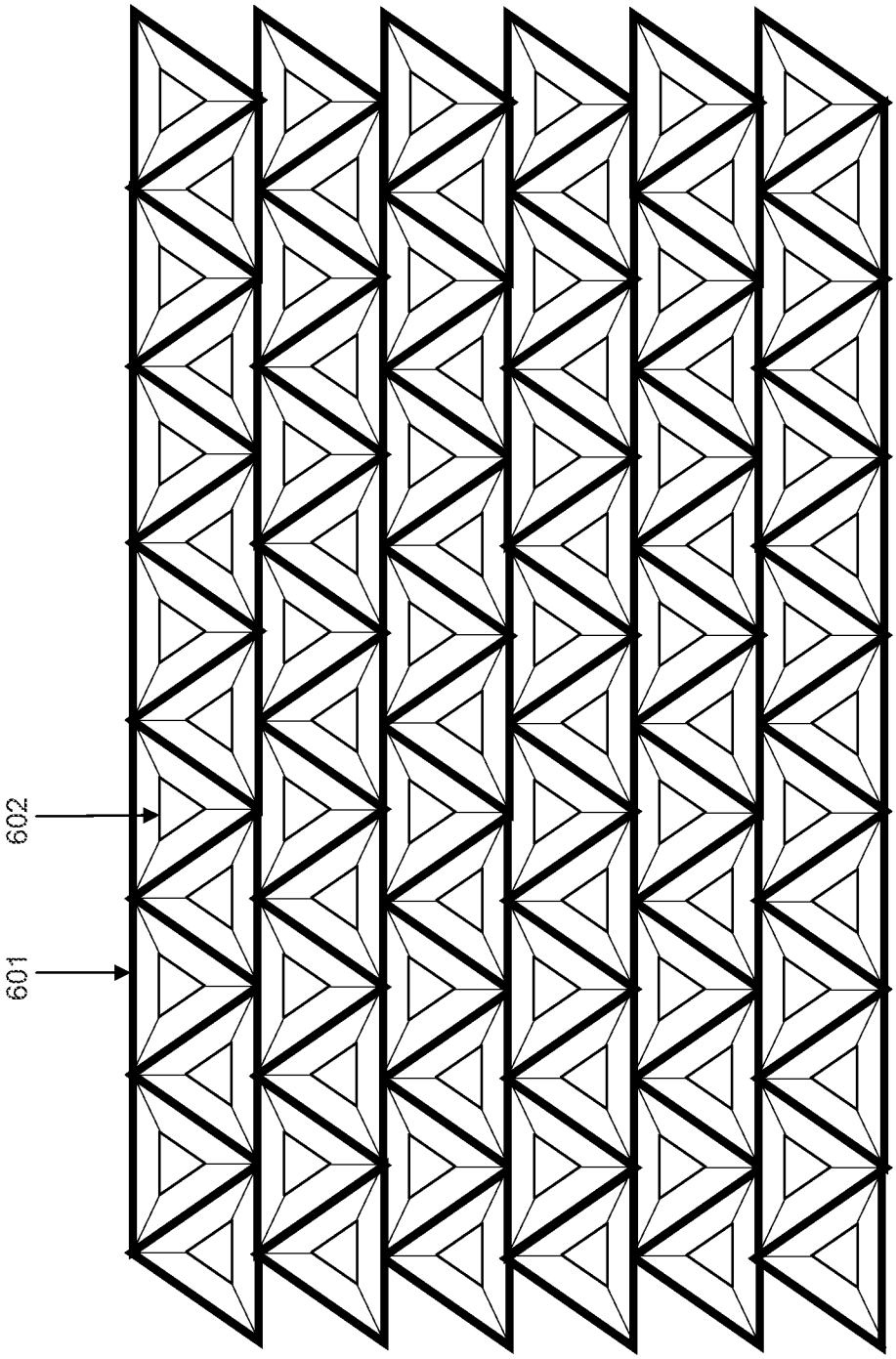


FIG. 6

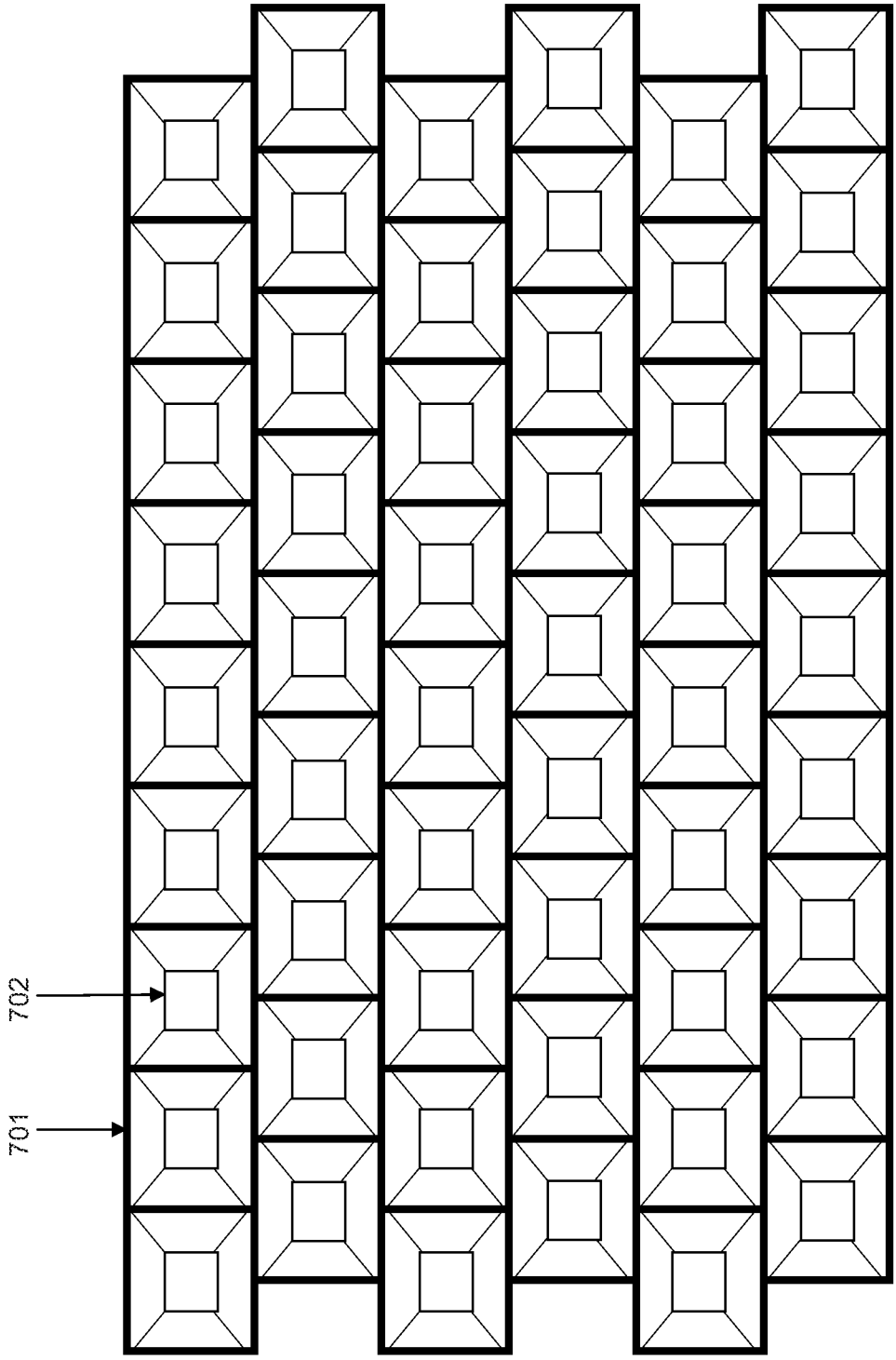


FIG. 7

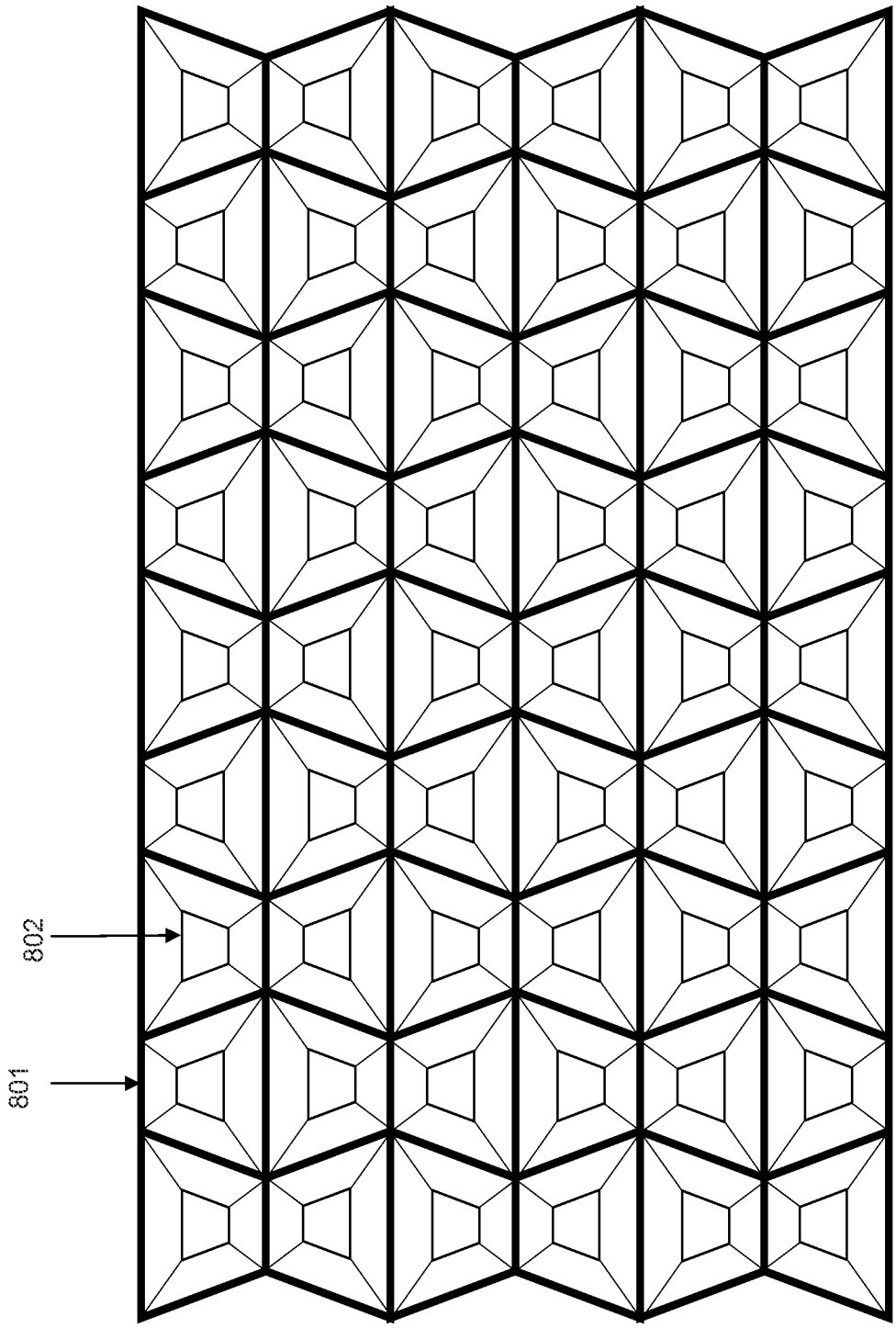


FIG. 8

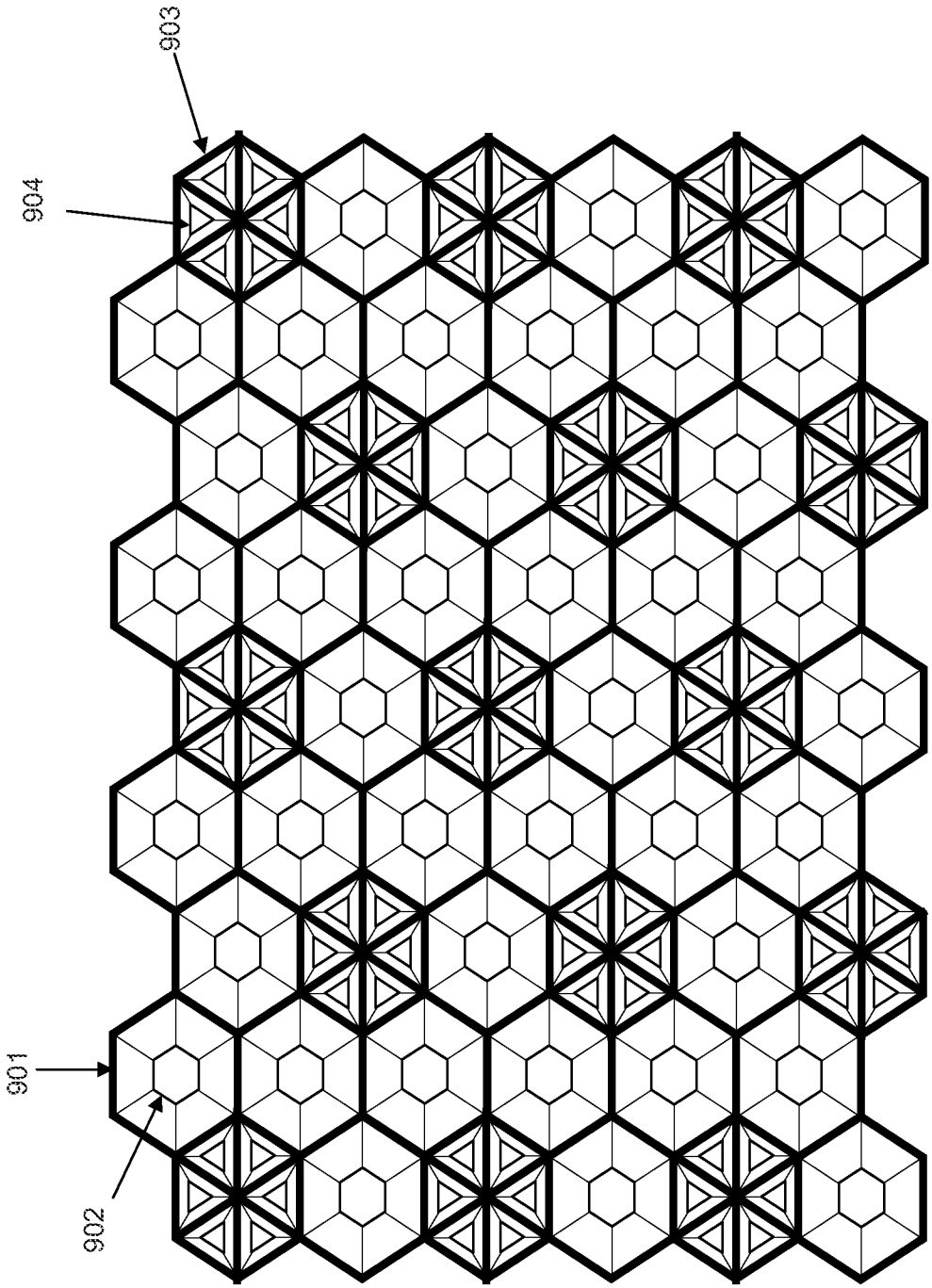


FIG. 9

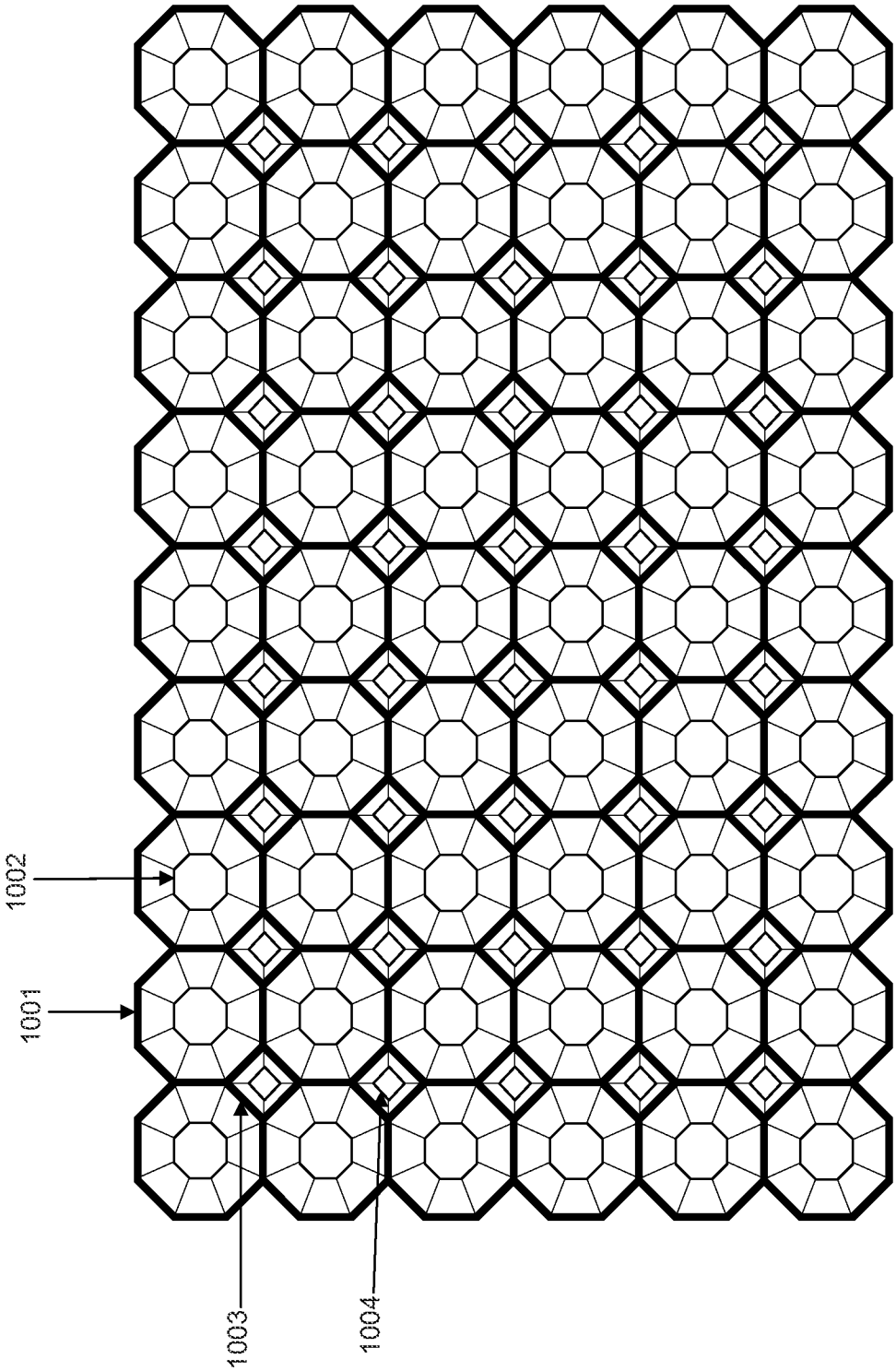


FIG. 10

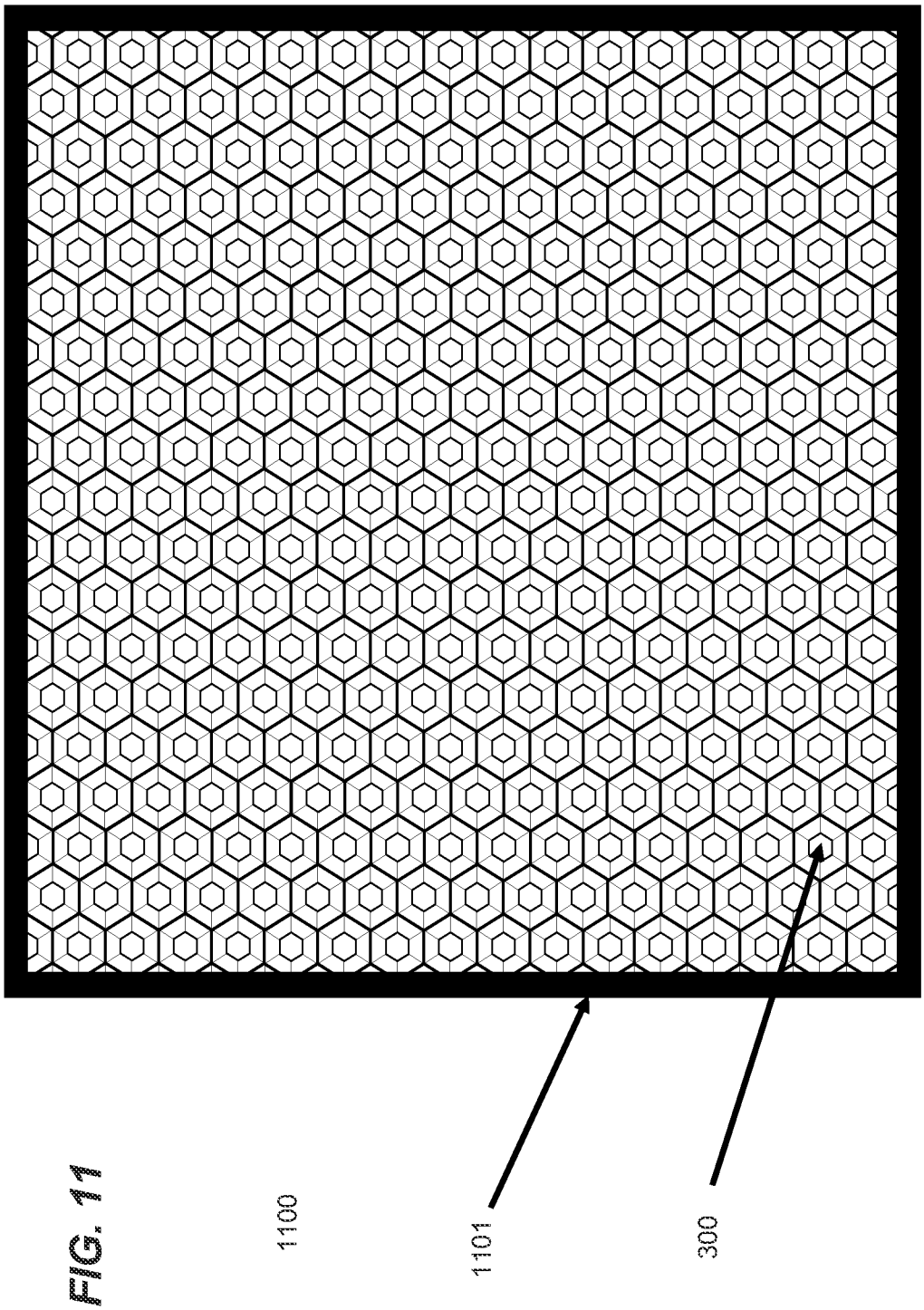


FIG. 11

FIG. 12

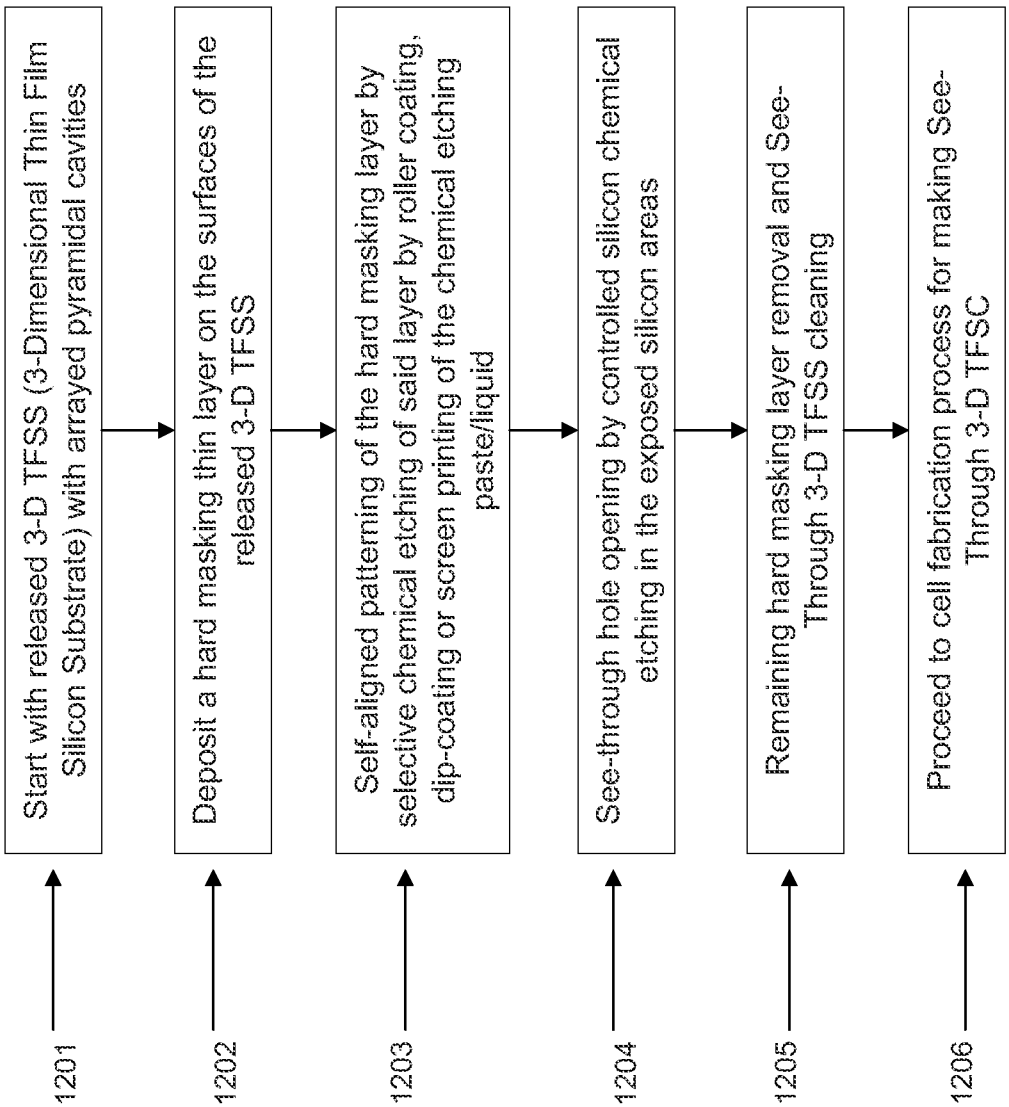

Start with released 3-D TFSS (3-Dimensional Thin Film Silicon Substrate) with arrayed pyramidal cavities
Deposit a hard masking thin layer on the surfaces of the released 3-D TFSS
Self-aligned patterning of the hard masking layer by selective chemical etching of said layer by roller coating, dip-coating or screen printing of the chemical etching paste/liquid
See-through hole opening by controlled silicon chemical etching in the exposed silicon areas
Remaining hard masking layer removal and See-Through 3-D TFSS cleaning
Proceed to cell fabrication process for making See-Through 3-D TFSC
1201
1202
1203
1204
1205
1206

FIG. 13A

FIG. 13B

FIG. 13C

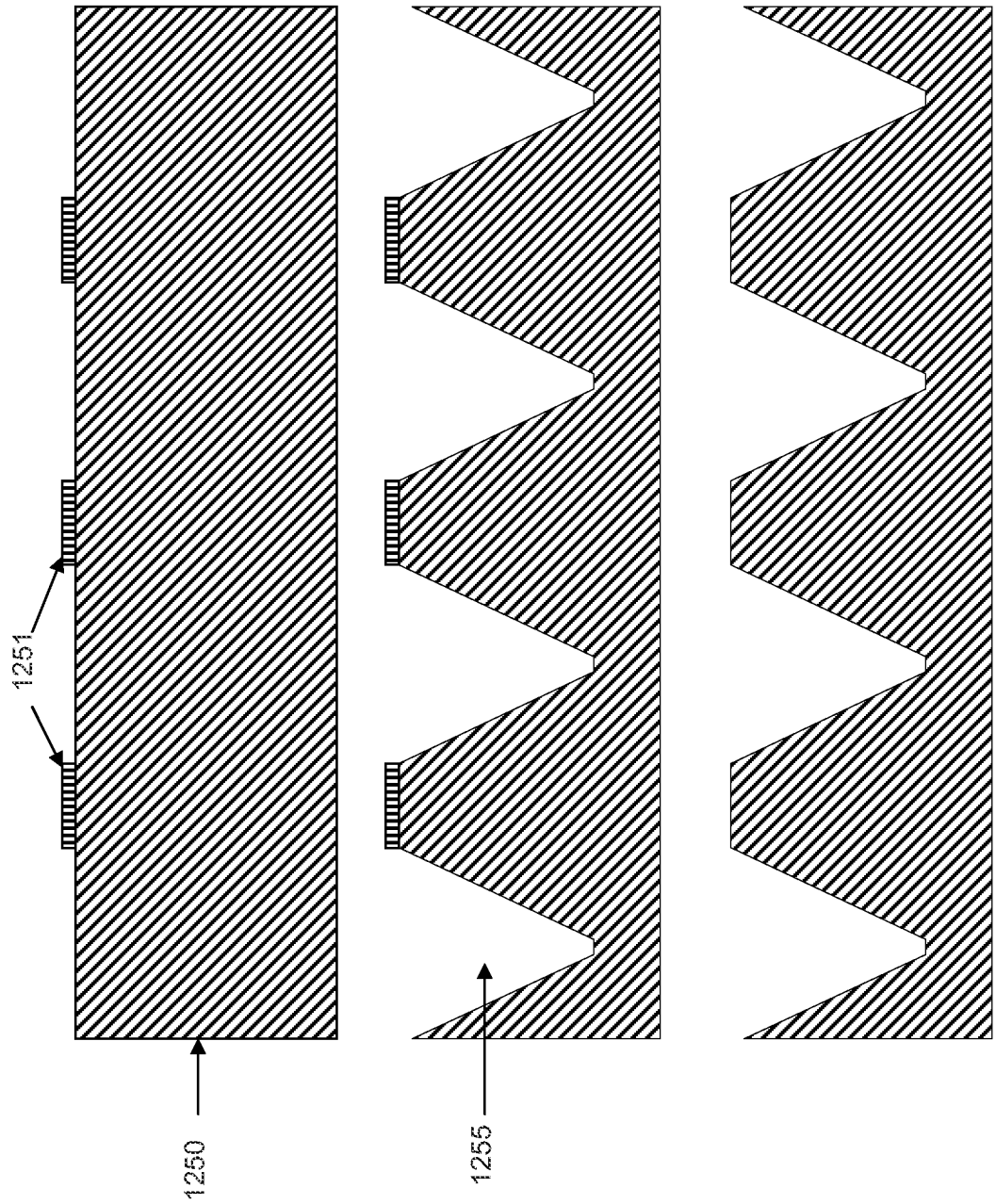


FIG. 14A

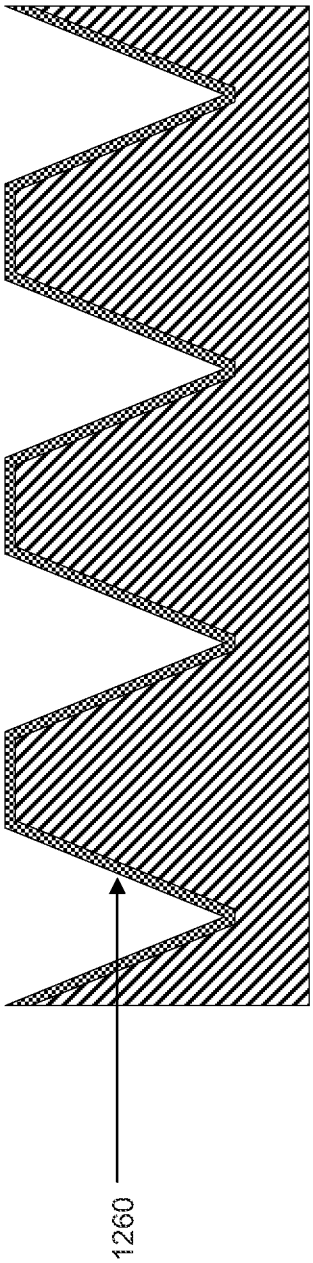


FIG. 14B

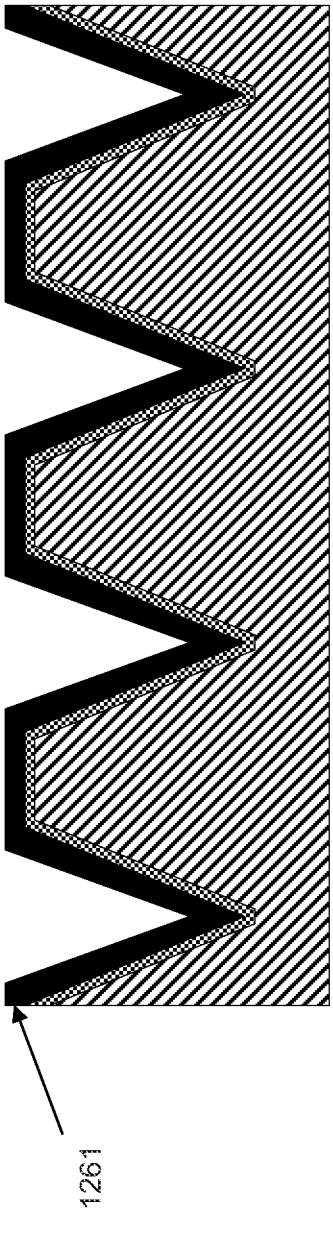


FIG. 14C

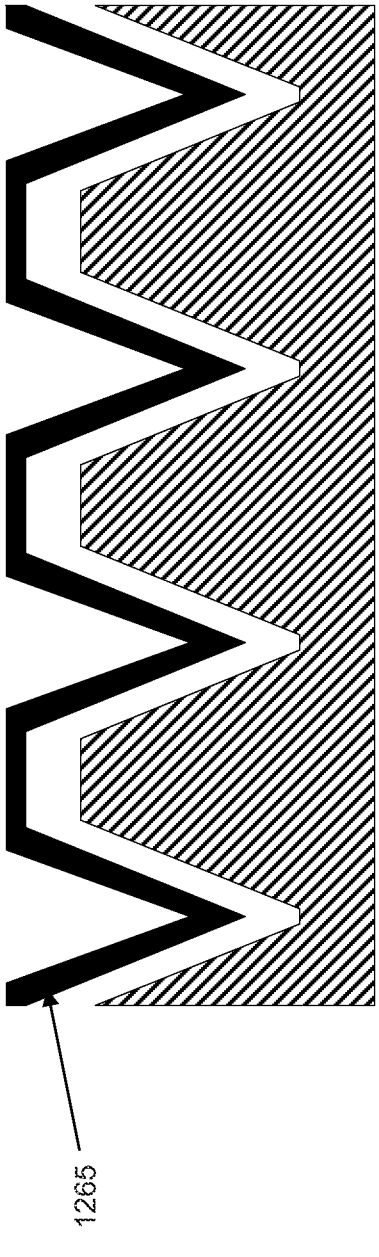


FIG. 15A

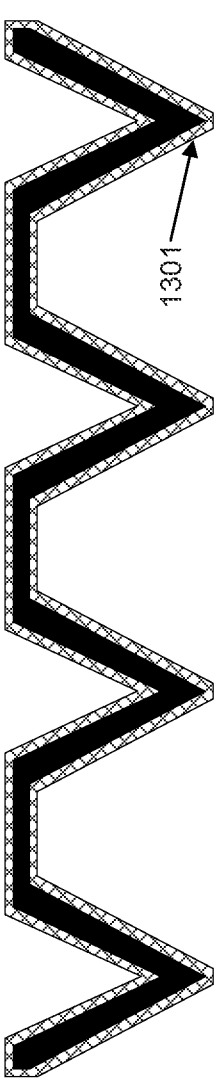


FIG. 15B

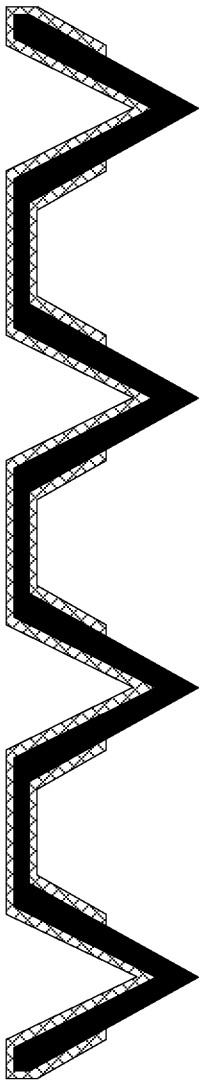


FIG. 15C

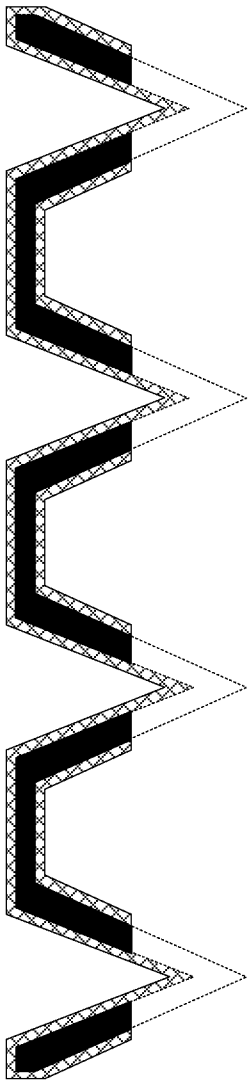
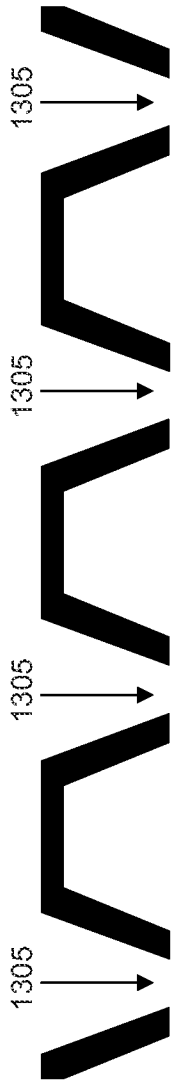


FIG. 15D



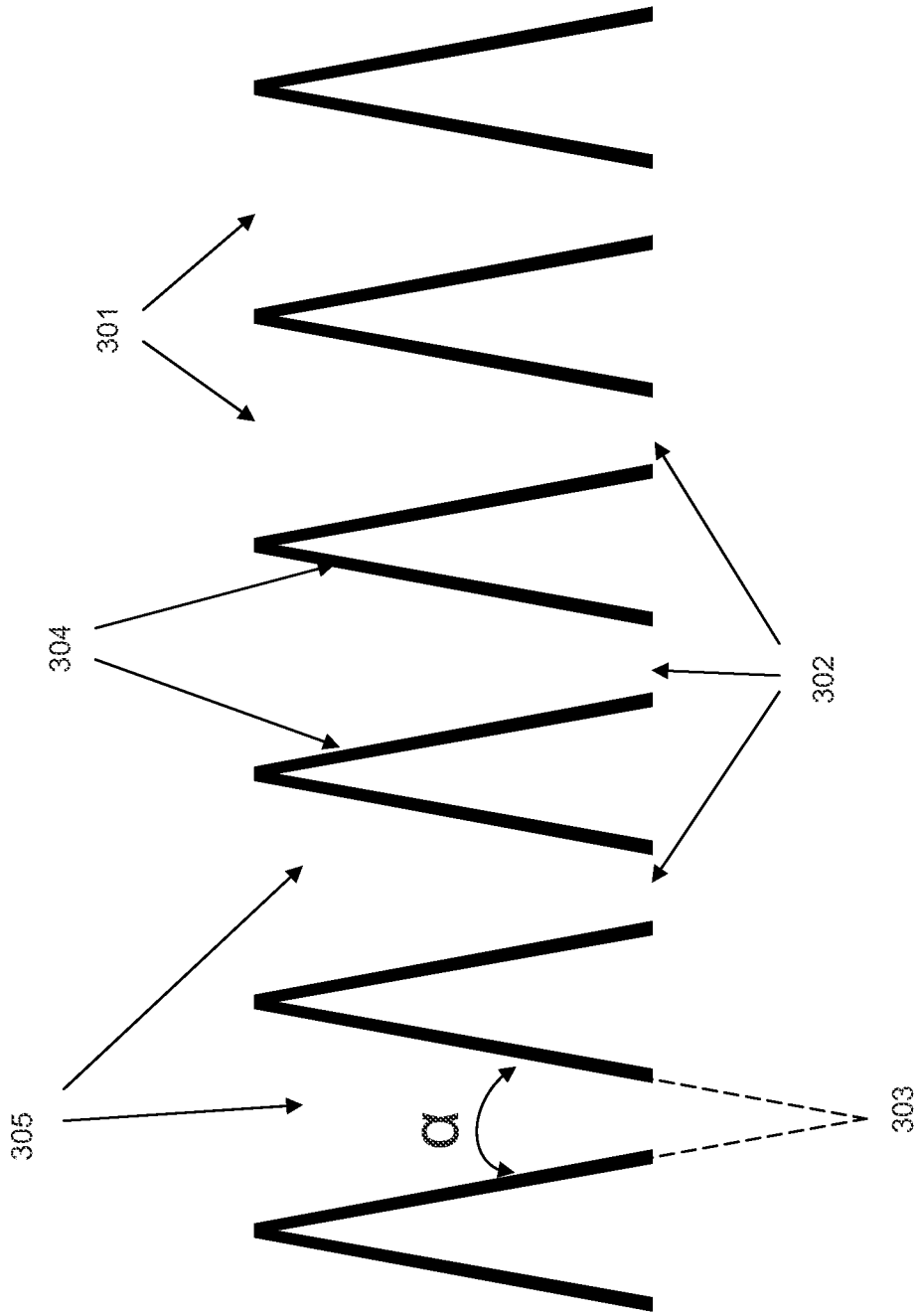


FIG. 16

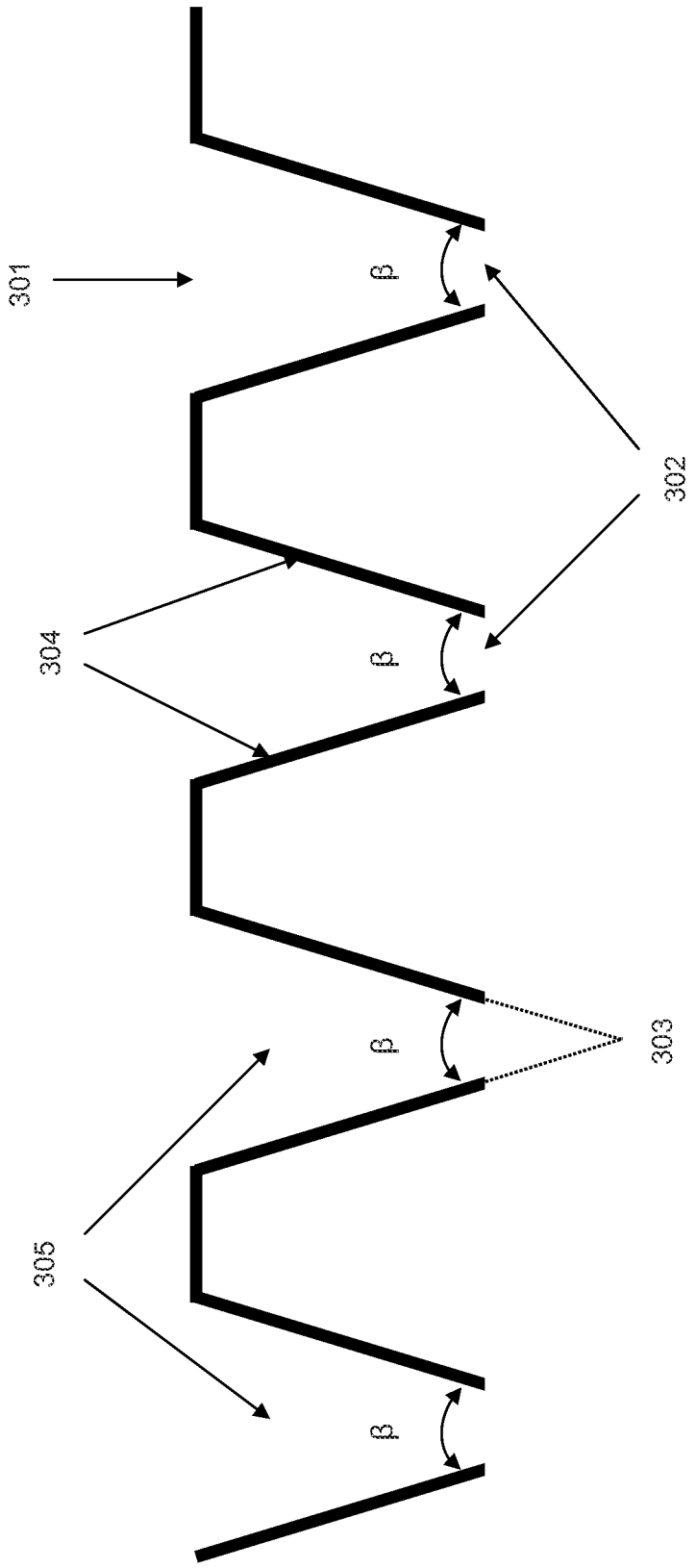


FIG. 17

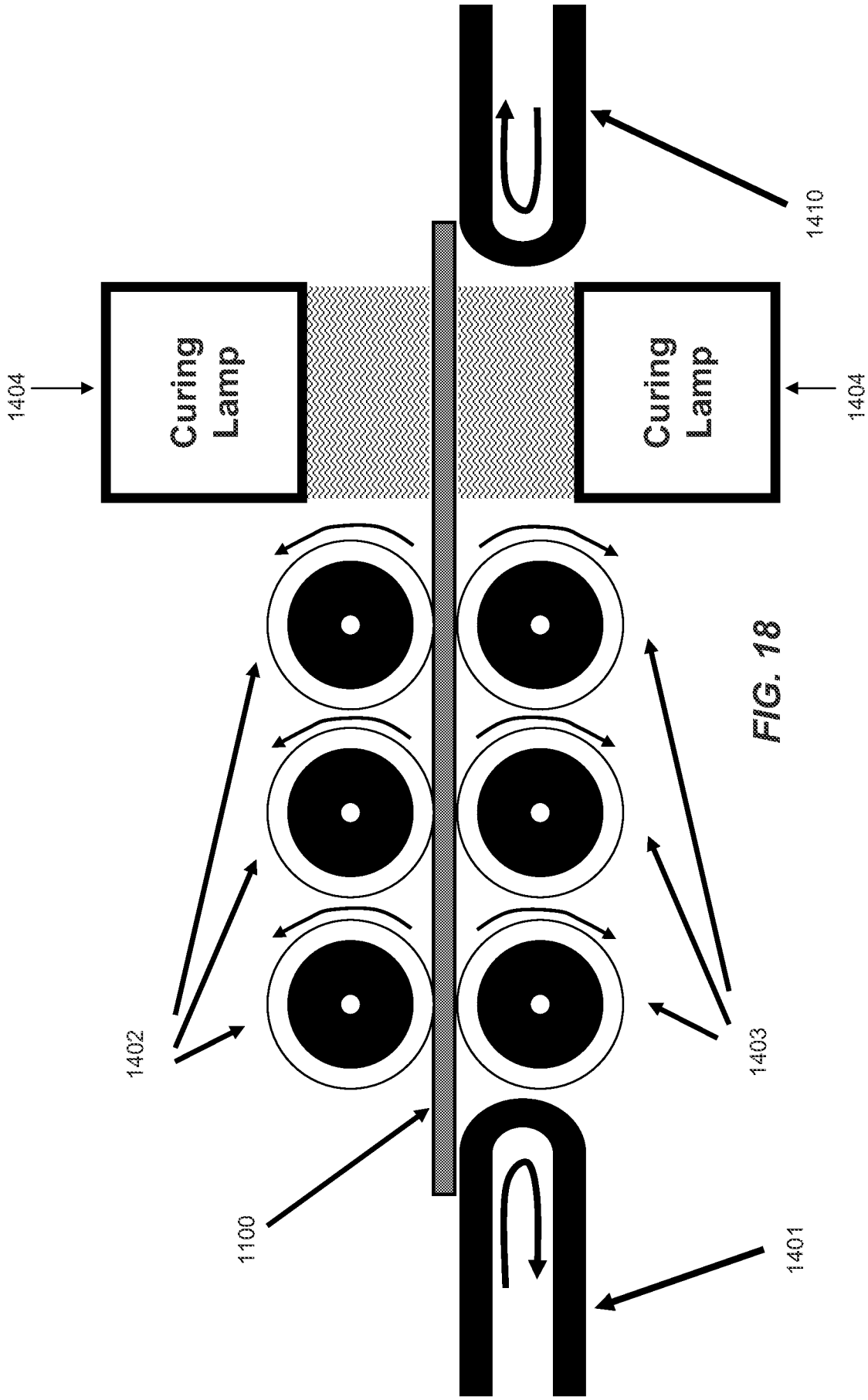


FIG. 18

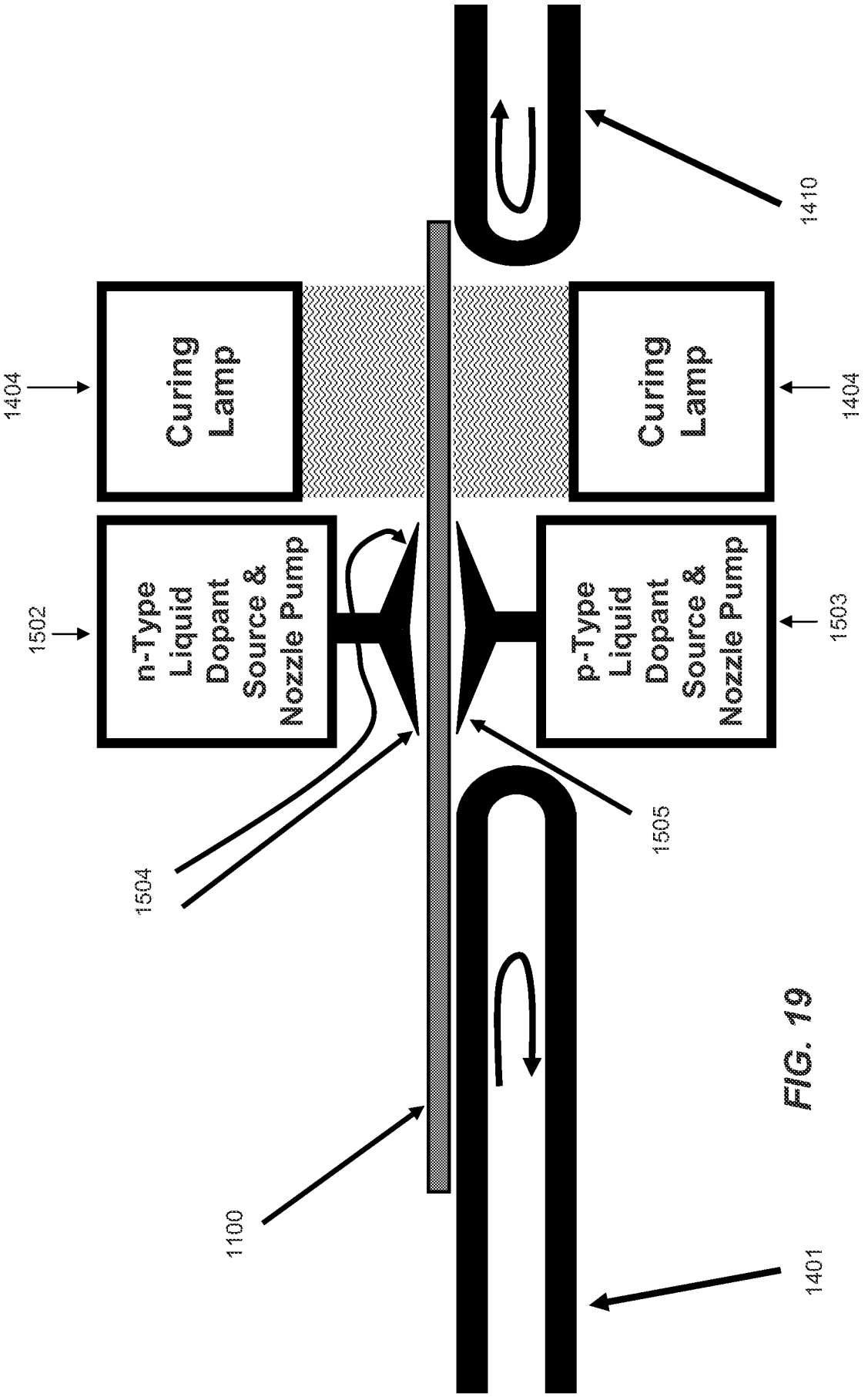

1410
1404
Curing Lamp
Curing Lamp
1404
1502
n-Type Liquid Dopant Source & Nozzle Pump
p-Type Liquid Dopant Source & Nozzle Pump
1503
1504
1505
1100
1401

FIG. 19

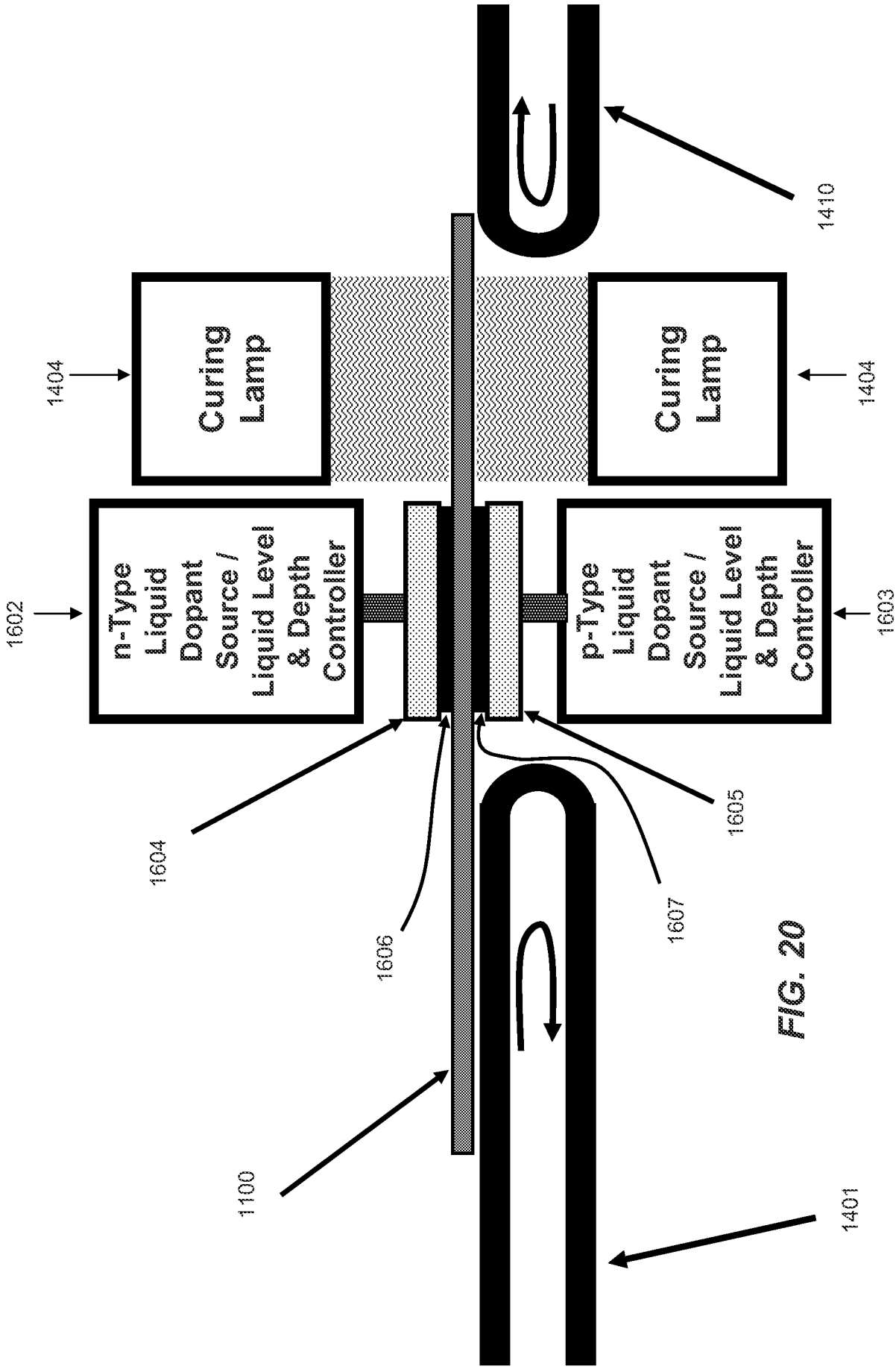

1410
1404
Curing Lamp
Curing Lamp
1404
1602
n-Type Liquid Dopant Source / Liquid Level & Depth Controller
p-Type Liquid Dopant Source / Liquid Level & Depth Controller
1603
1604
1605
1606
1607
1100
1401

FIG. 20

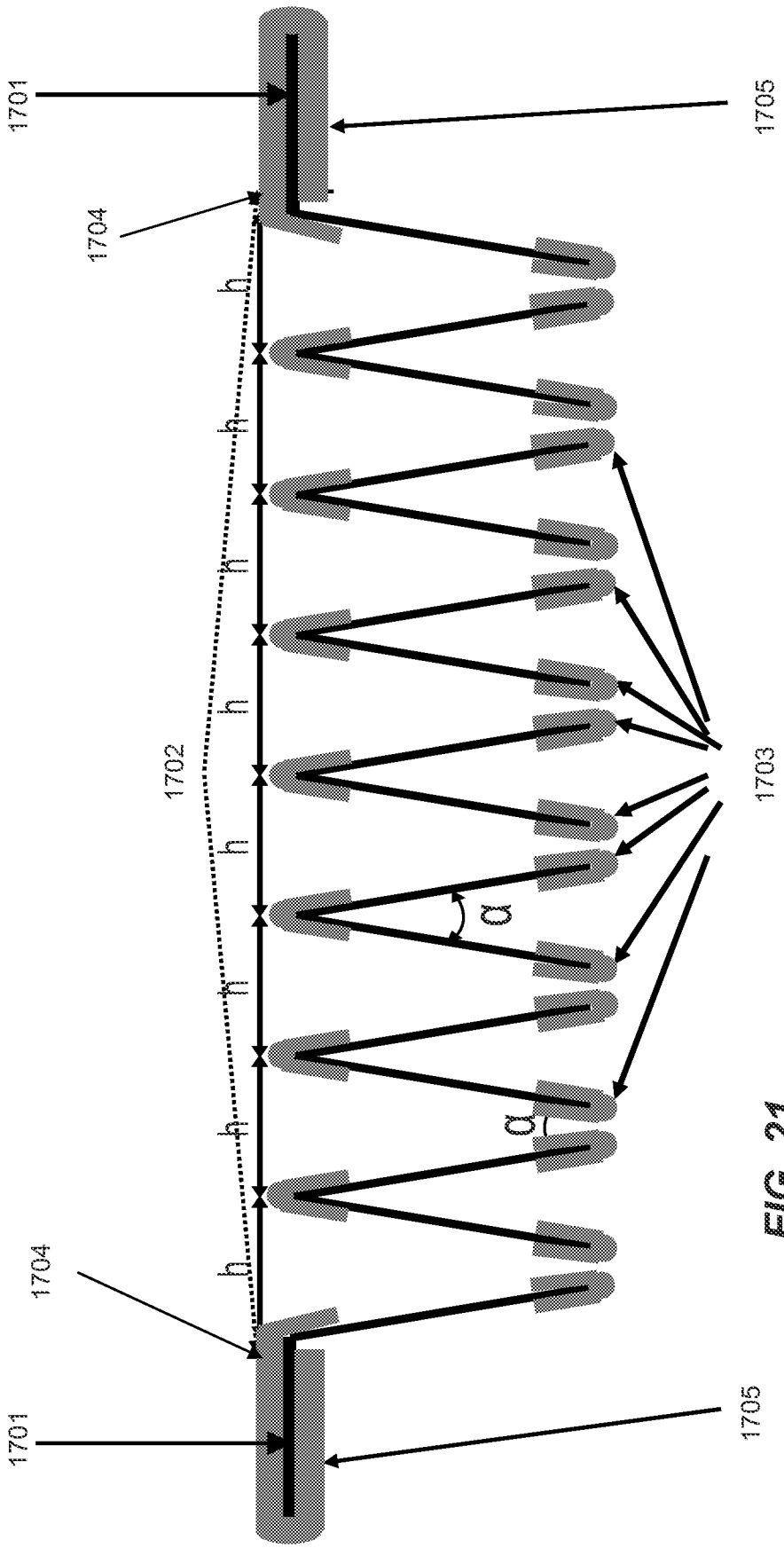


FIG. 21

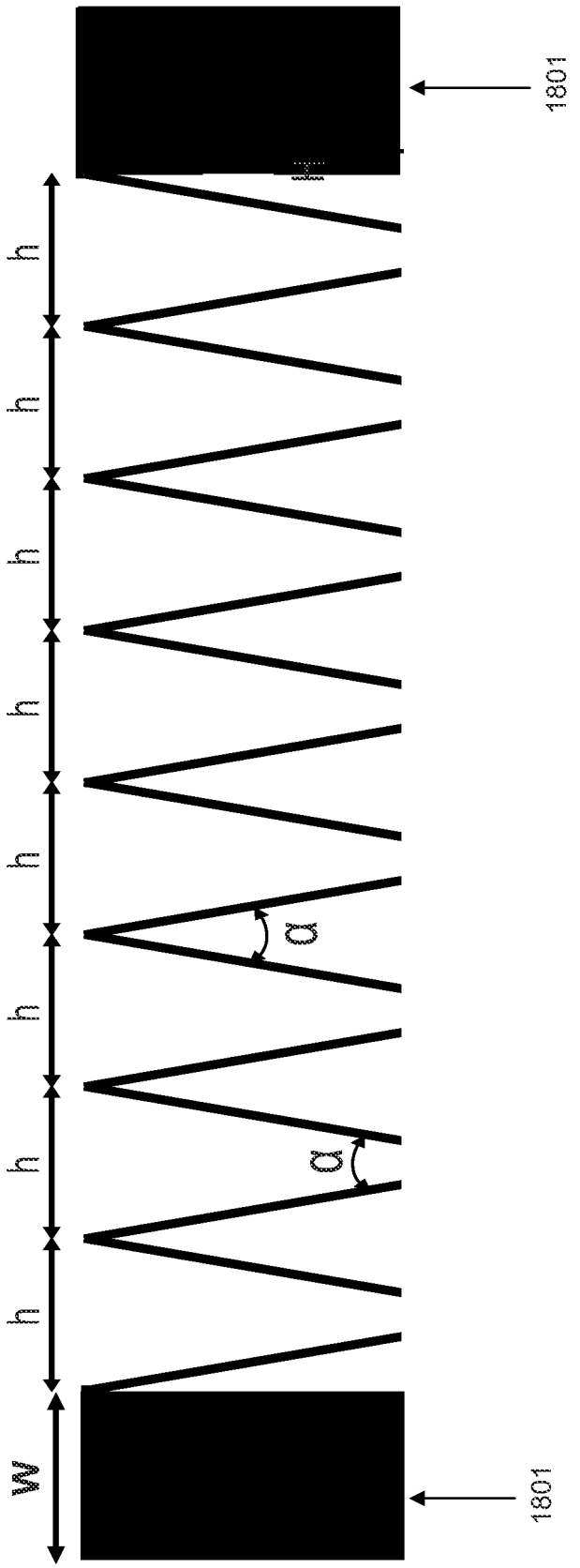


FIG. 22

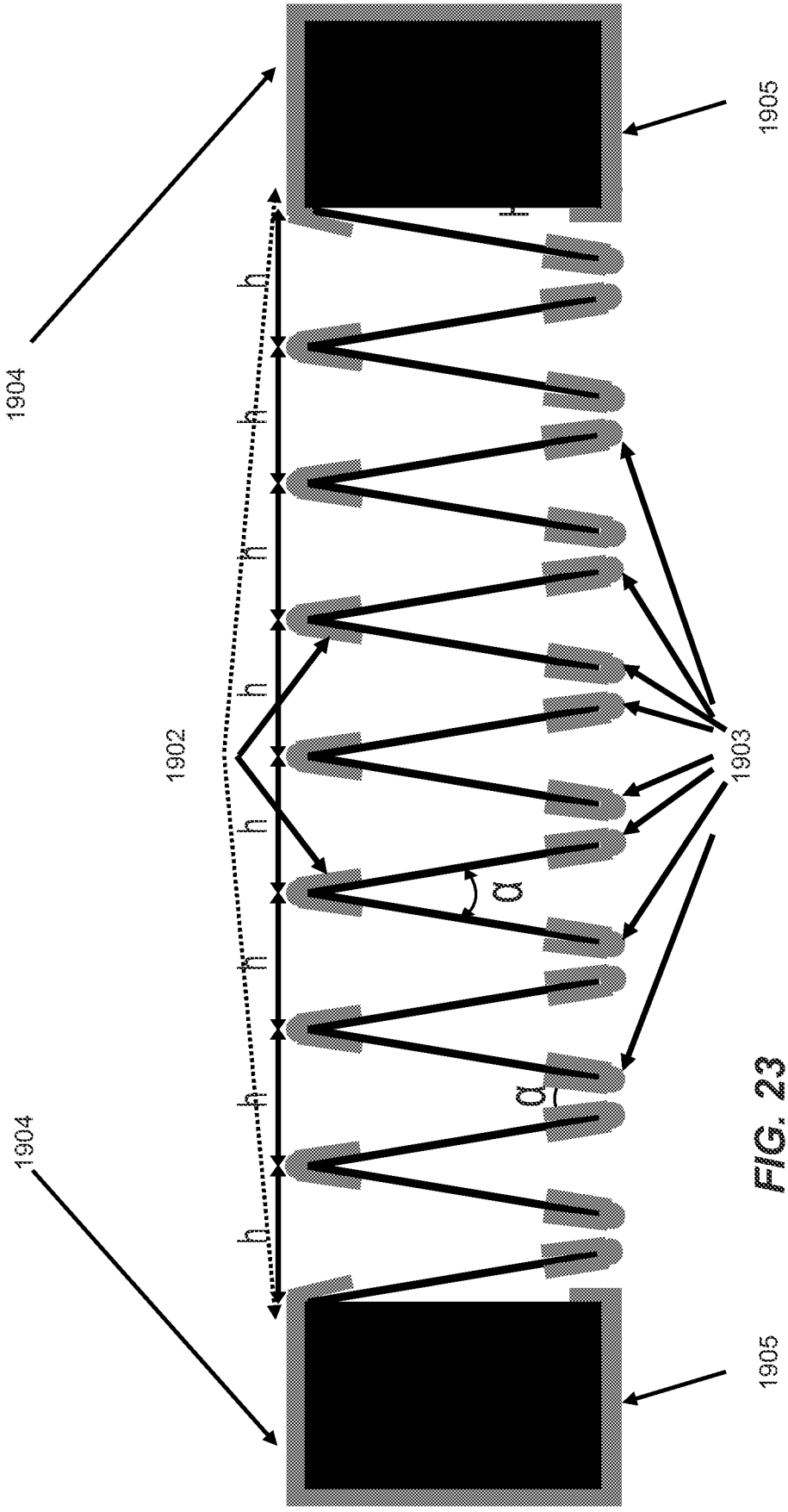


FIG. 23

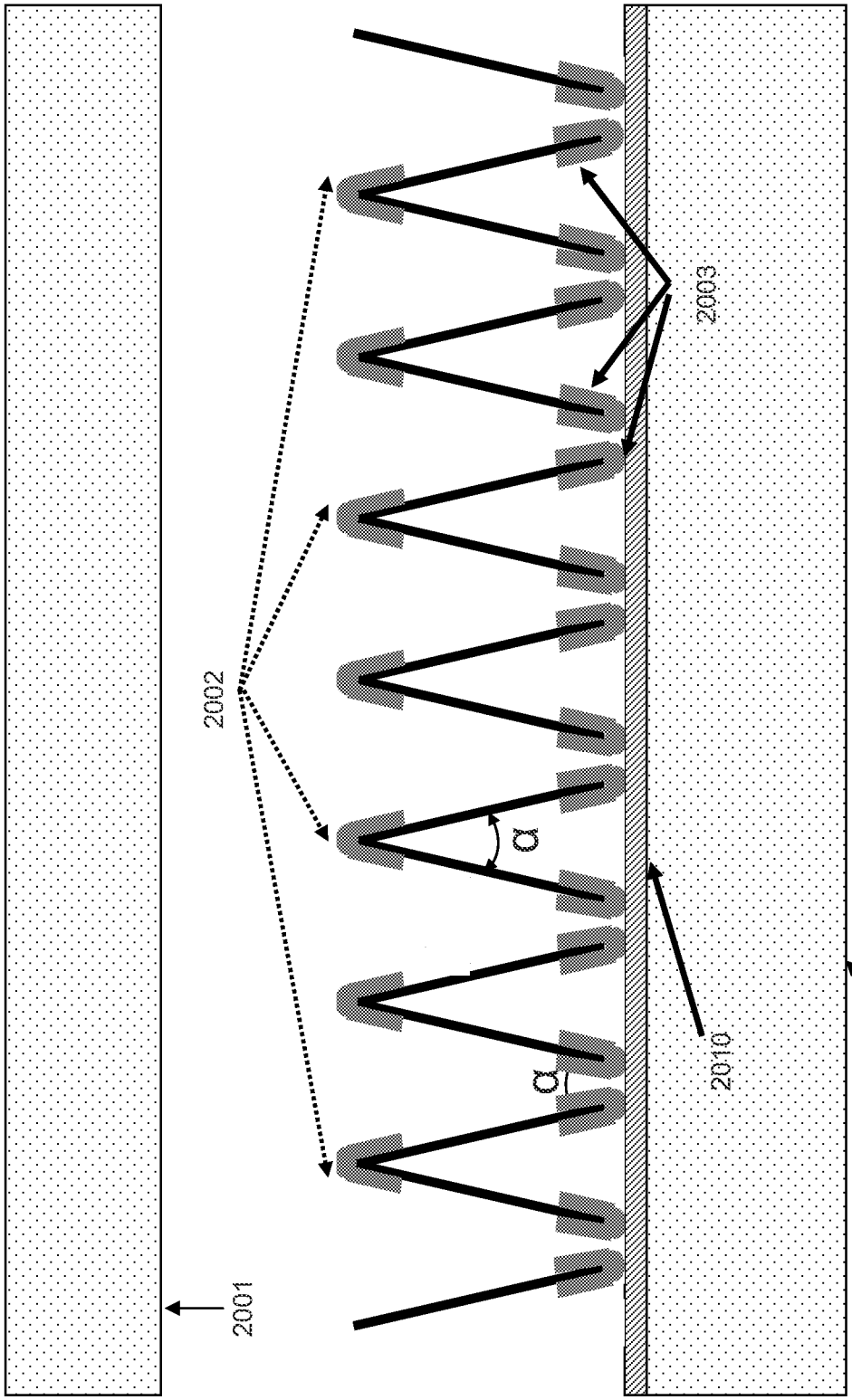


FIG. 24

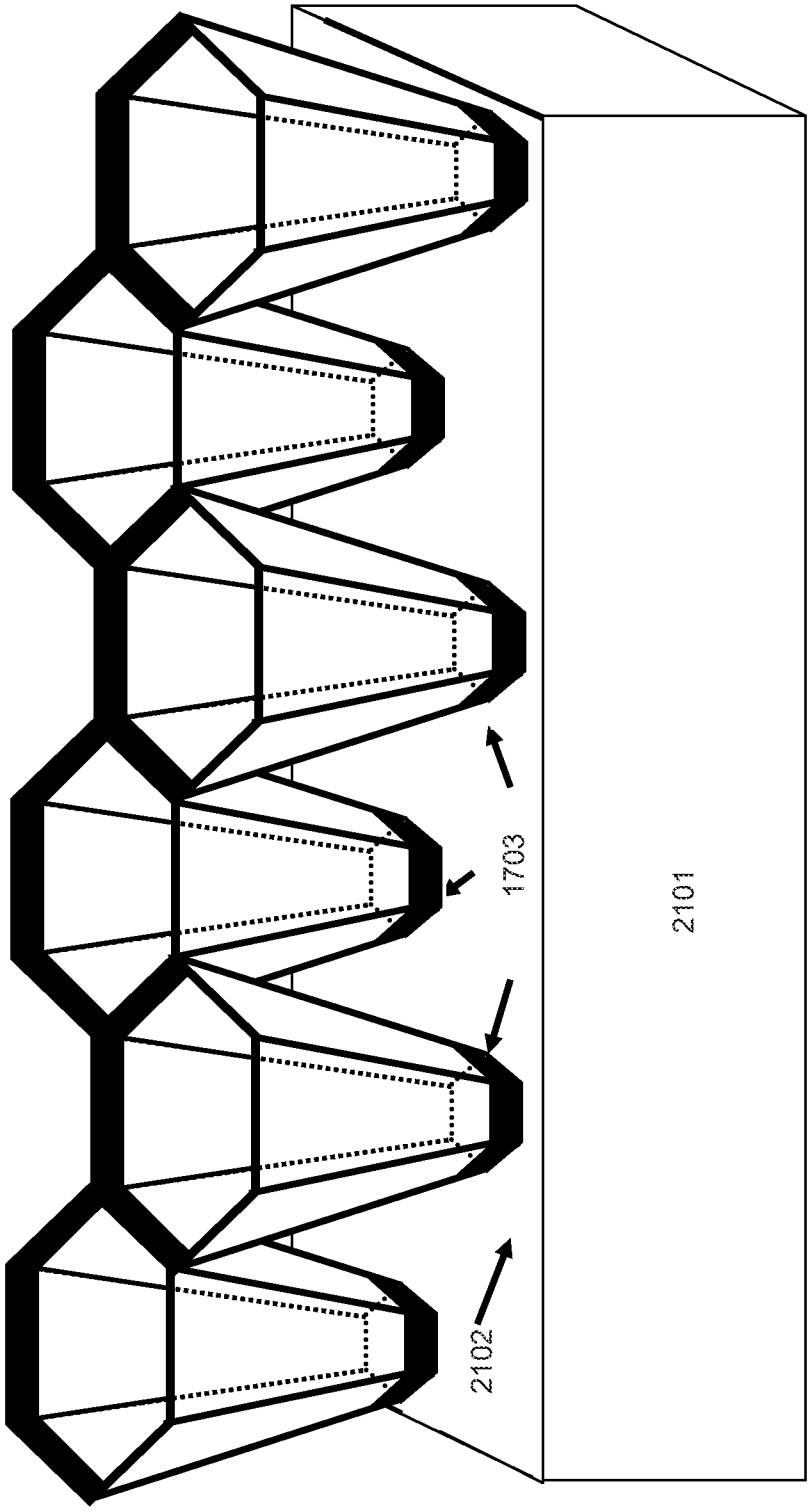


FIG. 25

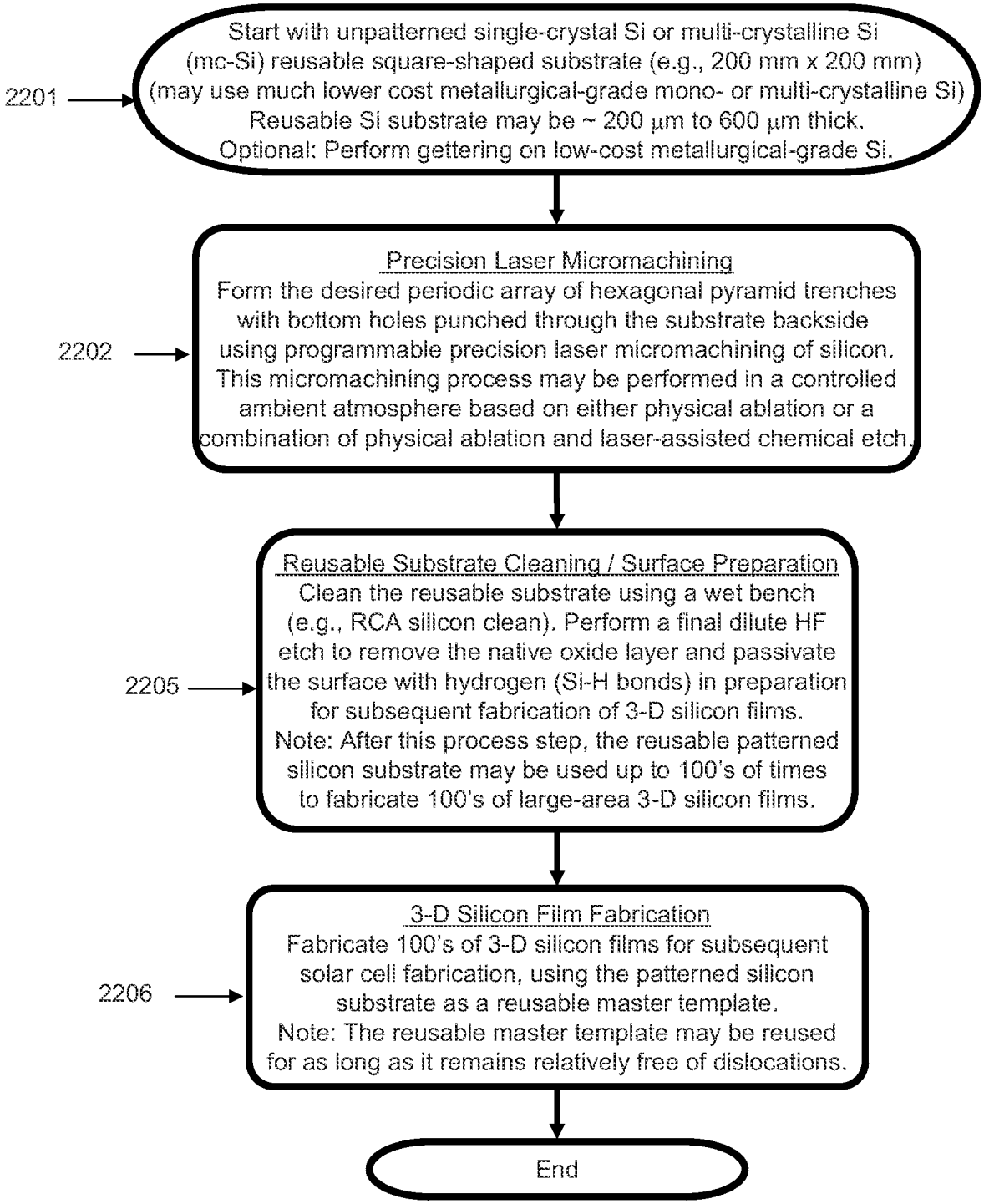

2201
Start with unpatterned single-crystal Si or multi-crystalline Si (mc-Si) reusable square-shaped substrate (e.g., 200 mm x 200 mm) (may use much lower cost metallurgical-grade mono- or multi-crystalline Si) Reusable Si substrate may be ~ 200 μm to 600 μm thick. Optional: Perform gettering on low-cost metallurgical-grade Si.
2202
Precision Laser Micromachining
Form the desired periodic array of hexagonal pyramid trenches with bottom holes punched through the substrate backside using programmable precision laser micromachining of silicon. This micromachining process may be performed in a controlled ambient atmosphere based on either physical ablation or a combination of physical ablation and laser-assisted chemical etch.
2205
Reusable Substrate Cleaning / Surface Preparation
Clean the reusable substrate using a wet bench (e.g., RCA silicon clean). Perform a final dilute HF etch to remove the native oxide layer and passivate the surface with hydrogen (Si-H bonds) in preparation for subsequent fabrication of 3-D silicon films. Note: After this process step, the reusable patterned silicon substrate may be used up to 100's of times to fabricate 100's of large-area 3-D silicon films.
2206
3-D Silicon Film Fabrication
Fabricate 100's of 3-D silicon films for subsequent solar cell fabrication, using the patterned silicon substrate as a reusable master template. Note: The reusable master template may be reused for as long as it remains relatively free of dislocations.
End

FIG. 26

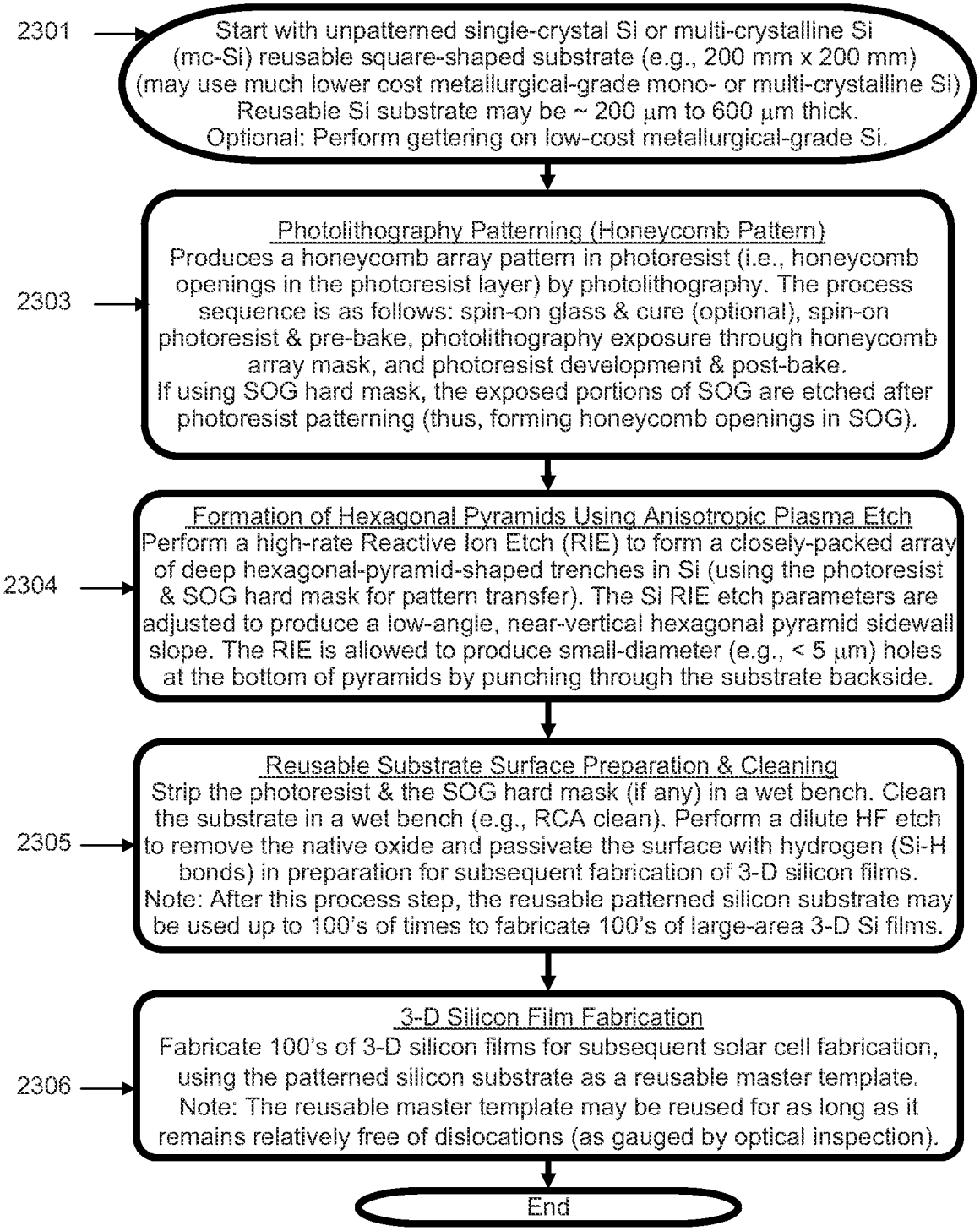

2301
Start with unpatterned single-crystal Si or multi-crystalline Si (mc-Si) reusable square-shaped substrate (e.g., 200 mm x 200 mm) (may use much lower cost metallurgical-grade mono- or multi-crystalline Si) Reusable Si substrate may be ~ 200 μm to 600 μm thick. Optional: Perform gettering on low-cost metallurgical-grade Si.
2303
Photolithography Patterning (Honeycomb Pattern)
Produces a honeycomb array pattern in photoresist (i.e., honeycomb openings in the photoresist layer) by photolithography. The process sequence is as follows: spin-on glass & cure (optional), spin-on photoresist & pre-bake, photolithography exposure through honeycomb array mask, and photoresist development & post-bake. If using SOG hard mask, the exposed portions of SOG are etched after photoresist patterning (thus, forming honeycomb openings in SOG).
2304
Formation of Hexagonal Pyramids Using Anisotropic Plasma Etch
Perform a high-rate Reactive Ion Etch (RIE) to form a closely-packed array of deep hexagonal-pyramid-shaped trenches in Si (using the photoresist & SOG hard mask for pattern transfer). The Si RIE etch parameters are adjusted to produce a low-angle, near-vertical hexagonal pyramid sidewall slope. The RIE is allowed to produce small-diameter (e.g., < 5 μm) holes at the bottom of pyramids by punching through the substrate backside.
2305
Reusable Substrate Surface Preparation & Cleaning
Strip the photoresist & the SOG hard mask (if any) in a wet bench. Clean the substrate in a wet bench (e.g., RCA clean). Perform a dilute HF etch to remove the native oxide and passivate the surface with hydrogen (Si-H bonds) in preparation for subsequent fabrication of 3-D silicon films. Note: After this process step, the reusable patterned silicon substrate may be used up to 100's of times to fabricate 100's of large-area 3-D Si films.
2306
3-D Silicon Film Fabrication
Fabricate 100's of 3-D silicon films for subsequent solar cell fabrication, using the patterned silicon substrate as a reusable master template. Note: The reusable master template may be reused for as long as it remains relatively free of dislocations (as gauged by optical inspection).
End

FIG. 27

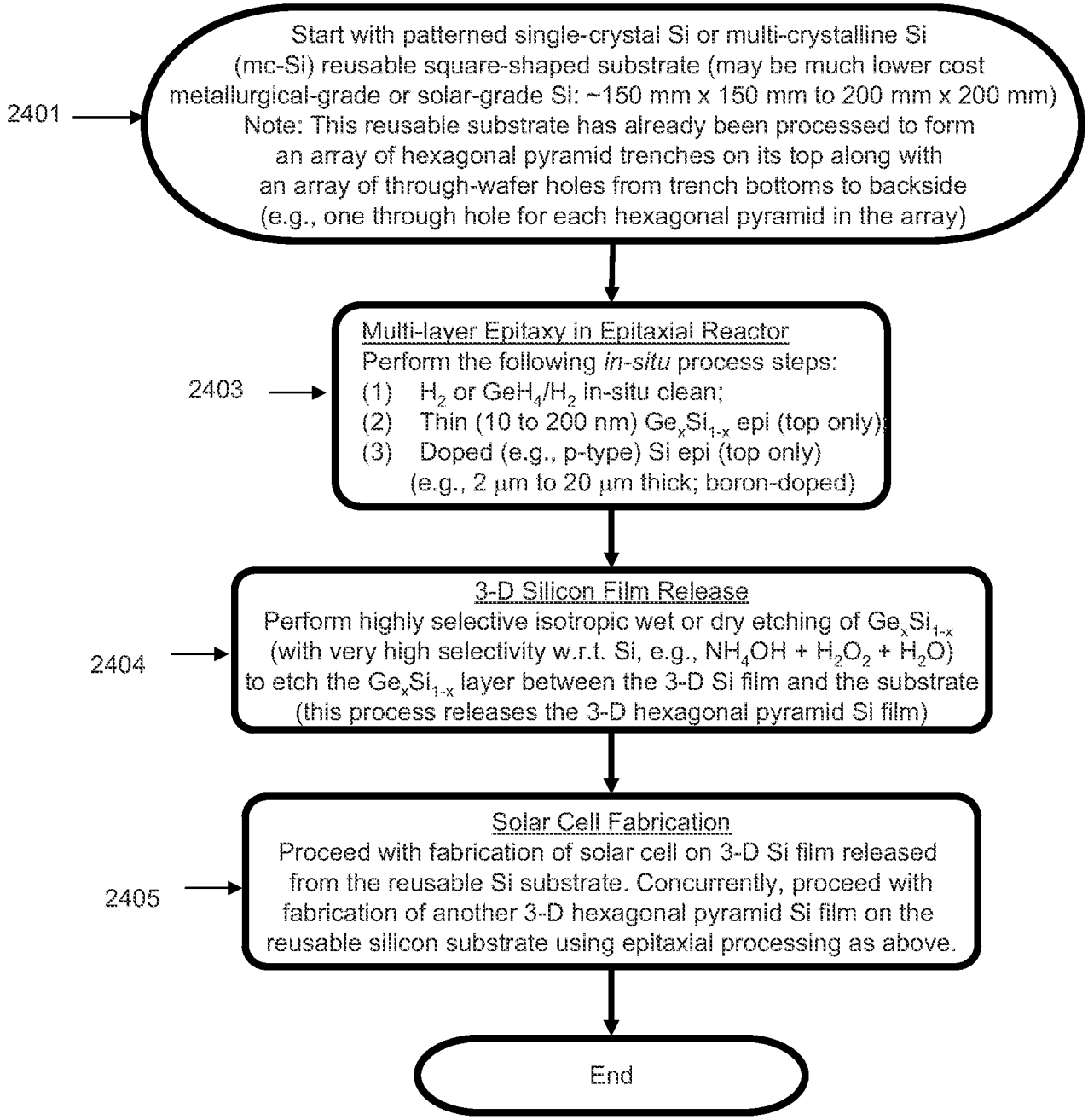

2401
Start with patterned single-crystal Si or multi-crystalline Si (mc-Si) reusable square-shaped substrate (may be much lower cost metallurgical-grade or solar-grade Si: ~150 mm x 150 mm to 200 mm x 200 mm)
Note: This reusable substrate has already been processed to form an array of hexagonal pyramid trenches on its top along with an array of through-wafer holes from trench bottoms to backside (e.g., one through hole for each hexagonal pyramid in the array)
2403
Multi-layer Epitaxy in Epitaxial Reactor
Perform the following in-situ process steps:
(1) H2 or GeH4/H2 in-situ clean;
(2) Thin (10 to 200 nm) GexSi1-x epi (top only);
(3) Doped (e.g., p-type) Si epi (top only)
(e.g., 2 μm to 20 μm thick; boron-doped)
2404
3-D Silicon Film Release
Perform highly selective isotropic wet or dry etching of GexSi1-x (with very high selectivity w.r.t. Si, e.g., NH4OH + H2O2 + H2O) to etch the GexSi1-x layer between the 3-D Si film and the substrate (this process releases the 3-D hexagonal pyramid Si film)
2405
Solar Cell Fabrication
Proceed with fabrication of solar cell on 3-D Si film released from the reusable Si substrate. Concurrently, proceed with fabrication of another 3-D hexagonal pyramid Si film on the reusable silicon substrate using epitaxial processing as above.
End

FIG. 28

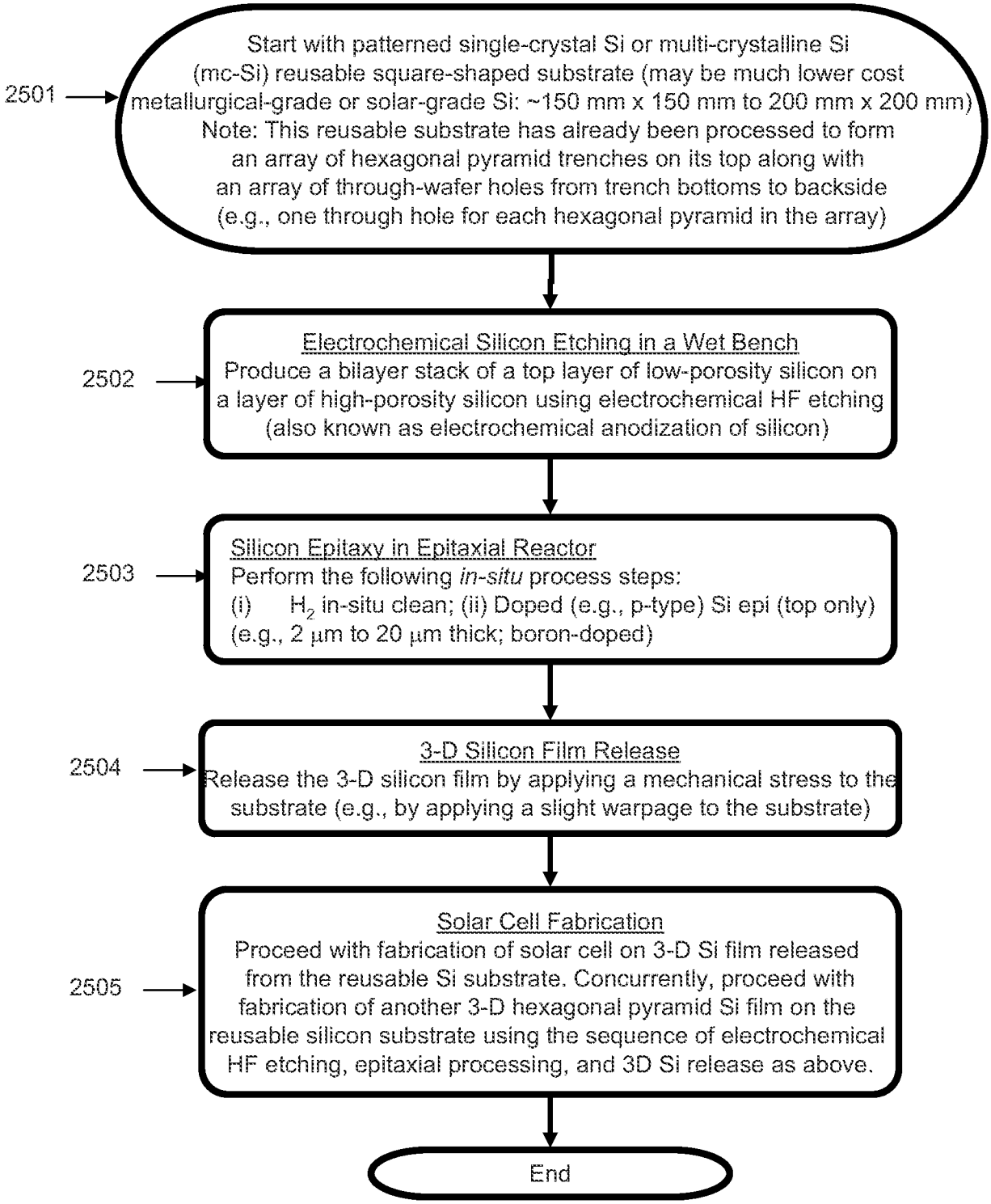

2501
Start with patterned single-crystal Si or multi-crystalline Si (mc-Si) reusable square-shaped substrate (may be much lower cost metallurgical-grade or solar-grade Si: ~150 mm x 150 mm to 200 mm x 200 mm) Note: This reusable substrate has already been processed to form an array of hexagonal pyramid trenches on its top along with an array of through-wafer holes from trench bottoms to backside (e.g., one through hole for each hexagonal pyramid in the array)
2502
Electrochemical Silicon Etching in a Wet Bench
Produce a bilayer stack of a top layer of low-porosity silicon on a layer of high-porosity silicon using electrochemical HF etching (also known as electrochemical anodization of silicon)
2503
Silicon Epitaxy in Epitaxial Reactor
Perform the following *in-situ* process steps:
(i) H_2 in-situ clean; (ii) Doped (e.g., p-type) Si epi (top only) (e.g., 2 μm to 20 μm thick; boron-doped)
2504
3-D Silicon Film Release
Release the 3-D silicon film by applying a mechanical stress to the substrate (e.g., by applying a slight warpage to the substrate)
2505
Solar Cell Fabrication
Proceed with fabrication of solar cell on 3-D Si film released from the reusable Si substrate. Concurrently, proceed with fabrication of another 3-D hexagonal pyramid Si film on the reusable silicon substrate using the sequence of electrochemical HF etching, epitaxial processing, and 3D Si release as above.
End

FIG. 29

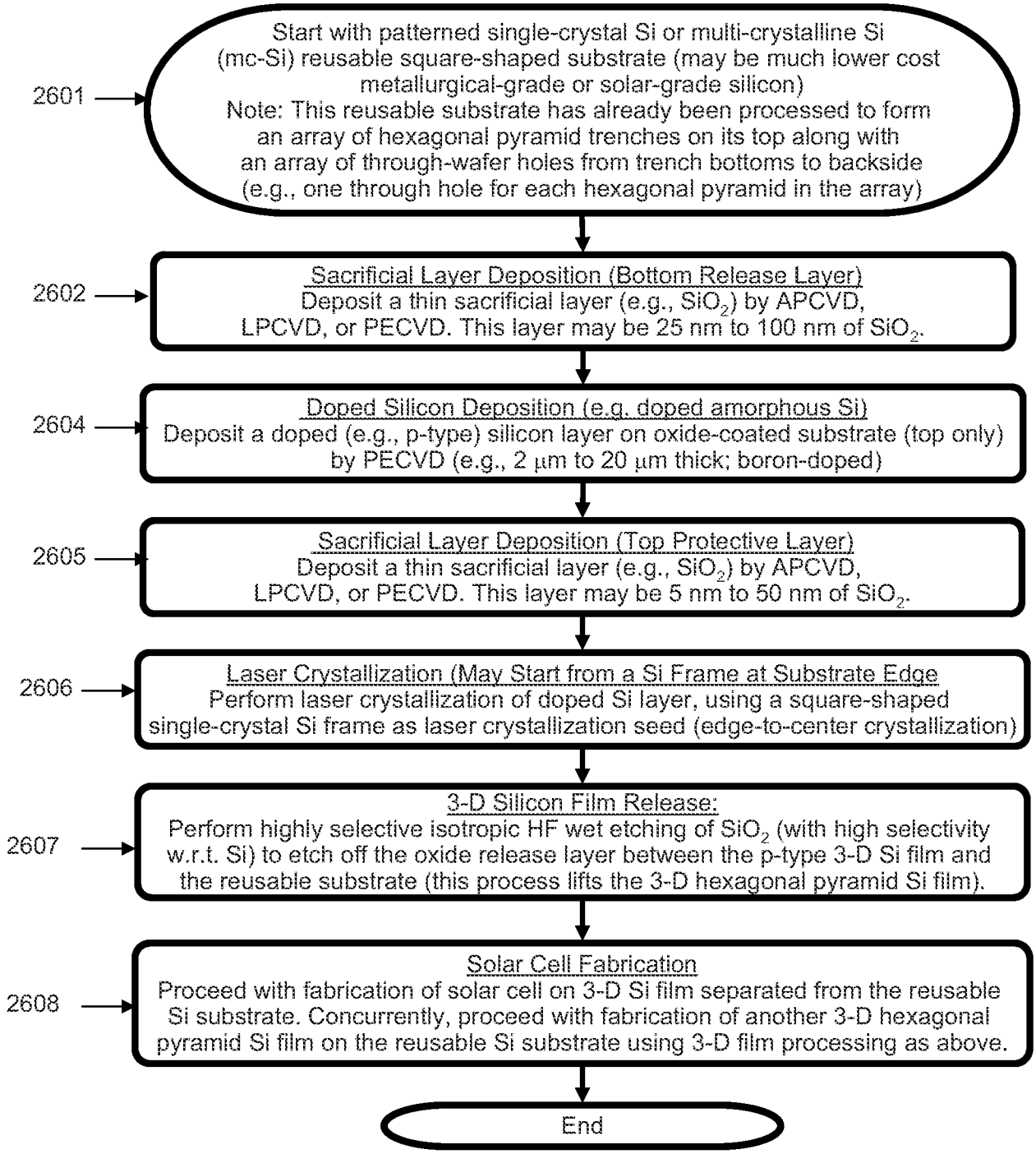

2601
Start with patterned single-crystal Si or multi-crystalline Si (mc-Si) reusable square-shaped substrate (may be much lower cost metallurgical-grade or solar-grade silicon)
Note: This reusable substrate has already been processed to form an array of hexagonal pyramid trenches on its top along with an array of through-wafer holes from trench bottoms to backside (e.g., one through hole for each hexagonal pyramid in the array)
2602
Sacrificial Layer Deposition (Bottom Release Layer)
Deposit a thin sacrificial layer (e.g., SiO2) by APCVD, LPCVD, or PECVD. This layer may be 25 nm to 100 nm of SiO2.
2604
Doped Silicon Deposition (e.g. doped amorphous Si)
Deposit a doped (e.g., p-type) silicon layer on oxide-coated substrate (top only) by PECVD (e.g., 2 μm to 20 μm thick; boron-doped)
2605
Sacrificial Layer Deposition (Top Protective Layer)
Deposit a thin sacrificial layer (e.g., SiO2) by APCVD, LPCVD, or PECVD. This layer may be 5 nm to 50 nm of SiO2.
2606
Laser Crystallization (May Start from a Si Frame at Substrate Edge
Perform laser crystallization of doped Si layer, using a square-shaped single-crystal Si frame as laser crystallization seed (edge-to-center crystallization)
2607
3-D Silicon Film Release:
Perform highly selective isotropic HF wet etching of SiO2 (with high selectivity w.r.t. Si) to etch off the oxide release layer between the p-type 3-D Si film and the reusable substrate (this process lifts the 3-D hexagonal pyramid Si film).
2608
Solar Cell Fabrication
Proceed with fabrication of solar cell on 3-D Si film separated from the reusable Si substrate. Concurrently, proceed with fabrication of another 3-D hexagonal pyramid Si film on the reusable Si substrate using 3-D film processing as above.
End

FIG. 30

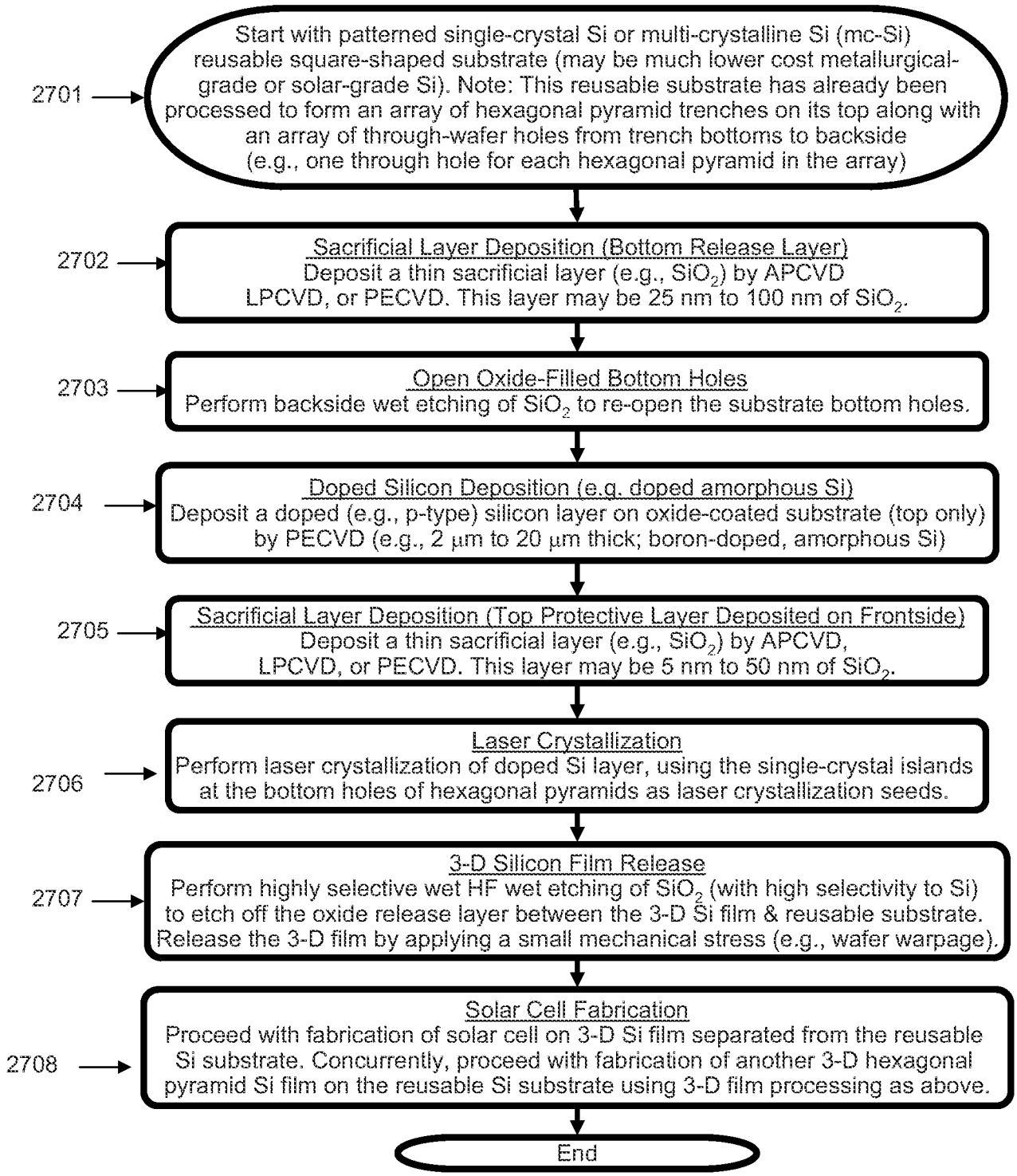

2701
Start with patterned single-crystal Si or multi-crystalline Si (mc-Si) reusable square-shaped substrate (may be much lower cost metallurgical-grade or solar-grade Si). Note: This reusable substrate has already been processed to form an array of hexagonal pyramid trenches on its top along with an array of through-wafer holes from trench bottoms to backside (e.g., one through hole for each hexagonal pyramid in the array)
2702
Sacrificial Layer Deposition (Bottom Release Layer)
Deposit a thin sacrificial layer (e.g., SiO2) by APCVD LPCVD, or PECVD. This layer may be 25 nm to 100 nm of SiO2.
2703
Open Oxide-Filled Bottom Holes
Perform backside wet etching of SiO2 to re-open the substrate bottom holes.
2704
Doped Silicon Deposition (e.g. doped amorphous Si)
Deposit a doped (e.g., p-type) silicon layer on oxide-coated substrate (top only) by PECVD (e.g., 2 μm to 20 μm thick; boron-doped, amorphous Si)
2705
Sacrificial Layer Deposition (Top Protective Layer Deposited on Frontside)
Deposit a thin sacrificial layer (e.g., SiO2) by APCVD, LPCVD, or PECVD. This layer may be 5 nm to 50 nm of SiO2.
2706
Laser Crystallization
Perform laser crystallization of doped Si layer, using the single-crystal islands at the bottom holes of hexagonal pyramids as laser crystallization seeds.
2707
3-D Silicon Film Release
Perform highly selective wet HF wet etching of SiO2 (with high selectivity to Si) to etch off the oxide release layer between the 3-D Si film & reusable substrate. Release the 3-D film by applying a small mechanical stress (e.g., wafer warpage).
2708
Solar Cell Fabrication
Proceed with fabrication of solar cell on 3-D Si film separated from the reusable Si substrate. Concurrently, proceed with fabrication of another 3-D hexagonal pyramid Si film on the reusable Si substrate using 3-D film processing as above.
End

FIG. 31

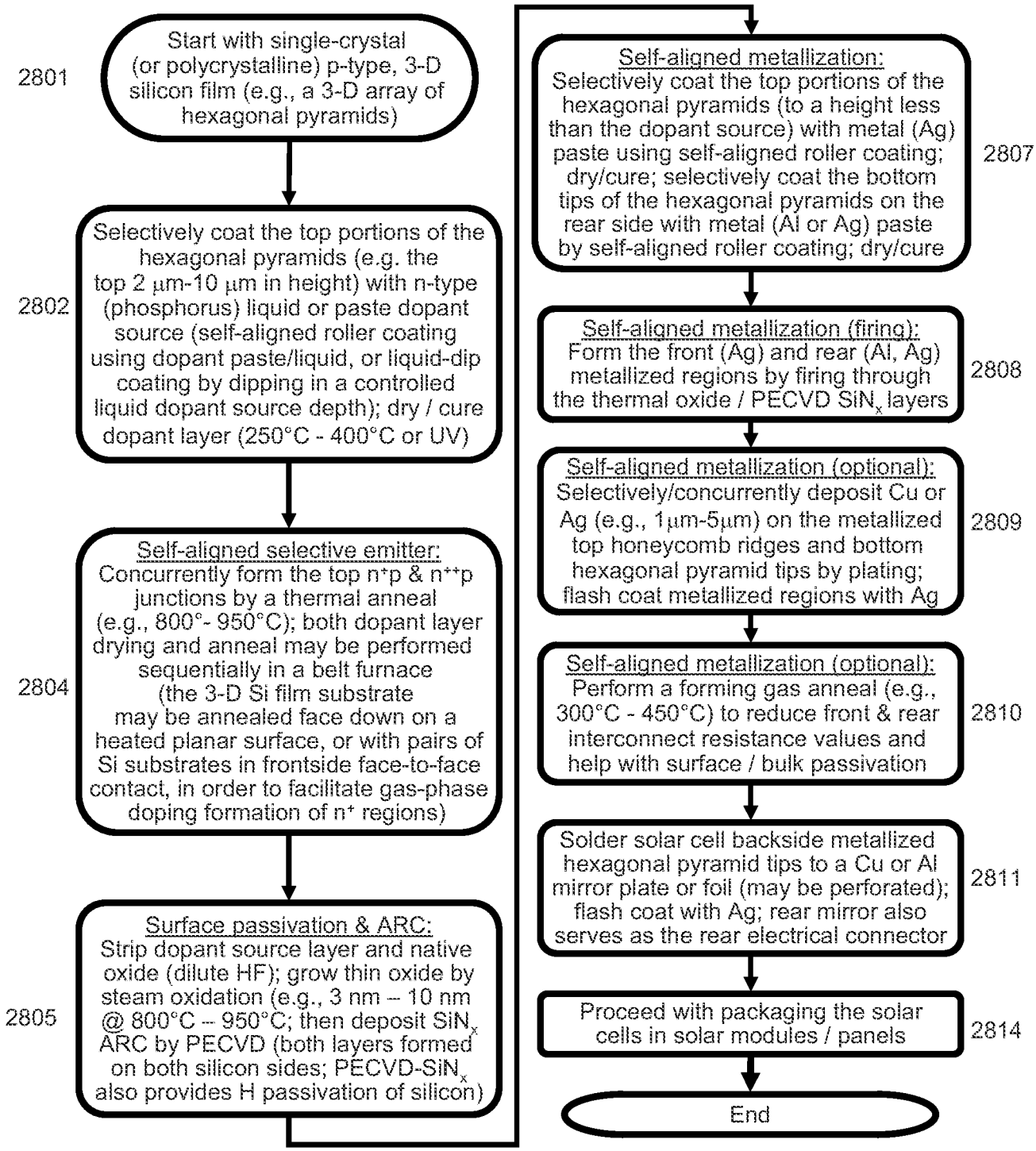

2801
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
2802
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
2804
Self-aligned selective emitter:
Concurrently form the top n+p & n++p junctions by a thermal anneal (e.g., 800°- 950°C); both dopant layer drying and anneal may be performed sequentially in a belt furnace (the 3-D Si film substrate may be annealed face down on a heated planar surface, or with pairs of Si substrates in frontside face-to-face contact, in order to facilitate gas-phase doping formation of n+ regions)
2805
Surface passivation & ARC:
Strip dopant source layer and native oxide (dilute HF); grow thin oxide by steam oxidation (e.g., 3 nm – 10 nm @ 800°C – 950°C; then deposit SiNx ARC by PECVD (both layers formed on both silicon sides; PECVD-SiNx also provides H passivation of silicon)
2807
Self-aligned metallization:
Selectively coat the top portions of the hexagonal pyramids (to a height less than the dopant source) with metal (Ag) paste using self-aligned roller coating; dry/cure; selectively coat the bottom tips of the hexagonal pyramids on the rear side with metal (Al or Ag) paste by self-aligned roller coating; dry/cure
2808
Self-aligned metallization (firing):
Form the front (Ag) and rear (Al, Ag) metallized regions by firing through the thermal oxide / PECVD SiNx layers
2809
Self-aligned metallization (optional):
Selectively/concurrently deposit Cu or Ag (e.g., 1μm-5μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating; flash coat metallized regions with Ag
2810
Self-aligned metallization (optional):
Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
2811
Solder solar cell backside metallized hexagonal pyramid tips to a Cu or Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
2814
Proceed with packaging the solar cells in solar modules / panels
End

FIG. 32

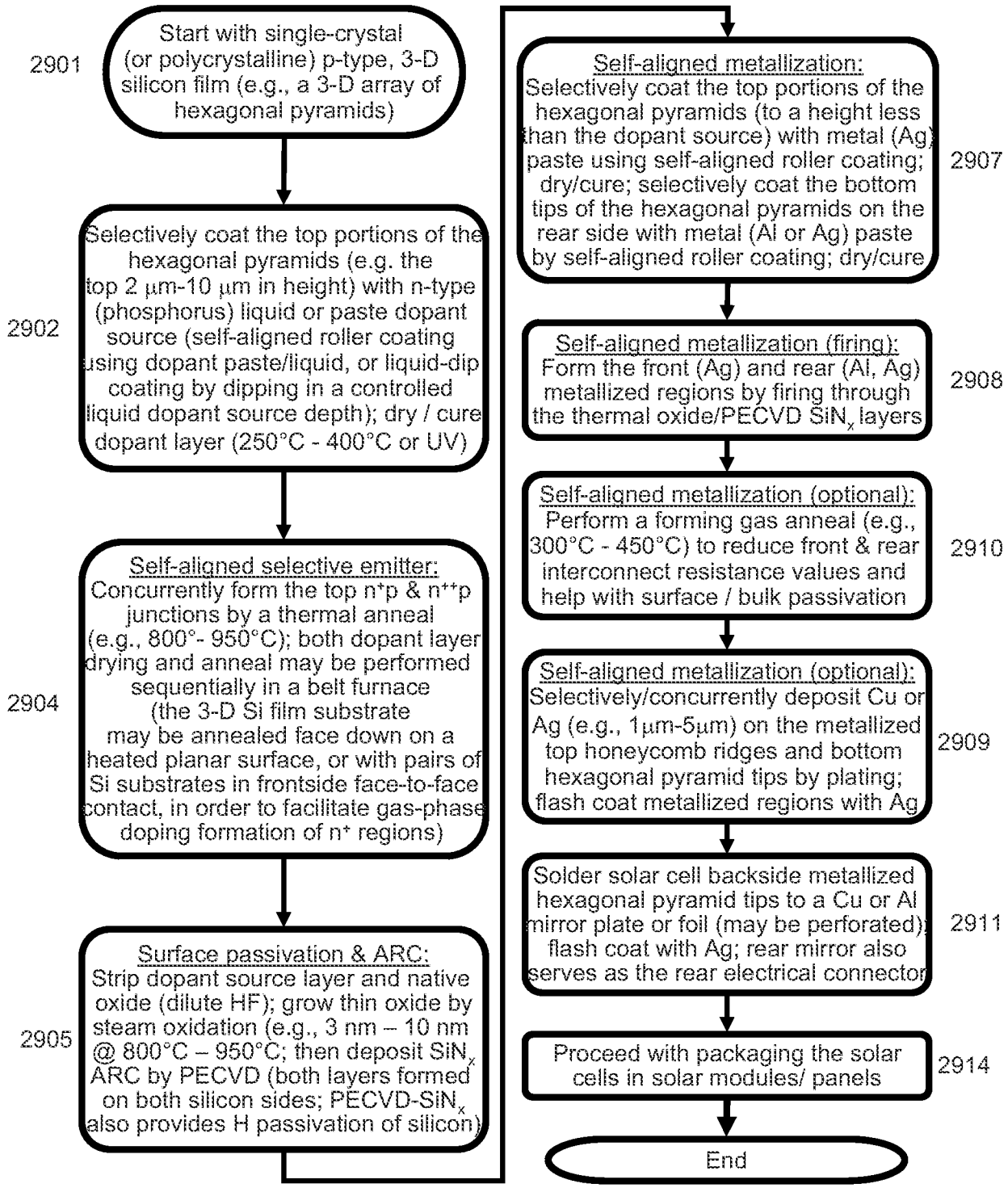

2901
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
2902
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
2904
Self-aligned selective emitter: Concurrently form the top n+p & n++p junctions by a thermal anneal (e.g., 800°- 950°C); both dopant layer drying and anneal may be performed sequentially in a belt furnace (the 3-D Si film substrate may be annealed face down on a heated planar surface, or with pairs of Si substrates in frontside face-to-face contact, in order to facilitate gas-phase doping formation of n+ regions)
2905
Surface passivation & ARC: Strip dopant source layer and native oxide (dilute HF); grow thin oxide by steam oxidation (e.g., 3 nm – 10 nm @ 800°C – 950°C; then deposit SiNx ARC by PECVD (both layers formed on both silicon sides; PECVD-SiNx also provides H passivation of silicon)
2907
Self-aligned metallization: Selectively coat the top portions of the hexagonal pyramids (to a height less than the dopant source) with metal (Ag) paste using self-aligned roller coating; dry/cure; selectively coat the bottom tips of the hexagonal pyramids on the rear side with metal (Al or Ag) paste by self-aligned roller coating; dry/cure
2908
Self-aligned metallization (firing): Form the front (Ag) and rear (Al, Ag) metallized regions by firing through the thermal oxide/PECVD SiNx layers
2910
Self-aligned metallization (optional): Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
2909
Self-aligned metallization (optional): Selectively/concurrently deposit Cu or Ag (e.g., 1μm-5μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating; flash coat metallized regions with Ag
2911
Solder solar cell backside metallized hexagonal pyramid tips to a Cu or Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
2914
Proceed with packaging the solar cells in solar modules/ panels
End

FIG. 33

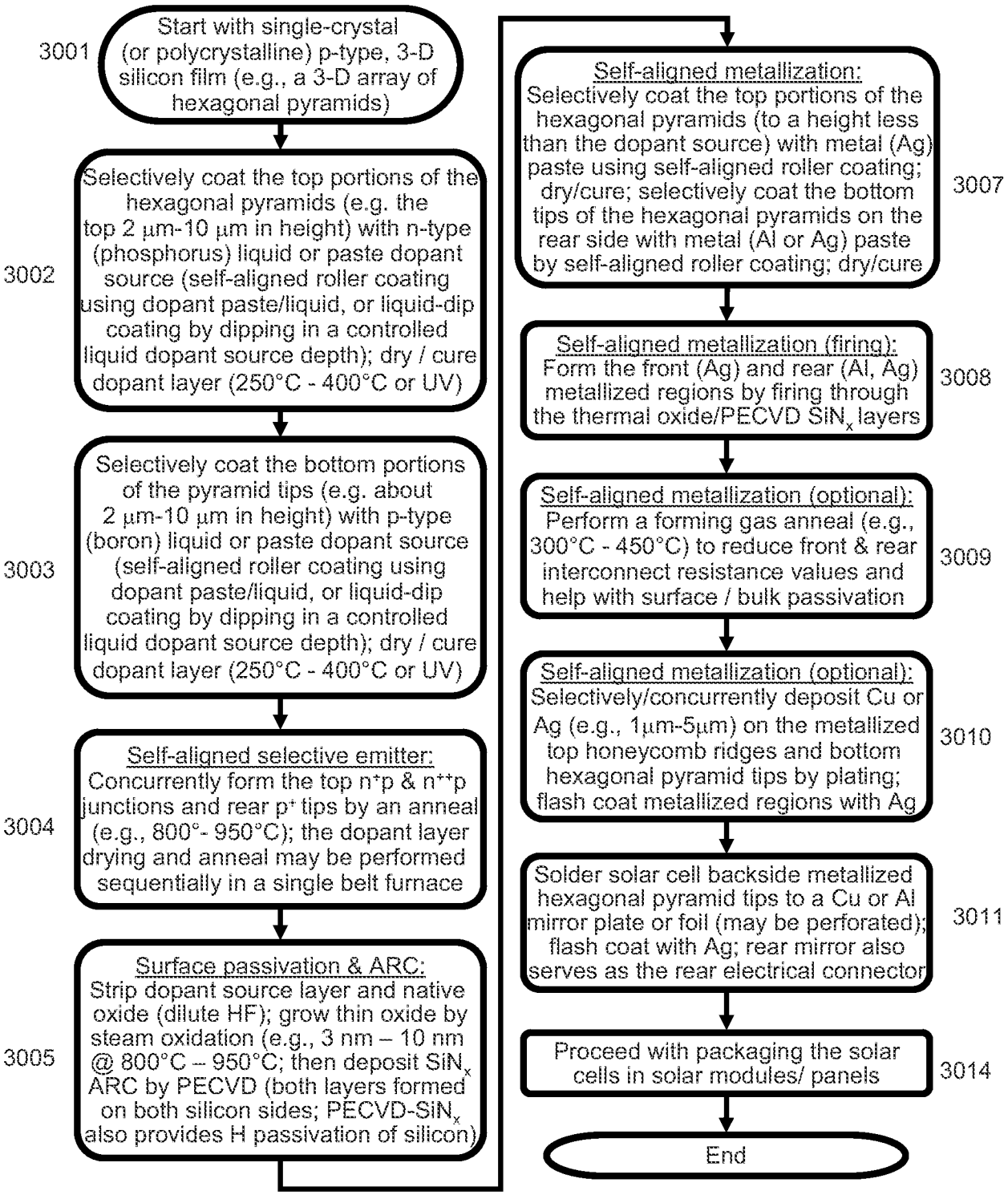

3001
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
3002
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3003
Selectively coat the bottom portions of the pyramid tips (e.g. about 2 μm-10 μm in height) with p-type (boron) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3004
Self-aligned selective emitter: Concurrently form the top n+p & n++p junctions and rear p+ tips by an anneal (e.g., 800°- 950°C); the dopant layer drying and anneal may be performed sequentially in a single belt furnace
3005
Surface passivation & ARC: Strip dopant source layer and native oxide (dilute HF); grow thin oxide by steam oxidation (e.g., 3 nm – 10 nm @ 800°C – 950°C; then deposit SiNx ARC by PECVD (both layers formed on both silicon sides; PECVD-SiNx also provides H passivation of silicon)
3007
Self-aligned metallization: Selectively coat the top portions of the hexagonal pyramids (to a height less than the dopant source) with metal (Ag) paste using self-aligned roller coating; dry/cure; selectively coat the bottom tips of the hexagonal pyramids on the rear side with metal (Al or Ag) paste by self-aligned roller coating; dry/cure
3008
Self-aligned metallization (firing): Form the front (Ag) and rear (Al, Ag) metallized regions by firing through the thermal oxide/PECVD SiNx layers
3009
Self-aligned metallization (optional): Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
3010
Self-aligned metallization (optional): Selectively/concurrently deposit Cu or Ag (e.g., 1μm-5μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating; flash coat metallized regions with Ag
3011
Solder solar cell backside metallized hexagonal pyramid tips to a Cu or Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
3014
Proceed with packaging the solar cells in solar modules/ panels
End

FIG. 34

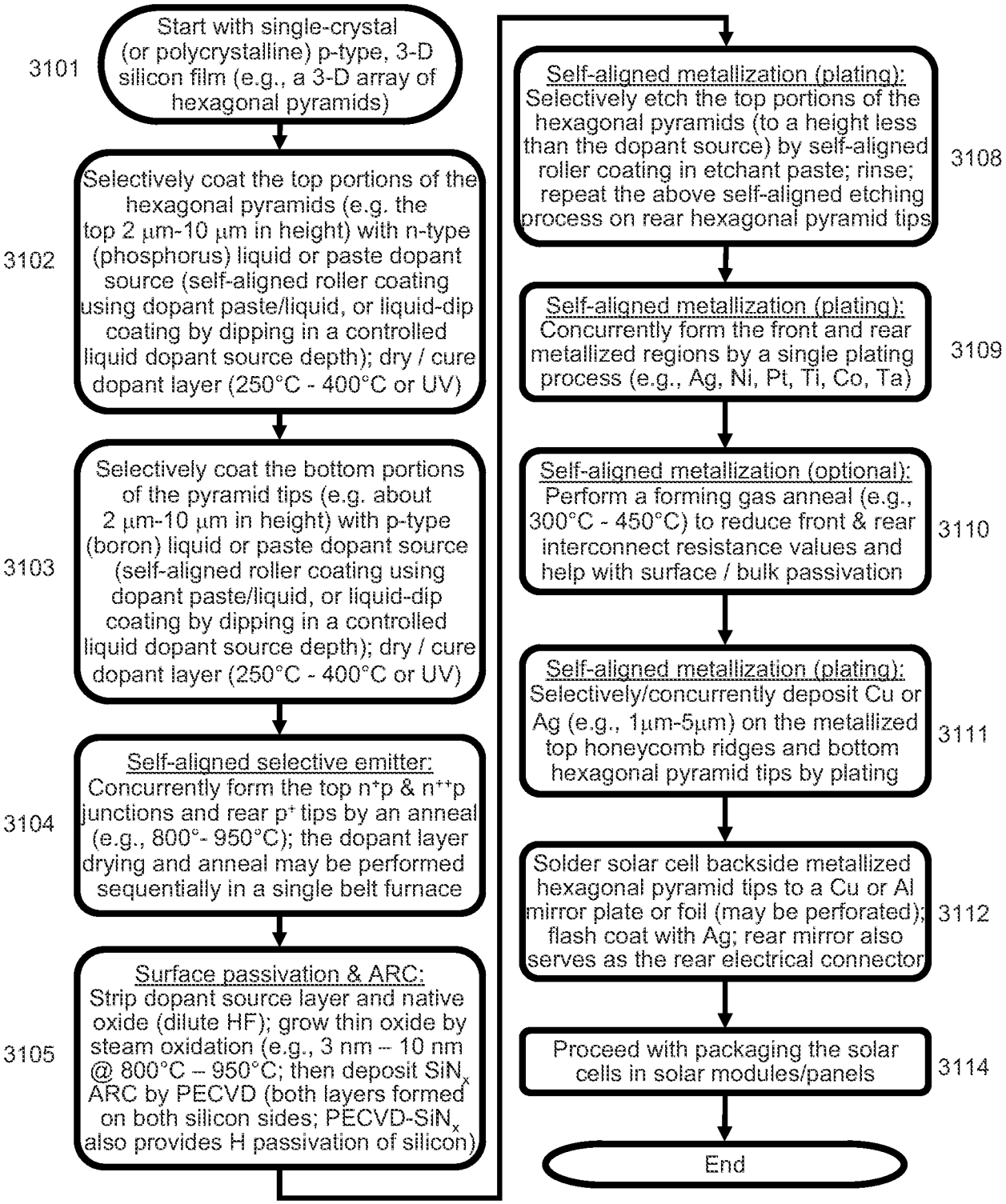

3101
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
3102
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3103
Selectively coat the bottom portions of the pyramid tips (e.g. about 2 μm-10 μm in height) with p-type (boron) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3104
Self-aligned selective emitter: Concurrently form the top n+p & n++p junctions and rear p+ tips by an anneal (e.g., 800°- 950°C); the dopant layer drying and anneal may be performed sequentially in a single belt furnace
3105
Surface passivation & ARC: Strip dopant source layer and native oxide (dilute HF); grow thin oxide by steam oxidation (e.g., 3 nm – 10 nm @ 800°C – 950°C; then deposit SiNx ARC by PECVD (both layers formed on both silicon sides; PECVD-SiNx also provides H passivation of silicon)
3108
Self-aligned metallization (plating): Selectively etch the top portions of the hexagonal pyramids (to a height less than the dopant source) by self-aligned roller coating in etchant paste; rinse; repeat the above self-aligned etching process on rear hexagonal pyramid tips
3109
Self-aligned metallization (plating): Concurrently form the front and rear metallized regions by a single plating process (e.g., Ag, Ni, Pt, Ti, Co, Ta)
3110
Self-aligned metallization (optional): Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
3111
Self-aligned metallization (plating): Selectively/concurrently deposit Cu or Ag (e.g., 1μm-5μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating
3112
Solder solar cell backside metallized hexagonal pyramid tips to a Cu or Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
3114
Proceed with packaging the solar cells in solar modules/panels
End

FIG. 35

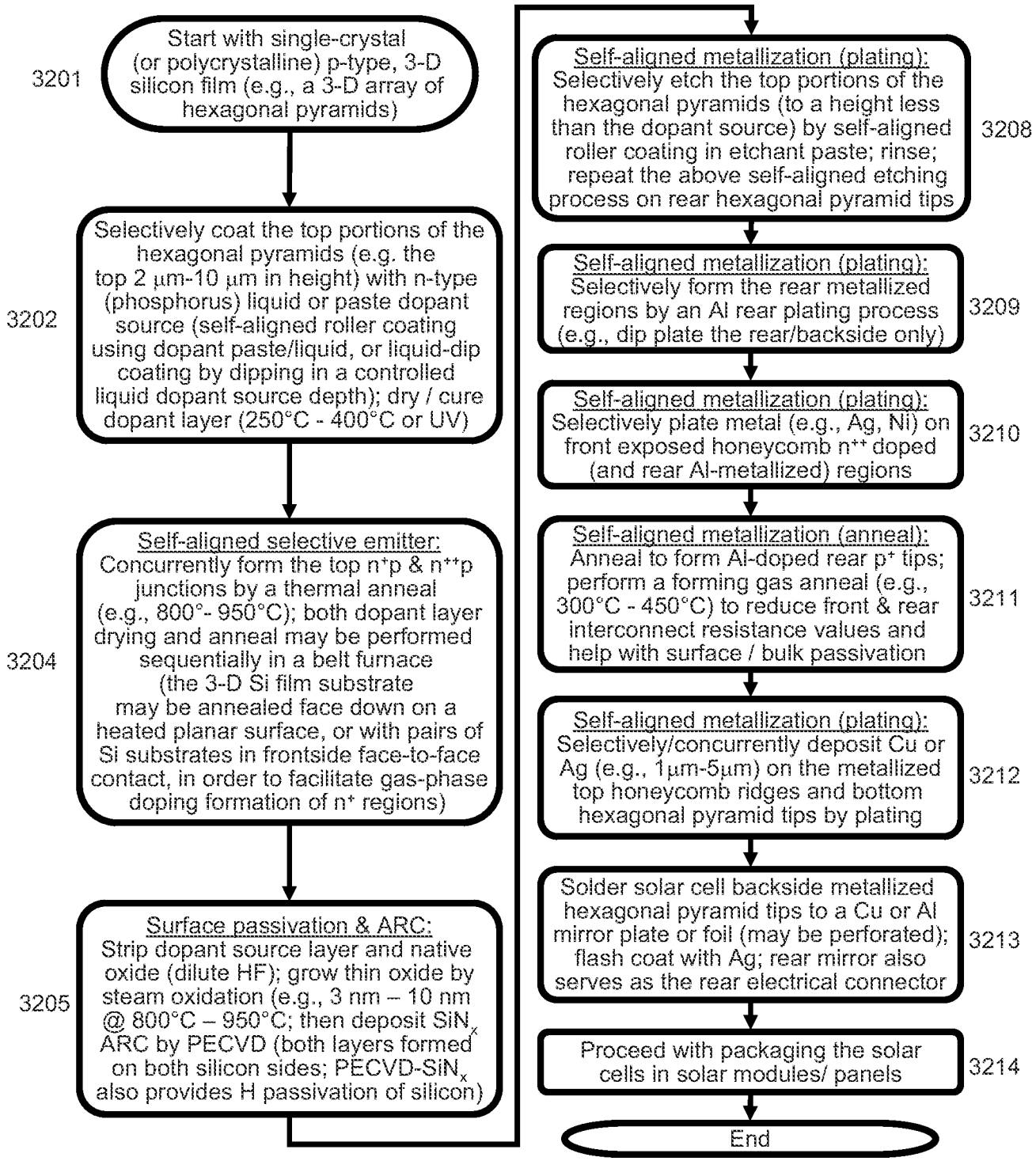

3201
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
3202
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3204
Self-aligned selective emitter:
Concurrently form the top n+p & n++p junctions by a thermal anneal (e.g., 800°- 950°C); both dopant layer drying and anneal may be performed sequentially in a belt furnace (the 3-D Si film substrate may be annealed face down on a heated planar surface, or with pairs of Si substrates in frontside face-to-face contact, in order to facilitate gas-phase doping formation of n+ regions)
3205
Surface passivation & ARC:
Strip dopant source layer and native oxide (dilute HF); grow thin oxide by steam oxidation (e.g., 3 nm – 10 nm @ 800°C – 950°C; then deposit SiNx ARC by PECVD (both layers formed on both silicon sides; PECVD-SiNx also provides H passivation of silicon)
3208
Self-aligned metallization (plating):
Selectively etch the top portions of the hexagonal pyramids (to a height less than the dopant source) by self-aligned roller coating in etchant paste; rinse; repeat the above self-aligned etching process on rear hexagonal pyramid tips
3209
Self-aligned metallization (plating):
Selectively form the rear metallized regions by an Al rear plating process (e.g., dip plate the rear/backside only)
3210
Self-aligned metallization (plating):
Selectively plate metal (e.g., Ag, Ni) on front exposed honeycomb n++ doped (and rear Al-metallized) regions
3211
Self-aligned metallization (anneal):
Anneal to form Al-doped rear p+ tips; perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
3212
Self-aligned metallization (plating):
Selectively/concurrently deposit Cu or Ag (e.g., 1μm-5μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating
3213
Solder solar cell backside metallized hexagonal pyramid tips to a Cu or Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
3214
Proceed with packaging the solar cells in solar modules/ panels
End

FIG. 36

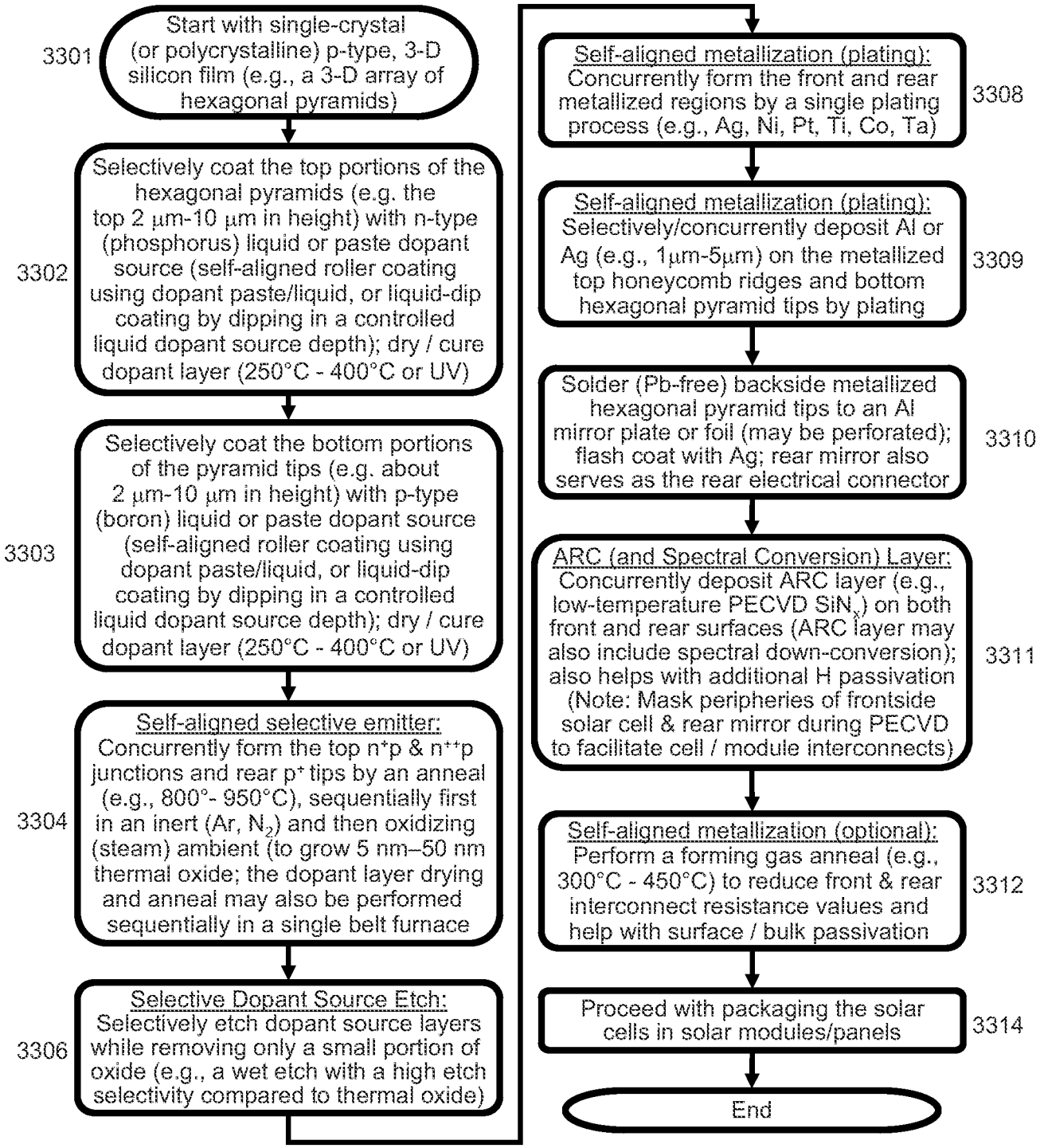

3301
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
3302
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3303
Selectively coat the bottom portions of the pyramid tips (e.g. about 2 μm-10 μm in height) with p-type (boron) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3304
Self-aligned selective emitter: Concurrently form the top n+p & n++p junctions and rear p+ tips by an anneal (e.g., 800°- 950°C), sequentially first in an inert (Ar, N2) and then oxidizing (steam) ambient (to grow 5 nm–50 nm thermal oxide; the dopant layer drying and anneal may also be performed sequentially in a single belt furnace
3306
Selective Dopant Source Etch: Selectively etch dopant source layers while removing only a small portion of oxide (e.g., a wet etch with a high etch selectivity compared to thermal oxide)
3308
Self-aligned metallization (plating): Concurrently form the front and rear metallized regions by a single plating process (e.g., Ag, Ni, Pt, Ti, Co, Ta)
3309
Self-aligned metallization (plating): Selectively/concurrently deposit Al or Ag (e.g., 1μm-5μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating
3310
Solder (Pb-free) backside metallized hexagonal pyramid tips to an Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
3311
ARC (and Spectral Conversion) Layer: Concurrently deposit ARC layer (e.g., low-temperature PECVD SiNx) on both front and rear surfaces (ARC layer may also include spectral down-conversion); also helps with additional H passivation (Note: Mask peripheries of frontside solar cell & rear mirror during PECVD to facilitate cell / module interconnects)
3312
Self-aligned metallization (optional): Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
3314
Proceed with packaging the solar cells in solar modules/panels
End

FIG. 37

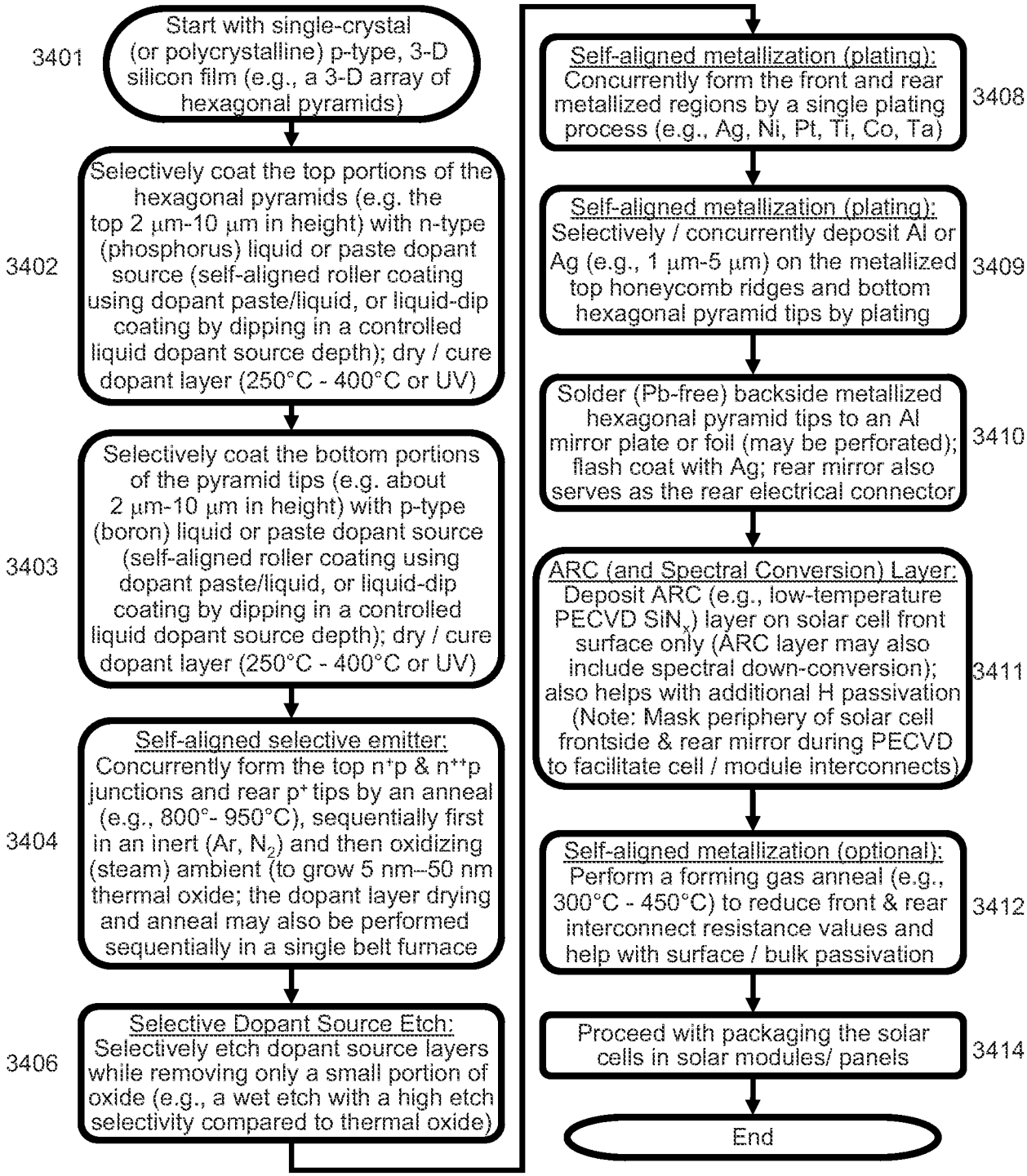

3401
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
3402
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3403
Selectively coat the bottom portions of the pyramid tips (e.g. about 2 μm-10 μm in height) with p-type (boron) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3404
Self-aligned selective emitter: Concurrently form the top n+p & n++p junctions and rear p+ tips by an anneal (e.g., 800°- 950°C), sequentially first in an inert (Ar, N2) and then oxidizing (steam) ambient (to grow 5 nm–50 nm thermal oxide; the dopant layer drying and anneal may also be performed sequentially in a single belt furnace
3406
Selective Dopant Source Etch: Selectively etch dopant source layers while removing only a small portion of oxide (e.g., a wet etch with a high etch selectivity compared to thermal oxide)
3408
Self-aligned metallization (plating): Concurrently form the front and rear metallized regions by a single plating process (e.g., Ag, Ni, Pt, Ti, Co, Ta)
3409
Self-aligned metallization (plating): Selectively / concurrently deposit Al or Ag (e.g., 1 μm-5 μm) on the metallized top honeycomb ridges and bottom hexagonal pyramid tips by plating
3410
Solder (Pb-free) backside metallized hexagonal pyramid tips to an Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
3411
ARC (and Spectral Conversion) Layer: Deposit ARC (e.g., low-temperature PECVD SiNx) layer on solar cell front surface only (ARC layer may also include spectral down-conversion); also helps with additional H passivation (Note: Mask periphery of solar cell frontside & rear mirror during PECVD to facilitate cell / module interconnects)
3412
Self-aligned metallization (optional): Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
3414
Proceed with packaging the solar cells in solar modules/ panels
End

FIG. 38

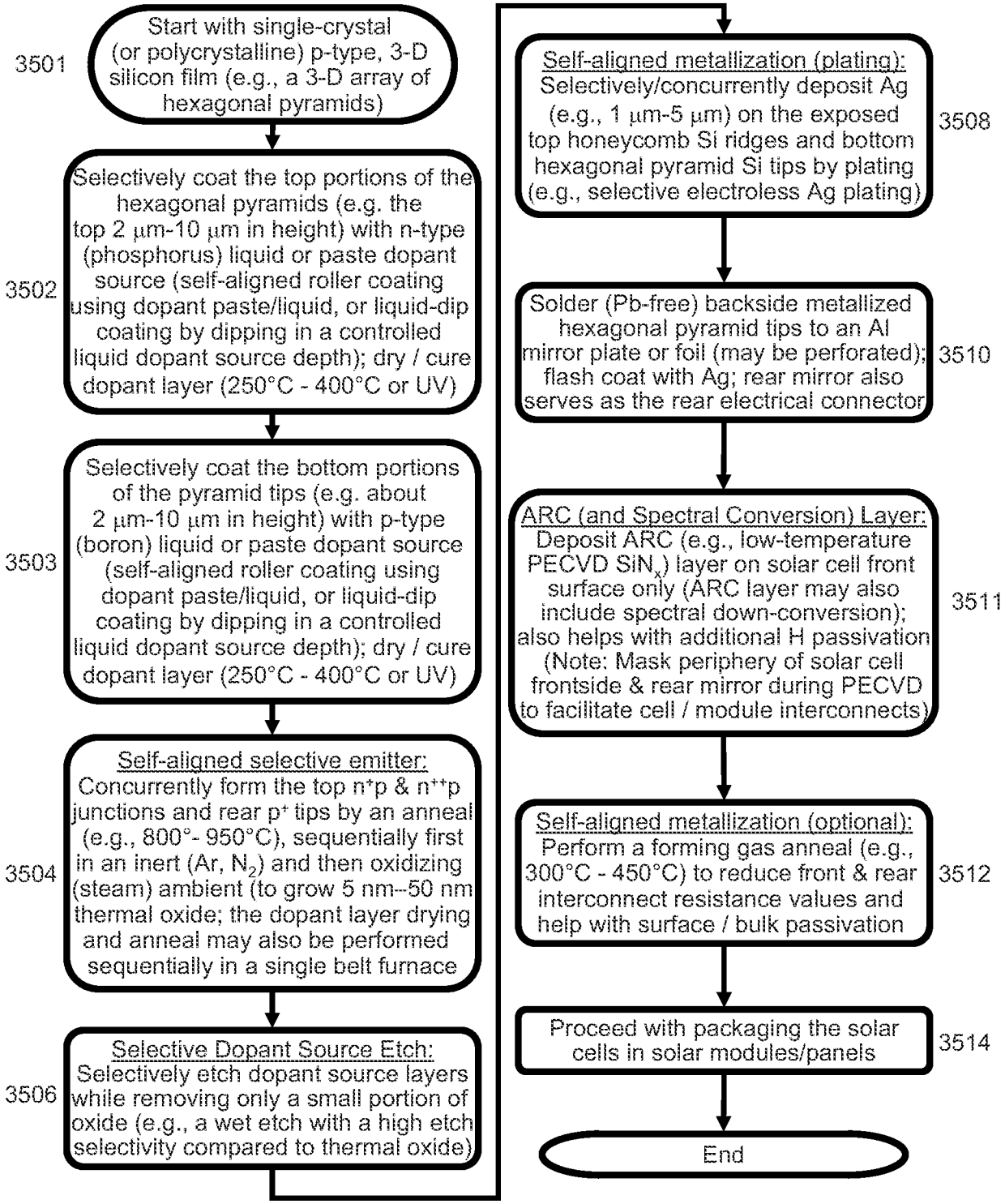

3501
Start with single-crystal (or polycrystalline) p-type, 3-D silicon film (e.g., a 3-D array of hexagonal pyramids)
3502
Selectively coat the top portions of the hexagonal pyramids (e.g. the top 2 μm-10 μm in height) with n-type (phosphorus) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3503
Selectively coat the bottom portions of the pyramid tips (e.g. about 2 μm-10 μm in height) with p-type (boron) liquid or paste dopant source (self-aligned roller coating using dopant paste/liquid, or liquid-dip coating by dipping in a controlled liquid dopant source depth); dry / cure dopant layer (250°C - 400°C or UV)
3504
Self-aligned selective emitter: Concurrently form the top n+p & n++p junctions and rear p+ tips by an anneal (e.g., 800°- 950°C), sequentially first in an inert (Ar, N2) and then oxidizing (steam) ambient (to grow 5 nm--50 nm thermal oxide; the dopant layer drying and anneal may also be performed sequentially in a single belt furnace
3506
Selective Dopant Source Etch: Selectively etch dopant source layers while removing only a small portion of oxide (e.g., a wet etch with a high etch selectivity compared to thermal oxide)
3508
Self-aligned metallization (plating): Selectively/concurrently deposit Ag (e.g., 1 μm-5 μm) on the exposed top honeycomb Si ridges and bottom hexagonal pyramid Si tips by plating (e.g., selective electroless Ag plating)
3510
Solder (Pb-free) backside metallized hexagonal pyramid tips to an Al mirror plate or foil (may be perforated); flash coat with Ag; rear mirror also serves as the rear electrical connector
3511
ARC (and Spectral Conversion) Layer: Deposit ARC (e.g., low-temperature PECVD SiNx) layer on solar cell front surface only (ARC layer may also include spectral down-conversion); also helps with additional H passivation (Note: Mask periphery of solar cell frontside & rear mirror during PECVD to facilitate cell / module interconnects)
3512
Self-aligned metallization (optional): Perform a forming gas anneal (e.g., 300°C - 450°C) to reduce front & rear interconnect resistance values and help with surface / bulk passivation
3514
Proceed with packaging the solar cells in solar modules/panels
End

FIG. 39

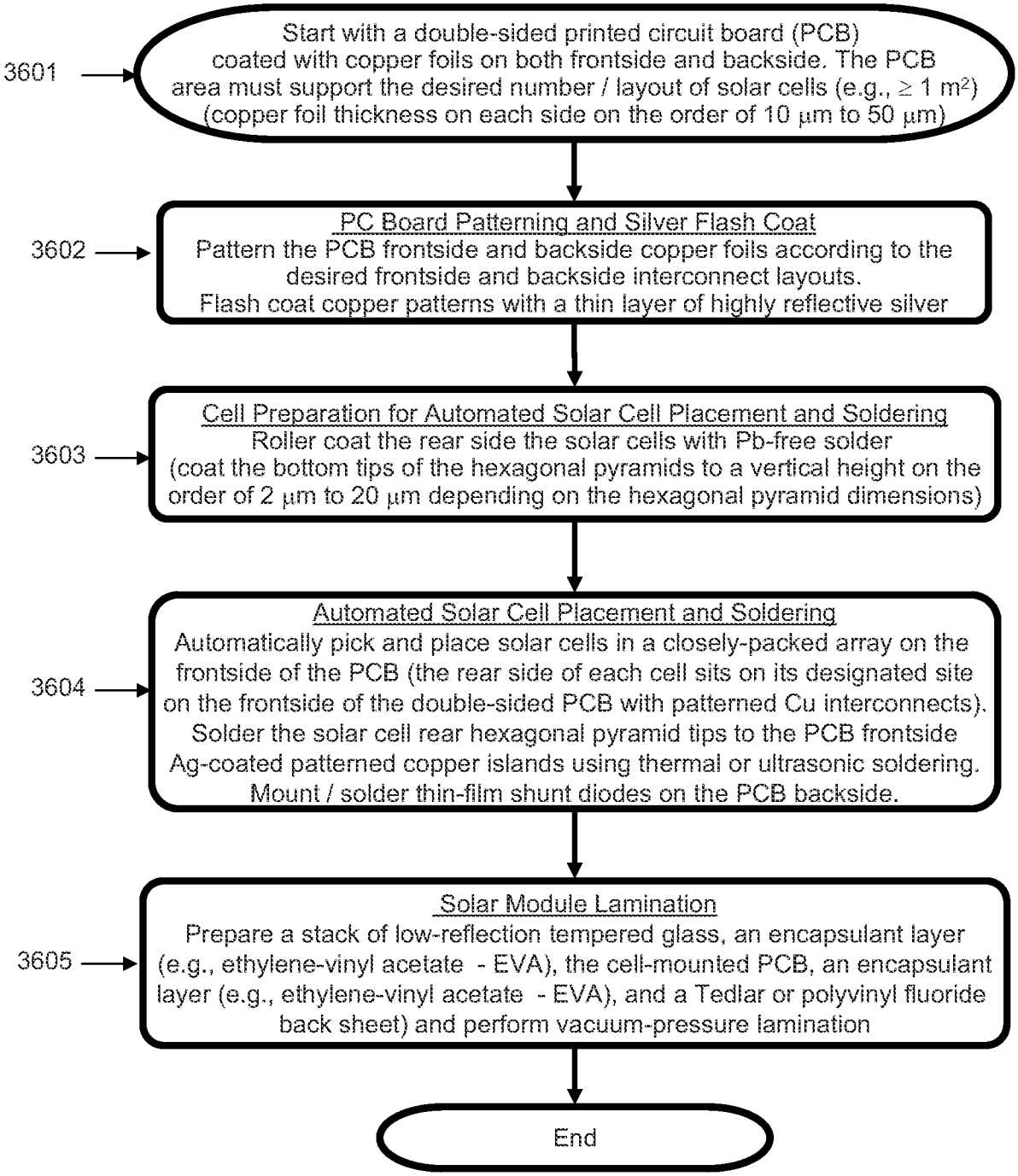

3601
Start with a double-sided printed circuit board (PCB) coated with copper foils on both frontside and backside. The PCB area must support the desired number / layout of solar cells (e.g., ≥ 1 m²) (copper foil thickness on each side on the order of 10 μm to 50 μm)
3602
PC Board Patterning and Silver Flash Coat
Pattern the PCB frontside and backside copper foils according to the desired frontside and backside interconnect layouts.
Flash coat copper patterns with a thin layer of highly reflective silver
3603
Cell Preparation for Automated Solar Cell Placement and Soldering
Roller coat the rear side the solar cells with Pb-free solder (coat the bottom tips of the hexagonal pyramids to a vertical height on the order of 2 μm to 20 μm depending on the hexagonal pyramid dimensions)
3604
Automated Solar Cell Placement and Soldering
Automatically pick and place solar cells in a closely-packed array on the frontside of the PCB (the rear side of each cell sits on its designated site on the frontside of the double-sided PCB with patterned Cu interconnects).
Solder the solar cell rear hexagonal pyramid tips to the PCB frontside Ag-coated patterned copper islands using thermal or ultrasonic soldering.
Mount / solder thin-film shunt diodes on the PCB backside.
3605
Solar Module Lamination
Prepare a stack of low-reflection tempered glass, an encapsulant layer (e.g., ethylene-vinyl acetate - EVA), the cell-mounted PCB, an encapsulant layer (e.g., ethylene-vinyl acetate - EVA), and a Tedlar or polyvinyl fluoride back sheet) and perform vacuum-pressure lamination
End

FIG. 40

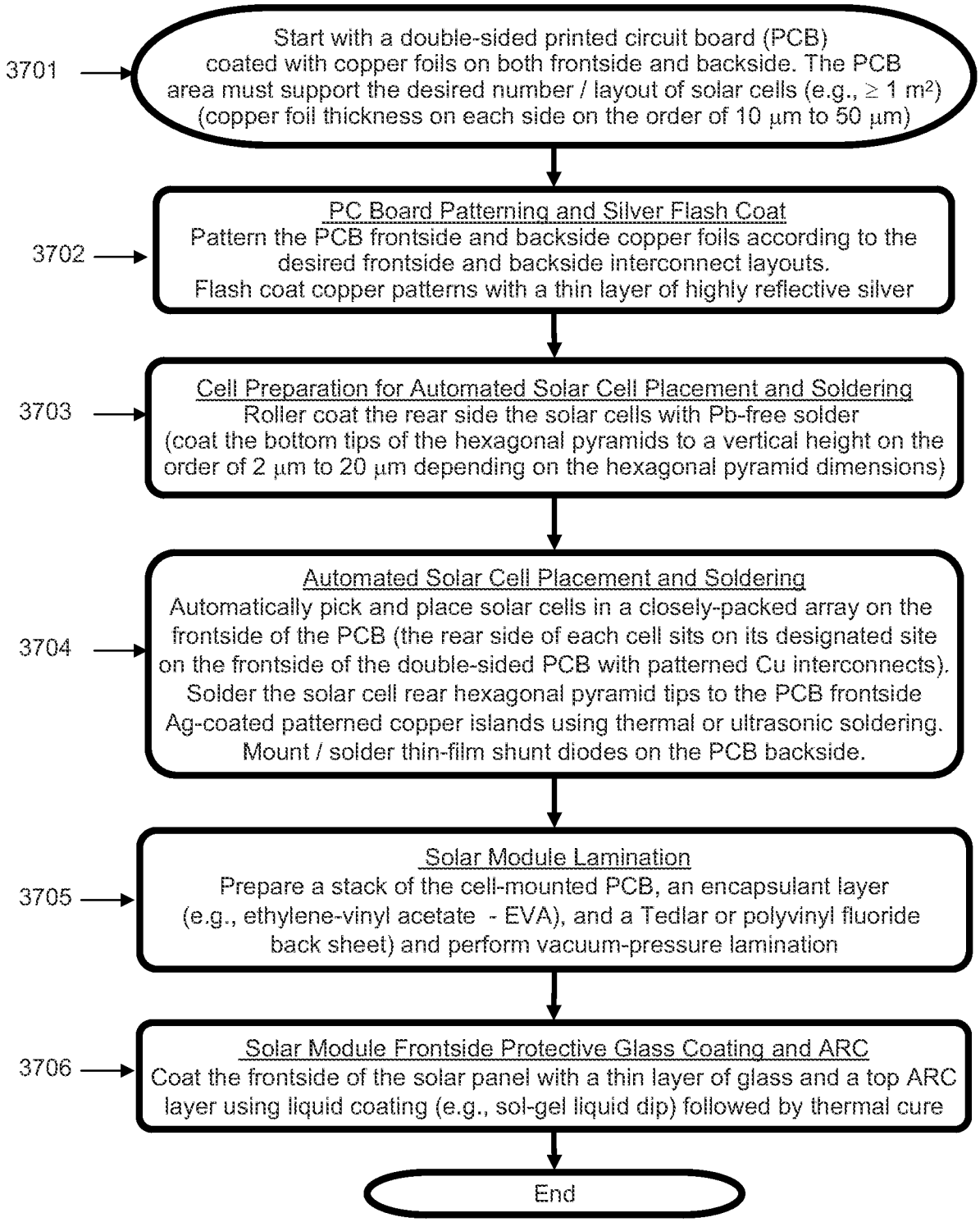

3701
Start with a double-sided printed circuit board (PCB) coated with copper foils on both frontside and backside. The PCB area must support the desired number / layout of solar cells (e.g., ≥ 1 m²) (copper foil thickness on each side on the order of 10 μm to 50 μm)
3702
PC Board Patterning and Silver Flash Coat
Pattern the PCB frontside and backside copper foils according to the desired frontside and backside interconnect layouts.
Flash coat copper patterns with a thin layer of highly reflective silver
3703
Cell Preparation for Automated Solar Cell Placement and Soldering
Roller coat the rear side the solar cells with Pb-free solder (coat the bottom tips of the hexagonal pyramids to a vertical height on the order of 2 μm to 20 μm depending on the hexagonal pyramid dimensions)
3704
Automated Solar Cell Placement and Soldering
Automatically pick and place solar cells in a closely-packed array on the frontside of the PCB (the rear side of each cell sits on its designated site on the frontside of the double-sided PCB with patterned Cu interconnects).
Solder the solar cell rear hexagonal pyramid tips to the PCB frontside Ag-coated patterned copper islands using thermal or ultrasonic soldering.
Mount / solder thin-film shunt diodes on the PCB backside.
3705
Solar Module Lamination
Prepare a stack of the cell-mounted PCB, an encapsulant layer (e.g., ethylene-vinyl acetate - EVA), and a Tedlar or polyvinyl fluoride back sheet) and perform vacuum-pressure lamination
3706
Solar Module Frontside Protective Glass Coating and ARC
Coat the frontside of the solar panel with a thin layer of glass and a top ARC layer using liquid coating (e.g., sol-gel liquid dip) followed by thermal cure
End

FIG. 41

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/66011

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/0264, 31/052 (2010.01)
USPC - 136/259, 136/261
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) ? H01L 31/0264, 31/052 (2010.01)
USPC ? 136/259, 136/261

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8) ? H01L 31/0264, 31/052 (2010.01), USPC ? 136/259, 136/261; 257/E31.004, 257/E27.125 - Keyword search, as below.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO PubWest (databases: PGPB,USPT,USOC,EPAB,JPAB); DialogWeb (databases: 349, 344, 351, 347, 371, 348); Google Scholar - Search Terms: photovoltaic, solar, cell, array, panel, element, unit, three dimensional, polygon, hexagon, triangle, square, quadrilateral, rectangular, pyramid, trapezoid, octagon, width, dimension, diameter, taper, angled,

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/0157283 A1 (MOSLEHI) 3 July 2008 (03.07.2008) para [0131]; [0177]; [0149]; [0070]; [0092]; [0142]; [0144]; [0234]; [0068]; [0178]; [0067]; Fig. 65	1-6
A	US 2008/0264477 A1 (MOSLEHI) 30 October 2008 (30.10.2008)	1-6
A	US 2006/0283495 A1 (GIBSON) 21 December 2006 (21.12.2006)	1-6

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 April 2010 (28.04.2010)	07 MAY 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/66011

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: claims 1-6, directed to a three-dimensional thin film silicon substrate comprising a first and second plurality of unit cells; wherein each unit cell comprises: a top and a bottom aperture, and a wall connecting said top and bottom aperture, wherein the apertures comprise a single convex polygon shape, and wherein the top aperture diameter (dimension) is larger than the bottom aperture diameter (dimension).

- Please see extra sheet for continuation -

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-6

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/66011

Continuation of Box III: Lack of Unity of Invention

Group II: claims 7-18, directed to a method for making a three-dimensional thin film solar cell, comprising: patterning a reusable semiconductor template with a plurality of convex polygonal trenches; forming a sacrificial layer on a surface of said reusable semiconductor template; depositing a silicon film onto said sacrificial layer; removing said silicon film from said reusable semiconductor template; removing a plurality of tips from said silicon film to create a plurality of holes;
doping said silicon film; and metallizing said silicon film..

Group III: claims 19-24, directed to a method for making holes in a silicon substrate having a plurality of tips comprising: depositing a hard masking layer on the substrate; selectively removing said hard masking layer from the plurality of tips; etching the substrate to remove the plurality of tips; and removing a remainder of said hard masking layer.

The inventions listed as Groups I - III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical feature of the Group I claims is a three-dimensional thin film silicon substrate comprising a first and second plurality of unit cells; wherein each unit cell comprises: a top and a bottom aperture, and a wall connecting said top and bottom aperture, wherein the apertures comprise a single convex polygon shape, and wherein the top aperture diameter (dimension) is larger than the bottom aperture diameter (dimension) - not required by the claims of Groups II or III. The special technical feature of the Group II claims is a a method for making a three-dimensional thin film solar cell, comprising: patterning a reusable semiconductor template with a plurality of convex polygonal trenches; forming a sacrificial layer on a surface of said reusable semiconductor template; depositing a silicon film onto said sacrificial layer; removing said silicon film from said reusable semiconductor template; removing a plurality of tips from said silicon film to create a plurality of holes;
doping said silicon film; and metallizing said silicon film - not required by the claims of Groups I or III. The special technical feature of the Group III claims is a method for making holes in a silicon substrate having a plurality of tips comprising: depositing a hard masking layer on the substrate; selectively removing said hard masking layer from the plurality of tips; etching the substrate to remove the plurality of tips; and removing a remainder of said hard masking layer - not required by the claims of Groups I or II. None of these special technical features is common to the other group, nor do they correspond to a special technical feature in the other group.

The only common technical element shared by the above groups is that they are related to silicon layers which comprise openings. This common technical element does not represent an improvement over the prior art of US 2008/0264477 A1 to Moslehi (see abstract, claim 1, para [0039], [0088], [0097], [0130], [0136]). Therefore, the inventions of Groups I - III lack unity of invention under PCT Rule 13 because they do not share a same or corresponding special technical feature.