(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
6 April 2006 (06.04.2006)

PCT

(10) **International Publication Number**
WO 2006/036566 A1

(51) **International Patent Classification**[7]: **H01L 33/00**

(21) **International Application Number:** PCT/US2005/032896

(22) **International Filing Date:** 15 September 2005 (15.09.2005)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) **Priority Data:**
10/951,042 22 September 2004 (22.09.2004) US

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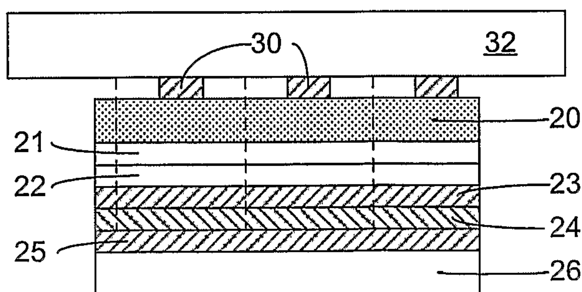
(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** HIGH EFFICIENCY GROUP III NITRIDE-SILICON CARBIDE LIGHT EMITTING DIODE



(57) **Abstract:** A method and resulting structures are disclosed for fabricating a high efficiency high extraction light emitting diode suitable for packaging. The method includes the steps of adding a light emitting active portion of wide-bandgap semiconductor material to a conductive silicon carbide substrate, joining the added active portion to a conductive sub-mounting structure, and removing a portion of the silicon carbide substrate opposite the added active portion to thereby reduce the overall thickness of the joined substrate, active portion and sub-mounting structure. The resulting the sub-mounting structure can be joined to a lead frame with the active portion positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active portion from the lead frame and avoid undesired electrical contact between the active portion and the lead frame.

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HIGH EFFICIENCY GROUP III NITRIDE-SILICON CARBIDE LIGHT EMITTING DIODE

Background

[0001] The present invention relates to light emitting diodes ("LEDs") and in particular relates to high-brightness light emitting diodes formed from Group III nitride active structures on silicon carbide substrates.

[0002] In general, light emitting diodes represent one class of photonic devices that are commercially well-established for numerous applications. For the first few decades of the semiconductor era, however, such light emitting diode applications (although numerous and successful) were limited to relatively low-intensity applications such as indicator lights or small displays (e.g., handheld calculators). One reason for such limited application was based in the available semiconductor materials, most typically silicon (Si) and gallium arsenide (GaAs). Basically, and as well-understood in this art, a light emitting diode emits light based upon the recombination of electrons and holes under the influence of an applied bias across a p-n junction. Because the frequency (and thus the wavelength) of emitted light is directly related to the energy of the transition leading to the recombination ($E = h\nu$), the frequency of light emitted by a light emitting diode is based upon (and ultimately limited by) the material's bandgap.

[0003] In that regard, GaAs has a bandgap of 1.4 electron volts (eV). Accordingly, the highest-energy transitions that GaAs can produce are in the red, orange and yellow portions of the visible spectrum.

[0004] A number of commonly assigned patents and co-pending patent applications likewise discuss the theory and nature of light emitting diodes, including but not limited to U.S. Patent Nos. 6,459,100; 6,373,077; 6,201,262; 6,187,606; 5,912,477; 5,416,342; and 5,838,706; and Published U.S. Applications Nos. 20020022290; 20020093020; and 20020123164.

[0005] In order to further commercialize light emitting diode applications, however, colors other than red, orange and yellow must be available. Specifically blue and green light emitting diodes are required (along with red diodes) to create white light or full color displays. Because these colors represent higher-energy portions of the visible spectrum, they require larger transitions than the bandgaps of silicon or

gallium arsenide can provide. Thus, in the last two decades, significant interest has been developed—and progress generated—in a wider bandgap materials such as silicon carbide (2.99 eV for the 6H polytype) and the Group III nitride's (e.g., 3.36 eV for gallium nitride). The Group III nitrides are particularly preferred because they are "direct" (and thus higher-efficiency) emitters.

[0006] In addition to providing blue, green, or white light (as well as emissions in the ultraviolet range), the Group III nitride light emitting diodes have the potential to provide replacement for long-standing illumination technologies such as incandescent and fluorescent lighting. In comparison to such mature technologies, light emitting diodes ("solid-state lighting") are longer-lasting, physically more rugged, use less power, and are more efficient. Historically, however, LEDs have lacked brightness comparable to incandescent, fluorescent or vapor-discharge lights and thus these older technologies have continued to occupy the field. Only recently, have white LEDs (or LED-based white-emitting devices) begun to make inroads into commercial lighting applications, with most of these being in smaller applications such as flashlights and related items.

[0007] It will be understood of course that a single diode will not produce a white emission because white light is a combination of non-white frequencies. In some LED applications, however, a blue or UV-emitting LED can be used in conjunction with a phosphor to produce white light from a single diode source.

[0008] In commercial embodiments of light emitting diodes (e.g., the XBRIGHT™ diodes offered by the assignee herein; Cree, Inc.; Durham, North Carolina) recent advances have included an inverted device design. U.S. Patent No. 6,740,906 discusses aspects of this design as does U.S. Patent Application Publication No. 20020123164. In this type of design, the Group III active layers are grown (typically epitaxially) on a silicon carbide substrate. Light emitting diodes of this type are then mounted with their epitaxial layers ("epilayers") "down" rather than "up"; i.e., the silicon carbide portions forms the display face of the mounted device while the epitaxial layers are mounted to and face a circuit or wiring most typically referred to as a "lead frame" that provides the electrical connection to the diode. The silicon carbide-up orientation increases light extraction from the device as set forth in the '906 patent and the '164 publication.

[0009] Silicon carbide can also be conductively doped. This provides advantages in comparison to sapphire based Group III nitride diodes. Because sapphire is an insulator, two top wire bonds are typically required to mount a working sapphire-based diode. In comparison, silicon carbide devices can be "vertically" oriented; i.e., with ohmic contacts on opposite ends of the device. Such vertical orientation is directly analogous to diodes formed in other conductive semiconductor materials such as gallium arsenide (GaAs), and thus the same mounting orientations and techniques can be used.

[0010] Although these "inverted" devices have successfully provided significant practical and commercial improvements, their "epilayer-down" orientation requires different, and to some extent more sophisticated, mounting on lead frames. In particular, because the active portion (p-n junction, multiple quantum well, etc.) is positioned closely adjacent to the lead frame, avoiding short circuits or other undesired interactions between the active portion and lead frame becomes more difficult.

[0011] For example, conventional LEDs (including Group III nitride on SiC devices) are often mounted on the lead frame using conductive silver epoxy. Silver epoxy is a mixture of more than about 50 percent by weight of microscopic silver particles with epoxy resin precursors. When used to connect electronic devices to circuits (or circuit boards) the silver epoxy provides flexibility, relative ease of handling, conductivity and good heat transfer properties. Because silver epoxy is (purposely) applied as a viscous liquid, it can and will flow accordingly and, unless other steps are taken, will tend to surround lower portions of any diode mounted with it. As noted above, if the active portions are adjacent the lead frame, the flowing silver epoxy can contact the active portion and cause short circuiting or other undesired interactions.

[0012] As a result, many conventional light emitting diode mounting techniques are either too difficult, too unreliable or simply unavailable for inverted Group III nitride silicon carbide devices. Other specific techniques should or must be incorporated to avoid these problems.

[0013] As another potential solution, the inverted device can be positioned on some sort of sub-structure, with the sub-structure being attached to the lead frame. Examples include U.S. Patent Application Publication No. 20030213965. The sub-

structure is included to add sufficient thickness to remove the active portions farther from the lead frame and its silver epoxy or related materials. As set forth in No. 20030213965, however, soldering the device to a substructure can undesirably tilt the device with respect to the sub-structure and thereby exacerbate the short-circuiting problem.

[0014] As another problem, the extra thickness resulting from the presence of the substructure is also a disadvantage, because manufacturers of end-use products frequently demand smaller and smaller—including "thinner"—light emitting diodes. Such demand includes, for example, flat-panel displays on small devices such as cellular phones and personal digital assistants ("PDAs").

[0015] Accordingly, it remains a continuing goal to increase the current capacity, light output (power) and light extraction (geometry) capabilities of inverted light emitting diodes while concurrently reducing their size and particularly reducing their thickness. It remains a similar goal to produce such diodes in designs that can be conveniently incorporated into lead frames, packages and circuits in a manner similar or identical to related diodes.

Summary

[0016] In one aspect, the invention is a wafer structure for high-efficiency inverted chip light emitting diode precursors. The wafer structure comprises a conductive silicon carbide substrate wafer, at least one light-emitting active layer on the substrate, at least one metal contact layer on the light emitting layer, a conductive sub-mounting structure on the metal contact layer, a plurality of ohmic contacts on the surface of the conductive silicon carbide substrate that is opposite from the light emitting active layer, and with the ohmic contacts defining a plurality of light emitting diode precursors.

[0017] In another aspect the invention is a method of fabricating and mounting a light emitting diode for high efficiency and extraction. In this aspect, the method comprises adding a light emitting active portion of wide-bandgap semiconductor material to a conductive silicon carbide substrate, joining the added active portion to a conductive sub-mounting structure, and removing a portion of the silicon carbide substrate opposite the added active portion to thereby reduce the overall thickness of

the joined substrate, active portion and sub-mounting structure. The resulting sub-mounting structure can be joined to a lead frame with the active portion positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active portion from the lead frame and avoid undesired electrical contact between the active portion and the lead frame.

[0018] In yet another aspect the method comprises adding a light emitting active layer of wide-bandgap semiconductor material to a conductive silicon carbide substrate wafer, adding at least one metal contact layer to the added active layers, joining the metal contact layer to a conductive sub-mounting wafer, removing a portion of the silicon carbide substrate wafer opposite the added active layers to thereby reduce the overall thickness of the joined wafers, adding ohmic contacts to the reduced silicon carbide substrate wafer and to the sub-mounting wafer to thereby define a plurality of individual diode precursors, separating the diode precursors into individual diodes, and joining the sub-mounting portion of the separated diodes to respective lead frames with the active layers positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active layers from the lead frame and avoid undesired electrical contact between the active layers and the lead frame.

[0019] In yet another aspect, the method comprises adding a light emitting active layer of wide-bandgap semiconductor material to a conductive silicon carbide substrate wafer, joining the added active layer to a conductive sub-mounting wafer, adding ohmic contacts to the reduced silicon carbide substrate wafer and to the sub-mounting wafer to thereby define a plurality of individual diode precursors, separating the diode precursors into individual diodes, and joining the sub-mounting portion of the separated diodes to respective lead frames with the active layers positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active layers from the lead frame and avoid undesired electrical contact between the active layers and the lead frame.

[0020] The foregoing and other objects and advantages of the invention and the manner in which the same are accomplished will become clearer based on the followed detailed description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

[0021] Figures 1 through 19 are schematic cross-sectional illustrations of the method steps of the invention and the resulting structures.

[0022] Figure 20 is an emission plot taken from a current commercially-available diode in which the silicon carbide substrate forms the emission face.

[0023] Figures 21 through 24 are corresponding emission plots taken from diodes according to the present invention.

[0024] Figures 25-29 and 31-33 are scanning electron microscope (SEM) photographs of diode portions illustrating aspects of the present invention.

[0025] Figure 30 is an x-ray spectrum corresponding to an analysis of portions of the diode illustrated in Figure 29.

Detailed Description

[0026] In a broad sense the invention is an aluminum indium gallium nitride based light emitting region sandwiched between a semiconducting or conducting substrate and a thin silicon carbide layer. When mounted, the conducting substrate forms the bottom of the device and this bottom portion has a thickness adequate to allow the use of epoxy pastes for chip attachment into a package. The upper silicon carbide layer is thin enough to limit the final device thickness to less than about 1 50 μm, which is adequate for most surface mount light emitting diode applications. This results in a thin, high-brightness light emitting diode chip with low forward voltage that can be attached by the manufacturer with standard electrically conducting epoxy pastes and that has a single wire bond on top. The design results in a more Lambertian emitting pattern. As a result, coupling to a phosphor for conversion to white light is expected to be more efficient over the use of currently available silicon carbide-based chips. The invention also allows for increasing size without the loss of efficiency.

[0027] The invention has application for light emitting diode displays, indicators, light conversion, small and large chips, and any other light emitting diode applications.

[0028] Certain method aspects of the invention are illustrated in Figures 1 through 19. Although Figures 1-19 do not illustrate every conceivable step, and although the

method can be described in fewer steps then illustrated in Figures 1-19, it will be understood that Figures 1-19 provide the skilled person with the information necessary to practice the information without undue experimentation. Similarly, Figures 1-19 are schematic, and not to scale.

[0029] Figure 1 illustrates that the method can be described as starting with a conductive silicon carbide wafer 20, preferably n-type, upon which the desired or necessary active layers are then fabricated. As will be described further herein, Figure 1 illustrates a "thick" silicon carbide wafer 20 which will later be trimmed for purposes to be described herein. As used herein, the term "thick" refers to a wafer with a thickness on the order of about 250-500 μm. Alternatively, the method could start with a "thinner" wafer having a thickness of about 75- 125 μm. A thicker wafer provides greater structural strength during a number of the steps described herein. Alternatively, the use of a thinner wafer, although less mechanically robust, can eliminate the steps described herein in which the substrate thickness is reduced.

[0030] Figure 2 illustrates two epitaxial active layers 21 and 22 as added to the substrate 20. In preferred embodiments these layers are n-type (21) and p-type (22) respectively. It will be understood, of course, that a number of different arrangements of one or more active layers (i.e., those layers in which the light-generating transitions occur) can be incorporated in devices of this type and that the illustrated active layer structure, although exemplary, is not limiting of the invention and that additional layers or and combinations of layers can be incorporated. Such layers and combinations can include buffer layers (usually adjacent the silicon carbide substrate), contact layers (e.g. p-GaN layers that enhance ohmic behavior at p-side contacts), and more complex active structures such as multiple quantum wells and superlattice structures. As used herein, the term "active layer structure" refers to a semiconductor structure that emits light when a current is applied. Typically, but not exclusively, some form of p-n junction structure is included. Figure 2 illustrates two layers (one p-type and one n-type) as being a basic junction structure for an LED.

[0031] Figure 3 illustrates the addition of one or more respective metal layers to the junction (epitaxial) side of the device. Two metal layers 23 and 24 are illustrated and it will be understood that these can be selected as desired or necessary from among those metals (or alloys or layered combinations of metals) that are best for light

reflection and ohmic contact purposes in conjunction with the Group III nitride active layers 21 and 22. It will be understood that although two metal layers 23, 24 are illustrated, such is exemplary rather than limiting of the invention and the number of layers can be increased for various purposes as desired or necessary consistent with the other objects of the invention. In this regard, Figures 15-19 expand upon the description of the metal layers. As another example, and as will be described with respect to Figure 8, this metal-deposition step can include the step of adding an etch-stop metal.

[0032] Figure 4 is inverted with respect to Figure 3 in order to illustrate the next step in which the device side of the structure is mounted to a second conductive wafer 26 or an equivalent multi-layer or composite structure. The second conductive wafer 26 is preferably attached to the metal layers 23 and 24 using a solder bond illustrated at 25 using pressure and heat with a solder layer 25 being first deposited on either the original wafer 20 (adjacent the metal layers 23 and 24) or on the second wafer 26 or both (e.g. Figures 16-19). The purpose of the second substrate wafer 26 is to support the structure for later mounting and grinding and to form a portion of the final device structure. Thus the wafer 26 must be sufficiently thick to serve this purpose, with presently preferred thicknesses being on the order of about 250 μm. It will be understood, however, that in a manner analogous to the original silicon carbide wafer 20, the second substrate wafer 26 can also be a thin wafer to start with, for example, on the order of 75 to 100 μm.

[0033] If both the original conductive wafer 20 and the second substrate wafer 26 are "thin" to start with, it will be understood that neither will need to be trimmed any further in the following steps described herein. Thinner substrates are, however, weaker in accordance with well understood principles of mechanical strengths of objects with respect to their geometric sizes and proportions. Thus, the use of "thicker" wafers combined with thinning steps is presently preferred.

[0034] Figure 5 illustrates the structure after the original silicon carbide substrate 20 has been mechanically thinned to a desired thickness, which is presently on the order of about 10-50 μm. As just noted, the process (e.g., Figures 1-4) can start with a thin substrate that acquires no further reduction. In preferred embodiments, however, the

original silicon carbide wafer 20 has a thickness sufficient to ease the fabrication steps illustrated in Figures 1 through 4.

[0035] Figure 6 illustrates an optional embodiment of the device in which the thinned silicon carbide substrate 20 is shaped or textured to produce a lenticular surface 27 for desired light extraction purposes. A number of texturing options are set forth in U.S. Patent Application Publication No. 20020123164 and thus will not be described in further detail herein. These can, however, be practiced by those of skill in this art without undue experimentation.

[0036] As illustrated in Figure 7, in the next step a plurality of ohmic contacts 30 representing a plurality of device precursors are added to the side of the silicon carbide substrate 20 opposite the epilayers 21 and 22. It will be understood that if the original substrate 20 carries a textured surface 27, then the portion of the substrate 20 underneath the ohmic contacts 30 need not carry such texturing.

[0037] Figure 8 schematically illustrates (with the vertical dotted lines) the step of dividing the original silicon carbide substrate wafer 20 into individual device precursors that are broadly designated at 31. The dividing step can be carried out by any appropriate technique that otherwise avoids interfering with the remaining process steps or with the resulting precursors or the finished devices. Exemplary methods include mechanical sawing, laser cutting, etching and water-jet cutting. Each of these is generally well-understood and can be practiced without undue experimentation by those of ordinary skill in this art. Figure 8 also illustrates that, if desired, an etch stop layer can be included when the metal layers 23 and 24 are originally added (Figure 3) to help control the depth and distance to which the etch is carried in the step illustrated in Figure 8. Such an etch stop layer is conductive and can be formed from an appropriate conductive oxide such as indium tin oxide (typically In_2O_3/SnO_2). Although the scale and schematic nature of Figure 8 do not illustrate an etch-stop layer per se, one exemplary position would be between the layers illustrated at 24 and 25 in Figure 8.

[0038] Additionally, although not illustrated in these schematic Figures, the divided edges of the device precursors 31 that result from the etching, can be passivated (typically with silicon oxide or silicon nitride) to isolate and protect the junctions or other necessary portions of the active layers 21 and 22.

[0039] As another option that is not illustrated at this point in these drawings, the ohmic contact that is later illustrated as 33 in Figure 11 can be added at this step provided that no subsequent thinning of the second substrate wafer 26 is required or carried out.

[0040] Figure 9 illustrates the next step in which the original substrate 20 side of the composite structure is attached to a temporary carrier 32. The temporary carrier 32 can be any structure that serves the intended purpose without otherwise interfering with the other method steps or with the resulting device precursors or devices. Typically, the temporary carrier 32 comprises a planar support that is sufficiently rigid for the task and that carries a temporary (i.e., releasable) bonding media. The temporary carrier 32 can comprise another substrate or grinding tape, both of which are widely available and well understood in this art and can be practiced without undue experimentation.

[0041] Figure 10 illustrates that the purpose of adding the temporary carrier is to provide the opportunity for thinning the second conductive wafer 26 (or an equivalent composite structure) to the desired thickness of between about 75 and 125 μm. Although the Figures are schematic, a comparison between Figure 4 and Figure 10 also illustrates a significant reduction in the overall thickness of the structure formed by and between the substrates 20 and 26.

[0042] Figure 11 illustrates the step of forming an ohmic contact 33 to the second substrate 26 (or its equivalent structure). The selection of metals for the ohmic contact and the method of forming the ohmic contact are generally well understood in this art and can be selected as desired provided that they are functionally consistent with the remainder of the method steps described herein.

[0043] Figure 12 illustrates the composite structure and the device precursors 31 after they have been removed from the temporary carrier 32. When the composite structure is in the stage of manufacture illustrated in Figure 12, the individual devices are tested, typically by probing in a manner well understood in this art to either confirm their operation or to identify those that (for whatever reason) were not formed correctly and will not operate. Those of ordinary skill in this art are well aware, of course, that on a typical wafer that can include dozens, hundreds, or even thousands

of device precursors, the failure of a small percentage is entirely normal and expected under typical manufacturing conditions.

[0044] Figure 13 illustrates the last step in which the devices are separated into individual diode structures one of which is broadly designated as 31.

[0045] In another aspect, the invention is a wafer structure for high-efficiency inverted chip light emitting diode precursors. In this aspect, the invention comprises the conductive silicon carbide substrate wafer 20, with at least one light-emitting active layer on the substrate wafer. Figure 2 illustrates two such layers at 21 and 22. At least one metal contact layer is on the light emitting layer and Figure 3 illustrates an embodiment with two metal layers 23 and 24 on the epitaxial layer 22. A conductive sub-mounting structure 26 (Figure 4) is on the metal contact layer, and is typically selected from the group consisting of metals and semiconductors, with silicon carbide being preferred.

[0046] In preferred embodiments the sub-mounting structure includes yet another metal solder layer 25 for attaching the sub-mounting structure to the silicon carbide wafer 20 and its epitaxial and metal layers. The metal layers can also be or include a mirror layer (i.e., a highly reflective metal) and can include etch stop metals for the purposes described with respect to the method aspects of the invention.

[0047] A plurality of ohmic contacts 30 are on the surface of the conductive silicon carbide substrate that is opposite from the light emitting active layers 21 and 22, with the ohmic contacts defining a plurality of light emitting diode precursors broadly designated at 31. Similarly, and as illustrated in Figures 11 and 12, the conductive sub-mounting structure carries another ohmic contact 33 opposite from the metal contact layers 23 and 24.

[0048] In a related embodiment that is schematically illustrated in Figures 8-12, the conductive silicon carbide substrate wafer 20 , the light-emitting active layers 21 and 22 and the metal contact layers 23 and 24 are physically separated into individual device precursors while the sub-mounting wafer 26 remains intact. This permits a passivation composition (not shown in Figures 8-12) to be added along the edges of the separated individual device precursors

[0049] In preferred embodiments, the conductive silicon carbide substrate wafer 20 is a single crystal and has a polytype selected from the group consisting of the 3C, 4H,

6H and 15R polytypes of silicon carbide. Similarly, the light-emitting active layers are Group III nitrides, with aluminum indium gallium nitride ($Al_xIn_yGa_{1-x-y}N$, where $0 \leq x, y \leq 1$) being particularly preferred, and indium gallium nitride ($In_yGa_{1-y}N$, exclusive of $y = 0$) being most preferred.

[0050] In the preferred embodiments the silicon carbide single crystal wafer 20 is no more than 25 microns thick between the ohmic contacts 30 and the active layers 21 and 22 active portion, and in the most preferred embodiments, the total dimension between and including the ohmic contacts 30 and 33 is no more than 100 microns.

[0051] Figure 14 is a schematic cross-sectional view of an individual diode 31 formed according to the method of the invention as just described and mounted for use. As with the other illustrations, it will be understood that Figure 14 is a schematic illustration and is not to scale. Furthermore, those of ordinary skill in this art will understand the more specific aspects of such a device and its mounting. In Figure 14, the diode 31 is mounted on an appropriate lead frame 34 which is formed of a conductive material, usually a silver-coated metal, and which provides the initial electrical connection to an appropriate circuit. As discussed in the Background, the diode 31 is typically held in place, at least partially, by a conductive epoxy 35 which includes conductive particles, often of (or coated with) silver (Ag). As Figure 14 illustrates, the active layers 21, 22 are positioned sufficiently above the lead frame 34 to minimize or eliminate the possibility that the silver epoxy 35 will contact the active layers 21, 22 during or after mounting, thus preventing the possibility of undesired current paths or short circuiting.

[0052] In order to illustrate the sequence of the method aspects of the invention, Figure 4 omits certain details and options that can be included. Some of these details and options are illustrated in Figures 15-19.

[0053] First, Figure 15 illustrates details about the metal layers 23 and 24. For purposes of comparison to the other Figures herein, Figure 15 broadly indicates the layers 23 and 24 using dashed lines and the position of the semiconductor layer 22 by the curved line. As Figure 15 illustrates, in preferred embodiments metal layer 23 is a three layer structure formed by a layer of platinum (Pt) that forms an ohmic contact 40. The platinum ohmic contact layer 40 is preferably thin enough to be transparent; i.e. it transmits at least fifty percent (50%) of incident light. A silver (Ag) mirror

layer 41 for light reflection is on the ohmic contact 40, and a barrier layer 42 not only covers, but also surrounds the ohmic contact and mirror layers 40, 41. As persons skilled in the metallurgy and semiconductor arts are well aware, silver tends to migrate among and between, and then react relatively quickly with, certain other metals and semiconductor materials. In the present invention, such migration is highly undesirable and thus the tin layer 42 is included to prevent silver from migrating beyond the mirror layer 41 and to similarly prevent the metal layer 24 from reacting with the silver mirror layer 41.

[0054] Other metals can be included in this portion of the structure, either in place of or in addition to those already described. For example, the barrier layer 42 can be formed of multiple layers, each of which can be a single metal or combination or alloy of two or more metals. In preferred embodiments, the barrier layer 42 is formed of such combinations or alloys of titanium, tungsten and platinum. The metals described with respect to Figure 15 are thus exemplary rather than limiting of the invention.

[0055] With the ohmic contact layer 40 and the mirror layer 41 in place and encapsulated by the barrier layer 42, Figure 15 further illustrates that the other metal layer 24 is on the barrier layer 42. In preferred embodiments the metal layer 24 is an alloy of gold (Au) and tin (Sn) for providing both excellent electrical conductivity and a secure bond when the original substrate and device (e.g. Figure 3) are brought together with the second substrate 26 and its metal layer 25 (e.g. Figure 4).

[0056] Figures 16-19 are included to illustrate that the entirely planar structure illustrated in Figure 4 is only one option and that diode precursors 31 can be formed as mesas before the first and second substrates 20, 26 and their respective structures, are joined to one another.

[0057] In Figure 16, the diode precursors 31 are mesas formed of the metal layers 23 and 24 and the semiconductor layers 21 and 22. In a similar manner, the metal layer 25 on the second substrate 26 can be formed as a plurality of mesas that correspond to, and can be aligned with, the diode precursors 31 on the first substrate 20. Partially or completely separating the device precursors 31 can, in certain circumstances, help prevent the later full separating step (e.g. Figure 13) from adversely affecting the metal layers 23 and 24 and the semiconductor layers 21 and 22. For example, if mechanical sawing is the desired separation technique, creating the mesas first will

help prevent the sawing action from mechanically affecting the metals and semiconductor layers in a fashion that damages or destroys their resulting end structure and function. As a more specific example, mechanical sawing can, in certain circumstances, carry the metals into undesired contact with the semiconductor materials creating inadvertent and undesired Schottky contacts (e.g. Figure 29).

[0058] In Figure 17, the precursors are again formed as mesas, but the metal layer 25 on the second substrate 26 remains as a full planar layer.

[0059] In Figure 18, only the metal layer 24 forms the mesa on the first substrate 20 while the metal layer 25 on the second substrate 26 is again formed as mesa.

[0060] Finally, in Figure 19, all of the layers are planer except for metal layer 24 which again forms mesas as in Figure 18.

[0061] As further noted elsewhere, the vertical structure of the resulting device (ohmic contacts at opposite ends rather than facing the same direction) permits the use of a single wire contact 36 for completing the electrical connections to the diode 31.

[0062] Figures 20 through 24 illustrate additional advantages of the invention. Each of these represents intensity measured in microwatts per square centimeter ($\mu W/cm^2$) plotted on a radial graph against the angle of measurement, with 0° representing the measurement from directly above the center of the diode. All of the measurements were taken using the mini-goniophotometer of an MAS 40 LED Station from Instrument Systems Optische Messtechnik (with North American offices at Instrument Systems Canada, 1960 Scott St., Suite 302 K1Z 8L8, Ottawa, Ontario, Canada) and with the results plotted using the IS-SPECWIN™ software from the same company.

[0063] Figure 20 illustrates an emission pattern representative of existing inverted chip designs and in particular represents the emission pattern of an XBRIGHT™ chip from Cree, Inc. of Durham, NC, the assignee of the present invention. Although the intensity is excellent in some directions, Figure 20 illustrates that the flux density is non-uniform (and not Lambertian) and thus highly dependent upon the direction of emission or (in complementary fashion) of observation. The diode measured and plotted in Figure 20 had a peak omission of 459 nm with a dominant wavelength of 464 nm with a full width at half maximum (FWHM) of 20 nm.

[0064] In comparison, Figures 21 through 24 illustrate emission patterns of several light emitting diodes according to the present invention. Each of Figures 21 through 24 illustrates a significant improvement in the uniformity of flux density as compared with the existing devices (Figure 20).

[0065] Figure 21 illustrates the emission pattern of a diode according to the present invention with a conventional straight cut, with a planar rather than a lenticular surface and without any bevels. The measured diode had a peak omission at 456 nanometers with a dominant portion at 461 nm and a FWHM of 19 nm.

[0066] Figure 22 illustrates the emission pattern of a diode according to the present invention with a beveled edge cut and a planar, rather than lenticular, surface. The measured diode had a peak output of 457 nm, a dominant wavelength of 462 nm, and a FWHM of 19 nm.

[0067] Figure 23 illustrates the emission pattern of a diode with a lenticular surface and straight cut edges. The measured diode had a peak wavelength of 455 nm, a dominant wavelength of 460 nm, and a FWHM of 19 nm.

[0068] Figure 24 illustrates the emission pattern of a diode according to the present invention with a lenticular surface and beveled edges. The measured diode had a peak wavelength of 457 nm, a dominant wavelength of 462 nm, and a FWHM of 19.6 nm.

[0069] Figures 25 through 33 are scanning electron microscope (SEM) photographs of a diode according to the present invention and certain of its portions.

[0070] The SEM photograph of Figure 25 illustrates a diode (at 300X magnification) corresponding to the schematic structure broadly designated at 31 in Figure 13, but with the thickness of the second substrate 26 not having been reduced. For reference purposes, the original substrate 20 is labeled as such in Figure 25 as is the ohmic contact 30. The diode includes a lenticular surface 27 and beveled edges 44, both for desired light-extraction purposes. The active layers 21 and 22 and the metal layers 23, 24 and 25 are not entirely visible in Figure 25 because they form a mesa (e.g. Figures 16 and 17) the edges of which are underneath the substrate 20.

[0071] Figures 26 and 27 are illustrations, taken at different magnifications, of one type of lenticular surface (27 in Figure 6) of the diode illustrated in Figure 25. A portion of the ohmic contact 30 also appears in Figure 27.

[0072] Figure 28 is a larger magnification (4000X) of an upper right hand edge portion of the diode of Figure 25. The original substrate 20 forms the top portion of Figure 28 and the mesa formed of the active layers 21 and 22 is visible immediately below the original substrate 20. Portions of the metal and solder layers 23, 24 and 25 are shown extending towards the edge of the diode.

[0073] Figure 29 is yet another SEM photograph of a diode according to the present invention and shows the lenticular surface 27, the original substrate 20, the second substrate 26, and the solder layer 25. Figure 29 also illustrates that if the metal layers are not joined properly, portions of gold and tin illustrated at 45 may migrate (or be forced) from their intended locations and come into direct contact with the substrate 20 to thus form undesired Schottky contacts. This can be confirmed with an x-ray spectrum such as illustrated in Figure 30 which is taken generally in the position circled at 46 in Figure 27. The x-ray spectrum confirms the presence of both gold and tin at this undesired position.

[0074] Figures 31, 32 and 33 illustrate alternative versions of the lenticular surface 27 of the diode 31. In Figure 31 the lenticular surface has a positive elliptical shape, in Figure 32 a positive pyramid shape, and in Figure 33 an off-center positive pyramid shape. The lenticular surface can be formed using techniques otherwise well understood in the art such as masking and patterning with photoresist, lasers, inductive coupling plasmas, or reactive ion etching, or can be embossed with a mask pattern and then selectively patterned with reactive ion etching.

[0075] In the drawings and specification there has been set forth a preferred embodiment of the invention, and although specific terms have been employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being defined in the claims.

Claims

1. A wafer structure for high-efficiency inverted chip light emitting diode precursors, said wafer structure comprising:

a conductive silicon carbide substrate wafer;

at least one light-emitting active layer on said substrate;

at least one metal contact layer on said light emitting layer;

a conductive sub-mounting structure on said metal contact layer;

a plurality of ohmic contacts on the surface of said conductive silicon carbide substrate wafer that is opposite from said light emitting active layer, said ohmic contacts defining a plurality of light emitting diode precursors.

2. A wafer structure according to Claim 1 wherein:

said conductive silicon carbide substrate wafer, said light-emitting active layer and said metal contact layer are physically separated into individual device precursors; and

said sub-mounting wafer remains undivided.

3. A wafer structure according to Claim 2 and further comprising a passivation composition along the separated edges of said separated individual device precursors

4. A wafer structure according to Claim 1 wherein said conductive silicon carbide substrate wafer is a single crystal and has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide and said light-emitting active layer is a Group III nitride.

5. A wafer structure according to Claim 1 wherein said light-emitting active layer is indium gallium nitride.

6. A wafer structure according to Claim 1 comprising a plurality of metal contact layers.

7. A wafer structure according to Claim 6 wherein said plurality of metal contact layers comprises:

a solder layer for joining said conductive silicon carbide substrate wafer to said conductive sub-mounting structure;

a silver layer for providing a mirror that enhances light extraction; and

a barrier layer on and surrounding said silver layer for preventing silver from said silver layer from migrating beyond said silver layer.

8. A wafer structure according to Claim 7 wherein said barrier layer is selected from the group consisting of platinum, tungsten and titanium and layers and alloys thereof.

9. A wafer structure according to Claim 6 wherein at least one metal contact layer is a mirror.

10. A wafer structure according to Claim 6 comprising at least one conducting etch-stop layer.

11. A wafer structure according to Claim 1 wherein said conductive sub-mounting structure is selected from the group consisting of silicon carbide, metals, and semiconductors.

12. A wafer structure according to Claim 1 wherein said conductive sub-mounting structure comprises a composite of at least two different materials.

13. A wafer structure according to Claim 1 comprising an ohmic contact on said conductive sub-mounting structure opposite from said metal contact layer.

14. A wafer structure according to Claim 13 having a total dimension between and including said ohmic contacts of no more than 100 microns

15. A wafer structure according to Claim 1 wherein said silicon carbide single crystal wafer is no more than 25 microns thick between said ohmic contacts to said wafer and said active layer on said wafer.

16. A wafer structure according to Claim 1 wherein said conductive silicon carbide wafer has a lenticular surface for increasing the light extraction from diodes separated from said wafer structure.

17. A method of fabricating a high efficiency high extraction light emitting diode suitable for packaging, the method comprising:

adding a light emitting active portion of wide-bandgap semiconductor material to a conductive silicon carbide substrate;

joining the added active portion to a conductive sub-mounting structure; and

removing a portion of the silicon carbide substrate opposite the added active portion to thereby reduce the overall thickness of the joined substrate, active portion and sub-mounting structure.

18. A fabricating method according to Claim 17 comprising joining the sub-mounting structure to a lead frame with the active portion positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active portion from the lead frame and avoid undesired electrical contact between the active portion and the lead frame.

19. A fabricating method according to Claim 17 wherein the step of adding the light emitting active portion comprises adding a Group III nitride semiconductor structure.

20. A fabricating method according to Claim 19 comprising adding at least one layer of indium gallium nitride.

21. A fabricating method according to Claim 17 further comprising:

adding at least one metal layer to the added active portion prior to the step of joining the active portion to the sub-mounting structure; and

joining the metal layer to the sub-mounting structure.

22. A fabricating method according to Claim 17 wherein the step of joining the added active portion to a sub-mounting structure comprises joining the active portion to a metal or a conductive semiconductor.

23. A fabricating method according to Claim 17 comprising passivating the light emitting active portion.

24. A fabricating method according to Claim 17 comprising reducing the thickness of the sub-mounting structure following the step of joining the active structure to the sub-mounting structure.

25. A fabricating method according to Claim 24 comprising positioning the conductive silicon carbide substrate on a temporary carrier prior to the step of reducing the thickness of the sub-mounting structure.

26. A fabricating method according to Claim 17 comprising forming a lenticular surface on the reduced silicon carbide substrate.

27. A method of fabricating a high efficiency high extraction light emitting diode according to Claim 17 comprising:

adding an active layer of the wide-bandgap semiconductor material to a conductive silicon carbide wafer;

adding at least one metal contact layer to the added active layers;

joining the metal contact layer to a conductive sub-mounting wafer;

removing a portion of the silicon carbide substrate wafer opposite the added active layers to thereby reduce the overall thickness of the joined wafers;

adding ohmic contacts to the reduced silicon carbide substrate wafer and to the sub-mounting wafer to thereby define a plurality of individual diode precursors; and

separating the diode precursors into individual diodes.

28. A fabricating method according to Claim 27 comprising joining the sub-mounting portion of the separated diodes to respective lead frames with the active layers positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active layers from the lead frame and avoid undesired electrical contact between the active layers and the lead frame.

29. A fabricating method according to Claim 27 comprising forming a mesa structure that includes at least the metal contact wafer prior to the step of joining the substrate wafer to the sub-mounting wafer.

30. A fabricating method according to Claim 29 comprising forming a mesa structure that includes at least a portion of the light emitting active layer.

31. A fabricating method according to Claim 27 comprising forming a metal solder layer on the sub-mounting wafer prior to joining the silicon carbide substrate wafer to the sub-mounting wafer; and

thereafter joining the metal contact layer on the silicon carbide substrate to the solder layer on the sub-mounting wafer.

32. A fabricating method according to Claim 27 comprising partially separating portions of the diode precursors from one another while maintaining the sub-mounting wafer intact.

33. A fabricating method according to Claim 32 wherein the step of partially separating the diode precursors is selected from the group consisting of etching, sawing, laser cutting, and water jet cutting.

34. A fabricating method according to Claim 32 comprising implant isolating the partially separated diode precursors.

35. A fabricating method according to Claim 32 comprising passivating the edges of the partially separated diode precursors.

36. A fabricating method according to Claim 32 comprising testing the partially separated diode precursors.

37. A fabricating method according to Claim 27 comprising:

positioning the joined conductive silicon carbide substrate wafer and the sub-mounting wafer on a temporary carrier with the side of the conductive silicon carbide wafer opposite the active layer being the side on the temporary carrier;

reducing the thickness of the sub-mounting layer while the joined wafers are on the temporary carrier; and

removing the joined wafers from the temporary carrier.

38. A method of fabricating a high efficiency high extraction light emitting diode suitable for packaging, the method comprising:

adding a light emitting active layer of wide-bandgap semiconductor material to a conductive silicon carbide substrate wafer;

joining the added active layer to a conductive sub-mounting wafer;

adding ohmic contacts to the silicon carbide substrate wafer and to the sub-mounting wafer to thereby define a plurality of individual diode precursors; and

separating the diode precursors into individual diodes.

39. A fabricating method according to Claim 38 comprising joining the sub-mounting portion of the separated diodes to respective lead frames with the active layers positioned between the silicon carbide substrate and the sub-mounting structure to thereby use the sub-mounting structure to separate the active layers from the lead frame and avoid undesired electrical contact between the active layers and the lead frame.

40. A fabricating method according to Claim 48 wherein the step of adding a light emitting active layer comprises adding a Group III nitride layer.

41. A fabricating method according to Claim 48 comprising partially separating portions of the diode precursors from one another while maintaining the sub-mounting wafer intact.

42. A fabricating method according to Claim 52 comprising implant isolating the partially separated diode precursors.

43. A fabricating method according to Claim 52 comprising passivating the edges of the partially separated diode precursors.

44. A fabricating method according to Claim 52 comprising testing the partially separated diode precursors.

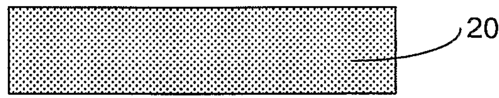


Fig. 1

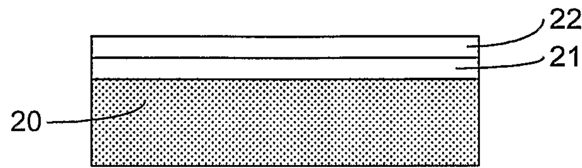


Fig. 2

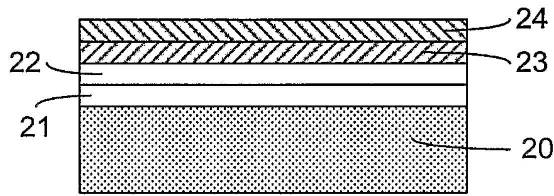


Fig. 3

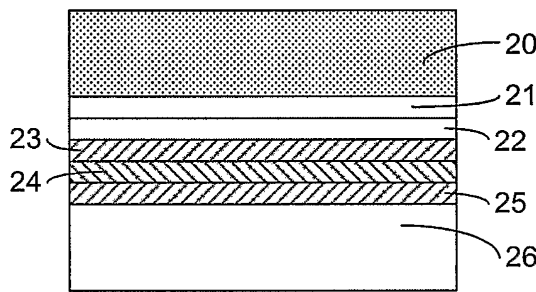


Fig. 4

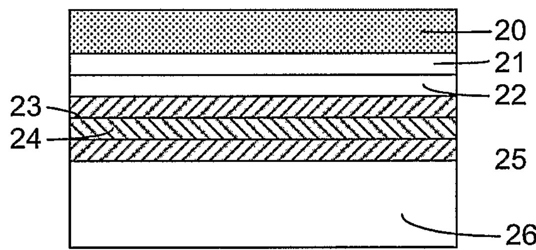


Fig. 5

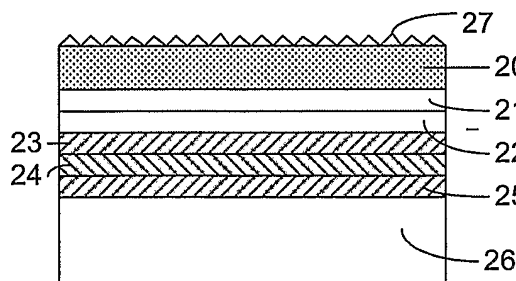


Fig. 6

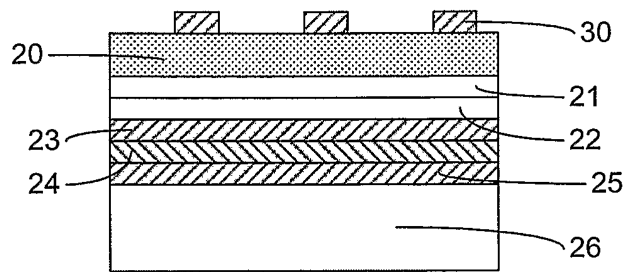


Fig. 7

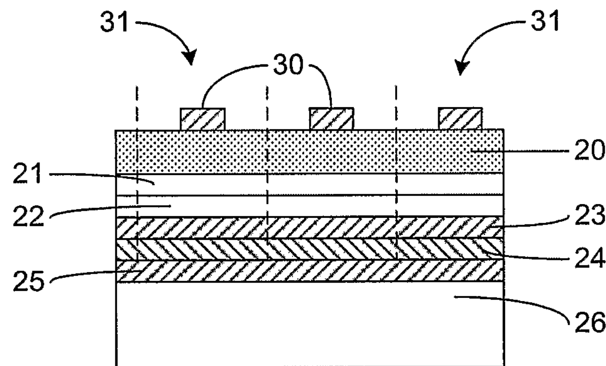


Fig. 8

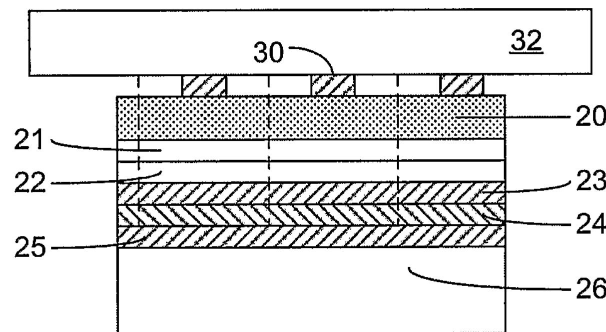


Fig. 9

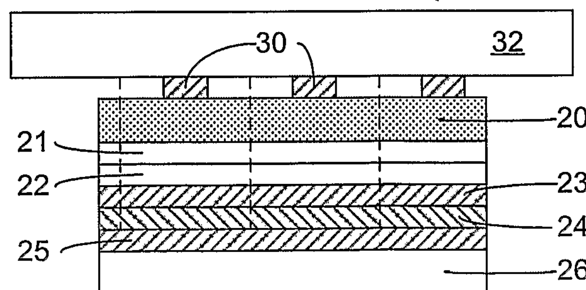


Fig. 10

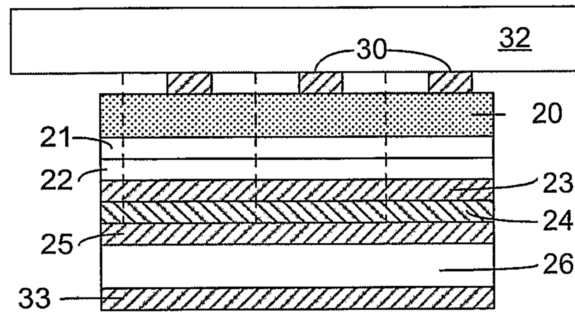


Fig. 11

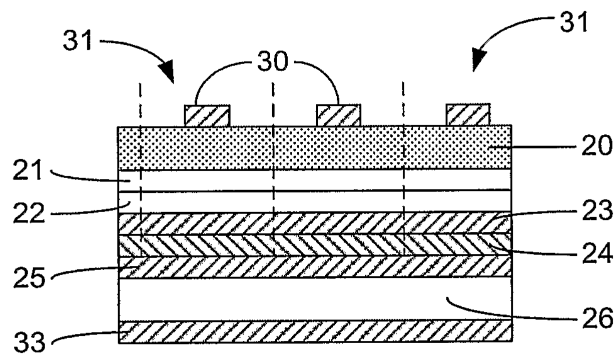


Fig. 12

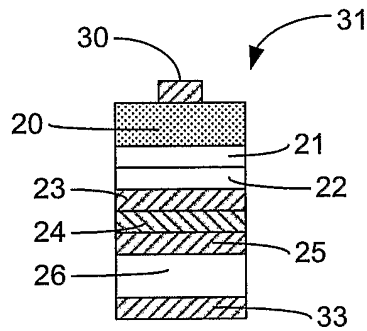


Fig. 13

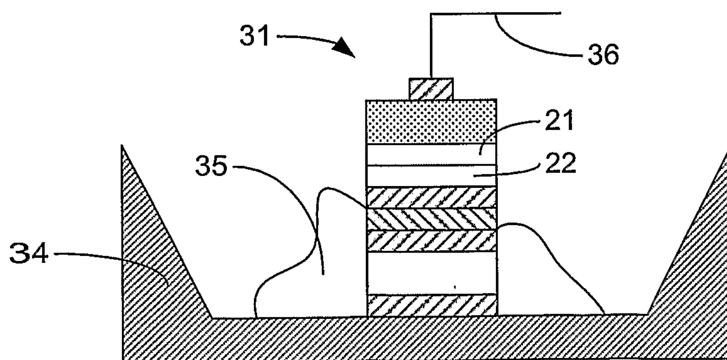


Fig. 14

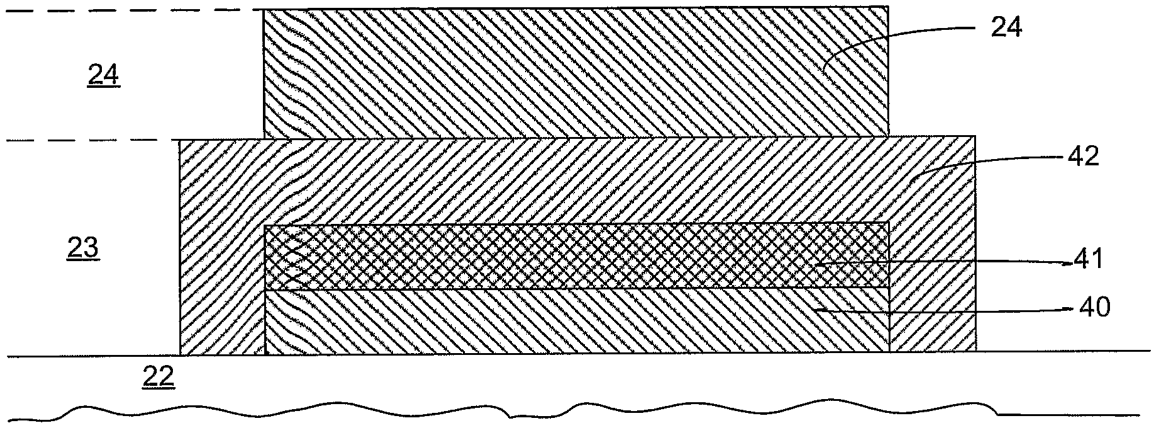
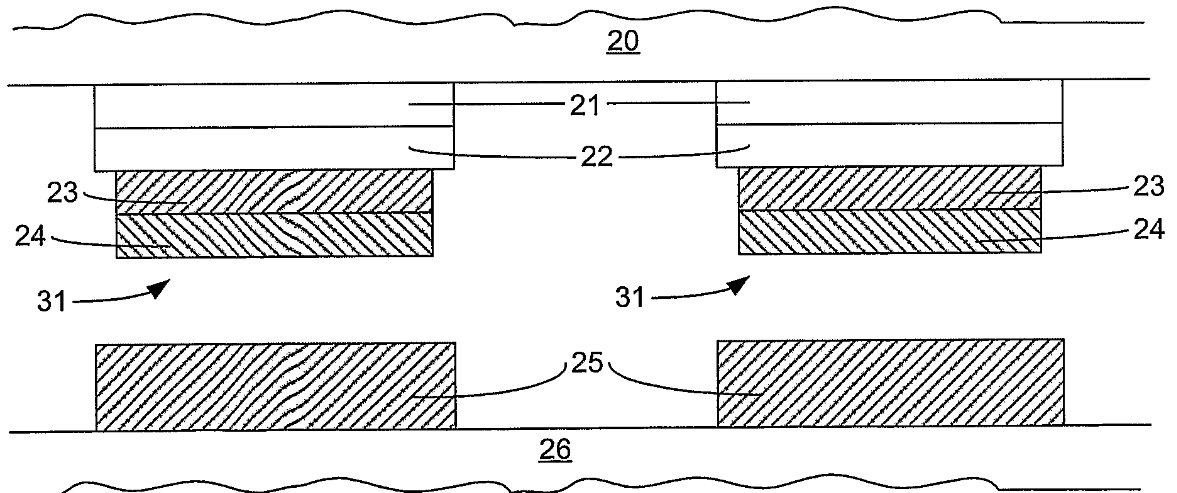


Fig. 15

Fig. 16



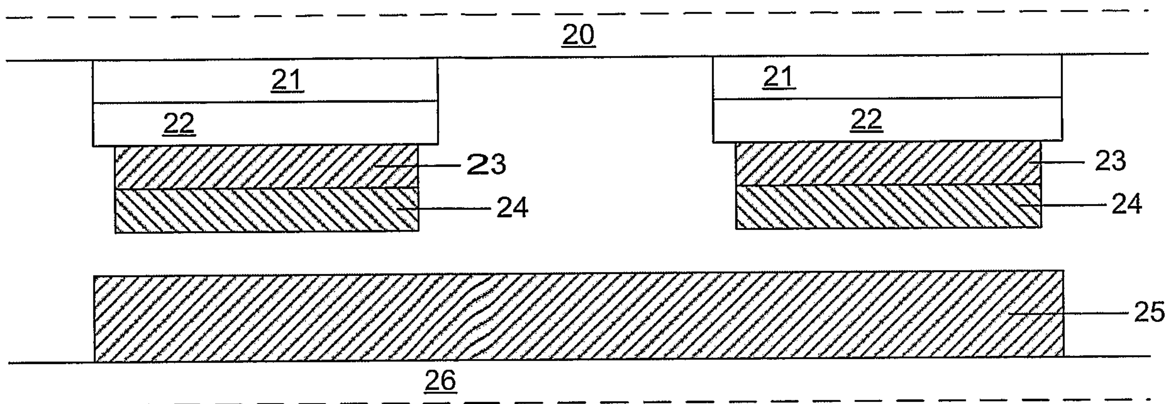


Fig. 17

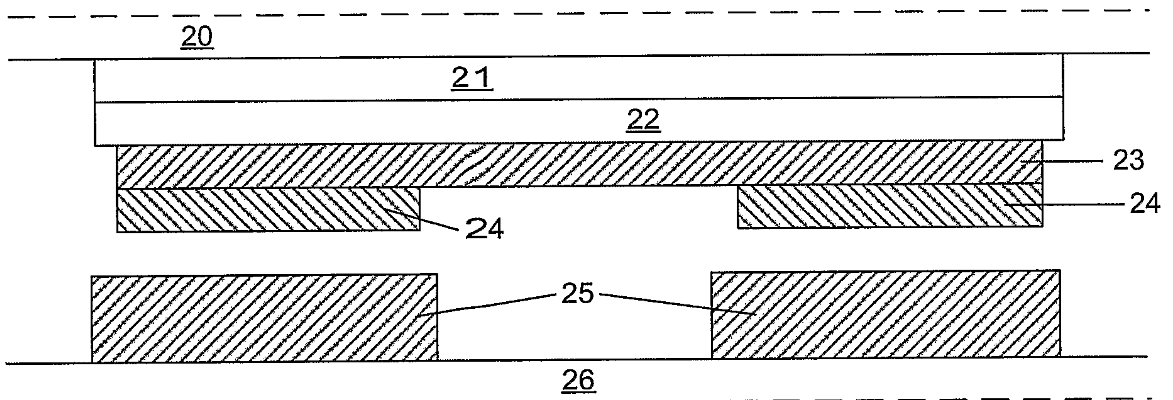
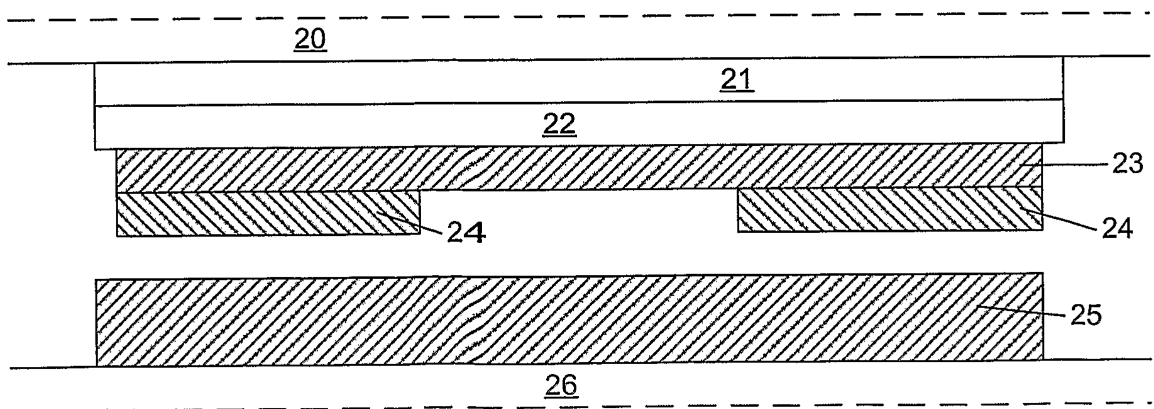


Fig. 18

Fig. 19



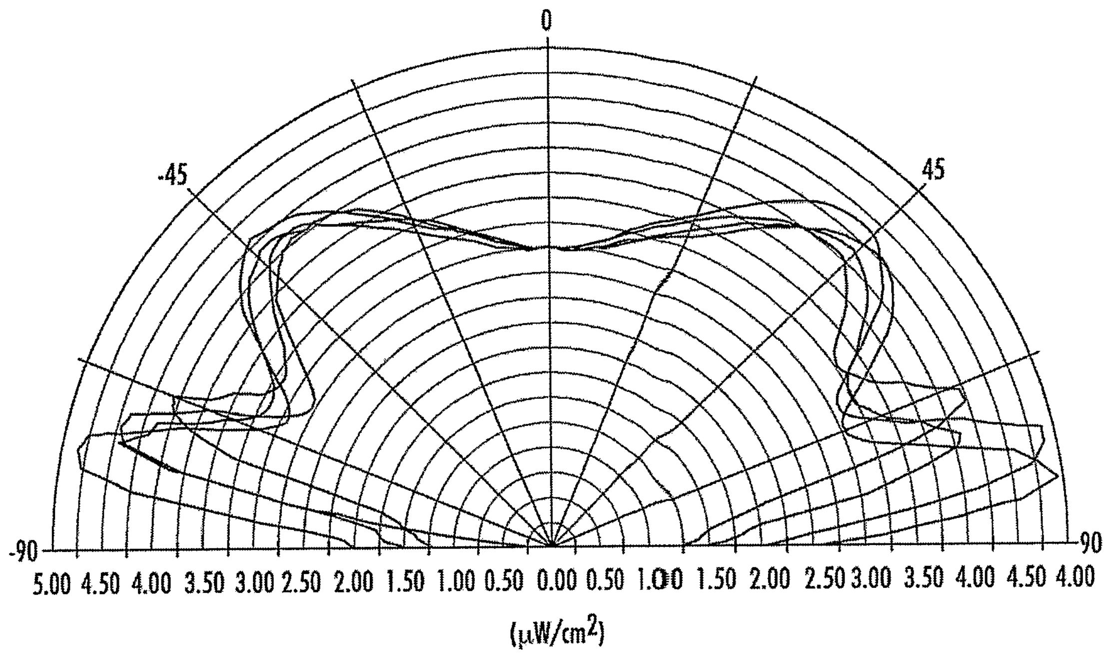


Fig. 20

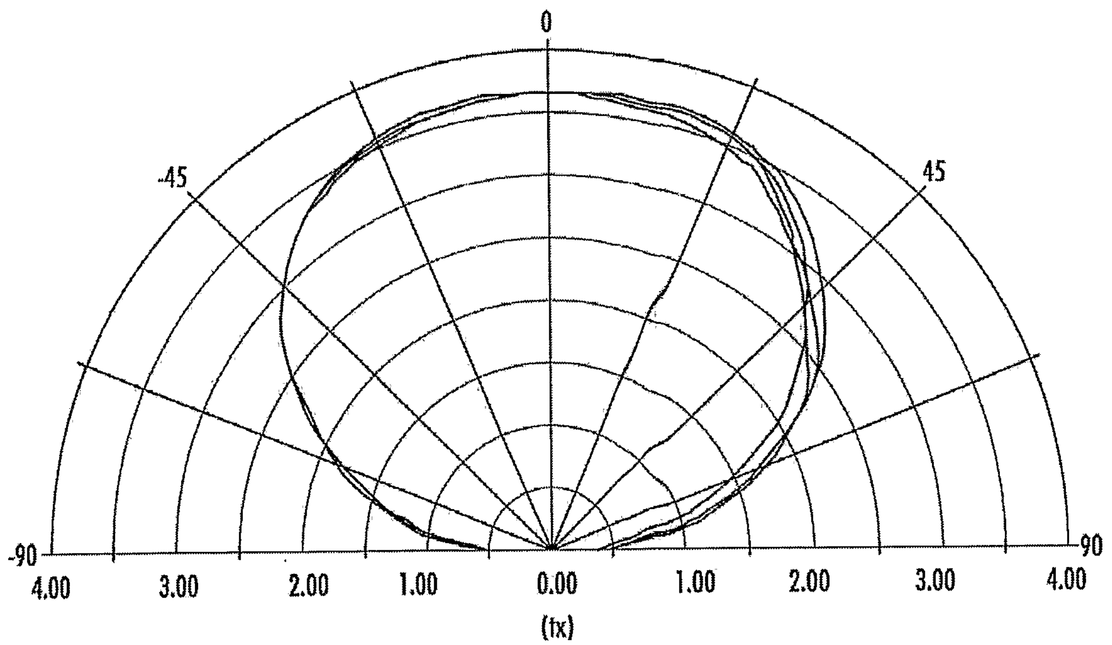


Fig. 21

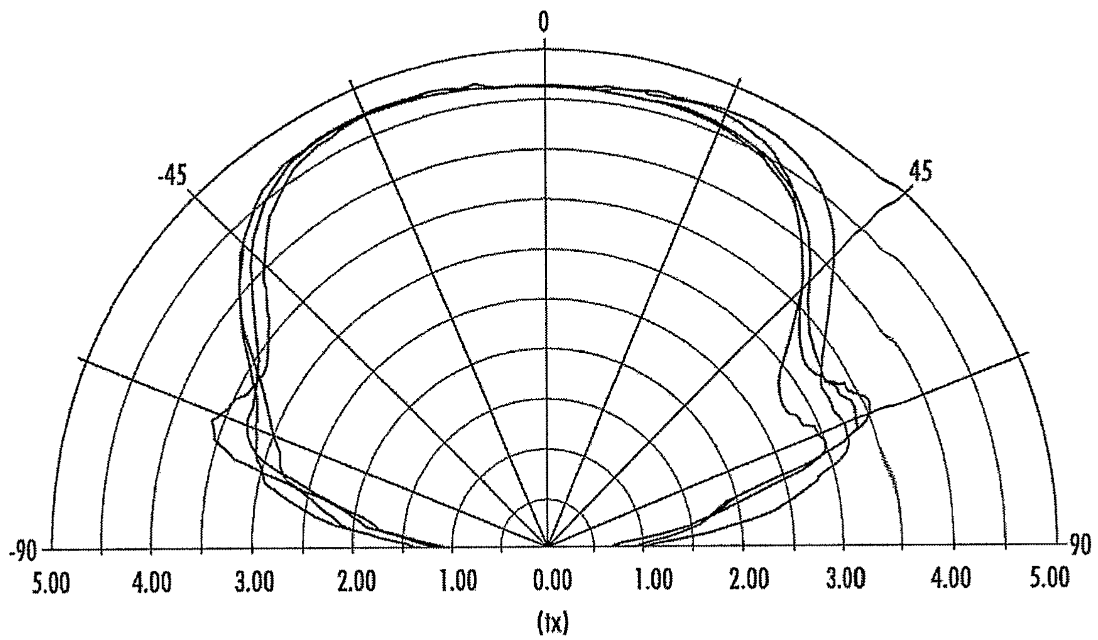


Fig. 22

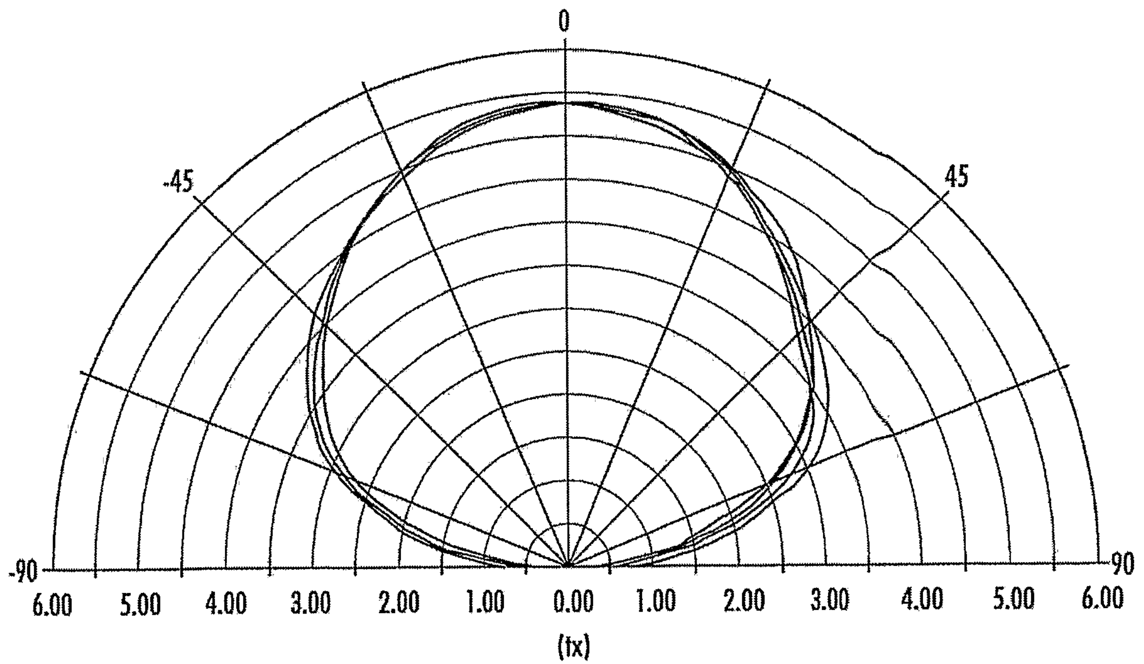


Fig. 23

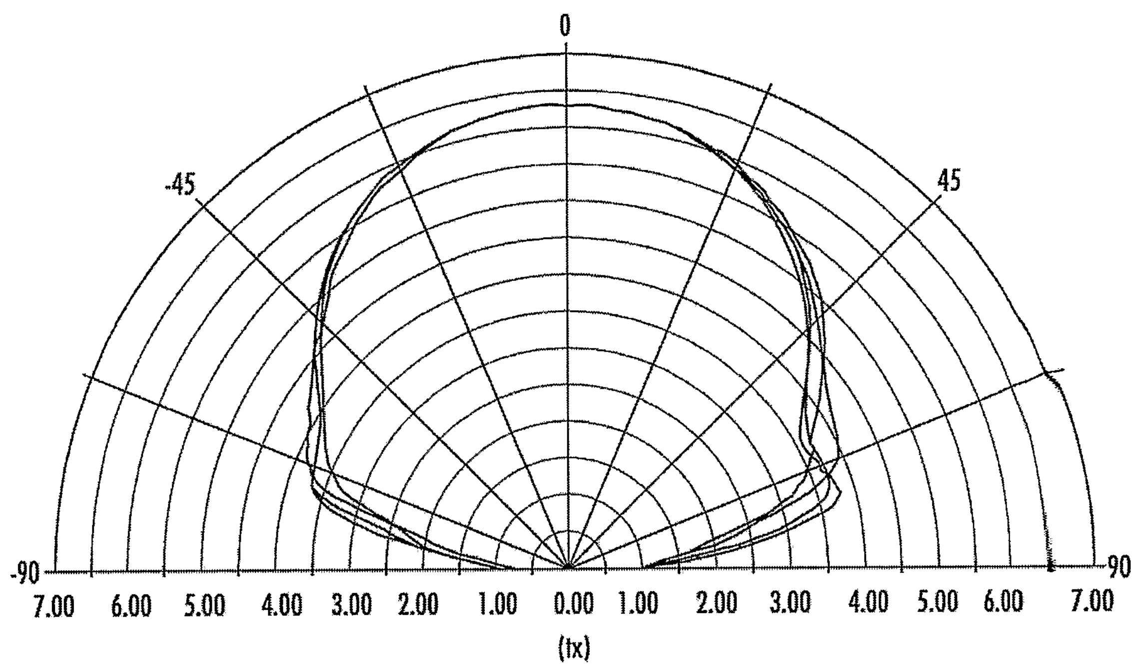


Fig. 24

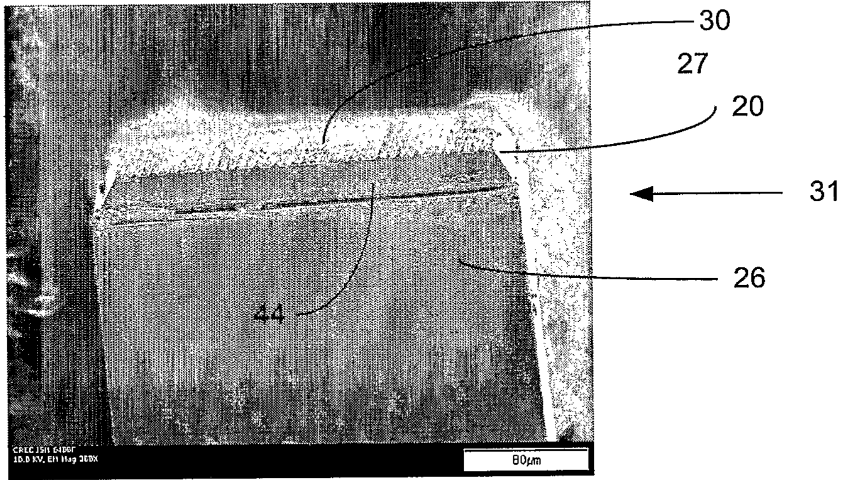


Fig. 25

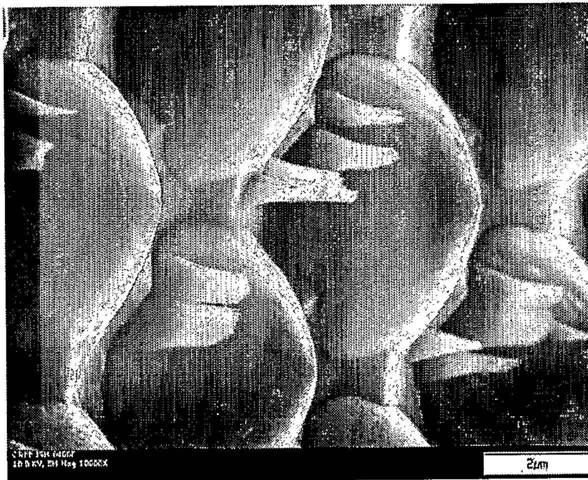


Fig. 26

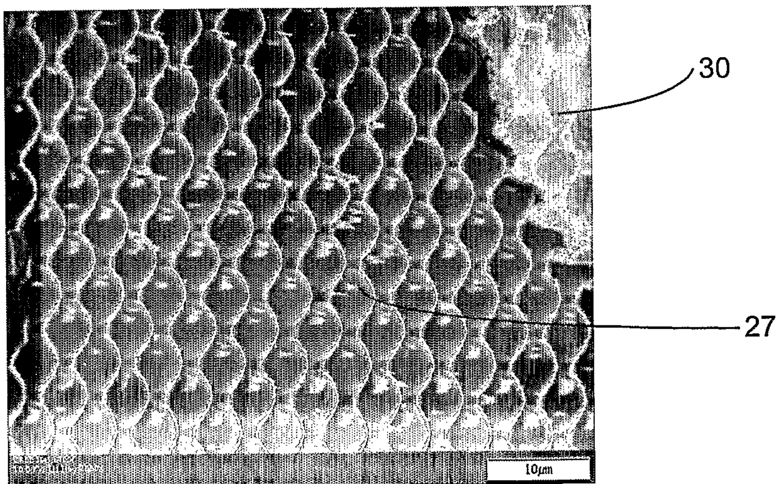


Fig. 27

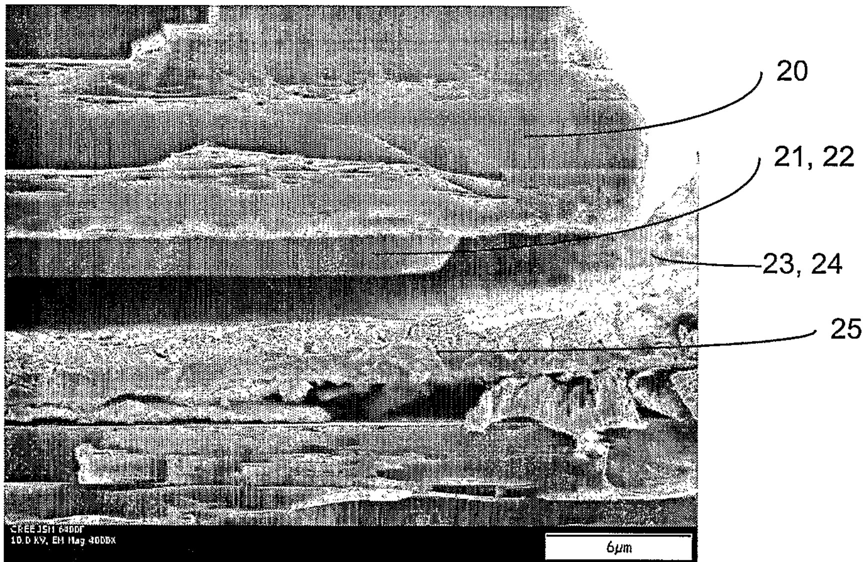


Fig. 28

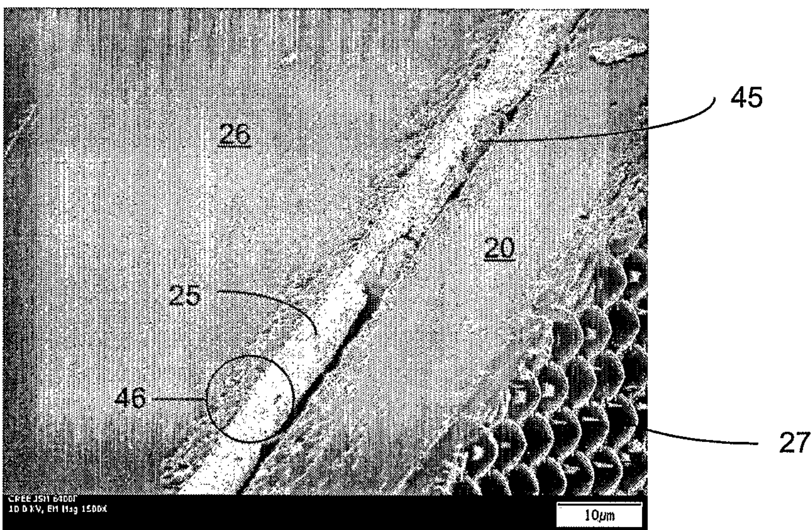


Fig. 29

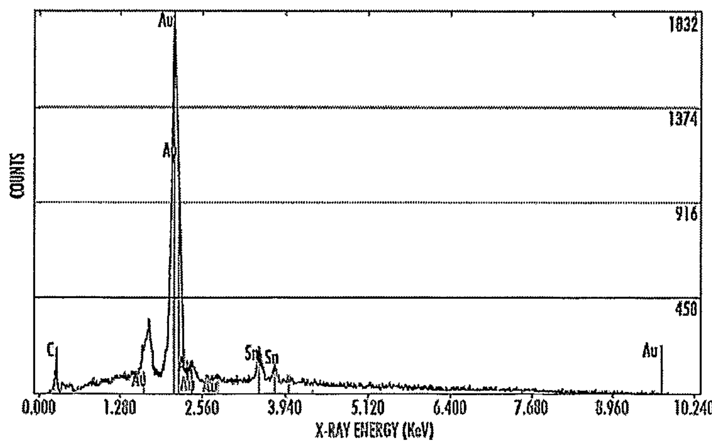


Fig. 30

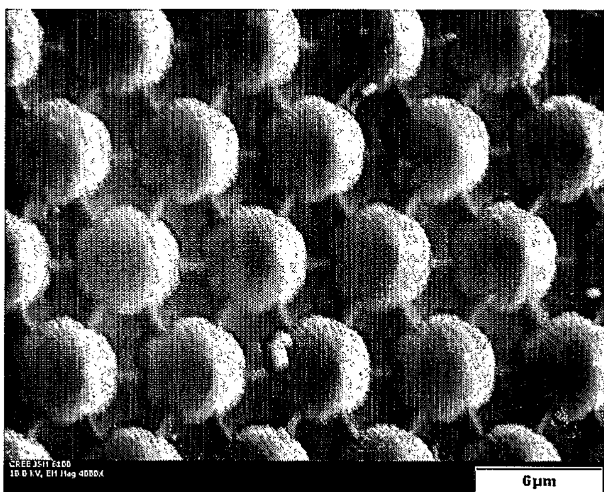


Fig. 31

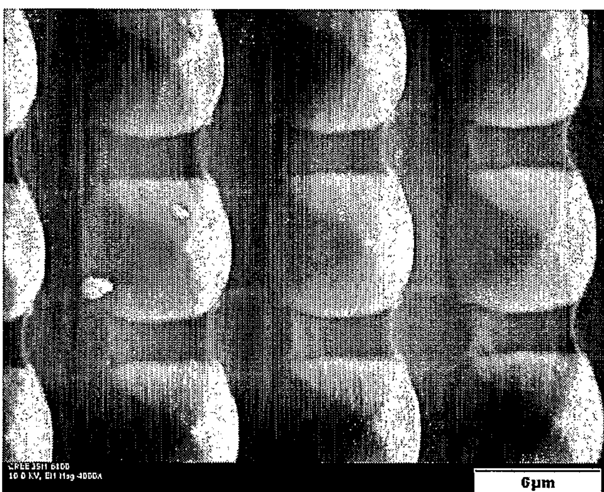


Fig. 32

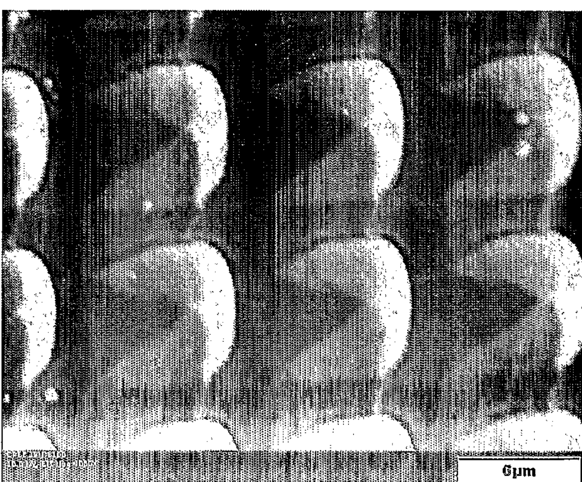


Fig. 33

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/032896

A. CLASSIFICATION OF SUBJECT MATTER
H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 100 104 A (HAERLE ET AL) 8 August 2000 (2000-08-08) figure 5	1-16, 38-44 17-37
Y	US 2003/197170 A1 (BADER STEFAN ET AL) 23 October 2003 (2003-10-23) the whole document	17-37
A	US 2002/068373 A1 (LO YU-HWA ET AL) 6 June 2002 (2002-06-06) paragraph ‘0041!	1-44
A	US 2004/033638 A1 (BADER STEFAN ET AL) 19 February 2004 (2004-02-19) the whole document	17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 January 2006	02/02/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Werner, A

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/135158 A1 (HON SCHANG-JING) 15 July 2004 (2004-07-15) abstract	
A	US 2003/015721 A1 (SLATER, DAVID B ET AL) 23 January 2003 (2003-01-23) cited in the application the whole document	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2005/032896

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: claims 1-16, 27-44

   SiC-based LED structure and related method with a "plurality of light emitting diode precursors"

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2. claims: 17-26

   Method of fabricating a LED structure with a SiC substrate and sub-mounting structure whereby a portion of the SiC substrate is removed.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/032896

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