The band process described herein exhibits high luminous efficiency and is capable of achieving highly efficient optical detection. The described processes can greatly enhance any application that uses functional substrates and can benefit from a high quality circuit layer, including but not limited to display technologies, light detection, MEMS, chemical sensors, and piezoelectric systems.

**Abstract:** This document discusses, among other things, a process for combining compound semiconductor or other direct band gap substrates with thin film circuitry, which can have an indirect band gap. In one example, an active matrix LED array that exhibits high luminous capabilities can be realized with the describe processes. In another example, a highly efficient optical detector is achievable through the combination described. The described structure can greatly enhance any application that uses functional substrates and can benefit from a high quality circuit layer, including but not limited to display technologies, light detection, MEMS, chemical sensors, and piezoelectric systems.
DIRECT BANDGAP SUBSTRATE WITH SILICON THIN FILM CIRCUITRY

CLAIM OF PRIORITY

This patent application claims the benefit of priority, under 35 U.S.C. Section 119(e), to Kymissis U.S. Provisional Patent Application Serial Number 60/964,935, entitled "ACTIVE MATRIX LED LIGHT ENGINE," filed on August 16, 2007 (Attorney Docket No. 2413.068PRV).

TECHNICAL FIELD

This document pertains generally to semiconductor technology, and more particularly, but not by way of limitation, to a substantially direct band gap substrate combined with thin film circuitry.

BACKGROUND

A substantially direct energy band gap material can provide more efficient light emission and absorption than indirect gap materials, such as silicon. In an example, a substantially direct energy band gap material can include a compound semiconductor material. A compound semiconductor includes semiconductor elements drawn from different groups of the periodic table of elements, e.g., Groups II, III, V, and VI. Compound semiconductors can provide desired capabilities of a more substantially direct energy band gap than non-compound semiconductors, which have more indirect energy band gap properties.

A thin film transistor can include a field effect transistor that can be made by forming a thin film of a semiconductor active layer, a dielectric layer, and conductive contacts upon a supporting substrate. The thin film semiconductor layer can be silicon-based, and can include amorphous silicon, microcrystalline silicon, or annealed polycrystalline silicon. In addition, thin film devices can be made using an organic material or an amorphous film of a metal oxide with semiconducting behavior, e.g., ZnO or its alloys.
OVERVIEW

This document discusses, among other things, a process for combining compound semiconductor or other direct band gap substrates with thin film circuitry, which can have an indirect band gap. In one example, an active matrix LED array that exhibits high luminous capabilities can be realized with the described processes. In another example, a highly efficient optical detector is achievable through the combination described. The described structure can greatly enhance any application that uses functional substrates and can benefit from a high quality circuit layer, including but not limited to display technologies, light detection, MEMS, chemical sensors, and piezoelectric system.

This overview is intended to provide an overview of subject matter of the present patent application. It is not intended to provide an exclusive or exhaustive explanation of the invention. The detailed description is included to provide further information about the present patent application.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, which are not necessarily drawn to scale, like numerals may describe similar components in different views. Like numerals having different letter suffixes may represent different instances of similar components. The drawings illustrate generally, by way of example, but not by way of limitation, various embodiments discussed in the present document.

FIG. 1 illustrates an example of a GaAs/InAlP compound semiconductor.
FIG. 2 illustrates an example of components used to create an LCD device using thin film circuitry.
FIG. 3 illustrates an example of a sequential lateral solidification (SLS) technique.
FIG. 4 illustrates an example of a difference between a regular SLS structure and a "2-shot" SLS structure.
FIG. 5 illustrates an example of a process flow for combining a compound semiconductor with a thin film transistor.
FIG. 6 illustrates an example of a light engine.
FIG. 7 illustrates an example of a cross-sectional view of an example of various stages in creating an example of an active matrix LED device.

FIG. 8 illustrates an example of a process flow for creating an active matrix LED device.

FIG. 9 is an example of a schematic diagram of an active matrix LED device.

FIG. 10 is an example of a schematic diagram of an example of an advanced active matrix LED device.

FIG. 11 is an example of a schematic diagram of an example of an advanced active matrix LED device.

DETAILED DESCRIPTION

In semiconductor processing, processing substrates with substantially direct band gaps (e.g., GaAs, etc.) presents different challenges and advantages than silicon processing. A substantially direct energy gap can provide for more efficient light emission and absorption than a silicon semiconductor. However, silicon semiconductor processing provides well-established techniques that are useful for fabricating complex integrated circuits for many different functions. Bulk silicon semiconductor processing techniques can be difficult to combine with processing techniques for substrates with direct band gaps for a number of reasons, including thermal budget and heteroepitaxy limitations.

However, the present inventors have recognized that another useful process permits fabricating circuitry using a thin film of silicon. More particularly, sequential lateral solidification (SLS) permits fabricating high-quality circuitry on virtually any substrate, including a glass sheet substrate or an organic substrate. The SLS process provides silicon re-crystallization so that no crystallographic templating on the substrate is required, the thermal load on the substrate is minimal, and the resulting re-crystallized crystal quality can be higher than non-SLS techniques and can produce higher quality transistors.

The present inventors have recognized, among other things, that marrying a substantially direct band gap substrate, such as a compound semiconductor, with
SLS thin film transistor technology can be used to make highly efficient devices, such as, for example, an active matrix LED array. Other approaches of integrating a direct band gap substrate and silicon circuitry to form a heterogeneous device can be difficult. Such other approaches of combining a direct band gap substrate and silicon can include shape self-assembly, wafer bonding, or magnetic retention. However, such techniques can suffer from impediments such as poor bonding, due to limited thermal budgets or mismatched coefficients of thermal expansion between the two different types of materials. Substrates with substantially direct band gaps, such as compound semiconductors, can be very sensitive to thermal (heat-intensive) semiconductor processing techniques. Another challenge in obtaining a hybrid silicon/non-silicon device is in locally interconnecting the non-silicon substrate with the silicon device to which it abuts.

As stated, a substrate with a direct band gap can provide unique properties. In an example, as shown in FIG. 1, an inorganic substrate with this property can be used as an inorganic light emitting diode (LED) 100. A substrate can be formed as a GaAs/InAlP wafer. To create this wafer, n+ GaAs cathode 101 cathode can be combined with an InAlP anode 102 to form an LED structure.

An inorganic LED can provide luminous efficiency that far surpasses many other light sources. The internal quantum efficiency of a compound semiconductor LED can be close to 100%. A range of output wavelengths from infrared (IR) to ultraviolet (UV) of saturated colors can also be achievable. In addition, the lifetime of an inorganic LED device can be in the tens of thousands of hours.

The present inventors have recognized that thin film transistor technology allows a field effect transistor to be made by depositing or otherwise forming a thin film of a semiconductor active layer over a supporting substrate. Unlike a bulk silicon semiconductor wafer process, a thin film transistor can be deposited or otherwise formed on more diverse types of substrates. Thin film circuitry can be placed on a glass substrate, such as shown in the example of FIG. 2, such as for use in an LCD display 200. The thin film circuitry that is used for the LCD process 201 can be deposited on top of a glass substrate 202.
In an example, the thin film Si can be manipulated or tailored, such as to exploit its semiconductor properties. The thin-film semiconductor layer can be converted into amorphous silicon, microcrystalline silicon, or it can be laser annealed into polysilicon. A technique that can be used to laser anneal thin film silicon is sequential lateral solidification (SLS).

SLS can include an extremely flexible thin-film pulsed-laser crystallization technique (where such "crystallization" can refer to or include "recrystallization"). SLS can be used to create a variety of polycrystalline microstructures such as by using different thin-film materials, different substrates, or different pulsed-laser sources. SLS can use a narrow energy-density window in laser crystallization of the Si thin film. The laser melts the film and forms a long "super-lateral growth" (SLG) of low-defect-density crystals.

SLG can be controlled, such as by inducing localized complete melting of the film. SLG can also include iterative translation and re-irradiation, which can lead to even more accurate control of the microstructure of the material.

FIG. 3 describes an example of SLS. At 300, a selected region of thin film silicon is melted, transforming the selected region into liquid 301. At 310, the liquid 301 re-crystallizes into lateral growth regions 312. At 320, this eventually results in a selective polysilicon region 321. Such techniques can be iteratively applied, such as to obtain translation of the liquid region 301 at 330, further lateral growth at 340, and ultimately the creation of elongated polysilicon grains 351, such as at 350. The formation of elongated polysilicon grains 351 allows the resulting material to be used for a high-mobility and a low-threshold-voltage transistor device.

This SLS process can be modified into a cheaper, faster, and more reliable "2-shot" SLS process. FIG. 4 shows an example of a difference between the two processes. The "2-shot" process, such as shown in FIG. 4, can allow for more elongated polysilicon grains, and therefore a transistor with high-mobility and a low-threshold. Either SLS technique can be used to combine a direct band gap substrate with a thin film silicon device having an indirect band gap. The present inventors have recognized that the above challenges in creating a silicon/non-silicon
heterogeneous structure can be overcome, such as by using such SLS techniques. Such SLS techniques can overcome these challenges, such as by (1) limiting the thermal budget used to create active circuitry and (2) using the compound semiconductor as a substrate and building circuitry and interconnects using the same process as that used for the compound semiconductor substrate. The thermal budget can be limited by narrowing the laser pulse duration or its size in the SLS process. By using the compound semiconductor as a substrate and directly attaching an interconnect onto the compound semiconductor, the challenges associated with micromachining small devices can be avoided.

FIG. 5 shows an example of a process flow for a silicon/non-silicon heterogenous structure. At 500, a wafer or other substrate can be obtained or manufactured. The wafer or other substrate can have a substantially direct energy band gap, therefore allowing efficient light emission or absorption. Some examples of suitable substrate materials can include, by way of example, but not by way of limitation, one or more of GaAs, AlGaAs, AlGaP, AlGaInP, GaAsP, GaP, GaN, AlGaN, InGaN, SiC, ZnSe, C, AlN, AlGaN, AlGaInN, InAlP, InSb, InAlSb, HgCdTe, or a combination or alloy thereof.

At 510, an insulating layer can be formed on the first side of the substrate. Some examples of suitable insulating layer materials can include, by way of example, but not by way of limitation, one or more of parylene, polymide, SiOx, SiNx, SiNOx, DLC, HfO, Al2O3, TaOx, RuOx, another insulating metal oxide, nitride, fluoride, chloride, polymer, or fluorocarbon material, or one or more combinations thereof. This insulating layer can serve as one or more of a thermal buffer, electrical insulator, passivation layer, or as an etch stop such as for a wet-etching process. At 520, a thin film can be formed on the device. At 530, the thin film can be doped, such as using ion implantation or by depositing one or more precursors onto the thin film. At 540, SLS can be performed on the thin film layer. The SLS can also activate the dopants into the re-crystallized thin film. The resulting structure can provide a doped source/drain region created by the merger of the dopants and the thin film. At 550, an electrode can be formed on the previously created source/drain region. At 560, a gate dielectric can be deposited or otherwise
formed on the resulting structure. At 570, a FET or other transistor gate can be
formed. At 580, a passivation layer can be formed on top of the resulting thin film
transistor device, such as to protect the resulting thin film transistor device. At 590,
conductive vias and other interconnection structures can be formed, such as to
electrically interconnect thin film transistor devices or to connect the thin film
transistor devices to external circuitry.

In a specific example, such a process can be used to create an active matrix
LED array, such as for use with a projection display. Projection displays can
provide a projected image that can be significantly larger than the electronics that
generate it, such as illustrated in the example of FIG. 6. In the example shown in
FIG. 6, a light engine 601 can be created, such as by using a thin film transistor
device for providing a current for directly driving an efficient inorganic LED device
in the direct band gap substrate. In this way, an active matrix array can be provided,
such as to project a light onto a screen 602. Because an inorganic LED formed from
a direct band gap substrate can provide a highly efficient luminous source, in an
illustrative example, a potential projection of a 56 inch diagonal image can be
obtained with an active matrix LED array integrated circuit chip that measures 36
millimeters diagonally.

FIG. 7 shows an example of a cross-sectional view of an example of an
active matrix LED device. FIG. 8. shows an example of a corresponding process
for creating such an active matrix LED device. At 800, a direct band gap substrate,
such as a compound semiconductor substrate, can be obtained or manufactured. An
example of a suitable material for the compound semiconductor is GaAs/InAlP. A
GaAs/InAlP compound semiconductor substrate can be manufactured, in an
example, by using a n+ GaAs 701 region of a starting substrate, and then depositing
an InAlP 702 onto the n+ GaAs region 701. The heterostructure of GaAs/InAlP can
emit light, such as at around the wavelength of 630 nanometers.

In addition, one or more mesas can be formed, such as to reduce or eliminate
current spreading from the addressed pixel to other neighboring pixels. The mesas
can be formed by etching the top layers of the LED stack down to an insulating
layer underneath. The formation of mesas allows for the electrical isolation of the
addressed pixel from its neighbors and prevents inadvertent biasing of unintended neighboring devices when reverse biasing is insufficient to turn unaddressed units off.

At 810, an insulating layer 712 can be formed upon the compound semiconductor substrate 711. In the example, the insulating layer 712 can include a layer thickness ranging from 50 nanometers to 10 micrometers of a chemical vapor deposition (CVD) deposited polymer material, such as parylene-C 713. Parylene-C can be vapor deposited at room temperature, and can be resistant to many wet and plasma etching processes. The parylene-C layer 713 can serve as an electrical insulator, passivation, or as an etch stop for an etching processes. In addition to parylene-C, the insulating layer 712 can include a silicon dioxide (SiO$_2$) layer 714, which can be deposited or otherwise formed such as to add extra thermal buffering. Thermal buffering can help protect the compound semiconductor 711 from heat, such as heat generated during subsequent SLS.

At 820, a thin film 721 of silicon (Si) can then be deposited or otherwise formed on the structure 710, such as by sputtering. The thin film Si layer 721 can be chosen for its compatibility with SLS. The thickness of the thin film Si layer 721 and the SiO$_2$ layer 722 can be chosen to protect the parylene-C layer 723 and compound semiconductor layer 724, such as from stresses caused during SLS laser crystallization. In an example, the thin film Si layer 721 can be a thickness within the range of 50 nanometers to 10 micrometers, and the SiO$_2$ layer 722 can be a thickness within the range of 50 nanometers to 10 micrometers. These thicknesses can be adjusted, such as to enhance the device performance or the overlayer protection.

At 830, active regions of the thin film Si layer 732 can be selectively doped, such as to provide conductively doped active regions 731 of the device. In an example, the active region doping can use ion implantation, such as by using a photoresist layer as a mask. Another technique can apply one or more solid-phase dopant precursors, such as by using an additional layer of lithographically patterned CVD deposited silicon dioxide or silicon nitride as a doping mask. In either case, after doping, the doping mask can be removed, leaving a selectively doped active
region. Some examples of other techniques of doping can include, by way of example, but not by way of limitation, one or more of engineering the source thin-film material, ion implantation, solid source doping, vapor phase doping, plasma doping, laser doping, printing, or one or more combinations thereof.

At 840, SLS laser annealing can be performed on the resulting structure 730. This creates an SLS crystallized thin film layer of silicon 741 with doped source/drain regions 742. The dopants can be activated and driven into the thin film Si layer 741, such as through the SLS laser annealing process. Examples of the SLS can include one or more of one-shot SLS, two-shot SLS, line SLS, sequential SLS, dot SLS, or the like, or one or more combinations or iterations thereof.

At 850, the resulting layers can be selectively etched down, such as to define the structures to create an active matrix LED transistor. In the example of the structure 750, a region can be mask-protected for the active matrix transistor 751 and a surrounding region can be etched down to the passivation layer for the LED 752. Electrodes 753 can be deposited, or otherwise formed, and patterned, such as to connect to the doped regions 754 of the thin film semiconductor. In an example, Al/Mo can be used as a source/drain contact material for the electrodes 753.

At 860, a gate dielectric such as silicon dioxide 761 can be deposited onto or otherwise formed upon the structure 750. In an example, a thickness of 100 nm can be used for the silicon dioxide layer 761. The particular thickness can be adjusted, such as based on the process or other experimental data.

At 870, a gate contact 771 can be deposited onto or otherwise formed upon the structure 760. Various materials can be used for the gate contact 771. In an example the gate contact 771 can include a 100 nm chrome layer that can be deposited and patterned or otherwise fabricated such as to form a gate having a desired size.

At 880, an additional passivation layer 781 can be formed upon the structure 770 resulting in the structure 780. In an example, the passivation layer 781 can be formed with parylene-C and can be 200 nm thick. The passivation layer 781 can cover both the transistor region 782 and the LED region 783.
At 890, the structure 780 can be patterned and etched, which can result in the structure 790. The silicon dioxide layer 784 and the passivation layer 781 can be selectively etched over the LED region 791 of the structure in 790. This can expose the compound semiconductor 793 over the LED region 791. Vias can be etched into the transistor region 792 of the structure 790. An anode layer, such as Indium Tin Oxide (e.g., ITO 90:10) 794 can be deposited or otherwise formed over the LED region 791, thereby forming an LED device 791. Indium Tin Oxide can be a good material for the anode of the LED 791 because it is a transparent conducting oxide. Therefore, it can form a transparent window (e.g., for light emission or detection) and it can be connected to the transistor region 792 using a conductive interconnect. Some other examples of suitable substantially transparent but electrically conducting materials, such as for use in providing such a "window," can include, by way of example, but not by way of limitation, one or more of: a doped metal oxide (e.g., ZnO, ZnAlO, SnO, CuO, or the like), a doped III-V compound, a doped II-VI compound, a doped group IV material, a thin noble metal, subwavelength stripes of metal conductors, carbon nanotube composites, or one or more alloys or combinations thereof.

FIG. 9 is a circuit schematic illustrating how the resulting structure 790 can serve as a highly effective active matrix LED. In the example of FIG. 9, a row select 901 can control the gate of the thin film Si transistor 903. A column bias 902 can be connected to the drain of the thin film Si transistor 903, thereby driving the LED device 904. In an array, if the row select 901 is asserted, and the column bias 902 is charged, the LED device 904 becomes electroluminescent.

In an illustrative example of the active matrix LED device described above, the LED can be 200 x 200 μm², and the transistor width and length can be 200 x 10 μm², respectively. In an illustrative conceptual example, the saturation current of the NMOS transistor, with a mobility of 300 cm²/V, and a gate drive voltage of \( V_{gs} - V_T = 5 \) V, can be 3 mA (delivering approximately 7.5A/cm² to the LED). In an illustrative conceptual example, for a GaAs/InAlP device, a current of 3 milliamps can be adequate to drive a 200 x 200 μm² LED at 14 millicandela in the emissive area. This can correspond to a brightness of 350 kilocandela per meter squared at
the source. A typical display can be projected at 100 candela per meter squared. Therefore, a device as described, assuming a loss factor of 2 due to the optics and screen, can provide a magnification on the order of 1750. With this magnification, a 1024x758 light engine with this pixel size (200 x 200 \(\mu\text{m}^2\) of active area and 300 x 300 \(\mu\text{m}^2\) pixel pitch), at the source can be approximately 30 x 20 mm\(^2\) overall and can project an image on the order of 1200 x 800 mm\(^2\) (approximately 56 inches along the diagonal).

The above example describes an active matrix array comprising single thin film Si transistor LED elements. In other examples, different circuitry can be used to create an advanced active matrix array. In a typical active matrix array, the pixel is active during the row select time, leaving the duty cycle for an \(n\) row display to be \(\frac{1}{n}\). An advanced active matrix array can avoid this by adding extra transistors that allow an LED to be charged for an extended time, increasing the brightness of the light engine.

FIG. 10 shows such an example, in which an extra transistor 1001 can be added to drive the gate 1006 of the transistor 1002 that controls the current driving the LED 1006 from the column bias 1004. When row select 1003 is asserted, a data value 1005 can be latched in, which in turn drives the column bias. Therefore, in this example, a current can still drive the LED even when the applicable row select 1003 is no longer asserted. In a circuit such as this, it can be more difficult to control the drive current on the LED due to the fact that the current/voltage relationship is a square law and depends on the threshold voltage of the device 1002, which may be process-dependent.

FIG. 11 presents an example of another version of an advanced matrix LED array. In the example of FIG. 11, the transistor 1101 is mirrored through transistor 1103. This can offer more controlled LED driving currents. In laying out the thin film Si transistors, to increase transconductance and optical matching, it can be helpful to line up the SLS grains for the transistors used in the current mirror.

The above example emphasizes a monochrome projection unit. However, the technology described herein can also be used for multicolor projection. For example, three color projection can be achieved by combining the light from three
units, such as in a beam splitter configuration. Such a configuration can retain certain features, such as avoiding requiring a color wheel or a color filter, and can provide for a long lifetime. Such a projection unit such can avoid requiring the spatial light modulators associated with typical digital light processors (DLP) micromirror arrays, polycrystalline-Si based LCD panels, or liquid crystal on silicon (LCOS) devices. Therefore, these advantages can lead to a significant enhancement of system and energy efficiency, while reducing the complexity of the optical subsystem, and improving the overall form factor.

Such an architecture can also be combined with a photonic crystal, which can lead to a superior performance of an optical system. Much of the light produced in an LED is wave guided in the material or emitted at angles which are not captured by the projection optics. Photonic crystal over layers can manage the light emission cone and increase the useful light output for the optical system.

The previous examples emphasize how the devices described can exploit the light emitting aspects of a compound semiconductor. In another example, the compound semiconductor can be used as a photodetector, such as that the photodetector replaces the light emitting areas. The photomatrix can be achieved by fabricating thin film semiconductor readout circuitry onto compound semiconductor photodetector structures. As with active matrix LED arrays, this can reduce or avoid many of the issues associated with wafer-bonded devices.

In general, many different hybrid compound/thin film semiconductor structures can be envisioned with the above-described technology. Some illustrative examples of devices that can benefit from the placement of active circuitry on thermally sensitive active substrates include: hybrid silicon logic/high speed or high power compound semiconductor devices, MEMS systems (e.g., instrumenting an accelerometer machined out of a non-silicon material), microfluidic systems (e.g., adding local amplifications to a flow sensor), microreactors (e.g., measuring and regulating temperature in a hydrogen reformer) and piezoelectric systems (e.g., making an active matrix piezoelectric device without de-poling the substrate).
The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as "examples." Such examples can include elements in addition to those shown and described. However, the present inventors also contemplate examples in which only those elements shown and described are provided.

All publications, patents, and patent documents referred to in this document are incorporated by reference herein in their entirety, as though individually incorporated by reference. In the event of inconsistent usages between this document and those documents so incorporated by reference, the usage in the incorporated reference(s) should be considered supplementary to that of this document; for irreconcilable inconsistencies, the usage in this document controls.

In this document, the terms "a" or "an" are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of "at least one" or "one or more." In this document, the term "or" is used to refer to a nonexclusive or, such that "A or B" includes "A but not B," "B but not A," and "A and B," unless otherwise indicated. In the appended claims, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended, that is, a system, device, article, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms "first," "second," and "third," etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.
What is claimed is:

1. A method comprising:
   providing a substrate with a substantially direct band gap for light emission or absorption;
   forming an insulating layer on a first side of the substrate;
   forming a silicon layer on the insulating layer;
   selectively melting and re-crystallizing an active region of the silicon layer;
   forming an electrical contact to the re-crystallized active region in the silicon layer; and
   forming an electrical contact to the substrate.

2. The method of claim 1, comprising forming a window to the substrate, wherein the window is substantially transparent to light at a wavelength emitted by the substantially direct energy gap of the substrate.

3. The method of claim 2, comprising:
   forming a thin film semiconductor device in the active region;
   forming electrodes contacting the thin film semiconductor device;
   forming an insulating layer over the thin film semiconductor device;
   forming vias in the insulating layer over the thin film semiconductor device;
   and
   forming a transparent conductor contact to a light emitting or light absorbing area of the substrate.

4. The method of claim 3, wherein forming a transparent conductor contact comprises using one or more of ITO, ZnO, AZO, GZO, SnO, Au, Pt, Pd, CuO, TiO, RuO, InCdO, Ag, CdO, TiN, or a noble metal.
5. The method of claim 4, wherein forming a transparent conductor contact comprises forming one or more of a subwavelength conductor contact, a carbon nanotube contact, or a semiconductor contact.

6. The method of claim 1, wherein providing a substrate comprises providing a compound semiconductor substrate.

7. The method of claim 6, wherein providing a substrate comprises providing a substrate comprising a mesa.

8. The method of claim 6, wherein providing a compound semiconductor substrate comprises providing a compound semiconductor substrate comprising one or more of GaAs, AlGaAs, AlGaP, AlGaInP, GaAsP, GaP, GaN, AlGaNJnGaN, SiC, ZnSe, AlN, AlGaN, AlGaInN, C, InAlP, InSb, InAlSb, or HgCdTe.

9. The method of claim 1, comprising doping the active region.

10. The method of claim 9, wherein doping the active region comprises ion-implanting a dopant.

11. The method of claim 1, wherein selectively melting and re-crystallizing an active region of the silicon layer comprises performing excimer laser re-crystallization.

12. The method of claim 1, selectively melting and re-crystallizing an active region of the silicon layer comprises performing sequential lateral solidification.

13. The method of claim 12, wherein performing sequential lateral solidification comprises performing at least one of two-shot sequential lateral solidification, line sequential lateral solidification, or dot sequential lateral solidification.
14. The method of claim 1, comprising forming an insulating layer, upon the selectively melted and re-crystallized active region of the silicon layer, the insulating layer comprising at least one of parylene, polyimide, SiOx, SiNx, SiNOx, DLC, HfO, Al2O3, TaOx, RuOx, metal oxide, nitride, fluoride, chloride, polymer, or fluorocarbon.

15. The method of claim 1, comprising:
   forming a gate insulator on the selectively melted and re-crystallized active region of the silicon layer; and
   forming a gate on the gate insulator.

16. The method of claim 1, wherein the forming the contact to the re-crystallized active region in the silicon layer comprises forming a contact to a transistor source or drain region.

17. An apparatus comprising:
   an inorganic light emitting or absorbing device formed in a substrate providing a substantially direct energy gap for light emission or absorption;
   an insulating layer upon the substrate;
   a thin film semiconductor circuit, upon the insulating layer, the semiconductor circuit comprising a selectively melted and re-crystallized semiconductor region; and
   an electrical connection, through the insulator, electrically connecting the inorganic light emitting or absorbing device with the thin film semiconductor circuit.

18. The apparatus of claim 17, wherein the inorganic light emitting or absorbing device comprises an inorganic light emitting diode (LED) formed in the substrate, the LED comprising:
   an n+ GaAs cathode region of the substrate; and
   an InAlP anode region of the substrate.
19. The apparatus of claim 17, wherein the inorganic light emitting or absorbing device comprises an inorganic light emitting diode (LED) formed in the compound semiconductor substrate, and comprising an active matrix array comprising a plurality of the inorganic LEDs.

20. The apparatus of claim 19, comprising a light projector comprising the active matrix array.

21. The apparatus of claim 19, wherein the active matrix array comprises a programmable current source circuit comprising the thin film semiconductor circuit.
**FIG. 1**

100

101
n⁺ GaAS

102
InAlP

**FIG. 2**

200

201
THIN FILM CIRCUITRY

202
GLASS
SLS
300-400 cm$^2$/Vs

"2-SHOT" SLS
200-300 cm$^2$/Vs

FIG. 4A

FIG. 4B
FIG. 5

1. OBTAIN COMPOUND SEMICONDUCTOR
2. FORM INSULATOR LAYER
3. FORM THIN FILM
4. DEPOSIT DOPANTS
5. PERFORM SLS
6. PLACE ELECTRODES
7. PLACE GATE DIELECTRIC
8. FORM GATE
9. FORM PASSIVATION LAYER
10. FORM INTERCONNECTS
FIG. 6
FIG. 8

1. Obtain compound semiconductor
2. Form insulator layer
3. Form thin film Si layer
4. Perform contact doping
5. Perform laser annealing
6. Define transistor region
7. Form SiOx layer
8. Form gate contacts
9. Encapsulate device with passivation
10. Pattern and etch, forming the structures required
FIG. 9

FIG. 10

FIG. 11
INTERNATIONAL SEARCH REPORT

International application No
PCT/US 08/09767

A CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/00 (2008.04)
USPC - 136/252
According to International Patent Classification (IPC) or to both national classification and IPC

B FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC 136/252

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC 136/243, 252, 261-263, 264, 244

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PUBWEST(USPT,PGPB,EPAB,IPAB), DialogPRO(Eng stem tags), Google Scholar
Search Terms LED, silicon recrystallization, inorganic LED, re-crystallizing, silicon layer, insulating layer, substrate, direct bandgap LED, compound semiconductor, thin film, thin film circuitry, light emitting, light absorbing

C DOCUMENTS CONSIDERED TO BE RELEVANT

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<tr>
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