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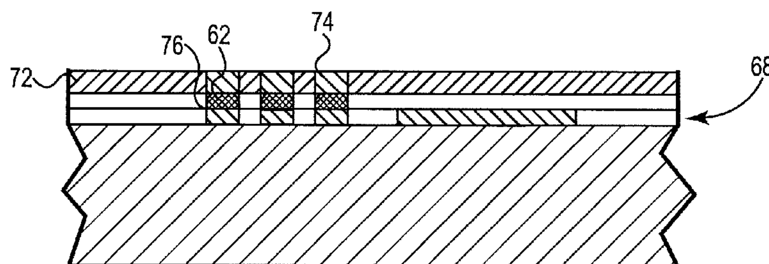

Fig. 5

(57) Abstract: A high performance electrical interconnect adapted to provide an interface between terminals on first and second circuit members. The electrical interconnect includes a first circuitry layer with a first surface and a second surface having a plurality of contact pads adapted to electrically coupled with the terminals on the first circuit member. At least one dielectric layer is printed on the first surface of the first circuitry layer. The dielectric layer includes a plurality recesses. A conductive material is deposited in at least a portion of the recesses to create circuit geometry electrically coupled with the first circuitry layer. A second circuitry layer includes a first surface a plurality of contact pads adapted to electrically couple with the terminals on the second circuit member and a second surface attached to the dielectric layers. The circuit geometry electrically couples the first circuitry layer to the second circuitry layer.

HIGH PERFORMANCE ELECTRICAL CIRCUIT STRUCTURE

Technical Field

[0001] The present disclosure relates to a high performance electrical interconnect for electrically coupling least two circuit members using a unique fabrication technique that merges processes used in the printed circuit and semiconductor packaging industries with the flexibility of additive printing technology.

Background of the Invention

[0002] Traditional printed circuits are often constructed in what is commonly called rigid or flexible formats. The rigid versions are used in nearly every electronic system, where the printed circuit board (PCB) is essentially a laminate of materials and circuits that when built is relatively stiff or rigid and cannot be bent significantly without damage.

[0003] Flexible circuits have become very popular in many applications where the ability to bend the circuit to connect one member of a system to another has some benefit. These flexible circuits are made in a very similar fashion as rigid PCB's, where layers of circuitry and dielectric materials are laminated. The main difference is the material set used for construction. Typical flexible circuits start with a polymer film that is clad, laminated, or deposited with copper. A photolithography image with the desired circuitry geometry is printed onto the copper, and the polymer film is etched to remove the unwanted copper. Flexible circuits are very commonly used in many electronic systems such as notebook computers, medical devices, displays, handheld devices, autos, aircraft and many others.

[0004] Flexible circuits are processed similar to that of rigid PCB's with a series of imaging, masking, drilling, via creation, plating, and trimming steps. The resulting circuit can be bent, without damaging the copper circuitry. Flexible circuits are solderable, and can have devices attached to provide some desired function. The materials used to make flexible circuits can be used in high frequency applications where the material set and design features can often provide better electrical performance than a comparable rigid circuit.

[0005] Flexible circuits are connected to electrical system in a variety of ways. In most cases, a portion of the circuitry is exposed to create a connection point. Once

exposed, the circuitry can be connected to another circuit or component by soldering, conductive adhesive, thermo-sonic welding, pressure or a mechanical connector. In general, the terminals are located on an end of the flexible circuit, where edge traces are exposed or in some cases an area array of terminals are exposed. Often there is some sort of mechanical enhancement at or near the connection to prevent the joints from being disconnected during use or flexure.

[0006] In general, flexible circuits are expensive compared to some rigid PCB products. Flexible circuits also have some limitations regarding layer count or feature registration, and are therefore generally only used for small or elongated applications.

[0007] Rigid PCBs and package substrates experience challenges as the feature sizes and line spacing are reduced to achieve further miniaturization and increased circuit density. The use of laser ablation has become increasingly used to create the via structures for fine line or fine pitch structures. The use of lasers allows localized structure creation, where the processed circuits are plated together to create via connections from one layer to another. As density increases, however, laser processed via structures can experience significant taper, carbon contamination, layer-to-layer shorting during the plating process due to registration issues, and high resistance interconnections that may be prone to result in reliability issues. The challenge of making fine line PCBs often relates to the difficulty in creating very small or blind and buried vias.

Brief Summary of the Invention

[0008] The present disclosure is directed to a high performance electrical interconnect that will enable next generation electrical performance. The present disclosure merges the long-term performance advantages of traditional PCB and semiconductor packaging with the flexibility of additive printing technology. By combining methods used in the PCB fabrication and semiconductor packaging industries, the present disclosure enables fine line high density circuit structures with attractive cost of manufacture.

[0009] The present disclosure includes adding a bulk material to create the vias and other circuit geometry to supplement or replace the traditional circuit production techniques. This approach enables the production of very small low resistance vias to increase density and reduce line and feature pitch of the circuits as well as a host of electrical enhancements that provide an electrical interconnect that may prove to

be superior to the traditional methods. In basic terms, the structure leverages methods used in the semiconductor packaging industry such as stud bumping, ball bonding, flip chip, or pillar termination or discrete particles or spheres of copper, solder or precious metal to act as the via connecting layers within the circuit stack.

[0010] The present high performance electrical interconnect can be treated as a system of its own by incorporating electrical devices or other passive and active function, such as for example, ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. In some embodiments, the electrical devices can be formed using printing technology, adding intelligence to the interconnect assembly.

[0011] The present high performance electrical interconnect can be produced digitally, without tooling or costly artwork. The high performance electrical interconnect can be produced as a “Green” product, with dramatic reductions in environmental issues related to the production of conventional flexible circuits.

[0012] The vias and associated circuit geometry can be printed in a variety of shapes and sizes, depending on the terminal structure on the circuit members. The contact members and vias can be positioned at a variety of locations, heights, or spacing to match the parameters of existing connections.

[0013] The use of additive printing processes permits the material set in a given layer to vary. Traditional PCB and flex circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0014] One embodiment is directed to a high performance electrical interconnect adapted to provide an interface between terminals on first and second circuit members. The electrical interconnect includes a first circuitry layer with a first surface and a second surface having a plurality of contact pads adapted to

electrically coupled with the terminals on the first circuit member. At least one dielectric layer is printed on the first surface of the first circuitry layer. The dielectric layer includes a plurality recesses. A conductive material is deposited in at least a portion of the recesses to form circuit geometry electrically coupled with the first circuitry layer. A second circuitry layer includes a first surface a plurality of contact pads adapted to electrically couple with the terminals on the second circuit member and a second surface attached to the dielectric layers. The circuit geometry electrically couples the first circuitry layer to the second circuitry layer.

[0015] A conductive plating layer is optionally applied on at least a portion of the circuit geometry. The conductive material can be sintered conductive particles or a conductive ink. In one embodiment, a compliant material is located in the dielectric layers to bias the contact pads into engagement with terminals on the first and second circuit members.

[0016] The resulting circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to the recesses. The use of additive printing processes permits conductive material, non-conductive material, and semi-conductive material to be located on a single layer.

[0017] In one embodiment, pre-formed conductive trace materials are located in the recesses. The recesses are than plated to form conductive traces with substantially rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the recesses. The conductive foil is sheared along edges of the recesses. The excess conductive foil not located in the recesses is removed and the recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0018] At least one electrical device is optionally printed on a dielectric layer and electrically coupled to at least a portion of the circuit geometry. Optical quality materials can be printed or deposited in at least a portion of the recesses to form optical circuit geometries. Alternatively, optical fibers can be located in the recesses.

[0019] The present disclosure is also directed to an edge connector on the high performance electrical interconnect. A first portion of the circuit geometry extends beyond the dielectric covering layer. A compliant material is located along a surface of the first portion of the circuit geometry. A second portion of the circuit geometry is located on top of the compliant material.

[0020] The present disclosure is also directed to an electrical interconnect assembly. A housing retains the high performance electrical interconnect. Electrical terminals on a first circuit member are compressively engaged with contact pads located along a first surface of the high performance electrical interconnect. Electrical terminals on a second circuit member are compressively engaged with contact pads located along a second surface of the high performance electrical interconnect. The first and second circuit members are selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

[0021] The present disclosure is also directed to a method of making a high performance electrical interconnect. A first circuitry layer is provided with a first surface and a second surface with a plurality of contact pads adapted to electrically couple with the terminals on a first circuit member. At least one dielectric layer is printed on a first surface of a first circuitry layer. The dielectric layer includes a plurality recesses. A conductive material is printed in at least a portion of the recesses to create circuit geometry electrically coupled with the first circuitry layer. A second surface of a second circuitry layer is attached to the dielectric layer such that the circuit geometry electrically couples the first circuitry layer to the second circuitry layer. The second circuitry layer includes a first surface with a plurality of contact pads adapted to electrically couple with terminals on a second circuit member.

[0022] The conductive material is preferably plated. The conductive material, compliant materials, electrical devices, optical quality material, and the contact members are all preferably printed.

[0023] The present disclosure is also directed to several additive processes that combine the mechanical or structural properties of a polymer material, while adding metal materials in an unconventional fashion, to create electrical paths that are refined to provide electrical performance improvements. By adding or arranging metallic particles, conductive inks, plating, or portions of traditional alloys, the high performance electrical interconnect reduces parasitic electrical effects and impedance mismatch, potentially increasing the current carrying capacity.

[0024] The present high performance electrical interconnect can serve as a platform to add passive and active circuit features to improve electrical performance or internal function and intelligence. For example, electrical features and devices are printed onto the interconnect assembly using, for example, inkjet printing technology

or other printing technologies. The ability to enhance the high performance electrical interconnect, such that it mimics aspects of an IC package and a PCB, allows for reductions in complexity for the IC package and the PCB, while improving the overall performance of the interconnect assembly.

[0025] The printing process permits the fabrication of functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

Brief Description of the Several Views of the Drawing

[0026] Figure 1 is a cross-sectional view of a method of making a high performance electrical interconnects in accordance with an embodiment of the present disclosure.

[0027] Figure 2 illustrates via formation on the high performance electrical interconnect of Figure 1.

[0028] Figure 3 illustrates application to a second circuitry layer to the high performance electrical interconnect of Figure 1.

[0029] Figure 4 illustrates an alternate method of making an electrical interconnect in accordance with an embodiment of the present disclosure.

[0030] Figure 5 illustrates application of a second circuitry layer to the electrical interconnect of Figure 4.

[0031] Figure 6 illustrates another method of making an electrical interconnect in accordance with an embodiment of the present disclosure.

[0032] Figure 7 illustrates via formation on the electrical interconnect of Figure 6.

[0033] Figure 8 illustrates an electrical interconnect with bulk metal deposited in recesses to form the vias in accordance with an embodiment of the present disclosure.

[0034] Figure 9 illustrates an electrical interconnect with recesses filed with conductive particles as the vias in accordance with an embodiment of the present disclosure.

[0035] Figure 10 is a side sectional view of an electrical interconnect in accordance with an embodiment of the present disclosure.

[0036] Figure 11 is a side sectional view of an alternate electrical interconnect with printed compliant material in accordance with an embodiment of the present disclosure.

[0037] Figure 12 illustrates an electrical interconnect with optical features in accordance with an embodiment of the present disclosure.

[0038] Figure 13 illustrates an alternate high performance electrical interconnect with optical features in accordance with an embodiment of the present disclosure.

[0039] Figure 14 illustrates an alternate high performance electrical interconnect with printed vias in accordance with an embodiment of the present disclosure.

[0040] Figure 15 illustrates an alternate high performance electrical interconnect with printed electrical devices in accordance with an embodiment of the present disclosure.

[0041] Figure 16 illustrates an alternate high performance electrical interconnect with printed compliant electrical pads to plug into another connector in accordance with an embodiment of the present disclosure.

[0042] Figure 17 illustrates a method of making a high performance electrical interconnect in accordance with an embodiment of the present disclosure.

[0043] Figures 18 and 19 illustrate other aspects of the method of Figure 17.

[0044] Figure 20 illustrates a high performance electrical interconnect made in accordance with the methods of Figures 17, 18 and 19.

[0045] Figure 21 illustrates a high performance electrical interconnect incorporated into a socket assembly in accordance with an embodiment of the present disclosure.

[0046] Figure 22 through 25 illustrate various alternate high performance electrical interconnects in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0047] A high performance electrical interconnect according to the present disclosure may permit fine contact-to-contact spacing (pitch) on the order of less than 1.0 mm pitch, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. Such fine pitch high performance electrical interconnects are especially useful for communications, wireless, and memory devices.

[0048] The present high performance electrical interconnect can be configured as a low cost, high signal performance interconnect assembly, which has a low profile that is particularly useful for desktop and mobile PC applications. IC devices can be

installed and uninstalled without the need to reflow solder. The solder-free electrical connection of the IC devices is environmentally friendly.

[0049] Figure 1 is a side cross-sectional view of a method of making an electrical interconnect 40 using additive processes in accordance with an embodiment of the present disclosure. The process starts similar to a traditional PCB with a first circuitry layer 52 laminated to a stiffening layer or core 50, such as glass-reinforced epoxy laminate sheets (e.g., FR4). The first circuitry layer 52 can be preformed or can be formed using a fine line imaging step is conducted to etch the copper foil 52 as done with many PCB processes. One or more dielectric layers 54, 56 are printed or placed to the surface 58 such that the first circuitry layer 52 is at least partially encased and isolated. In some embodiments, it may be desirable to use a preformed dielectric film to leave air dielectric gaps between traces. Recesses 60 in the dielectric layer 56 to expose circuitry 52 can be formed by printing, embossing, imprinting, chemical etching with a printed mask, or a variety of other techniques.

[0050] As illustrated in Figure 2, bond points 62, such as for example stud bumps or soldier balls, are added to the exposed circuitry 52 with a traditional bonding machine used in semiconductor packaging applications. Historically, fine gold wire has been used for bonding, with copper seeing increased use in recent years due to the rise in the cost of gold.

[0051] As illustrated in Figure 3, second circuitry layer 64 is applied to the previous construction such that the bond points 62 are deformed to create the interconnecting vias 66 during the lamination operation. The size and shape of the bond points 62 can be tailored to the ideal condition for deformation without piercing the foil 64.

[0052] The second circuitry layer 64 can be pre-etched with the next circuit pattern or can be laminated as a sheet and etched post lamination. In addition, the dielectric material 56 can be left in a tack cure or partial cure state such that a final bond is achieved at final cure. If desired, the bond bumps 62 can be coined planar prior to adding the second circuitry layer 64.

[0053] Figures 4 and 5 illustrate an alternate interconnect 68 with preformed holes or breaks 70 in the first circuitry layer 72 in accordance with an embodiment of the present disclosure. The holes 70 permit the bond points 62 to extend into the openings 70 or reside near the openings 70 so plating solution 74 can enter the mating region to plate the via structure 76 together. The plating 74 is preferably a corrosion resistant metallic material such as nickel, gold, silver, palladium, or multiple

layers thereof. One benefit of the present structure is the material set can be varied layer by layer or altered on a given layer to create some desired performance enhancement not possible with conventional construction.

[0054] Figures 6 and 7 illustrate an alternate construction in which bond points 80 are added to the circuitry 82 while it is planar, without upper dielectric layer 84 to provide clearance for the bonding tool to impact the circuitry 82 without encountering or damaging the dielectric 84. The bond points 80 can be coined en masse to planarize them either before or after the dielectric layer 84. In one embodiment, the dielectric layer 84 is added with the bond points 80 in place and then imaged to expose the vias 86 for subsequent application of the next pre-etched circuit layer to be placed and plated together (see e.g., Figures 2 and 4). The dielectric layer 84 can optionally be filled or doped with a near endless list of enhancement materials to lower dielectric constant, provide thermal management properties, create rigid, flexible, or compliant regions etc.

[0055] Figure 8 illustrates an alternate electrical interconnect 88 with solid bulk metal 90, such as copper or solder spheres, or plated copper, located in recesses 92 in dielectric layer 94 in accordance with an embodiment of the present disclosure. The bulk metal 90 electrically couples with the lower circuitry layer 96 and the upper circuitry layer 98 with slight deformation or material displacement. In one embodiment, the bulk metal 90 is plated, such as by flowing a plating solution through openings 100 in the upper circuitry 98. It may be possible to provide sufficient engagement to interconnect reliably without the need for plating since the bulk metal 90 is encased within dielectric 94 and environmentally sealed. In the event the bulk metal 90 is solder, the circuit layers 96, 98 can be interconnected when the solder 90 is reflowed with the dielectric 94 acting as a natural solder wicking barrier.

[0056] Figure 9 illustrates an alternate electrical interconnect 110 with reservoirs 112 between circuitry layers 114, 116 that can be filled with loose conductive particles 118 in accordance with an embodiment of the present disclosure. The conductive particles 118 can optionally be sintered, coined, tightly compacted, plated, mixed with an adhesive binder, etc. to create via 120. The method of Figure 9 can also be used to create the circuitry itself or supplement the etched foil structures. Use of reservoirs containing conductive particles is disclosed in commonly assigned

PCT/US2010/36313 entitled Resilient Conductive Electrical Interconnect, filed May 27, 2010, which is hereby incorporated by reference.

[0057] Figure 10 illustrates an alternate electrical interconnect 130 with an insulating layer 132 applied to the circuit geometry 134. The nature of the printing process allows for selective application of dielectric layer 132 to leave selected portions 136 of the circuit geometry 134 expose if desired. The resulting high performance electrical interconnect 130 can potentially be considered entirely "green" with limited or no chemistry used to produce beyond the direct write materials.

[0058] The dielectric layers of the present disclosure may be constructed of any of a number of dielectric materials that are currently used to make sockets, semiconductor packaging, and printed circuit boards. Examples may include UV stabilized tetrafunctional epoxy resin systems referred to as Flame Retardant 4 (FR-4); bismaleimide-triazine thermoset epoxy resins referred to as BT-Epoxy or BT Resin; and liquid crystal polymers (LCPs), which are polyester polymers that are extremely unreactive, inert and resistant to fire. Other suitable plastics include phenolics, polyesters, and Ryton® available from Phillips Petroleum Company.

[0059] In one embodiment, one or more of the dielectric materials are designed to provide electrostatic dissipation or to reduce cross-talk between the traces of the circuit geometry. An efficient way to prevent electrostatic discharge ("ESD") is to construct one of the layers from materials that are not too conductive but that will slowly conduct static charges away. These materials preferably have resistivity values in the range of 10^5 to 10^{11} Ohm-meters.

[0060] Figure 11 illustrates an alternate high performance electrical interconnect 150 in accordance with an embodiment of the present disclosure. Dielectric layer 152 includes openings 154 into which compliant material 156 is printed before formation of circuit geometry 158. The compliant printed material 156 improves reliability during flexure of the electrical interconnect 150.

[0061] Figure 12 illustrates an alternate high performance electrical interconnect 160 in accordance with an embodiment of the present disclosure. Optical fibers 162 are located between layers 164, 166 of dielectric material. In one embodiment, optical fibers 162 is positioned over printed compliant layer 168, and dielectric layer 170 is printed over and around the optical fibers 162. A compliant layer 172 is preferably printed above the optical fiber 162 as well. The compliant layers 168, 172 support

the optical fibers 162 during flexure. In another embodiment, the dielectric layer 170 is formed or printed with recesses into which the optical fibers 162 are deposited.

[0062] In another embodiment, optical quality materials 174 are printed during printing of the high performance electrical interconnect 160. The optical quality material 174 and/or the optical fibers 162 comprise optical circuit geometries. The printing process allows for deposition of coatings in-situ that enhance the optical transmission or reduce loss. The precision of the printing process reduces misalignment issues when the optical materials 174 are optically coupled with another optical structure.

[0063] Figure 13 illustrates another embodiment of a present high performance electrical interconnect 180 in accordance with an embodiment of the present disclosure. Embedded coaxial RF circuits 182 or printed micro strip RF circuits 184 are located with dielectric/metal layers 186. These RF circuits 182, 184 are preferably created by printing dielectrics and metallization geometry.

[0064] As illustrated in Figure 14, use of additive processes allows the creation of a high performance electrical interconnect 190 with inter-circuit, 3D lattice structures 192 having intricate routing schemes. Vias 194 can be printed with each layer, without drilling.

[0065] The nature of the printing process permit controlled application of dielectric layers 196 creates recesses 198 that control the location, cross section, material content, and aspect ratio of the conductive traces 192 and the vias 194. Maintaining the conductive traces 192 and vias 194 with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses 198 to control the aspect ratio of the conductive traces 192 and the vias 194 results in a more rectangular or square cross-section, with the corresponding improvement in signal integrity.

[0066] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to the recesses 198. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 198. The

trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 198 not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 198.

[0067] In another embodiment, a thin conductive foil is pressed into the recesses 198, and the edges of the recesses 198 acts to cut or shear the conductive foil. The process locates a portion of the conductive foil in the recesses 198, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses 198 for easy removal. Again, the foil in the recesses 198 is preferably post plated to add material to increase the thickness of the conductive traces 192 in the circuit geometry and to fill any voids left between the conductive foil and the recesses 198.

[0068] Figure 15 illustrates a high performance electrical interconnect 200 with printed electrical devices 202. The electrical devices 202 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like. In the illustrated embodiment, electrical devices 202 include printed LED indicator 204 and display electronics 206. Geometries can also be printed to provide capacitive coupling 208. Compliant material can be added between circuit geometry, such as discussed above, so the present electrical interconnect can be plugged into a receptacle or socket, supplementing or replacing the need for compliance within the connector.

[0069] The electrical devices 202 are preferably printed during construction of the interconnect assembly 200. The electrical devices 202 can be ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. For example, the electrical devices 202 can be formed using printing technology, adding intelligence to the high performance electrical interconnect 200. Features that are typically located on other circuit members can be incorporated into the interconnect 200 in accordance with an embodiment of the present disclosure.

[0070] The availability of printable silicon inks provides the ability to print electrical devices 202, such as disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et

al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson); 6,118,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. In particular, U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated by reference, teach using ink-jet printing to make various electrical devices, such as, resistors, capacitors, diodes, inductors (or elements which may be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistor (including, light emitting, light sensing or solar cell elements, field effect transistor, top gate structures), and the like.

[0071] The electrical devices 202 can also be created by aerosol printing, such as disclosed in U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,163 (Renn et al.); 7,485,345 (Renn et al.); 7,045,015 (Renn et al.); and 6,823,124 (Renn et al.), which are hereby incorporated by reference.

[0072] Printing processes are preferably used to fabricate various functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0073] Ink jet printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semi conductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[0074] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or Teflon.

[0075] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[0076] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from DuPont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[0077] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[0078] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic /organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[0079] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these

polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181, which is incorporated herein by reference.

[0080] A protective layer can optionally be printed onto the electrical devices. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[0081] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layer are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present disclosure.

[0082] The ink-jet print head preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[0083] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[0084] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric,

magnetostrictive, electromechanical, electro pneumatic, electrostatic, rapid ink heating, magneto hydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[0085] While ink jet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: pre-metered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques.

[0086] Figure 16 illustrates an alternate high performance electrical interconnect 220 with printed compliant material 222 added between circuit geometries 224, 226 to facilitate insertion of exposed circuit geometries 228, 230 into a receptacle or socket. The compliant material 222 can supplement or replace the compliance in the receptacle or socket. In one embodiment, the compliance is provided by a combination of the compliant material 222 and the exposed circuit geometries 228, 230.

[0087] Figure 17 is a side sectional view of a method of making a high performance electrical interconnect 250 in accordance with an embodiment of the present disclosure. Substrate 252 includes a plurality of cavities 254 extending through dielectric layer 256. The cavities 254 can be formed using a variety of techniques, such as molding, machining, printing, imprinting, embossing, etching, coining, and the like. Although the cavities 254 are illustrated as truncated cones or pyramids, a variety of other shapes can be used, such as for example, cones, hemispherical shapes, and the like.

[0088] As illustrated in Figure 18, metalizing layer is printed in the cavities 254 to create contact member 258, as discussed above. As illustrated in Figure 19, a compliant layer 260 is printed on the dielectric layer 256, followed by dielectric layer 262 creating recesses 263 for forming circuit geometry 264.

[0089] Figure 20 illustrates circuit geometries 264 printed as discussed above. In one embodiment, the circuit geometries 264 are formed by depositing a conductive material in a first state in the recesses 263, and then processed to create a second more permanent state. For example, the metallic powder is printed according to the

circuit geometry and subsequently sintered, or the curable conductive material flows into the circuit geometry and is subsequently cured. As used herein "cure" and inflections thereof refers to a chemical-physical transformation that allows a material to progress from a first form (e.g., flowable form) to a more permanent second form. "Curable" refers to an uncured material having the potential to be cured, such as for example by the application of a suitable energy source.

[0090] Second compliant layer 270 is printed on exposed surfaces 272 of the dielectric layers 262 and circuit geometries 264. The second compliant layer 270 and second dielectric layer 274 are selectively printed to permit printing of contact member 276. Alternatively, pre-fabricated contact members 276 can be bonded to the circuit geometries 264. As used herein, "bond" or "bonding" refers to, for example, adhesive bonding, solvent bonding, ultrasonic welding, thermal bonding, or any other techniques suitable for attaching adjacent layers to a substrate.

[0091] The dielectric layer 274 adjacent contact members 276 is optionally singulated to permit greater compliance. As used herein, “singulated” refers to slits, cuts, depressions, perforations, and/or points of weakness. In another embodiment, the high performance electrical interconnect 250 is made in two portions and then bonded together.

[0092] Figure 21 illustrates a socket assembly 300 incorporating the high performance electrical interconnect 250 of Figure 20, in accordance with an embodiment of the present disclosure. The dielectric layer 256 is separated from the substrate 252 to expose contact member 258. In the illustrated embodiment, the dielectric layer 274 is bonded to surface 302 of socket housing 304 so that contact members 276 are positioned in recess 306. First circuit member 308, such as an IC device, is positioned in the recess 306 so that the terminals 310 align with the contact members 276.

[0093] The contact members 258, 276 are optionally plated, either before or after the high performance electrical interconnect 250 is installed in the socket housing 304. In another embodiment, the contact members 258, 276 are deformed, such as for example by coining or etching, to facilitate engagement with terminals 310 on the first circuit member 308 and/or terminal 312 on second circuit member 314.

[0094] In operation, the first circuit member 308, socket assembly 300 and the second circuit member 314 are compressively coupled so that contact member 276 electrically couples with terminal 310 and contact member 258 electrically couples

with contact pad 312. Compliant layer 260 biases the contact member 276 into engagement with the terminal 310, while the compliant layer 270 biases the contact member 258 into engagement with the pad 312. The compliant layers 260, 270 also permit the contact members 276, 258 to deflect and compensate for non-planarity of the terminals 310 or the pads 312. As used herein, the term “circuit members” refers to, for example, a packaged integrated circuit device, an unpackaged integrated circuit device, a printed circuit board, a flexible circuit, a bare-die device, an organic or inorganic substrate, a rigid circuit, or any other device capable of carrying electrical current.

[0095] Figure 22 illustrates a high performance electrical interconnect 330 with compliant structure 332 printed to add compliance and normal force 334 external to the circuit geometry 336. For example, the compliant structure 332 can be a printed/sintering metallic spring. In another embodiment, the compliant structure 332 is a stamped or etched metallic, plastic, or overmolded leadframe that is added to the high performance electrical interconnect 330. The compliant members 332 can optionally be singulated in tandem with the circuit geometry 336 to allow for individual contact compliance.

[0096] Figure 23 illustrates a high performance electrical interconnect 350 with male contact member 352 in accordance with an embodiment of the present disclosure. Contact member 352 is preferably inserted through opening 354 printed in dielectric layers 356, 358 and circuit geometry 360. The resiliency of the dielectric layers 356, 358 permits plastic deformation to permit enlarged end 362 to penetrate the opening 354 in the high performance electrical interconnect 350. The resilience of the dielectric layers 356, 358 also permit the contact member 360 to move in all six degrees of freedom (X-Y-Z-Pitch-Roll-Yaw) to facilitate electrical coupling with first and second circuit members 364, 366.

[0097] Figure 24 illustrates a high performance electrical interconnect 370 with printed compliant member 372 located above contact member 374 in accordance with an embodiment of the present disclosure. The printed compliant member 372 and associated contact member 374 is preferably singulated to promote flexure and compliance.

[0098] Figure 25 illustrates an alternate embodiment of a high performance electrical interconnect 380 where printed compliant member 382 is located on circuit member 384. In the illustrated embodiment, secondary printed compliant member 386 is

located on the high performance electrical interconnect 380 above contact member 388.

[0099] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the disclosure. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the disclosure, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the present disclosure.

[00100] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[00101] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the present disclosure is not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[00102] Other embodiments of the disclosure are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the disclosure, but as merely providing illustrations of some of the presently preferred embodiments of this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed

embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the disclosure. Thus, it is intended that the scope of the present disclosure herein disclosed should not be limited by the particular disclosed embodiments described above.

[00103] Thus the scope of this disclosure should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present disclosure fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present disclosure is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean “one and only one” unless explicitly so stated, but rather “one or more.” All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present disclosure, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A high performance electrical interconnect adapted to provide an interface between terminals on first and second circuit members, the electrical interconnect comprising:

a first circuitry layer comprising a first surface and a second surface with a plurality of contact pads adapted to electrically coupled with the terminals on the first circuit member;

at least one dielectric layer printed on the first surface of the first circuitry layer, the dielectric layer comprising a plurality recesses;

a conductive material deposited in at least a portion of the recesses comprising circuit geometry electrically coupled with the first circuitry layer; and

a second circuitry layer comprising a first surface a plurality of contact pads adapted to electrically coupled with the terminals on the second circuit member and a second surface attached to the dielectric layers, the circuit geometry electrically coupling the first circuitry layer to the second circuitry layer.

2. The high performance electrical interconnect of claim 1 comprising a conductive plating layer on at least a portion of the circuit geometry.

3. The high performance electrical interconnect of claim 1 wherein the conductive material comprises one of sintered conductive particles or a conductive ink.

4. The high performance electrical interconnect of claim 1 wherein the dielectric layer comprises a printed compliant material located behind contact pads, the compliant material adapted to bias the contact pads toward the terminals on at least one of the first or second circuit members.

5. The high performance electrical interconnect of claim 1 comprising at least one printed electrical device located on a dielectric layer and electrically coupled to at least a portion of the circuit geometry.

6. The high performance electrical interconnect of claim 5 wherein the electrical device is selected from one of shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded IC devices, RF antennae, and the like.

7. The high performance electrical interconnect of claim 1 comprising an optical quality material deposited in at least a portion of the recesses comprising one or more optical circuit geometries.

8. The high performance electrical interconnect of claim 1 comprising one or more optical fibers located in at least a portion of the recesses comprising one or more optical circuit geometries.

9. The high performance electrical interconnect of claim 1 wherein at least a portion of the circuit geometry comprises a via electrically coupling the first circuitry layer to the second circuitry layer.

10. The high performance electrical interconnect of claim 1 comprising one or more contact members electrically coupled to at least a portion of the circuit geometry and extending above the dielectric covering layer.

11. The high performance electrical interconnect of claim 1 wherein the recesses in the circuit geometry comprise substantially rectangular cross-sectional shapes.

12. An edge connector on the high performance electrical interconnect of claim 1 comprising:

a first portion of the circuit geometry extending beyond the dielectric covering layer;

a compliant material located along a surface of the first portion of the circuit geometry; and

a second portion of the circuit geometry located on top of the compliant material.

13. The high performance electrical interconnect of claim 1 comprising a socket housing coupled to the electrical interconnect, the contact pads on the second circuitry layer positioned in a socket housing recess that is sized to receive the second circuit member.

14. The high performance electrical interconnect of claim 1 wherein the dielectric layers comprise at least one additional circuitry plane selected from one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, or a flexible circuit.

15. The high performance electrical interconnect of claim 1 comprising:

at least one dielectric covering layer on the second surface of the first circuitry layer; and

a plurality of openings in the dielectric covering layer providing access to the contact pads on the first circuitry layer.

16. The high performance electrical interconnect of claim 1 wherein the first circuitry layer comprises:

at least one printed dielectric layer comprising a plurality recesses; and

a conductive material deposited in at least a portion of the recesses comprising via structures electrically coupled with the first circuitry layer.

17. An high performance electrical interconnect assembly comprising:

a housing retaining the high performance electrical interconnect of claim 1;

a first circuit member comprising electrical terminals compressively engaged with the contact pads on the first circuitry layer; and

a second circuit member comprising electrical terminals compressively engaged with the contact pads on the second circuitry layer.

18. The electrical interconnect assembly of claim 17 wherein the first and second circuit members are selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

19. A method of making a high performance electrical interconnect comprising the steps of:

providing a first circuitry layer comprising a first surface and a second surface with a plurality of contact pads adapted to electrically coupled with the terminals on a first circuit member;

printing at least one dielectric layer on a first surface of a first circuitry layer, the dielectric layer comprising a plurality recesses;

printing conductive material in at least a portion of the recesses comprising circuit geometry electrically coupled with the first circuitry layer; and

attaching a second surface of a second circuitry layer to the dielectric layer such that the circuit geometry electrically couples the first circuitry layer to the second circuitry layer, the second circuitry layer comprising a first surface with a plurality of contact pads adapted to electrically coupled with terminals on a second circuit member.

20. The method of claim 19 wherein printing the conductive material comprises the steps of:

printing a conductive material in the recesses; and

sintering the conductive material.

21. The method of claim 19 comprising printing a compliant material in the dielectric layers to bias contact pads into engagement with terminals on the first and second circuit members.

21. The method of claim 19 comprising:

printing at least one electrical device on a dielectric layer; and

electrically coupled the electrical device to at least a portion of the circuit geometry.

22. The method of claim 19 comprising printing an optical quality material in at least a portion of the recesses comprising one or more optical circuit geometries.

23. The method of claim 19 comprising printing at least one via in a dielectric layer to electrically couple adjacent layers of the circuit geometry.

24. The method of claim 19 wherein conductive traces in the circuit geometry comprise substantially rectangular cross-sectional shapes.

25. The method of claim 19 comprising the steps of:

compressively coupling electrical terminals on the first circuit member with contact pads located along the second surface of the first circuitry layer; and

compressively coupling electrical terminals on a second circuit member with contact pads located along the first surface of the second circuitry layer.

26. The method of claim 25 wherein the first and second circuit members are selected from one of a dielectric layer, a printed circuit board, a flexible circuit, a bare die device, an integrated circuit device, organic or inorganic substrates, or a rigid circuit.

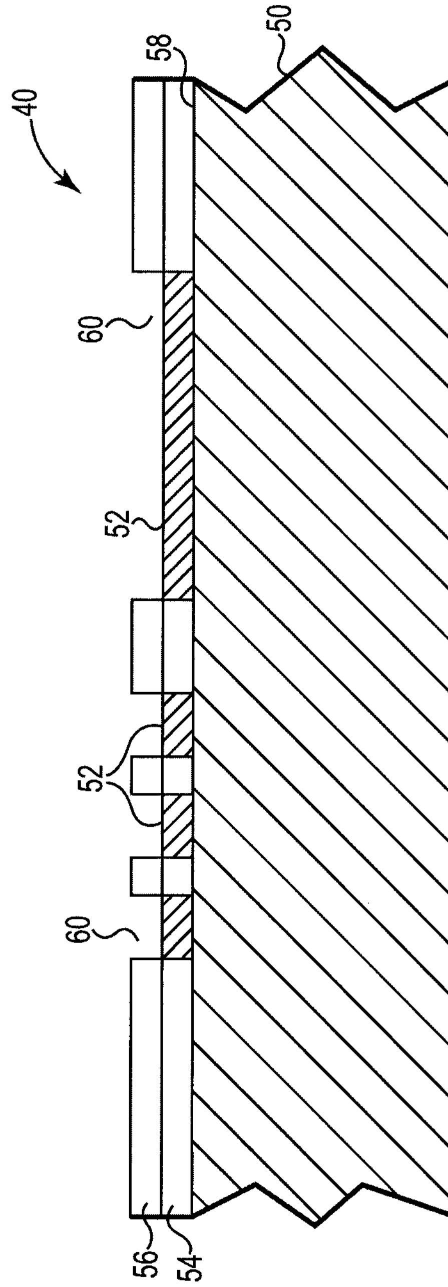

Fig. 1

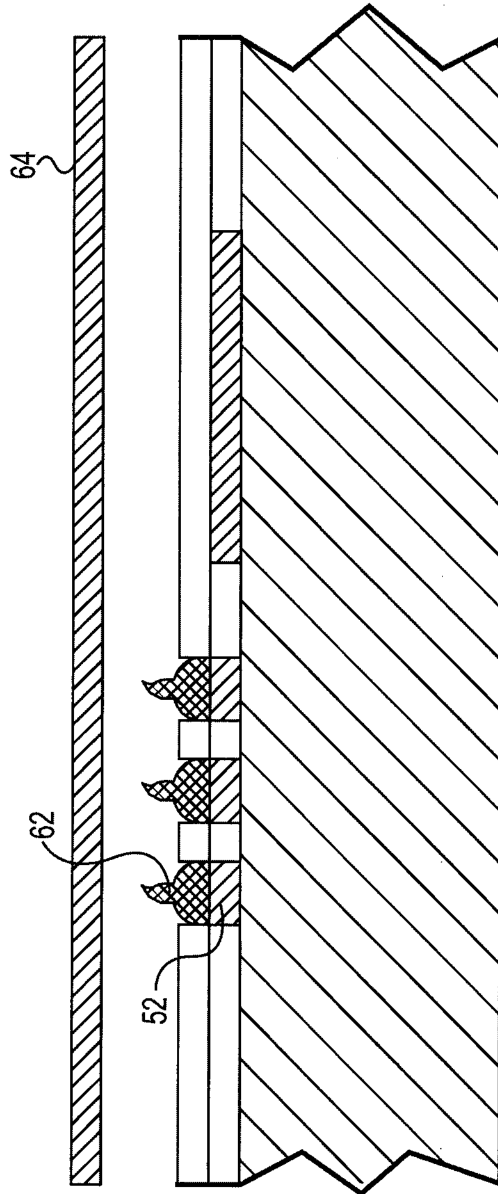

Fig. 2

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64
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Fig. 3

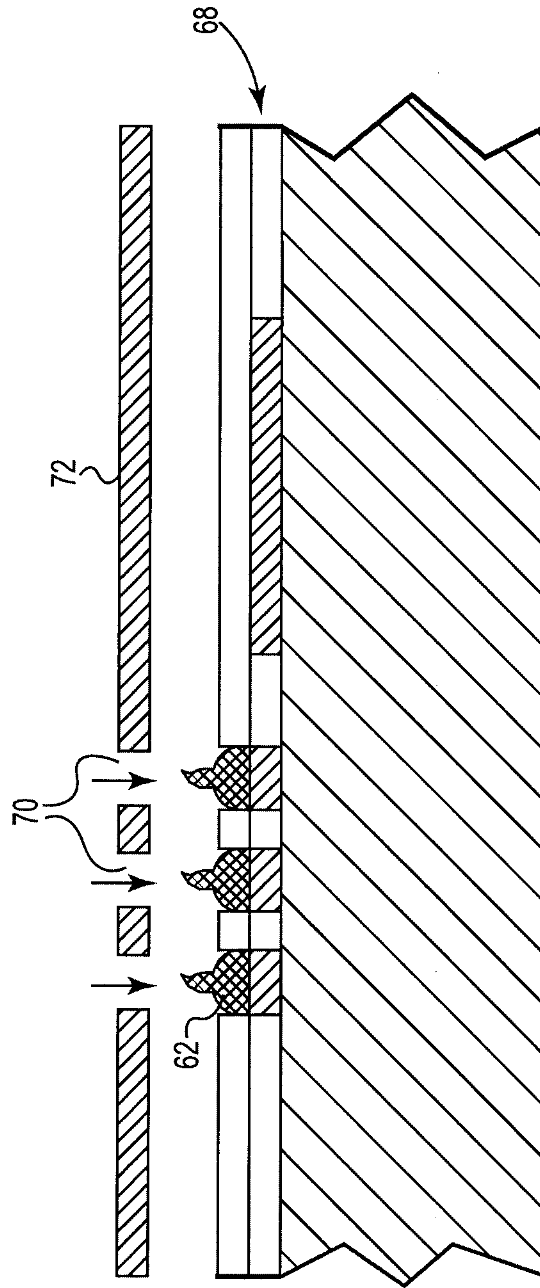

Fig. 4

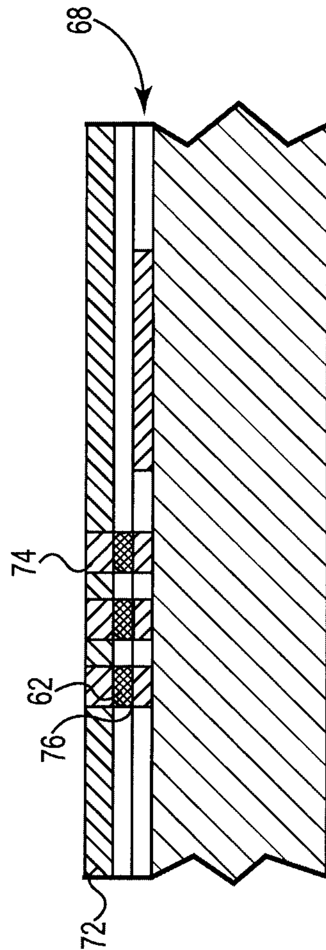

Fig. 5

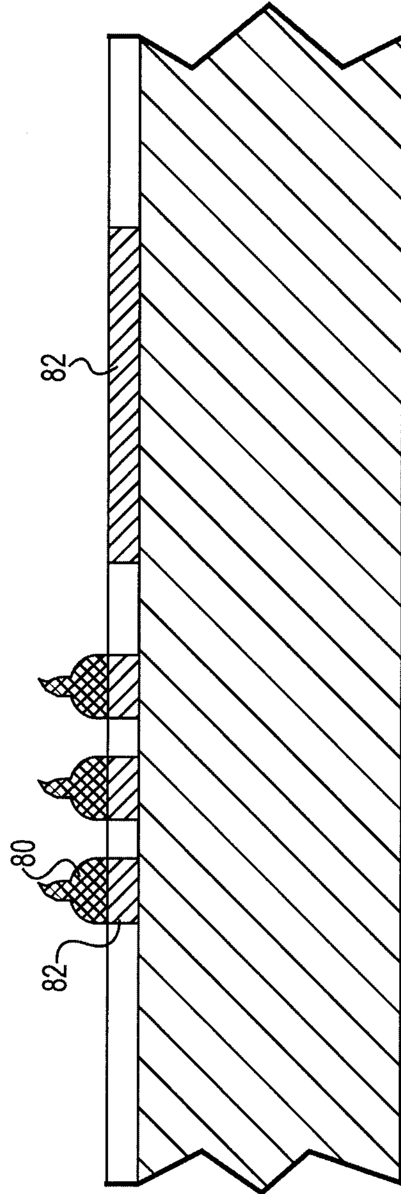

Fig. 6

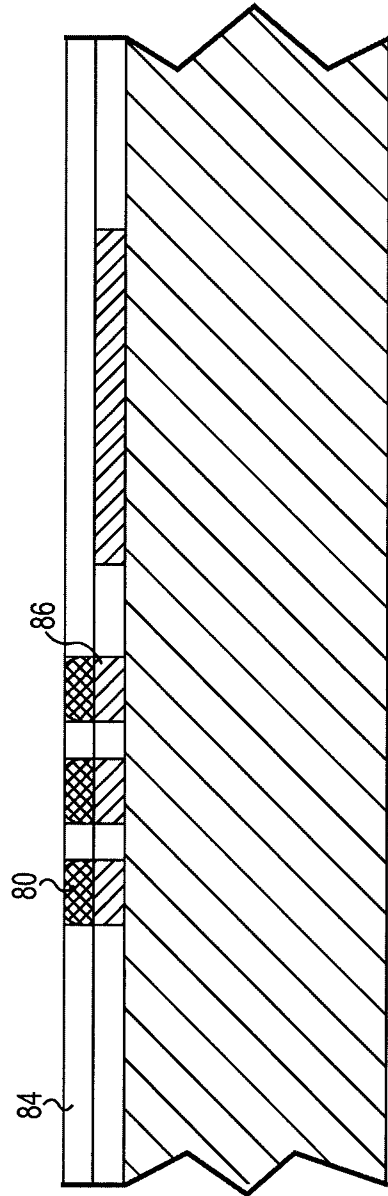

Fig. 7

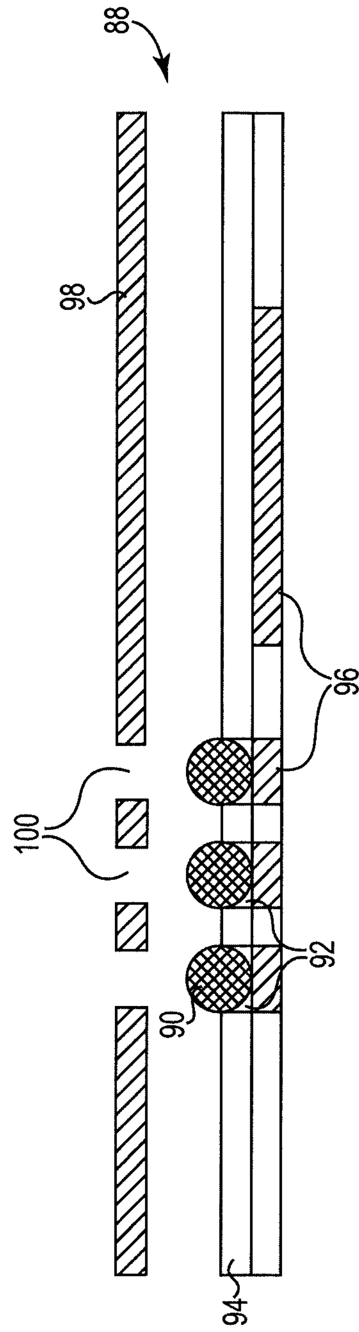

Fig. 8

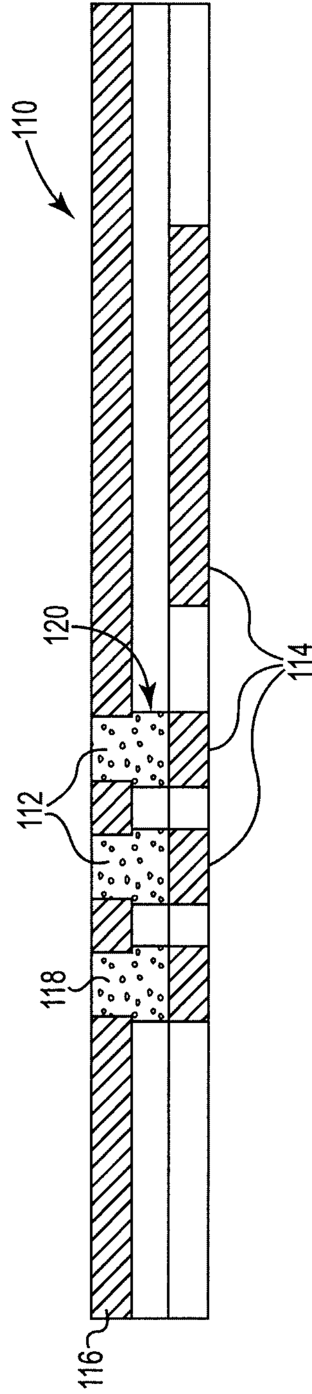

Fig. 9

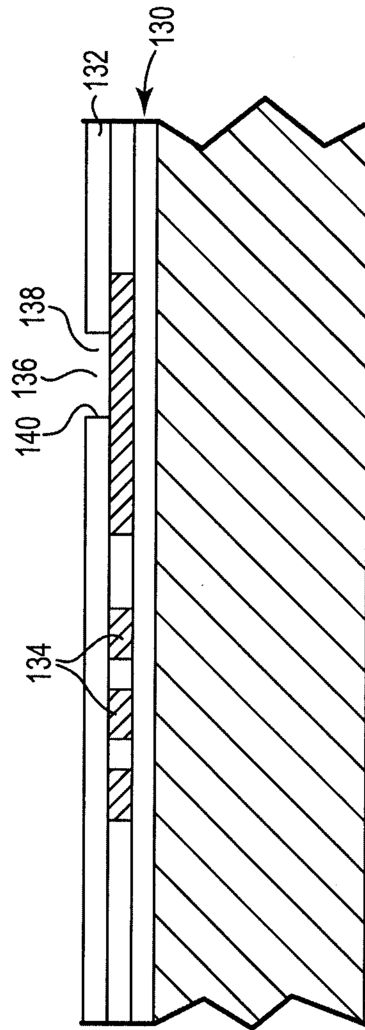

Fig. 10

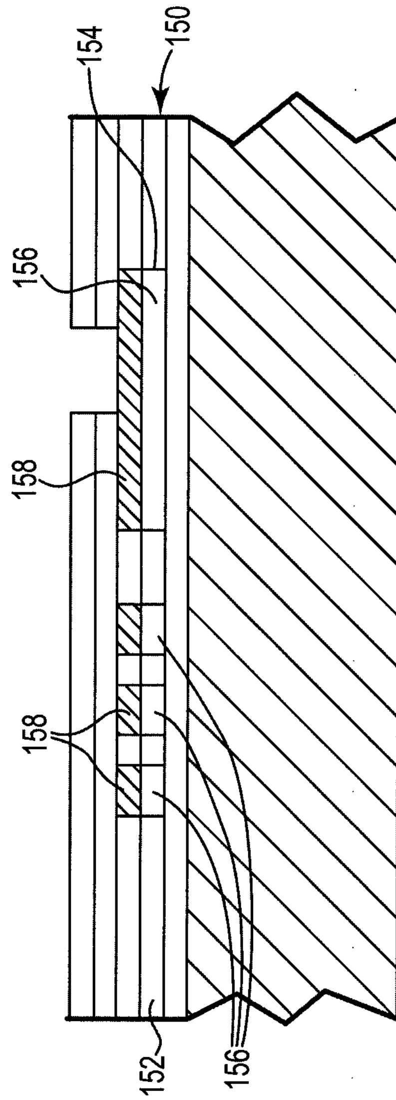

Fig. 11

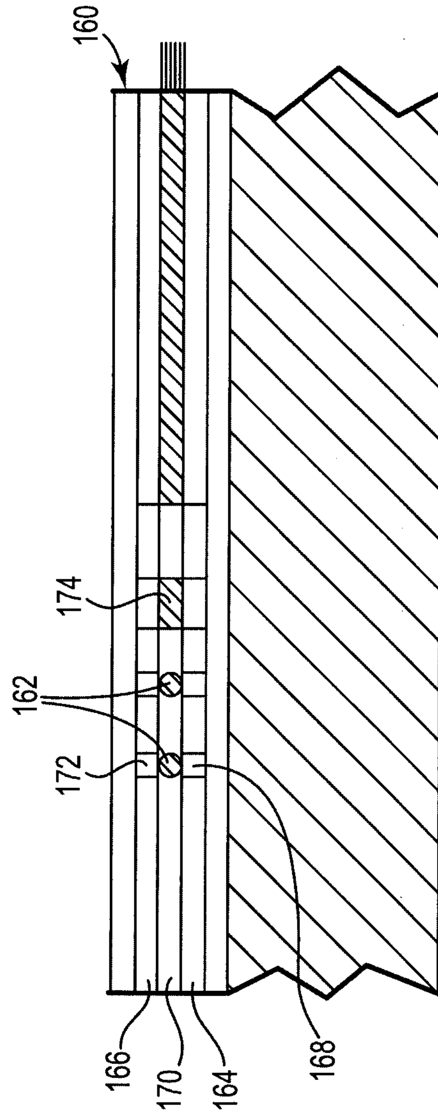

Fig. 12

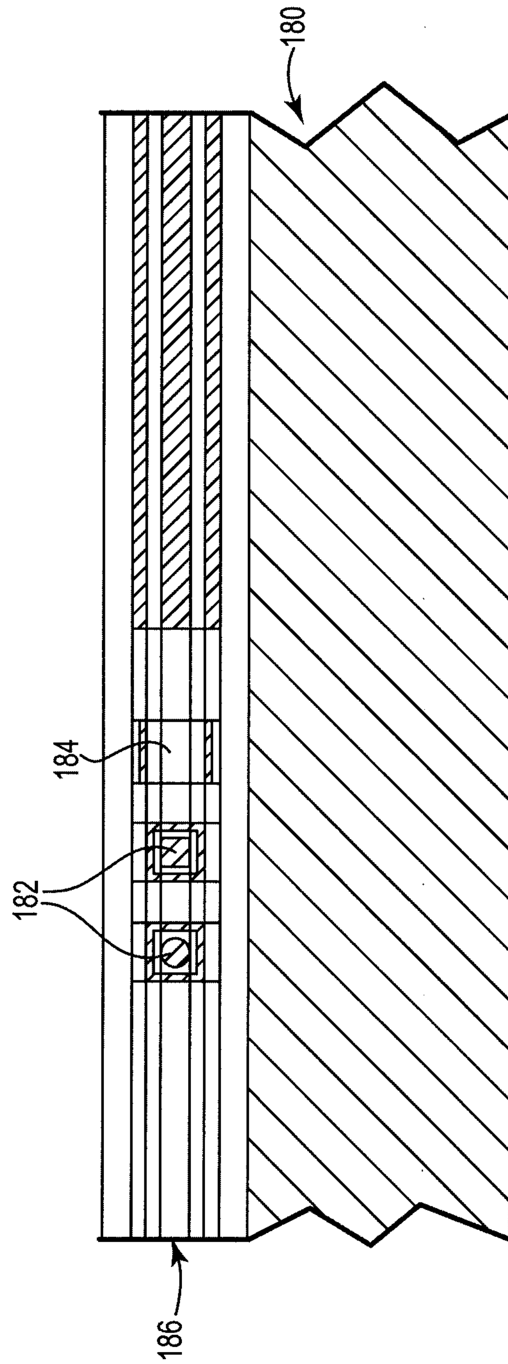

Fig. 13

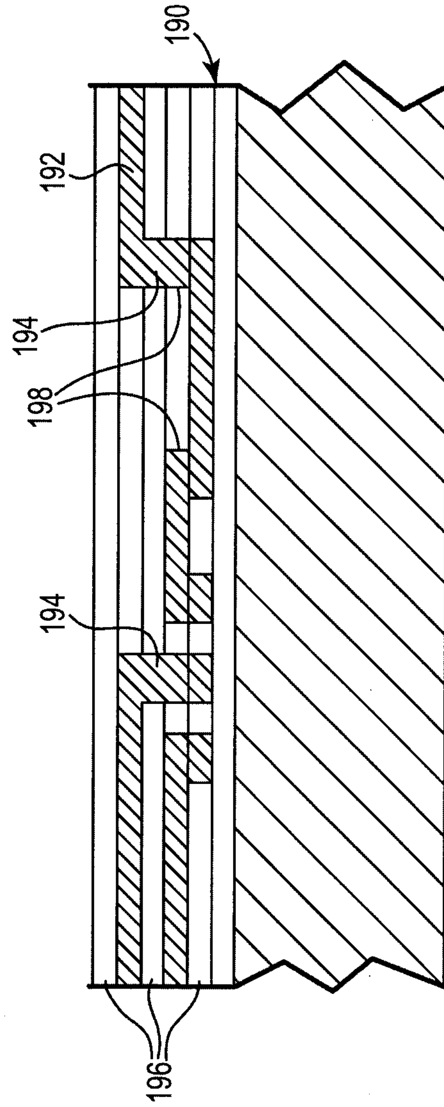
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Fig. 14

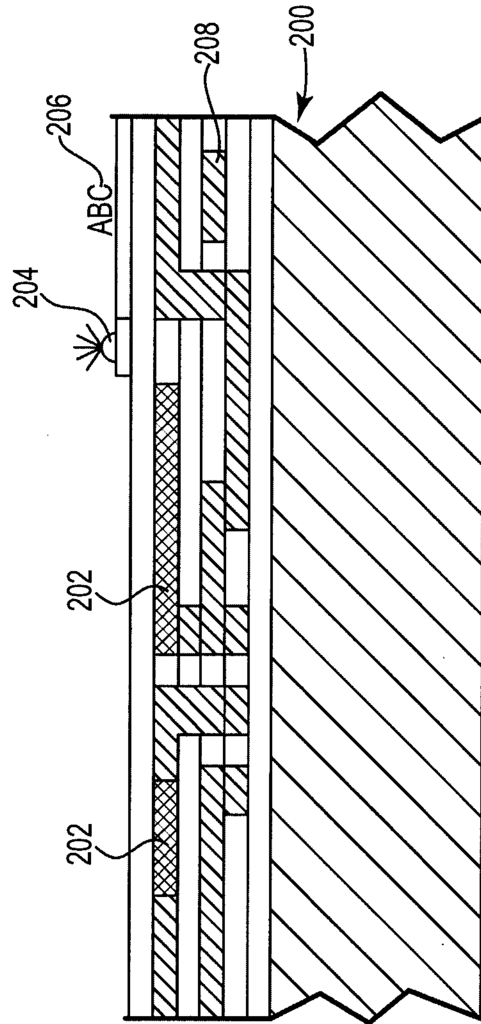

Fig. 15

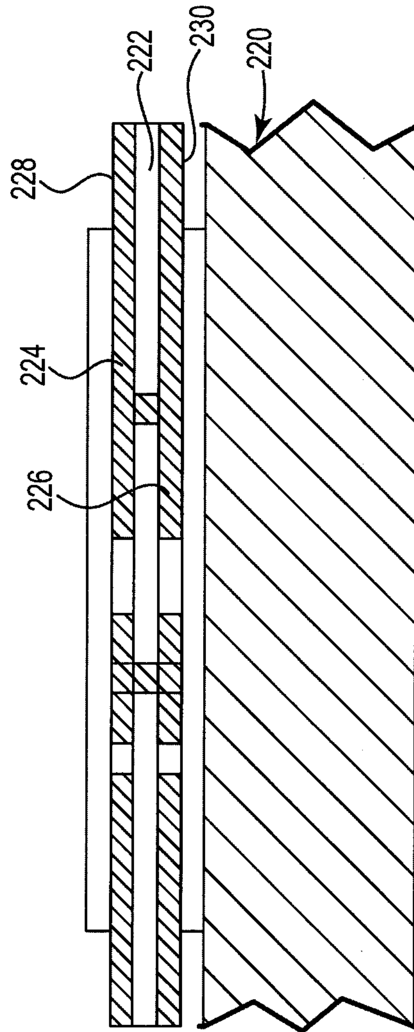

Fig. 16

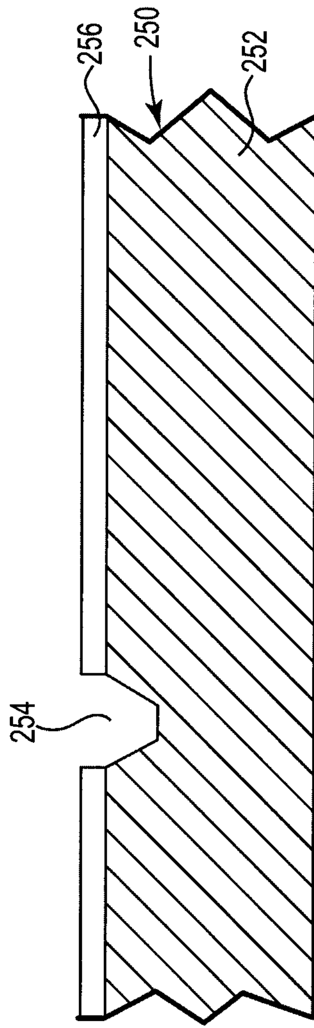

Fig. 17

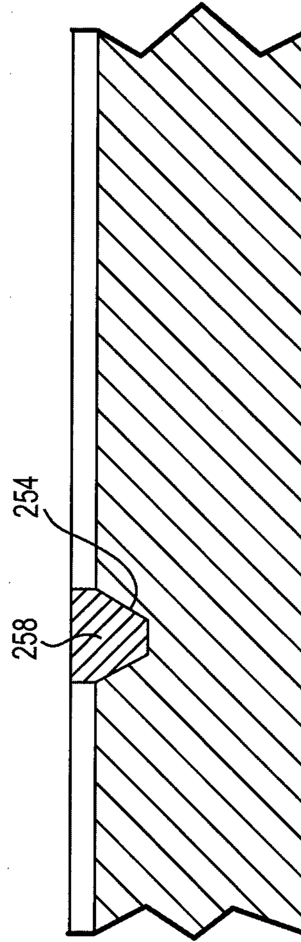

Fig. 18

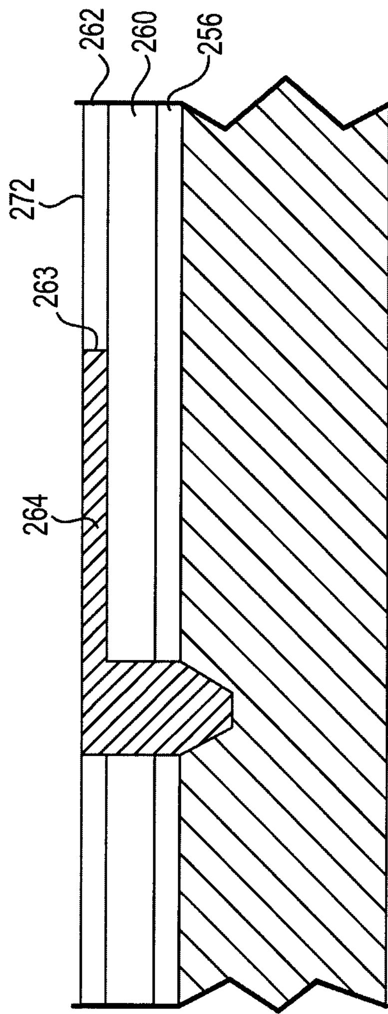

Fig. 19

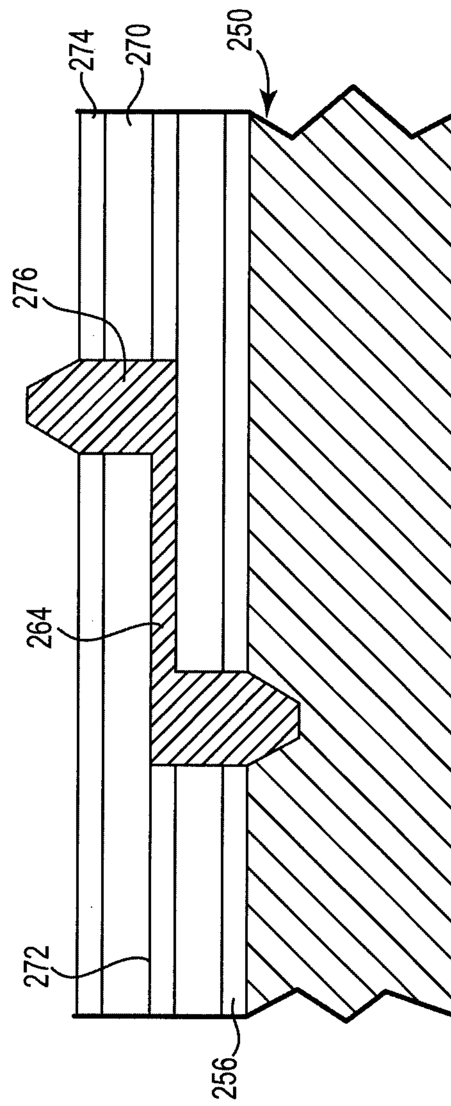

Fig. 20

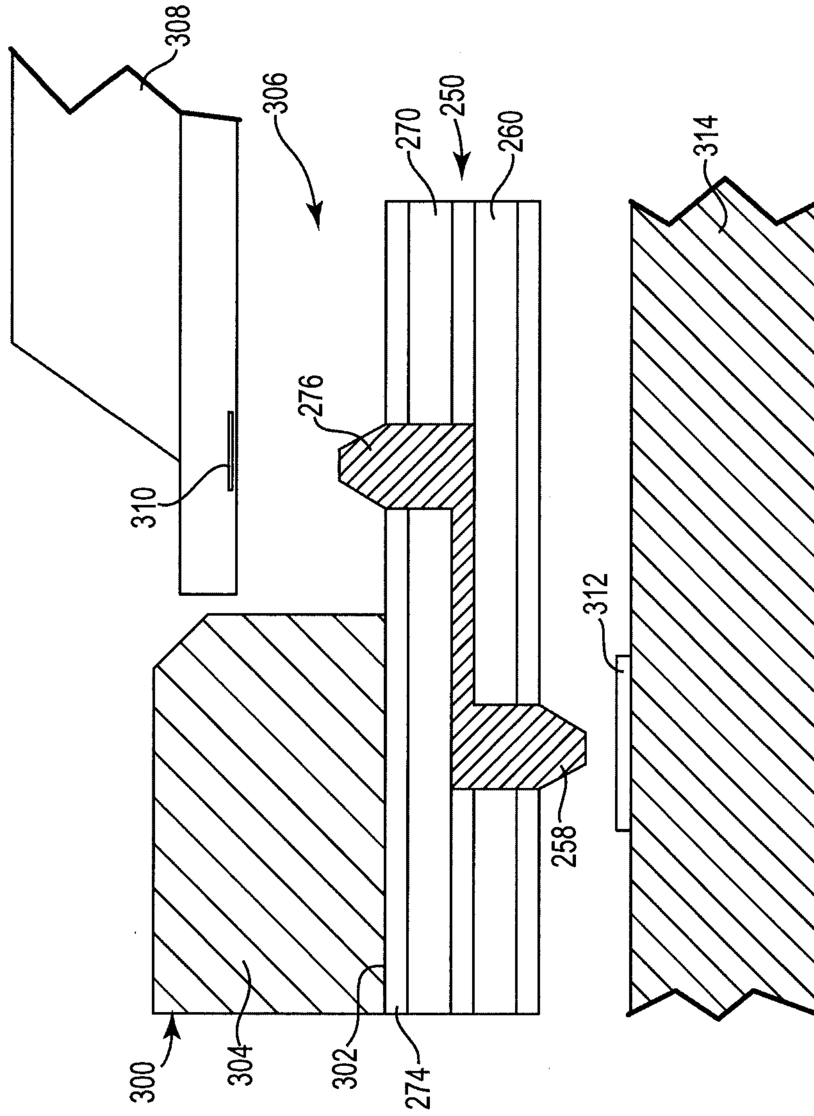

Fig. 21

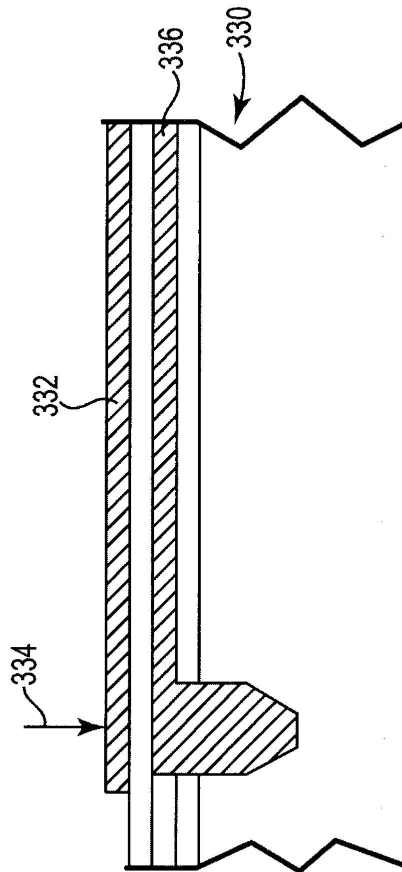

Fig. 22

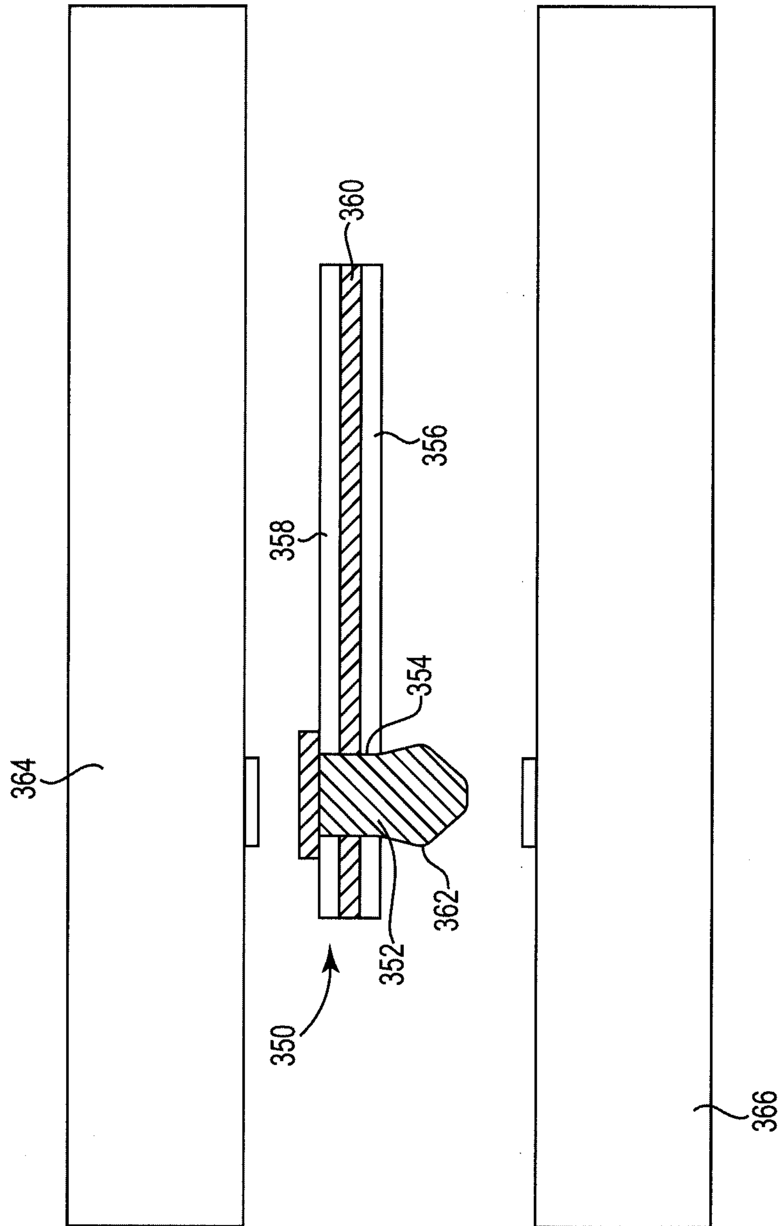

Fig. 23

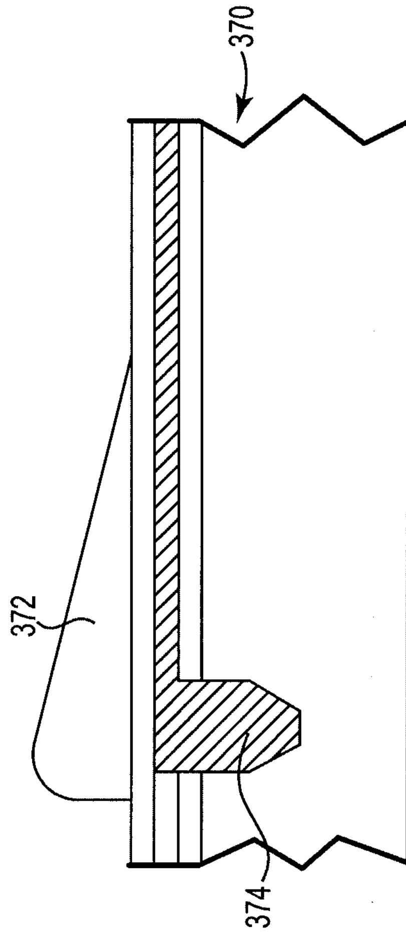

Fig. 24

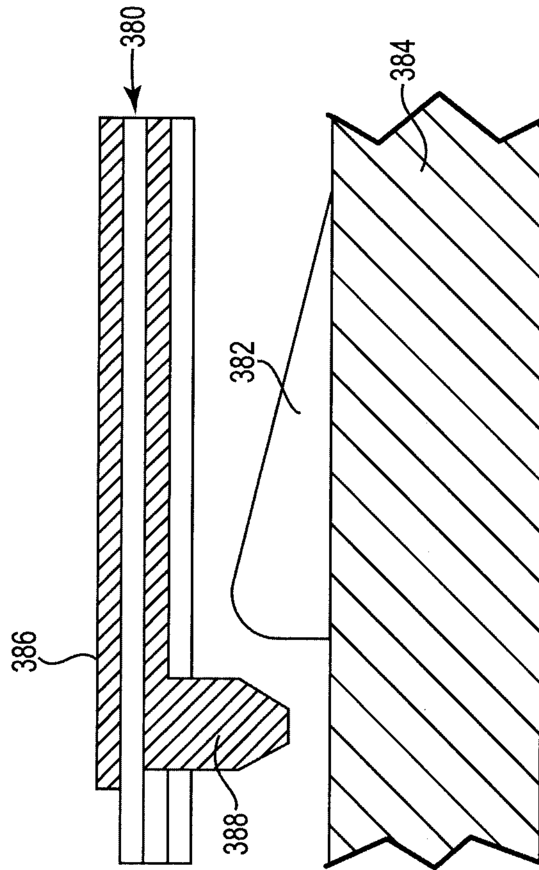

Fig. 25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/056664

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H05K 1/00 (2012.01)
USPC - 361/790
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H05K 1/00, 1/11, 7/00 (2012.01)
USPC - 361/750, 751, 760, 790, 803; 439/65, 66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 7,800,916 B2 (BLACKWELL et al) 21 September 2010 (21.09.2010) entire document	1, 2, 5, 6, 9-11, 13-19, 21B, 23-26 --- 3, 4, 7, 8, 12, 20, 21A, 22
Y	US 7,410,825 B2 (MAJUMDAR et al) 12 August 2008 (12.08.2008) entire document	3, 4, 7, 8, 12, 20, 21A, 22
A	US 7,220,287 B1 (WYRZYKOWSKA et al) 22 May 2007 (22.05.2007) entire document	1-20, 21A, 21B, 22-26
A	US 7,229,293 B2 (SAKURAI et al) 12 June 2007 (12.06.2007) entire document	1-20, 21A, 21B, 22-26
A	US 7,301,105 B2 (VASOYA) 27 November 2007 (27.11.2007) entire document	1-20, 21A, 21B, 22-26
A	US 7,423,219 B2 (KAWAGUCHI et al) 09 September 2008 (09.09.2008) entire document	1-20, 21A, 21B, 22-26

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 January 2012	08 FEB 2012

Name and mailing address of the ISA/US
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