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(71) Applicant: AMS-OSRAM INTERNATIONAL GMBH
[DE/DE]; Leibnizstr. 4, 93055 Regensburg (DE).

(72) Inventors: KREUTER, Philipp; Schützenheimweg 44,
93049 Regensburg (DE). HETZL, Martin; Buchenweg 21,
93351 Painten (DE). VON MALM, Norwin; Stockloher
Str. 8, 93152 Thumhausen/Nittendorf (DE). VARGHESE,
Tansen; Jakobstraße 6, 93047 Regensburg (DE).

(74) Agent: SJW PATENTANWÄLTE; Goethestraße 21,
80336 München (DE).

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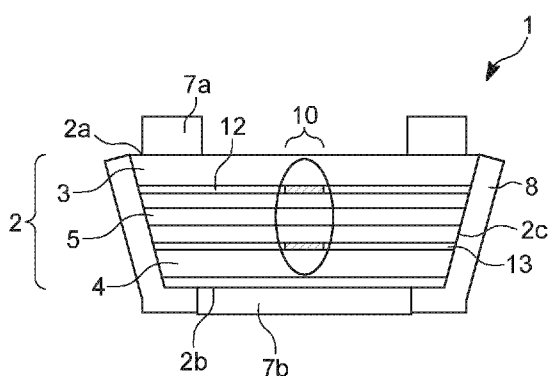


FIG. 1D

(57) Abstract: The invention concerns a μ -LED comprising a semiconductor layer stack having a first layer of a first doping type, a second layer of a second doping type, and an active region arranged between the first and the second layer. The semiconductor layer stack comprises a bottom surface and a top surface as well as mesa structured side surfaces connecting the top and bottom surface and a central region with a lateral dimension which is less than one half of a lateral dimension of the semiconductor layer stack. Further the semiconductor layer stack comprises a material including at least one of phosphide and arsenide and a current path from the first layer to the second layer through the active region is limited to the central region.

FAST-SWITCHING INGAALP OR INGAALAS-BASED μ LEDs FOR HIGH-SPEED DATA COMMUNICATION

The present application claims priority from German patent application
5 DE 10 2023 115 113.4 filed on June 08, 2023, the disclosure of which
is incorporated by way for reference in its entirety.

The present invention concerns a μ -LED for use as a means for optical
data communication, as well as a method for manufacturing the μ -LED.

BACKGROUND

Today's Internet relies on large data centres. However, their high-
power consumption poses problems to ensure their operation with purely
15 sustainable energy sources. Most of the power is consumed not for
computations, but for data transmission over short distances ($\ll 10\text{m}$):
CPU to GPU, server to server, rack to rack.

The use of μ -LEDs for optical and data communication has several
20 benefits. Apart from the small size, which provides an easier
interconnect to fibre optics, the vertical or horizontal optoelectronic
components provide an improved scalability and can be easily
implemented in existing designs at large numbers. In this regard a μ -
LED is an optoelectronic component that comprises a diameter or more
25 general a dimension that is smaller than $50\text{ }\mu\text{m}$ and in particular smaller
than $20\text{ }\mu\text{m}$. In some special applications, a μ -LED can range in diameter
between $1\text{ }\mu\text{m}$ and $10\text{ }\mu\text{m}$.

μ -LEDs in comparison to conventional LEDs with larger sizes further
30 require a very low current resulting in an overall low power
consumption, thereby reducing the amount of heat generated during
operation. This again not only saves power, which is particularly
suitable for short and midrange interconnects, but also simplifies the
requirements regarding the heat transfer layer enabling a dense
35 application of such optoelectronic components. However, apart from the
requirement of a high quantum efficiency to provide enough light, data
communication also requires a high switchability or more general a

large amplitude modulation depth at high frequencies. Current optical data communication ranges from several hundred Megahertz to a few Gigahertz, for example in the range between 10 GHz and 50 GHz.

5 As a result thereof, current μ -LEDs have to be switched on and off or at least modulated in their respective emission amplitude within that frequency range. Given the fact, that a light pulse in itself requires a certain length to be detected at the receiver end, such high frequencies require a radiative recombination lifetime in the range of
10 a few ten picoseconds and less. The radiative recombination lifetime is the time required for the minority charge carriers to recombine under radiation after turning off the current through the μ -LEDs. Consequently, the radiative recombination life directly affects the fall time of a light pulse emitted by the μ -LEDs.

15 Various measures have been proposed to reduce the rise and fall times during a pulse or amplitude modulated emission, as current μ -LEDs are limited in this regard resulting in a switching time of only a few hundred megahertz and rise and fall times to 100 ps or more.

20 As an example, background doping in the quantum barriers of the respective optoelectronic components can be implemented in order to increase the charge carrier density. While this is suitable in some cases, it requires a precise control during the epitaxial growth of
25 the quantum barriers. As an alternative, non-radiative defect centres within the active region can be provided to increase the non-radiative recombination competing with radiative recombination of the charge carrier. However, due to dopant or defect centre diffusion and other characteristics, those induced measures face reliability issues and
30 are difficult to control during processing of the devices.

It is thus an object of the present invention, to provide an optoelectronic device that can be used for optical data communication with a reduced energy consumption while maintaining or even increasing
35 the data transmission rate to be achieved or decreasing the switching time required for this.

SUMMARY OF THE INVENTION

This and other objects are addressed by the subject matter of the independent claims. Features and further aspects of the proposed principles are outlined in the dependent claims.

The inventors have recognized that for optoelectronic devices such as μ -LEDs based on a gallium arsenide (GaAs), or indium aluminum gallium arsenide (InAlGaAs) material systems, increasing the current density through the optoelectronic device increases the carrier concentration in the area of radiative recombination. This results in higher recombination rates and, thus, higher switching speeds to be achieved with the optoelectronic device. The current density at a given current and a given size of the optoelectronic device is thereby in particular increased by reducing the region through which the current flow is conducted through the active region of the optoelectronic device.

In an aspect of the proposed principle, an optoelectronic device such as a μ -LED comprises a semiconductor layer stack. The semiconductor layer stack includes a first layer having a first doping type and a second layer having a second doping type. The first doping type can for example include an n-type doping, while the second doping type may include a respective p-type doping. In this regard, the first and second layer may comprise a plurality of sub-layers including different doping concentrations and doping profiles, respectively. For example, doped sub-layers opposite an active region may comprise a higher doping concentration suitable for current distribution across the overall area of the respective doped layer.

An active region is arranged between the first and second layer. In some aspects, the active region may comprise a simple pn-junction. In some other aspects, the active region may comprise a quantum well layer. As a further alternative, the active region may include a multi-quantum well structure having a plurality of alternating barrier layers and quantum well layers, respectively.

In accordance with the proposed principle, the material for the semiconductor layer stack comprises gallium arsenide (GaAs), or aluminum gallium arsenide (InAlGaAs). Said combination of materials is suitable to emit light in the red, and infrared portion of the spectra.

5 In this regard, the aluminum (Al) content of the aluminum gallium arsenide $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers within the layer stack may vary with parameter x and can be in the range between 0% and 70%, respectively. In some aspects, the Al content varies depending on the colour and can reach up to 80% in the outer layers with decreasing Al content in the direction of the active region. With longer wavelengths, i.e. in the infrared spectrum, the Al content can be 30 % and less. In some aspects, the active region may comprise no Al content or less than 10% in some further aspects, the active region may comprise InAlGaAs with an In content from 0% to 50%. In this regard an active region may comprise a multi-quantum well with its barrier layers having an Al content of larger than 10% and its quantum well layers having an AL content of less than 10%.

The semiconductor layer stack comprises a top surface and a bottom surface opposite the top surface as well as mesa structured side surfaces connecting the top and bottom surface. The mesa structured side surfaces, extend from the first layer to the second layer. The side surfaces can be inclined with a varying degree of inclination. In some aspects, the side surfaces extend along a certain crystal direction, in particular in a direction that generates only a few natural non-radiative recombination centres. In some aspects, the inclination of the side surfaces can change. In particular, the inclination of the side surfaces close to the active region may be smaller than an inclination further away and particularly on one of the first and second layer, respectively.

The semiconductor layer stack further comprises a central region with a lateral dimension which is less than one half of a lateral dimension of the semiconductor layer stack. In particular the semiconductor layer comprises a central region extending between the top surface and the bottom surface and being spaced to the side surfaces by at least one fourth of the distance between two opposing side surfaces. The term

central region can in particular be understood as a region extending around the center of gravity of the semiconductor layer stack being spaced to the side surfaces by for example by at least one fourth of the distance between two opposing side surfaces, thus the central region comprises a lateral dimension which is less than three quarters, or less than one half of a lateral dimension of the semiconductor layer stack, wherein the lateral dimension extends between opposing side surfaces in a lateral direction. Less than one half of the lateral dimension can in particular mean that the central region comprises approximately less than one ninth of the area of the semiconductor layer stack.

In accordance with the proposed principle, a current path from the first layer to the second layer through the active region is limited to the central region. This can be achieved by several measures addressed in the following aspects. The different aspects allow for example an optimization of the active region size for high current density/switching speeds while keeping a respective size of the semiconductor layer stack for deheating the heat generated within the optoelectronic device during operation of the same. The improved heat management can thereby have positive effects on the reliability and lifetime of the optoelectronic device.

In some aspects, the semiconductor layer stack comprises a partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer arranged between the first layer and the active region and/or between the second layer and the active region. The parameter x is thereby in particular greater than 0.5 and in particular greater than 0.9 and in particular greater than 0.97. The oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer ranges from the side surfaces until the central region whereas the central region of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer remains substantially unoxidized. The partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer can for example comprise a thickness in the range of 5 nm to 20 nm and/or is optionally doped. By means of the oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer a current confinement of a current applied to the first and second layer is created, since the oxidized area has an insulating effect and the current therefore only flows through the non-oxidized central region

into and through the adjacent active region. Although this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device.

The oxidation of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer can for example be conducted in a wet oven after mesa structuring the semiconductor layer stack. The depth of the oxidation can in thereby in particular be tuned by for example the time of the step of oxidation within the wet oven. The partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer can be arranged in the blocking area/active region of the semiconductor layer stack on the first layer, on the second layer, or on both layers.

In some aspects, the active region comprises an intermixed, in particular quantum well intermixed, region outside the central region with a larger band gap than the active region within the central region. By means of the intermixed region of the active region, a current confinement of a current applied to the first and second layer is created, since the intermixed region with a larger bandgap as the central region has a more or less insulating or at least current guiding effect and the current therefore mostly flows through the central region through the active region. Although this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device.

A quantum well intermixing can at the same time result in an increase of the amount of defects (dangling bonds/ non-radiative recombination centers) along the side surfaces of the active region to influence the possibilities for non-radiative recombination in the active region. In particular by this the diffusion length/mean-free path of the charge carriers is limited to a central region of the active region in which recombination of the charge carriers under the emission of light can take place resulting in a reduced charge carrier lifetime.

By the term "charge carrier lifetime" it is in particular to be understood the time t , until which a charge carrier within the active region recombines under the emission of light or non-radiatively. A high charge carrier lifetime comes with a high switch off time of the optoelectronic devices and thus with a reduced possible switching time of the optoelectronic devices, as charge carriers within the active region with a high lifetime may recombine under the emission of light well after the point in time when the optoelectronic devices are already disconnected from their electrical supply. Such an "afterglow" does not allow to provide fast switching frequencies, e.g. in the GHz range. By means of a quantum well intermixing of the active region in regions outside the central region, the charge carrier lifetime can however be reduced resulting in a high switch off time of the optoelectronic device.

In some aspects, the active region and in particular the semiconductor layer stack comprises an ion implanted region outside the central region with having a worse conductivity than the active region within the central region and in particular the semiconductor layer stack within the central region. The ion implantation can in particular be conducted by means of an ion bombardment of the side surfaces of the semiconductor layer stack resulting in an ion implanted region outside the central region. The type of ions and the amount of ions implanted into the semiconductor layer stack outside the central region can thereby be chosen such that the ion implanted region outside the central region comprises a worse conductivity than within the central region or higher insulating properties than within the central region. In addition or as an alternative due to the ion implantation, the active region outside the central region can comprise a larger bandgap than within the active region.

By means of the ion implanted region outside the central region, a current confinement of a current applied to the first and second layer is created, since the ion implanted region with a larger bandgap and/or a worse conductivity as the central region has a more or less insulating or at least current guiding effect and the current therefore mostly flows through the central region through the active region. Although

this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device.

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As described for the quantum well intermixing, the ion implantation can at the same time result in an increase of the amount of defects (dangling bonds/ non-radiative recombination centers) along the side surfaces of the active region to influence the possibilities for non-radiative recombination in the active region. In particular by this the diffusion length/mean-free path of the charge carriers is limited to a central region of the active region in which recombination of the charge carriers under the emission of light can take place resulting in a reduced charge carrier lifetime. Hence, by means of a ion implantation of the active region in regions outside the central region, the charge carrier lifetime can be reduced resulting in a high switch off time of the optoelectronic device.

In some aspects, the first and/or the second layer is limited to the central region. The first and/or second layer can in particular be selectively grown on the active region such that it is limited to the central region. By means of this a current confinement of a current applied to the first and second layer is created, since the first and/or second layer being already limited to the central region resulting in a current guiding effect and the current therefore mostly flows through the central region through the active region. Although this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device.

Some further aspects concern the semiconductor layer stack. In some aspects, the semiconductor layer stack comprises a first and second, - in particular- undoped cladding layer. The cladding layers are located directly adjacent to the active region and may comprise, for example undoped aluminum gallium arsenide. The cladding layer is usually used to prevent an undesired diffusion of dopants from the doped first and

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second layers into the active region. The thickness of the cladding layer may range from a few nm to a few 10 nm.

In some aspects, the active region may comprise a quantum well layer having an additional doping level in the range between $1 \times 10^{16} \text{ 1/cm}^3$ to $1 \times 10^{18} \text{ 1/cm}^3$. The additional doping level increases the charge carrier density within the quantum well layer, thereby reducing the carrier lifetime. Accompanying it with the other measures, the overall radiative lifetime can be further reduced.

In some further aspects, the active region comprises a multi-quantum well structure having a plurality of alternating barrier layers and quantum well layers. The barrier layers comprise a higher Al content than the adjacent quantum well layers. In this regard, at least two barrier layers can comprise a doping level in the range of $1 \times 10^{16} \text{ 1/cm}^3$ to $1 \times 10^{18} \text{ 1/cm}^3$. Similar to the previous embodiment, the charge carrier density in the barrier layers is increased, thereby reducing the radiative lifetime.

In a further aspects, the active region may comprise a plurality of quantum dots, in particular, GaAs/AlGaAs quantum dots. Inserting quantum dots instead of quantum wells in the active region may also increase the overall switching speed due to their faster recombination. Similar to the previous embodiments, this aspect can be combined with the implementation of the non-radiative recombination centres.

In this regard, the optoelectronic device can be implemented as a vertical or horizontal optoelectronic device. In a horizontal optoelectronic device the device comprises their respective highly doped or otherwise conductive contact areas on the same side of the layer stack and preferably opposite the main emission surface of the device. A vertical optoelectronic device comprises respective highly doped or otherwise conductive contact areas on two opposing sides, wherein one of the contact areas may also include the main emission surface. The proposed principle illustrated in the various embodiments later on are not limited to vertical or horizontal optoelectronic devices but can be implemented in both.

In some aspects, the optoelectronic device further comprises at least one regrowth layer covering the side surfaces and/or optionally a passivation layer arranged on exposed surfaces of the regrowth layer and/or exposed surfaces of the semiconductor layer stack. The at least one regrowth layer can for example be a structure of alternating layers having different doping types such as for example a pnp or an npn structure covering the side surfaces of the semiconductor layer stack. Such an embodiment can in particular also be suitable even without any of aforementioned aspects for current confinement within the semiconductor layer stack when reducing the lateral dimensions of the semiconductor layer stack to an absolute minimum, and thus reducing the emission area of the active region. At the same time this results in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device. The at least one regrowth layer and/or passivation layer thereby acts as current confinement structure to guide the current through the active region and preserves the side surfaces from other unwanted effects.

In some aspects, the optoelectronic device further comprises a first contact element arranged on the first layer and/or a second contact element arranged on the second layer. The first and/or second contact element in particular serve to provide a supply current to the optoelectronic device. The first and/or second contact element can for example be of a transparent conductive oxide (TCO) to allow light being generated within the active region being emitted from the optoelectronic device and/or the first second contact element can when viewed onto the bottom surface, comprise a structure with a central region of the first and/or second layer remaining free of the first contact element and in particular forming a ring. It is however also conceivable that the first and/or second contact element completely cover the respective underlying semiconductor layer.

According to at least one aspect, the central region of the active region comprises a lateral dimension of less than the diffusion length of the material system of the active region. By this the charge carrier

lifetime can further be reduced and desired switching times for the optoelectronic device can be achieved.

According to at least one aspect, the optoelectronic device is configured to have a switching on and/or off time in the range of 0,5 ns to 10ns, in particular a switching on and/or off time down to 0,1ns. With such a switching time, fast switching frequencies, e.g. in the GHz range, can be realized.

According to a further aspect of the present invention, the optoelectronic device according to at least one of aforementioned aspects can be used as a means for optical data communication, in particular short distance communication of less than 10m. The optoelectronic device according to at least one of aforementioned aspects can in particular be used for data transmission in large data centres and the like, to transmit data over short distances ($<10\text{m}$) for example from CPU to GPU, server to server, and/or rack to rack.

Further aspects refer to a method of manufacturing an optoelectronic device. The method provides a semiconductor layer stack having a first layer and a second layer. The first layer comprises a first doping type and the second layer comprises a second doping type. An active region is arranged between the first and second layer. The semiconductor layer stack is thereby comprising a material including at least one of phosphide and arsenide and is for example based on an GaAs/AlGaAs material combination.

In a further step, a mesa etching process is conducted to form side surfaces connecting a top and a bottom surface of the semiconductor layer stack and exposing portions of the active region in a circumferential perimeter. In a top view, said perimeter can have the shape of a circle, a rectangle, or a polygon like a hexagon for example.

The semiconductor layer stack is then processed in such a way that a central region with a lateral dimension which is less than one half of a lateral dimension of the semiconductor layer stack is formed and such that a current path from the first layer to the second layer through the active region is limited to that central region. Hence the

semiconductor layer stack is processed to realize a current confinement of a current applied to the first and second layer to a central region of at least the active region. This can be achieved by several measures addressed in the following aspects. The different aspects allow for example an optimization of the active region size for high current density/switching speeds while keeping a respective size of the semiconductor layer stack for deheating the heat generated within the optoelectronic device during operation of the same. The improved heat management can thereby have positive effects on the reliability and lifetime of the optoelectronic device.

In some aspects, the step of providing a semiconductor layer stack comprises depositing an $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer arranged between the first layer and the active region and/or between the second layer and the active region. The parameter x is thereby in particular greater than 0.5 and in particular greater than 0.9 and in particular greater than 0.97. The $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer can for example comprise a thickness in the range of 5 nm to 20 nm and/or is optionally doped in the same range as the first and second doped layers of the layer stack. Suitable doping concentrations are known to the skilled person.

In some aspects, the step of processing the semiconductor layer stack comprises partially oxidizing the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) such that the oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer ranges from the side surfaces until the central region and the central portion remains substantially unoxidized. Hence the semiconductor layer stack comprises a partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer arranged between the first layer and the active region and/or between the second layer and the active region. The oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer ranges from the side surfaces until the central region whereas the central region of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer remains substantially unoxidized. By means of the oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer a current confinement of a current applied to the first and second layer is created, since the oxidized area has an insulating effect and the current therefore only flows through the non-oxidized central region into and through the adjacent active region. Although this results in a smaller emission area of the active region it results

on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device.

5 The oxidation of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer can for example be conducted in a wet oven after mesa structuring the semiconductor layer stack. The depth of the oxidation can in thereby in particular be tuned by for example the time of the step of oxidation within the wet oven. The partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer can be arranged in the blocking
10 area/active region of the semiconductor layer stack on the first layer, on the second layer, or on both layers.

In some aspects, the step of processing the semiconductor layer stack comprises implanting ions into at least the active region and in
15 particular the semiconductor layer stack outside the central region forming an ion implanted region outside the central region having a worse conductivity and or higher bandgap than the active region within the central region and in particular the semiconductor layer stack within the central region. The ion implantation can be conducted by
20 means of an ion bombardment of the side surfaces followed by for example a step of annealing such that at least the active region and in particular the semiconductor layer stack outside the central region forms an ion implanted region outside the central region having a worse conductivity and/or larger bandgap than the active region within the
25 central region and in particular the semiconductor layer stack within the central region. By means of the ion implanted region outside the central region a current confinement of a current applied to the first and second layer is created, since the ion implanted region has an insulating effect and the current therefore only flows through the
30 central region through the active region. Although this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device.

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In some aspects, the step of processing the semiconductor layer stack comprises intermixing, in particular quantum well intermixing, the

active region outside the central region forming a region of the active region with a larger band gap than the active region within the central region. By means of the intermixed region outside the central region a current confinement of a current applied to the first and second layer is created, since the intermixed region has an insulating effect and the current therefore only flows through the central region through the active region. Although this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device. The intermixing of the active region can thereby be conducted by any know process known in the art.

In some aspects, the step of providing or the step of processing the semiconductor layer stack comprises a structuring and/or selective growth of the first and/or the second layer such that the first and/or second layer is limited to the central region. In particular a selective growth of the first and/or the second layer on the active region comprises providing a hardmask of for example SiO_2 or Si_3N_4 on the active region adjacent to the central region and growing the first and/or the second layer on the active region in the central region. The limitation of the first and or second layer results in a current confinement of a current applied to the first and second layer, since the current only flows through the central region through the active region. Although this results in a smaller emission area of the active region it results on the other hand in a higher carrier concentration in the area of radiative recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device. The structuring and/or growing of the first and/or second layer can thereby be conducted by any know process known in the art.

In some aspects, the method further comprises a step of regrowing at least one regrowth layer on the side surfaces and/or optionally a step of growing a passivation layer on exposed surfaces of the regrowth layer(s) and/or on exposed surfaces of the semiconductor layer stack.

In some aspects, the method further comprises a step of providing a first contact element on the first layer and/or a bottom contact element on the second layer. The first and/or second contact element can thereby be formed according to aforementioned aspects described for the optoelectronic device.

In some aspects, the step of providing the semiconductor layer stack comprises providing a first and a second, in particularly undoped cladding layer directly adjacent to the active region. To this extent the semiconductor layer stack comprises in some aspects a first and a second, in particularly undoped cladding layer directly adjacent to the active region. Those layer prevent diffusion of dopants but can also be used as a charge carrier blocking structure.

The optoelectronic device such as a μ -LED presented herein is suitable for a variety of applications, in which a high switching or current modulation frequency is required. In some aspects, the optoelectronic device according to the proposed principle is used in optical data communication, particularly in the short and medium range with modulation frequencies larger than 1 GHz and particularly larger than 10 GHz.

SHORT DESCRIPTION OF THE DRAWINGS

Further aspects and embodiments in accordance with the proposed principle will become apparent in relation to the various embodiments and examples described in detail in connection with the accompanying drawings in which

Figures 1A to 1D show steps of a method for manufacturing an optoelectronic device in accordance with some aspects of the proposed principle;

Figures 2A to 2D show steps of a method for manufacturing a further embodiment of an optoelectronic device in accordance with some aspects of the proposed principle;

Figures 3a to 3D show steps of a method for manufacturing a further embodiment of an optoelectronic device in accordance with some aspects of the proposed principle;

Figures 4A to 4D show steps of a method for manufacturing a further embodiment of an optoelectronic device in accordance with some aspects of the proposed principle; and

Figures 5A to 5D show steps of a method for manufacturing a further embodiment of an optoelectronic device in accordance with some aspects of the proposed principle.

DETAILED DESCRIPTION

The following embodiments and examples disclose various aspects and their combinations according to the proposed principle. The embodiments and examples are not always to scale. Likewise, different elements can be displayed enlarged or reduced in size to emphasize individual aspects. It goes without saying that the individual aspects of the embodiments and examples shown in the figures can be combined with each other without further ado, without this contradicting the principle according to the invention. Some aspects show a regular structure or form. It should be noted that in practice slight differences and deviations from the ideal form may occur without, however, contradicting the inventive idea.

In addition, the individual figures and aspects are not necessarily shown in the correct size, nor do the proportions between individual elements have to be essentially correct. Some aspects are highlighted by showing them enlarged. However, terms such as "above", "over", "below", "under" "larger", "smaller" and the like are correctly represented with regard to the elements in the figures. So it is

possible to deduce such relations between the elements based on the figures.

Figures 1A to 1D illustrate steps of a method for manufacturing an optoelectronic device, in particular μ -LED 1 in accordance with the proposed principle. These steps are conducted in a similar manner in all the respective embodiments illustrated herein. However, certain variations and deviations from the illustrated steps can be implemented without deviating from the overall scope. In addition, although only vertical optoelectronic devices are illustrated herein, one will recognize that the proposed principle is not restricted to such devices. Rather, the respective contact areas can be arranged on the same side with a via leading through the active region and connecting the desired doped layer.

Figure 1A illustrates the epitaxial deposition of a semiconductor layer stack 2 on the respective growth substrate 11. The growth substrate 11 comprises an n-doped gallium arsenide layer, which acts as wafer substrate, on which the subsequent layers are epitaxially deposited. Furthermore, the n-doped gallium arsenide substrate may comprise a plurality of buffer layers to smooth and flattening its surface, such as to provide a substantially defect free surface.

In a subsequent step, an n-doped aluminum gallium arsenide layer 3 is epitaxially deposited on the surface of the growth substrate as a first semiconductor layer. The first layer 3 can comprise a doping distribution and/or a varying doping concentration based on the required needs. For example, the doping concentration closer to the growth substrate 11 may be larger than further away to improve the charge carrier injection into the aluminum gallium arsenide layer 3. Furthermore, the aluminum content of the first layer 3 may vary and also comprise a respective distribution over the thickness of the first layer 3. To this extent, first layer 3 can include one or more sublayers, in which the above-mentioned varying concentrations and distributions of dopants and Al content are implemented.

On top of the first layer 3, first $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 is arranged, where parameter x is greater than 0.5 and in particular greater than 0.9 and in particular greater than 0.97. First $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 can in particular comprise an Al content such that first $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 can easily be oxidized.

On top of the first $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 an undoped aluminum gallium arsenide first cladding layer 14 is deposited. The aluminum content of that layer may be similar to the aluminum content of the first layer 3 but can also vary to improve the charge carrier transport diffusion into the active region 5 epitaxially deposited on top of first cladding layer 14. The thickness of first cladding layer 14 is in the range between 10 nm and 50 nm. The purpose of first cladding layer 14 is to prevent diffusion of dopants from the first layer 3 and the first $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 respectively into the active region 5.

Active region 5 is deposited thereupon and comprises a pn-junction or a multi-quantum well structure in this embodiment. The multi-quantum well structure for example includes a plurality of barrier layers and quantum well layers, respectively, whereas the aluminum content for the barrier layers is slightly larger than the aluminum content of the respective quantum well layers. Consequently, a varying band gap in the semiconductor material of active region 5 is provided, trapping the charge carriers between the "valleys" of the bandgap.

Active region 5 is covered by another cladding layer 15 of aluminum gallium arsenide similar to the first cladding layer 14.

On top of the second cladding layer 15, second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 13 is arranged, where parameter x is greater than 0.5 and in particular greater than 0.9 and in particular greater than 0.97. Second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 13 can in particular comprise an Al content such that second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 13 can easily be oxidized.

On top of the second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 13 a p-doped layer 4 is deposited as a second semiconductor layer. Similar to the n-doped layer 3, the

doping concentration as well as the doping distribution of the p-doped aluminum gallium arsenide layer 4 may vary.

In this regard, both layers 3 and 4 may not only comprise aluminum gallium arsenide sublayers, but can also include one or more gallium arsenide sub-layers or aluminum gallium arsenide sub-layers with varying aluminum content. The purpose of these sublayers is to distribute the injected charge carriers across the overall area of the semiconductor layer stack 2 and will provide a continuous and equally distributed diffusion towards the active region.

The top surface of the second layer 4 is covered by a highly doped gallium arsenide contact layer 16. The contact layer 16 provides not only a connection to a conductive metal or a transparent conductive oxide, but also acts as the main emission surface in operation of the device 1 later on.

The first and the second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 and 13 are for example very thin layers containing aluminum gallium arsenide with a high aluminum content introduced between the first and second layer 3 and 4 and the respective cladding layer 14 and 15 or more generally between the first and second layer 3 and 4 and the active region 5. The aluminum content of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers comprise a very high aluminum content with parameter x larger than 0.9 and particularly larger than 0.97.

The next step of the proposed method is illustrated in Figure 1B. A not shown mask layer material is deposited on the p-doped gallium arsenide contact layer 16 and subsequently structured to form a central portion of the hard mask layer.

In a top view the central portion forms a circle, a rectangle, or any other polygon like a hexagon structure. Then, one or more mesa etching steps are performed to provide side surfaces 2c exposing the facets of active region 5 as well as the first and second layer 3 and 4, respectively. The results of the mesa etching process is illustrated in Figure 1B and can be achieved by several subsequent mesa etching steps. In a twostep process, the side surfaces 2c of the semiconductor

layer stack 2 and in particular of the active region 5 can in addition for example be cleaned and annealed after the first etching step to remove any plasma damages from the side surfaces 2c.

For example, in a first mesa etching step, material of contact layer 16, the p-doped aluminum gallium arsenide layer 4, the cladding layers 14 and 15, first and second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 and 13 as well as active region 5 is removed using a plasma etching process or any similar suitable way. The exposed surfaces are cleaned and annealed using NH_3 or other suitable gas. The cleaning reduces the damages and the non-radiative recombination centres after the mesa etching process to obtain more defined side surfaces 2c, preferably with only a small number of non-radiative recombination centres and thus a defined surface state.

To increase the charge carrier density within the active region 5, the semiconductor layer stack 2 is then processed as shown in Figure 1C. The semiconductor layer stack is therefore exposed to an oxygen containing atmosphere (shown by the two arrows), initiating an oxidation of the aluminum within the first and second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 and 13. Due to the oxygen containing atmosphere and the high Al content of layers 12 and 13, a portion of the layers 12 and 13 starting from the side surfaces 2c is oxidized resulting in oxidized thin portions of the layers 12 and 13 until a central region 10 of the semiconductor layer stack 2.

The oxidation results in a constrain of the conductivity of the first and second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer 12 and 13 to some smaller central portion thereof similar to apertures for the charge carriers, as indicated in Figure 1D. Hence, the charge density within the active region 5 inside the central region is significantly increased by the resulting aperture like structure, while at the same time for example in addition a defined amount of non-radiative recombination centres can be formed beneath and above the active region 5 as well as on the circumferential perimeter. By this, the rise and fall time of the optoelectronic device can be decreased by changing the charge carrier density within the active region.

To receive the optoelectronic device as shown in Figure 1D, the growth substrate 11 is removed, top and bottom contact elements 7a, 7b are provided on the top and bottom surface 2a, 2b of the semiconductor layer stack 2 and the side surfaces are passivated by means of a passivation layer 8. In the embodiment shown, the bottom contact element 7a is exemplarily arranged on the bottom surface 2a comprises the shape of a ring leaving the central region 10 of the semiconductor layer stack 2 uncovered.

The method according to the proposed principle follows the latter approach but can be combined with other measures to increase the charge density or the bandgap structure to provide a faster radiative recombination.

Figures 2A to 2D illustrate a respective embodiment thereof. The steps of providing a semiconductor layer stack 2 as well as mesa structuring the semiconductor layer stack 2 shown in Figures 2A and 2B thereby relate to the embodiment shown in Figures 1A and 1B but without providing the first and the second $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer. To increase the charge carrier density within the active region 5, the semiconductor layer stack 2 is then processed as shown in Figure 2C.

To increase the charge carrier density within the active region 5, a structured mask 9 is provided on the semiconductor layer stack 2 to conduct a quantum well intermixing (indicated by the vertical arrows) of the active region 5 in a region between the side surfaces 2c and the central region 10. Therefrom intermixed regions 17 of the active region 5 result having a larger bandgap than the active region within the central region 10 not being quantum well intermixed.

The intermixing results in a higher bandgap of the active region 5 outside the central region 10. Hence the charge density within the active region 5 inside the central region is significantly increased by the resulting aperture like structure, while at the same time a defined amount of non-radiative recombination centres is formed beneath and above the active region 5 as well as on the circumferential perimeter. By this, the rise and fall time of the optoelectronic device

can be decreased by changing the charge carrier density within the active region and increase the amount of non-radiative recombination centres in the intermixed region 17.

5 To receive the optoelectronic device as shown in Figure 2D, the growth substrate 11 is removed, top and bottom contact elements 7a, 7b are provided on the top and bottom surface 2a, 2b of the semiconductor layer stack 2 and the side surfaces 2c are passivated by means of a passivation layer 8. In the embodiment shown, the bottom contact
10 element 7a is exemplarily arranged on the bottom surface 2a comprises the shape of a ring leaving the central region 10 of the semiconductor layer stack 2 uncovered.

Figures 3A to 3D illustrate a further embodiment a current confinement
15 to the central region of an optoelectronic device 1. The steps of providing a semiconductor layer stack 2 as well as mesa structuring the semiconductor layer stack 2 shown in Figures 3A and 3B thereby relate to the embodiment shown in Figures 2A and 2B with the difference of providing an active region with a simple pn-junction and not a
20 quantum well or multi quantum well layer. This is however understood to be exemplary and can also be in the same way as shown in Figures 2A and 2B. To increase the charge carrier density within the active region 5, the semiconductor layer stack 2 is then processed as shown in Figure 3C.

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To increase the charge carrier density within the active region 5, a structured mask 9 is provided on the semiconductor layer stack 2 to conduct an ion bombardment of the side surfaces 2c (indicated by the arrows) of the semiconductor layer stack 2 in a region between the side
30 surfaces 2c and the central region 10. Therefrom ion implanted regions 18 of semiconductor layer stack 2 result having semi insulating properties and in particular a worse conductivity than the semiconductor layer stack 2 within the central region 10. In addition, the ion bombardment can cause the active region outside the central
35 region 10 having a larger bandgap than the active region 5 within the central region 10.

The ion bombardment results in a worse conductivity of the layers adjacent to the active region 5 as well as a higher bandgap of the active region 5 outside the central region 10. Hence the charge density within the active region 5 inside the central region is significantly increased by the resulting aperture like structure, while at the same time a defined amount of non-radiative recombination centres is formed beneath and above the active region 5 as well as on the circumferential perimeter. By this, the rise and fall time of the optoelectronic device can be decreased by changing the charge carrier density within the active region and increase the amount of non-radiative recombination centres in the intermixed region 17.

To receive the optoelectronic device as shown in Figure 3D, the growth substrate 11 is removed, and top and bottom contact elements 7a, 7b are provided on the top and bottom surface 2a, 2b of the semiconductor layer stack 2. In the embodiment shown, the bottom contact element 7a is exemplarily arranged on the bottom surface 2a comprises the shape of a ring leaving the central region 10 of the semiconductor layer stack 2 uncovered.

Figures 4A to 4D illustrate a further embodiment a current confinement to the central region of an optoelectronic device 1. The steps of providing a semiconductor layer stack 2 as well as mesa structuring the semiconductor layer stack 2 shown in Figures 4A to 4C thereby relate to the embodiment shown in Figures 3A and 3B with the difference that the second layer 4 as well as the contact layer 16 is provided selectively on the active region 5 using a structured mask 9 only in the central region 10 of the semiconductor layer stack 2. This step can in this embodiment already be understood as the step, by means of which the charge carrier density within the active region 5 is increased. The semiconductor layer stack 2 is then mesa structured as shown in Figure 4C to receive side surfaces 2c of the semiconductor layer stack 2.

The selective growth results in current feed into the active region 5 only in the central region 10. Hence the charge density within the active region 5 inside the central region is significantly increased

by the resulting aperture like structure. By this, the rise and fall time of the optoelectronic device can be decreased by changing the charge carrier density within the active region 5.

5 To receive the optoelectronic device as shown in Figure 4D, the growth substrate 11 is removed, top and bottom contact elements 7a, 7b are provided on the top and bottom surface 2a, 2b of the semiconductor layer stack 2 and the side surfaces 2c are passivated by means of a passivation layer 8. In the embodiment shown, the bottom contact
10 element 7a is exemplarily arranged on the bottom surface 2a comprises the shape of a ring leaving the central region 10 of the semiconductor layer stack 2 uncovered.

Figures 5A to 5D illustrate a further embodiment a current confinement
15 to the central region of an optoelectronic device 1. The steps of providing a semiconductor layer stack 2 as well as mesa structuring the semiconductor layer stack 2 shown in Figures 5A and 5B thereby relate to the embodiment shown in Figures 3A and 3B with the difference that by means of the mesa structuring using a structured mask 9, an
20 already smaller semiconductor layer stack 2 is pixelated with smaller lateral dimensions compared to aforementioned embodiments.

By this the charge carrier density within the active region 5 can be increased compared to a larger sized layer stack 2 with larger lateral
25 dimensions and assuming the same current is applied to the active region 5. To now increase the efficiency of the optoelectronic device regrowth layers 6 are provided along the side surfaces 2c of the semiconductor layer stack 2. The regrowth layers 6 can for example be a structure of alternating layers having different doping types such
30 as for example a pnp or a npn structure covering the side surfaces 2c of the semiconductor layer stack 2. Such an embodiment can in particular also be suitable in combination with any of aforementioned aspects for current confinement within the semiconductor layer stack 2. This results in a higher carrier concentration in the area of radiative
35 recombination resulting in higher recombination rates and, thus, higher switching speeds of the optoelectronic device 1. The regrowth layers 6 thereby act as current confinement structure to guide the current

through the active region 5 and preserve the side surfaces 2c from unwanted effects.

To receive the optoelectronic device as shown in Figure 5D, the growth
5 substrate 11 is removed, and top and bottom contact elements 7a, 7b
are provided on the top and bottom surface 2a, 2b of the semiconductor
layer stack 2. In the embodiment shown, the bottom contact element 7a
is exemplarily arranged on the bottom surface 2a comprises the shape
of a ring leaving the central region 10 of the semiconductor layer
10 stack 2 uncovered.

LIST OF REFERENCES

	1	optoelectronic device, μ -LED
	2	layer stack
5	2a	top surface
	2b	bottom surface
	2c	side surface
	3	layer
	4	layer
10	5	active region
	6	regrowth layer
	7a	contact element
	7b	contact element
	8	passivation layer
15	9	mask
	10	central region
	11	growth substrate
	12	$\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer
	13	$\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer
20	14	cladding layer
	15	cladding layer
	16	contact layer
	17	intermixed region
	18	implanted region
25		

CLAIMS

1. A μ -LED (1) comprising:

a semiconductor layer stack (2) having a first layer (3) of a first doping type, a second layer (4) of a second doping type, and an active region (5) arranged between the first and the second layer (3, 4);

wherein the semiconductor layer stack (2) comprises a bottom surface (2a) and a top surface (2b) as well as mesa structured side surfaces (2c) connecting the top and bottom surface (2a, 2b);

wherein the semiconductor layer stack (2) comprises a central region (10) with a lateral dimension which is less than one half or less than three fourth of a lateral dimension of the semiconductor layer stack (2);

wherein the semiconductor layer stack (2) comprises a material including at least one of phosphide and arsenide; and

wherein a current path from the first layer (3) to the second layer (4) through the active region (5) is limited to the central region (10).

2. The μ -LED according to claim 1, wherein the semiconductor layer stack (2) comprises a partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer (12, 13) arranged between the first layer (3) and the active region (5) and/or the second layer (4) and the active region (5),

wherein parameter x is greater than 0.5 and in particular greater than 0.9 and in particular greater than 0.97,

wherein the oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) ranges from the side surfaces (2c) until the central region (10) and the central region (10) of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) remains substantially unoxidized, and

wherein optionally the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) comprises a thickness in the range of 5 nm to 20 nm; and/or

wherein optionally the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) is doped.

3. The μ -LED according to claim 1 or 2, wherein the active region (5) comprises an intermixed, in particular quantum well intermixed, region (17) outside the central region (10) with a larger bandgap than the active region (5) within the central region (10).
- 5
4. The μ -LED according to any one of claims 1 to 3, wherein the active region (5) and in particular the semiconductor layer stack (2) comprises an ion implanted region (18) outside the central region (10) having a worse conductivity and/or larger bandgap than the
- 10 the semiconductor layer stack (2) within the central region (10).
5. The μ -LED according to any one of claims 1 to 4, wherein the first and/or the second layer (3, 4) is limited to the central region
- 15 (10).
6. The μ -LED according to any one of claims 1 to 5, wherein the semiconductor layer stack (2) comprises a first and a second, in particularly undoped, cladding layer (14, 15) directly adjacent to
- 20 the active region (5).
7. The μ -LED according to any one of claims 1 to 6, wherein the active region (5) comprises at least one of:
- At least one quantum well layer comprising a doping level in the

25 range between $1 \times 10^{16} \text{ 1/cm}^3$ and $1 \times 10^{18} \text{ 2/cm}^3$;

 - At least two barrier layers encompassing at least one quantum well layer, said at least two barrier layers comprising a doping level in the range between $1 \times 10^{16} \text{ 1/cm}^3$ and $1 \times 10^{18} \text{ 1/cm}^3$;
 - A plurality of quantum dots.
- 30
8. The μ -LED according to any one of claims 1 to 7, further comprising at least one regrowth layer (6) covering the side surfaces (2c) and/or optionally a passivation layer (8) arranged on exposed surfaces of the regrowth layer(s) (6) and/or exposed surfaces of
- 35 the semiconductor layer stack (2).

9. The μ -LED according to any one of claims 1 to 8, further comprising a first contact element (7a) arranged on the first layer (3) and/or a second contact element (7b) arranged on the second layer (4).

10. The μ -LED according to claim 9, wherein, when viewed onto the bottom surface (2a), a central region of the first layer (3) remains free of the first contact element (7a), the first contact element (7a) in particular comprising the form of a ring.

11. The μ -LED according to any one of the preceding claims, wherein the central region (10) of the active region (5) comprises a lateral dimension of less than the diffusion length of the material system of the active region (5).

12. The μ -LED according to any one of the preceding claims, wherein the μ -LED (1) is configured to have a switching on and/or off time in the range of 0,1 ns to 10ns.

13. Use of a μ -LED (1) according to any one of the preceding claims as a means for optical data communication, in particular short distance communication of less than 10m.

14. A method for manufacturing μ -LED (1), comprising the steps:

Providing a semiconductor layer stack (2) having a first layer (3) of a first doping type, a second layer (4) of a second doping type, and an active region (5) arranged between the first and the second layer (3, 4) with the semiconductor layer stack (2) comprising a material including at least one of phosphide and arsenide;

Structuring the semiconductor layer stack (2) such that the semiconductor layer stack (2) comprises side surfaces (2c) connecting a top and a bottom surface (2a, 2b) of the semiconductor layer stack (2);

Processing the semiconductor layer stack (2) in such a way that a central region (10) with a lateral dimension which is less than one half of a lateral dimension of the semiconductor layer stack (2) is formed and such that a current path from the first

layer (3) to the second layer (4) through the active region (5) is limited to that central region (10).

15. Method according to claim 14, wherein the step of providing a semiconductor layer stack (2) comprises:

- Depositing an $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer (12, 13) arranged between the first layer (3) and the active region (5) and/or between the second layer (13) and the active region (5), wherein parameter x is greater than 0.5 and in particular greater than 0.9 and in particular greater than 0.97; and wherein
- optionally the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) comprises a thickness in the range of 5 nm to 20 nm; and/or wherein
- optionally the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) is doped.

16. Method according to claim 15, wherein the step of processing the semiconductor layer stack (2) comprises

partially oxidizing the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) such that the oxidized portion of the partially oxidized $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) ranges from the side surfaces (2c) until the central region (10) and such that the portion of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) (12, 13) within the central region (10) remains substantially unoxidized.

17. Method according to any one of claims 14 to 16, wherein the step of processing the semiconductor layer stack (2) comprises

implanting ions into at least the active region (5) and in particular the semiconductor layer stack (2) outside the central region (10) forming an ion implanted region (18) outside the central region (5) having a worse conductivity and/or larger bandgap than the active region (5) within the central region (10) and in particular the semiconductor layer stack (2) within the central region (10).

18. Method according to any one of claims 14 to 17, wherein the step of processing the semiconductor layer stack (2) comprises

intermixing, in particular quantum well intermixing, the active region (5) outside the central region (10) forming an intermixed

region (17) of the active region (5) with a larger band gap than the active region (5) within the central region (10).

19. Method according to any one of claims 14 to 18, wherein the step of
5 processing the semiconductor layer stack (2) comprises structuring the first and/or the second layer (3, 4) such that the first and/or second layer (3, 4) is limited to the central region (10).

10 20. Method according to any one of claims 14 to 19, further comprising a step of regrowing at least one regrowth layer (6) on the side surfaces (2c) and/or optionally growing a passivation layer (8) on exposed surfaces of the regrowth layer(s) (6) and/or exposed surfaces of the semiconductor layer stack (2).

15 21. Method according to any one of claims 14 to 20, further comprising a step of providing a first contact element (7a) on the first layer (3) and/or a second contact element (7b) on the second layer (4).

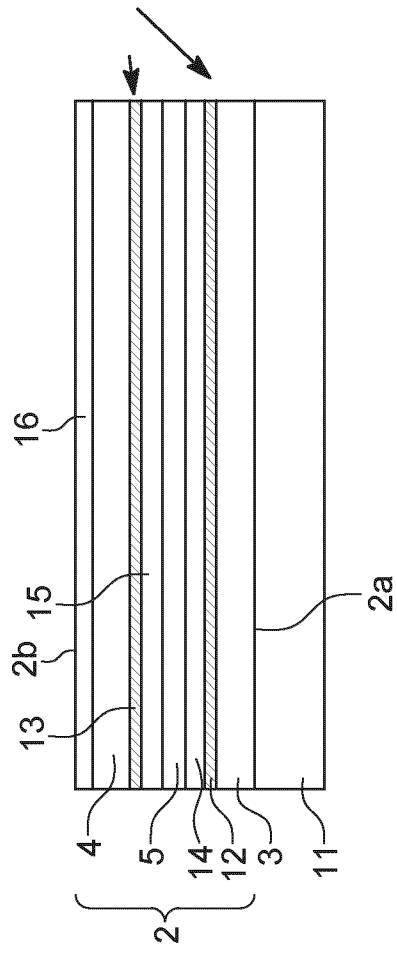


FIG. 1A

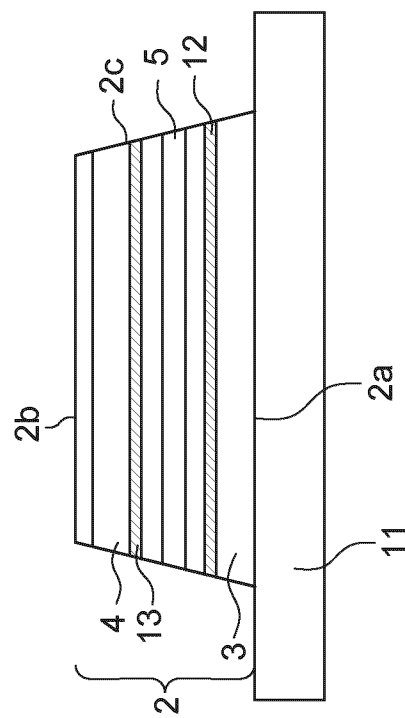


FIG. 1B

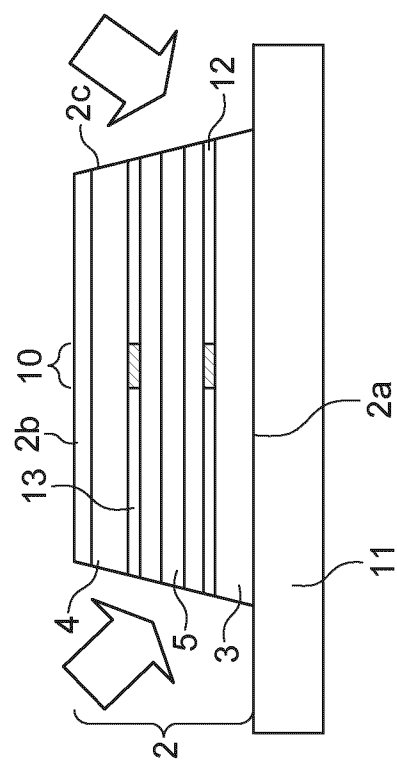


FIG. 1C

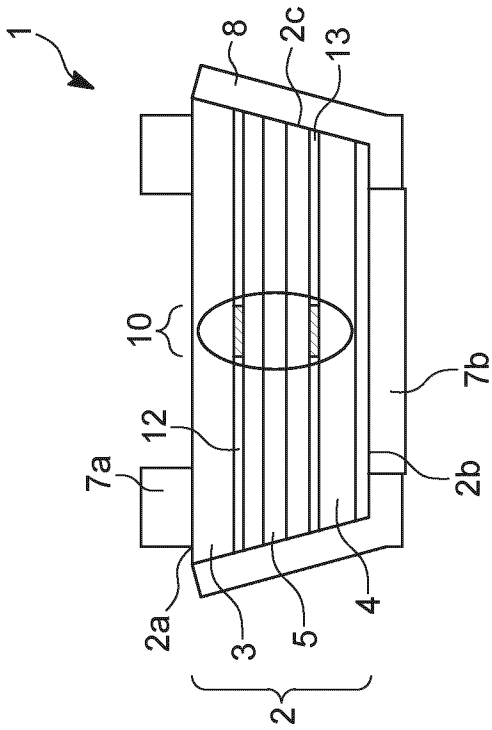


FIG. 1D

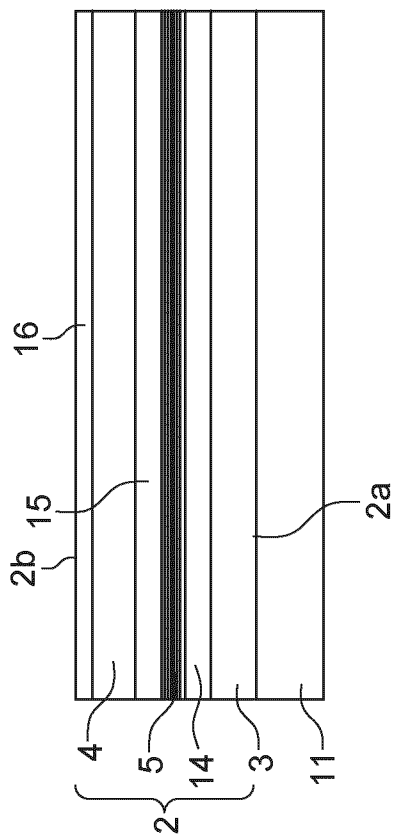


FIG. 2A

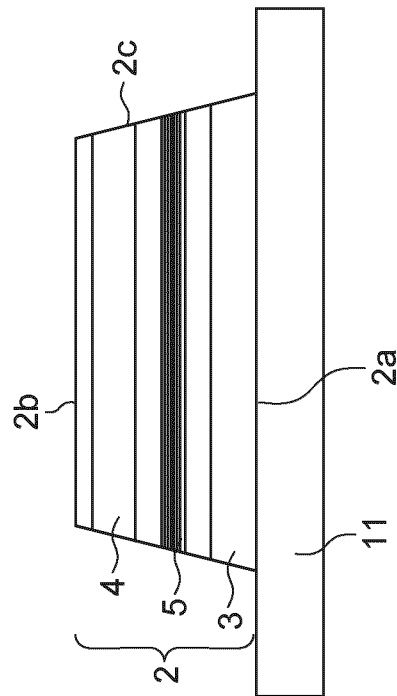


FIG. 2B

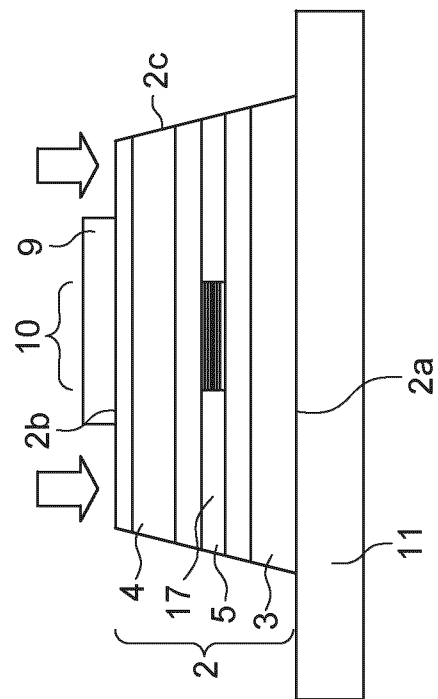


FIG. 2C

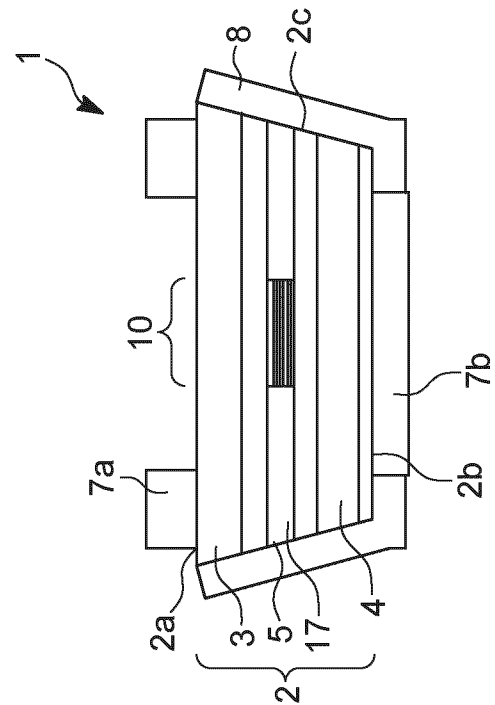


FIG. 2D

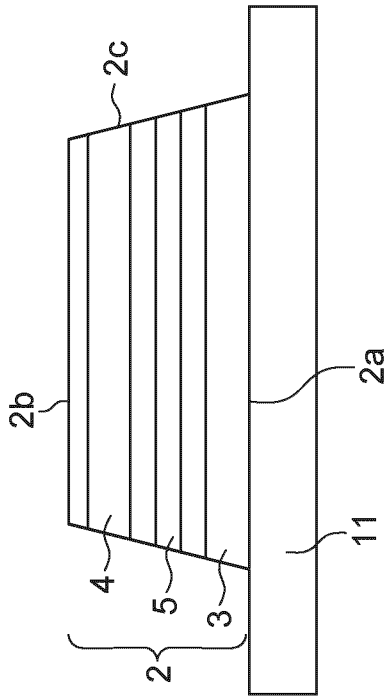


FIG. 3A

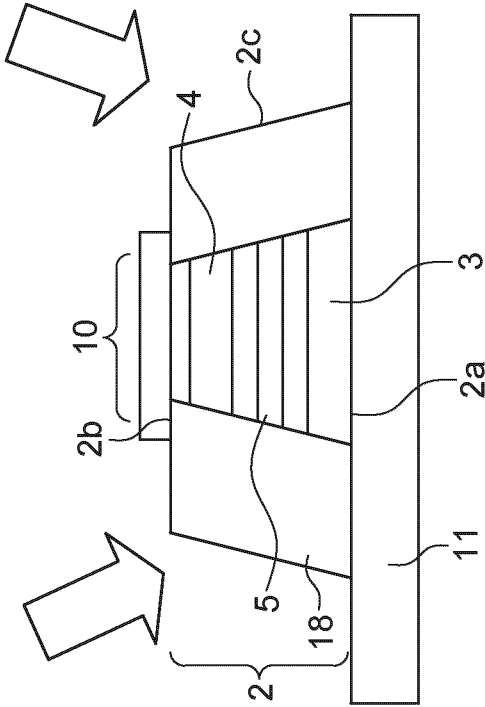


FIG. 3B

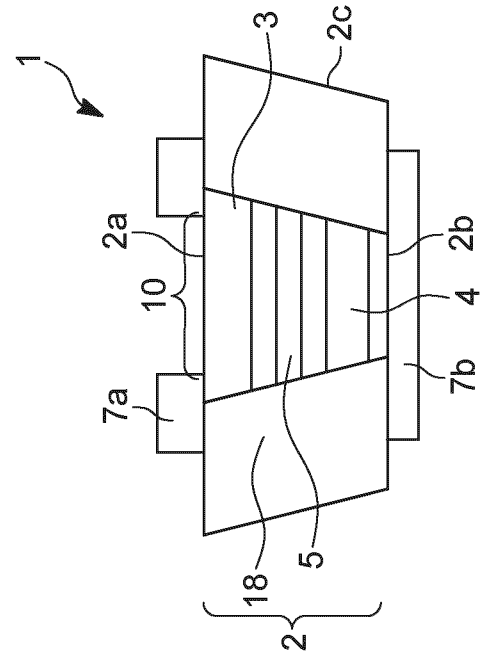


FIG. 3C

FIG. 3D

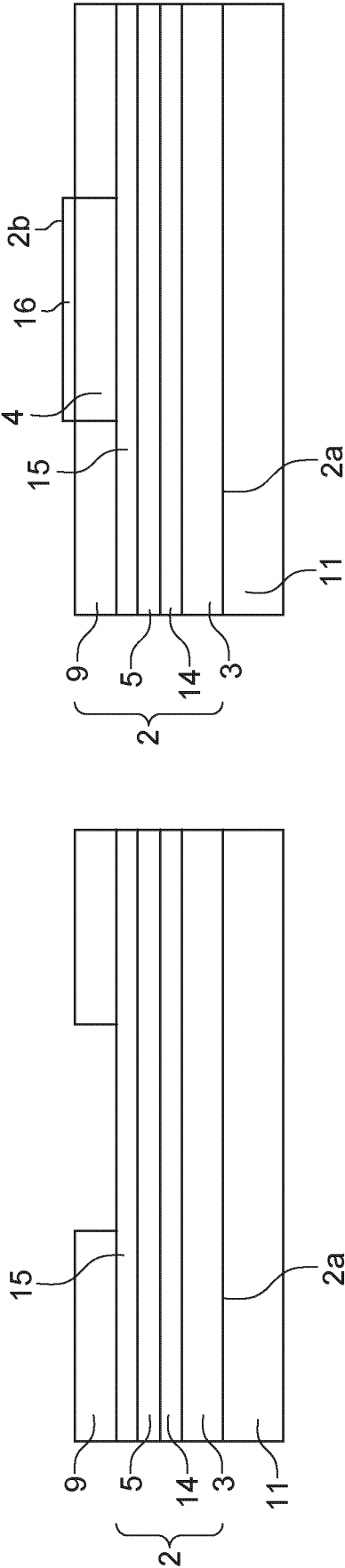


FIG. 4B

FIG. 4A

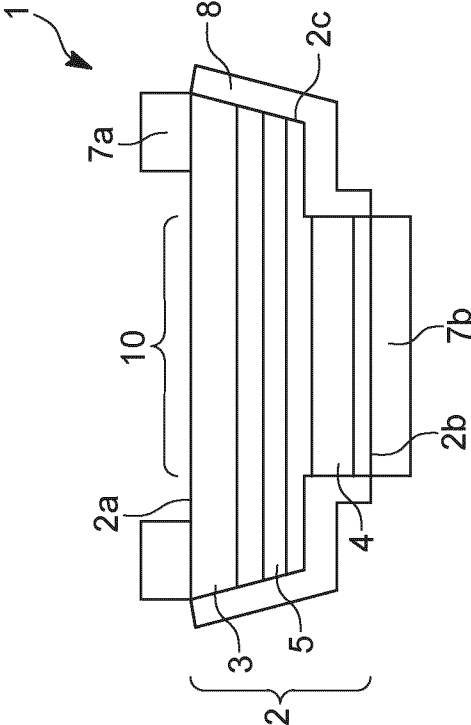


FIG. 4D

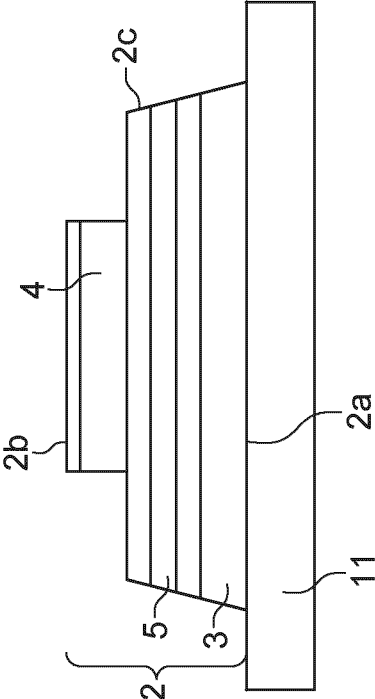


FIG. 4C

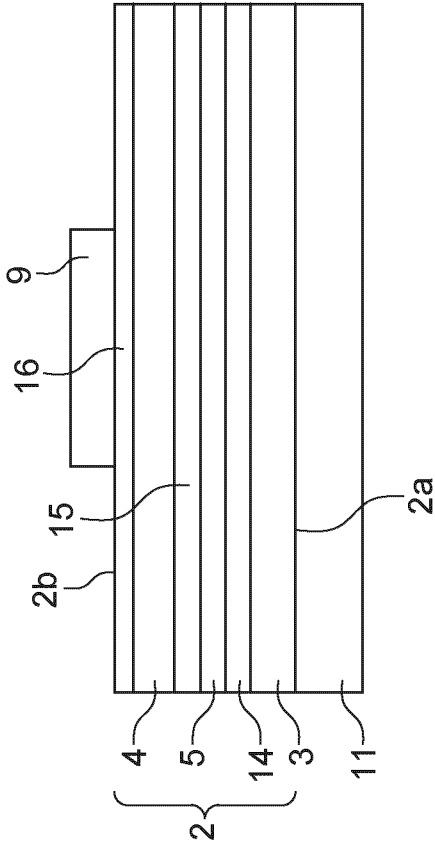


FIG. 5A

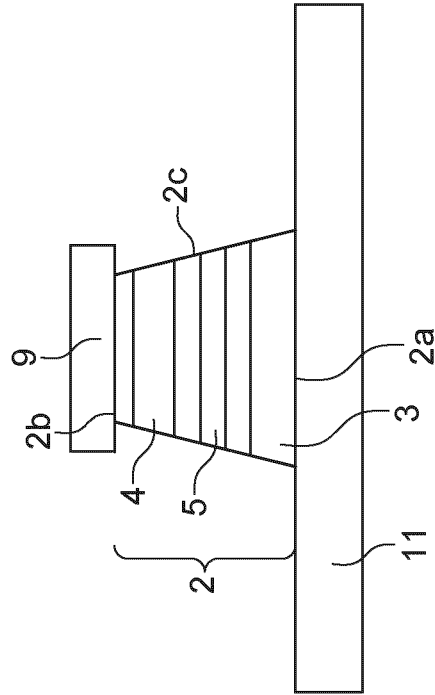


FIG. 5B

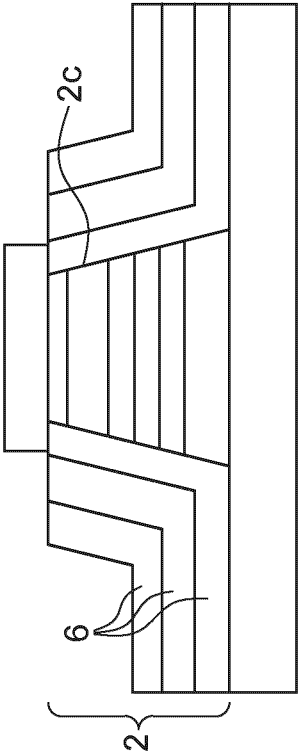


FIG. 5C

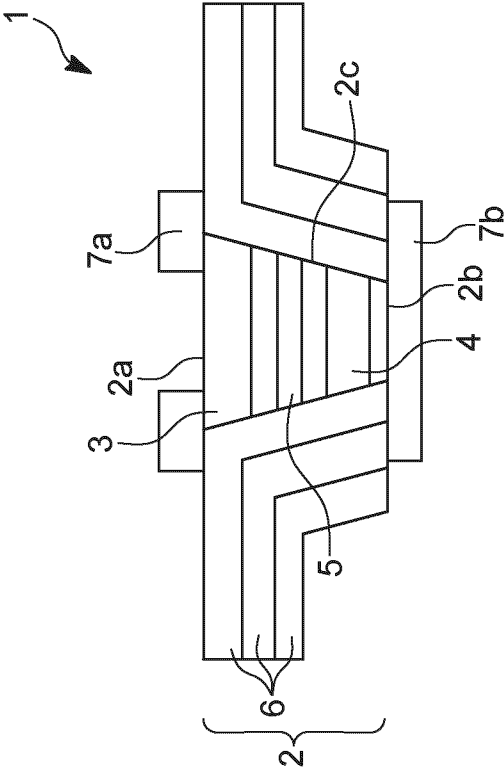


FIG. 5D

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2024/065331

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L33/14 H01L33/44 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2020/052158 A1 (BOUR DAVID P [US] ET AL) 13 February 2020 (2020-02-13) paragraphs [0056] - [0057], [0066], [0087] - [0091], [0098]; figures 1-14 -----	1,3-21
X	US 2005/040415 A1 (KISH FRED A [US] ET AL) 24 February 2005 (2005-02-24)	1,2,9,21
A	paragraphs [0015], [0038] - [0060]; figures 1-11 -----	16
X	US 2007/153853 A1 (CHUA CHRISTOPHER L [US] ET AL) 5 July 2007 (2007-07-05) paragraph [0049]; figure 5 -----	1,9,21
X	US 2013/200492 A1 (DOSANJH SUKHJIBAN [GB] ET AL) 8 August 2013 (2013-08-08) paragraphs [0013], [0052] - [0054]; figures 1-7 ----- -/-	1
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 13 September 2024		Date of mailing of the international search report 24/09/2024
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Chin, Patrick

INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LU TINGWEI ET AL: "High-speed visible light communication based on micro-LED: A technology with wide applications in next generation communication", OPTO-ELECTRONIC SCIENCE, [Online] vol. 1, no. 12, 29 December 2022 (2022-12-29), pages 220020-220020, XP093195927, ISSN: 2097-0382, DOI: 10.29026/oes.2022.220020 Retrieved from the Internet: URL:https://www.ojournal.org/data/article/oes/preview/pdf/oes-2022-0020-WuTingzhu.pdf> [retrieved on 2024-08-16] the whole document -----	12,13

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2024/065331

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2020052158 A1	13-02-2020	CN 108369974 A	03-08-2018
		EP 3357096 A1	08-08-2018
		JP 6781251 B2	04-11-2020
		JP 2018533847 A	15-11-2018
		KR 20180074726 A	03-07-2018
		KR 20190137941 A	11-12-2019
		US 2018374991 A1	27-12-2018
		US 2020052158 A1	13-02-2020
		WO 2017112490 A1	29-06-2017
US 2005040415 A1	24-02-2005	US 2003173571 A1	18-09-2003
		US 2004235213 A1	25-11-2004
		US 2005040415 A1	24-02-2005
		US 2005145863 A1	07-07-2005
		US 2005151144 A1	14-07-2005
US 2007153853 A1	05-07-2007	NONE	
US 2013200492 A1	08-08-2013	CN 103125054 A	29-05-2013
		EP 2526593 A2	28-11-2012
		JP 5746222 B2	08-07-2015
		JP 2013519241 A	23-05-2013
		KR 20120123123 A	07-11-2012
		US 2013200492 A1	08-08-2013
		WO 2011098797 A2	18-08-2011