



- (51) International Patent Classification:
H01L 21/336 (2006.01) *H01L 21/31* (2006.01)
H01L 29/78 (2006.01)
- (21) International Application Number:
PCT/US201 1/063433
- (22) International Filing Date:
6 December 201 1 (06.12.201 1)
- (25) Filing Language: English
- (26) Publication Language: English
- (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).
- (72) Inventors; and
- (75) Inventors/ Applicants (for US only): PRADHAN, Sameer [IN/US]; 17923 NW Sylvania Lane, Portland, Oregon 97229 (US). LUCE, Jeanne [US/US]; 4134 NE Azalea Street, Hillsboro, Oregon 97124 (US).
- (74) Agent: WINKLE, Robert; Winkle, PLLC, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on nextpage]

(54) Title: INTERLAYER DIELECTRIC FOR NON-PLANAR TRANSISTORS

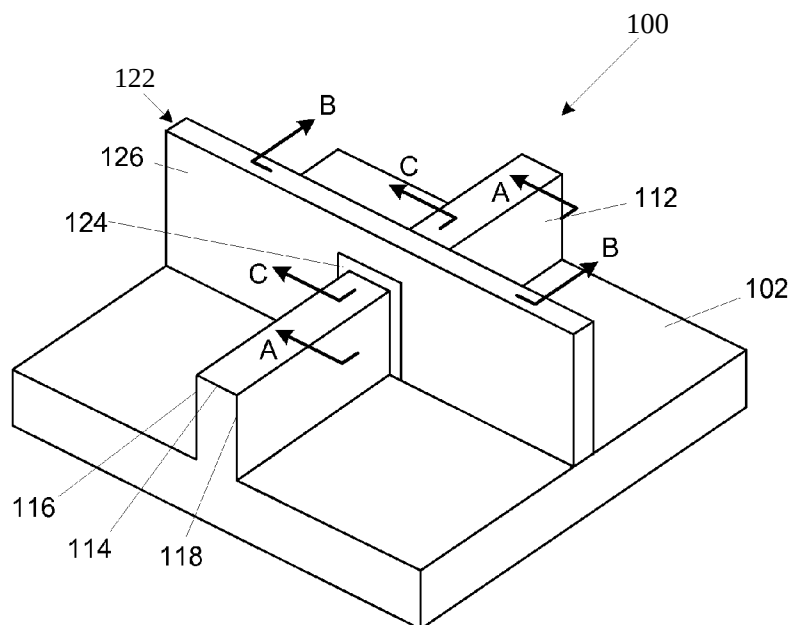


FIG. 1

(57) Abstract: The present description relates the formation of a first level interlayer dielectric material layer within a non-planar transistor, which may be formed by a spin-on coating technique followed by oxidation and annealing. The first level interlayer dielectric material layer may be substantially void free and may exert a tensile strain on the source/drain regions of the non-planar transistor.

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

Published:

— *-with international search report (Art. 21(3))*

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

INTERLAYER DIELECTRIC FOR NON-PLANAR TRANSISTORS

BACKGROUND

5 Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of a first level interlayer dielectric material layer in a non-planar transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be
15 described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

20 FIG. 2 illustrates side cross-sectional views of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates side cross-sectional views of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

25 FIG. 4 illustrates side cross-sectional views of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates side cross-sectional views of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal
5 dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of an adhesion layer formed on the structure
10 of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of a first interlayer dielectric material layer deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 10, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the first interlayer dielectric material layer
15 of FIG. 11 being oxidized and annealed, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-section view of the structure of FIG. 12 wherein a portion of the first interlayer dielectric material layer is densified by the oxidization and annealing of FIG. 13, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of the structure of FIG. 13 after planarizing
20 the first interlayer dielectric material layer to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of the structure of FIG. 15 after the
25 formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 16, according to an embodiment of the present description.

FIG. 18 illustrates a side cross-sectional view of the structure of FIG. 17 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of the structure of FIG. 18 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of the structure of FIG. 19 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of the structure of FIG. 20 after the removal of excess capping dielectric material to form a capping structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of a second interlayer dielectric material layer deposited over the first interlayer dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 21, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 22, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 23, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of the structure of FIG. 24 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 26 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 25, according to an embodiment of the present description.

FIG. 27 illustrates a side cross-sectional view of the structure of FIG. 25 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

FIG. 28 illustrates a computing device, according to one implementation of the present description.

DETAILED DESCRIPTIONS the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate

material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of a first level interlayer dielectric material layer within a non-planar transistors, which may be formed by a spin-on
5 coating technique followed by oxidation and annealing. The first level interlayer dielectric material layer may be substantially void free and may exert a tensile strain on the source/drain regions of the non-planar transistor.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an
10 embodiment of the present disclosure, the microelectronic substrate 102 may be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

15 The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by
20 forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

25 The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium
30 oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-

known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 126 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrode 126 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing portions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art. In still another embodiment, the source and drain regions may be formed by epitaxially growing doped or undoped strain layers on the fins 112.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrated in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a portion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art,

including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form a pair of gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a source region 150a and a drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the source region 150a and the drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of N-type or P-type ion dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions or N-type ions, collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the source region 150a and the drain region 150b may be formed in place of the removed portions. In still another embodiment, the source and drain regions may be formed by epitaxially growing doped or undoped strain layers on the fins 112. The source region 150a and the drain region will hereinafter be referred to collectively as "source/drain region 150". As will be understood to those skilled in the art, transistors having P-type source and drains are referred to as "PMOS" or "p-channel metal-oxide-semiconductor" transistors, and transistors having N-type source and drains are referred to as "NMOS" or "n-channel metal-oxide-semiconductor" transistors.

As shown in FIG. 10, an adhesion liner 152, such as silicon dioxide, may be conformally deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor

fin 112, and the microelectronic substrate 102. The adhesion line 152 may provide a sufficient adhesion between a subsequently formed interlayer dielectric material layer, and the structure of FIG. 9, i.e., the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102.

5 As shown in FIG. 11, a first interlayer dielectric material layer 154 may be formed on the adhesion liner 152 with a spin-on coating technique, which may be used to apply a substantially uniform thin film to a substrate. In one embodiment of the present description, an excess amount of interlayer dielectric material may be deposited on the adhesion liner 152. The microelectronic substrate 102 may then be rotated, generally at a high speed, to spread the interlayer dielectric material across the microelectronic substrate 102 by centrifugal force; thus, forming the first interlayer dielectric material layer 154. The spin-on coating technique may have the capability
10 scale to relatively pitch sizes, while still achieving effective gap fill (e.g. little or substantially no void formation) even with high aspect ratio structures.

As shown in FIG. 12, the first interlayer dielectric material layer 154 may be oxidized
15 follow by an annealing (the oxidation and annealing steps are illustrated as arrows 156). Although the oxidation and annealing steps are illustrated in a single drawing with common arrows 156, this is merely for conciseness in the illustrations. It is understood that the oxidation and annealing steps can be separated by one or more processing steps.

In one embodiment, the oxidation may be performed in a vertical diffusion furnace at
20 about 410 degrees Celsius in about a 93% steam atmosphere for about 2 hours. The oxidation may drive out solvent from the first interlayer dielectric material layer 154 and may result in a volume shrinkage of the first interlayer dielectric material layer 154 of between about 10% and 12%. This shrinkage may exert a tensile strain and has been shown to increase drive currents of NMOS tri-gate transistors up to about 7% due to channel mobility enhancement, as
25 will be understood to those skilled in the art. In one embodiment, the annealing may be achieved by a two step anneal in a high density plasma chamber with a helium gas (or other such inert gas) atmosphere. The first step may comprise powering up RF electrodes within the high density plasma chamber, such as top and side electrodes, to about 16kW for a time duration of about six (6) minutes. The second step may comprise powering up the high density plasma chamber
30 RF electrodes, such as top and side electrodes, to about 6kW for a time duration of about two (2) minutes.

As shown in FIG. 13, a portion 158 of the first interlayer dielectric 154 may be densified as a result of the oxidation and annealing step previously described. The densified dielectric

portion 158 may assist in protecting the first interlayer dielectric 154 during downstream processing.

As shown in FIG. 14, the first interlayer dielectric layer 154 may be planarized to expose the sacrificial gate top surface 148. The planarization of the first dielectric material layer 154
5 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP). As shown in FIG. 14, a portion of the densified dielectric portion 158 may remain after planarization.

As shown in FIG. 15, the sacrificial gate 136 of FIG. 14 may be removed to form a gate trench 164. The sacrificial gate 136 may be removed by any technique known in the art, such as
10 a selective etch. As shown in FIG. 16, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed. The materials and methods of forming the gate dielectric 124 have been previously discussed.

As shown in FIG. 17, a conductive gate material 166 may be deposited in the gate trench 164, and excess conductive gate material 166 (e.g. conductive gate material 166 not within the
15 gate trench 166 of FIG. 16) may be removed to form the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 18. The materials and methods of forming the gate electrode 126 have been previously discussed. The removal of the excess conductive gate material 166 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 19, a portion of the non-planar transistor gate electrode 126 of FIG. 18
20 may be removed to form a recess 168 and a recessed non-planar transistor gate 172. The removal may be accomplished by any known technique, including but not limited to wet or dry etching. In one embodiment, the formation of the recess may result from a combination of a dry etch and a wet etch.

As shown in FIG. 20, a capping dielectric material 174 may be deposited to fill the recess 168 of FIG. 19. The capping dielectric material 174 may be any appropriate material, including
25 but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate deposition technique. The capping dielectric material 174 may be planarized to remove excess capping dielectric material 174 (e.g. capping dielectric material 174 not within
30 the recess of FIG. 19) to form a capping dielectric structure 176 on the recessed non-planar transistor gate 172 and between a gate spacers 144, as shown in FIG. 21. The removal of the excess capping dielectric material 174 may be achieved by any technique known in the art,

including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 22, a second interlayer dielectric layer 178 may be deposited over the first dielectric material layer 154, the gate spacers 144, and the capping dielectric structure 176. The second interlayer dielectric layer 178 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As shown in FIG. 23, an etch mask 182 may be patterned with at least one opening 184 on the second interlayer dielectric layer 178, such as by well known lithographic techniques.

As shown in FIG. 24, a contact opening 192 may be formed through the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 by etching through the etch mask opening 184 of FIG. 23 to expose a portion of the source/drain region 150. The etch mask 182 of FIG. 24 may be removed thereafter, as shown in FIG. 25. In one embodiment, the first interlayer dielectric layer 154 and the second dielectric material layer 178 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 176, such that the etching of the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 may be selective to the gate spacers 144 and the capping dielectric structure 176 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 26, a conductive contact material 196 may be deposited in the contact opening 192 of FIG. 25. The conductive contact material 196 may include, but is not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. It is understood that various adhesion layers, barrier layers, silicide layers, and/or conductive layers may be conformally disposed or formed in the contact opening 192 of FIG. 25 prior to the deposition of the conductive contact material 196.

As shown in FIG. 27, excess conductive contact material 196 of FIG. 26 (e.g. conductive contact material 196 not within the contact opening 192 of FIG. 24) may be removed to form a source/drain contact 198. The removal of the excess conductive contact material 196 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 differs from dielectric material of both the gate spacers

144 and the capping dielectric structure 176, such that the etching of the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 may be selective to the gate spacers 144 and the capping dielectric structure 176 (i.e. etches faster). Thus, the recessed non-planar transistor 172 is protected during the formation of the contact opening 192. This allows for the
5 formation of a relatively large sized source/drain contact 198, which may increase the transistor drive current performance, without the risk of shorting between the source/drain contact 198 and the recessed non-planar transistor gate 172.

FIG. 28 illustrates a computing device 1000 in accordance with one implementation of the present description. The computing device 1000 houses a board 1002. The board 1002 may
10 include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006. The processor 1004 is physically and electrically coupled to the board 1002. In some implementations the at least one communication chip 1006 is also physically and electrically coupled to the board 1002. In further implementations, the communication chip 1006 is part of the processor 1004.

15 Depending on its applications, computing device 1000 may include other components that may or may not be physically and electrically coupled to the board 1002. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio
20 codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to
25 describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE
30 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006.

For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

5 The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some implementations of the present description, the integrated circuit die of the processor includes one or more devices, such as non-planar transistors that are formed in accordance with implementations of the present description. The term "processor" may refer to any device or portion of a device that processes electronic data
10 from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

 The communication chip 1006 also includes an integrated circuit die packaged within the communication chip 1006. In accordance with another implementation of the present description, the integrated circuit die of the communication chip includes one or more devices,
15 such as non-planar transistors that are formed in accordance with implementations of the present description.

 In further implementations, another component housed within the computing device 1000 may contain an integrated circuit die that includes one or more devices, such as non-planar transistors that are formed in accordance with implementations of the present description.

20 In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1000 may be any other
25 electronic device that processes data.

 It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-28. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

 Having thus described in detail embodiments of the present invention, it is understood that
30 the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

What is claimed is:

1. A method of fabricating a microelectronic transistor, comprising:
forming a transistor gate including a gate electrode adjacent a substrate and a pair of
gates spacers on opposing sides of the gate electrode;
5 forming a source/drain region;
forming a first interlayer dielectric material layer adjacent the source/drain region and
adjacent at least one gate spacer;
oxidizing the first interlayer dielectric material layer; and
annealing the first interlayer dielectric material layer.
10
2. The method of claim 1, wherein forming the first interlayer dielectric material layer
comprises depositing the first interlayer dielectric material layer with a spin-on coating
technique.
- 15 3. The method of claim 1, further including forming an adhesion liner adjacent the
source/drain region and adjacent at least one gate spacer, prior to forming the first interlayer
dielectric material layer.
4. The method of claim 1, wherein oxidizing the first interlayer dielectric material layer
20 comprises heating the first interlayer dielectric material layer in a steam atmosphere.
5. The method of claim 4, wherein heating the first interlayer dielectric material layer in a
steam atmosphere comprises heating the first interlayer dielectric material layer to a temperature
of about 410 degrees Celsius in about a 93% steam atmosphere for about 2 hours.
25
6. The method of claim 1, wherein annealing the first interlayer dielectric material layer
comprises annealing the first interlayer dielectric material layer with high density plasma in an
inert atmosphere.
- 30 7. The method of claim 1, wherein oxidizing and annealing the first interlayer dielectric
material layer shrinks the first interlayer dielectric material layer to exert a tensile strain on the
source/drain region.
8. A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;
depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;
forming non-planar transistor gate spacers from a portion of the dielectric material layer
5 adjacent the sacrificial non-planar transistor gate;
forming a source/drain region;
removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;
forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;
10 depositing conductive gate material within the gate trench;
removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;
forming a capping dielectric structure within the recess;
forming a first interlayer dielectric material layer over the source/drain region, the non-
15 planar transistor gate spacers, and the capping dielectric structure; and
oxidizing the first interlayer dielectric material layer; and
annealing the first interlayer dielectric material layer.

9. The method of claim 8, wherein forming the first interlayer dielectric material layer
20 comprises depositing the first interlayer dielectric material layer with a spin-on coating technique.

10. The method of claim 8, further including forming an adhesion liner adjacent the source/drain region and adjacent at least one gate spacer, prior to forming the first interlayer
25 dielectric material layer.

11. The method of claim 8, wherein oxidizing the first interlayer dielectric material layer comprises heating the first interlayer dielectric material layer in a steam atmosphere.

30 12. The method of claim 11, wherein heating the first interlayer dielectric material layer in a steam atmosphere comprises heating the first interlayer dielectric material layer to a temperature of about 410 degrees Celsius in about a 93% steam atmosphere for about 2 hours.

13. The method of claim 8, wherein annealing the first interlayer dielectric material layer
35 comprises annealing the first interlayer dielectric material layer with high density plasma in an

inert atmosphere.

14. The method of claim 8, further including planarizing the first interlayer dielectric material layer.

5

15. The method of claim 8, further including forming a contact through the at least one dielectric material to contact at least a portion of the source/drain region.

16. The method of claim 8, wherein oxidizing and annealing the first interlayer dielectric material layer shrinks the first interlayer dielectric material layer to exert a tensile strain on the source/drain region.

17. A microelectronic transistor, comprising:
a transistor gate including a gate electrode formed adjacent a substrate and a pair of gate spacers disposed on opposing sides of the gate electrode;
a source/drain region adjacent the transistor gate; and
a first interlayer dielectric material layer formed adjacent the substrate, adjacent the source/drain region, and adjacent at least one gate spacer, wherein the first interlayer dielectric material layer includes a densified portion formed proximate a first surface of the first interlayer dielectric material layer.

18. The microelectronic transistor of claim 17, wherein the transistor gate is non-planar.

19. The microelectronic transistor of claim 17, wherein the source/drain region is non-planar.

25

20. The microelectronic transistor of claim 17, further including a capping dielectric structure disposed adjacent the non-planar gate electrode and between the pair of gate spacers.

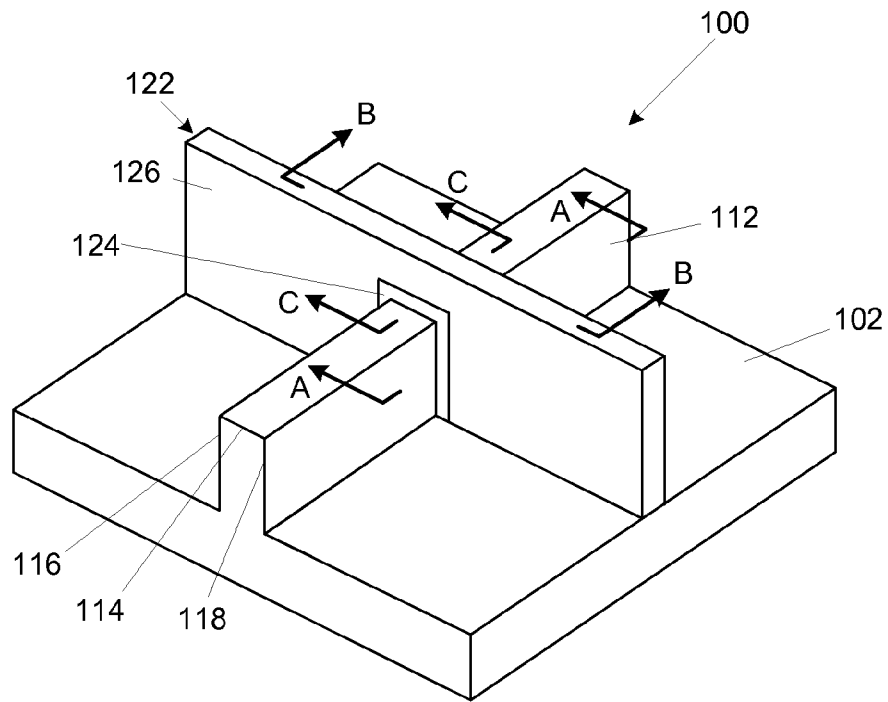


FIG. 1

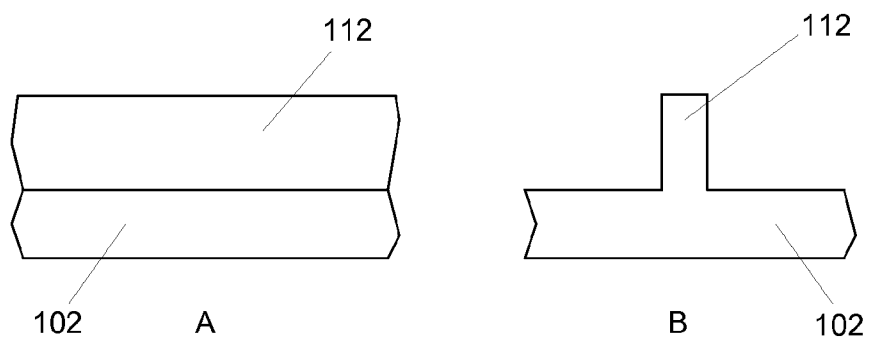


FIG. 2

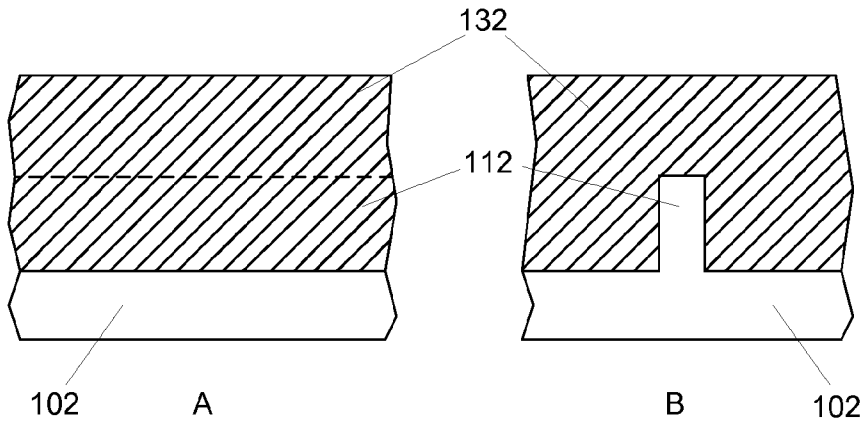


FIG. 3

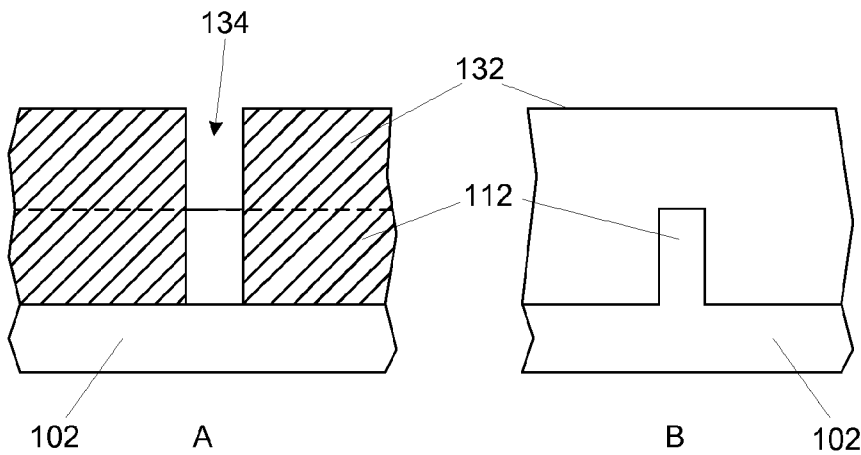


FIG. 4

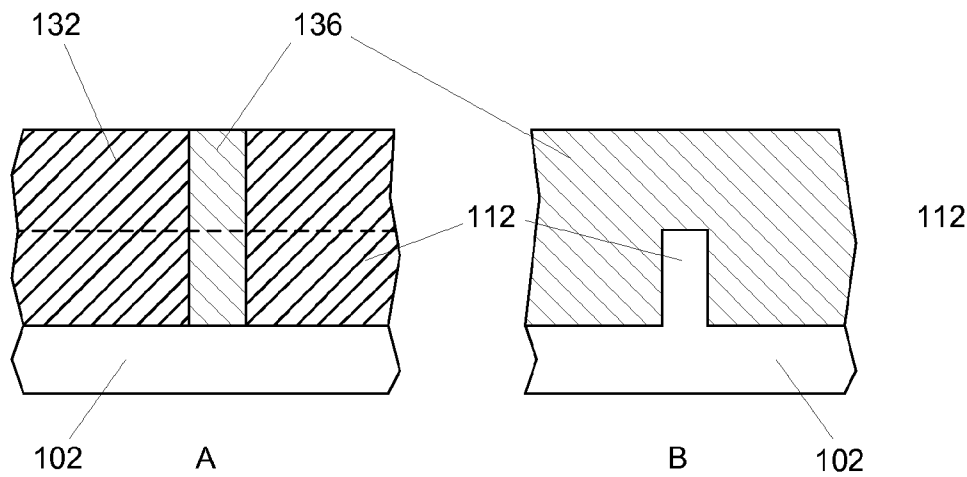


FIG. 5

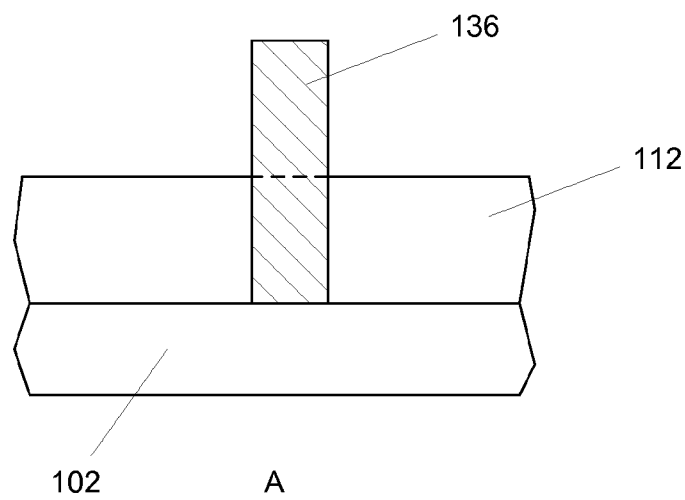


FIG. 6

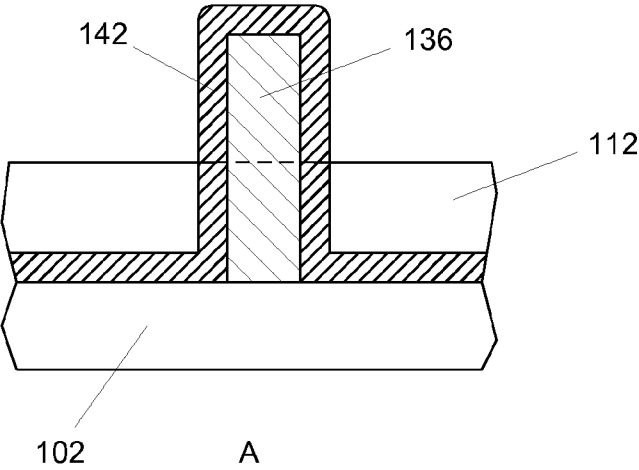


FIG. 7

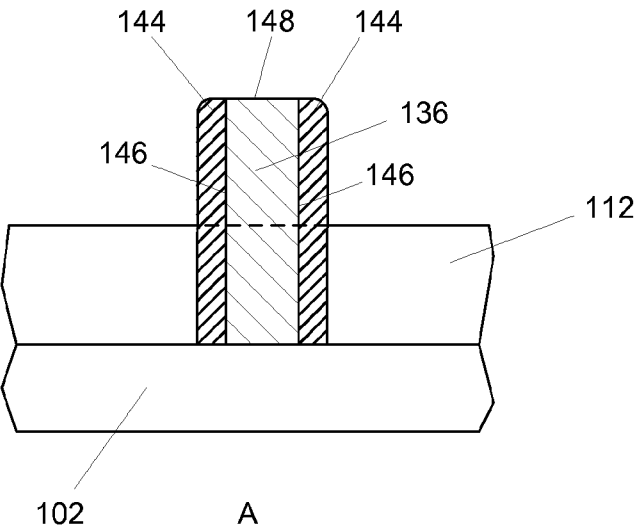


FIG. 8

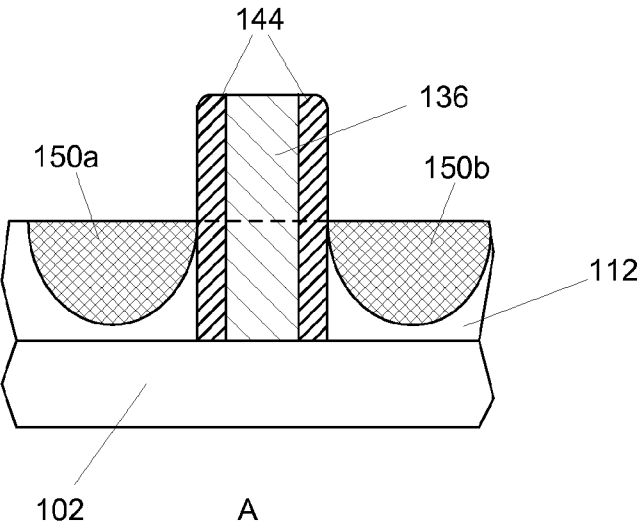


FIG. 9

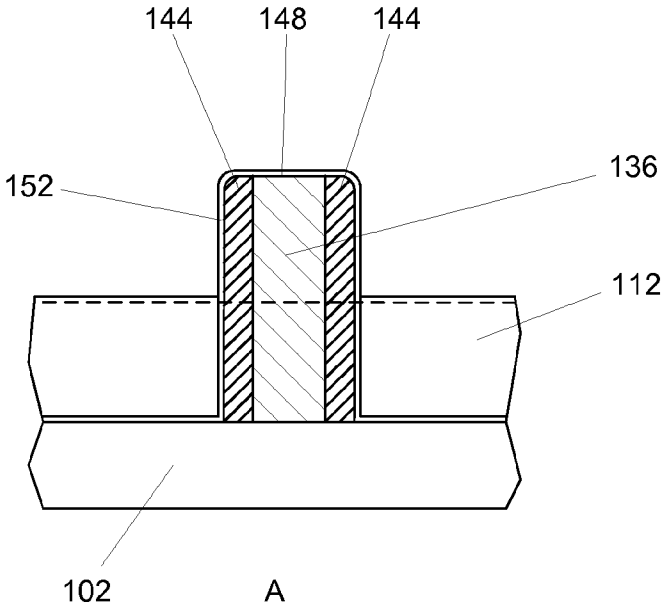


FIG. 10

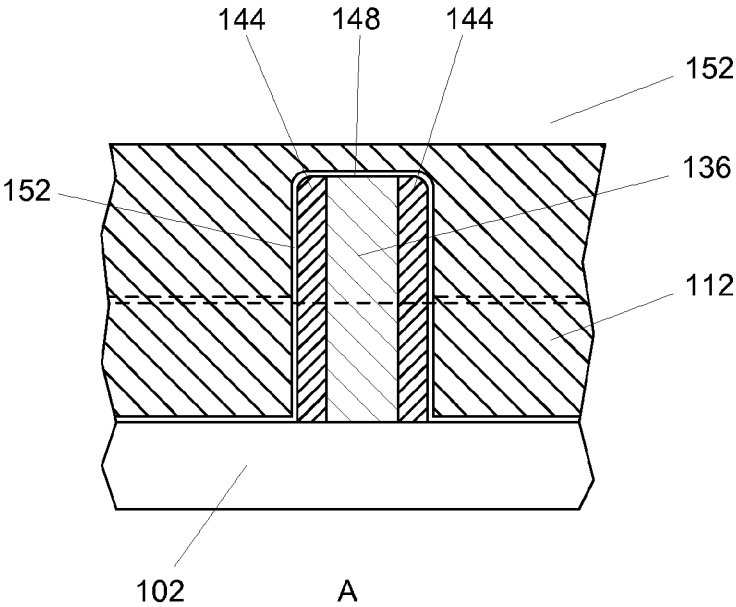


FIG. 11

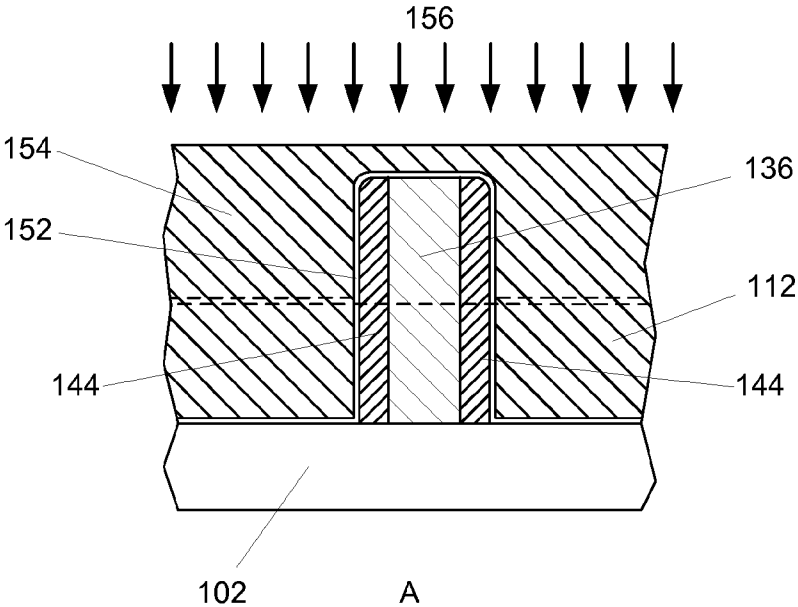


FIG. 12

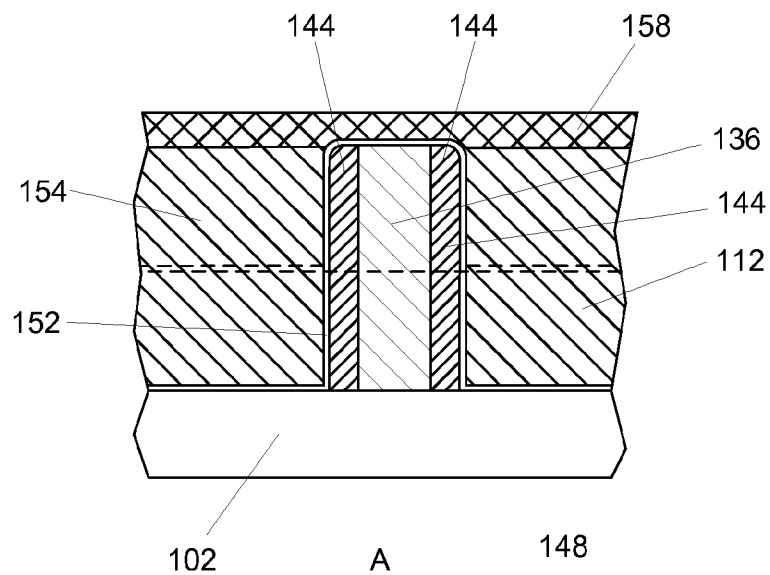


FIG. 13

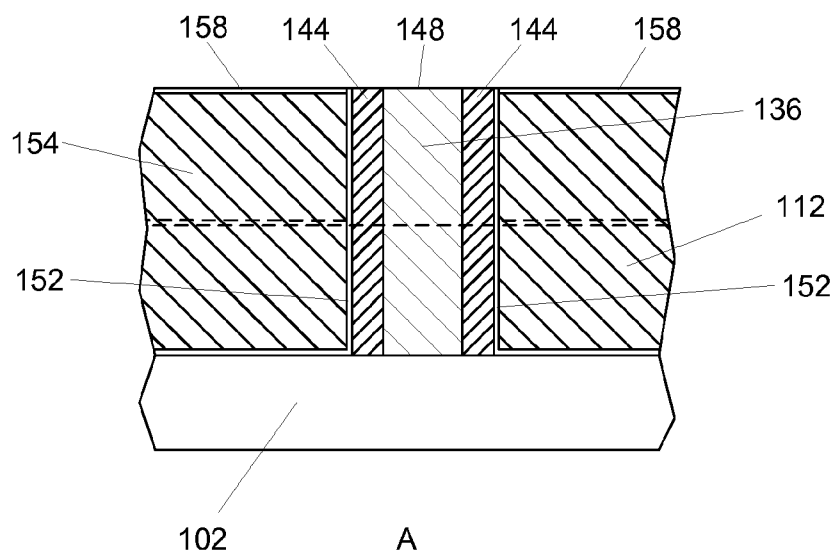


FIG. 14

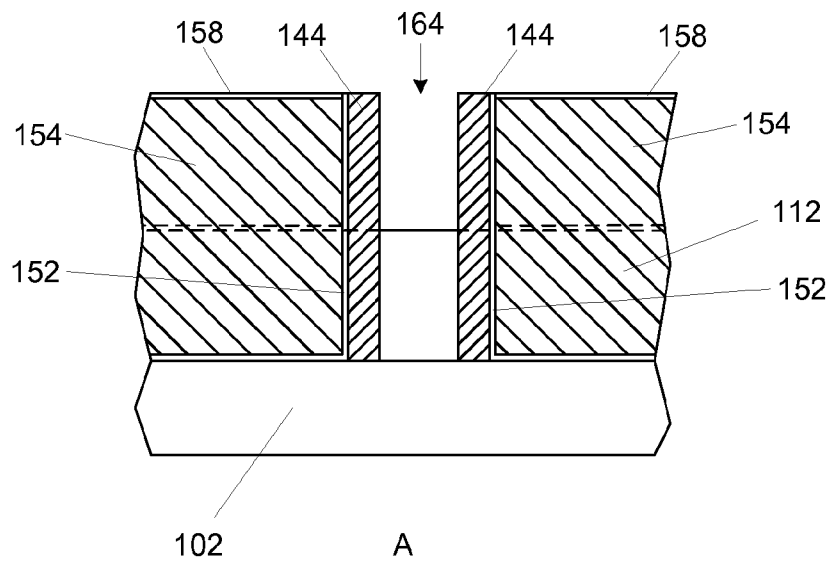


FIG. 15

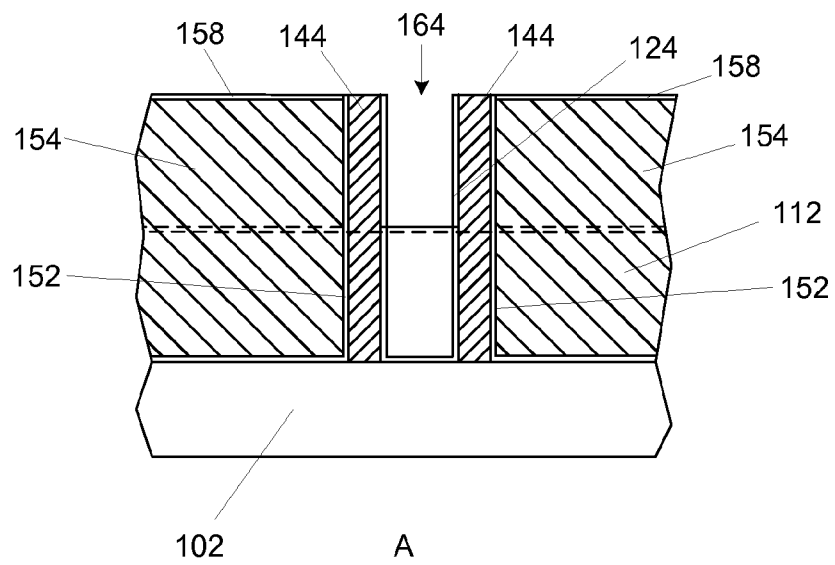


FIG. 16

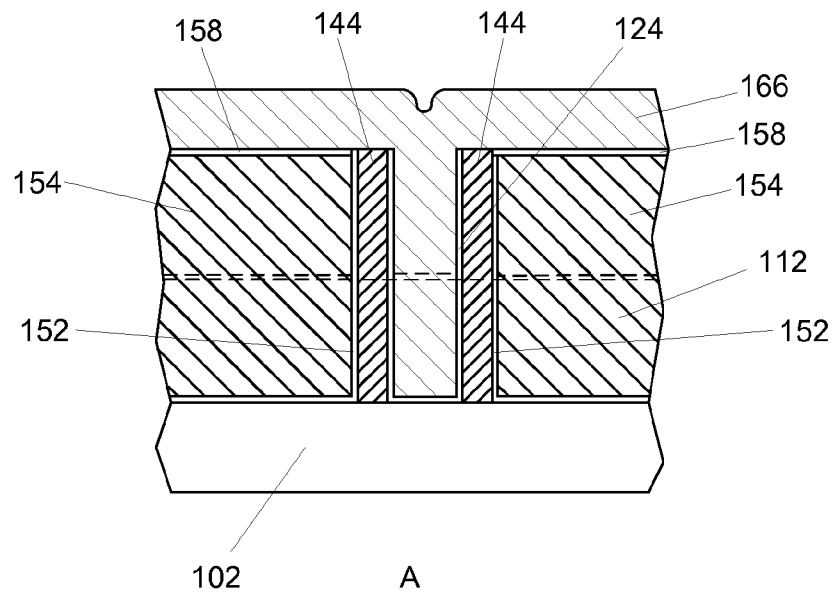


FIG. 17

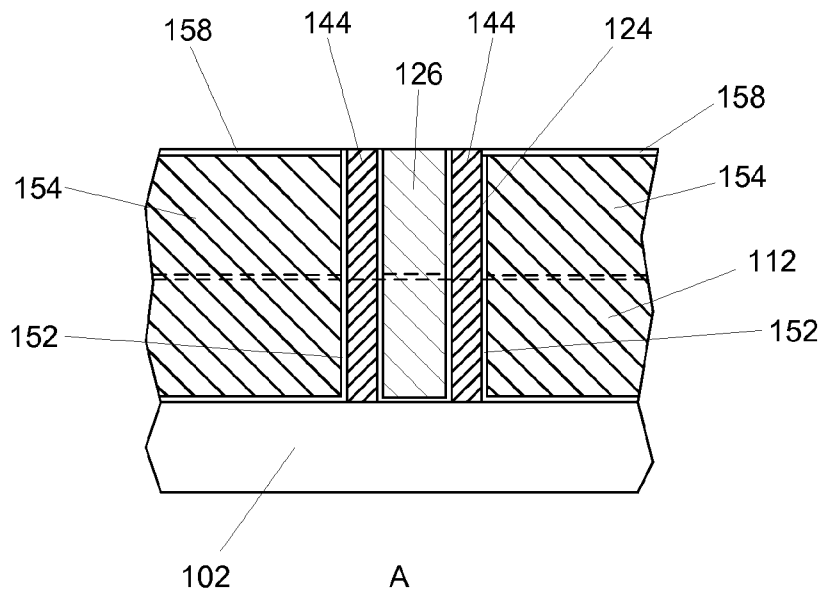


FIG. 18

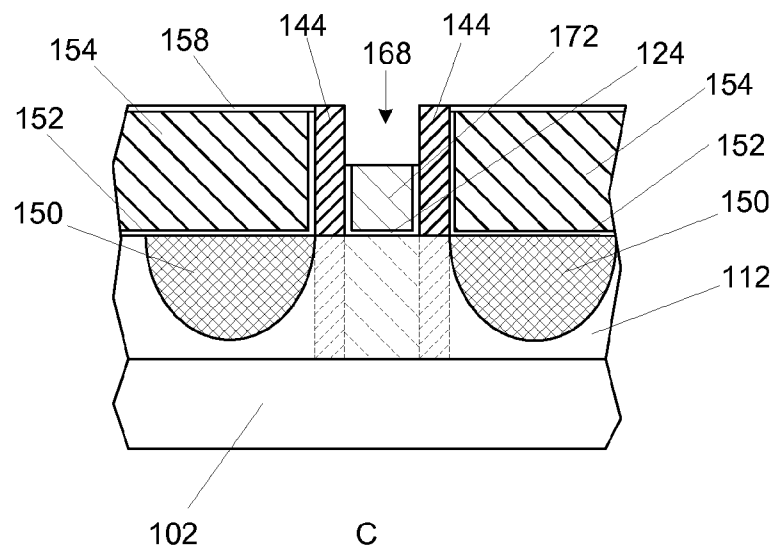


FIG. 19

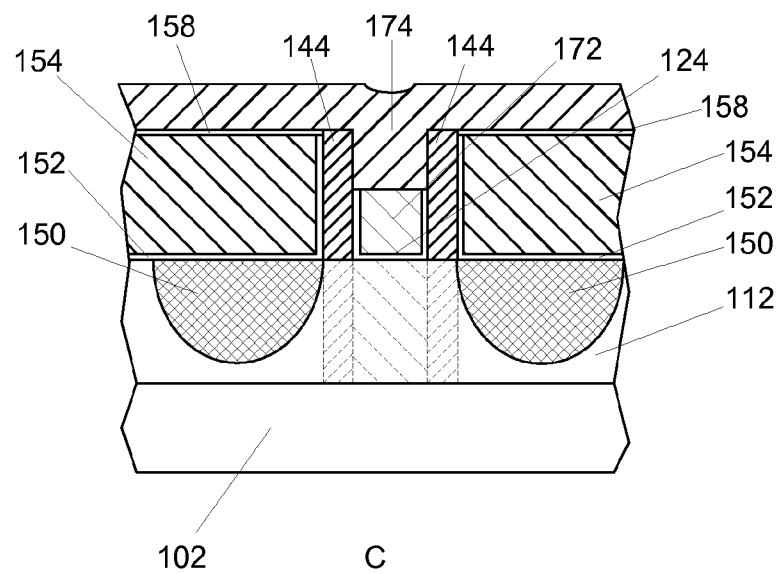


FIG. 20

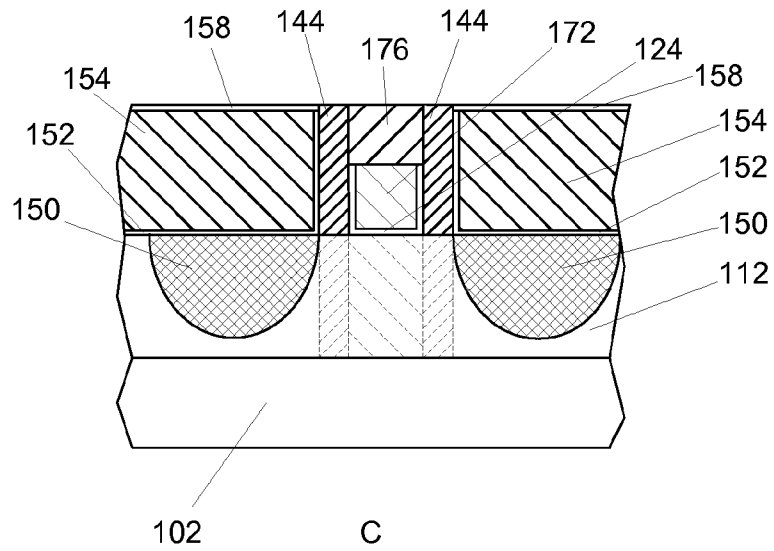


FIG. 21

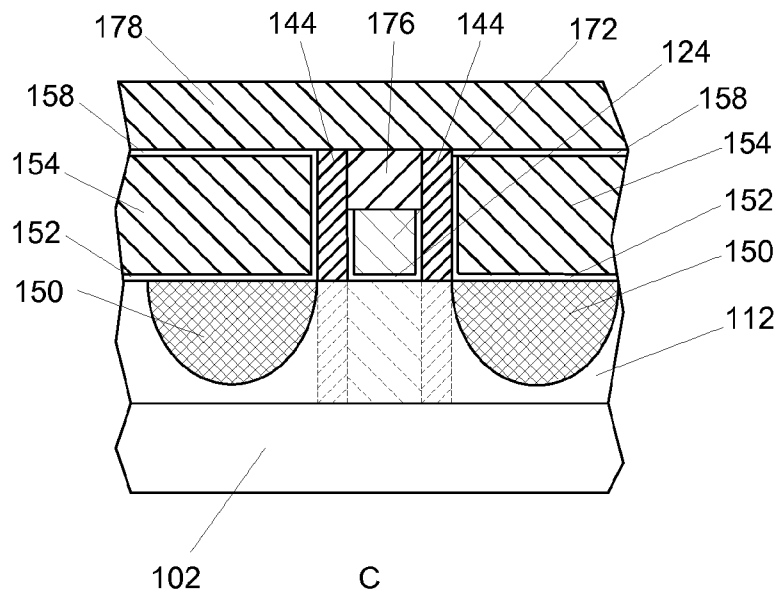


FIG. 22

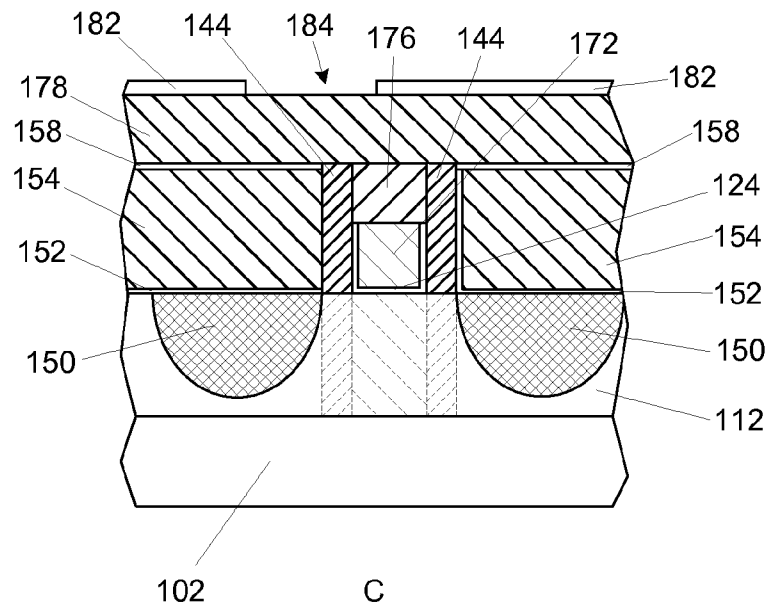


FIG. 23

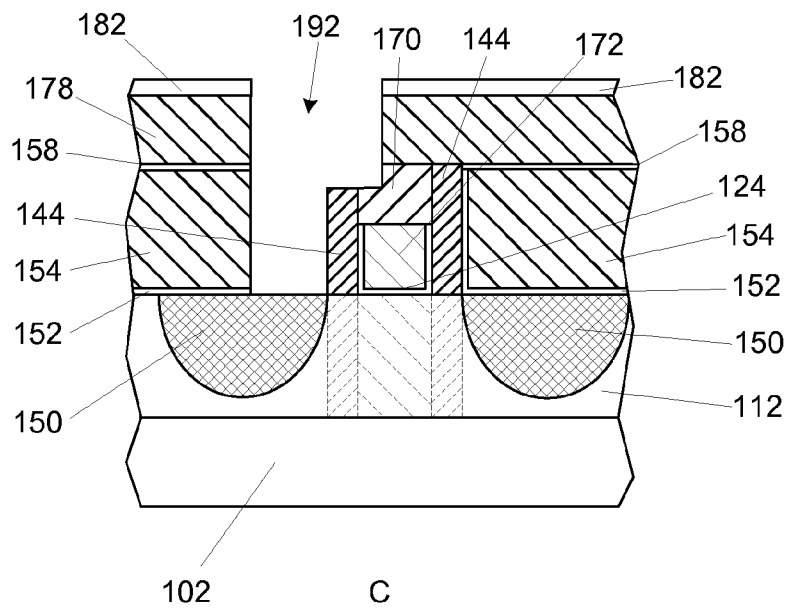


FIG. 24

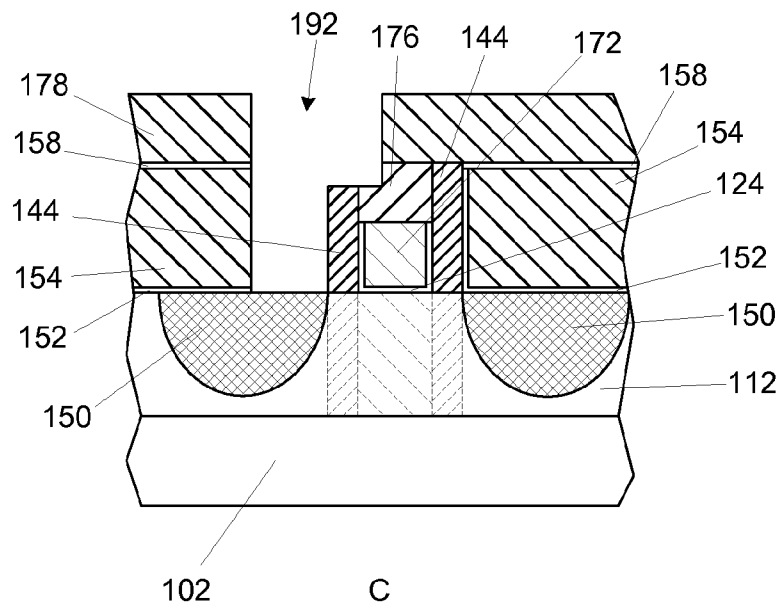


FIG. 25

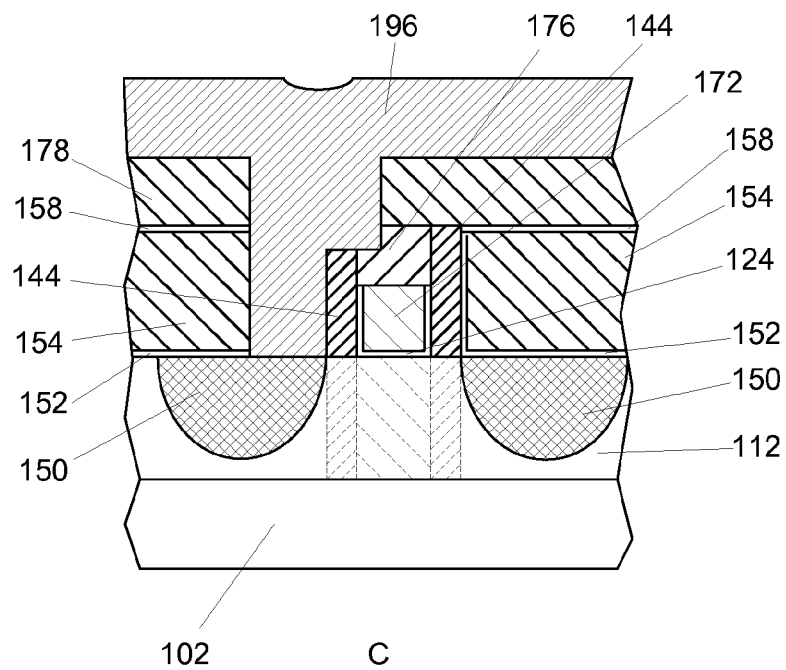


FIG. 26

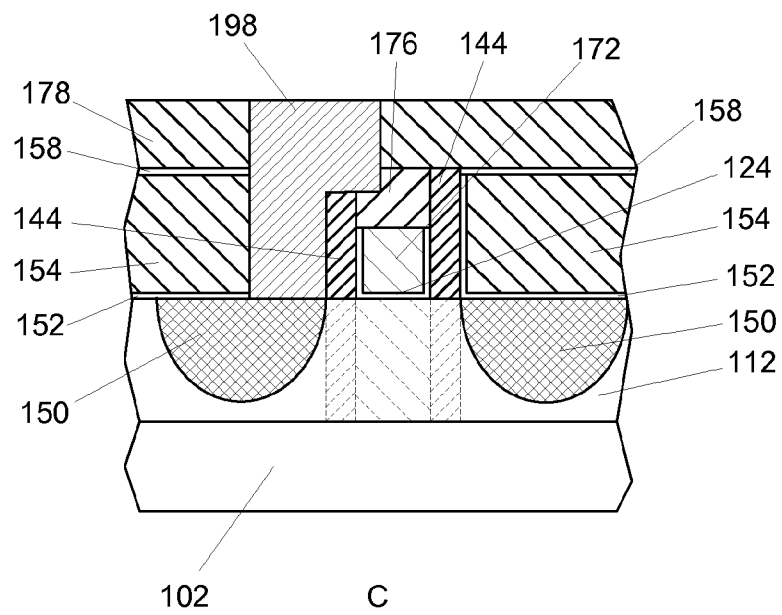


FIG. 27

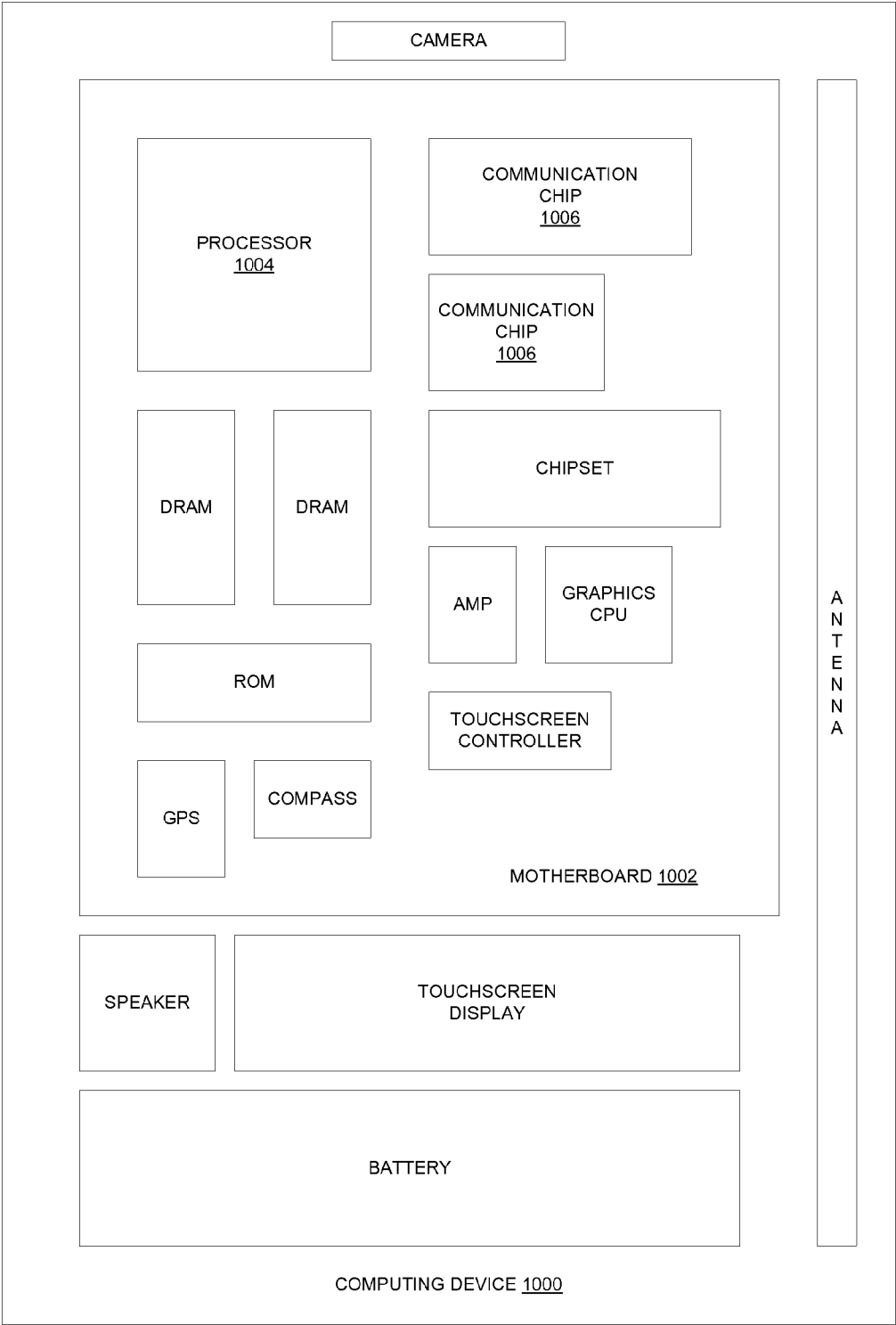


FIG. 28

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US20 11/063433**A. CLASSIFICATION OF SUBJECT MATTER****HOIL 21/336(2006.01)i, HOIL 29/78(2006.01)1, HOIL 21/31(2006.01)1**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 21/336; HOIL 21/8234; HOIL 29/76; HOIL 27/1 1; HOIL 21/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: gate, dielectric, spacer, interlayer, oxidizing, annealing, tensile, electrode, capping, trench, non-planar.**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2004-0050519 A (HYNIX SEMICONDUCTOR CO., LTD.) 16 June 2004 See abstract, page 3, claim 1 and figures 1a-1d.	1-20
A	US 2002-0130372 A1 (HYUNG-SHIN KWON et al.) 19 September 2002 See abstract, paragraphs [0026] -[0028], [0031M0037] and figures 10-12.	1-20
A	KR 10-2008-0021918 A (DONGBU ELECTRONICS CO., LTD.) 10 March 2008 See abstract, paragraphs [0042] -[0065], claims 1,3 and figures 3a-3j.	1-20
A	US 2006-0189058 A1 (JONG-WOOK LEE et al.) 24 August 2006 See abstract, paragraphs [0049] -[0086] and figures 7-15.	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

19 JULY 2012 (19.07.2012)

Date of mailing of the international search report

20 JULY 2012 (20.07.2012)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Jung Jin

Telephone No. 82-42-481-5962



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/063433

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2004-00505 19 A	16 .06 .2004	None	
US 2002-0130372 A 1	19 .09 .2002	KR 10-0399357 B1	26. 09 .2003
		US 2004-0198032 A1	07. 10 .2004
		US 2007-0290280 A1	20. 12 .2007
		US 2007-0293030 A1	20. 12 .2007
		US 6767814 B2	27. 07 .2004
		US 7385260 B2	10. 06 .2008
KR 10-2008-002 19 18 A	10 .03 .2008	None	
US 2006-0189058 A 1	24. 08 .2006	KR 10-05788 18 B1	11.05 .2006
		US 7442596 B2	28. 10 .2008